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2020-02-06 Technical information

- **Contract status feat. Lena**
- **Additional documentation**
- **Topics related to the Up- / Downconversion stages**
- **Questions and their answers**
- **IQ mixing concept introduction**

Christian Križan
Research engineer, QTL
krizan@chalmers.se

Contract status

Added content since last time

- General notes on development and testing procedures
  - Hints on testing, development suggestions, the minimal system
- Updates in the module descriptive document from last lecture
- (Student contract)
- Datasheets
  - Target platform ADC/DAC
  - The PHY chip on the Nexys 4
- As usual, lecture slides with additional notes

IF, FIFO and IQ frequencies

IF, FIFO and IQ frequencies

- Clocking FIFOs at 100 MHz was insufficient in Mats' earlier experiments.
- Meaning that you should aim for a design which would allow for the maximum IF frequency if possible.

… see next slide

Table 26: **IO_FIFO Switching Characteristics**

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1Q/-1M	-1LI	-2LE	
IO_FIFO Clock to Out Delays								
T_{OFFCKO_DO}	RDCLK to Q outputs	0.55	0.60	0.68	0.68	0.68	0.81	ns
T_{CKO_FLAGS}	Clock to IO_FIFO flags	0.55	0.61	0.77	0.77	0.77	0.79	ns
Setup/Hold								
T_{CCK_D}/T_{CKC_D}	D inputs to WRCLK	0.47/0.02	0.51/0.02	0.58/0.02	0.58/0.18	0.58/0.02	0.76/0.09	ns
$T_{IFFCCK\_WREN}/T_{IFFCKC\_WREN}$	WREN to WRCLK	0.42/–0.01	0.47/–0.01	0.53/–0.01	0.53/–0.01	0.53/–0.01	0.70/–0.05	ns
$T_{OFFCCK\_RDEN}/T_{OFFCKC\_RDEN}$	RDEN to RDCLK	0.53/0.02	0.58/0.02	0.66/0.02	0.66/0.02	0.66/0.02	0.79/–0.02	ns
Minimum Pulse Width								
$T_{PWH\_IO\_FIFO}$	RESET, RDCLK, WRCLK	1.62	2.15	2.15	2.15	2.15	2.15	ns
$T_{PWL\_IO\_FIFO}$	RESET, RDCLK, WRCLK	1.62	2.15	2.15	2.15	2.15	2.15	ns
Maximum Frequency								
F_{MAX}	RDCLK and WRCLK	266.67	200.0	200.00	200.00	200.00	200.00	MHz

IF, FIFO and IQ frequencies

- Clocking FIFOs at 100 MHz was insufficient in Mats' earlier experiments.
- Meaning that you should aim for a design which would allow for the maximum IF frequency if possible.
- … given that nothing breaks, such as insufficient space constraints.
- Remember:
  Implementations relying solely on a single fixed clock frequency tend to cut corners,
  and generally end up being hard to work with in the end.

  Make your design sufficiently generic without relying on the clock rate.

More on IF, FIFO and IQ frequencies

- The target platform maximum FIFO clock rate is 500 MHz (516 actually).
- Scaling down with the same ratio (500/200), a fictitious development board ADC/DAC should input/output at 4000/2.5 = 1600 MSa/s.
- Meaning:
  Your IF stream rate should be 100 MHz.
  Your IQ mixers should up/downconvert with a factor of 2.
  With eight parallel samples – we achieve an effective sample throughput of 1.6 GSa/s.

  Not bad for a 100 MHz main system clock.

200 MHz?

- But wait, the main system clock is 100 MHz?
- You will have to use tricks from IP cores, such as the MMCM (Mixed-Mode Clock Manager) including PLL. Clock multipliers are definitely a thing, especially in digital radio applications.

  Spoiler below (copy-paste whitetext to see):

- Just for additional reference, the 100 MHz clock rate will also scale with a factor 2.5 on the target FPGA platform. Meaning that the target board will run its stream controller FIFOs at 250 MHz.

By the way


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The Nexys4 board is a complete, ready-to-use digital circuit development platform based on the latest Artix-7™ Field Programmable Gate Array (FPGA) from Xilinx. With its large, high-capacity FPGA (Xilinx part number XC7A100T-1CSG324C), generous external memories, and collection of USB, Ethernet, and other ports, the Nexys4 can host designs ranging from introductory combinational circuits to powerful embedded processors. Several built-in peripherals, including an accelerometer, temperature sensor, MEMs digital microphone, speaker amplifier and lots of I/O devices allow the Nexys4 to be used for a wide range of designs without needing any other components.
The Artix-7 FPGA is optimized for high performance logic, and offers more capacity, higher performance, and more resources than earlier designs. Artix-7 100T features include:
15,850 logic slices, each with four 6-input LUTs and 8 flip-flops
4,860 Kbits of fast block RAM
Six clock management tiles, each with phase-locked loop (PLL)
240 DSP slices
Internal clock speeds exceeding 450MHz
On-chip analog-to-digital converter (XADC)
The Nexys4 also offers an improved collection of ports and peripherals, including:
16 user switches
USB-UART Bridge
12-bit VGA output
3-axis accelerometer
16Mbyte CellularRAM
Pmod for XADC signals
16 user LEDs
Two tri-color LEDs
PWM audio output
Temperature sensor
Serial Flash
Digilent USB-JTAG port for FPGA programming and communication
Two 4-digit 7-segment displays
Micro SD card connector
PDM microphone
10/100 Ethernet PHY
Four Pmod ports
USB HID Host for mice, keyboards and memory sticks

Let’s talk about filters

Filters

- You'll notice that a lot of places in your DSP design benefit from filtering.
- NCO's, mixers and filter tap memories can quickly consume a lot of LUTs. Since your design will contain a heavy amount of asynchronous parallelisation, using the large amount of available BRAM on the Nexys 4 might prove impossible.
- *"A design based on interpolation + FIR + mixer is not normal in the business. You should look into CIC."*

  - Mats
- CIC filters will droop in the passband. Meaning that, if you go with CIC filtering, you'll typically need an impulse response filter afterwards. Yet, IRL, the operator could theoretically plug in a compensator in the signal generator and compensate before the signal even enters your system.
- But the take-home message is:

  The quality of your filters will depend on your implementation, and is a typical metric that your group will try to engineer as optimal as possible.

  Besides, the engineering choices here constitute pretty good stuff for your report.

Filters cont.

- *OK. So what do I plug into t-filter?* [1]

  I would start with a very flat passband at 0.1 dB ripple and -30 dB noise suppression.

  This we know yields rather decent filters on the Nexys 4 hardware.

[1] http://t-filter.engineerjs.com

Answers to questions

Vivado IP blocks are 100% OK

Provided you did not buy them for this project yourselves.

Questions and answers

- *Should we package the outgoing data to the host PC as UDP also?*

  Yes please, this would make it easier.

- *Does the Central stream controller also ask the host PC for data when its memory is not full?*

  ***"*This is a good point. Yes, it should." This means that, if there is no incoming data into the DRAM, and the DRAM can accept additional packages, then the Central stream controller should poll the Ethernet communications module to ask the host PC for more data.**

- *On the topic of the skip / store block:*

  There may be advantages in the downconversion path gained by setting the skip / store block directly after the ADC input. If your memory is sufficient, you sure could try.

More answers

- **I should clarify that the QPU core is a passive device.**
  An RF signal goes in, a modified RF signal goes out.

  There are no mixers in the signal path leading to/from the core after your interface device.
  There are 12 GHz LP filters, circulators, and attenuator-amplifier pairs at best.

  The qubits themselves act as frequency-dependent C-LC filters.
  See my thesis on Canvas for details.

- **You should not have to squash spurious contaminants in the output of the IQ mixer, by for instance applying a bandpass filter.**

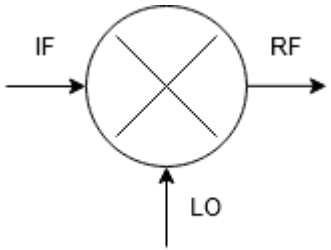
  Harmful spurs similar to LO-leakage spikes, are IRL squashed by the operator by calibrating the amplitude and phase of the NCO's.

IQ mixing

Let’s start with just mixing

- Mixers, analogue or digital, are used for blending two incoming signals – producing signals at new output frequencies. They receive some frequency band content, and put said content at some other frequency band. Frequency converters, if you may.

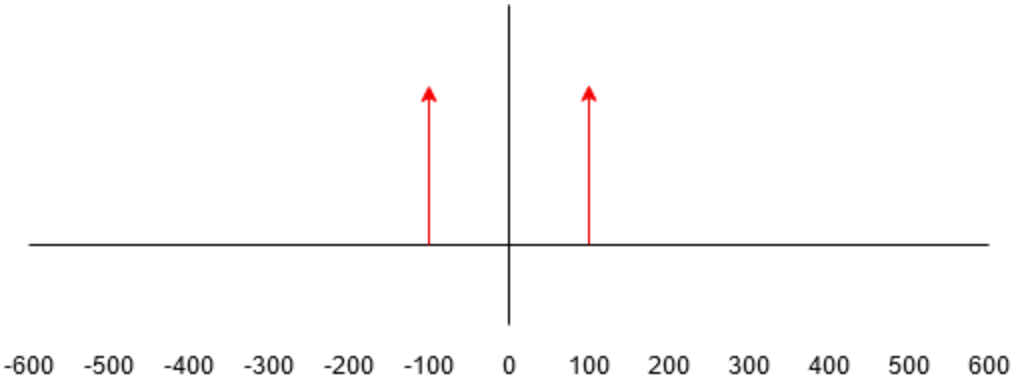
A key component in all of radio technology, invented almost 120 years ago.



The mixed output of f_{IF} and f_{LO} yields two new signals. We’ll combine these and call them f_{RF}.

$$f_{RF} = [f_{IF}+f_{LO}] + [f_{IF}+f_{LO}]$$

Some real content



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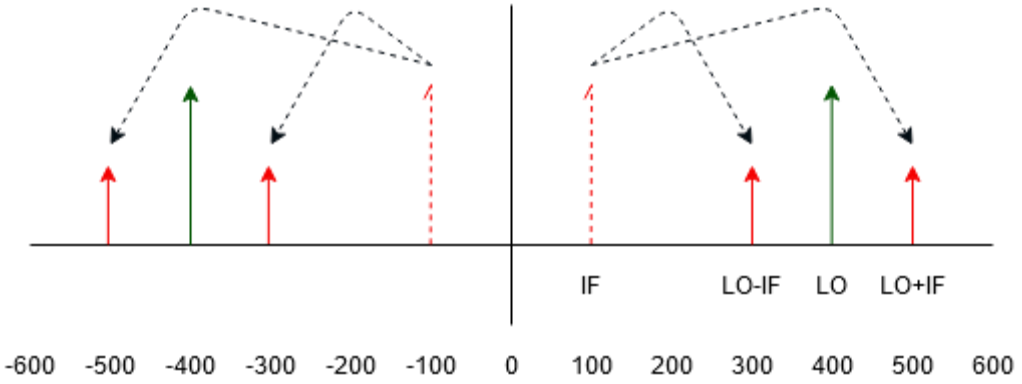
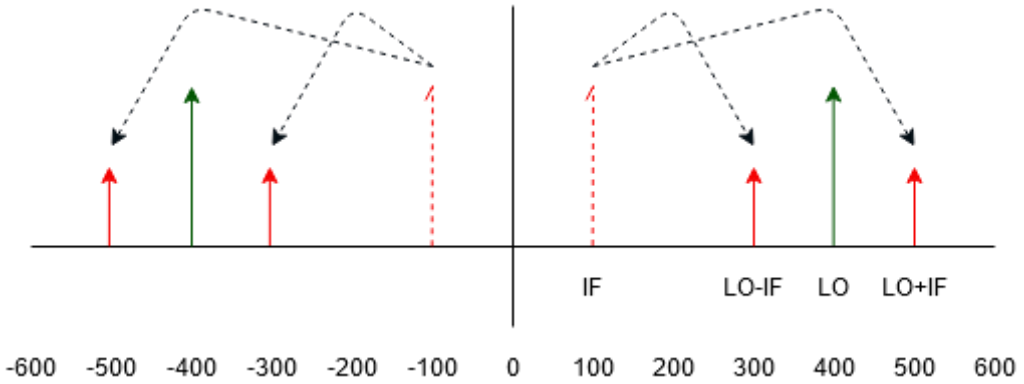




$$\cos\omega_1 \cos\omega_2 = \frac{\cos(\omega_1 + \omega_2)}{2} + \frac{\cos(\omega_1 - \omega_2)}{2}$$

So a mixer is just a multiplication?

In the digital domain, yes.

What is the deal about IQ then?

- In phase and quadrature components, ie. one original signal ω_I and its 90° phase-shifted copy ω_Q, allow for breaking the Y-axis symmetry.

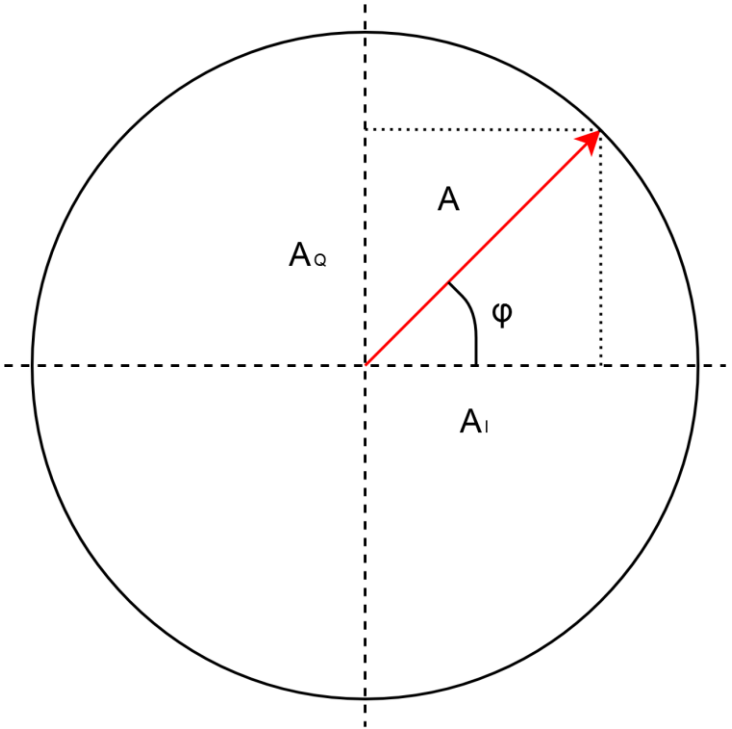
- You'll likely se literature calling this 'complex mixing' – since we are rather equivalently operating in the complex plane. The resulting signals are also known as complex signals.

- The signal is only complex because you observe both I and Q together.
  On their own, they are still very real signals.

- … and if you were to probe a multimeter to an output bearing the summation of I and Q, you'd still see Y-axis symmetric frequency content. The signal is real, after all.

IQ by vector diagram

- The amplitude of the Q-component in a way represents the imaginary axis, while the I-component represents the real.
- | ”I + Q” | is thus the amplitude of A, while the phase of ”I+Q” is φ



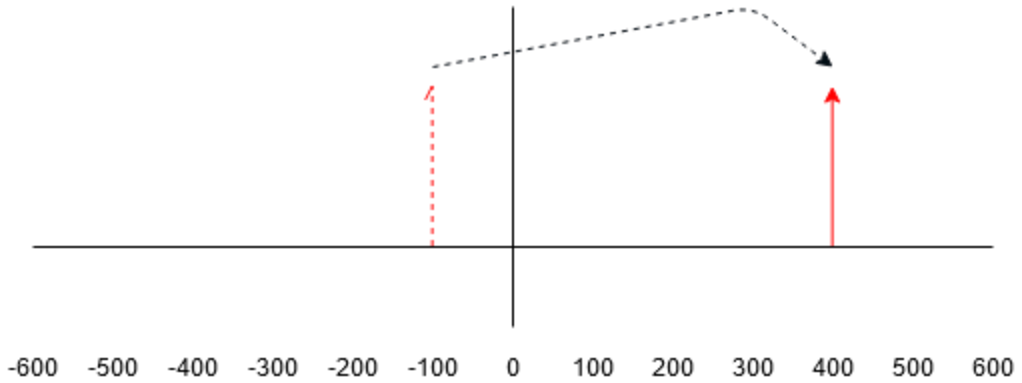
The point

We may use the complex plane to describe any signal

And why should we use it?

- Every data sample contains the I and Q part of the target signal. By operating in the complex plain, the operator may easily specify some content at only -300 kHz or similar.

- An IQ mixer allows for moving this single spike to some target frequency, without generating conflicting spurs.



With this basic idea, go wild

There are hundreds of IQ tutorials online.

Some final notes on interpolation, filtering, mixing

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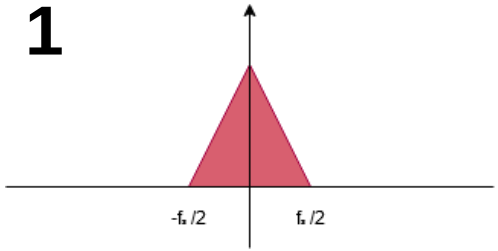

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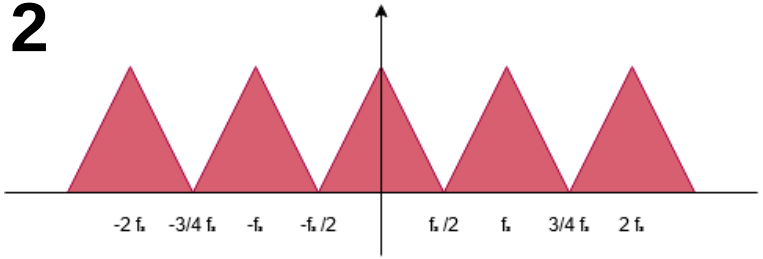

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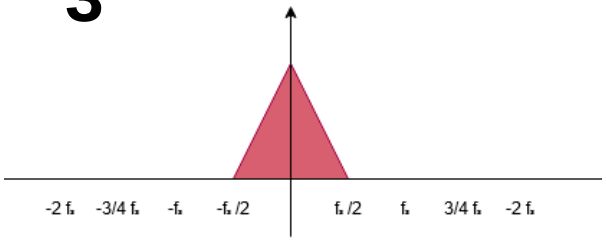

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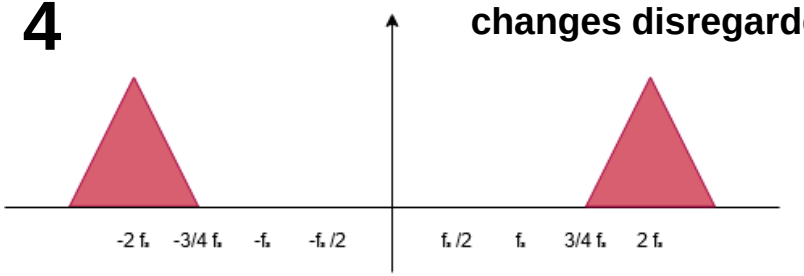

NOTE: amplitude changes disregarded

Open-class questions

My mailbox is open: krizan@chalmers.se

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