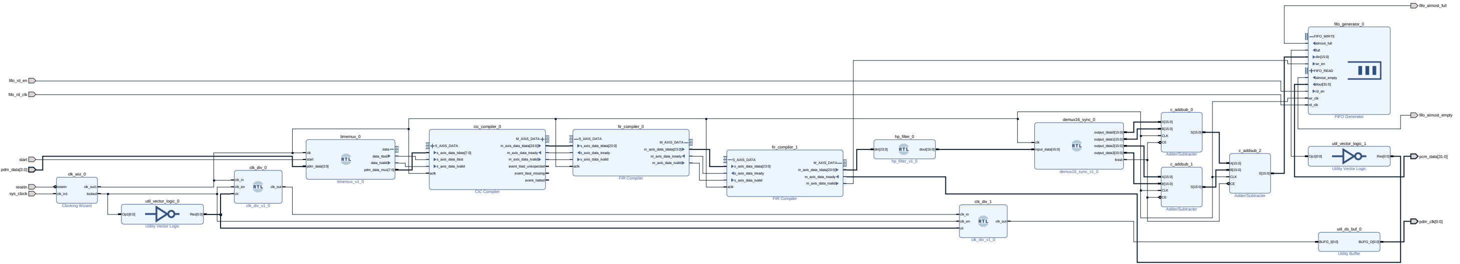
fifo_rd_en
fifo_rd_clk
start
pdm_data[3:0]
resetn
sys_clock
clk_wiz_0
resetn
clk_in1
clk_out1
locked
Clocking Wizard
util_vector_logic_0
Op1[0:0]
Res[0:0]
Utility Vector Logic
clk_div_0
clk_in
clk_en
clr
clk_out
RTL
clk_div_v1_0
timemux_0
clk
start
pdm_data[3:0]
RTL
data
data_tlast
data_tvalid
pdm_data_mux[7:0]
timemux_v1_0
cic_compiler_0
S_AXIS_DATA
s_axis_data_tdata[7:0]
s_axis_data_tlast
s_axis_data_tvalid
aclk
M_AXIS_DATA
m_axis_data_tdata[23:0]
m_axis_data_tready
m_axis_data_tvalid
event_tlast_unexpected
event_tlast_missing
event_halted
CIC Compiler
fir_compiler_0
S_AXIS_DATA
s_axis_data_tdata[23:0]
s_axis_data_tready
s_axis_data_tvalid
aclk
M_AXIS_DATA
m_axis_data_tdata[23:0]
m_axis_data_tready
m_axis_data_tvalid
FIR Compiler
fir_compiler_1
S_AXIS_DATA
s_axis_data_tdata[23:0]
s_axis_data_tready
s_axis_data_tvalid
aclk
M_AXIS_DATA
m_axis_data_tdata[23:0]
m_axis_data_tready
m_axis_data_tvalid
FIR Compiler
hp_filter_0
din[23:0]
RTL
dout[15:0]
hp_filter_v1_0
clk_div_1
clk_in
clk_en
clr
RTL
clk_out
clk_div_v1_0
demux16_sync_0
clk
input_data[15:0]
RTL
output_data0[15:0]
output_data1[15:0]
output_data2[15:0]
output_data3[15:0]
finish
demux16_sync_v1_0
c_addsub_0
A[15:0]
B[15:0]
CLK
CE
S[15:0]
Adder/Subtracter
c_addsub_1
A[15:0]
B[15:0]
CLK
CE
S[15:0]
Adder/Subtracter
c_addsub_2
A[15:0]
B[15:0]
CLK
CE
S[15:0]
Adder/Subtracter
fifo_generator_0
FIFO_WRITE
almost_full
full
din[15:0]
wr_en
FIFO_READ
almost_empty
dout[31:0]
rd_en
wr_clk
rd_clk
FIFO Generator
util_vector_logic_1
Op1[0:0]
Res[0:0]
Utility Vector Logic
util_ds_buf_0
BUFG_I[0:0]
BUFG_O[0:0]
Utility Buffer
fifo_almost_full
fifo_almost_empty
pcm_data[31:0]
pdm_clk[0:0]