Written examination for

MCC092 Introduction to Integrated Circuit Design

Saturday October 29, 2016, at 8.30-13.30 at SB building

Staff on duty: Lena Peterson, D&IT, phone ext: 1822, or mobile 0706-268907.

Lena will visit around 9.30 and 12.00.

Administration: Send exams to Lena Peterson D&IT, and send lists to CSE student administration office.

Allowed technical aids for students: This is a closed-book exam. Allowed aids: A Chalmers-allowed calculator (non graph-drawing) plus pencil, eraser, ruler, and dictionary (these are always allowed).

The results from the examination will be sent to you via the Ladok system within three weeks. The grading reviews will take place:

Monday November 14 2016, 12:15-13:15 in room 4128

Tuesday November 15 2016 same time and place.

Solutions: will be posted on the course web site in PingPong no later than Monday October 31. Any student who does not have access to the 2016 course web site can contact Lena Peterson (via e-mail to lenap@chalmers.se) to obtain the solution.

Instructions:

Write legibly.

State any assumptions you make.

Partial credits can be awarded but requires that you **explain** your reasoning and calculations.

Number all pages and write your code on each page.

Put only one problem per page.

Good luck!

Grades:

The written examination contains six problems, each worth 10 points. You need 30 points to pass (grade "3"), at least 40 points for grade "4" and at least 50 points for grade "5". Bonus points from the fall 2016 course instance will be added before the higher grades are assigned.

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1. **Power consumption, delay** Circuit performance optimization is crucial in high-performance circuit design. In this problem, we consider the impact of three important transistor and process parameters. They are:

   Supply voltage, V_{DD}
   Transistor widths, W
   Transistor threshold voltages, $|V_T|$

   Consider one well-designed CMOS inverter (inverter 1), the output of which is connected to the inputs of four identical inverters. Your task is to optimize its power consumption and delay by changing these three parameters. You have three options for your answer for each parameter: **Increase, Decrease** or **No impact**. When a parameter is changed it impacts all five inverters similarly. You may assume that the input signal to inverter 1 has similar rise and fall times as does its output and that the quadratic MOS-transistor current equations hold.

   The four optimization cases are:

   a) Minimize the **switching power consumption** of inverter 1.
   b) Minimize the **short-circuit power consumption** of inverter 1.
   c) Minimize the **FO4 propagation delay** of inverter 1.
   d) Minimize the **static power consumption due to subthreshold leakage** of inverter 1.

   No motivation is required, but is allowed if you want to include it. Summarize your answer in the form of a table like this one:

	V_{DD}	W	$\|V_T\|$
Case a)			
Case b)			
Case c)			
Case d)			

(10 p is given for a completely correct solution - one point is deducted for each wrong or missing answer)

2. **Logical functions, layout** Below you see the Cadence schematic for a four-input gate from the cell library for the 65-nm process we have used in the course.

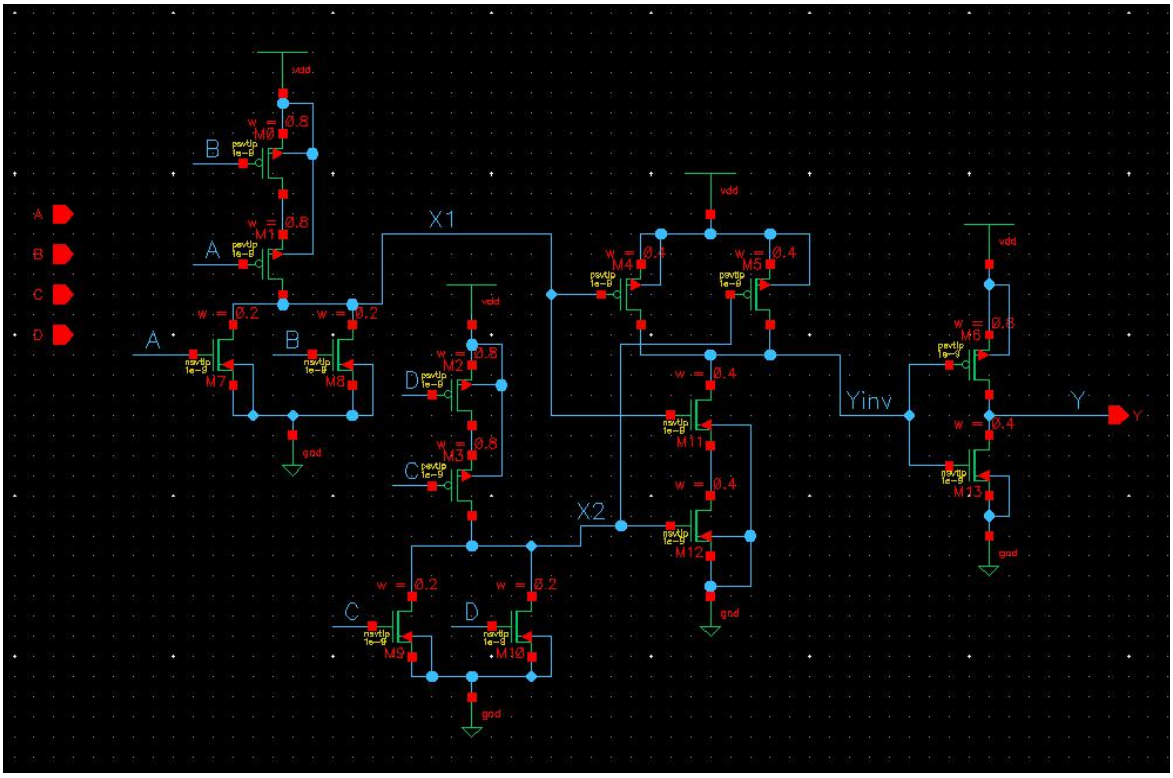


Figure 1: The schematic of a 4-input gate from the 65-nm cell library.

a) What is the logic function of the gate? (2 p)

b) Draw a schematic for **one** compound gate that implements the function you arrived at in a). (1 p)

c) Draw the layout for the schematic given above in the template below. Use shared diffusion areas at gate output nodes whenever possible. The template is repeated twice in larger scale at the end of the exam so you can tear it off and hand it in with your solutions. (5 p)

d) Give **two** reasons for why it may be good idea to implement this logic function as shown in Figure 1 rather than the with one you drew in task b). (2 p)

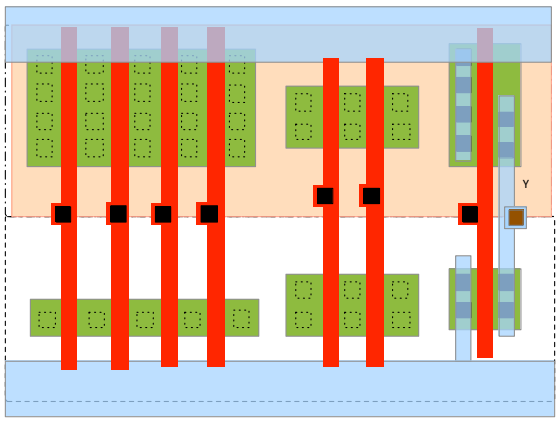


Figure 2: Layout template for task 2.c. Use the larger copy at the end of the exam.

3. Logical effort, gate sizing Again consider the schematic shown in Figure 1 above.

a) Derive values for the intrinsic delay, p, and the logical effort, g, for the **entire** cell, the schematic of which is shown in Figure 1, with the transistor sizes shown in the schematic. (5 p)

b) Assume that the cell from Figure 1 is to be scaled for optimal delay when loaded with a capacitance of $28.8\ C_{in}$ or $\frac{144}{5} C_{in}$ where C_{in} is the input capacitance for each of the inputs A, B, C, D in Figure 1. How should each gate be scaled? What is the resulting delay with this scaling? (5 p)

4. An inverter is driving another identical inverter across a long resistive wire. The RC product of the long wire, $R_W C_W$, is 100 times that of the $R_{eff} C_G$ product of the inverter in the technology used. Furthermore, in this technology, the inverter's output capacitance is about the same as its input capacitance. In this problem you are to explore how best to insert a number of additional inverters (repeaters) along the wire to minimize the delay

a) Draw a figure of the wire with the driver and receiver at each end of the wire and t**wo** additional inverters (repeaters) inserted at equal distances along the wire. Draw the corresponding circuit model for the entire system of wire segments and inverters. (2 p)

b) Derive the optimal number of wire segments driven by repeaters to minimize the delay from the input of the driver inverter to the input of the receiver inverter at the end of the long wire. (3 p)

c) For the situation resulting from task b), what is the minimum total delay? Assume that all four terms in the total delay are equal to the geometric mean of the two RC products. (3 p)

d) What if the RC product of the wire is only 49 times larger than the RC product of the inverter, how many wire segments would then be optimal for minimum delay if a non-inverted signal is required at the end of the wire? (2 p)

Note: Students taking this exam for the old MCC091 course may opt to solve problem 7 instead of problem 5.

5. Sequential Assume that you are designing an adder for the minimalistic 3-bit ArmStrong processor. The adder is built from three full adders such that the carry-out signal of the first adder is the carry-in signal to the second adder and the carry out from the second adder is the carry in of the third adder, as shown in Figure 3. At the input and output of the adder are two registers made up of flip-flops.

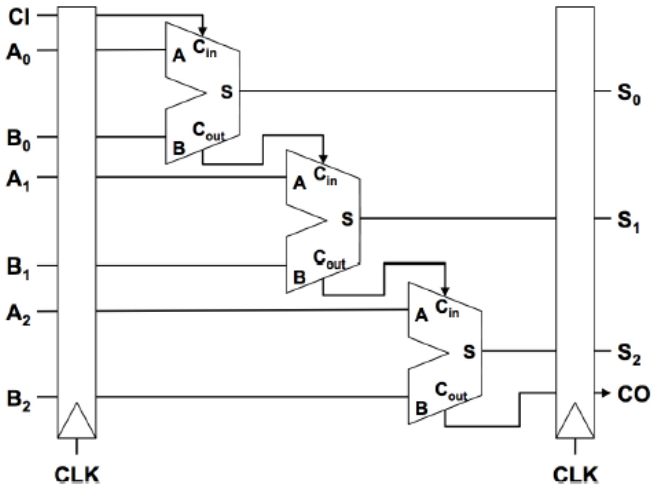


Figure 3: The three-bit adder for the ArmStrong processor.

a) If there is no clock skew, what is the maximum operating frequency of the circuit? Assume the delays for typical CMOS-process parameters, given in the leftmost column in the table below. (2 p)

b) How much clock skew can the circuit tolerate before it might experience a hold violation? Again assume the delays for typical CMOS process parameters from the table below. (2 p)

c) Assume we had characterized the flip-flop and full-adder cells also for the fast-fast and slow-slow corners and arrived at the delays shown in the two right-hand columns in the table below. **Describe** how you would go about extending the results from tasks a) and b) with these additional data so that you can be sure that your adder works correctly also for these two extreme corners. **Carry out** your proposed calculations. Did you have to modify your results from a) and b)? If so, what are the updated results? (6 p)

Delays for full adder and flip-flop cells: **Full adder:**	Delays for **typical** CMOS process parameters [ps]	Delays with CMOS process parameters from **fast-fast** corner [ps]	Delays with CMOS process parameters from **slow-slow** corner [ps]
tpd: A or B → S	30	25	35
tcd: A or B → S	22	16	20
tpd: A or B → Cout	25	20	30
tcd: A or B → Cout	22	17	25
tpd: Cin → S or Cout	20	17	25
tcd: Cin → S or Cout	15	12	20
Flip-flop:			
tpcq	35	28	40
tccq	21	16	24
tsetup	30	25	35
thold	10	5	20

6. Prefix Adders

a. Figure 4 below shows another type of 16-bit prefix-tree adder than the Sklansky adder, namely the Brent-Kung adder. The prefix-adder solution involves an inverse tree to distribute the carries from the top tree to the SUM XOR-gates. Use your knowledge about binary trees to derive a general expression for the worst case carry delay through the prefix-trees for any size *N*-bit Brent-Kung adder.

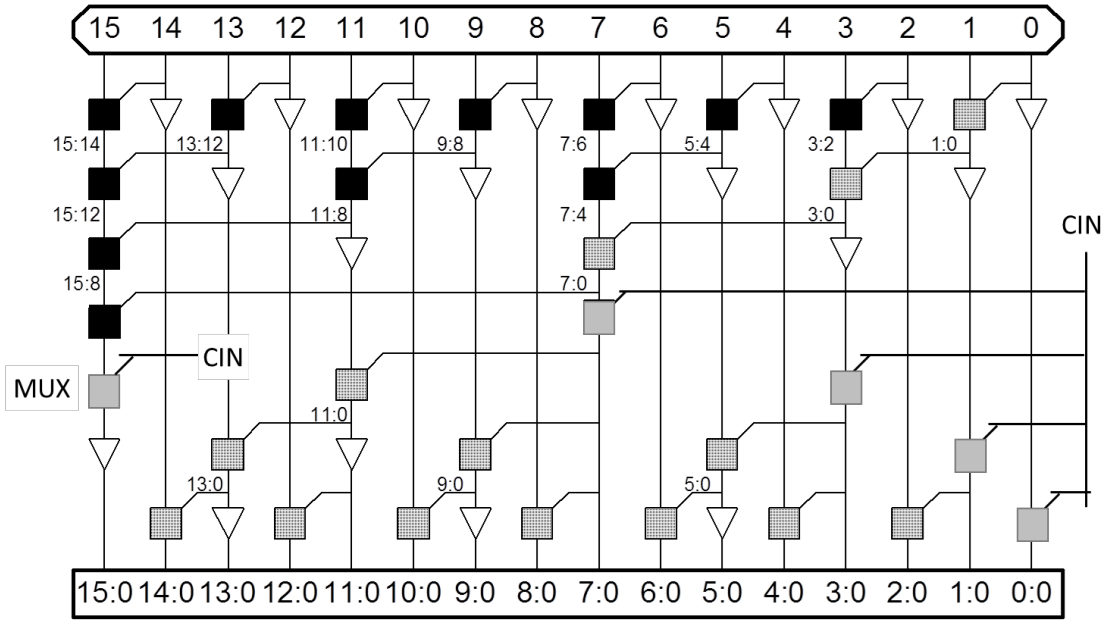


Figure 4: The prefix tree for a 16-bit Brent-Kung adder

(4 p)

b. We found two cells in the cell library, AO312 and AND3, shown in Figure 6, and that raised our curiosity in designing a valency-3 Sklansky adder like the one shown in Figure5 in the Excel template format. The design seems to work properly. Now, the question for you to answer is how these two cells from the cell library are used in the valency-3 Sklansky adder. In particular you should write the logical expressions for cells E10, K10, and Q10 that are marked in grey in the template. (6 p)

		C	D	E	F	G	H	I	J	K	L	M	N	O	P2	Q	R	S
	1										A=	6	<<<<<	ENTER TWO NUMBERS				
	2	ADD=0; SUB=1 >>>			1						B=	-65	<<<<<	-128<NUMBER<128				
	3										SUM=	71						
	4	a8	b8	a7	b7	a6	b6	a5	b5	a4	b4	a3	b3	a2	b2	a1	b1	
	5	0	1	0	0	0	1	0	1	0	1	1	1	1	1	0	1	
	6	0	0	0	1	0	0	0	0	0	0	1	0	1	0	0	0	
	7	G8	P8	G7	P7	G6	P6	G5	P5	G4	P4	G3	P3	G2	P2	G1	P1	G0
	8	0	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0	1
	9	0	0	0	0			0	0	0	0			0	0	0		↓
	10	0	0	0	0			0		0		0		0		0		1
	11	0		1		0		0		0		1		1		1		
	12	SUM8		SUM7		SUM6		SUM5		SUM4		SUM3		SUM2		SUM1		
	13	↓		↓		↓		↓		↓		↓		↓		↓		
	14	SUM converted back to decimal:					71			Both sums are equal?				YES				
	15									OVERFLOW?				NO				

Figure 5: A valency-3 version of the 8-bit Sklansky prefix adder simulated in Excel.

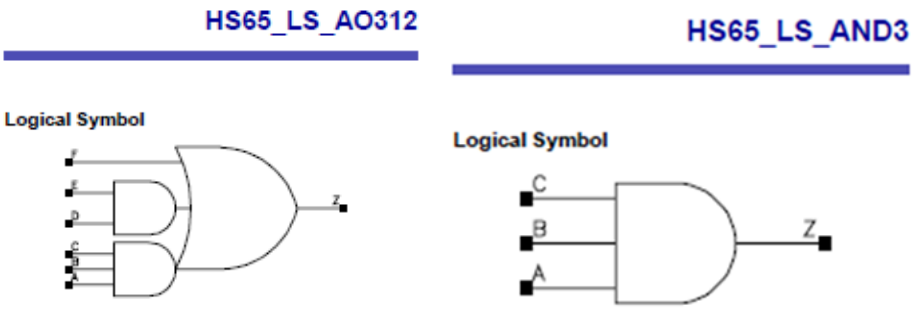


Figure 6: The AO312 and AND3 cells from the cell library for the 65 nm cell library.

THE END!

PROBLEM 7 on the next page is only for students taking this exam for the old MCC091 course.

NOTE: This problem is only for students taking the exam for the discontinued MCC091 course!

7.

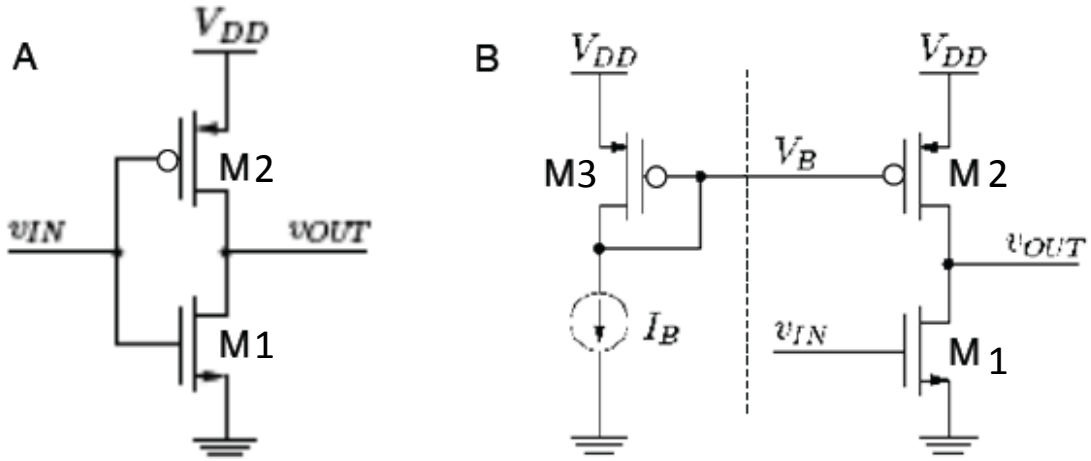


Figure 7: Two CMOS inverters: (A) a CMOS inverter, (B) a pseudo-NMOS inverter.

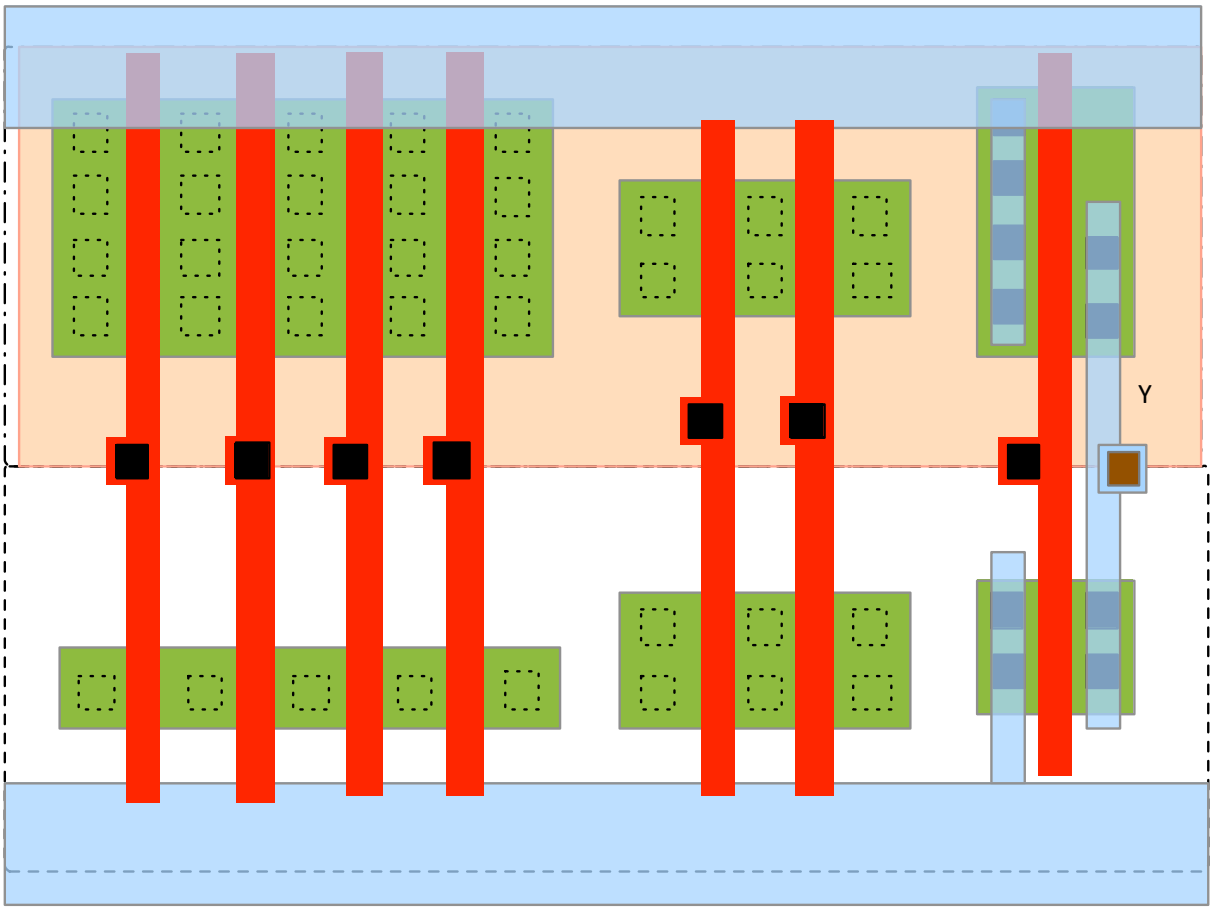
In Figure 7 are the circuit diagrams for two CMOS inverter. The one to the left, (A), is an ordinary CMOS inverter, while the one to the right, (B), is a pseudo-NMOS inverter with a static PMOS load, M2. Transistor M2 is biased through a current mirror so that the bias current $\mathbf{I_B}$ flows also through the amplifier/inverter. In the two circuits the two MOSFETs marked M1 are identical, as are the three pMOS devices marked M2 and M3. Both inverters have the same switching voltage $\mathbf{V_{sw}=v_{IN}=v_{OUT}=V_{DD}/2}$.

a. Determine the bias voltage $\mathbf{V_B}$! (1 p)
b. How are the current gain factors $\mathbf{k_1}$ and $\mathbf{k_2}$ of MOSFETs M1 and M2 related assuming that ew have $V_{TN}=-V_{TP}$? (2 p)
c. In a $\mathbf{v_{OUT}/v_{IN}}$ diagram, mark the areas where both M1 and M2 are saturated for the two inverters! (2p)
d. Draw the small-signal diagram for each of the two amplifiers. (3 p)
e. How large is the small-signal voltage amplification of amplifier B if amplifier A has a voltage amplification $\mathbf{A_V}$ of -20? Motivate! (2 p)

MCC092 2016-10-29 Layout template for task 2c Page number:_____

Anonymous code: _____

Label all nodes clearly. The layout should correspond exactly to the schematic in Figure 1. Use shared drain areas for output nodes whenever possible.



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Label all nodes clearly. The layout should correspond exactly to the schematic in Figure 1. Use shared drain areas for output nodes whenever possible.