Written examination in **Integrated Circuit Design MCC091**

Monday January 5, 2015, at 14.00-18.00 at Mechanical Engineering bldg

Staff on duty: Lena Peterson, D&IT, phone ext: 1822, or mobile 0706-268907. Will visit around 14.30 and 17.00.
Administration: Send exams to Lena Peterson D&IT, and send lists to Susannah Carlsson, MC2.

Technical aids for students: This is a closed-book, no-calculator examination.
The results from the examination will be sent to you via the Ladok system within three weeks. The reviews of this exam will take place Wednesday January 21 12.30-13.00 room 4128 at the CSE dept and Thursday Jan 22, 12.30-13.00 in Lena's office. Solutions will be posted on the course web site in PingPong shortly after the examination. Any student who does not have access to the 2014-2015 PingPong page can contact Lena Peterson (via e-mail to lenap@chalmers.se) to obtain the solution.

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The written examination contains six problems, each worth 10 points. You need 30 points to pass, 40 points for grade "4" and 50 points for grade "5". Any bonus points from the fall 2014 course instance will be added for the higher grades.

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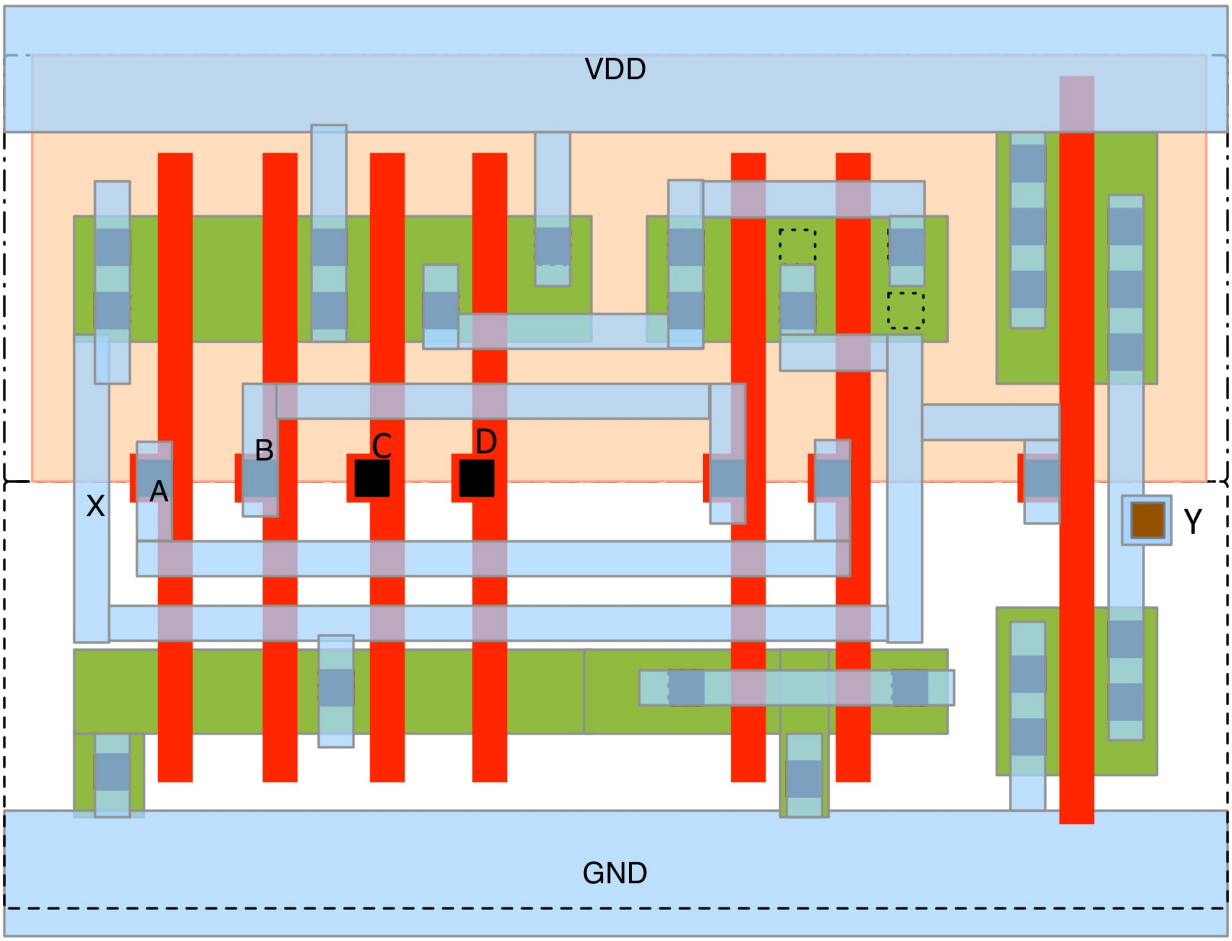
1) Layout, static CMOS logic Below is the layout of a four-input standard cell.

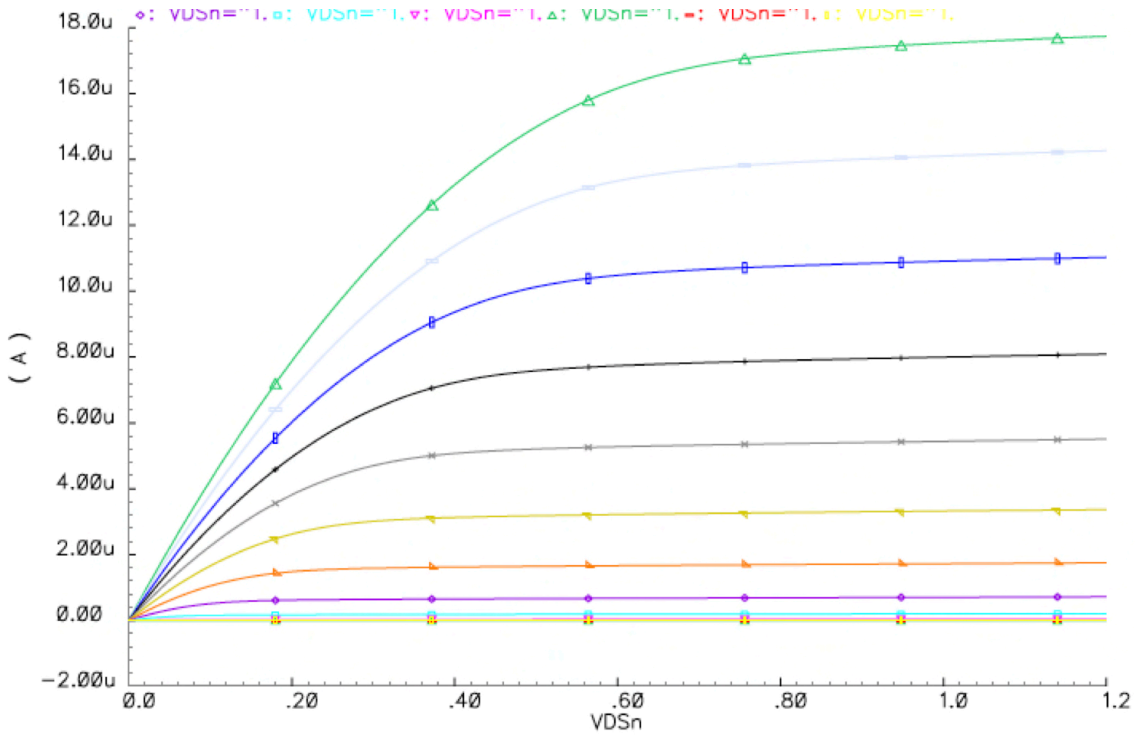
a) Draw the corresponding transistor diagram. Make sure that your transistor diagram matches the layout exactly! (6 p)

b) Identify the logical function that the layout implements. (4 p)



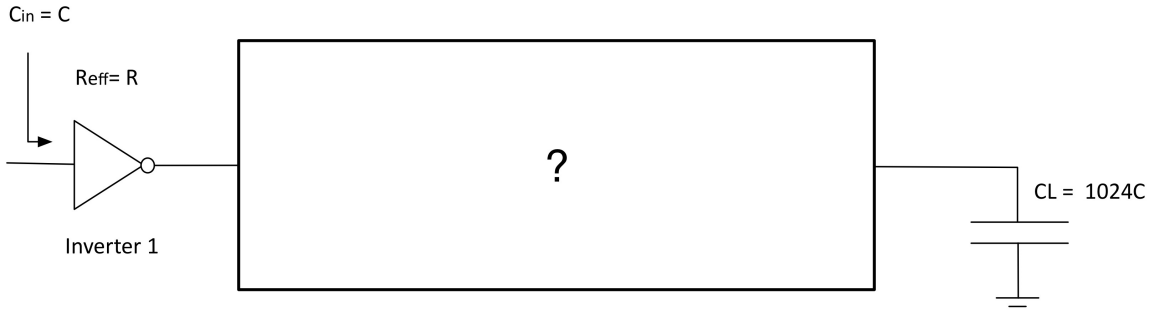
2) **Amplifier large and small signal analysis** An nMOS transistor from the 65-nm process is used as an amplifier with a resistor, R_D, as its load. Below is the output diagram for the nMOS transistor; that is curves for I_D as a function of V_{DS} for different values of V_{GS}. The topmost, green, curve is for the value V_{GS}=1.2 V. The spacing between the curves is 0.1 V, so the light blue one below is for V_{GS} = 1.1 V, the dark blue is for V_{GS}=1.0 V, and so on. The diagram is repeated in a larger scale at the end of the exam.

a) Draw the load line in the output diagram with R_D = 120 kΩ. Use the copy of the output diagram at end of the exam and turn it in with the exam. (2 p)
b) Draw the V_{OUT} vs V_{IN} diagram for the amplifier with R_D = 120 kΩ. (2 p)
c) From your V_{OUT} vs V_{IN} diagram determine approximate values for the maximum small-signal voltage gain of the amplifier and the V_{OUT} value at which the gain has its maximum value. (2 p)
d) What if we wanted the amplifier to have its maximum gain when V_{OUT} is around 0.6 V? What value of R_D should we use then? Approximately, what would the maximum small-signal gain be then? (4 p)



I apologize for the ugly graphics that is due to AWD. The second curve is barely visible when printed. If you look at the curves attached at end I have filled in that curve to make it a little better.

3) **Design & tapering** In a chip you are responsible for designing a driver for an output pad. The capacitance of the pad is (around) 1024C where C is the input of the minimum inverter in the process. The setup is shown in the figure below. The polarity of the output signal is not important in this particular case. Assume that the parasitic output capacitance is half of the inverter input capacitance (that is p_{inv}=0.5). Tau in the particular process is 4 ps. The operating frequency is 200 MHz and you can assume that α is 0.25 for the signal that drives the pad.



a) If minimum delay is the main design goal, how many inverters do you choose to use in the box with the question mark? How would you size them? Draw a figure of your entire inverter chain with the inverter sizes clearly marked. Motivate your design choices, but proofs are not required. (4 p)

b) For your design what is the delay? (2 p)

c) For your design what is the dynamic power consumption? (2 p)

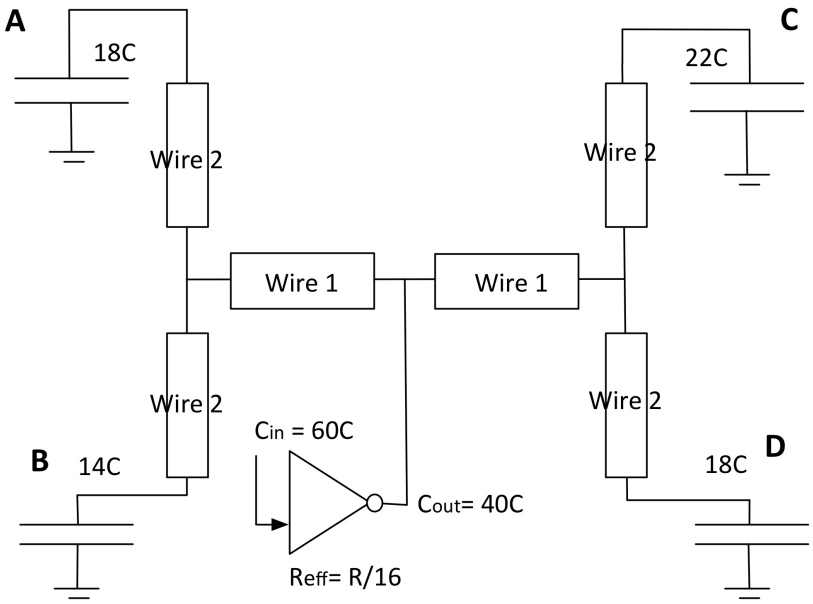
d) From the usual formula used for the dynamic power consumption is seems that to minimize the power consumption during switching there should be no inverters in the box in the figure above. Why is this conclusion incorrect? (2 p)

BONUS QUESTION

e) What if in a similar design situation as in (a) the polarity at the output were of importance and the obvious design choice was an odd number of inverters? Would you add one more inverter or would you remove one? Discuss your considerations. (2 p)

4) **Wire delay** An H-tree is a symmetrical fractal structure that has been used in many chips for the wiring of the clock distribution network. A problem in clock distribution is that the number of flip-flops connected to the clock tree not the same across the chip, so the capacitive load is not the same for all the leaves of the clock tree. In this problem you will investigate the effect of such a load difference, but you will only study a two-level tree.

Below is the two-level H-tree that you are to investigate:
Wire 1 has a total capacitance of 12C and a resistance R.
Wire 2 is narrower and has a capacitance of 6C and a resistance 2R.

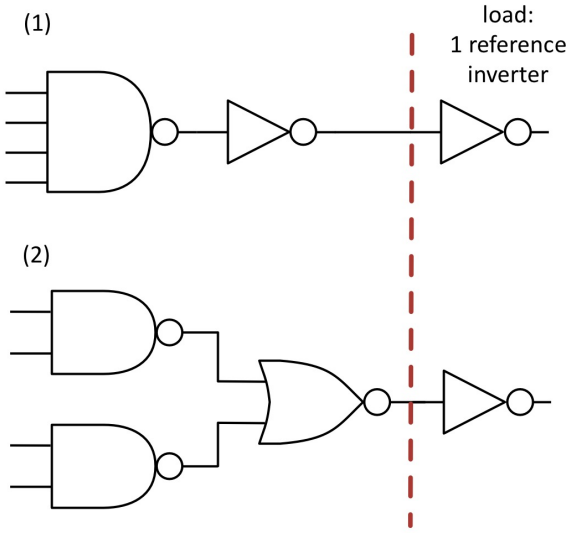


Calculate the clock skews for all pairs of signal in this clock network when driven by the driver in the figure. Since there are four outputs: A, B, C and D, there are six combinations of signals. (10 p)

5) **Logical effort** Below are two possible implementations of a 4-input AND gate. In (1) a 4-input NAND gate is followed by an inverter, in (2) two 2-input NAND gates feed into a 2-input NOR gate. In both cases the outputs are loaded by one reference inverter.

a) Determine which solution is preferable w.r.t. delay, by determining which one has the smaller normalized delay when loaded by one reference inverter as shown in the figure. (6 p)

b) Find the general expressions for the normalized delay, in the form gh+p, for both AND gates. (4 p)

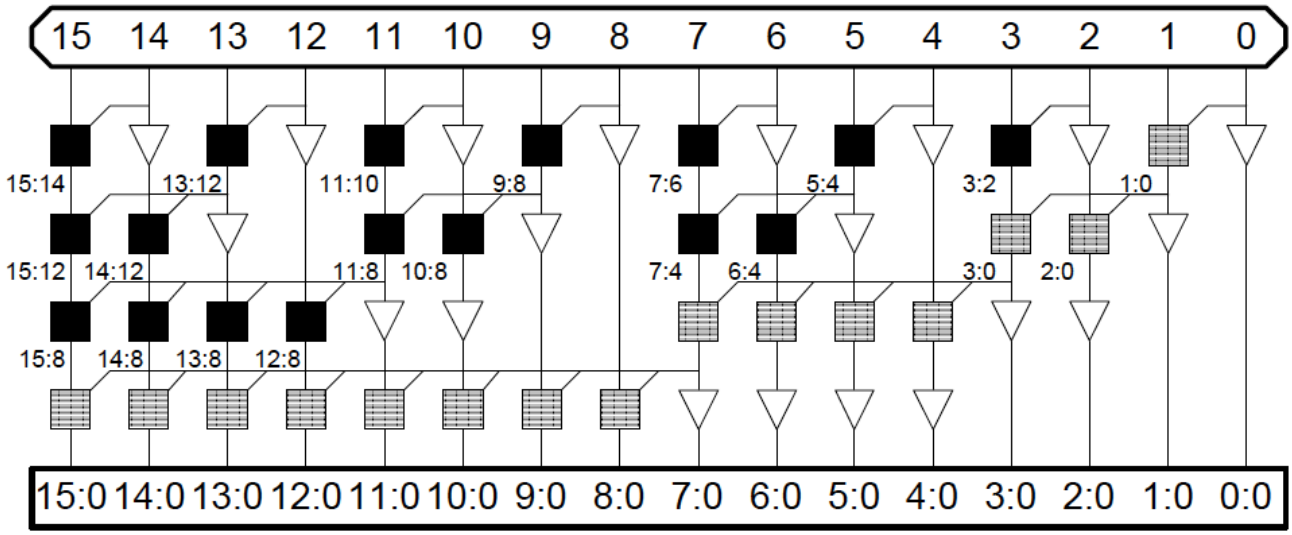


6) Adders Below you see the structure of the well-known Sklansky adder that you analyzed in detail in class this year. This is the figure from the book – please ignore the buffers. In this task you will investigate the use of multiple threshold logic cells in this type of adder. In most modern CMOS processes there are several transistor thresholds for the purpose of saving static power in parts of the circuit that are not delay critical. In our process there are three thresholds: a standard one, a lower one and a higher one.

a) First mark the critical path in Sklansky adder. The figure is repeated at the end of the exam for your convenience so you can turn it in with your exam. (2 p)

b) Then calculate that delay including setup cells and sum generation. Assume that the grey cells for bits 2-3 and 4-7 have sizes X8 at their outputs and X4 at their inputs while all other cells have X4 outputs and X2 inputs. For simplicity assume that the constant part of the normalized delay for all cells is 8 except for EXOR gates that have 6. (3 p)

c) Now assume that the entire adder is synthesized using the standard-threshold library. What if we wanted to decrease the delay of the critical path by speeding up just the cells in that path? Assume that cells with the lowest threshold has 75% of the delay of the cells using the standard threshold (that is their tau is 75% of that of the standard cell). Which other cells would you also have to change to the low-threshold library to make sure that the critical path is still the one with the longest delay? Do not resize any cells. In this problem it is judged more important to reason well than to make detailed calculations! (5 p)



Problem 6 Sklansky ADDER **Student code:_____**