Written examination in **Integrated Circuit Design MCC091**

Thursday October 29, 2015, at 8.30-13.30 at the Mechanical Engineering Bldg

Staff on duty: Lena Peterson, D&IT, phone ext: 1822, or mobile 0706-268907. Will visit around 9.30 and 12.00.
Administration: Send exams to Lena Peterson D&IT, and send lists to CSE student administration office.

Technical aids for students: This is a closed-book exam. Allowed aids: A Chalmers-allowed calculator (non graph-drawing) plus pencil, eraser, ruler, and dictionary (these are always allowed). **The results** from the examination will be sent to you via the Ladok system within three weeks. The grading reviews will take place Monday November 16 2015, 12.15-13.15 in room 4128 and Tuesday November 17, 9-10 in the same room. Solutions will be posted on the course web site in PingPong the day after the examination. Any student who does not have access to the 2015 PingPong page can contact Lena Peterson (via e-mail to lenap@chalmers.se) to obtain the solution.

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The written examination contains six problems, each worth 10 points. You need 30 points to pass, 40 points for grade "4" and 50 points for grade "5". Bonus points from the fall 2015 course instance will be added for the higher grades.

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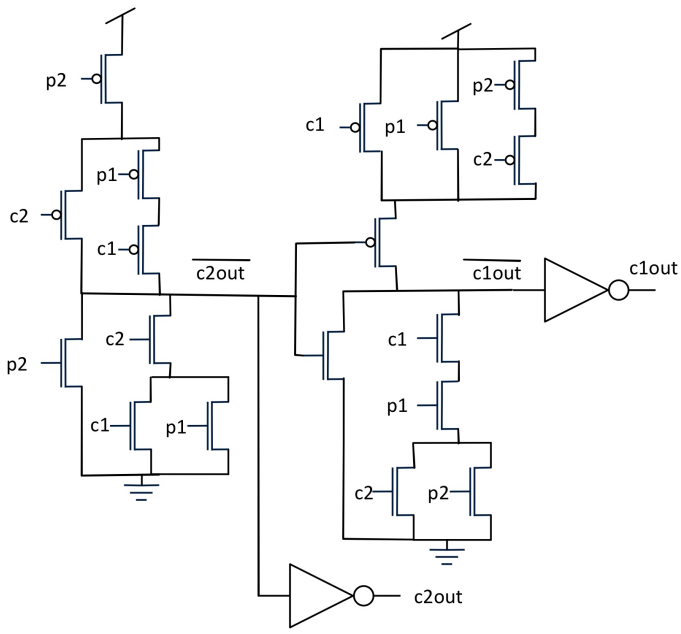
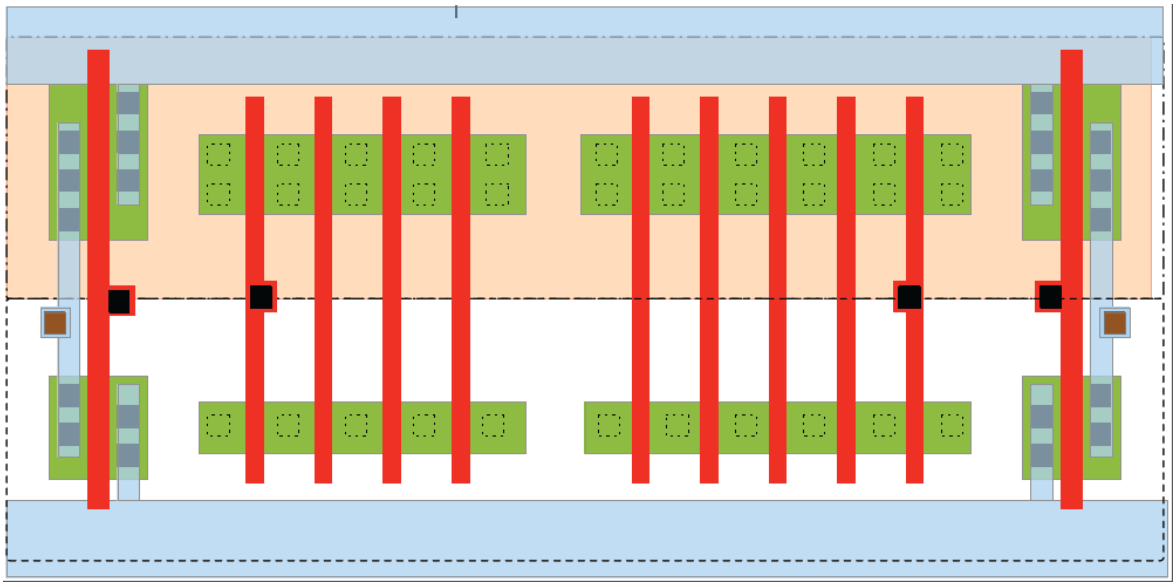
1) **Layout and logic functions** In the figure below, you see the schematic for a proposed carry chain in an unusal adder that can add three numbers. The signals p1 and p2 are partial sums of the three input bits and c1 and c2 are the two carry bits.

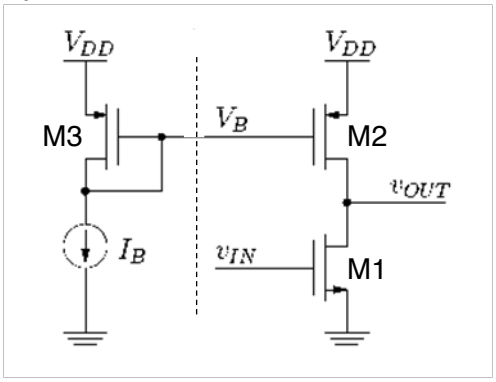


a) What is the logical function for $c2_{out}$? (2 p)

b) Draw the layout for a standard cell that contains the two compound gates and the two inverters in the provided template shown on the next page. Use a single-line-of-diffusion solution for each of the compound gates. Make sure that the output nodes of both compound gates are connected to shared diffusion areas in all cases when there are more than one transistor connected to the compound-gate output node. Each input signal should connect to only one point in the cell. You are allowed to change the order of transistors if necessary, but if you do so, you must also submit your modified circuit diagram that corresponds to your layout. The template is repeated twice on separate pages at the end of the exam so that you can tear it off and hand in. (8 p)



2) Amplifiers and transistor characteristics



V_{DD} = 1.2 V
V_{tn} = -V_{tp} = 0.3 V
V_A ≈ 5 V
I_B=3 µA
V_{OUT} = 0.6 V
Transistors M2 and M3 are identical

In the figure above an nMOS transistor (M1) is used as an amplifier with a pMOS transistor (M2) used as an active load. The current mirror, made up of transistors M2 and M3, is used to mirror (that is, create a copy of) the bias current, I_B, to bias the amplifier transistor. On the next page are simulated output diagrams for transistors M1 and M2.

a) Use diagrams A and B on the next page to determine the values for the voltages V_B and V_{IN}. (2 p)
b) From diagrams A and B estimate the low-frequency voltage gain $|A_V|$ in the operating point. (2 p)
c) Derive the small-signal diagram for the amplifier (include only transistors M1 and M2 in your derivation and use the small-signal diagram to derive the expression for small-signal low-frequency voltage gain, $|A_V|$. (2 p)
d) What if we halve I_B, from 3 µA to 1.5 µA, and adjust V_{IN} so that V_{OUT} is still 0.6 V? Approximately what would the new values for V_B and V_{IN} be? What would happen to the voltage gain $|A_V|$? Would it **increase**, **decrease** or **remain the same**? If the gain would change, approximately how large would the change be? (4 p)

Diagram A

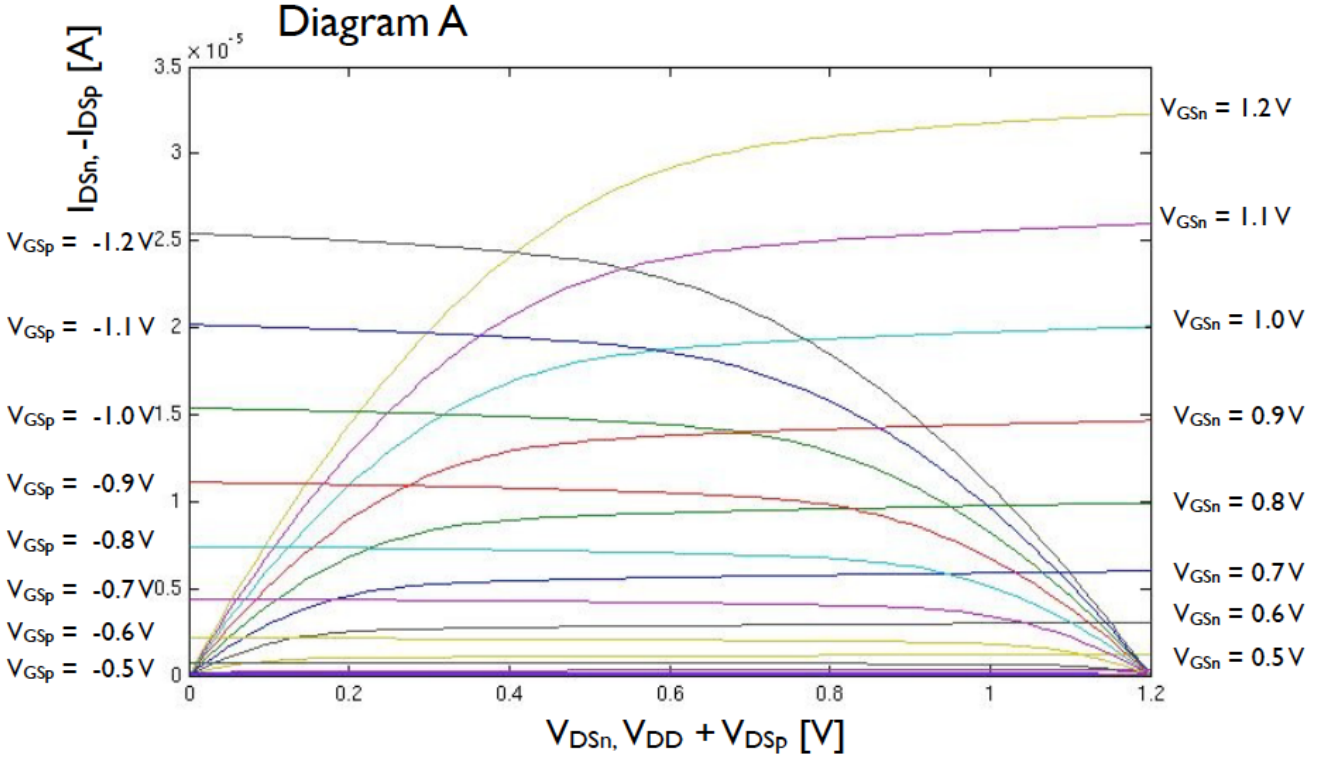
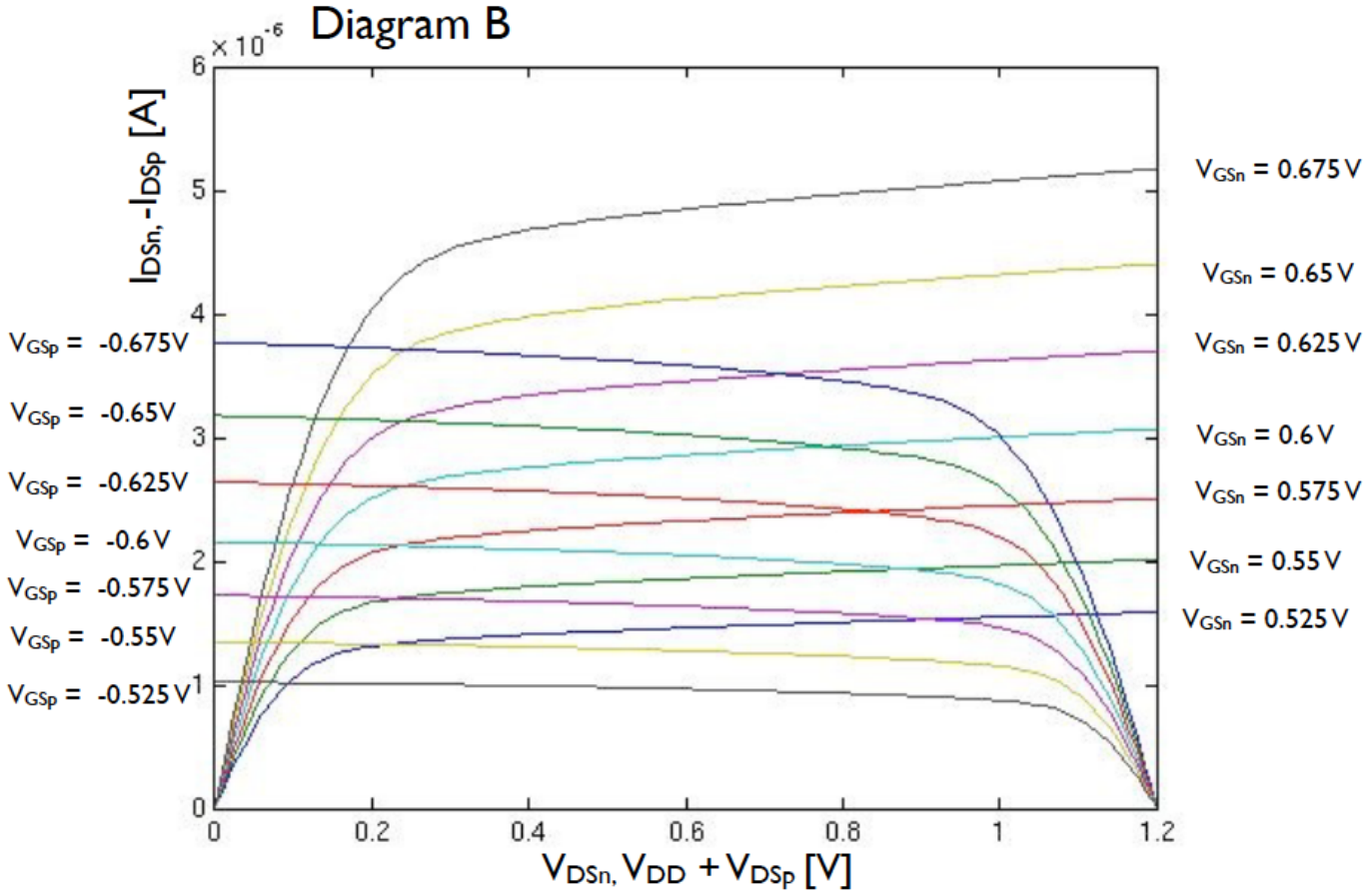


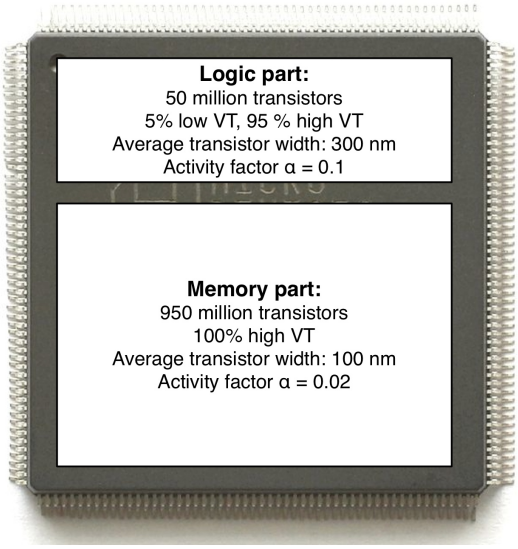
Diagram B



3) Dynamic and static power

A digital system on a chip has 1 billion transistors. Of these 50 million are used in static CMOS logic gates and the rest are used in memories. The two parts of the chip are illustrated in the figure below, which also includes relevant chip and process data:

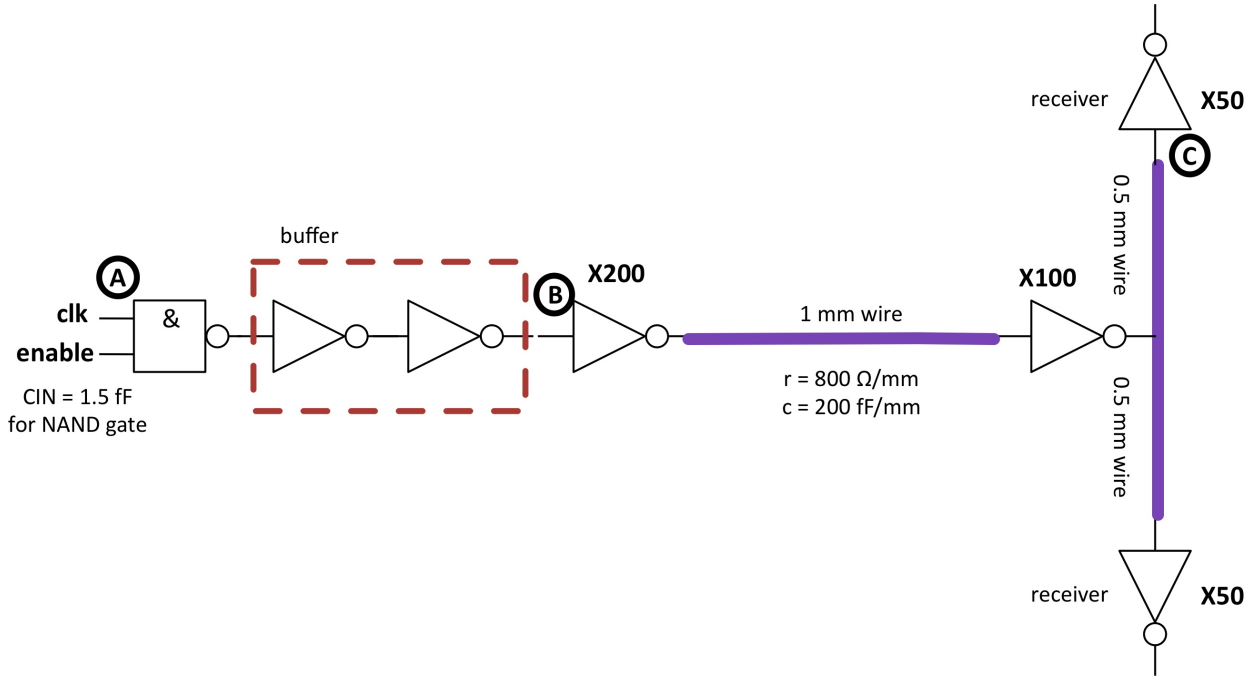
65-nm process data:
V_{DD} = 1.2 V
C_G = 1 fF/µm
$C_D = 0.8 * C_G$
$I_{subthreshold}$ for high VT= 10 nA/µm
$I_{subthreshold}$ for low VT = 100 nA/µm
$I_{gate\ leakage}$ = 5 nA/µm



a) Using data from the figure above, estimate the power due to dynamic switching at a clock frequency of 1 GHz, if we neglect the effects of short-circuit current and wire capacitances. (2 p)
b) Using data from the figure above, estimate the static power consumption for the chip. (2 p)
c) What if the logic part can be redesigned so that fewer transistors than before require the low VT: only 1% of the original number, while the total number of logic transistors has to be increased by 20 %. The activity factor stays the same. What are the effects of this redesign on the static and dynamic power consumption for the logic part? (2 p)
d) If the measures above are not enough, one may have to use power gating to reduce the leakage further. What if we are to power-gate the entire logic part in the chip? We can tolerate only a 5% drop of V_{DD} due to the resistance in the power switch, otherwise the increase in delay will be too large. How wide would our switch have to be if the pMOS transistor ON resistance is 2kΩ/µm? Assume the dynamic power consumption of the logic calculated in task a). (2 p)
e) How much energy would be required to switch the power-gating transistor on and off once? How long a time with the leakage current for the logic part only, as calculated in task b), does that energy correspond to?
BONUS QUESTION (2 p)
f) When considering power gating, would it be better to start with the situation described in tasks a) and b) or the one described in task c)? Discuss the design considerations! (2 p)

4) Wire delay, wire and inverter delay

The figure below shows part of a clock-gated network for distributing a system clock on a chip. The largest available inverter in the cell library (X200, C_{IN}=72 fF, R=100 Ω) was chosen to drive the wire network.



a) Calculate the delay from the input of the X200 inverter (point B) to the input of one of the X50 receivers (point C). You may assume that the input of the X200 inverter is driven by an infinitely strong driver. (4 p)

b) There is a two-inverter buffer inserted between the clock-gating NAND gate and the X200 inverter. Design this buffer – that is, determine the sizes and/or input capacitances of the two buffer inverters for minimum delay from the CLK input of the NAND gate (point A) to the X200 inverter input (point B). (3 p)

c) Calculate the resulting delay from the CLK input of the NAND gate (point A) to the X200 inverter input (B) . (3 p)

5) Critical timing paths, logical effort

In this problem, your task is to make a reasonable estimate of the delay of the time-critical path shown below through a number of 2-input NAND gates, implemented in a 45 nm CMOS process, using data supplied by the manufacturer of the standard-cell library.

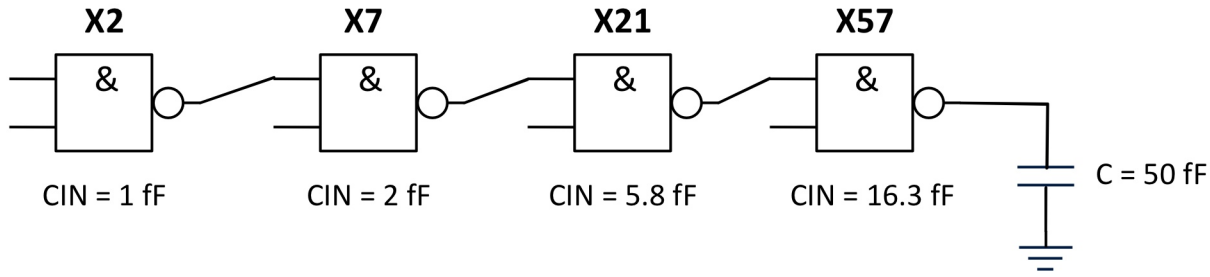


Table 1

INVERTER DATA	X2	X4	X7	X13	X27	X53	X106
Input capacitance [fF]	1	1.3	1.6	3.3	5.8	12	25.1
KLOAD = 0.7Reff [kΩ]	4.1251	2.3529	1.6004	0.7612	0.4298	0.2101	0.1021
Intrinsic delay	13.2	11.9	10.5	10	9.9	10.1	10.6

Note: Unit for intrinsic delay is ps.

Table 2

2-input NAND data	X2	X7	X21	X57
Input capacitance [fF]	1	2	5.8	16.3
KLOAD = 0.7Reff [kΩ]	6.9746	2.2207	0.6572	0.2312
Intrinsic delay	17.6	15.9	14.9	14.6

Note: Unit for intrinsic delay is ps.

a) Based on data from Table 1, determine the FO4 delay. Use data for inverters for which the influence of any non-scalable capacitances is negligible; that is, don't use data for the smaller inverters. (2 p)

b) Extract a value for the logical effort, *g*, of the 2-input NAND using data from Table 2. As before avoid using the data for the smaller gate sizes. How does your extracted value for the logical effort compare to the theoretical value used previously during the course? (2 p)

c) Extract a value for the 2-input NAND gate parasitic delay, *p,* using data from the same gates as you used in task b). How does this value compare to the theoretical value used previously during the course? (2 p)

d) Estimate the path delay using your extracted values and compare the estimated value to the delay obtained using our theoretical values for *p* and *g*. (4 p)

6) Adders

PART A The figure below shows a spreadsheet implementation of one 8-bit carry-skip adder block.

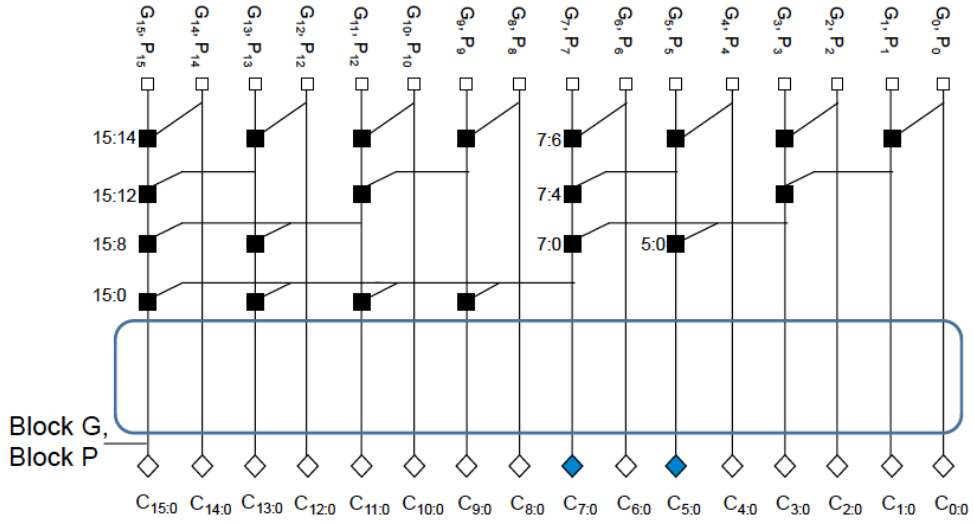
	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T
5		ADD/SUBTRACT					ADD=0		CIN=?		A=	65	<<<<<	ENTER TWO NUMBERS					
6		CONTROL SIGNAL:			0		SUB=1		CIN=?		B=	-65	<<<<<	-128<NUMBER<128					
7											SUM=	0							
8		a7	b7	a6	b6	a5	b5	a4	b4	a3	b3	a2	b2	a1	b1	a0	b0		
9		0	1	1	0	0	1	0	1	0	1	0	1	0	1	1	1		
10		0	1	1	0	0	1	0	1	0	1	0	1	0	1	1	1		
11		G7	P7	G6	P6	G5	P5	G4	P4	G3	P3	G2	P2	G1	P1	G0	P0		
12	MUX	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	0	CIN	P
13	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	1
14	COUT<<	G7:0	P7:0	G6:0	P6:0	G5:0	P5:0	G4:0	P4:0	G3:0	P3:0	G2:0	P2:0	G1:0	P1:0	G0:0	P0:0		
15		0		0		0		0		0		0		0		0			
16		SUM7		SUM6		SUM5		SUM4		SUM3		SUM2		SUM1		SUM0			
17																			
18		SUM converted back to decimal:					0			Both sums are equal?				YES					
19										OVERFLOW?				NO					

a) What is the logic code (that is, the logic function and the inputs that it takes) that describes the output multiplexer in cell B13?

b) What type of logic gates are used in the bit cells to implement the dot operator (also called PG logic in Weste & Harris) used to forward the incoming pairs of carry and propagate signals?

PART B

c) The figure below shows the beginning of a Ladner-Fischer adder design. It is similar to the Sklansky adder, but the fanout of some heavily loaded cells in the Sklansky adder has been reduced to half. Instead, one extra row of dot operator cells has to be added in the highlighted area. Complete the design by adding these missing cells so that all input carries needed for the SUM operation are available at the bottom. As an example, it can be mentioned that C7:0 and C5:0 (blue in the figure) are already available for calculating SUM8 and SUM6, respectively. The figure below is repeated on a separate sheet at the end of the exam that can be handed in with your solutions.



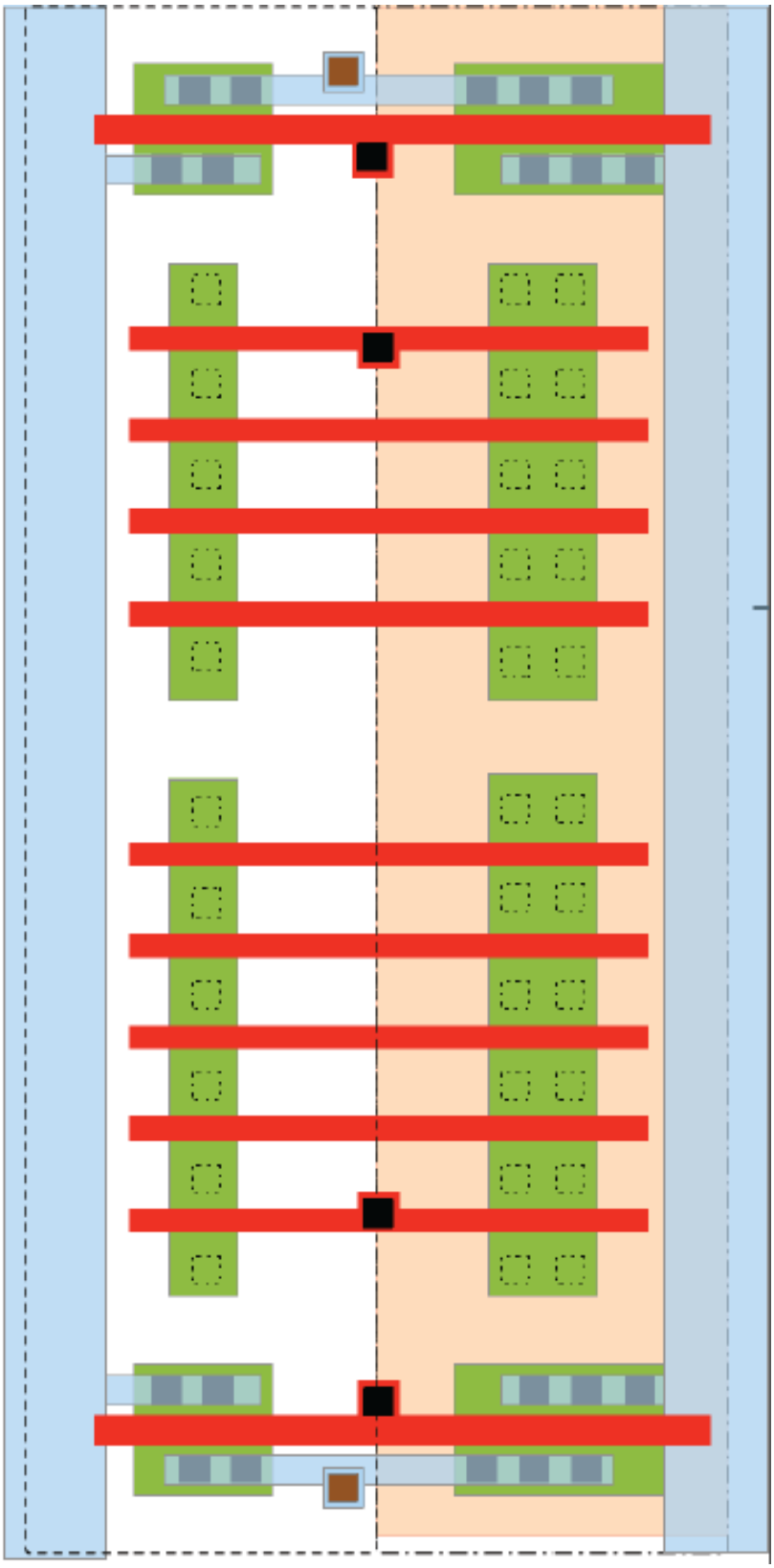
THE END!

Tear-off templates for tasks 1b and 6c are on the following pages

MCC091 2015-10-29 Layout template for problem 1b

Anonymous code: _____

Label all inputs and outputs clearly.



MCC091 2015-10-29 Layout template for problem 1b

Anonymous code: _____

Label all inputs and the output clearly!

MCC091 2015-10-29 Ladner-Fischer adder design for problem 6c

Anonymous code: _____