Written examination in **Integrated Circuit Design MCC091**

Tuesday January 14, 2014, at 14.00-18.00 in the VV-building

Staff on duty: Kjell Jeppson, MC2, phone ext: 1856, or mobile 0703-088581.

Administration: Send exams to Kjell Jeppson, MC2/BNSL, and send lists to Jeanette Träff, MC2/Photonics.

Technical aids for students: None, this is a closed-book no-calculator examination.

The results from the examination will be sent to you via the Ladok system within three weeks. The exact time and place for review of this examination will be posted later on the course web page. Solutions will be posted on the course web site in pingpong directly after the examination.

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The written examination contains six problems, each worth 10 points. You need 30 points to pass, 40 points for grade "4" and 50 points for grade "5".

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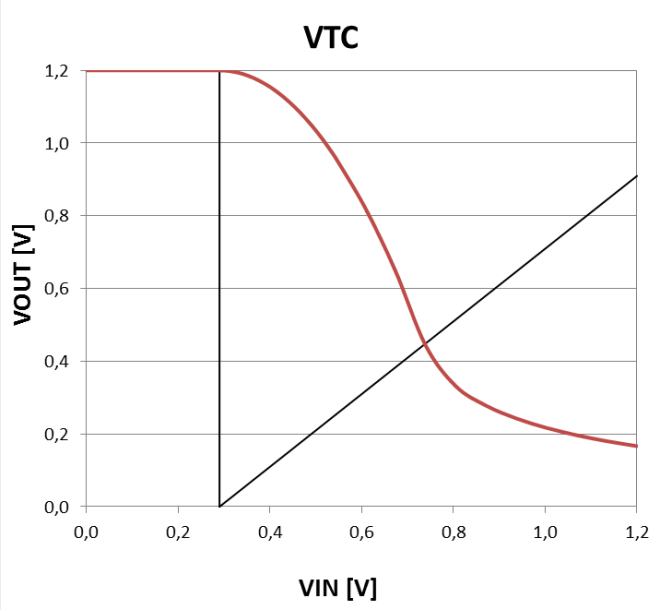
1. **Layout of standard cells.** Make a stick diagram layout of the logic cell F=AB+CD(F+E)! The layout should follow the standard-cell template attached to this thesis. Tear off and hand in the template.(10 p)

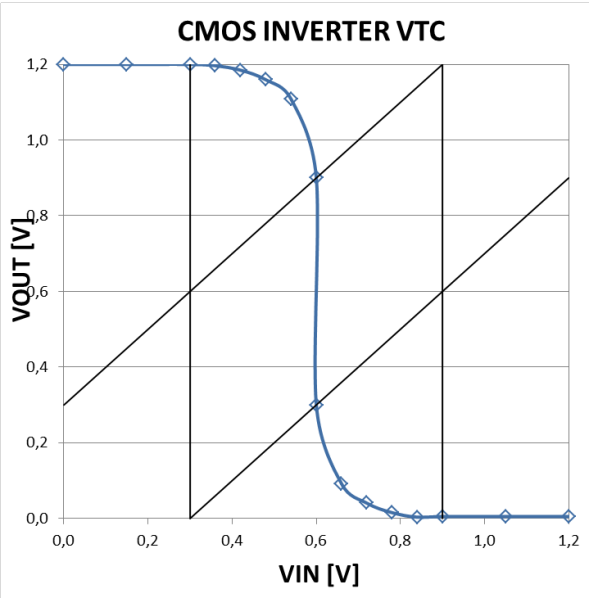
2. A) The left-hand graph below shows **the voltage transfer curve** of a basic MOS amplifier/inverter with a resistive load, R_L. Show, by answering the following two questions, that you have understood the meaning of a square-law model by giving a good (i.e. more or less exact) explanation of how this VTC changes when the parameter kR_L is increased by a factor of four:

   a. How does the curve change in the region where the MOSFET is saturated? (3 p)
   b. How does the value of V_{OUT} for $V_{IN}=V_{DD}$ change if we can assume that $kR_L>>1$? (2 p)

   B) An electrically balanced CMOS inverter, with $k_N=k_P$, has a **switching voltage** $V_{SW}=V_{DD}/2$ as shown in the right-hand VTC graph below. The threshold voltages are equal to $V_{DD}/4$, i.e. $V_{TN}=-V_{TP}=V_{DD}/4$.

   a. What would be the switching voltage of a NAND2 gate using the same MOSFET sizes, when it has both its inputs connected? (3 p)
   b. What would be the switching voltage of a NAND3 gate again using the same MOSFET sizes with all three inputs connected? (2 p)

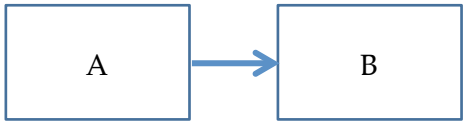




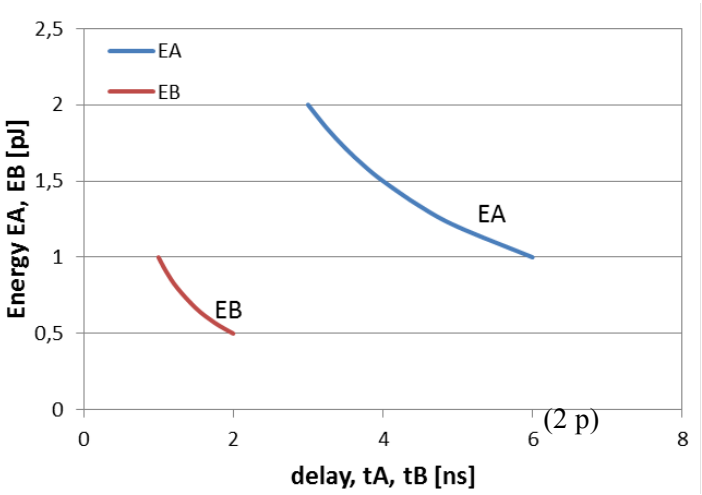
3. **Switching activities**. Calculate the output switching activity of an AOI21 gate if the probabilities that the inputs are "ones" are equal to P=1/2! Inputs can be considered fully random and uncorrelated which means that any of the eight possible input combinations are just as probable. (10 p)

4. **Power.** Consider a logic block consisting of two sub-blocks A and B. Sub-block A can be sized for a minimum delay of 3 ns at the nominal supply voltage, and sub-block B can be sized for a minimum delay of 1 ns at the same nominal supply voltage. Sub-block delays are additive so the minimum delay of the whole block is 4 ns. Your task is to minimize the energy per operation of this block when allowing a total delay of 5 ns (which is more than the minimum delay) using two different methods: by sizing and by reducing the supply voltage.

   a. Minimize the energy per block operation by reducing the supply voltage! Assume for simplicity that the threshold voltage is much smaller than the supply voltage. (4 p)



   b. Minimize the energy per block operation by resizing the blocks while keeping the supply voltage constant. The energy-delay trade-offs with respect to sizing are given by[1] (4 p)



   c. Which method seems to be the most energy efficient? (2 p)

5. **Wire delay**. While determining the optimal tapering factor in a CMOS buffer driving a large capacitive load, we relied on the fact that if the product of some numbers (i.e., the product of tapering factors $f_1 f_2 f_3 \ldots f_N = F$) is constant, then the sum of these numbers has its minimum value when all numbers are equal.

   For the problem of an inverter driving a wire, the RC product of the inverter/repeater is assumed to be constant for all sizes of the inverter/repeater. Similarly, the RC product of the wire, $R_w C_w$, is a constant for any given wire.

   a. First, use the same reasoning to show that the optimal number of wire segments, when inserting repeaters to minimize the wire delay, is given by $M = \sqrt{R_w C_w / RC}\,/2$. (4 p)

   b. How large are the M-dependent delay terms in terms of $\sqrt{(R_w C_w RC)}$ when the optimal M-value has been chosen? (1 p)

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1 There is a small risk here that you might at first be somewhat confused about the statement that resizing the block gates from, say, using X4 gates to using X9 or X13 gates would affect the delay. In our first-order simple RC-model the RC product was assumed to be constant, independent of gate sizing. However, for simplicity this first-order approximation neglected the fact that some percentage of the MOSFET capacitance is not scalable,

$$C_G = \frac{WL\varepsilon_{ox}}{t_{ox}}\left(1+\frac{W_0}{W}\right).$$

This improved second-order capacitance model leads to the following delay and energy models:

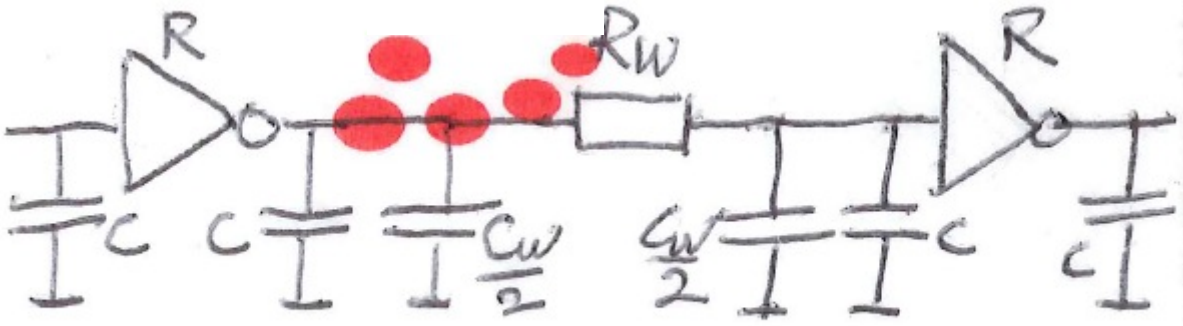
$$t_d = \frac{CV_{DD}}{\frac{W}{L}k'\left(V_{DD}-V_T\right)^2} = t_0\left(1+\frac{W_0}{W}\right), \text{ and } E = CV_{DD}^2 = E_0\left(1+\frac{W}{W_0}\right), \text{ respectively.}$$

These two relationships yield the approximate relationship between energy and delay as given above.

c. Second, use the same reasoning to show that the optimal repeater size for minimum delay is given by $R=R_w/2M$, i.e. a repeater resistance equal to half the resistance of the wire segment! (4 p)

d. How large are the non-M-dependent delay terms with respect to $\sqrt{(R_wC_wRC)}$ when M and R has been selected for minimum delay? (1 p)

e. Bonus point: What airline has supplied the napkin used for the illustrations? (1 p)



Airline napkin illustration of wire problem

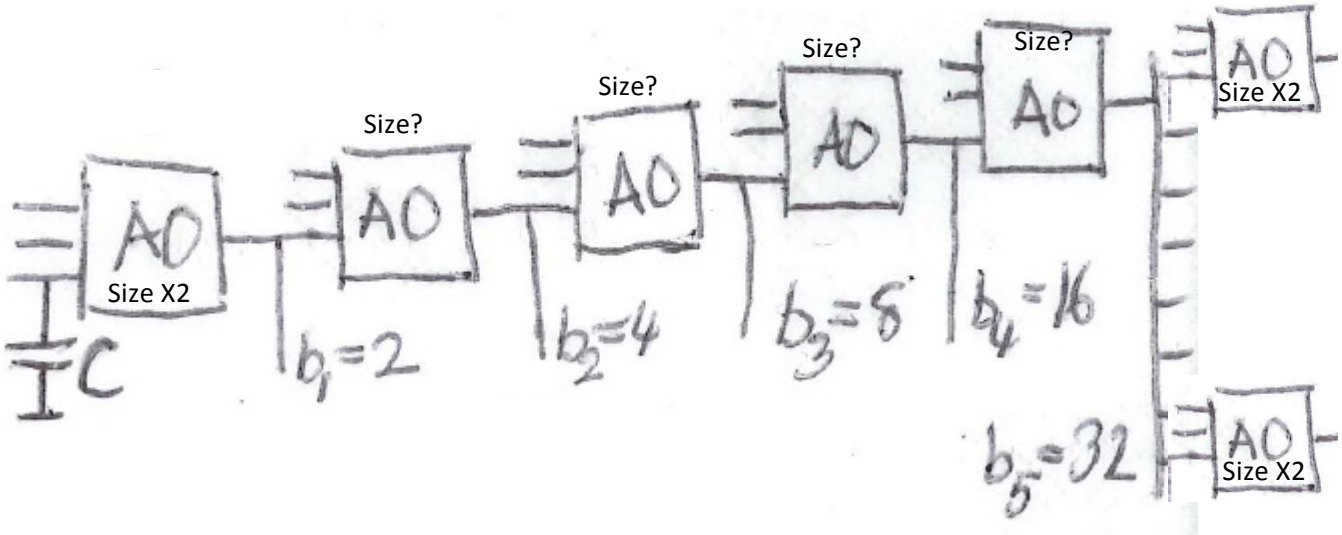
6. Sklansky adder. Assume that we have been assigned the task of designing a 32-bit Sklansky adder. Assume further that we have chosen to design the prefix-tree using AO21 gates from the standard-cell library as shown below. The unit size of the leftmost and the 32 rightmost AO21 gates is X2, which means size X2 input capacitances and size X4 output inverter driving capabilities. The branching factors along the critical path are also shown in the figure. Your task, now, is to determine the X-sizes of the other AO21 gates along the critical path for minimum delay.

a. Outline a plan for how you intend to solve the problem of minimizing the path delay! (2 p)

b. What impact on the optimization process does the path parasitic delay P have? (2 p)

c. Determine the gate sizes for minimum delay according to the plan outlined in a). (4 p)

d. How much faster is the optimized solution compared to a solution with only X2 gates? (2 p)



Airline napkin illustration of the Sklansky adder critical path

STANDARD-CELL LAYOUT TEMPLATE **Exam number:_____**