Written examination in **Integrated Circuit Design MCC091**
Monday October 21, 2013, at 8.00-12.00 in the V-building

Staff on duty: Kjell Jeppson, MC2, phone ext: 1856, or mobile 0703-088581, and Lena Peterson 1822.
Administration: Send exams to Kjell Jeppson, MC2/BNSL, and send lists to Jeanette Träff, MC2/Photonics.

Technical aids for students: None, this is a closed-book, no calculator, examination.
The results from the examination will be sent to you via the Ladok system within three weeks. The exact time and place for review of this examination will be posted later on the course web page. Solutions will be posted at the course web site in pingpong after the examination is over.

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The written examination contains six problems, each worth 10 points. You need 30 points to pass, 40 points for grade "4" and 50 points for grade "5".

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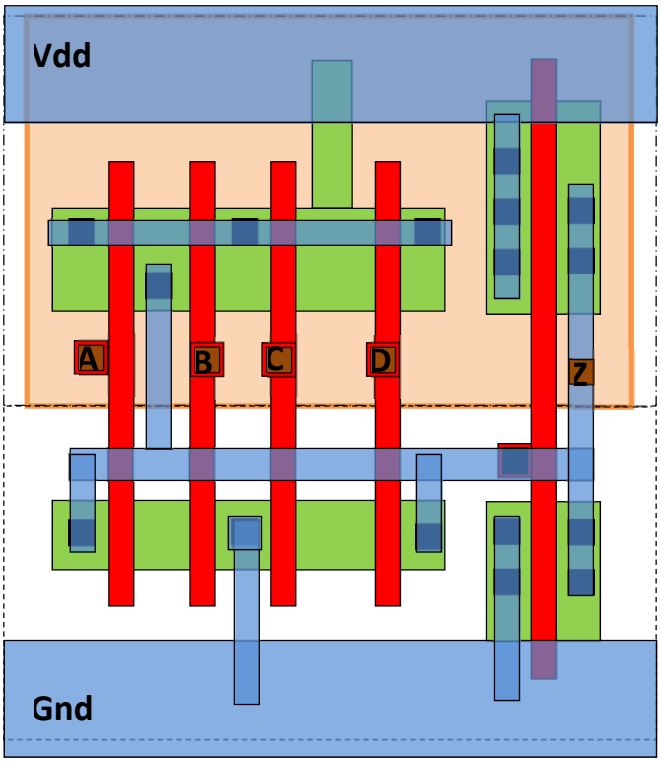
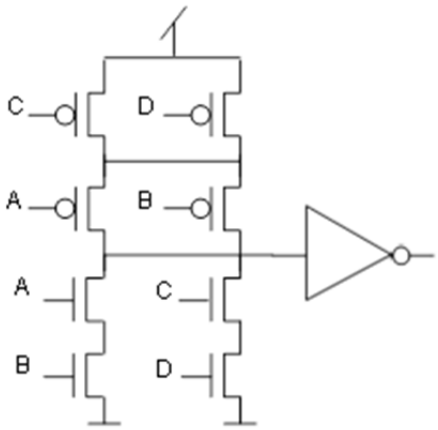
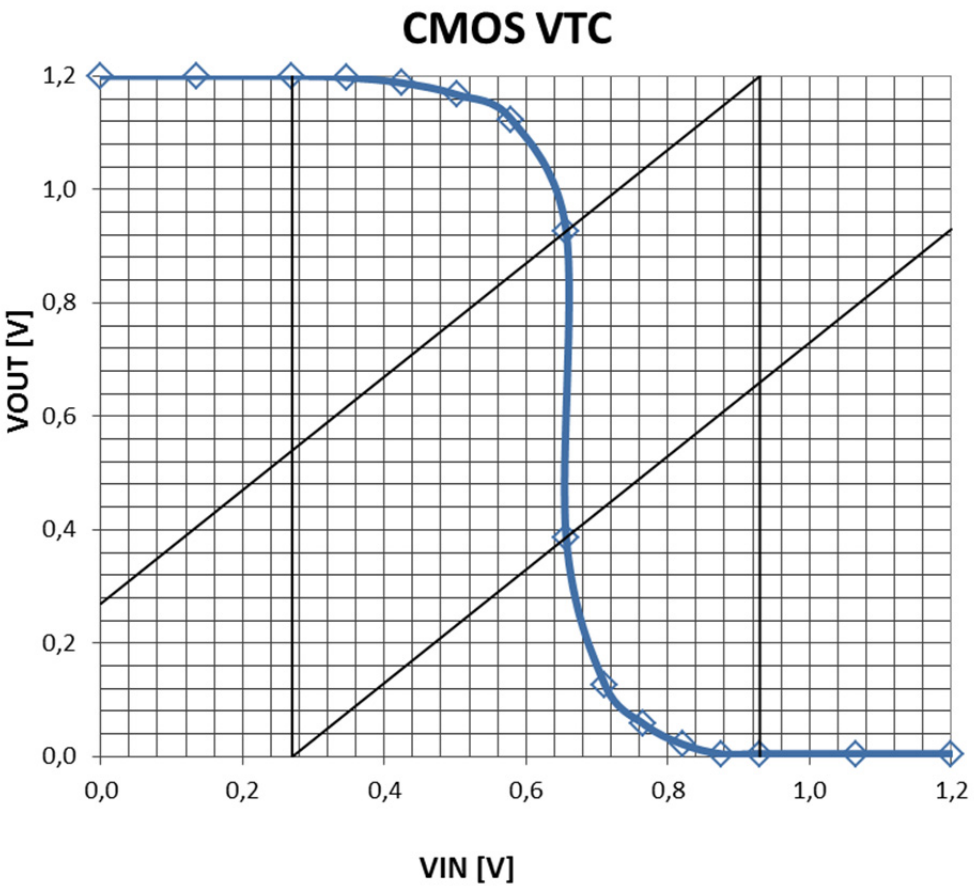
1. **Layout of standard cells**

   What if we are confused by the error messages from the LVS, how shall we go about to find the discrepancies between the layout and the schematic entry? In other words, find the errors in the layout shown below for an AO22 gate!





2. What if we wanted to determine the low and high and noise margins of a 2-input logic gate, to what result would we come by determining NML and NMH from the VTC graph shown below?



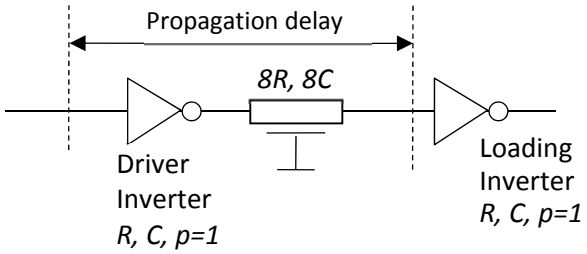
3. **Wire delay and repeaters**

A bus wire from the data path of a processor to the on-chip data cache memory has the resistance $8R$, and the capacitance $8C$, where R and C are equal to the effective resistor and gate capacitances, respectively, of the two identical driving and receiving inverters.

Since the wire is quite long and wire delay increases as L^2, where L is the wire length, maybe it would be wise to insert repeaters.

a. What if we were to insert repeaters, what would be the optimal number of repeaters, M? (5 p)

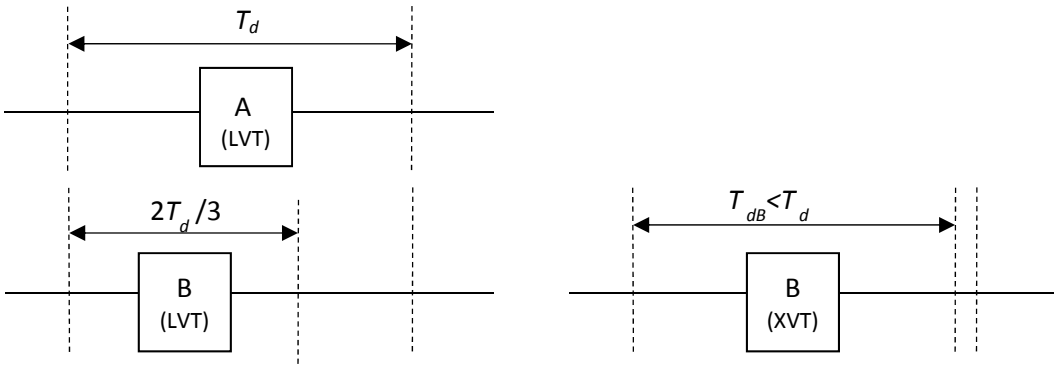
b. What if we inserted repeaters, how much shorter would the delay be as compared to driving the wire without repeaters? Use the optimal number of inverters, or if you cannot find this number, use M=2. (5 p)



4. **Subthreshold leakage and choice of threshold voltage in a multi-VT CMOS process**

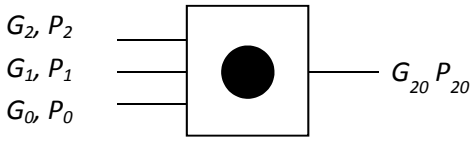
In a processor we have two circuit blocks, A and B, working in parallel. Both blocks are designed using the low-VT standard-cell library (where $V_T=V_{DD}/5$). The delay of block B is only two thirds of the delay of block A, so in a way it is too fast and in some sense probably wasting energy. For block B the supply voltage could be reduced to save energy, or equivalently, the threshold voltage be increased and the timing constraint still be met. The CMOS process used for the design comes with three different threshold voltages, low VT, standard VT and high VT. By redesigning block B with cells from a library with a higher VT, the static leakage power can be reduced and timing constraints still be met. Remember that a 100 mV increase in V_T leads to a factor of ten reduction of the subthreshold current. The standard $V_T=0.3V_{DD}$ and the high $V_T=0.4V_{DD}$.

What if we were to redesign block B using a higher threshold voltage, which cell library would we use, the standard SVT library or the high VT library, if we still were to meet the T_d timing constraint? Assume that the simple square-law MOSFET saturation current model can be used to estimate the MOSFET driving capability! All parameters but the threshold voltages are the same between libraries.



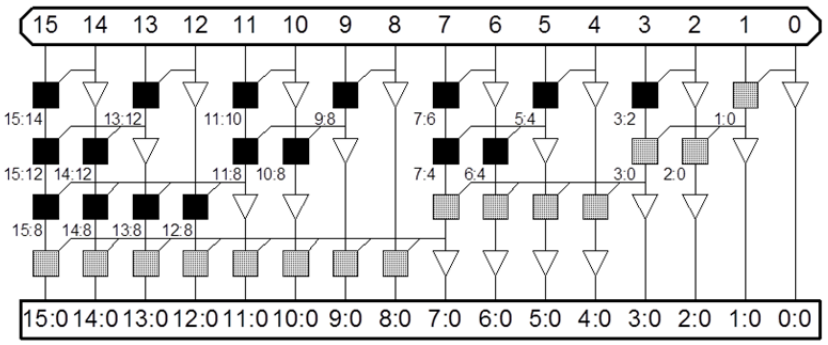
5. **Sklansky adders**

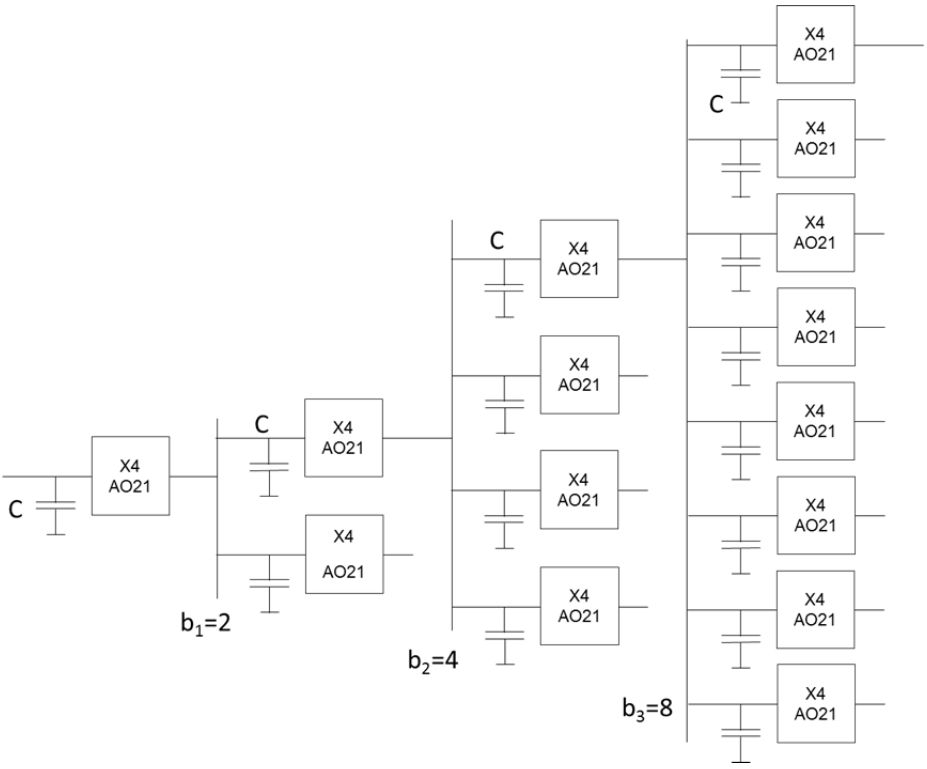
What if we were designing a prefix-tree adder and wanted to try out a so called valency (3) implementation, to what conclusion should we arrive concerning the choice of logic cells from the standard-cell library for the 3-bit input dot operator?

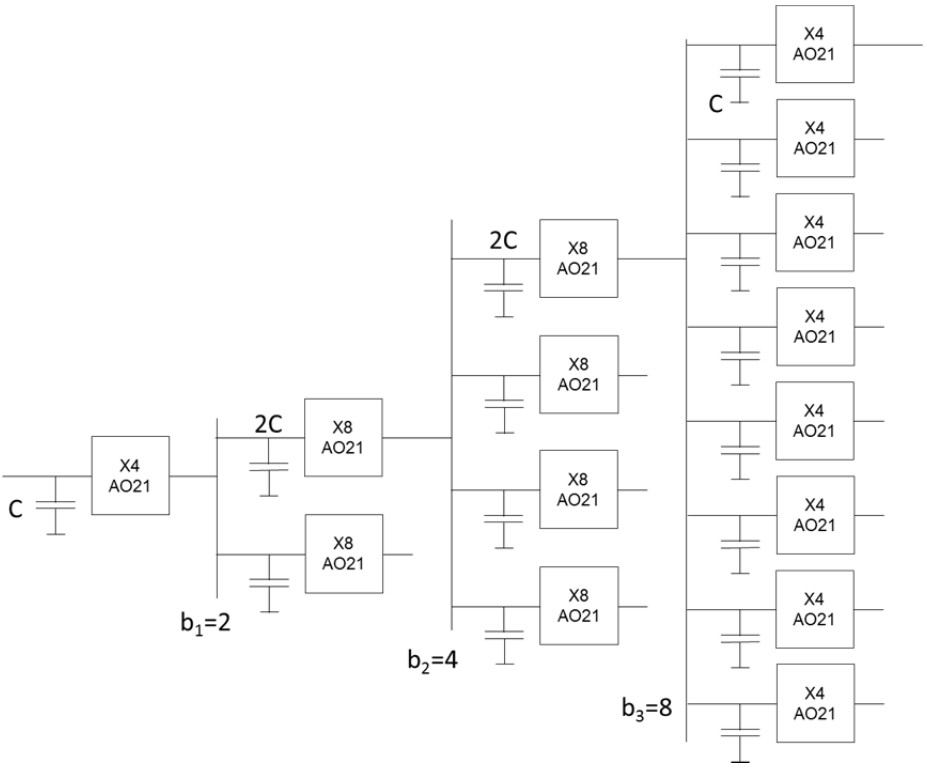


6. **Sklansky adders**

What if we were designing a 16-bit Sklansky adder and were comparing two different cell implementations (see figures), to what result would we come concerning the difference in worst-case propagation delay between the two implementations? In an X4 AO21 gate, the X2 MOSFETs forming the logic function have one set of widths (200 nm for n-channel devices and 400 nm for p-channel devices), while the X4 MOSFETs in the output inverter has twice those widths. Your solution should include a calculation of the logical effort of the AO21 gate!

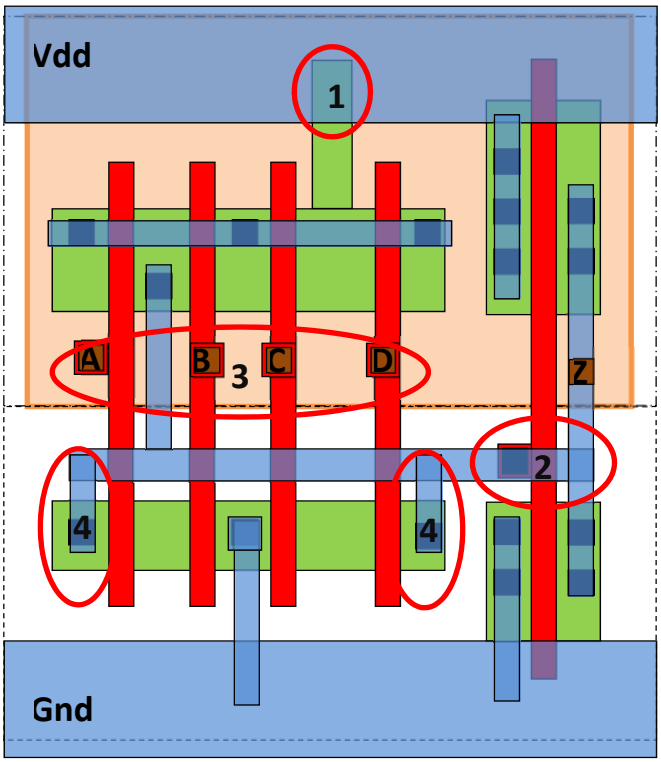

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
15:14 13:12 11:10 9:8 7:6 5:4 3:2 1:0
15:12 14:12 11:8 10:8 7:4 6:4 3:0 2:0
15:8 14:8 13:8 12:8
15:0 14:0 13:0 12:0 11:0 10:0 9:0 8:0 7:0 6:0 5:0 4:0 3:0 2:0 1:0 0:0

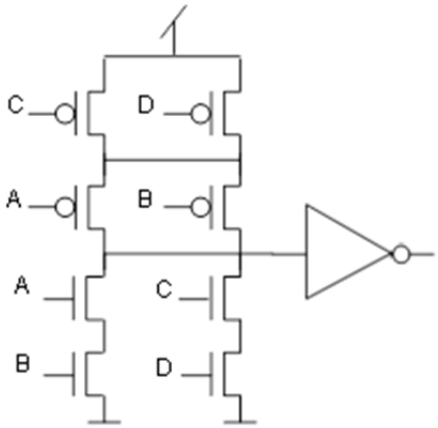

X4 AO21
C
b_1=2
b_2=4
b_3=8


X4 AO21
X8 AO21
C
2C
b_1=2
b_2=4
b_3=8

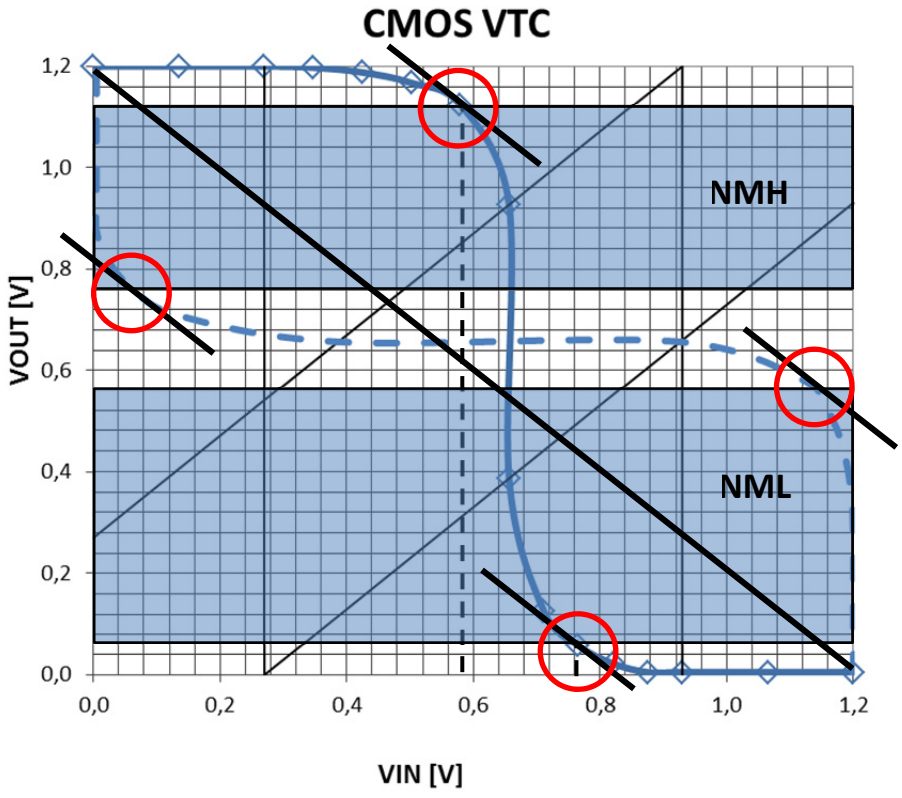
SOLUTIONS

1. 1. Missing V_{DD}-contact to p-active, 2. Inverter input shorted to output, 3. Wrong ordering of inputs compared to schematic, 4. Accidentally misplaced metal wire





2. VOH,min=1.12 V, VIL,max=0.58 V; VIH,min=0.76 V; VOL,max=0.06 V.
   NML=VIL,max-VOL,max=0.58-0.06=0.52 V; NMH=VOH,min-VIH,min=1.12-0.76=0.36 V
   Solid black lines indicate voltage gain A_V=-1.



SOLUTIONS

3. Insert M repeaters. Total delay $t_d=M(R(2C+8C/M)+8R/M*(C+4C/M))$.

   M-dependent part of delay: $RC(2M+32/M)$; Take derivative wrt M: $dtd/dM=2-32/M^2$. $M_{opt}=4$;

   Delay without repeaters (M=1): 50RC; Delay with repeaters (M=4): 32RC.

4. Our delay formula is delay=RC, where $R=\frac{V_{DD}}{\frac{k}{2}(V_{DD}-V_T)^2}$; Maximum delay is given by T_d!

   Block B delay with LVT: $\frac{2}{3}T_d=\frac{2}{3}\frac{2C}{kV_{DD}(1-0.2)^2}=\frac{2C}{kV_{DD}0.96}<T_d=\frac{2C}{kV_{DD}0.64}$;

   Block delay with SVT: $\frac{2}{3}\frac{2C}{kV_{DD}(1-0.3)^2}=\frac{2C}{kV_{DD}0.74}<T_d$;

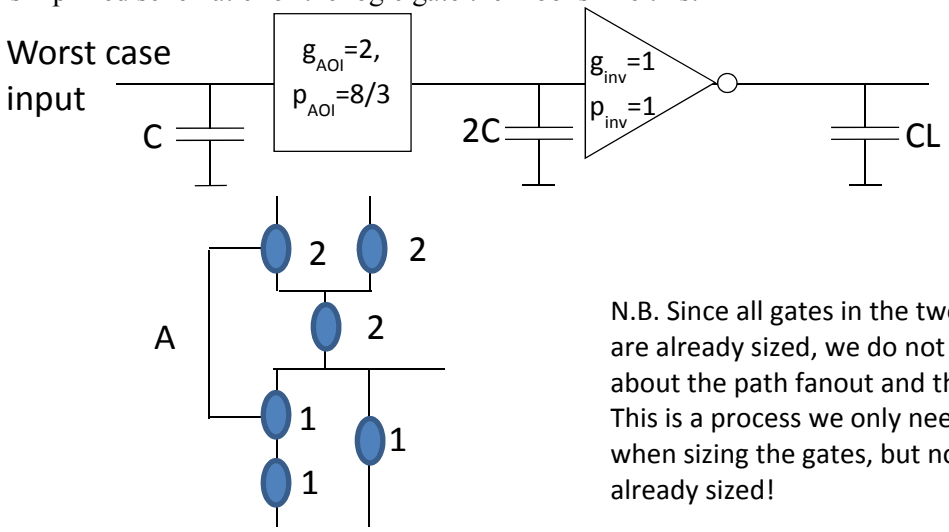
   Block delay with HVT: $\frac{2}{3}\frac{2C}{kV_{DD}(1-0.4)^2}=\frac{2C}{kV_{DD}0.54}>T_d$;

   Conclusion: we can change to SVT cell library, but not to HVT cell library.

5. $G_{20}=G_2+P_2G_1+P_2P_1G_0$; $P_{20}=P_2P_1P_0$; Chosen gates are AO321 and AND3

6. The question is how large the *delay difference* is between two given implementations. Then we can forget about the parasitic delay because it is the same in both implementations. But we need the logical effort of the AO21 gate. In a non-inverting X4 gate all logic MOSFETs are size X2, which means nMOSFETs are 200 nm wide and pMOS logical MOSFETs are 400 nm wide to compensate for lower mobility. The X4 output inverter devices are twice as wide. As indicated by the given capacitances in the schematic, X8 logic MOSFETs are sized X4.

   The simplified schematic for the logic gate then looks like this:



   N.B. Since all gates in the two critical paths are already sized, we do not need to worry about the path fanout and the path efforts. This is a process we only need to go through when sizing the gates, but now gates are already sized!

   Total delay of AO21 gate is given by $t_d=p_{AOI}+g_{AOI}*2+p_{inv}+C_L/2C=(p_{AOI}+g_{AOI}*2+p_{inv})+0.5*CL/C$. The conclusion is that the logical effort of the AO21 gate is 0.5 because of the factor 2 larger output inverter (X2/X4=0.5).

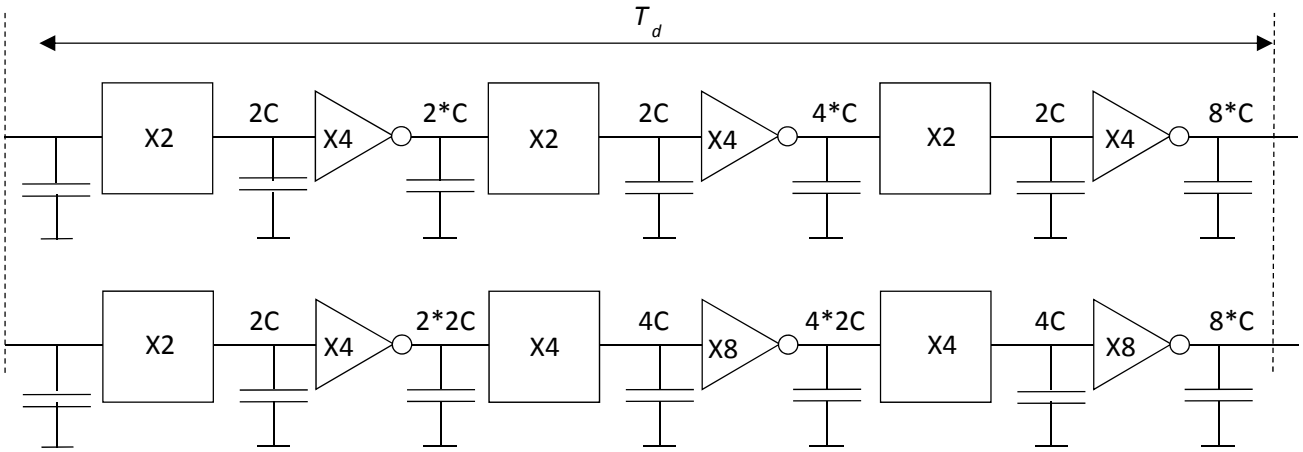
   The delay in the first case is: $parasitic\_delay+g_{AO21}*(2+4+8)= parasitic\_delay+7$.

   The delay in the second case is given by: $parasitic\_delay+g_{AO21}*(4+4+4)= parasitic\_delay+6$.

   We showed during lecture 13 that the second case is the optimal case with minimal delay. However, the speed gain between the two cases is only one RC delay unit.

SOLUTIONS

An alternative solution could look like this (without involving the logical efforts of anything else but the inverter for which g=1 by definition, and because h=2 for the AOI gate in all instances):



Between the two cases it is only the inverter delays that changes.

Top case delay= parasitic_delay+2*C/2C+4*C/2C+8*C/2C=parasitic_delay+7

Bottom case delay= parasitic_delay+2*2C/2C+4*2C/4C+8*C/4C=parasitic_delay+6

Hence, the bottom case solution is one delay-unit faster than the top case solution.