Written examination in **Integrated Circuit Design MCC091/MCC090**
Friday January 18, 2013, at 14.00-18.00 in the Maskin building. ☺

Staff on duty: Lena Peterson, mobile 0706-268907. Will visit around 15.00 and 17.00.
Administration: Send exams to Lena Peterson, D&IT, and send lists to Lena Ackevall.

Technical aids for students: This is a closed-book examination, only the calculator is allowed.
The results from the examination will be sent to you via the Ladok system within three weeks. The exact time and place for review of this examination will be posted later on the course web page. Solutions will be posted at the course web site in pingpong.

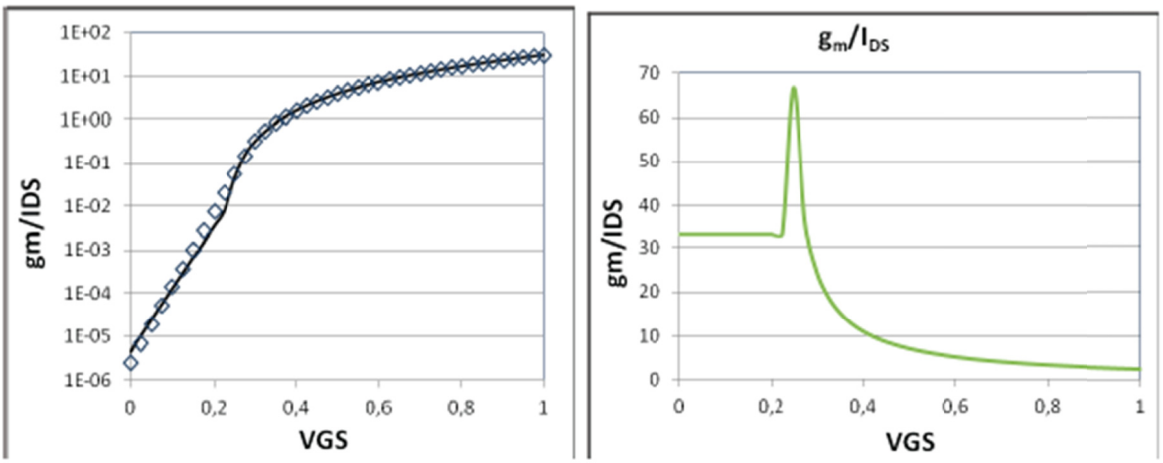
==========

The written examination contains six problems, each worth 10 points. You need 30 points to pass, 40 points for grade "4" and 50 points for grade "5". Any bonus points earned academic year 2012/2013 are added to the exam result.

==========

1. Checking learning outcomes concerning MOSFETs and amplifiers. Students taking the exam for MCC090 should do only task b.

a) The figures below show a student MOSFET model fitted to experimental data, and the corresponding g_m/I_{DS} curve. Comment on the model to data fit, and use the g_m/I_{DS} diagram to discuss the most suitable amplifier biasing points. (5 p)



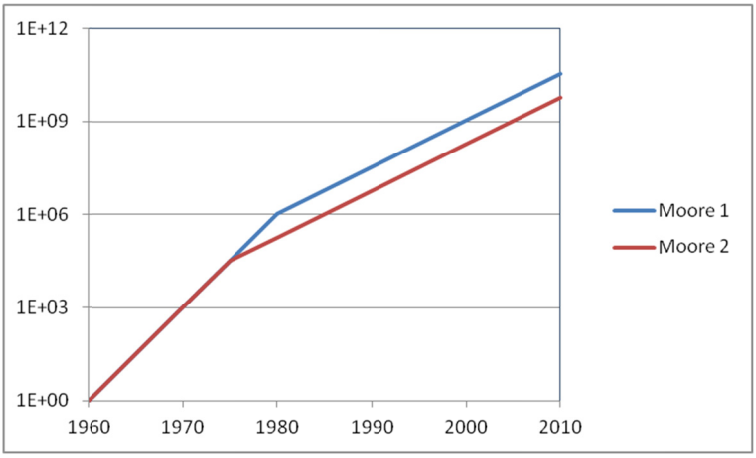
b) Assume that the MOSFET has a square-law V_{GS} dependence, i.e. no velocity saturation, but that the threshold voltage varies with V_{DS} due to a phenomenon named drain-induced barrier-lowering (DIBL). A simple linear model for threshold voltage can be written $V_T=V_{T0}-\sigma V_{DS}$, where V_{T0} is the zero-V_{DS} threshold voltage and sigma is the model parameter (σ=0.025). Calculate the output conductance (that is the partial derivative w.r.t. V_{DS}) in the bias point I_{ON}, V_{DD}, and the corresponding Early voltage! V_{DD}=1.2 V. (5 p)

2. **Checking learning outcomes for scaling** In 1965 Gordon Moore noted that the number of transistors on a chip had doubled every year from 1 transistor in 1960 to 2^5=32 transistors five years later. In a visionary paper in the Electronics magazine he made the prediction that this doubling of the number of devices every year would continue at least until 1980.

a) How many transistors would then be possible on a chip in 1980 according to this prediction? (3 p)

b) In 1975 Gordon Moore modified his prediction and said that from 1980 the number of transistors on a chip would double only every two years. What year would we see the first one billion transistor chip according to this modified model? (3 p)

c) In reality, the change in rate he predicted came already in 1975. What year would we then see the first one billion transistor chip? (4 p)

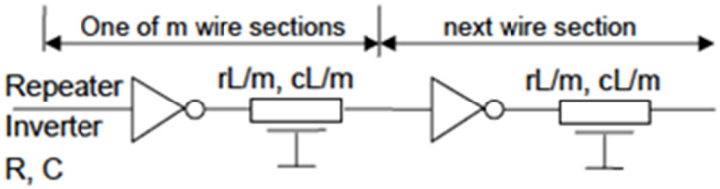


3. Checking learning outcomes concerning CMOS propagation delay and wire delay

This problem concerns a wire on a chip in a 65-nm process. The wire is part of a bus that connects the register file with an ALU. The wire is 1 mm long and 125 nm wide. It has a capacitance of 0.1 fF/µm and a resistance of 0.8 Ω/□.

a) Calculate the resistance per µm, the total capacitance and the total resistance of the wire. (2 p)

b) We assume the wire is driven be an inverter. Your task is to insert similar repeater inverters in the wire to decrease the delay. You ay assume that the receiver at the end of the wire is a similar inverter. The setup can be visualized like this:



where L is the length of the wire, c the capacitance per length and r the resistance per length and m the numver of wire segments. Fins an expression for the number of wire segmetns, m, that gives the minimum delay. You can neglect the parasitic capacitance of the inverters. (6 p)

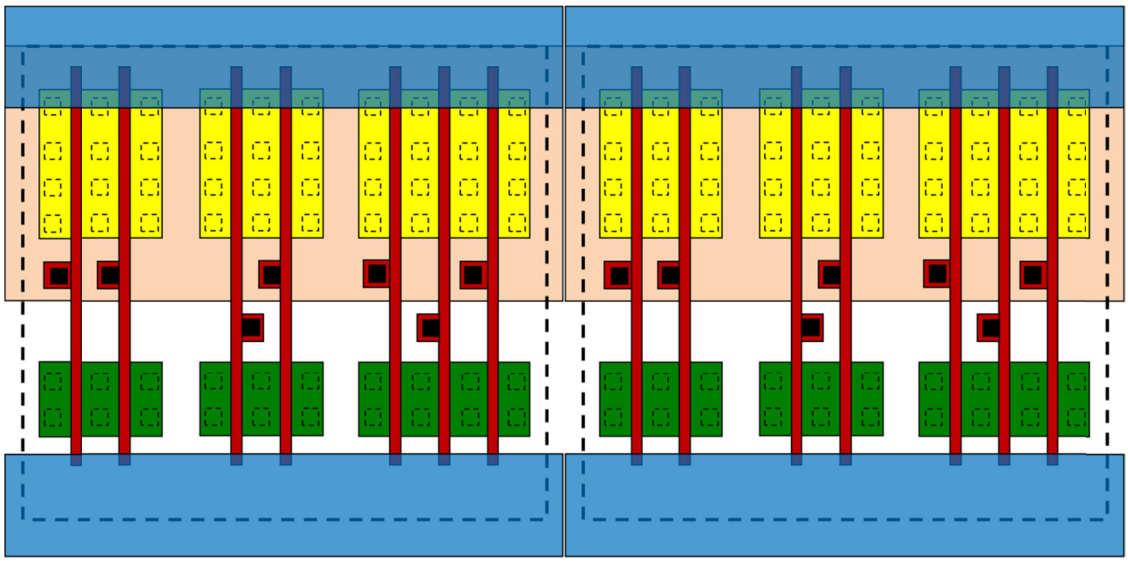
c) As a designer you now have to plug in the numbers and decide on what actual number of repeaters to use. Assume R = 1 kΩ and C = 6 fF for the inverters you are to use. What number of repeater would you select? Motivate! (2 p)

d) **Additional question only for those taking this exam for MCC090** Calculate the delay of the wire with no repeaters (only the driver and the receiver inverter). Calculate the delay with the number of repeaters you selected in task c). Compare! (5 p)

4. Checking learning outcomes concerning CMOS layout and dot operators

a) Use the enclosed standard cell layout template to design a dot operator cell! (7 p)

b) What would be the area of such a 32-bit PG ripple chain if the size of the template is 3.2*2.6 μm²? (3 p)



5. Checking learning outcomes concerning power dissipation and driving large capacitances.

A pad, which connects a chip to the outside world, has a large capacitance due to its size – and it cannot be scaled down substantially since the physical connection has to be made to the outside world. Its capacitance is 0.5 pF. This problem concerns the power dissipated in the circuitry that drives the pad and also the delay in this circuitry. We assume that we use a 65-nm process with V_{DD} = 1 V.

a) What is the dynamic power consumption of the pad capacitance if it is carrying a signal that has frequency of 100 MHz? (1 p)

b) If you drive this large a capacitance with a small inverter the dynamic power will be larger than what you calculated in a). Why? (2 p)

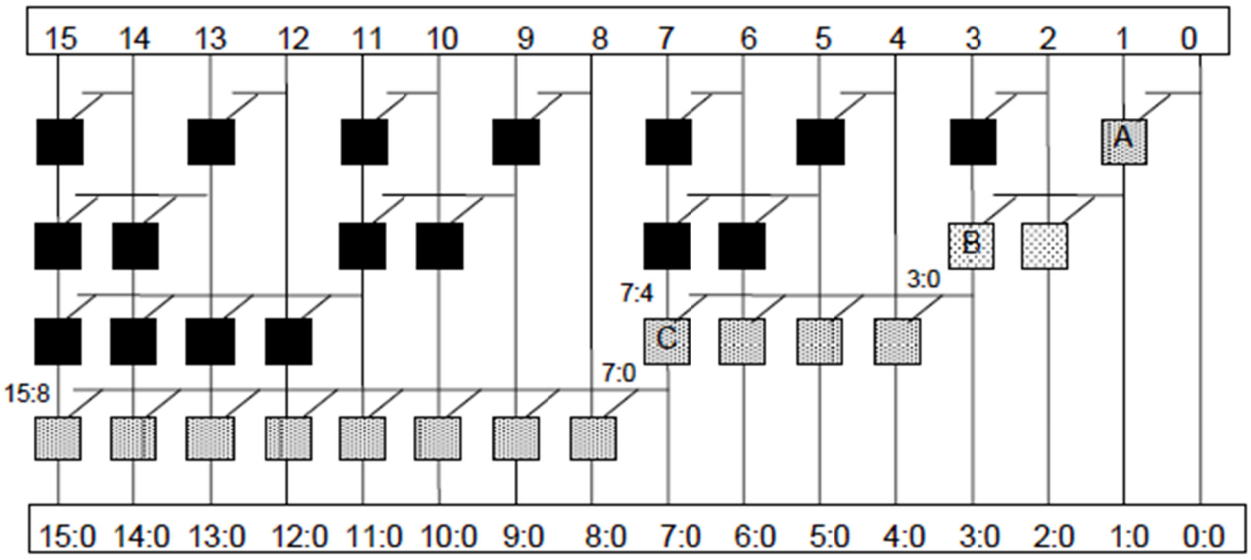
c) Suggest a solution with scaled inverters that can drive the pad capacitance at 100 MHz (the chain is to start with the standard-size inverter which in this process we assume to have an input capacitance of 5 fF and a resistance of 1 kΩ). Motivate your solution. (5 p)

d) What is the dynamic power consumption of the entire chain of inverters including the pad. What percentage of this power is due to the inverters? (2 p)

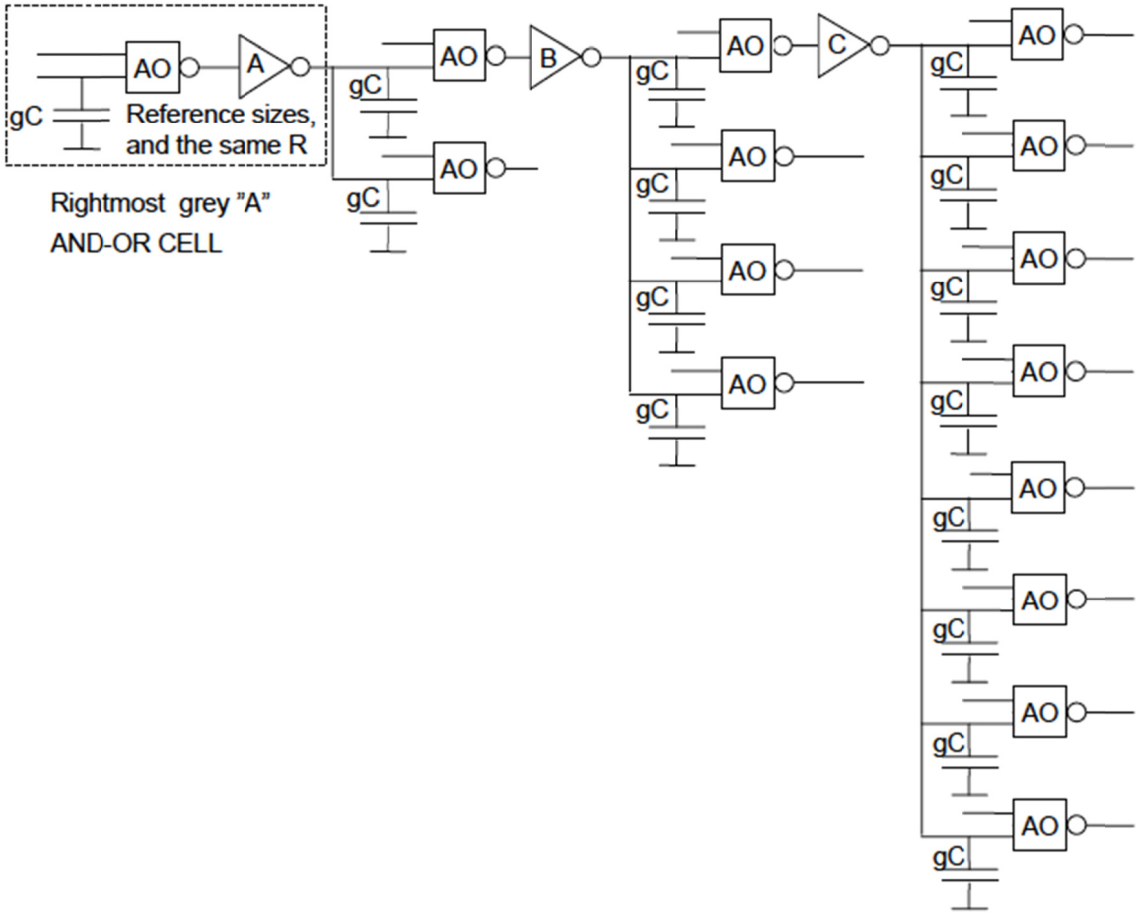
6. Checking learning outcomes concerning adders and path delay.

The figure below shows the Sklansky adder. The black cells in the prefix tree are complete dot operators containing both P and G logic. The gray cells are simpler AO gates, i.e. AND-OR gates, delivering a G output according to $(G_{out})=(G_i,+P_iG_{in})$. Here, (G_i,P_i) are the bit G and P control signals from the bit setup cell which is not shown explicitly in the figure.

Each gray AO cell contains an AOI gate followed by an inverter. All the AOI cells are of the same size, with the same driving capability and the same input capacitance. However, the size of the inverter can be chosen to minimize the delay. Assume that the logical effort of the AOI gate is two.



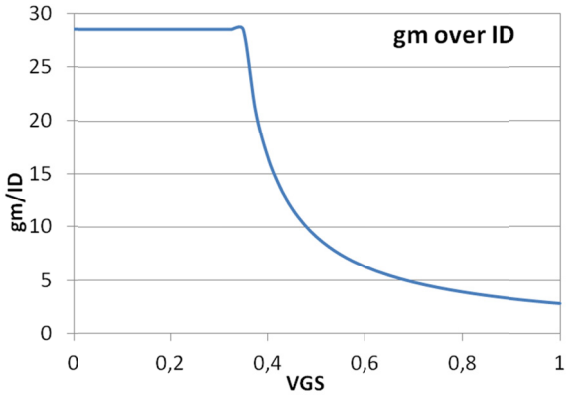
Your task as a designer is to determine the sizes of the sizes of the inverters in the AO gates B and C to minimize the delay. Below you find a figure that shows a more detailed view of the network of AOI gates and inverters. Note that the inversion of the AOI gates are shown with bubbles and therefore the text is "AO" on these cells. (10 p)



Solutions:

1. Amplifiers and inverters

a) In the subthreshold region I_{OFF} and n are not chosen properly. The transconductance, that is the derivative, is not continuous in the point where the MOSFET leaves subthreshold region for the saturation region.
I_{ON} should be chosen lower and n should be larger, see diagram to the right. A suitable bias point is close to the threshold voltage, say 100-200 mV above threshold.



b) Output conductance $g_{DS} = \frac{\partial I_{DS}}{\partial V_{DS}} = k(V_{GS} - V_T)\sigma = \frac{\sigma I_{DS}}{(V_{GS}-V_T)/2}$
In the desired bias point (I_{ON}, V_{DD}): $g_{DS} = \frac{\sigma I_{ON}}{(V_{DD}-V_T)/2}$

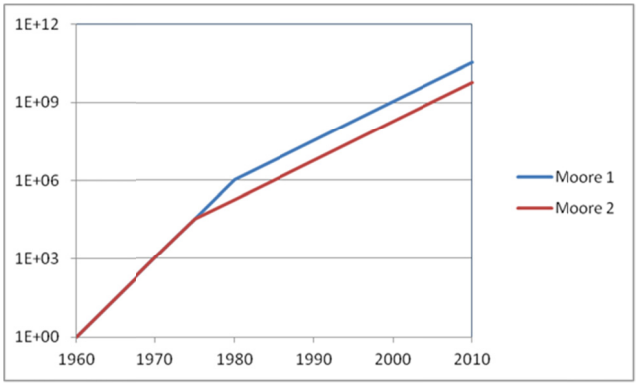
But we also have: $g_{DS} = \frac{I_{ON}}{V_{DD}+V_A}$. Hence $V_A = \frac{V_{DD}-\sigma V_{DD}-V_{T0}}{2\sigma} \approx \frac{V_{DD}-V_{T0}}{2\sigma}$.
With V_{DD}= 1V, V_{T0}=0.2 V and σ=0.025, we obtain V_A=16 V.

2. Scaling

a. Number of transistors 1980, i.e. after 20 years:
$2^{20}=(2^5)^4=(32*32)^2=1000^2$= 1 million transistors

b. Another factor of 1000 now takes not only 10 but 20 years, so the answer is year 2000.

c. Five years shift means 1975+10+20years=year 2005.



3. CMOS propagation delay and wire delay

a) The total capacitance is easy: C_w=0.1fF/µm*1000 µm= 100 fF= 0.1 pF. For calculating the wire resistance we need to know its width. Assume W µm. Wire resistance is then $0.8*1/W$ Ω/µm and $800/W$ Ω.
Assuming W=100 nm=0.125 µm we obtain 6.4 Ω/µm and 6.4 kΩ/mm, respectively.
In conclusion: C_w=0.1 pF, R_w=6.4 kΩ, and R_wC_w=640 ns. R=1 kΩ, C=6 fF, $t_{d,buf}=RC$=6 ps.

b) Cut the wire into m segments and insert m buffer inverters with delay $t_{d,buf}=RC$=6 ps. The essential m-dependent parts of the propagation delay is given by

$$t_d = m\left(t_{d,buf} + \frac{rcL^2}{2m^2}\right).$$

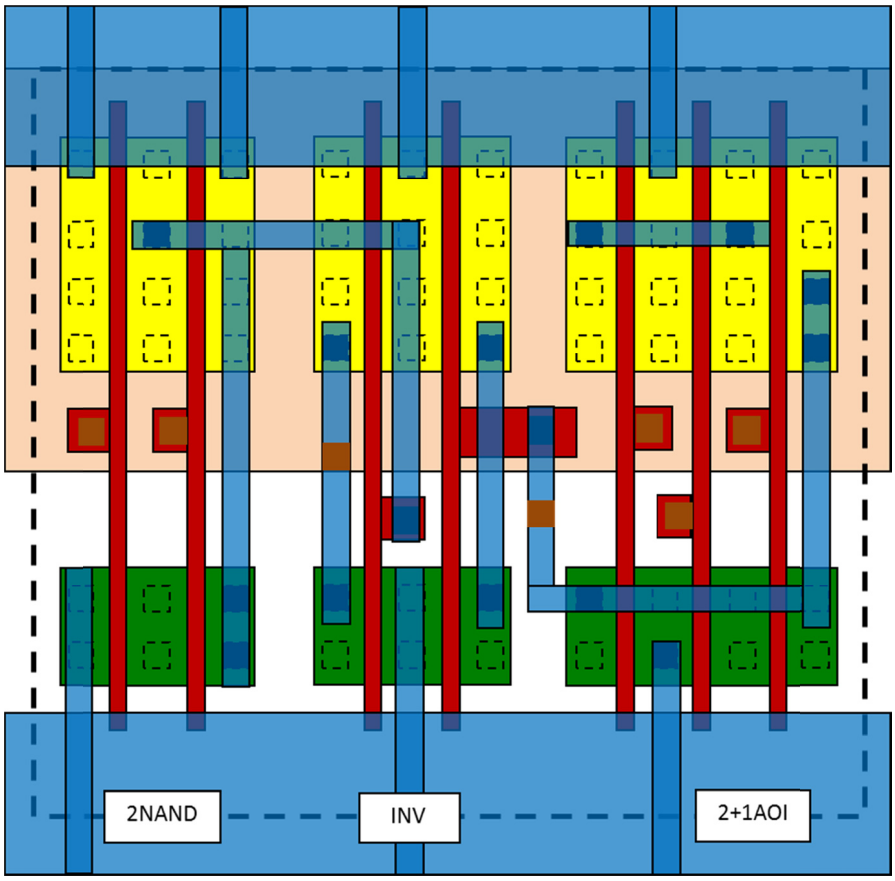
Minimum delay is obtained by taking the derivative w.r.t. m and setting it equal to 0.
Minimum delay is then obtained for $t_{d,buf} = \frac{rcL^2}{2m^2}$, i.e. for $m = L\sqrt{\frac{rc}{2t_{d,buf}}}$.

c) With RC=6 ps and rcL^2=0.1 pf*6.4kΩ =0.64 ns=640 ps, we obtain m=40/√30≈8 (even number preferred).

d) **Task for MCC090**:
Delay without repeaters: Complete delay expression according to Elmore delay model:
$t_d = RC + \frac{R_wC_w}{2} + RC_w + R_wC = 6 + 400 + 100 + 48 = 554$ ps.
Delay with repeaters:
$t_d = m\left(RC + \frac{R_wC_w}{2m^2} + R\frac{C_w}{m} + \frac{R_w}{m}C\right) = 6m + \frac{400}{m} + 100 + 48 = 48 + 50 + 148 = 246$ ps.
Conclusion: Propagation has been brought down to less than half. However, as my first guess I would have believed that repeater insertion should mean a larger delay reduction than that.

Solutions:

4. CMOS layout and dot operators. Dot operator logic cell contains 2AND and 21AO.



b) Area: 32*3.2*2.6=102,4*2.6=266 μm^2.

5. Power dissipation and driving large capacitances

a. Power dissipation: $P=fCV_{DD}^2$=100MHz*0.5pF*1V*1V=50 μW.

b. Because of long rise/fall times when driving large caps with small drivers there will be extra short-circuit power.

c. I would try with two buffers with a tapering factor f=$\sqrt[3]{100}$≈4.64. A reasonable value close to 4, the "magic number" (as in FO4 delay). I know by experience that optimum tapering factor is approximately 2.72<f<5.

d. We now have three inverters driving the output pad, they have input capacitances 5, 25 and 100 fF. Power dissipation in inverters is then: $P=fCV_{DD}^2$=100MHz*0.130pF*1V*1V=13 μW.
Total power dissipation 63 μW. Percentage: 13/63=20%.

6. Adders and path delay.

Neglecting parasitic delay, the important part of the propagation delay from the output of inverter A to the output of inverter C is given by the following expression:

$$t_d = f_B + \frac{4g}{f_B} + f_C + \frac{8g}{f_C}.$$

Minimum delay conditions are obtained by taking the derivatives w.r.t inverter tapering factors f_B and f_C, respectively. The results are f_B=√8=3 and f_C=√16=4.