Task 1: Basic skills here include the ability to translate a Boolean expression to the corresponding pull-up (PU) and pull-down (PD) networks. **"**Products" yield MOSFETs in series, while "sums" yield MOSFETs in parallel. MOSFETs in series in the PD-network correspond to MOSFETs in parallel in the PU-network. Second, the schematic is to be translated into a physical layout. Find the appropriate Euler paths for correct MOSFET ordering. Check that ordering is the same in schematic and layout; otherwise LVS will signal for errors. Check that correct nets are connected to the supply lines. Check that no nodes are left dangling.

Task 2A: a) Square-law means V_{IN}-V_T is divided by $\sqrt{4}$=2 for any V_{OUT}.

b) In the linear region $V_{OUT}(V_{DD})$ is divided by 4 (i.e. a linear relationship).

Why? In the saturation region we can write the VTC equation as

$$V_{OUT} = V_{DD} - kR_L\left(V_{IN} - V_T\right)^2 \times factor$$

At each output level V_{OUT}=xV_{DD}, we can rewrite to obtain $V_{IN} - V_T = \sqrt{\frac{(1-x)V_{DD}}{kR_L/2}} \times \frac{1}{\sqrt{factor}}$

In the linear region, at V_{IN}=V_{DD}, the output voltage can be obtained by voltage division

$$V_{OUT} = \frac{R_{ON}}{R_{ON}+R_L} = \frac{1}{1+G_{ON}R_L} \approx \frac{1}{G_{ON}R_L} \sim \frac{\text{revious value}}{factor}.$$

Task 2B: The required knowledge is knowing how to obtain the switching voltage of a CMOS inverter from equal currents through the nMOS and pMOS transistors, i.e. $I_{DSAT,N}$= $I_{DSAT,P}$, yielding

$$V_{SW} = \frac{V_{DD} + V_{TN} + \sqrt{x}V_{TN}}{1+\sqrt{x}}, \text{ where } x = k_N / k_P.$$

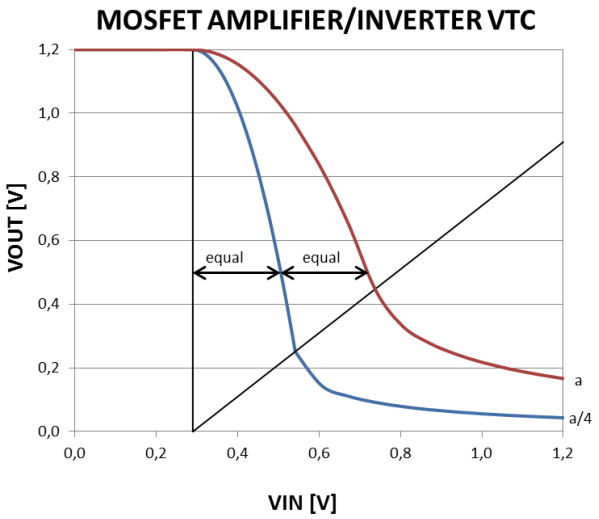
First, validate formula correctness concerning signs by checking that x=1 yields V_{sw}=V_{DD}/2. Second, reflect over what to expect. Will the switching voltage of a NAND gate be higher or lower than that of the inverter? Simple voltage division will give an indication.

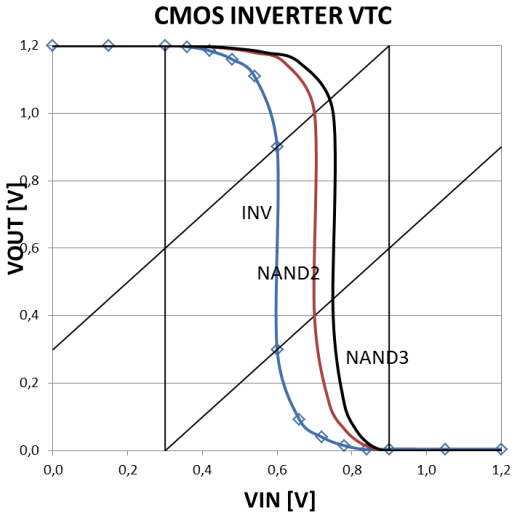
For a NANDX gate, the PU-network resistance will be R/X, while the PD-network resistance is XR. Voltage division would yield the following output voltage:

$$\frac{"V_{SW}"}{V_{DD}} = \frac{XR}{XR + R/X} = \frac{1}{1+1/X^2} \geq 1/2.$$

Hence, we expect V_{sw} to increase. (For NOR gates it will decrease.) Returning to the equation for the switching voltage derived above, we obtain the following results:

a) For a NAND2 gate x=1/4, yielding V_{sw}=7/12
b) For a NAND3 gate x=1/9, yielding V_{sw}=5/8.





Task 3. The AOI-gate has a logic "one" output for three of the eight input combinations, and a logic "zero" for the other five (AB=1 means two minterms, and C=1means another three minterms when the output is low). Hence, the probability for a logical 'one' output is given by P=3/8. Hence, the switching activity= $P(1\text{-}P)$=15/64. Please, note that the switching activity only refers to the output going high, thereby consuming power from the power supply, since the switching activity is to be used for calculating the power dissipation.

Task 4. a) **Voltage scaling:** Assume that a simple block delay model is given by

$$t_d = \frac{C_{A,eff}V_{DD}}{k_{A,eff}\left(V_{DD}-V_T\right)^2} + \frac{C_{B,eff}V_{DD}}{k_{B,eff}\left(V_{DD}-V_T\right)^2} \approx \frac{K}{V_{DD}} = \frac{4}{V_{DD}}.$$

Delay is 4 ns for the nominal supply voltage. Now, if we only need a propagation delay of 5 ns, the supply voltage can be reduced to 80%.

b) **Sizing.** For sizing we use a somewhat simplified model relating the switching energy and the sub-block delays,

$$E_{tot} = E_A + E_B = \frac{6}{t_A} + \frac{1}{t_B}.$$

If we limit the total block delay to 5 ns, t_A+t_B=5 ns, the total energy per operation is given by

$$E_{tot} = E_A + E_B = \frac{6}{x} + \frac{1}{5-x}.$$

Minimum energy is obtained by taking the derivatives

$$\frac{dE_{tot}}{dx} = -\frac{6}{x^2} + \frac{1}{(5-x)^2} = 0 \rightarrow \sqrt{6}(5-x) = x \rightarrow 3.45x = 2.45\times 5 \rightarrow x \approx 3.5$$

Hence, the two delays of blocks A and B are 3.5 ns and 1.5 ns, respectively.

c) By voltage scaling, switching energy is reduced by 1-0.8^2=36%. By sizing, switching energy is reduced from 3 pJ to about 2.4 pJ, i.e. by 20 %. Voltage scaling seems to be more efficient.

Task 5. Here we must use Elmore´s formula to estimate the repeater & wire delay

$$t_d = M\left[R\left(2C + \frac{C_w}{M}\right) + \frac{R_w}{M}\left(C + \frac{C_w}{2M}\right)\right] = 2MRC + RC_w + R_wC + \frac{R_wC_w}{2M}.$$

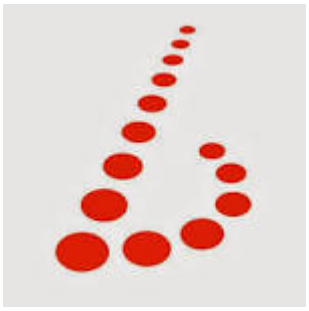
a) Let us start by determining the optimal M-value. Usually we solve this problem by taking the derivatives of this delay expression wrt M. However, in this case we are asked to solve the problem by equaling the two M-dependent terms since their product is constant!

$$2MRC = \frac{R_wC_w}{2M} \text{ since } 2MRC * \frac{R_wC_w}{2M} = \text{constant}; \Rightarrow M = \sqrt{\frac{R_wC_w}{4RC}}.$$

b) With optimal M-value , we obtain $2MRC = \frac{R_wC_w}{2M} = \sqrt{R_wC_wRC}$.

c) Second, determine the best R-value for minimum delay once optimal M-value has been chosen. Usually we solve this problem by taking the derivative of the delay expression wrt R. However, this time we are asked to solve the problem differently by equaling the two R-dependent delay terms: equaling the second and third terms in the Elmore delay expression equal yields RC_w=R_wC (the product is constant)

$$RC_w = R_wC \text{ yields } R = \frac{R_w}{M}\frac{C}{C_w}M = \frac{R_w}{M}\sqrt{\frac{R_wC}{4RC_w}} = \frac{R_w}{2M}.$$



d) In c) we have derived $RC_w=R_wC$. Multiply both sides by $RC_w \Rightarrow (RC_w)^2 = R_wC_wRC$. Similarly, multiply both sides with $R_wC \Rightarrow (R_wC)^2 = R_wC_wRC$. Hence, all four delay terms are equal, and the total delay is given by $t_{d,tot} = 4\sqrt{R_wC_wRC}$.

e) Brussels Airlines.

Task 6.

a) A good plan is to make the solution as simple as possible. One way would be to start by calculating the path effort $F=GHB$, and then to determine the optimal tapering factor, $f=\sqrt[5]{F}$. We can easily find the path electrical effort H=1, and the path branching factor B=2*4*8*16*32=2^15;
Determining the logical effort of the AO-gate to g=0.5, we find path logical effort G=1/32. Hence, ***F*=2^10**, and the **optimal tapering factor**, ***f*=$\sqrt[5]{F}$=4**.
The driving capability of an AO21 gates is twice that of a reference inverter, but the input capacitance is the same. Hence the logical effort of the AO21 gate is g=0.5 as already mentioned above. Hence, the stage electrical effort is h=8, since $f=gh$.

b) Parasitic delay P is not affected by optimization attempts. No need to calculate it at all.

c) From left to right (or vice versa) with h=8 we find the gate sizes: X2, X8, X16, X16, X8, X2. Validate last stage for instance: 32 X2-gates loading an X8-gate: h=32*X2/X8=8.

d) Total delay $d=P+5*4=P+20$ in the optimized case, while in a non-optimized case using X2-gates only, the total delay is given by $d=P+g*(2+4+8+16+32)=P+31$. Hence, there is a considerably gain in speed obtained by sizing the AO gates for optimal fanout and tapering.