Written examination for

MCC092 Introduction to Integrated Circuit Design

Thursday December 21, 2017, at 8.30-13.30 at the Mechanical Engineering building

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Staff on duty: Lena Peterson, D&IT, phone ext: 1822, or mobile 0706-268907. Lena will visit around 9.30 and 12.00.

Administration: Exams will be picked up after the exam. Send lists to CSE student administration office.

Allowed technical aids for students: This is a closed-book exam. Allowed aids: A Chalmers-allowed calculator (non graph-drawing) plus pencil, eraser, ruler, and dictionary (these are always allowed).

Results: The results from the examination will be sent to you via the Ladok system within three weeks. The grading review will take place Thursday January 18 12.30-13.30 in room 4128 at the CSE department.

Solutions: Solutions will be posted on the course web site in PingPong no later than Friday December 22. Any student who does not have access to the 2017 course web site can contact Lena Peterson (via e-mail to lenap@chalmers.se) to obtain the solutions.

Instructions:

- Write legibly.
- State any assumptions you make.
- Explain your reasoning and calculations (except when the problem says otherwise). Partial credits can be awarded, but if we do not understand you that is not possible.
- Number all pages and write your code on each page.
- Put only one problem per page.
- Do not write in red since that is the color used for the grading.

Good luck!

Grades:

The written examination contains six problems, each worth 10 points. You need 30 points to pass (grade "3"), at least 40 points for grade "4" and at least 50 points for grade "5". Bonus points from the fall 2016 course instance will be added before the higher grades are assigned.

Problem 1: Wire delays, adder delay and area

a) Consider a pair of 1 mm long wires where each wire has a capacitance of 0.08 fF/µm to ground and 0.12 fF/µm to its neighbor (the wire resistance is negligible). Each wire is driven by an inverter with an effective resistance of 10 kΩ. What is the delay of the path formed by one of the the drivers and its wire if that driver switches, while the other driver does not change. For simplicity neglect the parasitic capacitance of the inverter. (2 p)

b) Again consider the two wires with drivers in task a). What if the other driver switches too exactly at the same time? What will the delay of the original path be then? Consider the case when the two drivers switch in the same direction (from ground to V_{DD} or from V_{DD} to ground) and the case they switch in opposite directions. Find the resulting delays for the two cases. Discuss the implications of your findings on the delay calculations for buses. (4 p)

c) When using a synthesis tool to automatically map the addition operator, "+", to hardware, the tool will select the type of adder to meet the timing constraint while minimizing the area. One can make an experiment by synthesizing the same adder with tighter and tighter timing constraints and see what type of adder the tool selects and how large area the resulting adders occupy. Figure 1 shows the results of such an experiment carried out for both 32-bit and 64-bit adders. The used synthesis tool had these four types of adders available (listed in alphabethical order: (A) carry lookahead adders (B) carry-select adders (C) prefix adders (D) ripple-carry adders. Match the four types of adders with the four labels in graph of Figure 1. No motivation is required. (4 p)

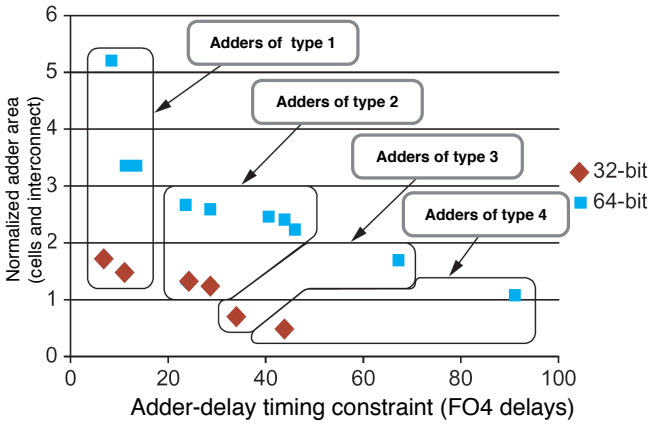

Figure 1: The resulting normalized area when synthesising a 32-bit and a 64-bit adder with different timing constraints. The four types of adders listed in alphabetical order are (A) carry lookahead adders (B) carry-select adders (C) prefix adders and (D) ripple-carry adders. But which one is which?

Problem 2: Static CMOS inverter static characteristics

The pMOS transistor performance has typically be the limiting factor in many applications. In digital circuits, its size has been twice that of the nMOS transistor for equivalent performance. Today, manufacturers of small feature-size CMOS processes use different tricks to improve the pMOS devices, which are of interest both in analog and digital applications.

In this task we have an inverter built in an unknown modern CMOS process. The pMOS transistor has twice the width of then nMOS, as we traditionally have seen in older processes such as the 65 nm process. The pMOS transistor here has a threshold voltage of $V_{Tp} = -0.15\,V$ and the nMOS transistor has a threshold voltage of $V_{Tn} = 0.2\,V$. In this process we have $V_{DD} = 0.8\,V$. For simplicity, lets assume that $k_n = k_p$ when the pMOS transistor is twice as wide as the nMOS transistor.

a) What is the switching voltage for the inverter with the above specified parameters? (4 p)

b) What should the width ratio between the nMOS and the pMOS transistors in the inverter be, in order to get a switching voltage that is equal to $V_{DD}/2$? (6 p)

Problem 3: Layout of standard cells

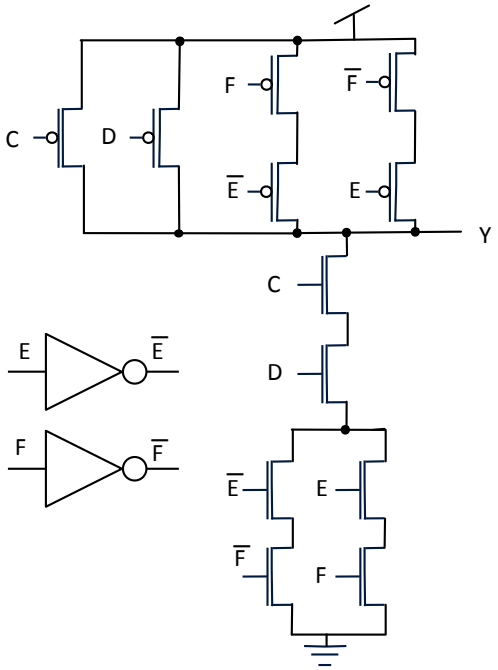

Figure 2: The schematic for a cell comprising one compound gate and two inverters.

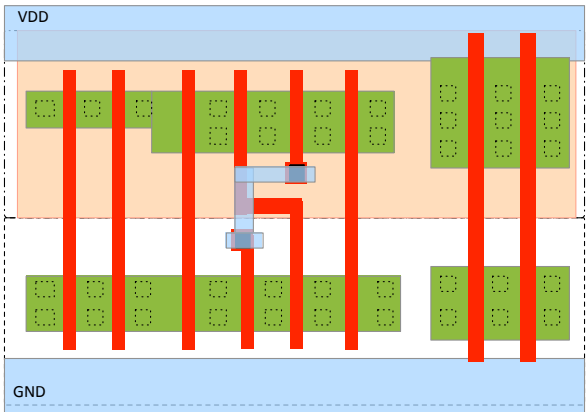

Figure 3: Layout template for task 3 a). The template is repeated twice on tear-off sheets at the end of the exam.

Consider the cell shown in Fig 2, comprising a compound gate and two inverters. Your task is to complete the layout using the template in Figure 3. As you can see from the template two poly lines have to cross for the layout to be possible with single-line-of-diffusion for both the n-net and p-net.

a) Draw the layout of the cell, while considering the best transistor sizing for equal worst-case resistance, and trying to minimize the parasitic capacitances at the output of the compound gate. Each of the four inputs, C, D, E and F should only have to be connected by the router to one point within the cell. Try to use only metal-1 for your connections so that metal-2 can be used freely by the router. If absolutely necessary you may use metal-2, but there will be a 3-point deduction if you do so. You are allowed to change the order of the E and F transistors as necessary to complete the layout. (8 p)

b) What is the parasitic delay for your layout of the compound gate? Calculate the parasitic delay also from the schematic shown in Figure 2 and compare the two results. (2 p)

Problem 4: Sequential circuits **NOTE! If you are taking this exam for the old course, MCC091, you can select to solve problem 7 instead of this problem.**

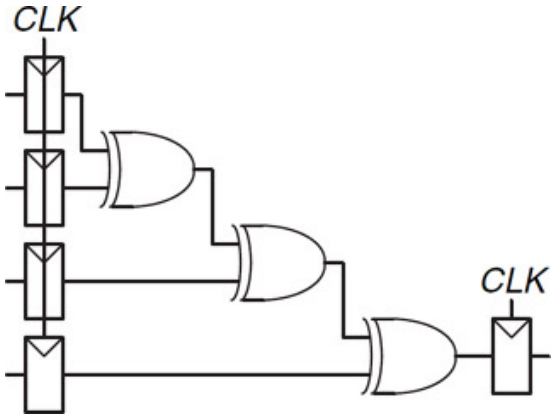

Figure 4: The four-input XOR gate with registers at the input and outputs that Ben designed.

Ben has designed the circuit shown in Figure 4 to compute a registered four-input XOR function. Each two-input XOR gate has a propagation delay, t_{pd}, of 100 ps and a contamination delay, t_{cd} of 55 ps. Each flip-flop has a setup time, t_{setup} of 60 ps, a hold time, t_{hold} of 20 ps, a clock-to-Q propagation delay, t_{pcq}, of 70 ps, and a clock-to-Q contamination delay, t_{ccq}, of 50 ps.

a) If there is no clock skew, what is the maximum operating frequency of the circuit? (2 p)

b) How much clock skew can the circuit tolerate if it must operate at 2 GHz? (2 p)

c) How much clock skew can the circuit tolerate before it might experience a hold time violation? (2 p)

d) Alice points out that she can redesign the combinational logic between the registers to be faster and tolerate more clock skew. Her improved circuit also uses three two-input XOR gates, but they are arranged differently. What is her circuit? What is its maximum frequency if there is no clock skew? How much clock skew can the circuit tolerate before it might experience a hold time violation? (4 p)

Problem 5: Delay, power and scaling

A microprocessor was fabricated in an old 90 nm CMOS technology. This microprocessor operated at 3.8 GHz with a 1.2 V supply and a 100 W power dissipation A dual-core microprocessor was also to be designed in the same technology, by duplicating the single-core design.

a) What would be the frequency and supply voltage for the dual-core design if the same size of the heat sink is to be maintained, that is if $P_{\text{DUAL\_CORE}} = P_{\text{SINGLE\_CORE}}$? Assume that all the power dissipation is due to dynamic (switching) power, and, for simplicity, assume that the frequency of operation is linearly proportional to the supply voltage. (3 p)

b) When the single-core design from above is moved to a newer 45 nm technology node, what would be its power and frequency of operation with a 0.8 V power supply? Assume Dennard scaling for all parameters except the power supply. (3 p)

c) Now consider the following what-if situation: assume that 10% of the 100 W total power dissipated by the single-core processor in task a) was due to static (leakage) power and that 90% was due to dynamic switching power. Furthermore, in the 45 nm process the standard threshold voltage (svt) is almost 100 mV lower than in the 90 nm process, yielding an eight-fold increase in leakage current at room temperature. What would be the total power dissipation of the single-core processor when transferred to the 45 nm process? How many percent would be leakage power? (4 p)

Problem 6: Faster adders, path-delay optimization

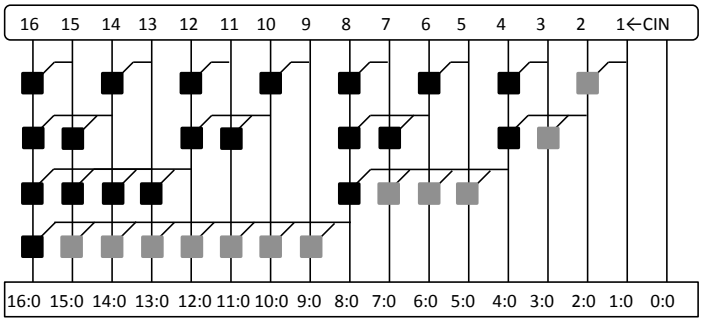

Figure 5: The Sklansky 16-bit PG tree.

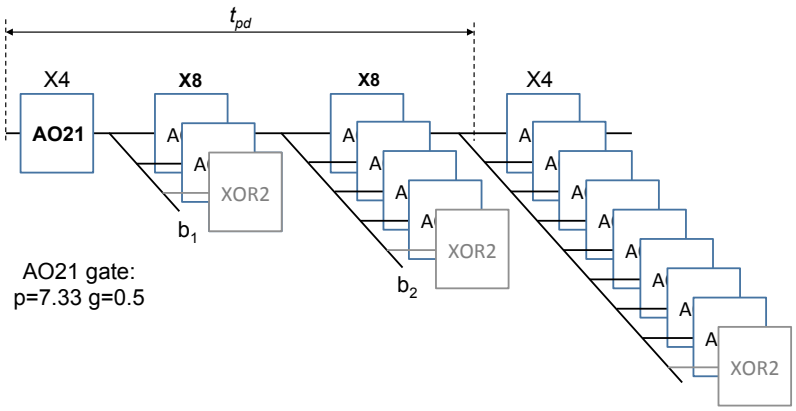

Figure 6: The Sklansky tree for calculating the group generate signals with the optimal sizes for the AO21 cells derived by Kjell and data for the AO21cell.

Consider the 16-bit Sklansky adder PG tree shown in Figure 5. Kjell derived the optimal sizes for the AO21 (and-or 2-1) cells that are used to form the group generate signals in this tree. See Figure 6 for the equivalent circuit of the tree with the optimal sizes which Kjell derived while disregarding the sum XOR gates. Each AO21 cell is made up of one and-or-invert 2-1 gate and one inverter. But what if we use invertering cells in the tree instead? Would the delay be shorter then? This is the question you are to investigate in this problem.

In the circuit you are to investigate every other gate in the tree is an and-or-invert 2-1 gate (AOI21 for short) and every other an or-and-invert 2-1 gate (OAI21 for short). Of course the sum gates will have to keep track of which signals are inverted, but that is not a huge complication.

a) Calculate the delay, t_{pd}, of the original tree using AO21 gates, with the sizes and the parasitic delay and logical effort values shown in Figure 6. The sum XOR gates should be completely disregarded! (2 p)

b) The AOI21 gate is shown in Figure 7. But you also need the OAI21 gate in your tree. Draw the circuit diagram for that gate and calculate its logical effort for the input that is the critical one in the Sklansky tree and its parasitic delay. (2 p)

c) With inverting cells in the tree, calculate the path effort and use it to find the optimal stage effort. As Kjell did, you should entirely disregard the sum XOR gates! (4 p)

d) What is the resulting delay with the optimal efforts you calculated in task c)? Is it shorter than the one the one you calculated in task a)? Discuss the results. (2 p)

AOI21 gate:
p=2.33, $g_{B,C}$=2

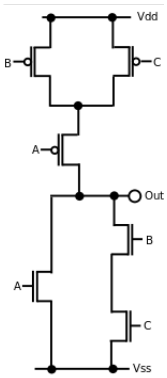

Figure 7: The and-or-invert 2-1 gate.

Problem 7: Amplifiers **This problem is only for students who are taking this exam for the old course MCC091 which ran until fall term 2015.**

An often used measure of how efficient an amplifier uses its power (that is its bias current) is the g_m over I_D ratio: g_m/I_D, which is the transconductance divided by the bias drain current.

a) Derive an expression for the transconductance for an nMOS transistor operating in saturation and above threshold. (2 p)

b) What it the simplest approximation of for g_m/I_D above threshold? (2 p)

c) Below threshold the drain-to-source current depends exponentially on V_{GS}. The equation for the current is:

$$I_D = I_{\text{OFF}} e^{\frac{V_{GS}}{nV_{TH}}}$$

where V_{TH} is the thermal voltage (around 25 mV at room temperature) and the parameter n is a constant that is usually around 1.5. Derive an expression for the transconductance below threshold. (2 p)

d) Find an expression for g_m/I_D below threshold. (2 p)

e) Draw a sketch of g_m/I_D as a function of V_{GS} above and below threshold. (2 p)

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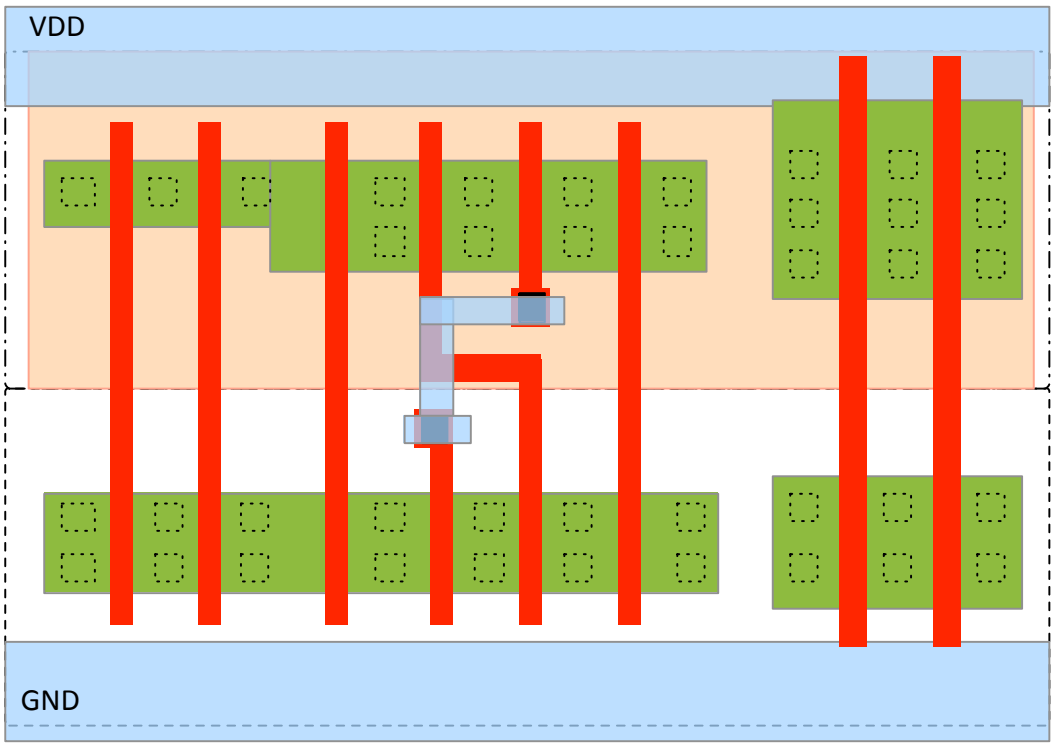
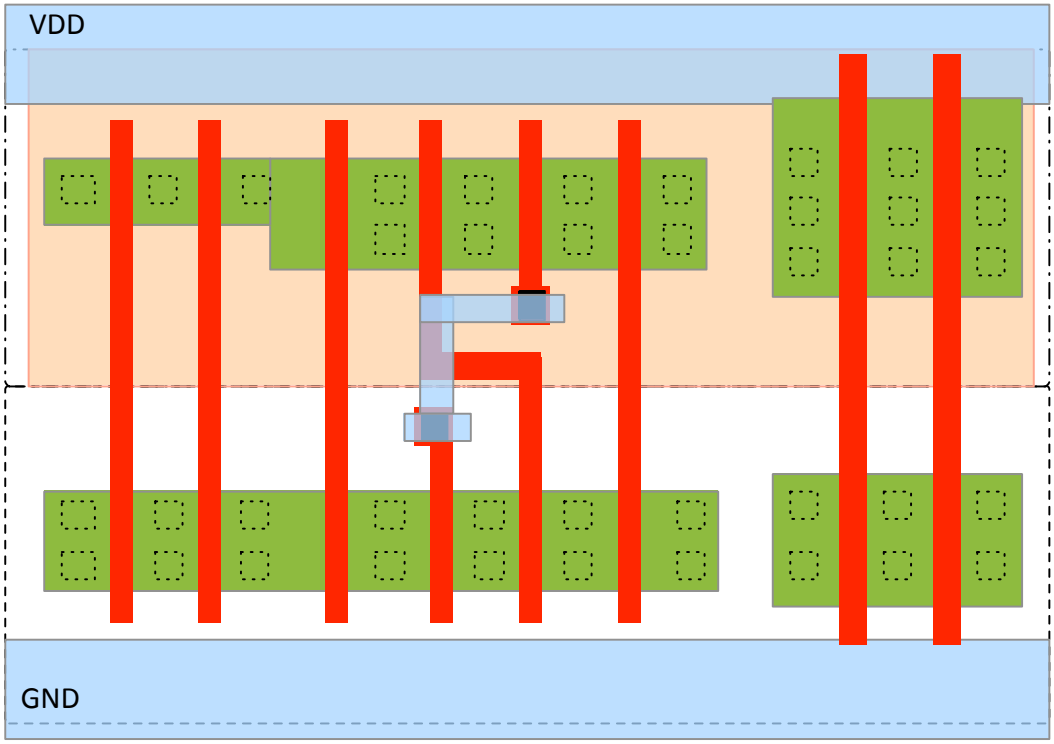
MCC092 2017-12-21 Tear-off page for task 3 a). Write your anonymous code here:



MCC092 2017-12-21 Tear-off page for task 3 a). Write your anonymous code here:



Solution for written examination for

MCC092 Introduction to Integrated Circuit Design, December 21, 2017

Solutions are not done yet.

Solution 1: Wire delays, adder delay and area

a) We find the capacitance to ground for each wire to be $C_{\text{gnd}} = 0.08\,\text{fF}/\mu\text{m} \times 1000\,\mu\text{m} = 80\,\text{fF}$ and similarly the capacitance to the neighboring wire $C_{\text{adj}} = 0.12\,\text{fF}/\mu\text{m} \times 1000\,\mu\text{m} = 120\,\text{fF}$. The delay is $0.7RC_{\text{eff}}$. When the neighboring wire sits still (regardless of if it sits at V_{rmDD} or at ground) we have $C_{\text{eff}} = C_{\text{gnd}} + C_{\text{adj}}$. Thus, the resulting propagation delay is:

$$t_{pd1} = 0.7 \times 10\,\text{k}\Omega \times 200\,\text{fF} = 1.4\,\text{ns}. \tag{1}$$

b) When the two wires switch simultaneously in the same direction the voltage across the capacitance between the wires, C_{adj}, will be constant (and equal to 0) all the time. Thus, this capacitance will not be recharged and will consequently have no effect on the delay. So we have $C_{\text{eff}} = C_{\text{gnd}}$ and

$$t_{pd2} = 0.7 \times 10\,\text{k}\Omega \times 80\,\text{fF} = 0.56\,\text{ns}. \tag{2}$$

When the two wires are switched in opposite directions the voltage across C_{adj} goes from V_{DD} to $-V_{\text{DD}}$ (or the other way around). The voltage swing across C_{adj} is thus $2V_{\text{DD}}$. Thus, the effect on the driver is (at least approximately) as if the capacitance had been twice as large and connected to ground but being switched only with a voltage swing of V_{DD}. This is the so called Miller effect, which you may have heard of if you have taken any course on analog design. The resulting capacitance in this case is thus $C_{\text{eff}} = C_{\text{gnd}} + 2C_{\text{adj}}$. And the delay is computed as:

$$t_{pd3} = 0.7 \times 10\,\text{k}\Omega \times 320\,\text{fF} = 2.24\,\text{ns}. \tag{3}$$

In conclusion we find that for this system of two wires we have the longest delay, the propagation delay, as t_{pd3} and the shortest delay, the contamination delay is t_{pd2}. When you design a system with a bus you have to carefully design test vectors for when you calculate the delays and when you simulate the system.

c) See Figure 8.

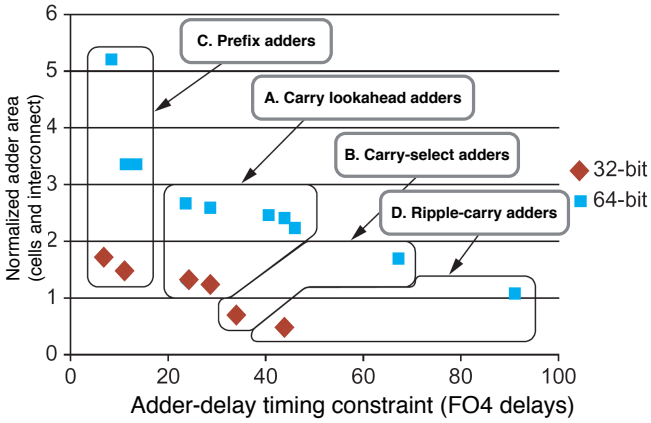


Figure 8: Solution to task 1 c). The types of adders in the synthesis experiment.

Solution 2: CMOS inverter static characteristics

a) Solution is $V_{sw} = 0.425\,\text{V}$.

b) The expression for the ratio is: $x = \frac{2}{\left(\frac{0.4+V_{th,p}}{0.4-V_{th,n}}\right)^2}$. With the values we have in this task we find that the pMOS transistor should be 1.28 times wider than the nMOS transistor. These are the detailed steps for finding the solution:

$$0.4 = \frac{0.8 + V_{th,p} + \sqrt{\frac{\mu_n w_n}{\mu_p w_p}} V_{th,n}}{1 + \sqrt{\frac{\mu_n w_n}{\mu_p w_p}}} = \frac{0.8 + V_{th,p} + \sqrt{\frac{\mu_n w}{\frac{\mu_n}{2} wx}} V_{th,n}}{\sqrt{\frac{\mu_n w}{\frac{\mu_n}{2} wx}}} \tag{4}$$

$$0.4(1 + \sqrt{\frac{2}{x}}) = 0.8 + V_{th,p} + \sqrt{\frac{2}{x}} V_{th,n} \tag{5}$$

$$\sqrt{\frac{2}{x}}(0.4 - V_{th,n}) = 0.8 - 0.4 + V_{th,p} = 0.4 + V_{th,p} \tag{6}$$

$$\frac{2}{x} = \left(\frac{0.4 + V_{th,p}}{0.4 - V_{th,n}}\right)^2 \tag{7}$$

$$x = \frac{2}{\left(\frac{0.4+V_{th,p}}{0.4-V_{th,n}}\right)^2} \tag{8}$$

Solution 3: Layout of standard cells

a) See Figure 9

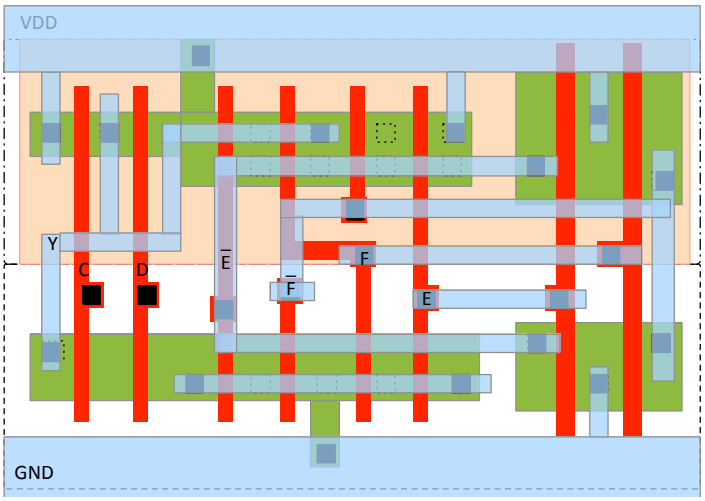


Figure 9: One solution for task 3 a). The layout could be further compacted to reduce the parasitic capacitances of the output node and also other circuit nodes.

b) From the schematic we find that the parasitic delay is $p_{\text{schem}} = \frac{4+2+2+4+4}{3} = \frac{16}{3}$ with the sizing for equal worst-case resistance in all branches. In the layout we can share diffusion areas in the p-net. Thus, the resulting parasitic delay is $p_{\text{layout}} = \frac{4+2+4}{3} = \frac{10}{3}$. We reduce the parasitic delay by 3/8 or 37.5 by using a smart layout.

Solution 4: Sequential logic

a) The sequencing overhead is $t_{pcq} + t_{\text{setup}}$. The propagation delay for the 4-input XOR gate is $3t_{pd}$. Thus, we find

$$T_{\text{clk}} = t_{pcq} + t_{\text{setup}} + 3t_{pd} = 430\,\text{ps} \tag{9}$$

And we have

$$f_{\text{clk}} = \frac{1}{T_{\text{clk}}} = 2.32\,\text{GHz} \tag{10}$$

b) A clock frequency of 2 GHz corresponds to a clock period of 500 ps. The difference from the calculalted clock period from task a) is thus 70 ps. So we find $t_{\text{skew}} = 70\,\text{ps}$.

c) A hold violation occurs when the input to register changes before is has been properly "locked in" or "held". We have

$$t_{\text{shortest}} = t_{ccq} + 3t_{cd} = 215\,\text{ps} \tag{11}$$

while we have

$$t_{\text{hold}} = 20\,\text{ps} \tag{12}$$

So the here we find $t_{\text{skew}} = 215\,\text{ps} - 20\,\text{ps} = 195\,\text{ps}$.

d) If you arrange the three XOR gates in a tree structure we reduce the delay from three XOR delays to two XOR delays. This is good for the setup violation where the longest delay, the propagation delsy, becomes shorter than before, $2t_{pd}$ instead of $3t_{pd}$ However, the shortest delay, the contamination delay, is also shorter than before: $2t_{cd}$ instead of $3t_{cd}$. This makes the hold violation requirement harder to fulfil. So we find:

$$T_{\text{clk}} = t_{pcq} + t_{\text{setup}} + 2t_{pd} = 330\,\text{ps} \tag{13}$$

The maximum clock frequency is thus:

$$f_{\text{clk}} = \frac{1}{T_{\text{clk}}} = 3.03\,\text{GHz} \tag{14}$$

The margin to setup violation has increased with t_{pd} to $t_{\text{skew}} = 170\,\text{ps}$. For the hold violation we find

$$t_{\text{shortest}} = t_{ccq} + 2t_{cd} = 160\,\text{ps} \tag{15}$$

while we have

$$t_{\text{hold}} = 20\,\text{ps} \tag{16}$$

So the here we find $t_{\text{skew}} = 160\,\text{ps} - 20\,\text{ps} = 140\,\text{ps}$. So now it is the hold requirement that limits the clock skew.

Solution 5: Delay, power and scaling

a) The specification $f = \alpha V_{\text{DD}}$ means we have $P_{\text{dyn}} = C \times V_{DD}^3$. We also know that the dual-core will have twice the capacitance of the single core. So then $P_{DUAL-CORE} = P_{SINGLE-CORE}$ means

$$2C(xV_{\text{DD}})^3 = CV_{\text{DD}}^3, \tag{17}$$

where x is the scale factor. Hence we get $x = \frac{1}{\sqrt[3]{2}} \approx \frac{1}{1.26}$. Thus, the new supply voltage has to be $V_{\text{DD}} = \frac{1.2}{1.26} \approx 0.95\,\text{V}$.

b) The scaling is from 0.90 to 0.45 µm, that is $S = \frac{1}{2}$.

If frequency scales as V_{DD} it becomes $3.8 \times \frac{0.8}{1.2} = 2.53\,\text{GHz}$.

Power: the capacitance is scaled to a fourth since it scales as S^2 so the new power is $P_{\text{dyn}_{\text{new}}} = \frac{P_{\text{dyn}_{\text{old}}}}{4}(\frac{0.8}{1.2})^3 = \frac{100}{4}(\frac{0.8}{1.2})^3 \approx 7.4\,\text{W}$.

c) We now assume 10 W of static power and 90 W of dynamic power to begin with. 10 W of static power at $V_{\text{DD}} = 1.2\,\text{V}$ corresponds to a leakage current of 8.3 A. A eight-fold increase of the static leakage current would mean a 66 A leakage current, and hence, 52.8 W of static power at $V_{\text{DD}} = 0.8\,\text{V}$. The dynamic power was originally 90 W, and becomes $0.074 \times 90 = 6.66\,\text{W}$ in the new technology, when we use the reduction factor we already calculated in task b). The new total power dissipation is close 60 W, but now the static power is almost 90% - reversal from before. Obviously, the leakage has to be reduced when processes are scaled down.

Solution 6: Faster adders, path delay optimization

a) The normalized delay for the three optimized stages are:

$$d = \sum p + 2 + 2 + 2 = 3 \times 7.33 + 6 \approx 28 \tag{18}$$

b) An OAI gate will later be shown in a figure here. It has the logical effort $g_{BC} = 2$ and the parasitic delay $\frac{8}{3} = 2.67$. Thus the path effort is

$$F = G \times B \times H = 2^3 \times 2 \times 4 \times 8 = 256 \tag{19}$$

The optimal stage effort is thus $\sqrt[3]{512} = 8$.

c) The normalized delay with theses stage efforts is

$$d = \sum p + 3 \times 8 = 2.33 + 2.67 + 2.33 + 24 = 31.33 \tag{20}$$

Interestingly, the resulting sizes are the same as in Figure 6. This is because stages with electrical efforts $g = 0.5$ and stage efforts $f = 2$ will result in the same electrical efforts, h, as stages with electrical efforts $g = 2$ and stage efforts, $f = 8$. Still the solution with more logic levels is a bit faster which is a bit surprising.

Solution 7: Amplifiers

This solution will be added later.