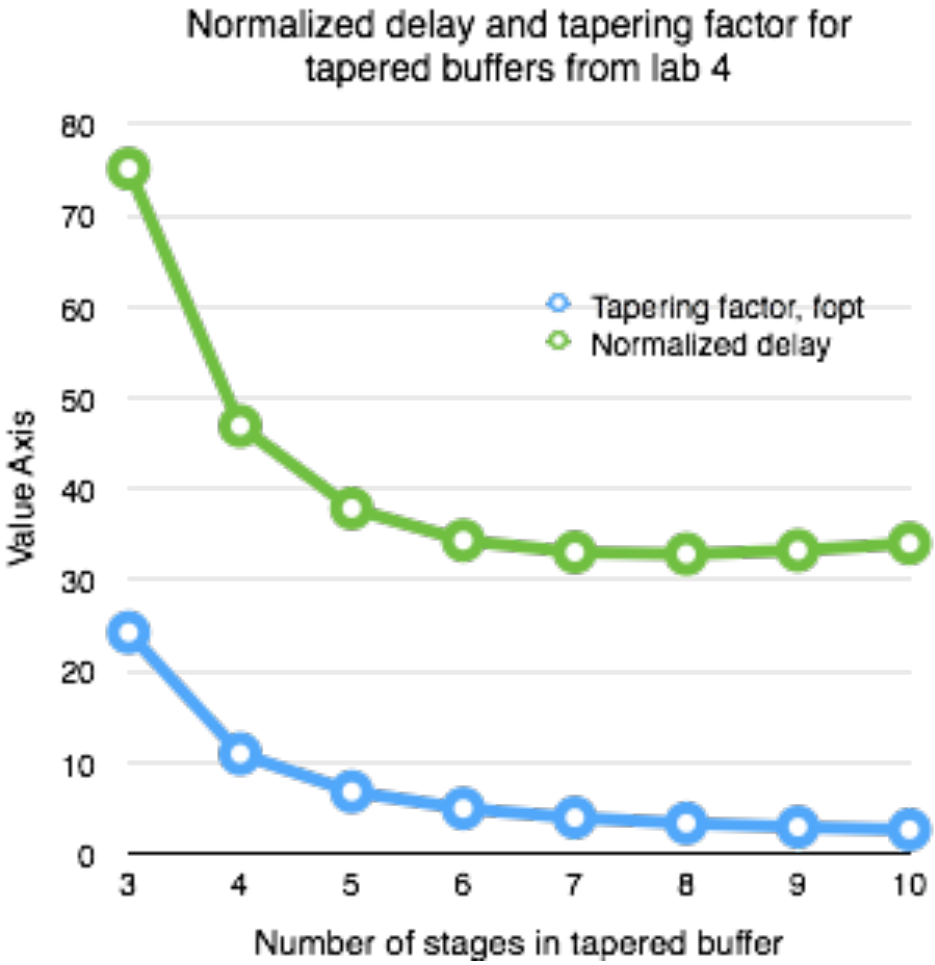
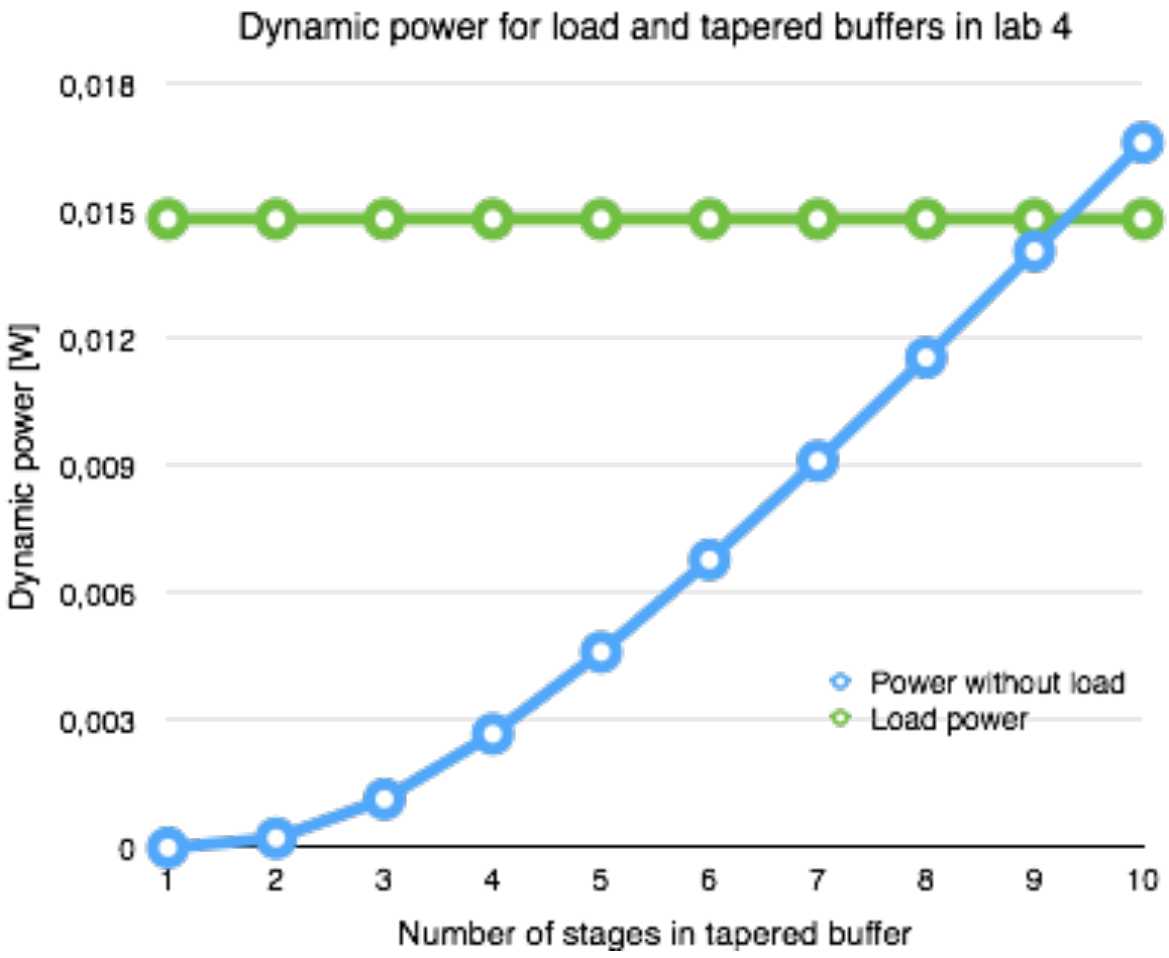
Feedback on hand-in problem set 2
Feedback on muddy issues
Adder delay optimization

Hand-in problem set 2

Task 1. The tapered buffer



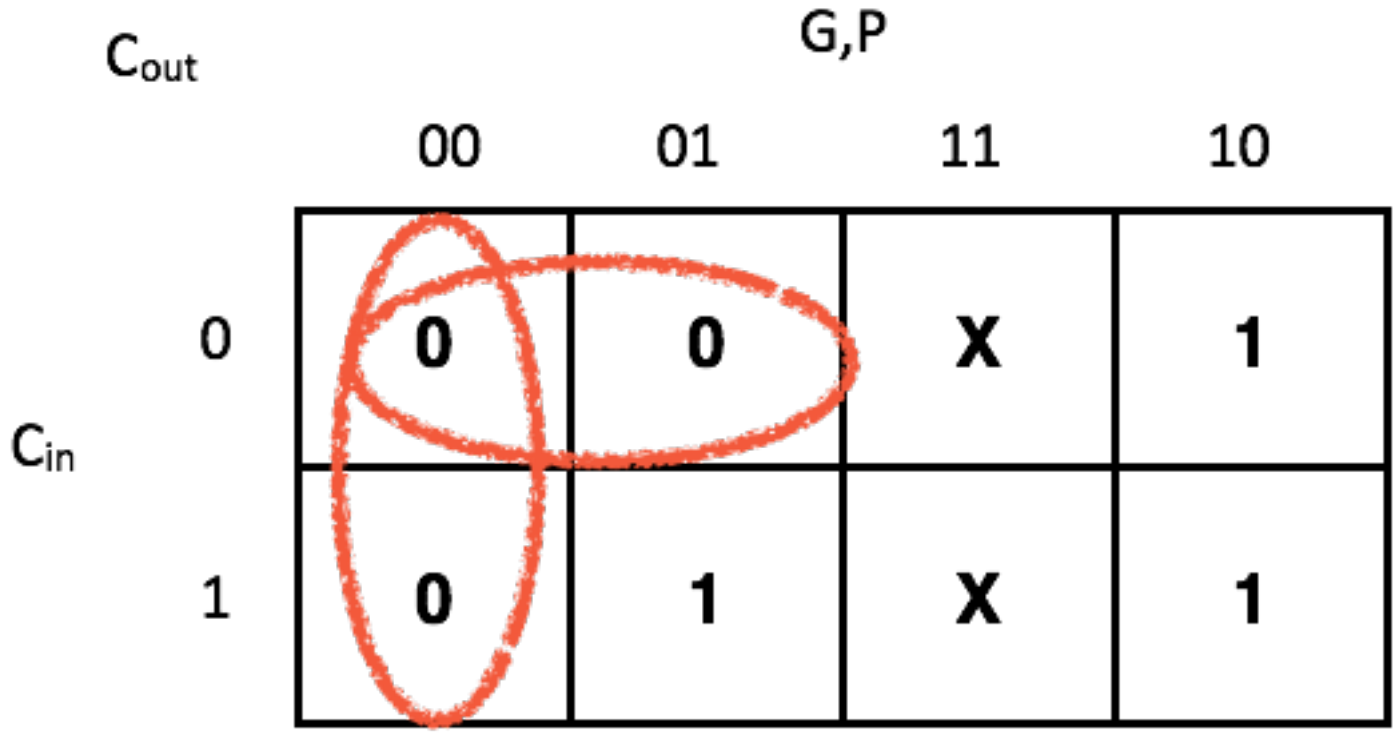
Task 1. The tapered buffer



Task 1. The tapered buffer

- The majority of you did not draw any conclusions in task e)!
  - Why not?
  - That is the most important thing!
  - I promise there will be some task like that in the exam.
  - I promise you that life will be that way!

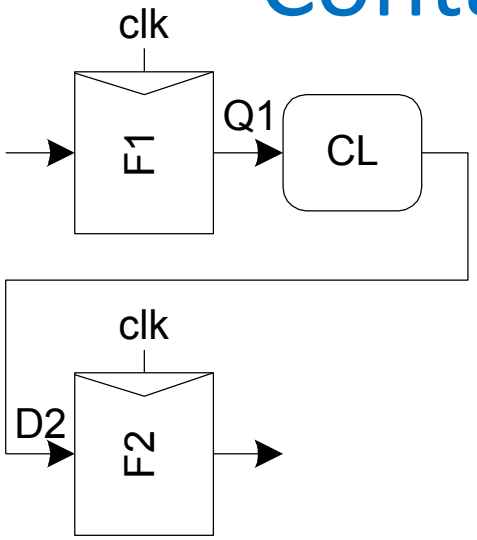
Task 4. Still some confusion about inversion

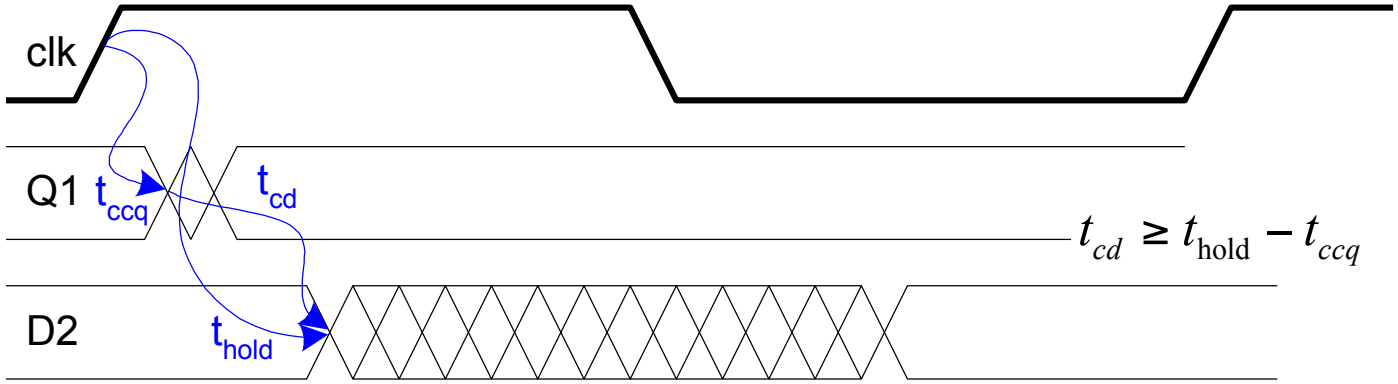


MUD cards

- Hold violation
  - Tpd too short? How can it be too short?
  - The gap between tpcd and tc.
- Metastability
  - Metastability window, when input goes close to clock edge
  - Regarding rate and exit time
  - Derivation still not clear.
  - Graphical representation in logarithmic scale
  - Does metastability occur between contamination delay and propagation delay?
  - The probabilities for entering metastability and failure etc. The exact equations
  - How to decrease the probability metastable entry and exit window in complex gates.
  - What is probability to enter and to exit?
  - How to avoid or detect failure to synchronize.
- Other
  - There should be more problems to solve on metastability.
  - Names, notation of signals seem rather inconsistent.

Minimum ~~Propagation~~ Delay
Contamination delay





- MTBF is a time
  - It is how long time it will take on average between errors
  - 1/MTBF is the frequency of errors
  - MTBF depends on fundamental properties of the systems that operate.

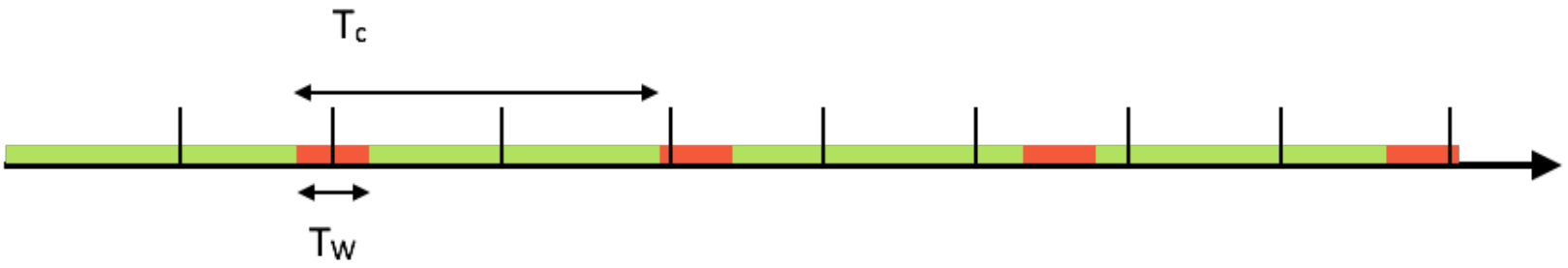
Entering metastability

- Now and then the unsynchronized input changes. It happens "randomly", f_D times per second.
- The sensitive time window for a flipflop is T_w long. This window is repeated once every clock cycle.
- The number of clock cycles per second is f_c.
- How many times per second do the data transitions occur when the flipflop is in its sensitive time window?

$$Rate = f_D T_W f_c$$

Entering metastability

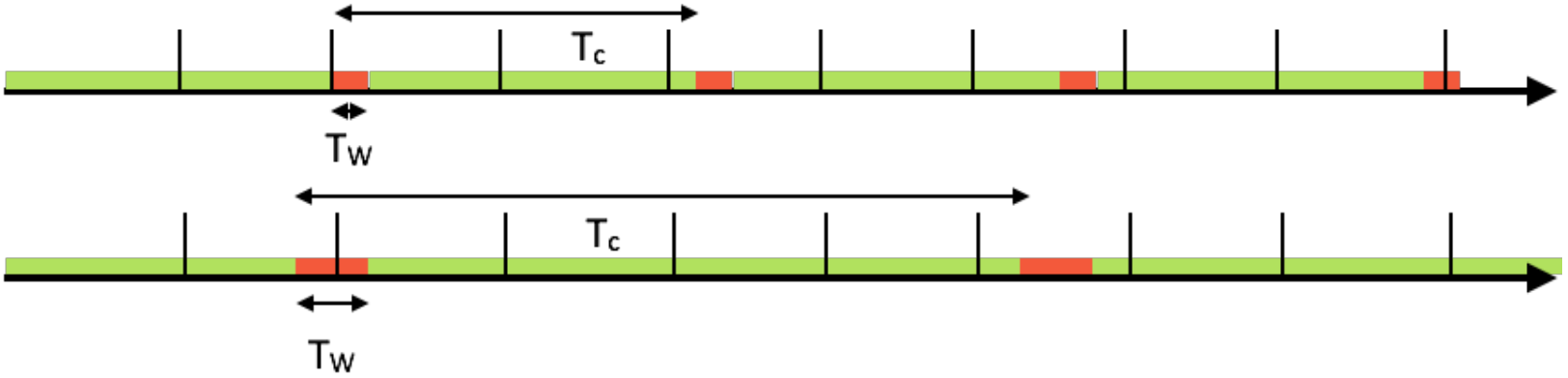
A flip-flop has a sensitive time window around the time when the clock edge happens: T_W
It happens once every clock cycle, T_c, or with a rate of f_c



Then asynchronous events/signals arrive at any time with a rate of f_D

Some times they hit the sensitive time windows, sometimes they don't.

Two ways to lower rate of entering: Faster flip-flops or lower clock frequency



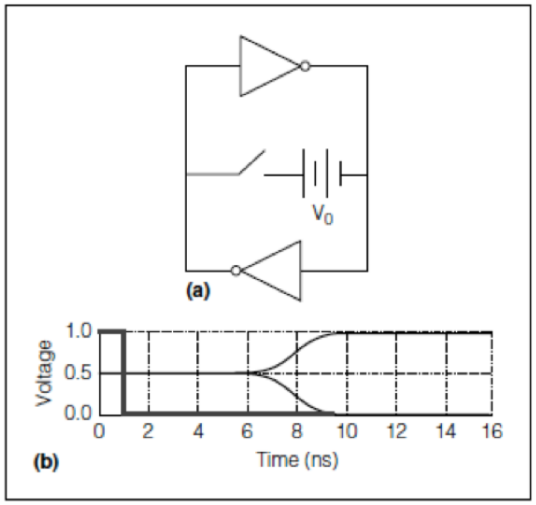
Entering metastability

- To lower the rate of entering we can:
  - Use a flipflop that has a shorter Tw time.
    - In principle a faster flip-flop.
  - Lower the clock frequency.
    - So that the Tw window does not occur so often.
  - Maybe make the input change less often.

Exiting metastability

- The rate of exiting depends exponentially on how long we wait, that is the allowed resolution time.
- So if we just can wait long enough the rate of getting an error will decrease a lot (1/MTBF)
- Or another way to put it is MTBF will increase exponentially with the time we wait.

Exiting



$$V_1 = V_0 e^{\frac{t_m}{\tau}}$$

$$t_m = \tau \ln\left(\frac{V_1}{V_0}\right)$$

Time to exit depends logarithmically on V_0 but not on the end voltage V_1 which is fixed.

V_0 is unknown. But probabilistic analysis shows that if latch is metastable at time 0 the probability that it remains metastable at time *t* is:

$$e^{-\frac{t}{\tau}}$$

Failure rate / MTBF

S: is the allotted synchronization time

Failure is to remain metastable after this time

$$Rate(failures) = T_W f_D f_c e^{-\frac{S}{\tau}}$$

$$MTBF = \frac{e^{\frac{S}{\tau}}}{T_W f_c f_D}$$

Parameters

- Flipflops characteristics:
  - T_W and τ
- System characteristics:
  - fc and (to some extent) f_D
- What we have to play with:
  - S: the allotted synchronization period

En example – determine required S (here called t_r)

$$MTBF\ (t_r) = \frac{\exp\left(t_r / \tau\right)}{T_o f\ a}$$

MTBF = 1000 yrs.
F = 25 MHz
a = 100 KHz
t_r = ?

Device	τ (ns)	T_o (s)	t_r (ns)
74LS74	1.50	$4.0 \cdot 10^{-1}$	77.71
74S74	1.70	$1.0 \cdot 10^{-6}$	66.14
74S174	1.20	$5.0 \cdot 10^{-6}$	48.62
74S374	0.91	$4.0 \cdot 10^{-4}$	40.86
74F74	0.40	$2.0 \cdot 10^{-4}$	17.68
PALC16R8-25	0.52	$9.5 \cdot 10^{-12}$	14.22*
PALC22V10B-20	0.26	$5.6 \cdot 10^{-11}$	7.57*
PALCE22V10-7	0.19	$1.3 \cdot 10^{-13}$	4.38*
7300-series CPLD	0.29	$1.0 \cdot 10^{-15}$	5.27*
9500-series CPLD	0.17	$9.6 \cdot 10^{-18}$	2.30*

Example due to Peter Cheung, Imperial college

How to avoid metastability

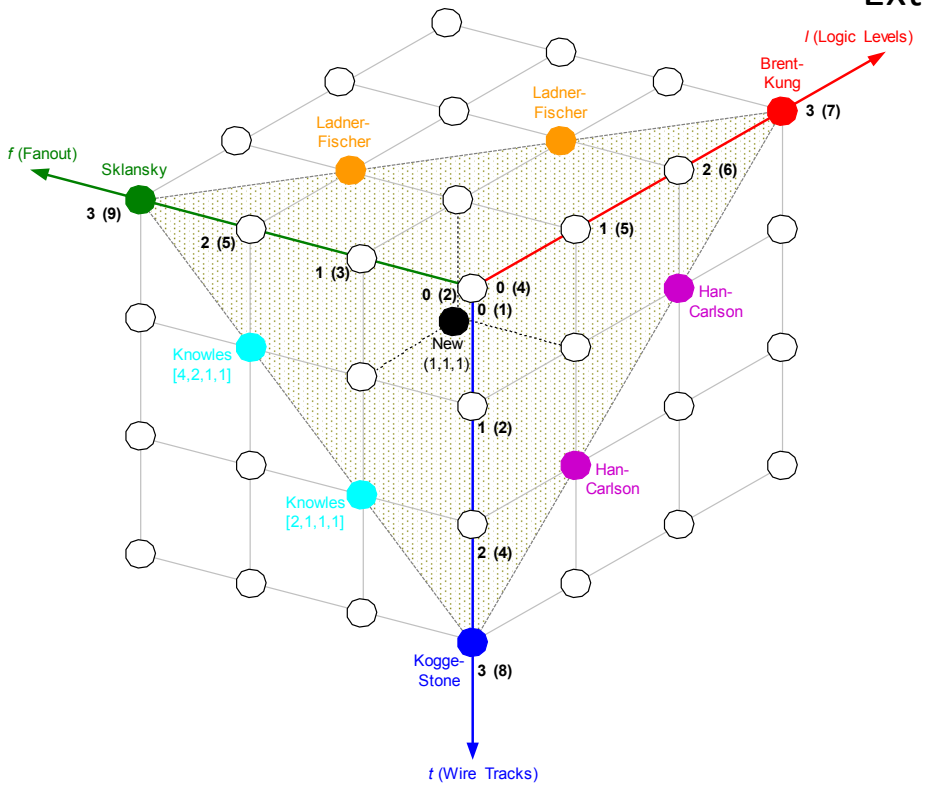
- Entering:
  - Use fast flipflops and clock them with as low clock frequency as possible.
  - Keep data rate of incoming signal as low as possible.
- Exiting:
  - Allot “long enough” synchronization period S.
  - Use well-designed synchronizers.
- What is “long enough” MTBF?
  - Note that with many units MTBF decreases!

More about tree adders

Tree Adder Taxonomy

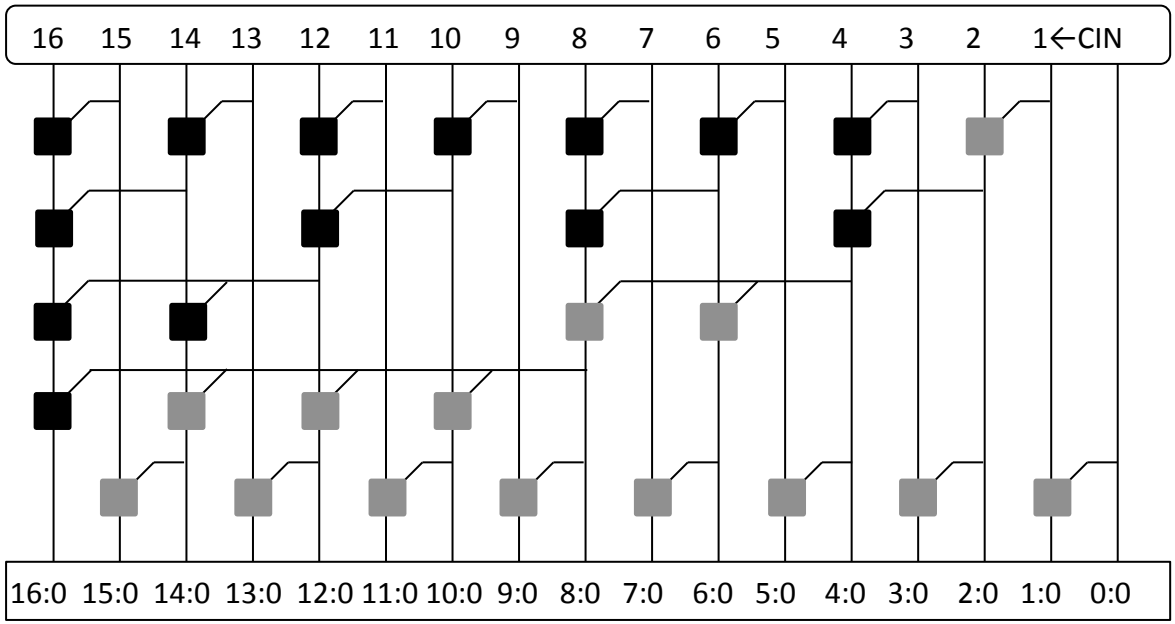
Extra logic levels

Extra fanout



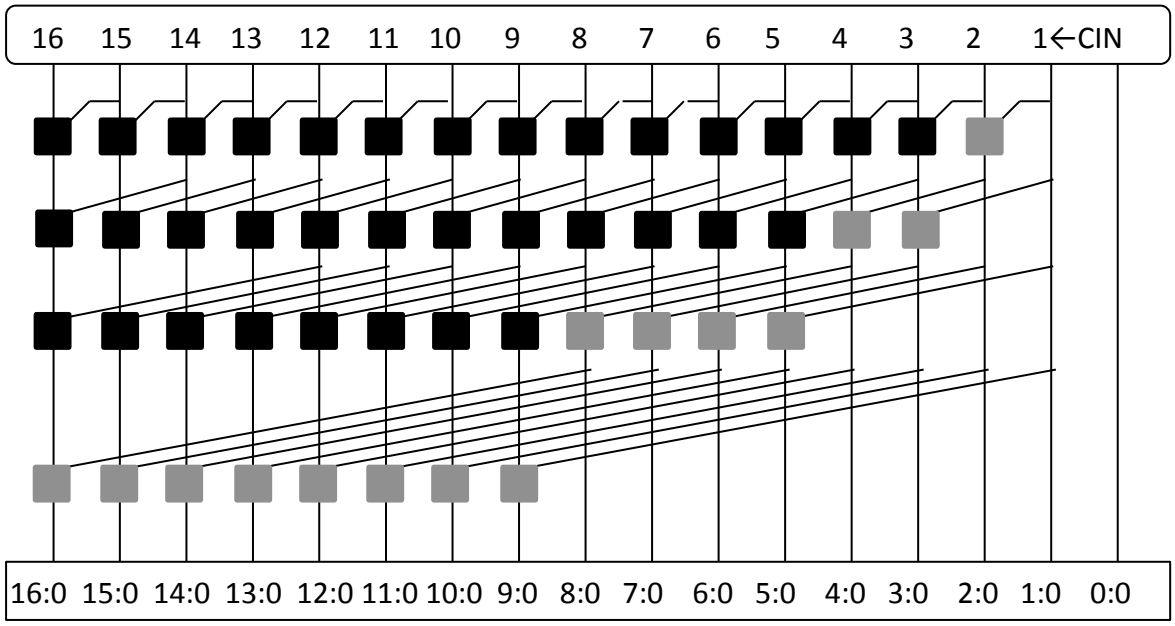
Extra wire tracks

Ladner-Fischer adder



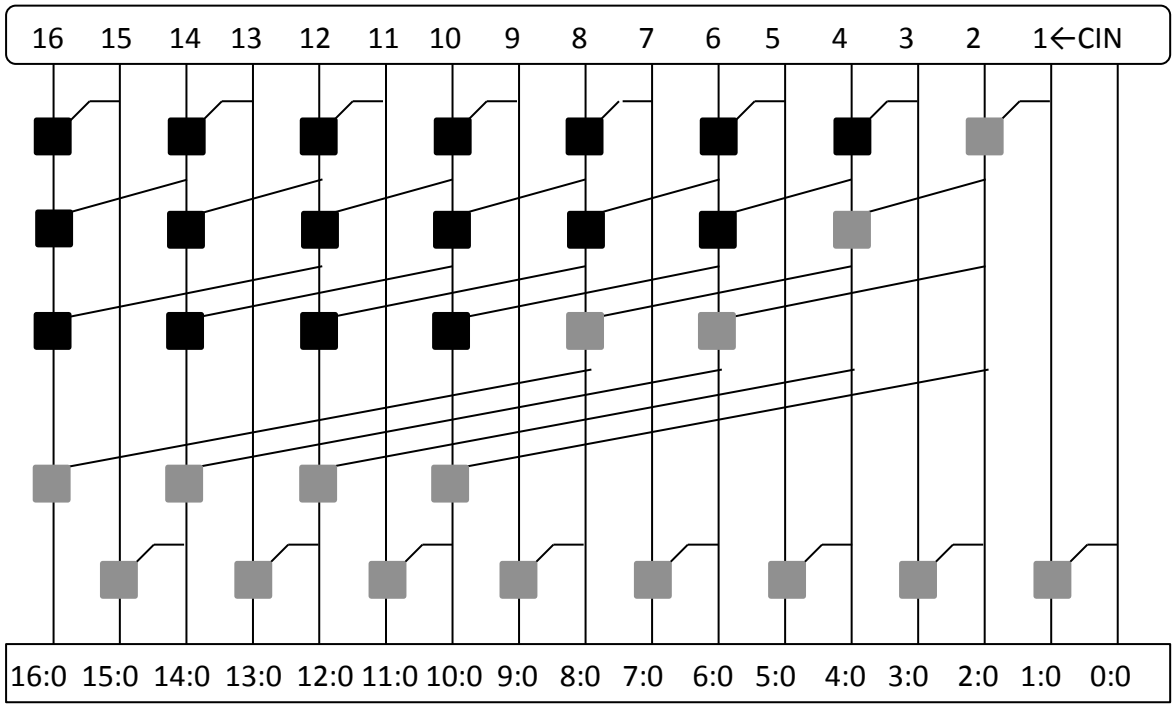
Logic levels L=5
Extra levels l=1
Fanout 2^f+1=5
f=2
Wire tracks 2^t=1
t=0
$l+f+t=L-1=3$
(1, 2, 0)

Kogge-Stone adder



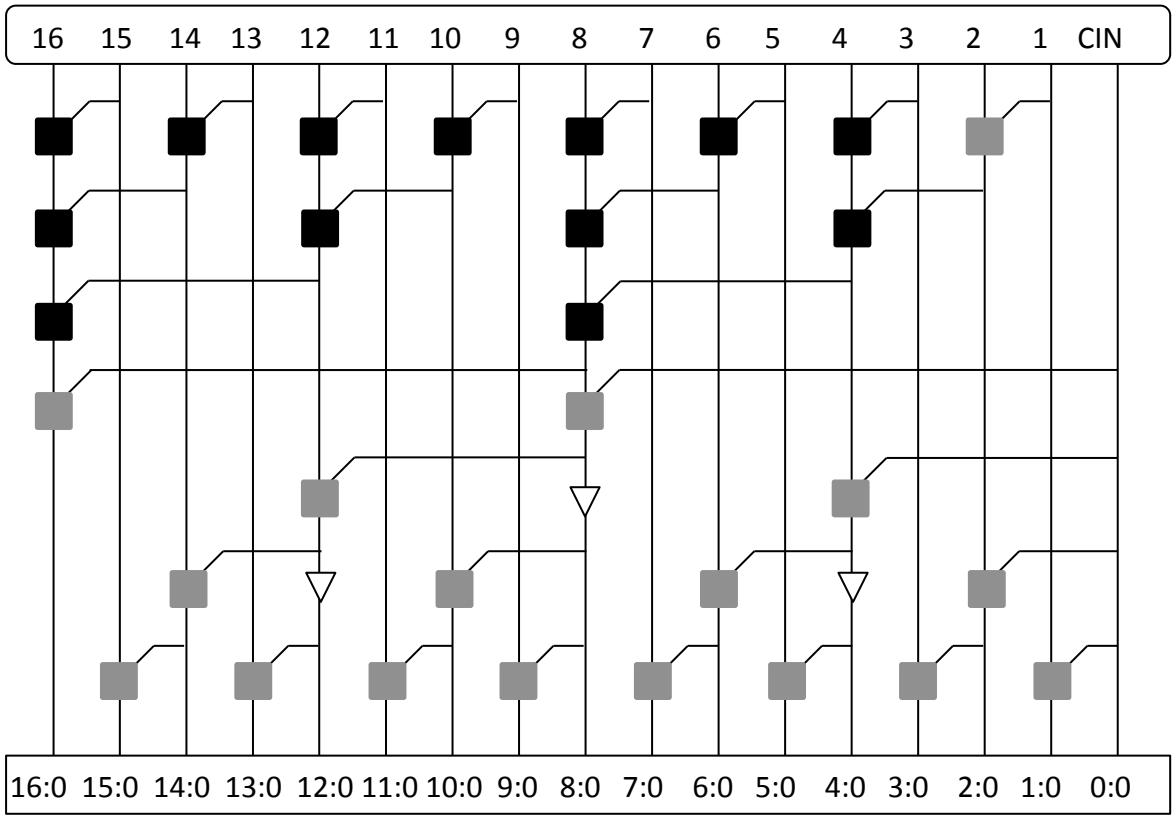
Logic levels L=4
Extra levels l=0
Fanout 2^f+1=2
f=0
Wire tracks 2^t=8
t=3
$l+f+t=L-1=3$
(0, 0, 3)

Kogge-Stone adder



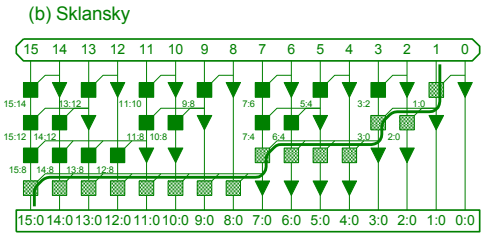
Logic levels L=5
Extra levels l=1
Fanout 2^f+1=2
f=0
Wire tracks 2^t=4
t=2
$l+f+t=L-1=3$
(1, 0, 2)

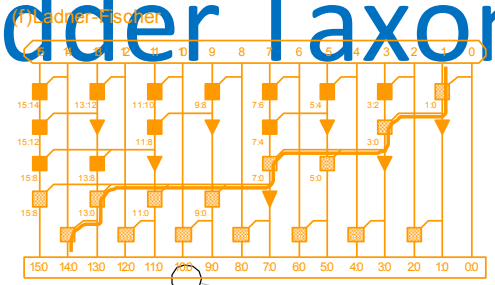
Brent-Kung adder



Logic levels L=6
Extra levels l=3
Fanout 2^f+1=2
f=0
Wire tracks 2^t=1
t=0
$l+f+t=L-1=3$
(3, 0, 0)

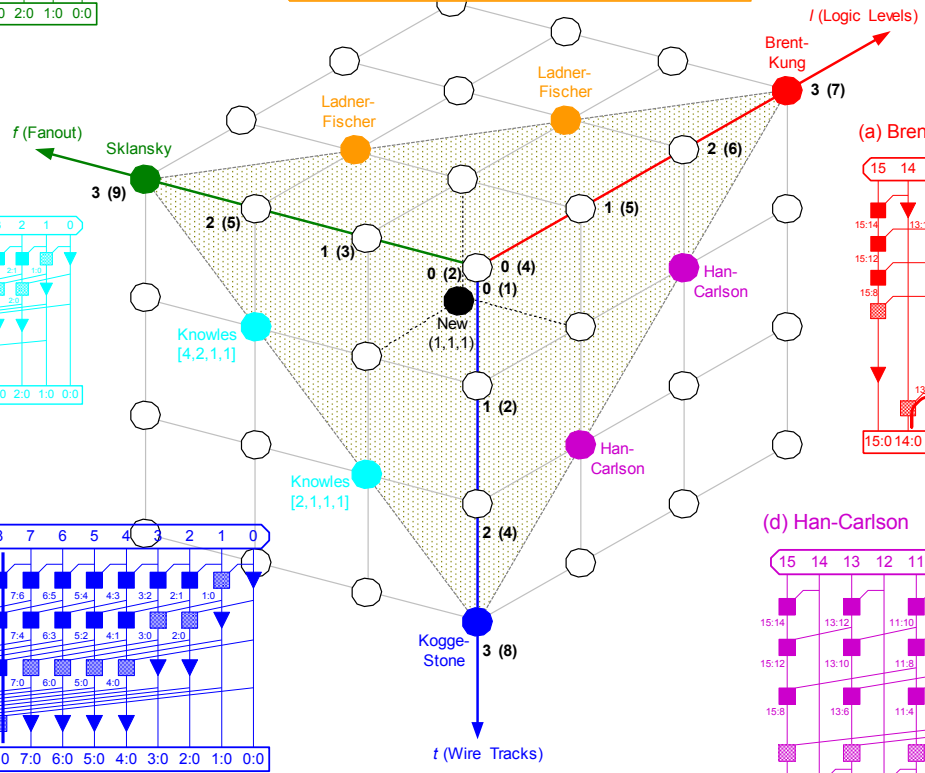
Tree Adder Taxonomy

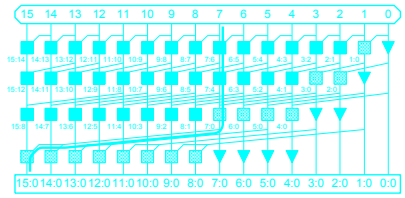


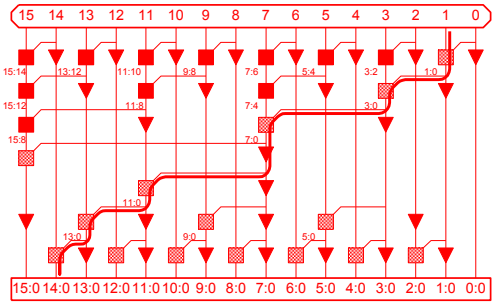


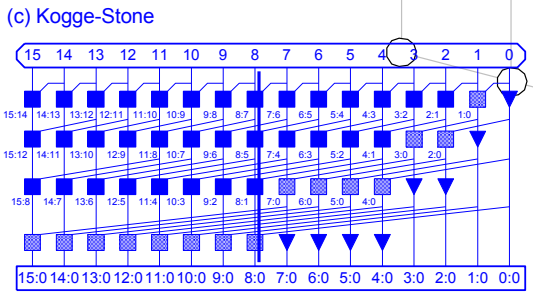
Extra logic levels

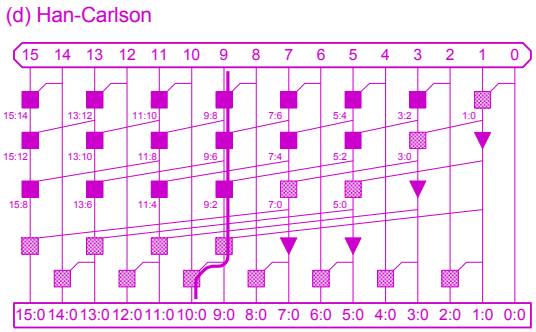
Extra fanout











Extra wire tracks

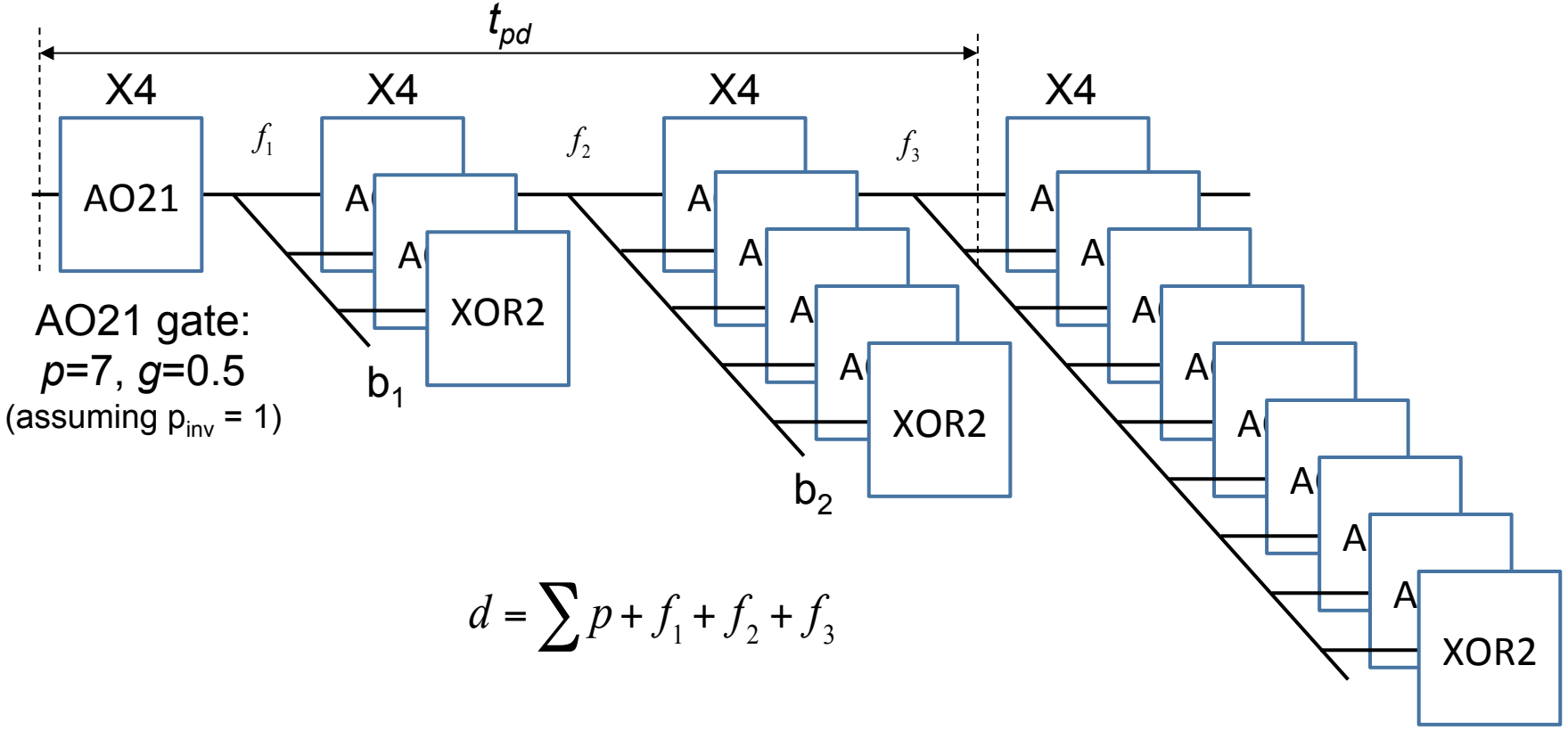
Sklansky adder propagation delay

Timing constraints

Using the path effort to minimize delay by optimizing stage efforts through gate sizing

Sklansky Adder Propagation Delay

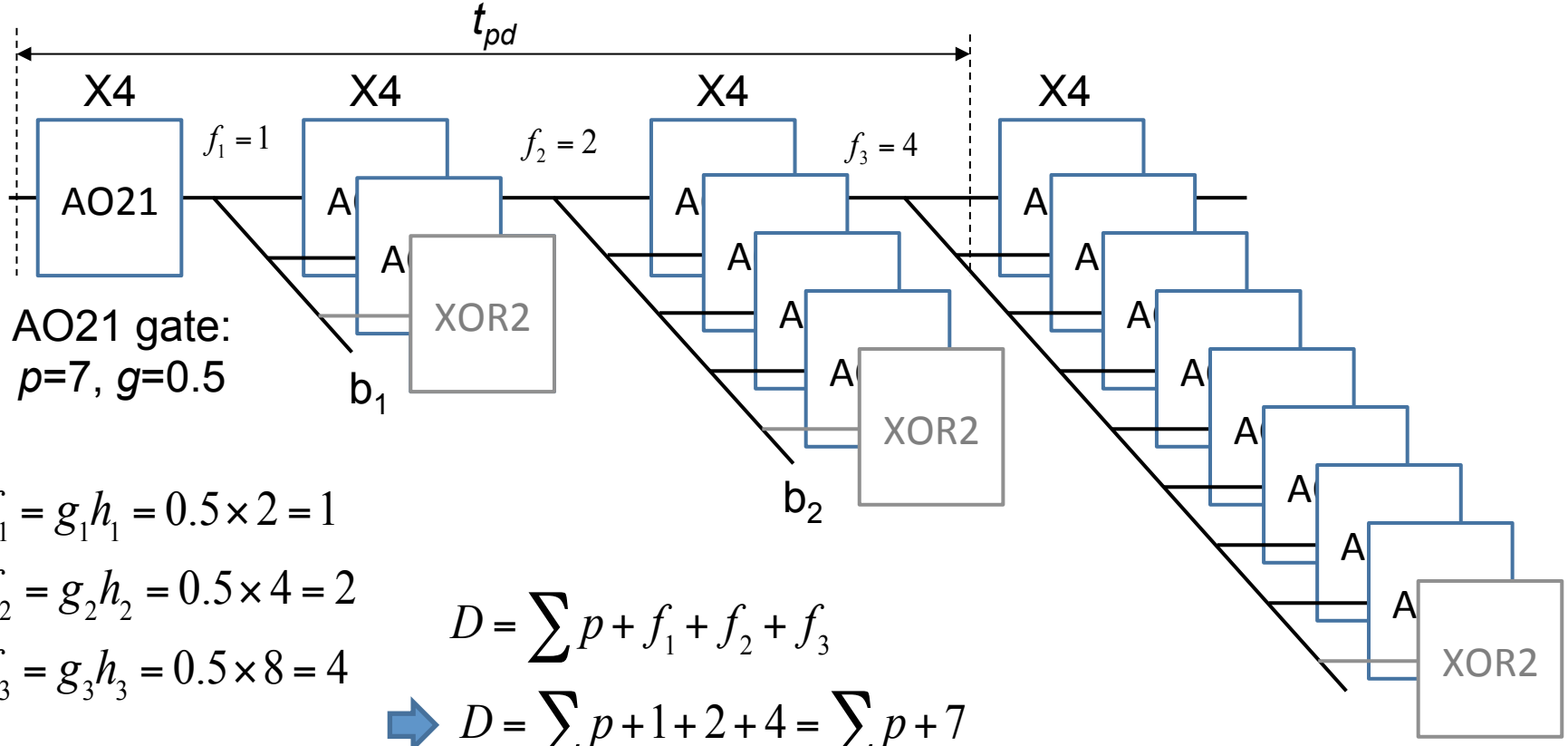
X4 non-inverting logic cell means: X4 input logic – X8 output driver



$$d = \sum p + f_1 + f_2 + f_3$$

Sklansky Adder Propagation Delay

For starters: concentrate on tree delay, all X4 gates, and neglect the SUM XOR gates



$$f_1 = g_1 h_1 = 0.5 \times 2 = 1$$

$$f_2 = g_2 h_2 = 0.5 \times 4 = 2$$

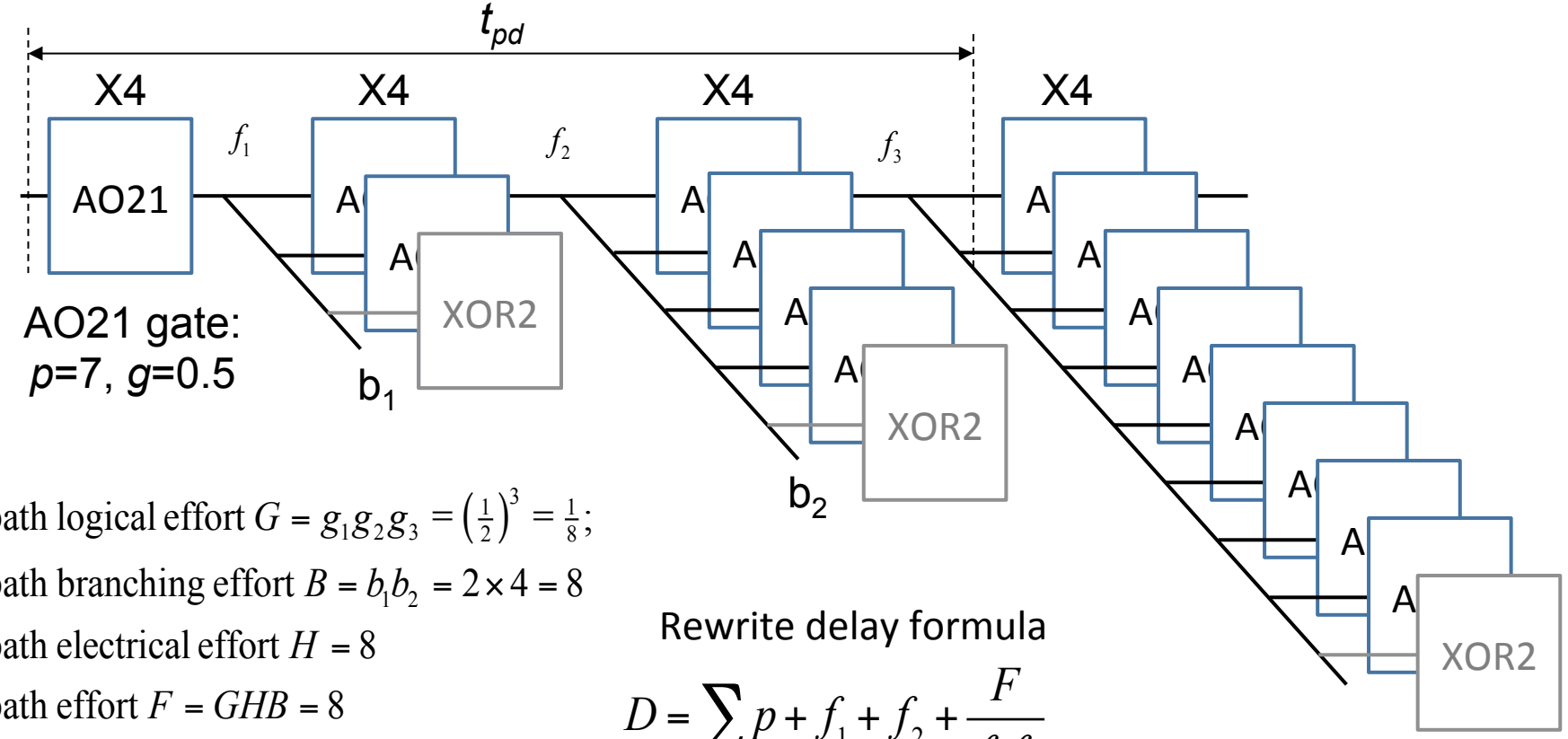
$$f_3 = g_3 h_3 = 0.5 \times 8 = 4$$

$$D = \sum p + f_1 + f_2 + f_3$$

$$\Rightarrow D = \sum p + 1 + 2 + 4 = \sum p + 7$$

Sklansky Adder Propagation Delay

For starters: concentrate on tree delay, all X4 gates, and neglect the SUM XOR gates
Note that all stage efforts are different, would equal stage efforts be more efficient?



path logical effort $G = g_1 g_2 g_3 = \left(\frac{1}{2}\right)^3 = \frac{1}{8}$;

path branching effort $B = b_1 b_2 = 2 \times 4 = 8$

path electrical effort $H = 8$

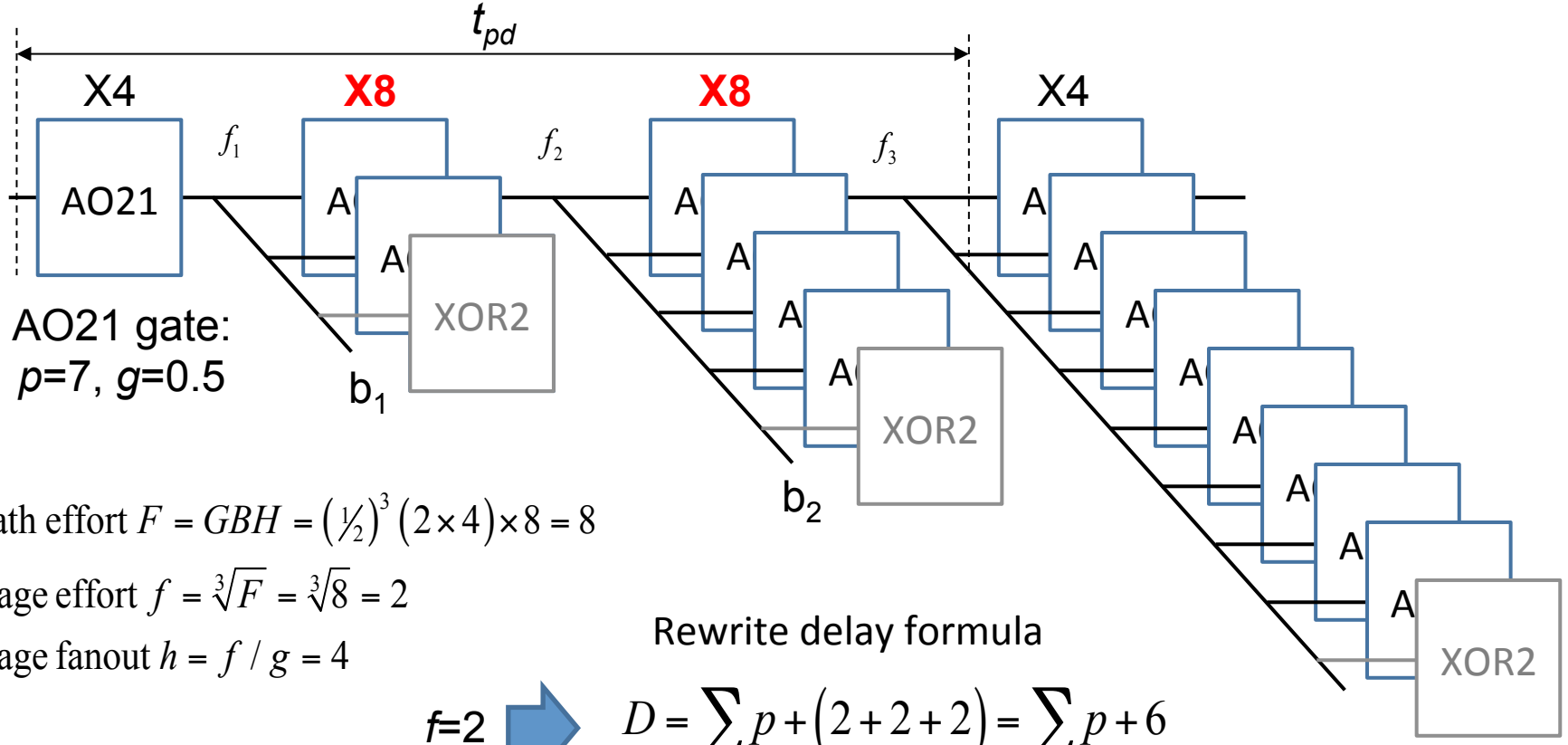
path effort $F = GHB = 8$

Rewrite delay formula

$$D = \sum p + f_1 + f_2 + \frac{F}{f_1 f_2}$$

Sklansky Adder Propagation Delay

For starters: concentrate on tree delay, all X4 gates, and neglect the SUM XOR gates
Note that all stage efforts are different, would equal stage efforts be more efficient?



path effort $F = GBH = \left(\frac{1}{2}\right)^3 (2\times 4)\times 8 = 8$

stage effort $f = \sqrt[3]{F} = \sqrt[3]{8} = 2$

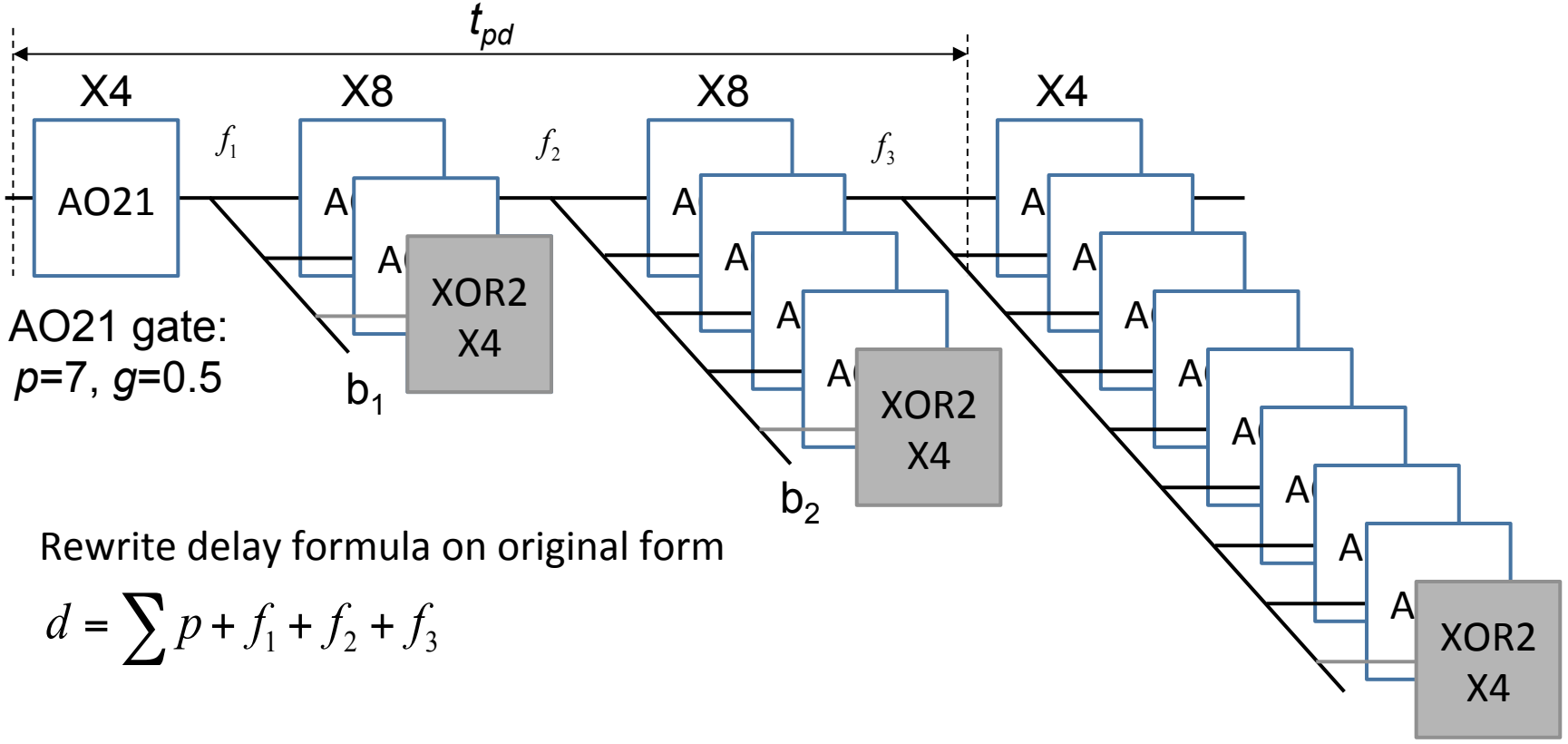
stage fanout $h = f / g = 4$

Rewrite delay formula

f=2 ⇒ $D = \sum p + (2+2+2) = \sum p + 6$

Sklansky Adder Propagation Delay

Now, consider also the SUM XOR gates!

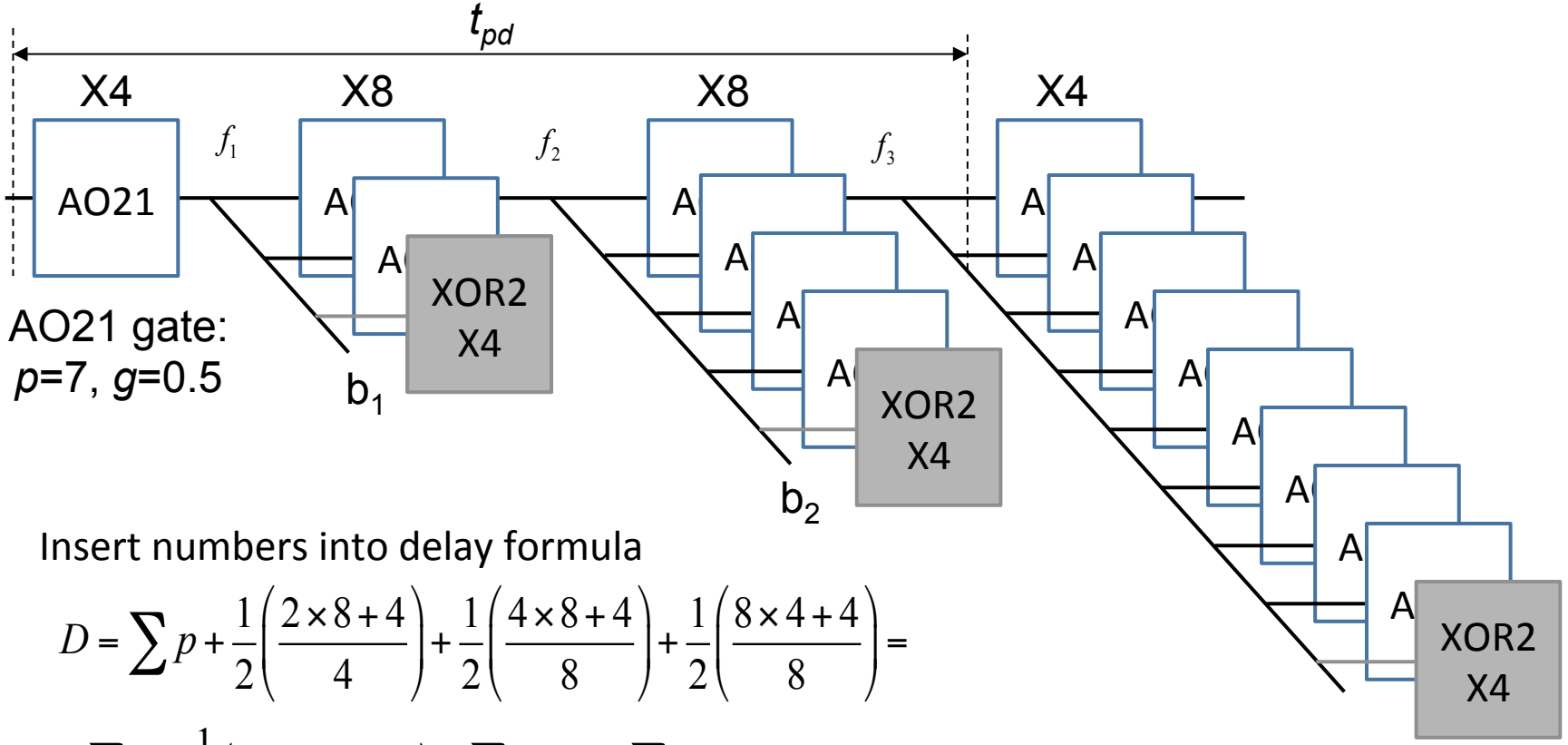


Rewrite delay formula on original form

$$d = \sum p + f_1 + f_2 + f_3$$

Sklansky Adder Propagation Delay

Now, consider also the SUM XOR gates!



Insert numbers into delay formula

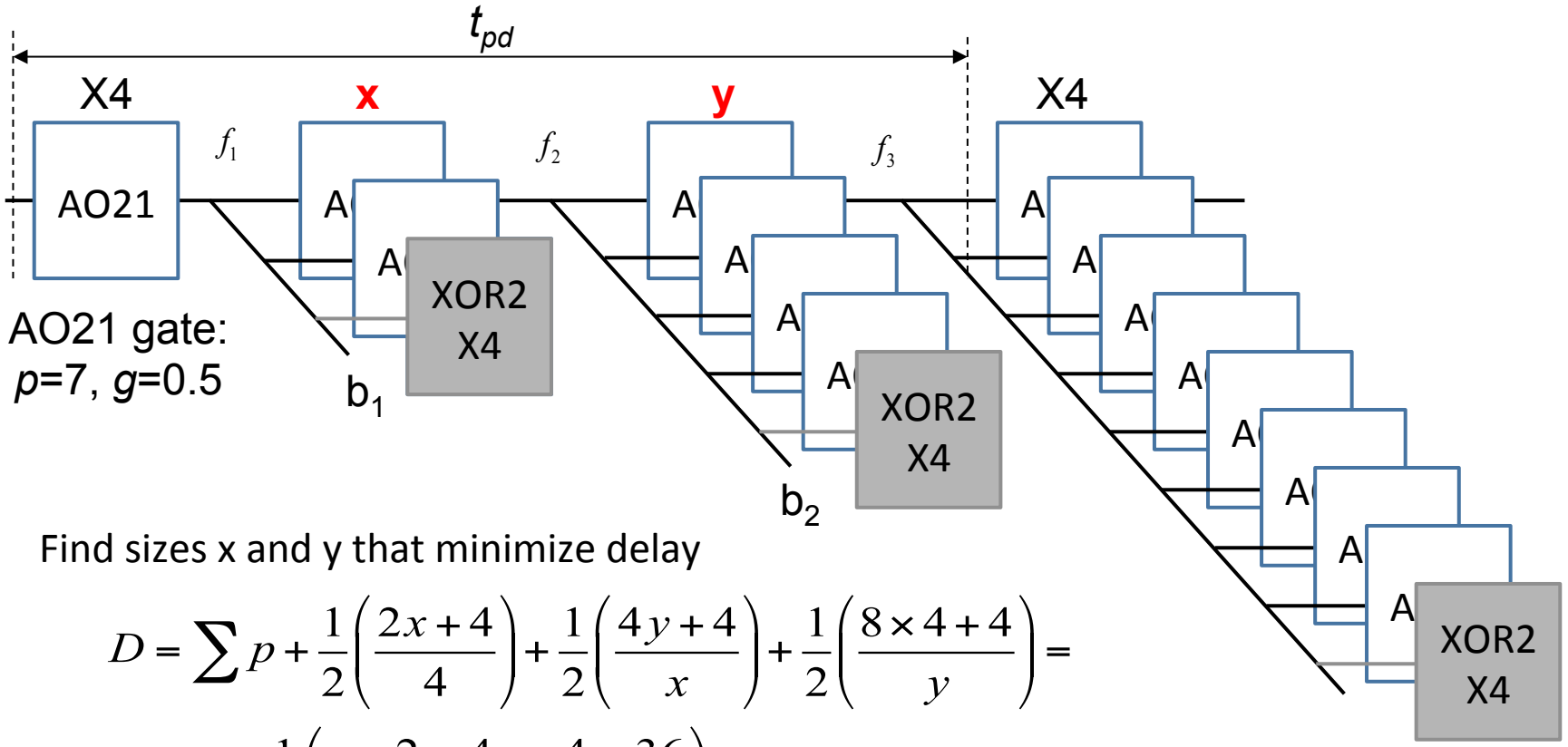
$$D = \sum p + \frac{1}{2}\left(\frac{2\times 8+4}{4}\right) + \frac{1}{2}\left(\frac{4\times 8+4}{8}\right) + \frac{1}{2}\left(\frac{8\times 4+4}{8}\right) =$$

$$= \sum p + \frac{1}{2}\left(5+4.5+4.5\right) = \sum p + 7 > \sum p + 6.0$$

only a small difference

Sklansky Adder Propagation Delay

Now, consider also the SUM XOR gates!



Find sizes x and y that minimize delay

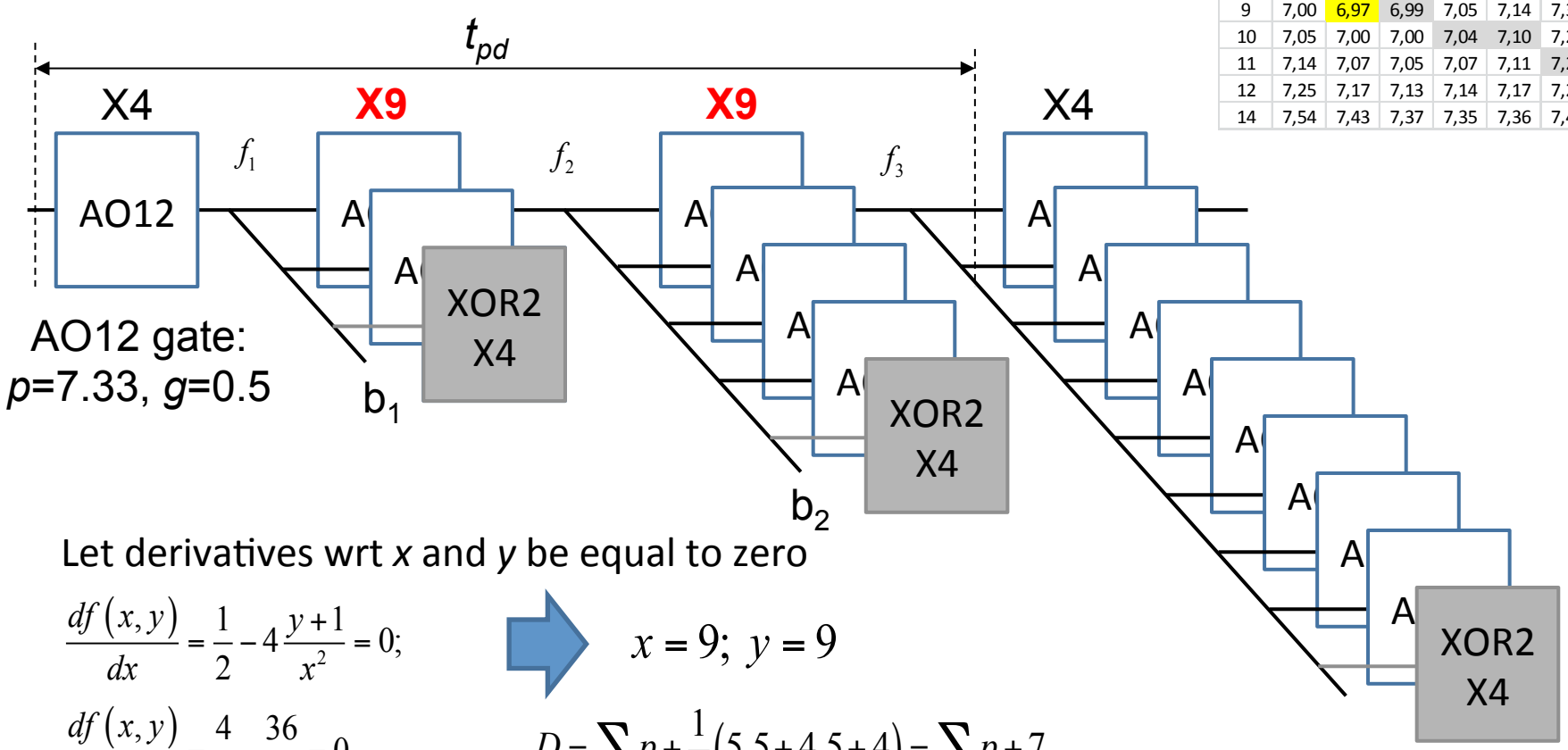
$$D = \sum p + \frac{1}{2}\left(\frac{2x+4}{4}\right) + \frac{1}{2}\left(\frac{4y+4}{x}\right) + \frac{1}{2}\left(\frac{8\times 4+4}{y}\right) =$$

$$= \sum p + \frac{1}{2}\left(\frac{x+2}{2} + \frac{4y+4}{x} + \frac{36}{y}\right)$$

Sklansky Adder Propagation Delay

Now, consider also the SUM XOR gates!

x\y	8	9	10	11	12	14
7	7,07	7,11	7,19	7,31	7,46	7,82
8	7,00	7,00	7,05	7,14	7,25	7,54
9	7,00	6,97	6,99	7,05	7,14	7,37
10	7,05	7,00	7,00	7,04	7,10	7,29
11	7,14	7,07	7,05	7,07	7,11	7,26
12	7,25	7,17	7,13	7,14	7,17	7,29
14	7,54	7,43	7,37	7,35	7,36	7,43



Let derivatives wrt *x* and *y* be equal to zero

$$\frac{df(x,y)}{dx} = \frac{1}{2} - 4\frac{y+1}{x^2} = 0;$$

$$\frac{df(x,y)}{dy} = \frac{4}{x} - \frac{36}{y^2} = 0$$

$$x = 9;\ y = 9$$

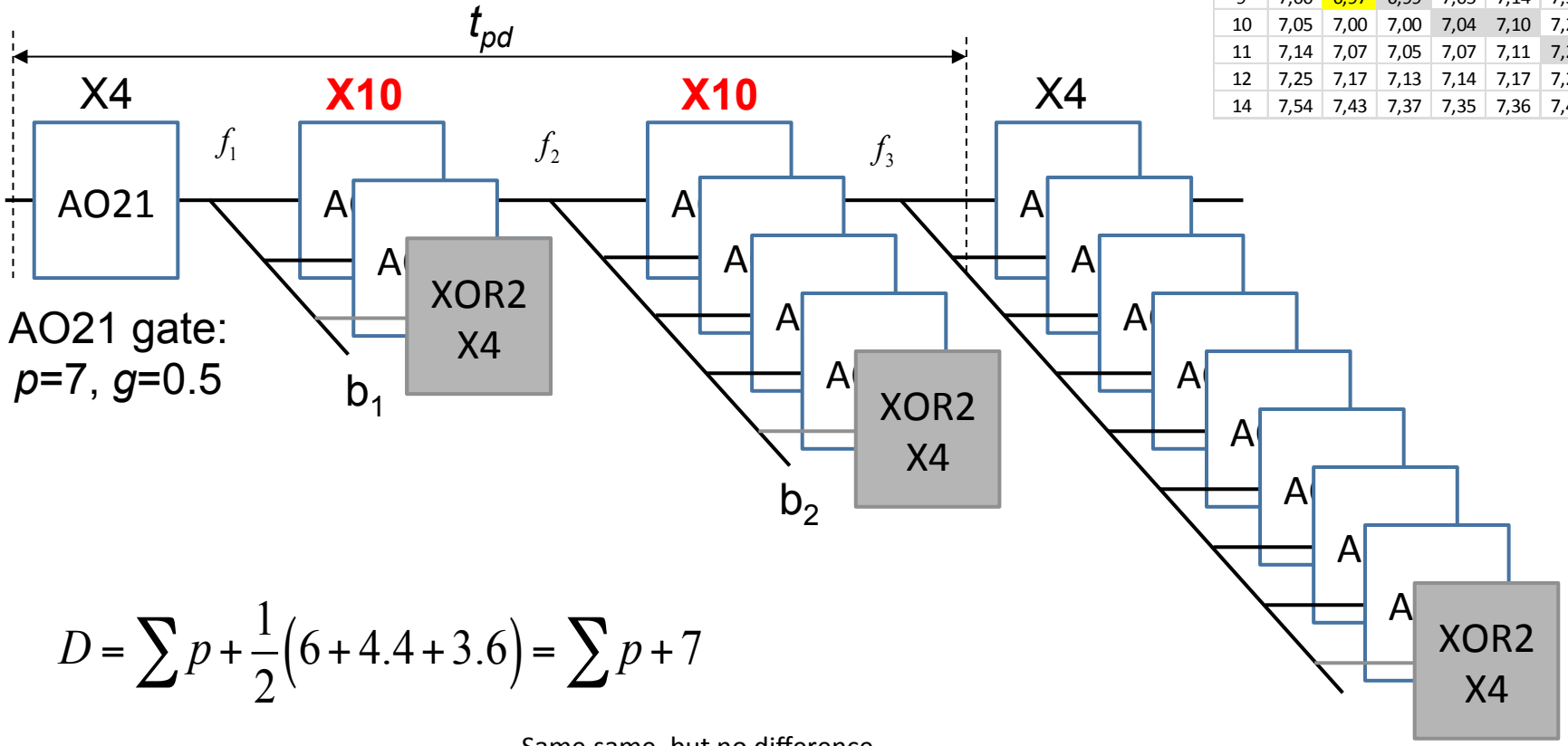
$$D = \sum p + \frac{1}{2}(5.5 + 4.5 + 4) = \sum p + 7$$

Really no difference

Sklansky Adder Propagation Delay

What difference would sizes X10 do?

x\y	8	9	10	11	12	14
7	7,07	7,11	7,19	7,31	7,46	7,82
8	7,00	7,00	7,05	7,14	7,25	7,54
9	7,00	6,97	6,99	7,05	7,14	7,37
10	7,05	7,00	7,00	7,04	7,10	7,29
11	7,14	7,07	7,05	7,07	7,11	7,26
12	7,25	7,17	7,13	7,14	7,17	7,29
14	7,54	7,43	7,37	7,35	7,36	7,43

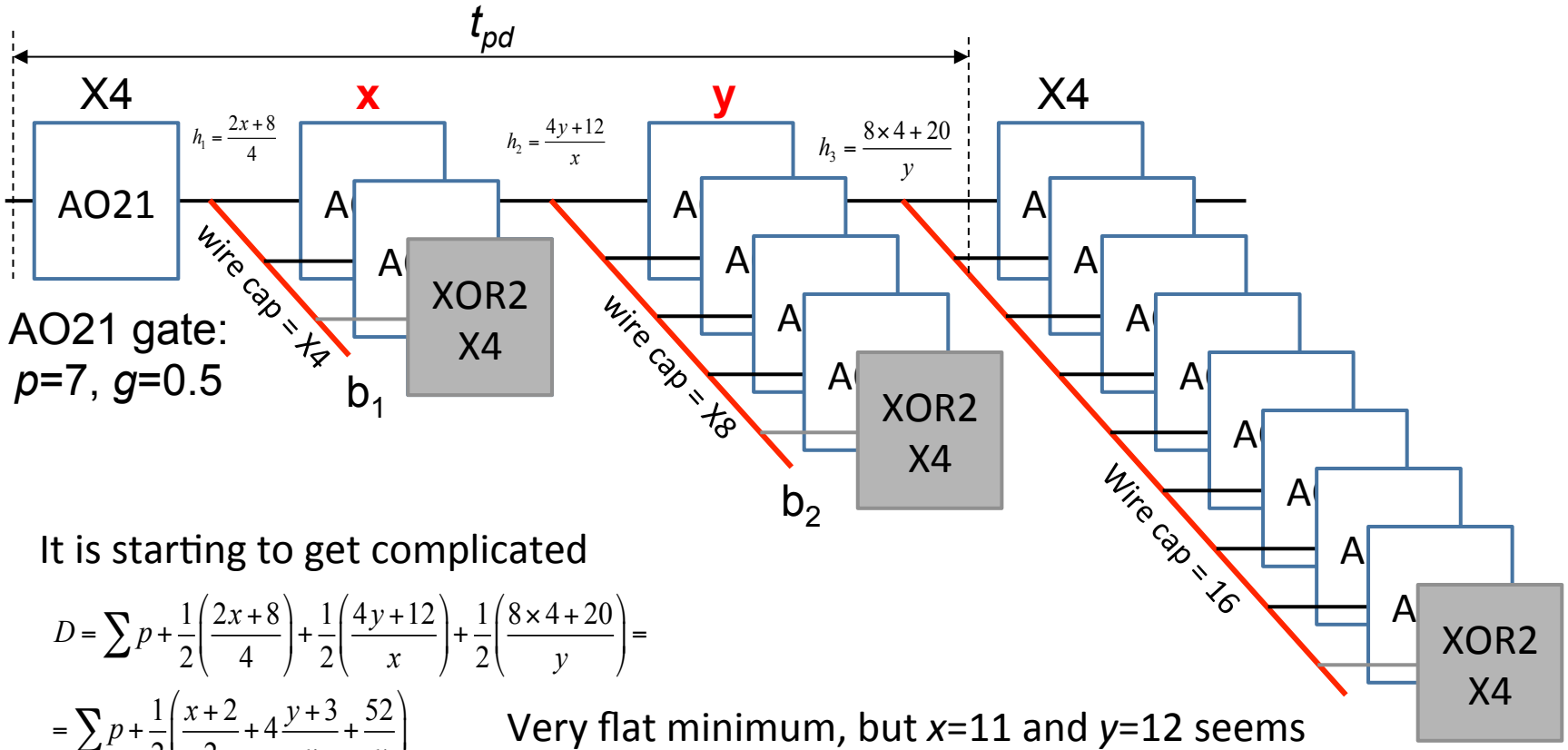


$$D = \sum p + \frac{1}{2}\left(6 + 4.4 + 3.6\right) = \sum p + 7$$

Same,same, but no difference

Sklansky Adder Propagation Delay

What if we add wire capacitances?



It is starting to get complicated

$$D = \sum p + \frac{1}{2}\left(\frac{2x+8}{4}\right) + \frac{1}{2}\left(\frac{4y+12}{x}\right) + \frac{1}{2}\left(\frac{8\times4+20}{y}\right) =$$

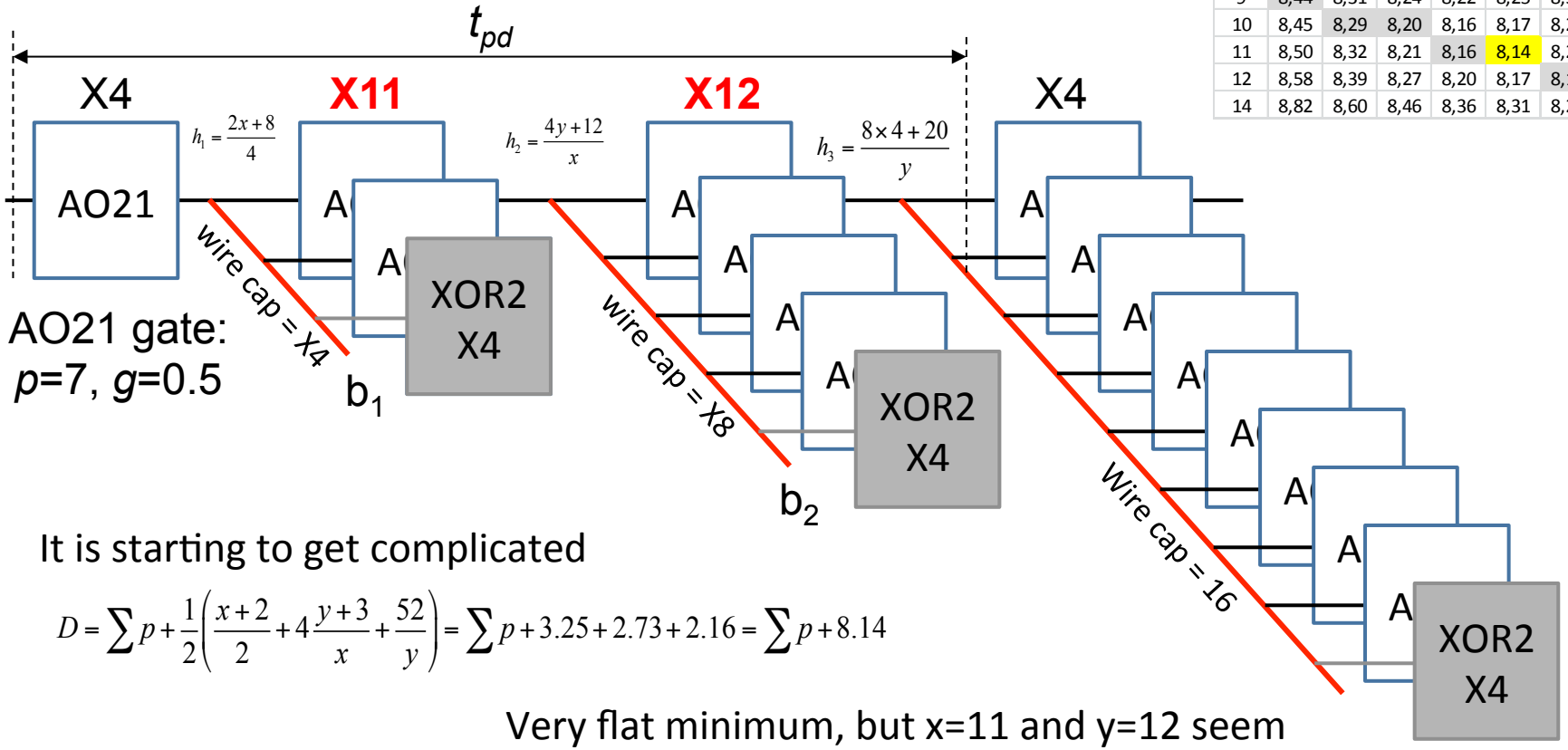
$$= \sum p + \frac{1}{2}\left(\frac{x+2}{2} + 4\frac{y+3}{x} + \frac{52}{y}\right)$$

Very flat minimum, but x=11 and y=12 seems to minimize delay (if not by very much).

Sklansky Adder Propagation Delay

What if we add wire capacitances?

x\y	8	9	10	11	12	14
7	8,64	8,57	8,56	8,61	8,70	8,96
8	8,50	8,39	8,35	8,36	8,42	8,61
9	8,44	8,31	8,24	8,22	8,25	8,38
10	8,45	8,29	8,20	8,16	8,17	8,26
11	8,50	8,32	8,21	8,16	8,14	8,20
12	8,58	8,39	8,27	8,20	8,17	8,19
14	8,82	8,60	8,46	8,36	8,31	8,29



It is starting to get complicated

$$D = \sum p + \frac{1}{2}\left(\frac{x+2}{2} + 4\frac{y+3}{x} + \frac{52}{y}\right) = \sum p + 3.25 + 2.73 + 2.16 = \sum p + 8.14$$

Very flat minimum, but x=11 and y=12 seem to minimize delay (if not by very much).

Summary

Q & A