MCC092

Postlab lab 3

Prelab lab 4

2018-10-02

Lena Peterson

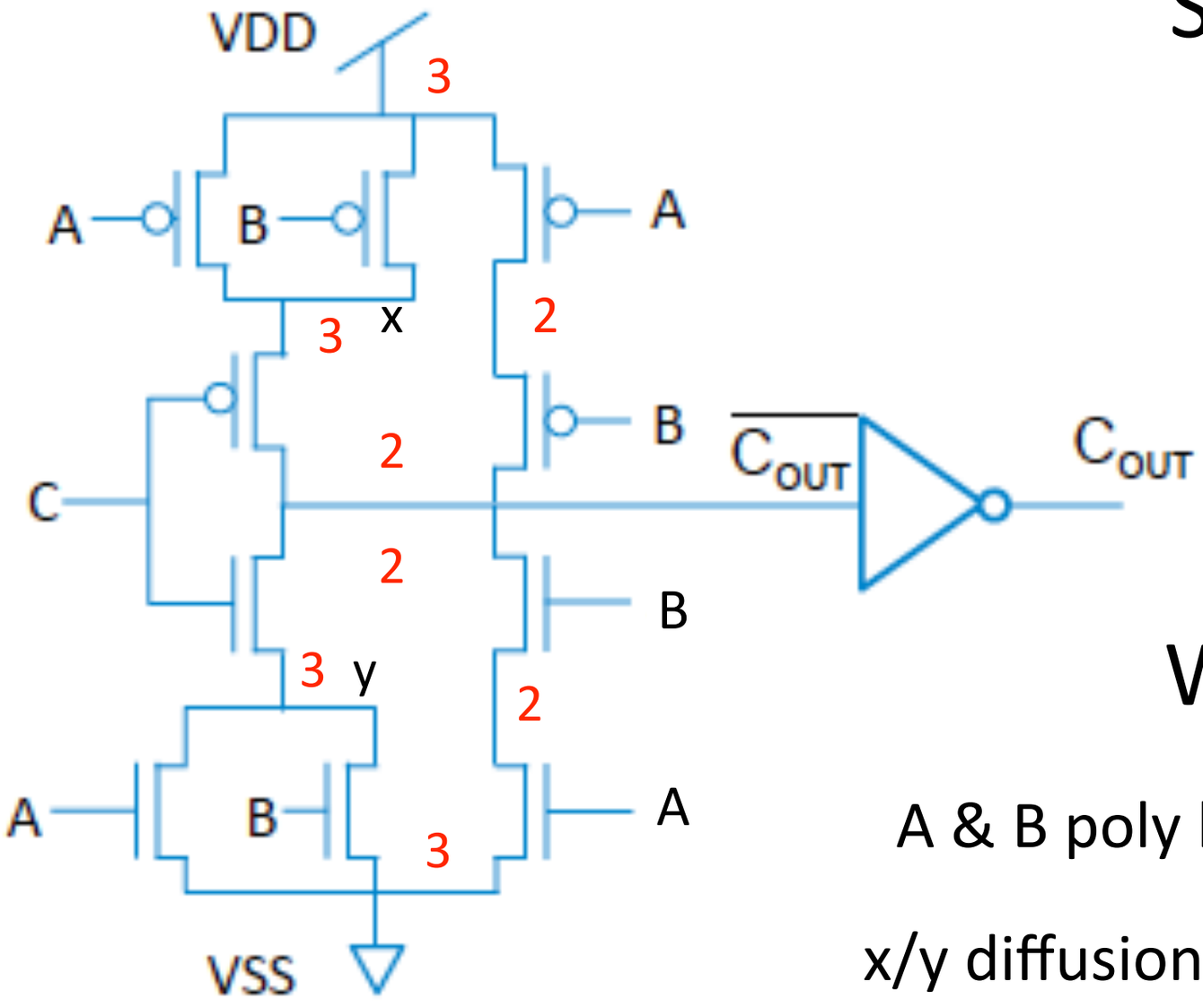
Week 5

- Monday October 1
  - Lab 3
- Tuesday October 2
  - Lecture on wires (Kjell)
  - Postlab 3 + prelab 4 session
- Thursday October 4
  - Prelab 4 + preparation for adder exercise 1
  - Wire exercise
- Friday October 5
  - Deadline prelab 4

Lab 3

- Do your design on paper first.
- Euler analysis is good - but there may be multiple solutions.
- Stick diagrams help.
  - If you must revise your solution do that on paper first!
- Usually no metal-2 in standard cells.

Euler path



Same topology in n-net and p-net.

Odd order nodes:

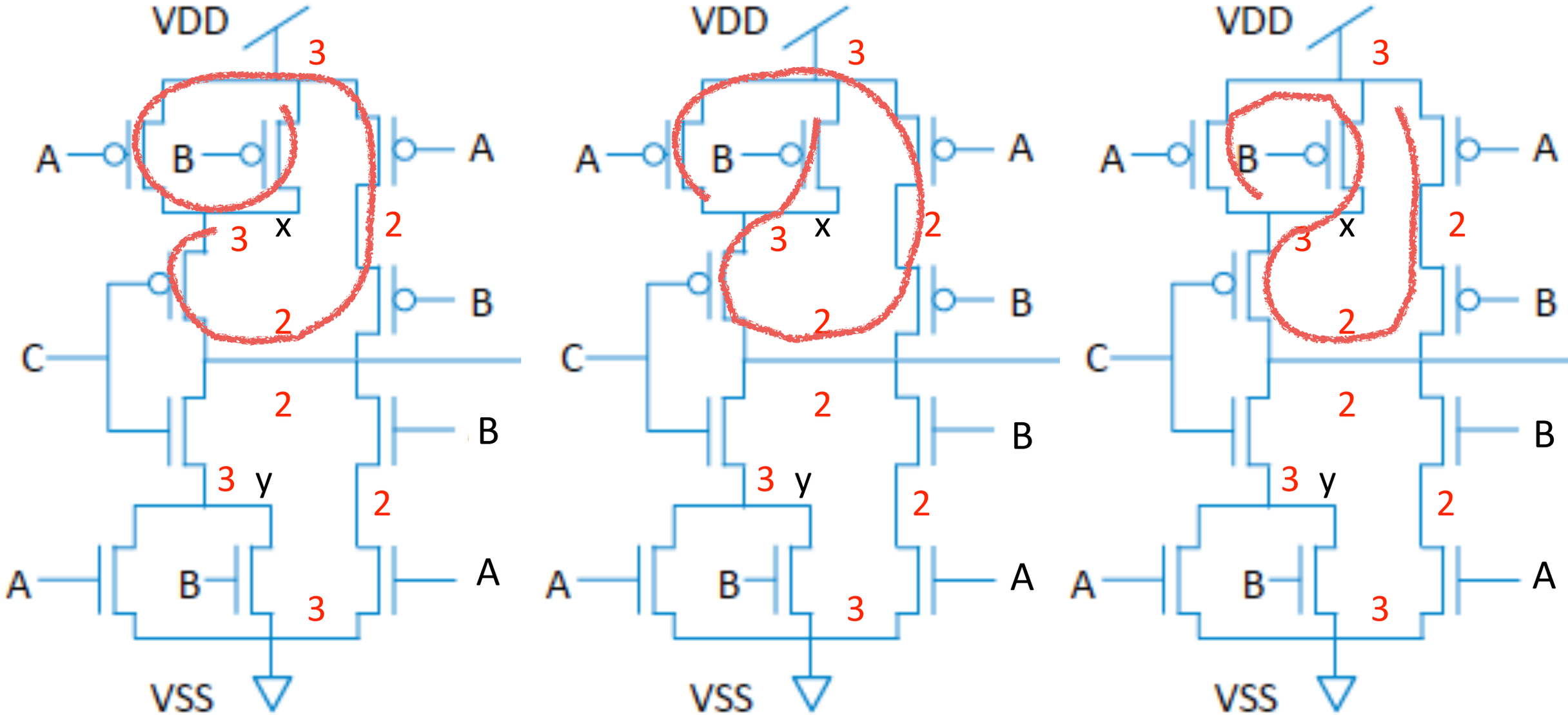
Start/end in x/y and V_{DD}/V_{SS}

Which one too choose?

A & B poly lines must be connected

x/y diffusion areas must be connected with metal-1 wire since their node order is > 2

Three Euler paths



(1) That is: BAABC

(2) Also possible: ABABC

(3) That is: AABCB

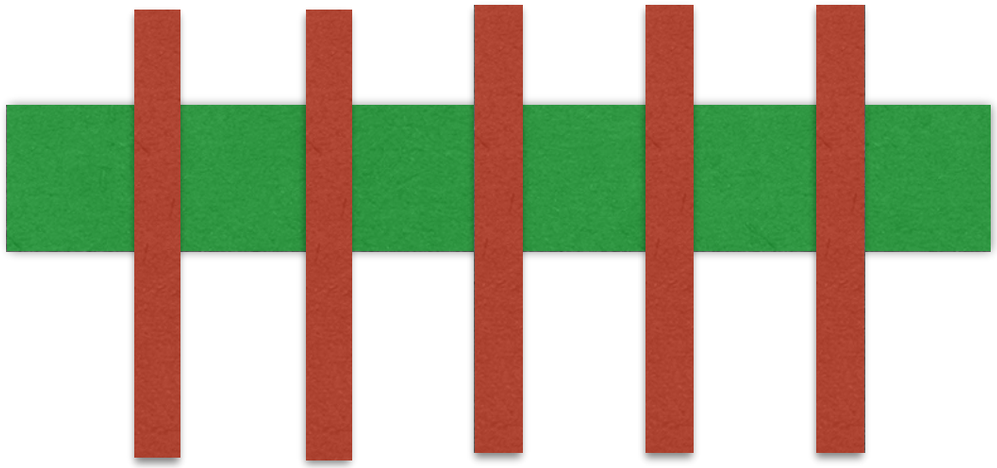
(4) Also possible: BABCA

(5) That is: ABCBA

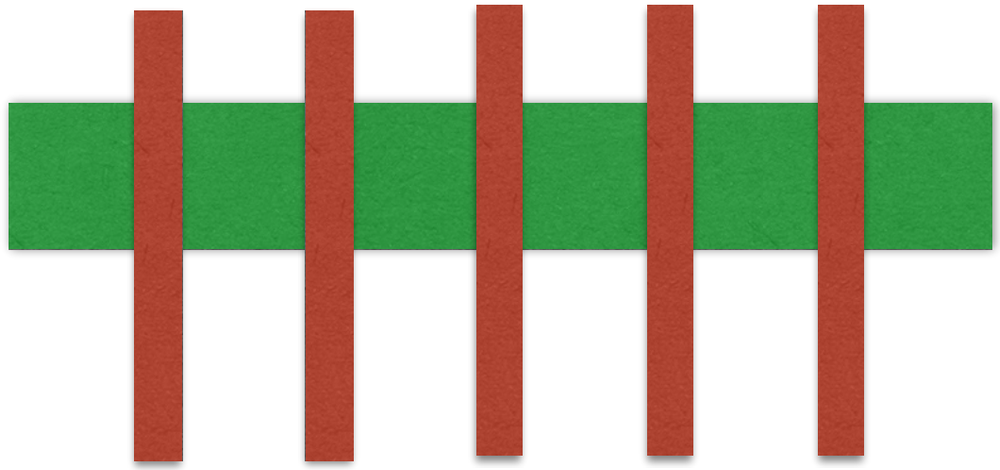
(6) Also possible: BACBA

Four single-lines-of diffusion

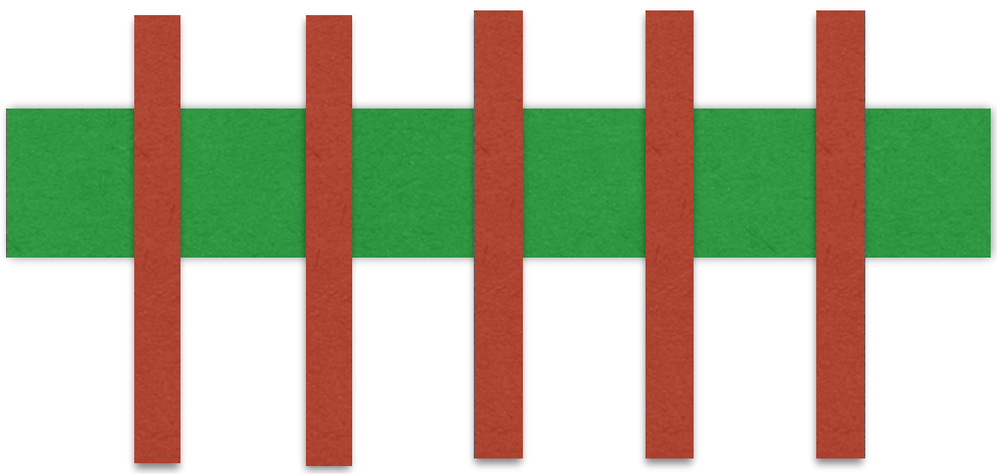
(1) BAABC

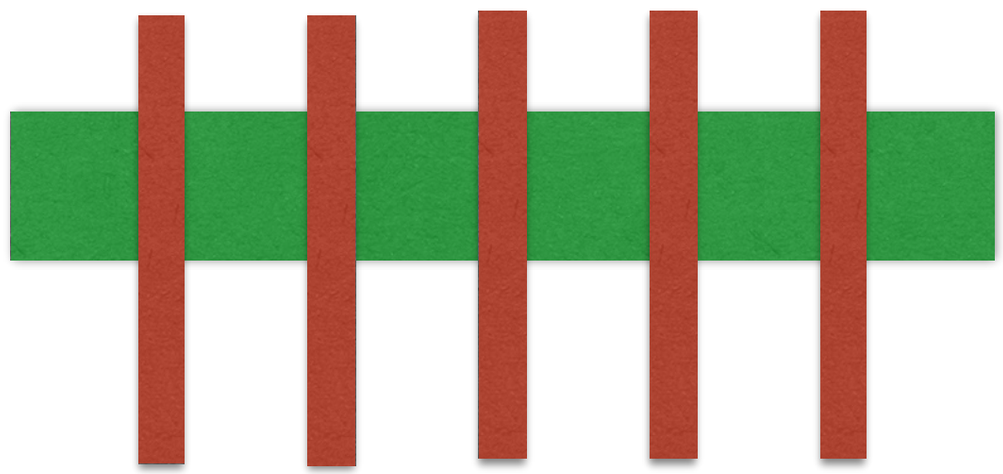


(3) AABCB



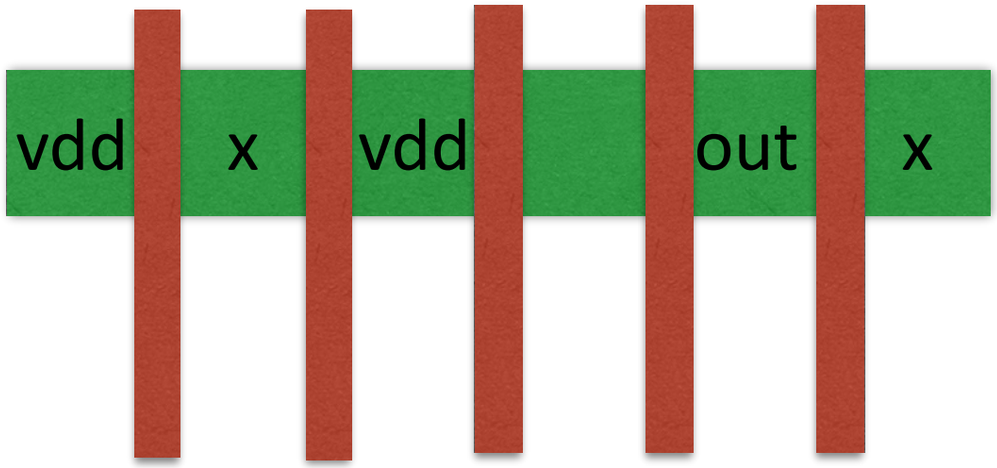
(5) ABCBA



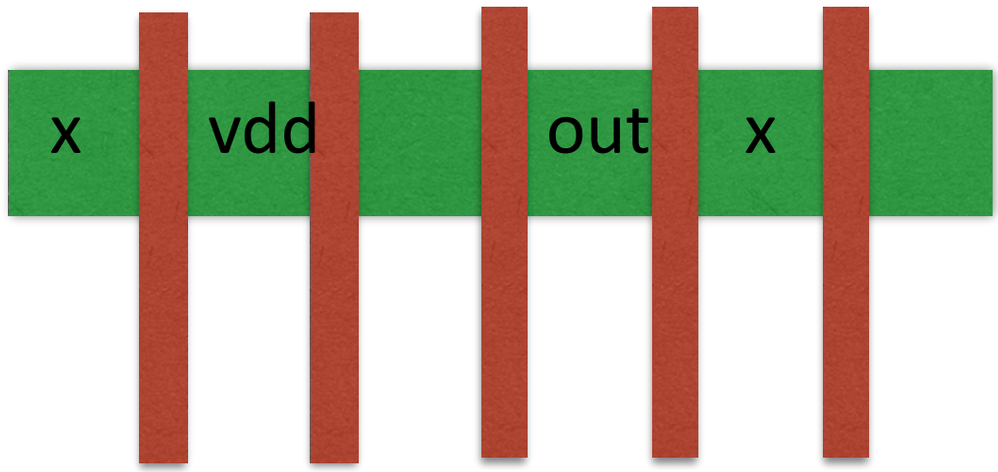


Four single-lines-of diffusion

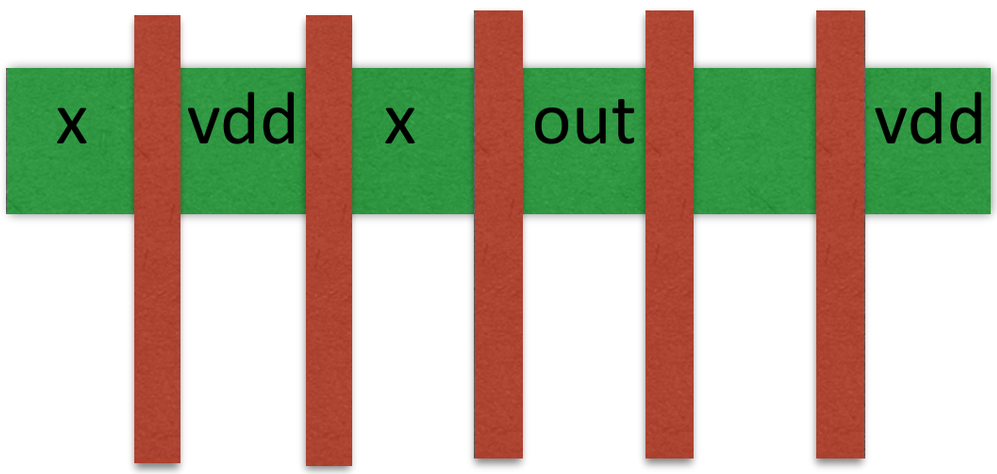
(1) BAABC

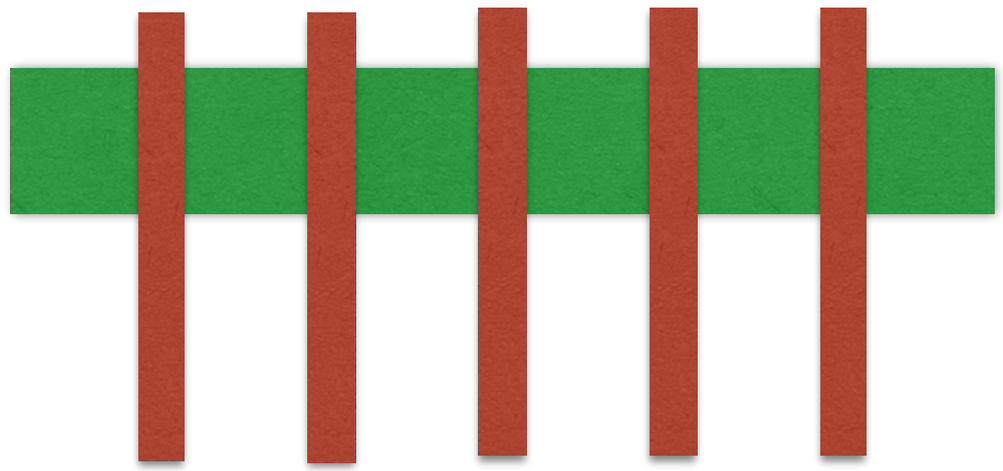


(3) AABCB



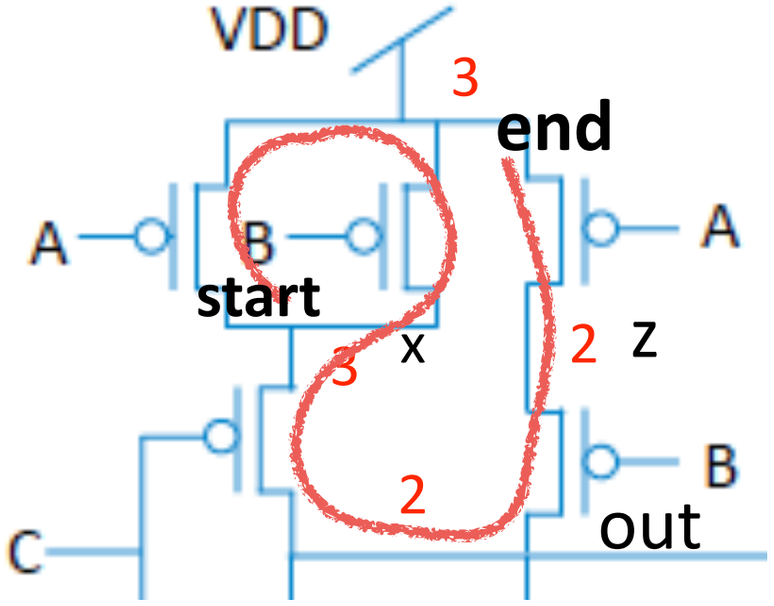
(5) ABCBA



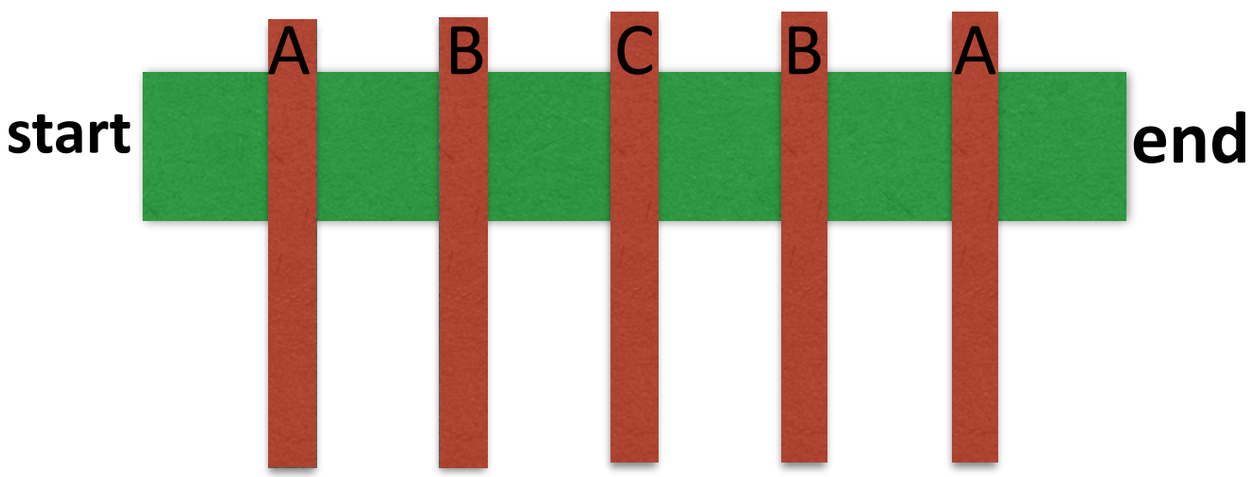


Mapping path to single-line-of diffusion

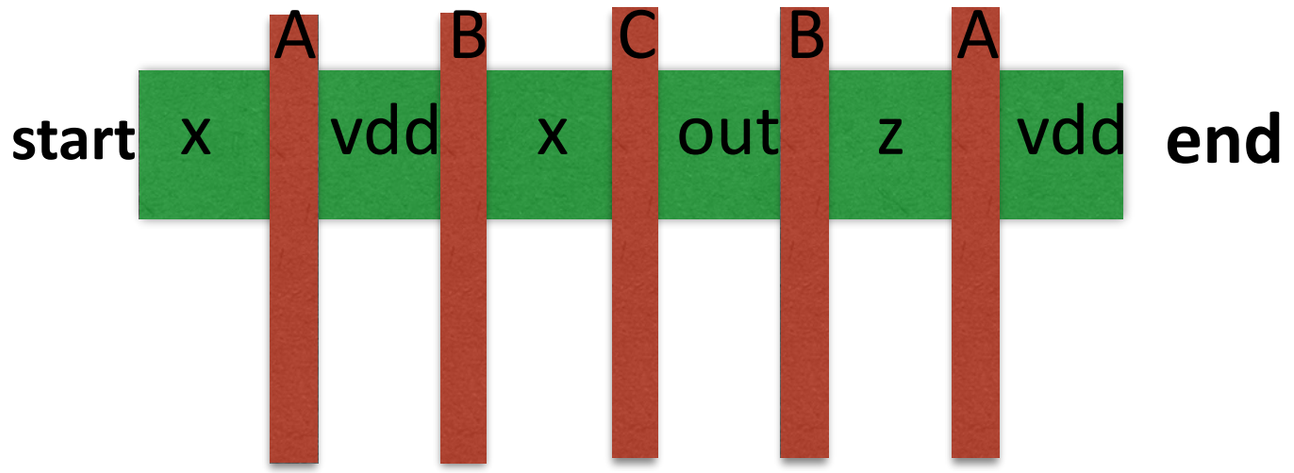
Step 1: The path as drawn



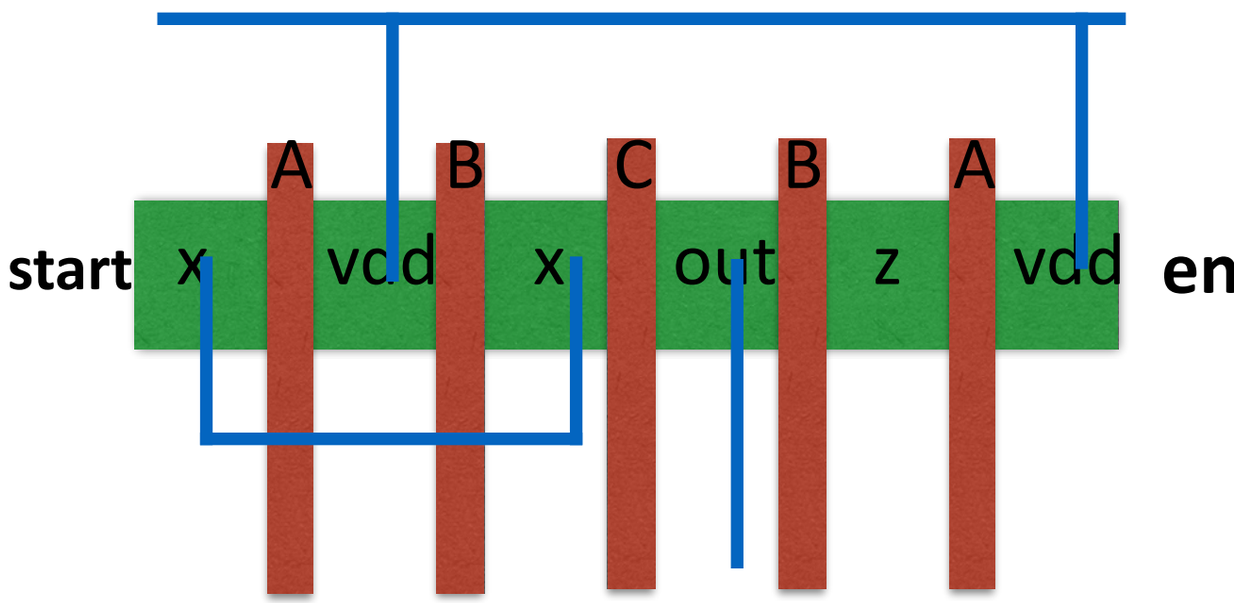
Step 2: Label the gates on diffusion from start to end of path



Step 3: Label the circuit nodes along the path from start to end



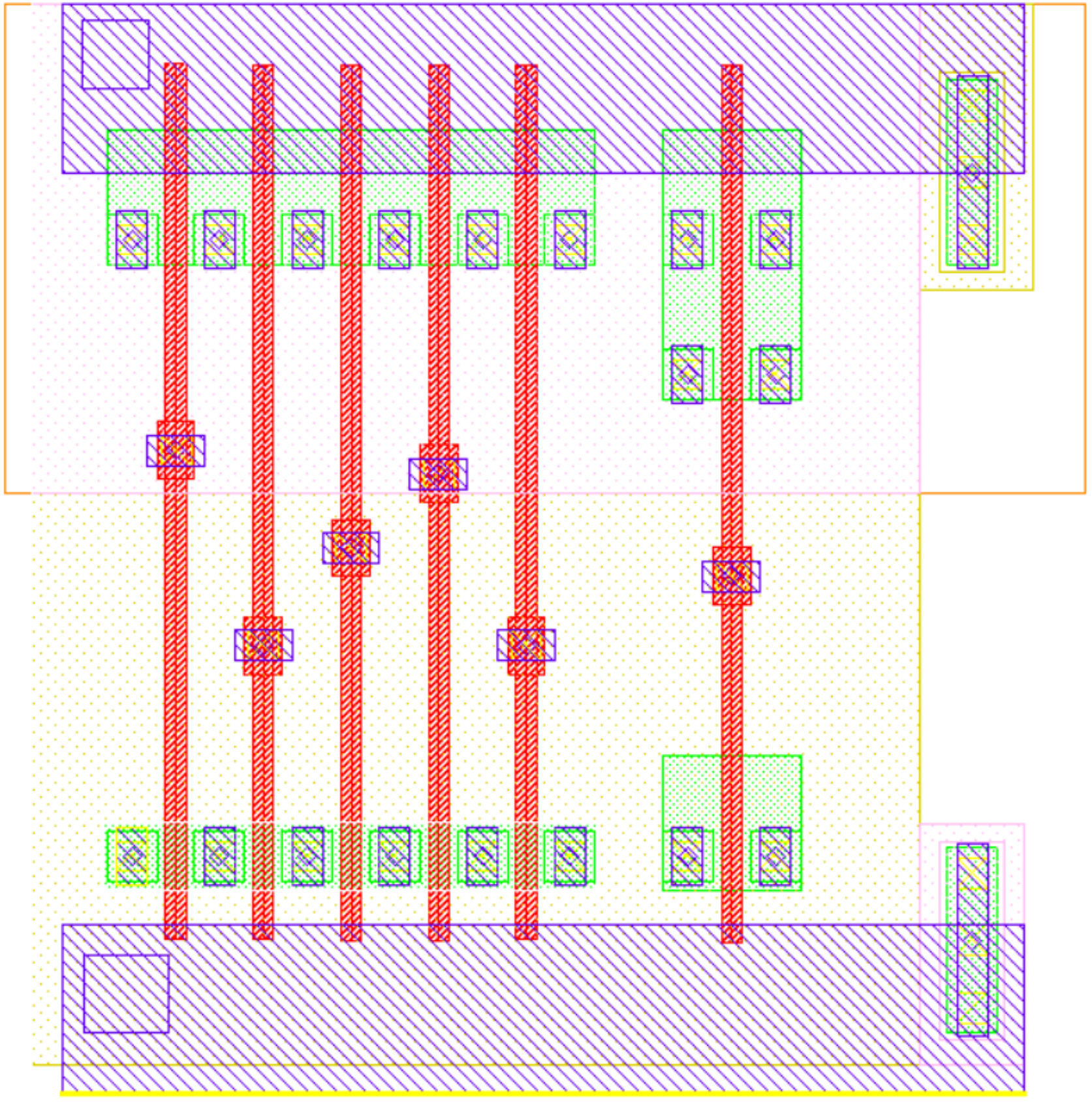
Step 4: Draw (stick) connections to connect areas that are the same ckt node



Layout quick questions

Alternatives:

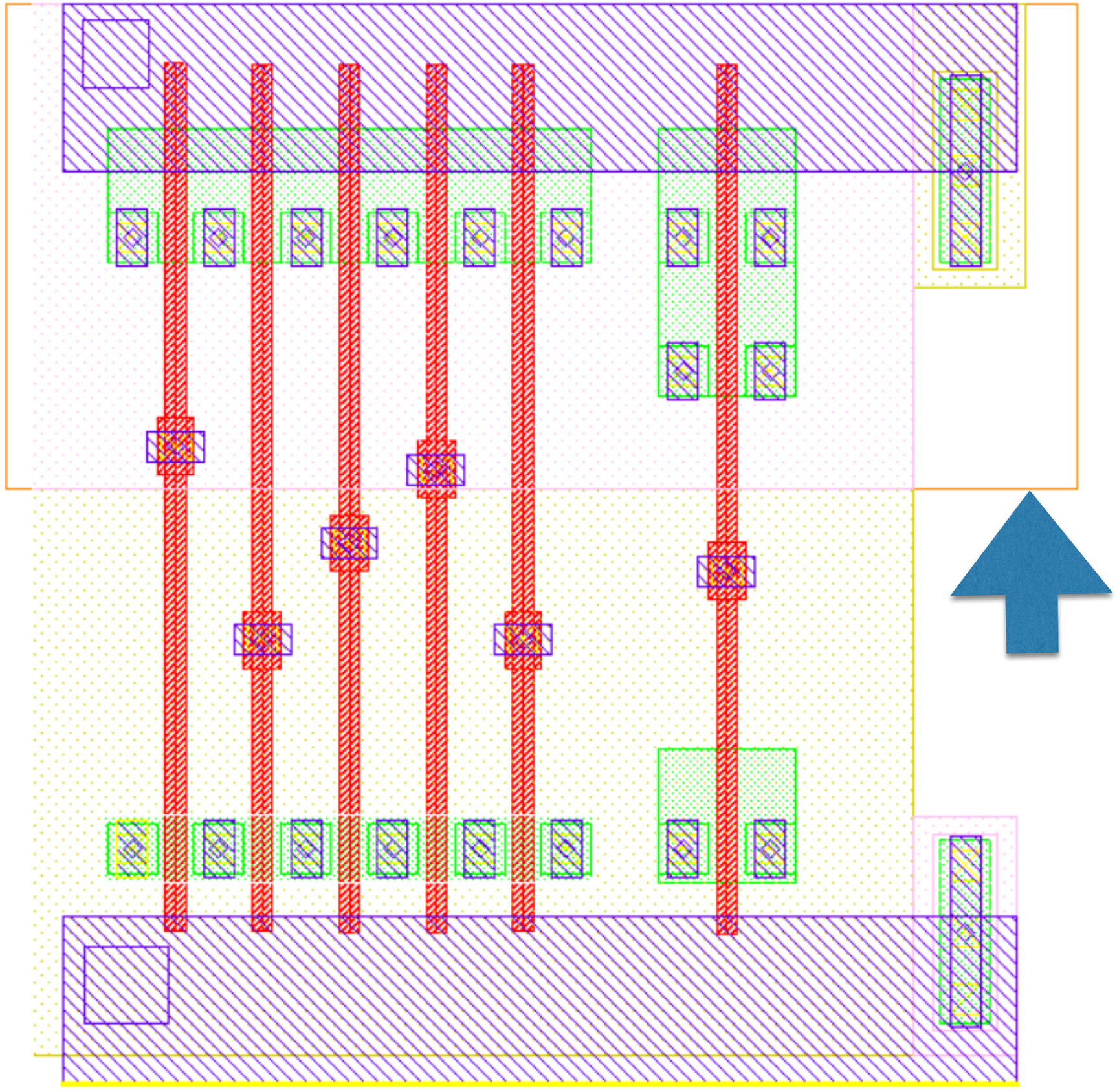
1. Diffusion
2. Pplus
3. Nplus
4. N-well
5. Poly



Layout quick questions

Alternatives:

A. Diffusion
B. Pplus
C. Nplus
D. N-well
E. Poly



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A. Diffusion
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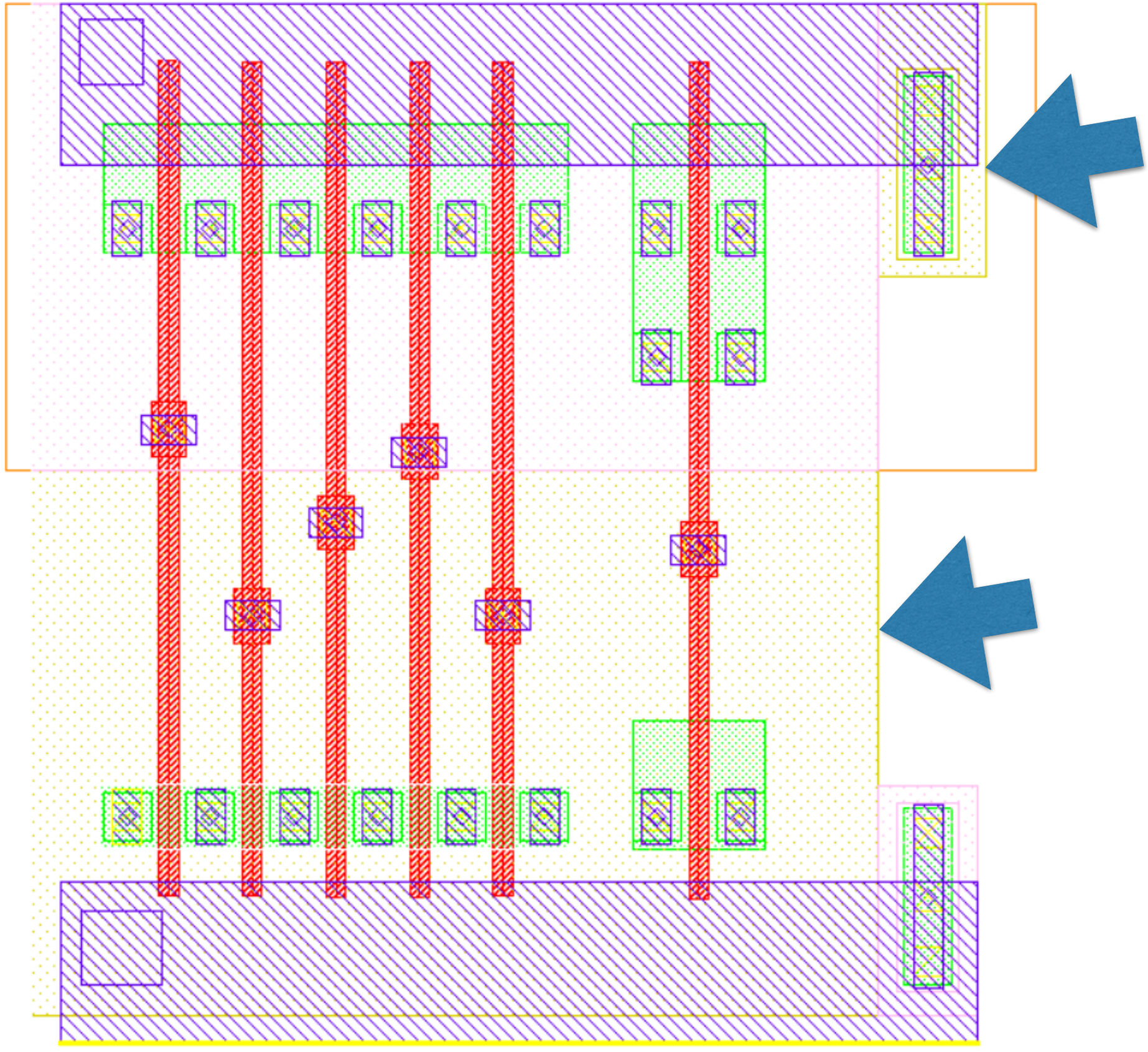
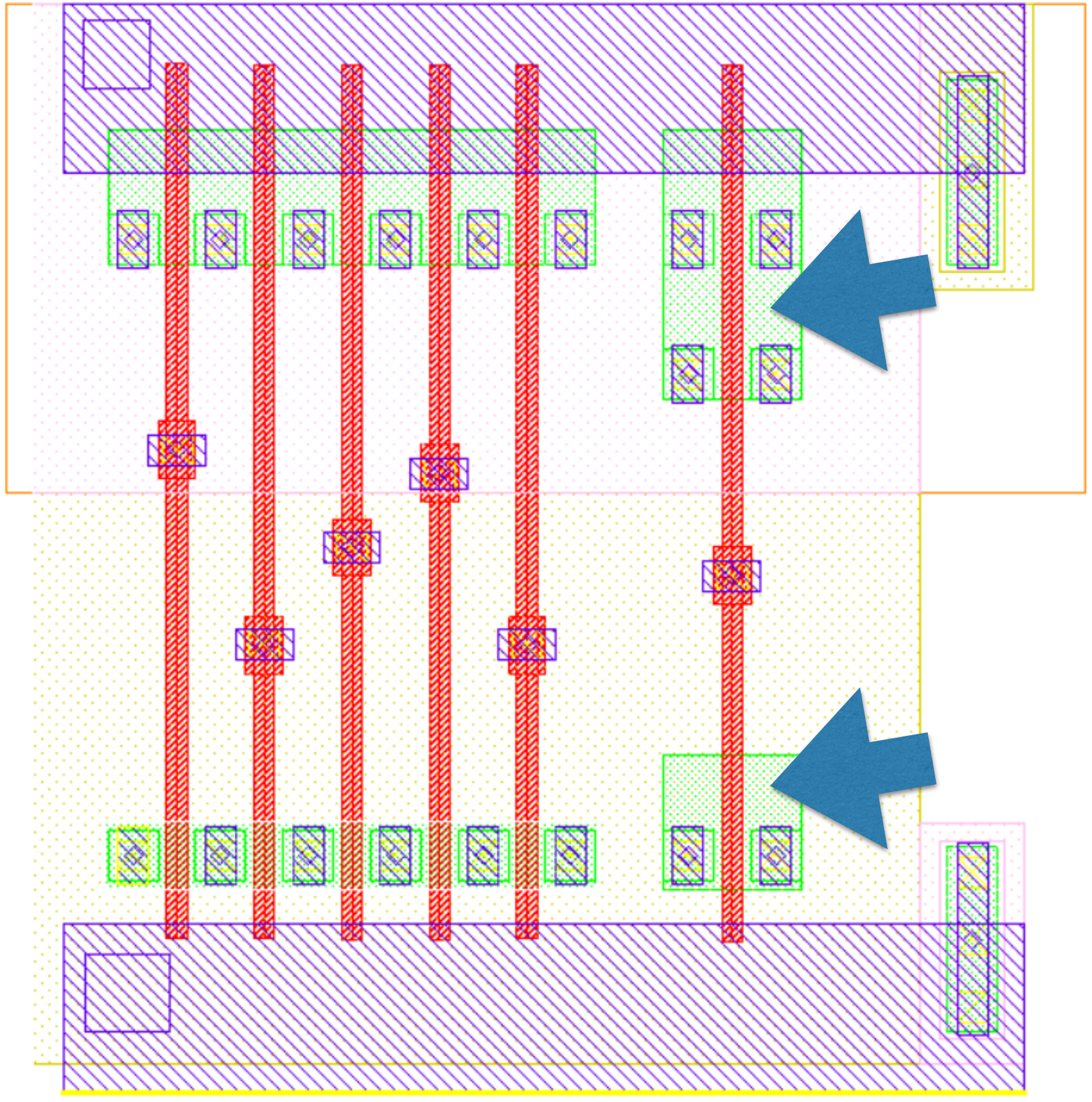


Layout quick questions

Alternatives:

A. **Diffusion**
B. Pplus
C. Nplus
D. N-well
E. Poly



Layout quick questions

Alternatives:

A. Diffusion
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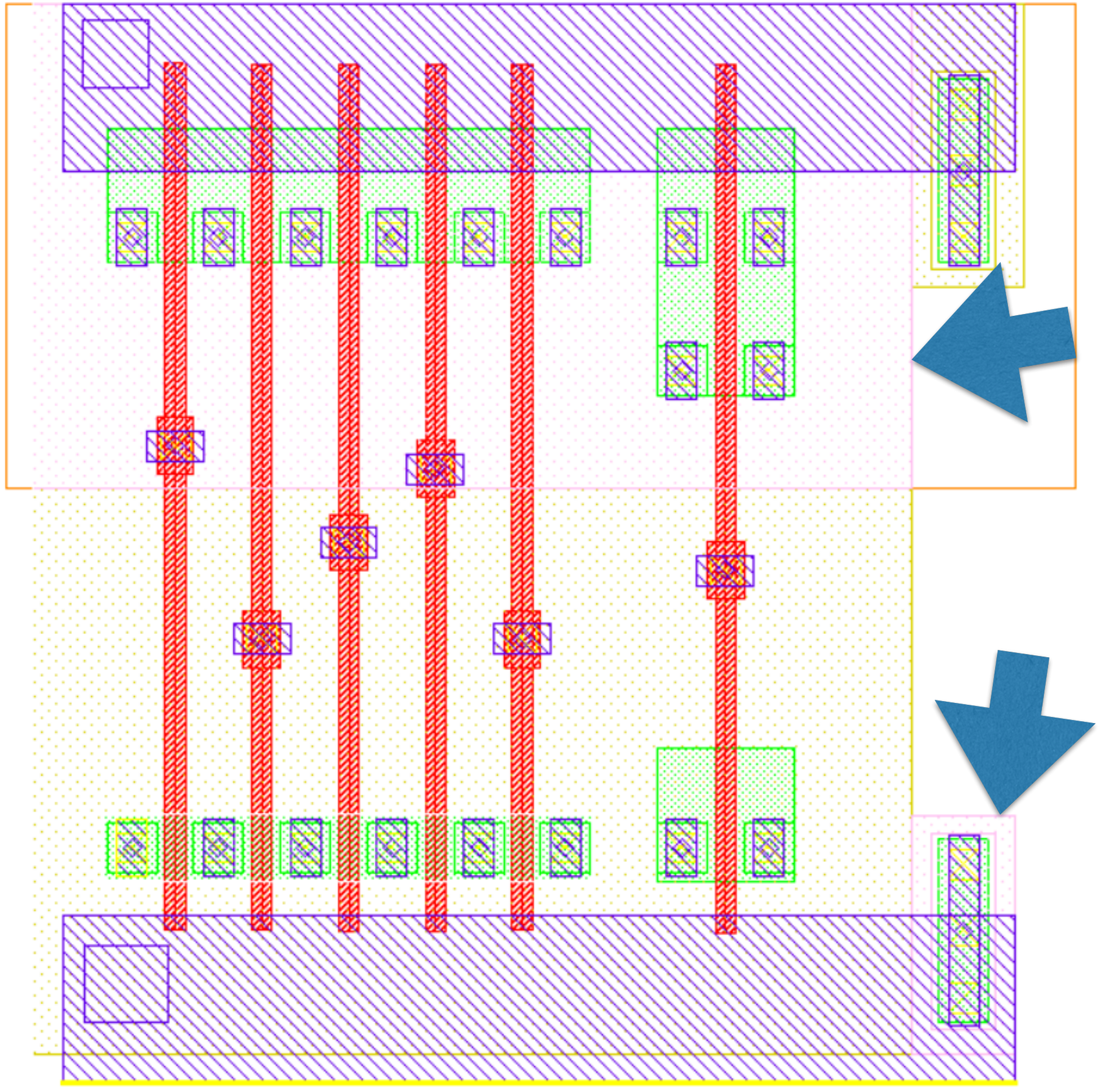
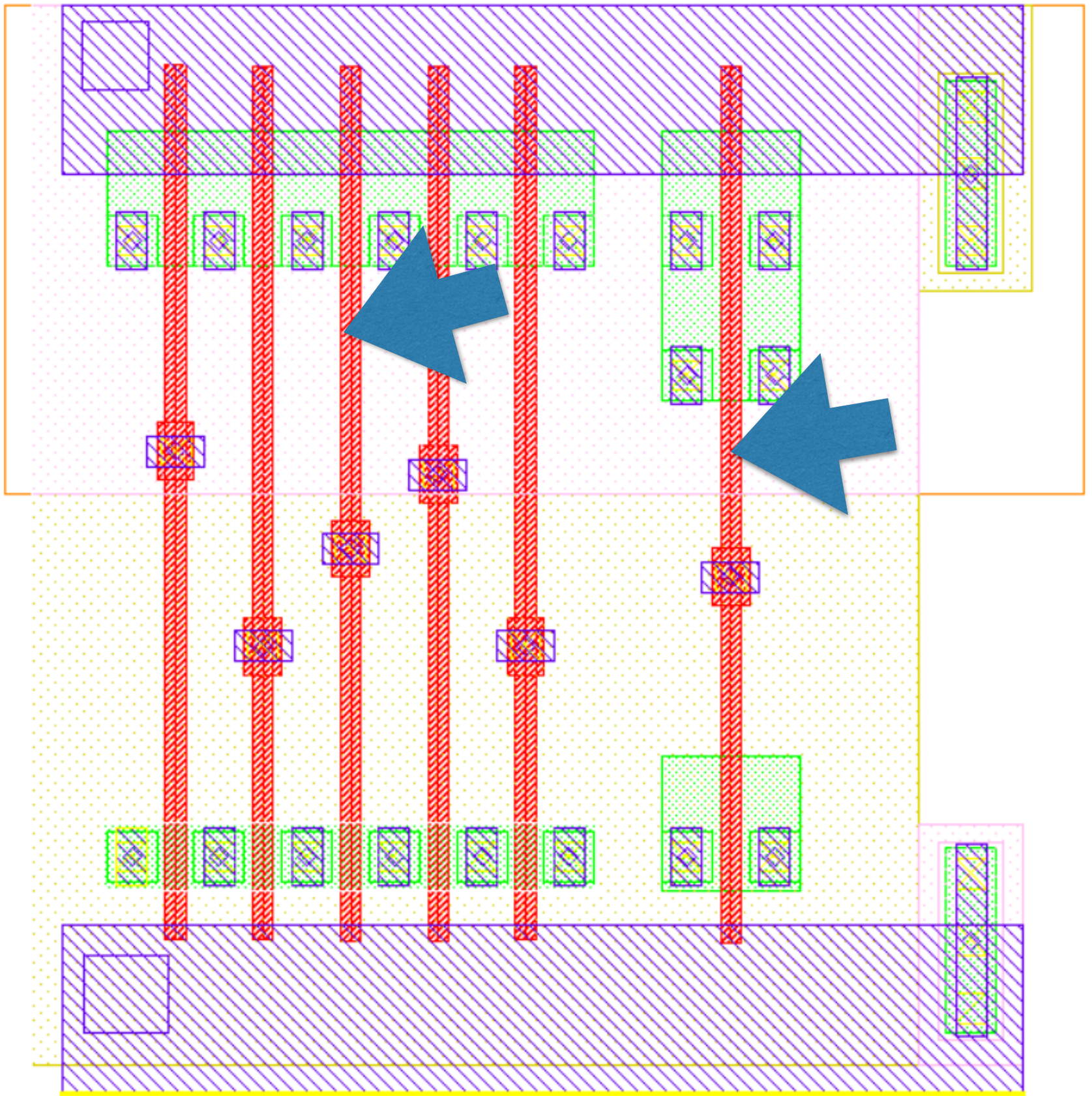


Layout quick questions

Alternatives:

A. Diffusion
B. Pplus
C. Nplus
D. N-well
E. Poly



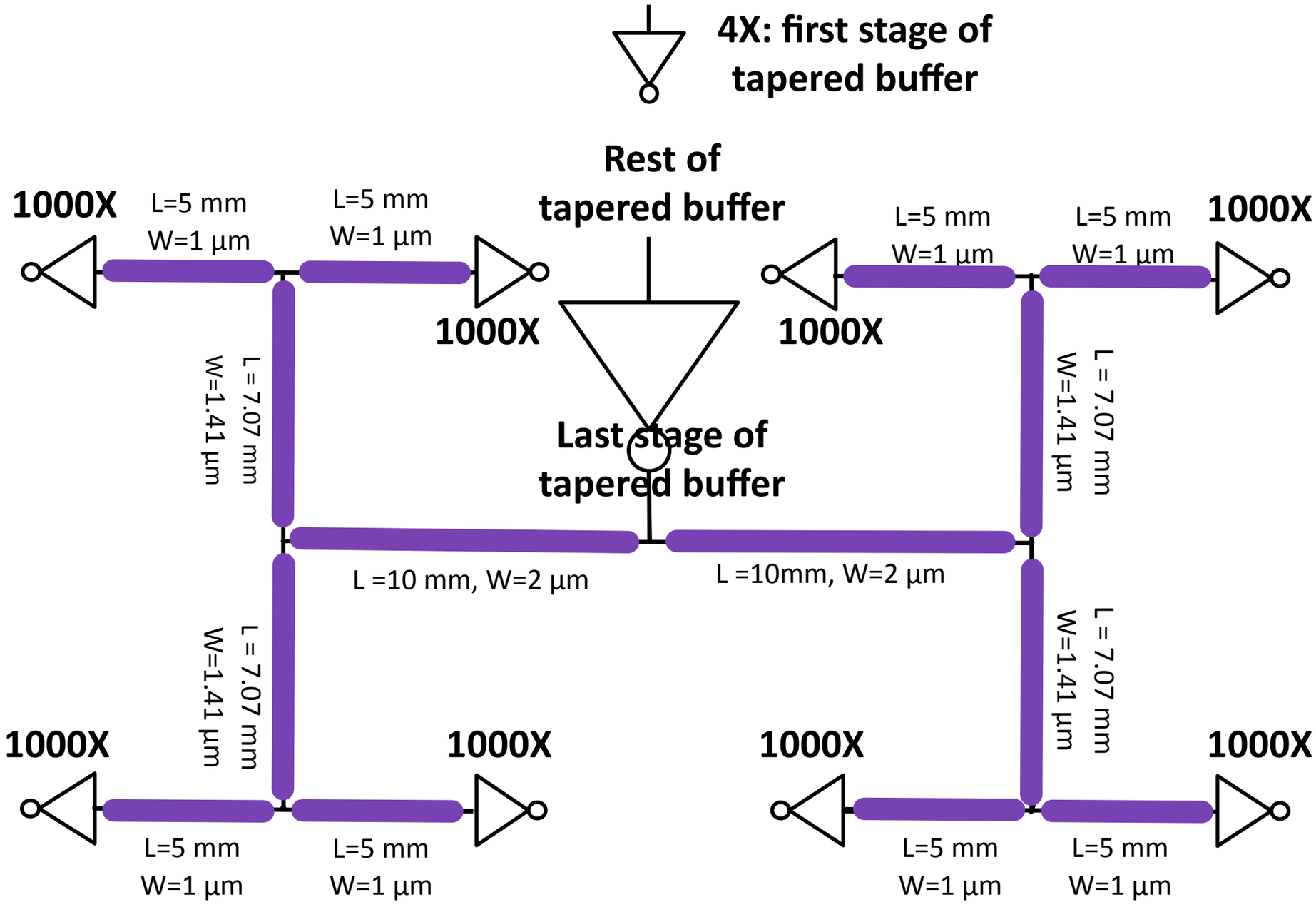
Rules

- Many rules!
- If you are to fabricate even more rules!
- Minimum area of metal 1: 0.042 μm^2
- All poly has to be covered by nplus or pplus

Layout-versus-schematics

- The graphs have to match exactly:
  - Order of transistors matter
  - If you have unconnected the NTAP from Vdd p-transistor bulks are not connected to Vdd.
  - Labels have to be exactly the same (case matters)

Prelab 4


4X: first stage of tapered buffer
Rest of tapered buffer
Last stage of tapered buffer
1000X
L=5 mm
W=1 µm
L = 7.07 mm
W=1.41 µm
L =10 mm, W=2 µm
L =10mm, W=2 µm

Lab 4

- All documents updated today!
- Clock H tree:
  - C only - design tapered buffer
  - C+R effect on delay
  - Repeaters in tree
  - Effect of skew in capacitive load of tree

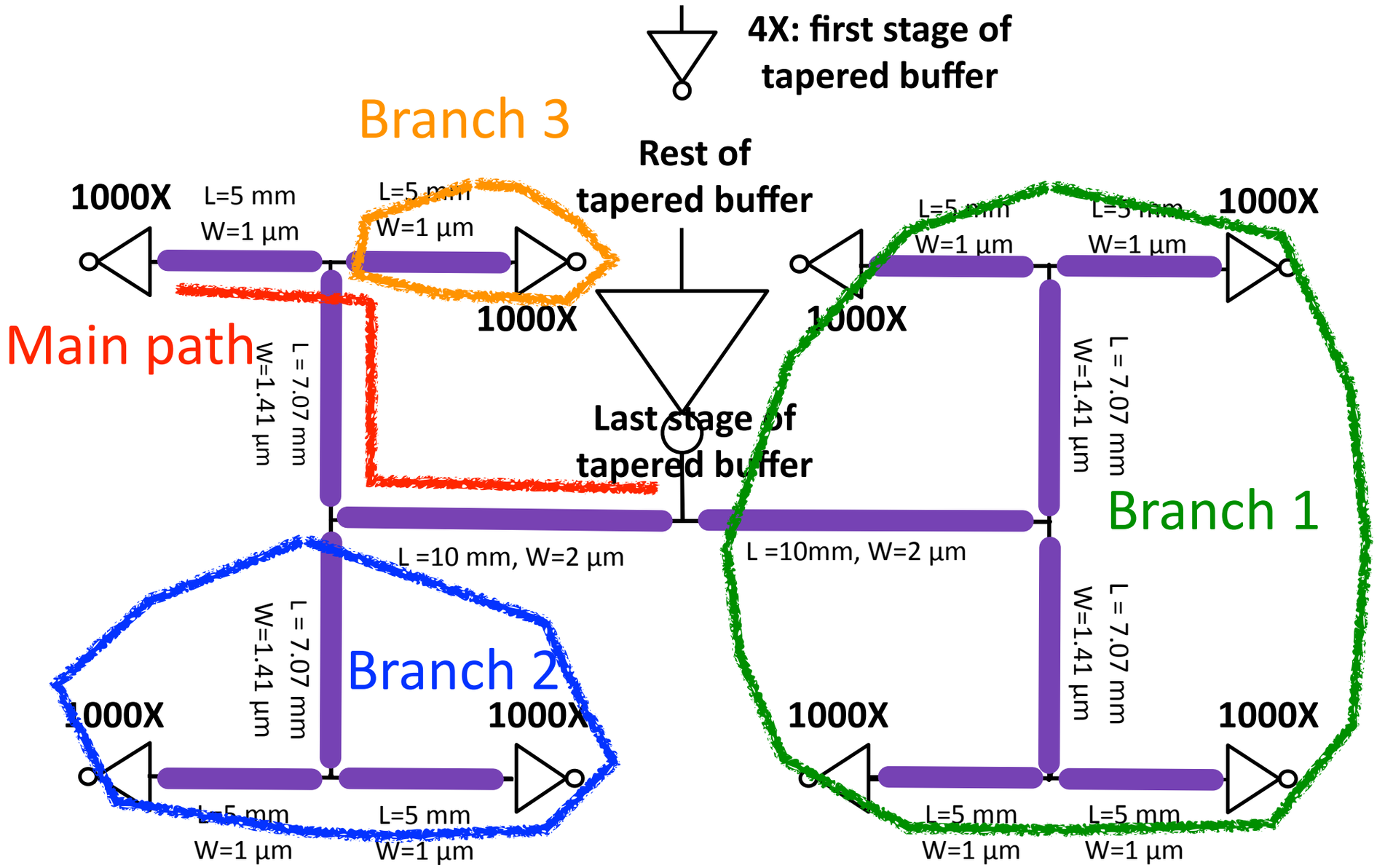
Prelab 4, calculations part 1

- Each wire segment = one pi link
- First, R_{SH}=0, that is whole tree is one big capacitance
- Design a tapered buffer to drive this huge capacitance
- How many stages, N, to use? What is f_{opt}?
  - Note that N has to be an integer, f_{opt} does not.

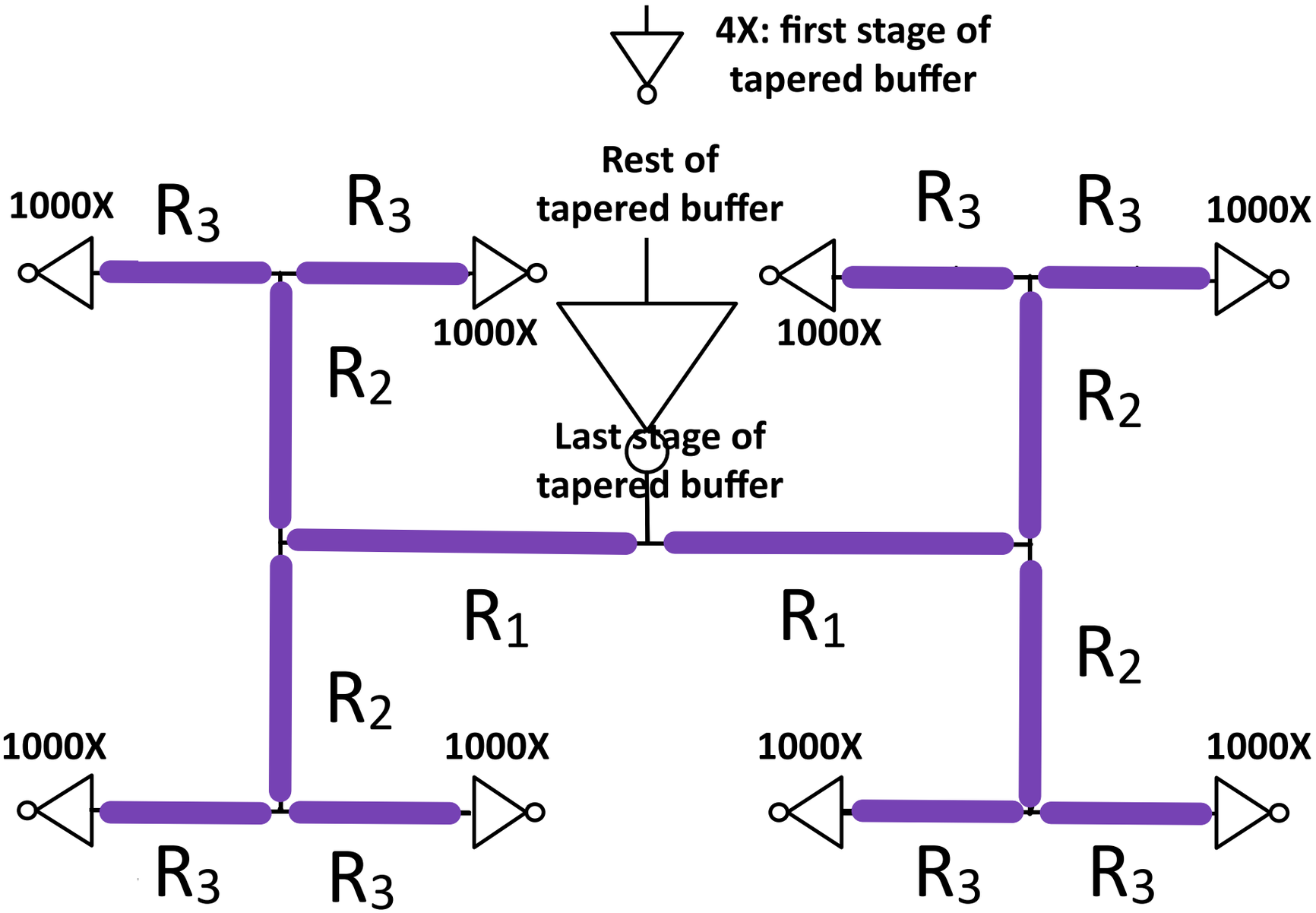
Prelab 4, calculations part 2

- Assume $R_{SH} \neq 0$
- Calculate delay to leaves using Elmore model
- Collapsed tree helps!

H-tree branching

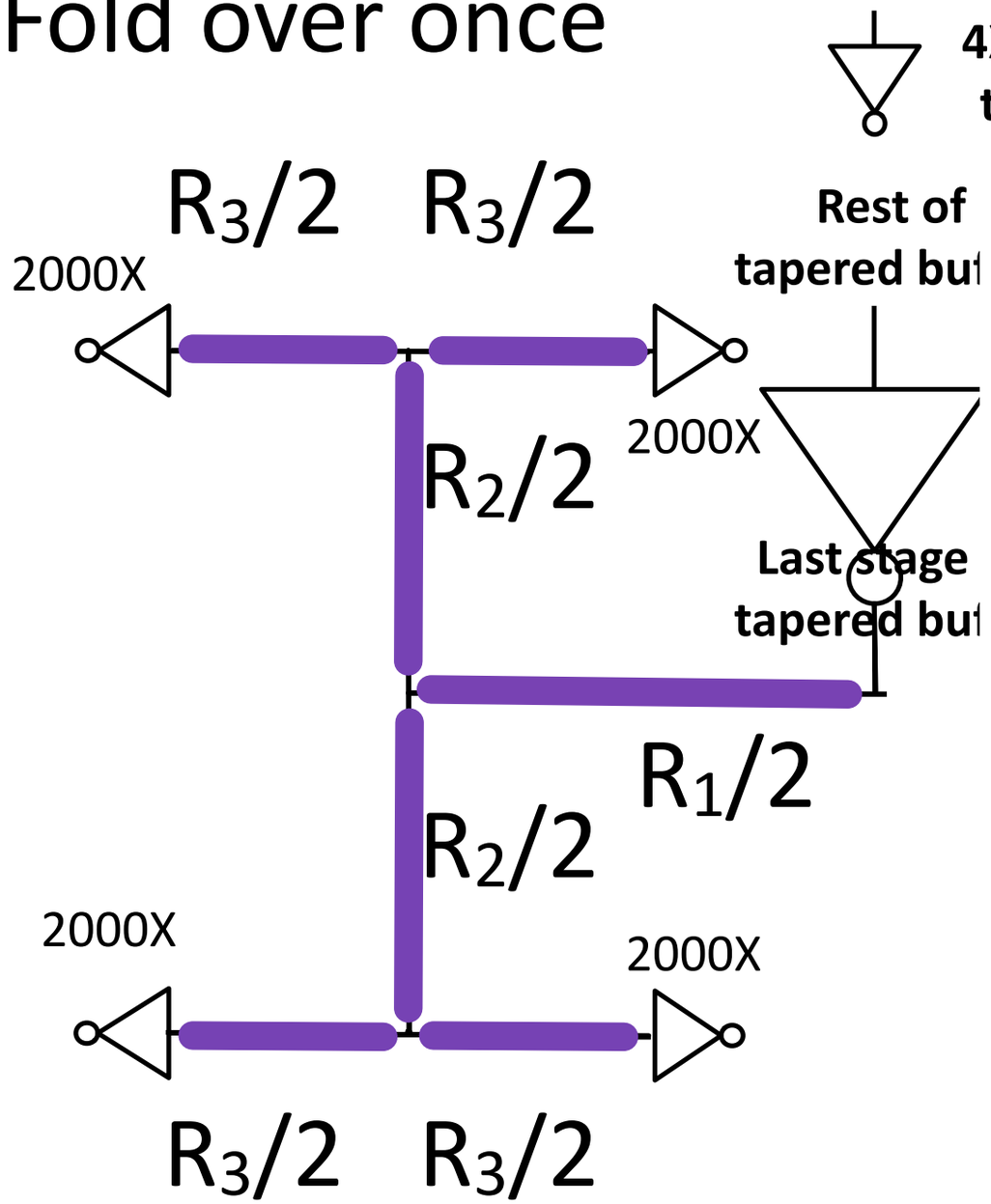


H-tree collapsing



H-tree collapsing

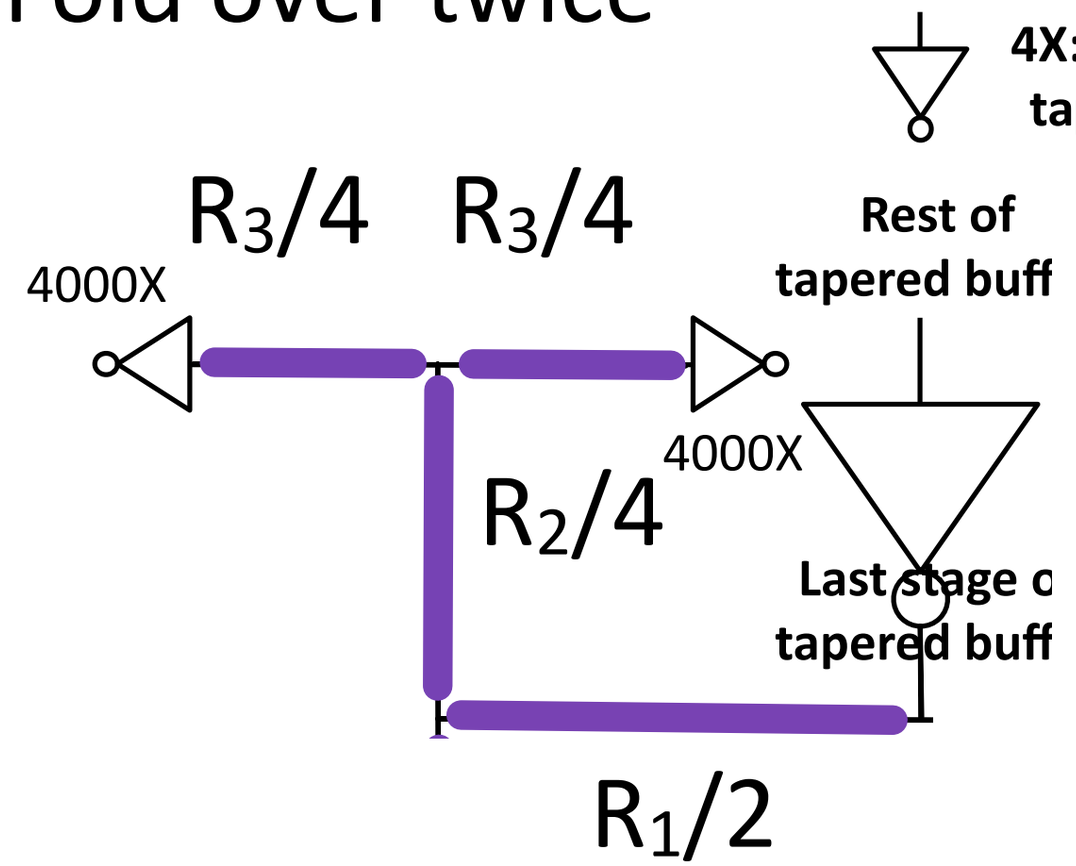
Fold over once



And wire capacitances in parallel are added

H-tree collapsing

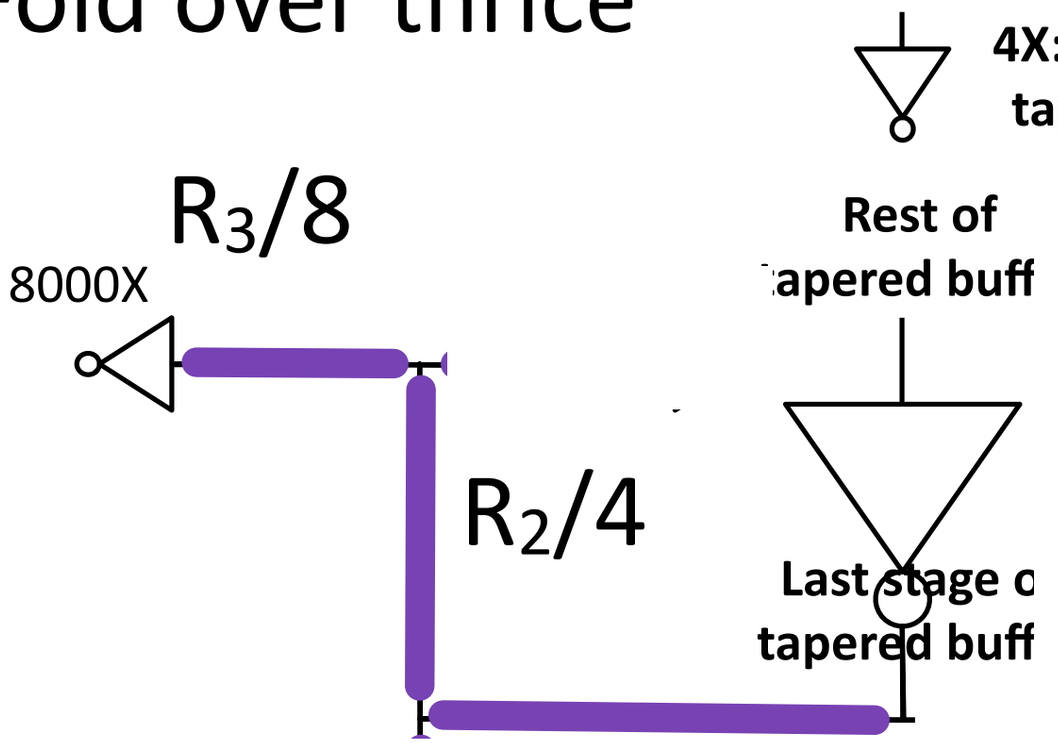
Fold over twice



And wire capacitances in parallel are again added

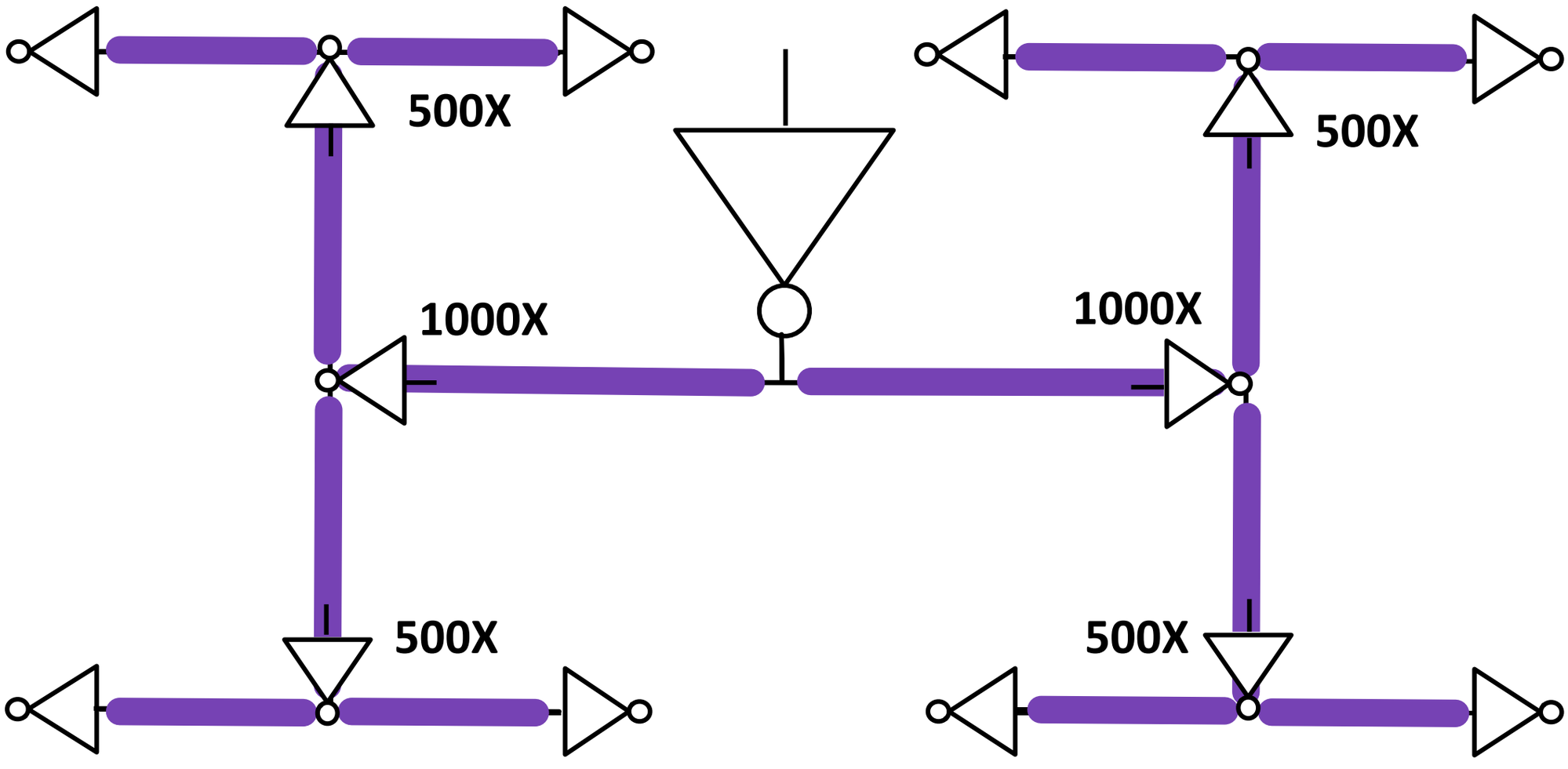
H-tree collapsing

Fold over thrice



And wire capacitances are added again

Prelab 4, calculations part 3



Prelab 4

- We will use Spectre with command-line input.
- Write the Spectre input file properly!
  - Otherwise you have to spend valuable lab time doing that.
  - File will be copied to `heffalump` before lab.
- Consultation times:
  - Thursday 9.15-10 w. Victor
  - Thursday 16.00-17.00 w. Lena
  - Friday 9-10 w. Lena