MCC092 Lab 1 review

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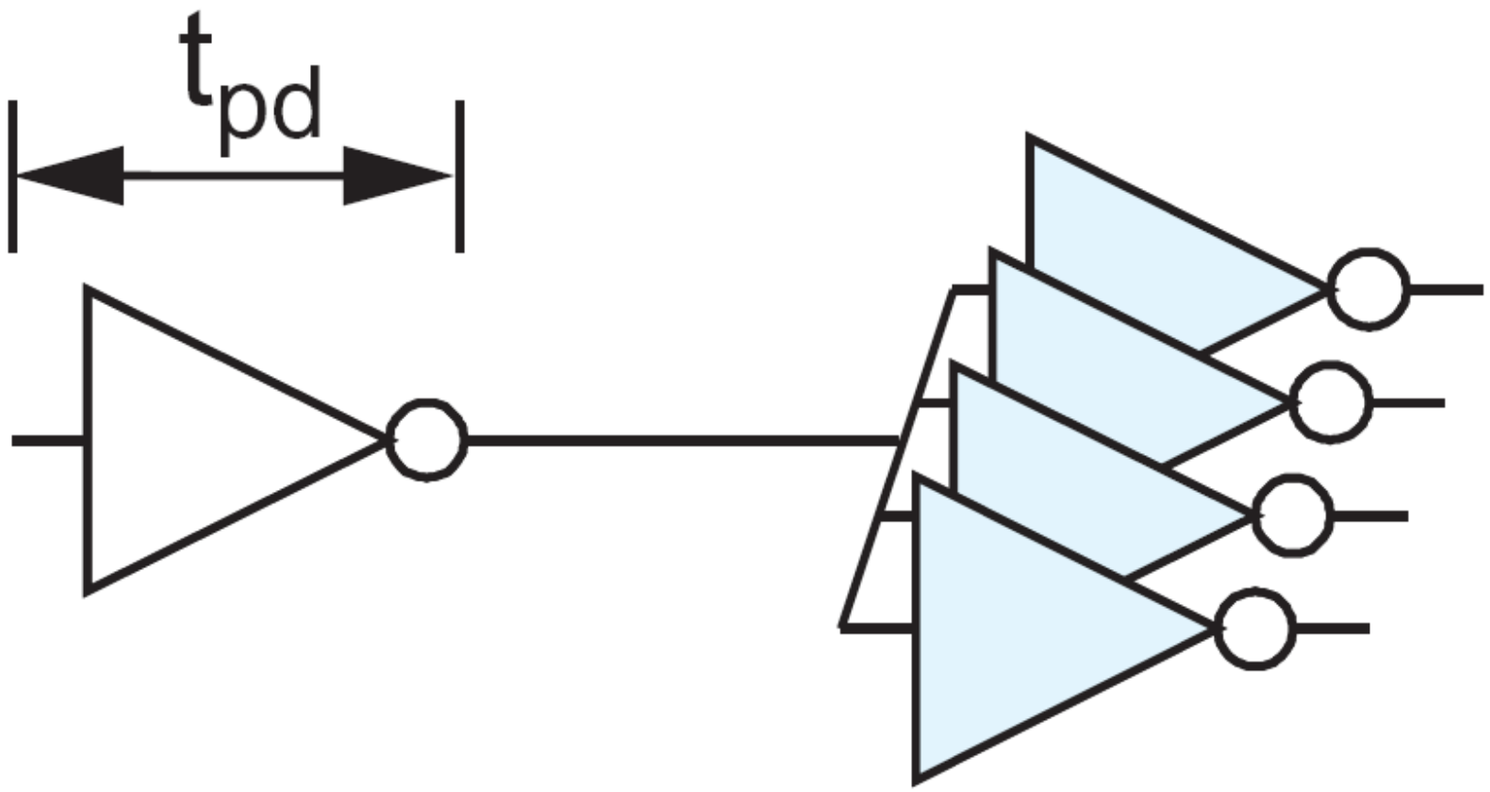
2018-09-18

Content

- Inverter schematic and cell
- Dynamic: FO4 propagation delay
  - Rise and fall time
  - Rise and fall delays
- Static
  - Switching voltage
  - Noise margins
- Extras

Why did the FO4 V_{DD} current look so strange?



family

Subwindows: 1

Data Point 936470588m

Classic

lab1 invFO4-tb schematic

Transient Response

Wed Sep 14 21:56:32 2016 1

Name | Vis

/in

/out

/V0/PLUS

/V0/PLUS
520.0223ps
-150.524uA

V (V)

I (uA)

time (ps)

mouse L: M: R:

12(25) Trace: /V0/PLUS; Context: /chalmers/users/lenap/test2016/simulation/invFO4-tb/spectre/schematic/psf; Dataset: tran-tran

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cadence

Subwindows: 1

Data Point 936470588m

family

Classic

lab1 invFO4-tb schematic

Transient Response

Wed Sep 14 21:56:32 2016 1

Name | Vis

/in

/out

/V0/PLUS

/V0/PLUS
1.0151307ns
-72.9785uA

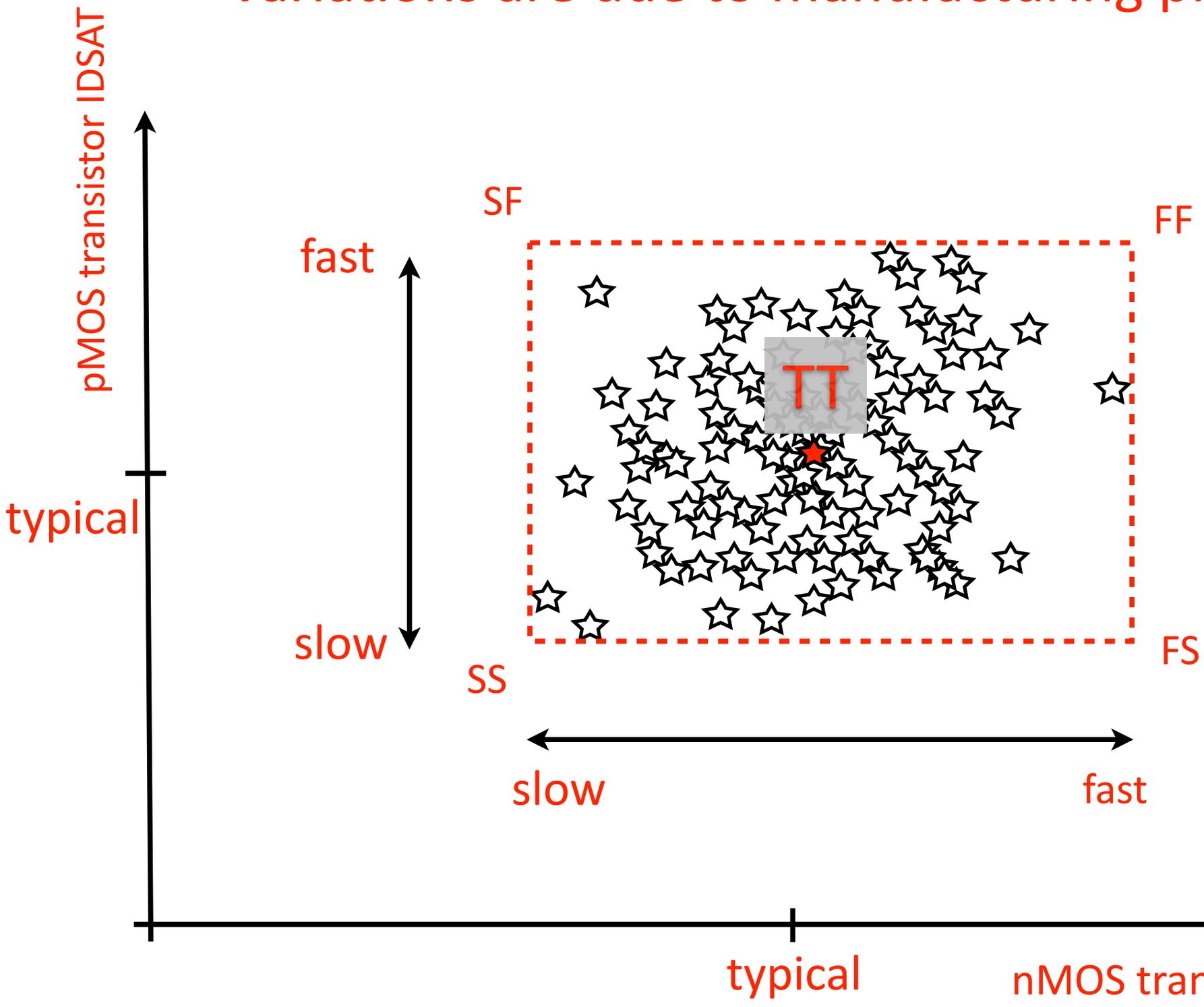
V (V)

I (uA)

time (ns)

What are process corners?

Variations are due to manufacturing process



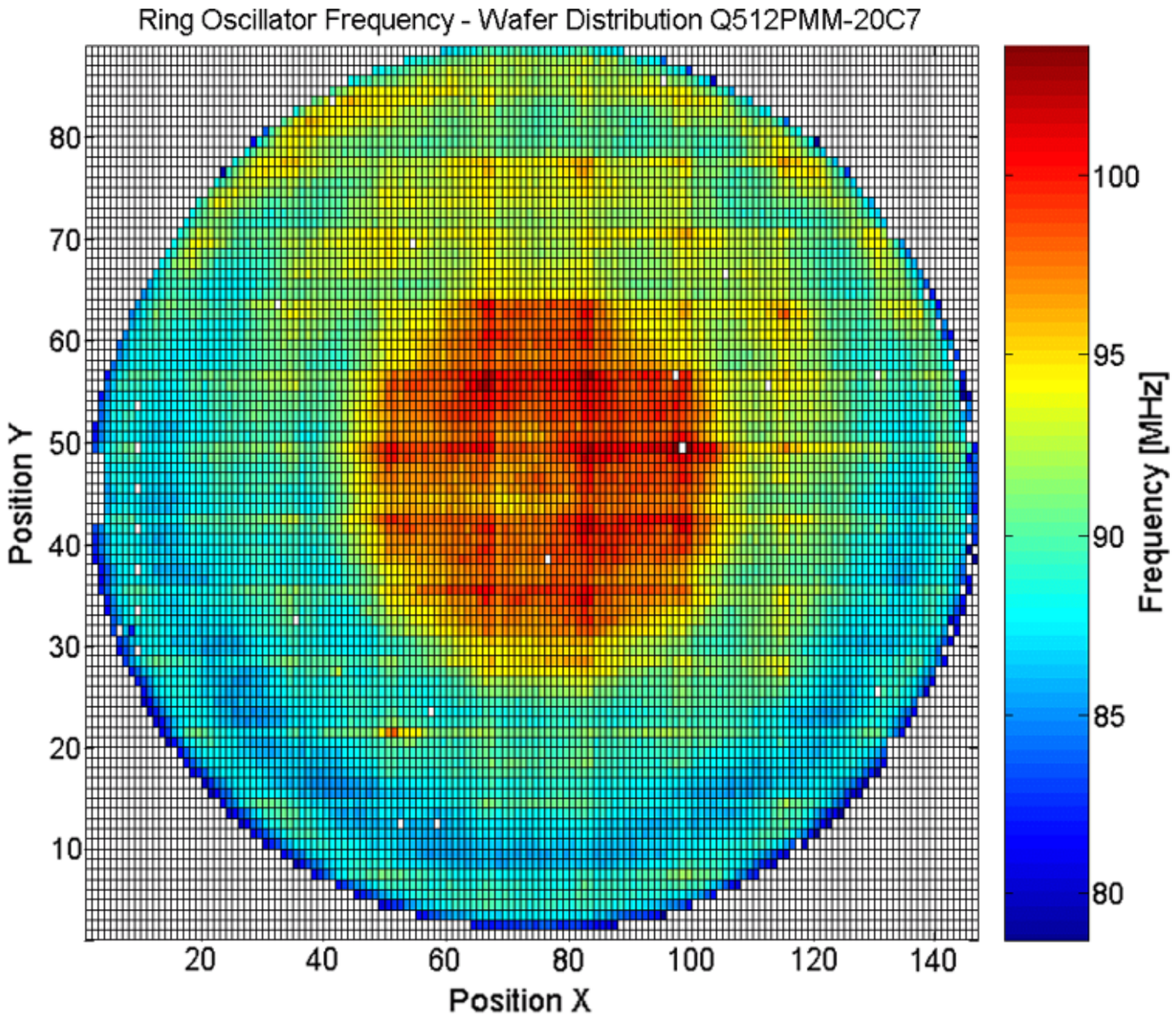
As a designer you have to *verify* that your design fulfils the specifications for all possible cases.

Note: There is no way to *design* for a particular corner.

Common question: What is the worst case?

Binning is also a possibility.

Binning



Variability:
The exact same chip
may differ in speed due to
variability in manufacturing
process.

Binning:
Test chips and sort them
according to speed.
Charge more for faster ones.

Subwindows: 1 | Data Point :986727270n | Classic

lab1 invFO4-tb schematic

ient Response

Wed Sep 14 21:56:32 2016 1

Vis

/in
/out
/V0/PLUS
/in
/out
/V0/PLUS
/in
/out
/V0/PLUS

M9: 1.0216872ns 589.53909mV

M10: 1.0298673ns 596.84305mV

M8: 1.0049277ns 591.32823mV

dx: 24.939537ps
dy: 5.51482mV
s: 221.12758MV/s

SSt

dx: 16.759431ps
dy: 1.78914mV
s: 106.75411MV/s

FFt

V (V)

I (uA)

1.3 1.2 1.1 1.0 0.9 0.8 0.7 0.6 0.5 0.4 0.3 0.2 0.1 0.0 -0.1

120.0 100.0 80.0 60.0 40.0 20.0 0.0 -20.0 -40.0 -60.0 -80.0 -100.0 -120.0 -140.0 -160.0 -180.0 -200.0 -220.0 -240.0 -260.0 -280.0

0.975 0.985 0.995 1.005 1.015 1.025 1.035 1.045 1.055 1.065 1.075

time (ns)

e L: M: R:

Trace: /out; Context: /chalmers/users/lenap/test2016/simulation/invFO4-tb/spectre/schematic/psf; Dataset: tran-tran

Virtuoso (R) Visualization & Analysis XL

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cadence

Subwindows: 1

Data Point .348669200p

family

Classic

lab1 invFO4-tb schematic

Transient Response

Wed Sep 14 21:56:32 2016 1

Name | Vis

/in
/out
/V0/PLUS
/in
/out
/V0/PLUS
/in
/out
/V0/PLUS

M12: 532.8654ps 600.1922mV

M11: 515.0561ps 593.2679mV

M13: 539.3487ps 600.9443mV

dx: 17.80925ps
dy: 6.92429mV
s: 388.8033MV/s

FFt

dx: 24.29257ps
dy: 7.67641mV
s: 315.9981MV/s

SSt

V (V)

I (uA)

time (ps)

mouse L: M: R:

Does it compute?

L=60 nm, W=1 μm	SS corner	TT corner	FF corner	
$I_{DSAT,N}$	500	600	800	μA/μm
$I_{DSAT,P}$	250	300	400	μA/μm

How much slower is SS? -20 %

How much faster is FF? + 33%

If we assume the capacitances remain the same.

Virtuoso (R) Visualization & Analysis XL

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cadence

Subwindows: 1

Data Point .348669200p

family

Classic

lab1 invFO4-tb schematic

Transient Response

Wed Sep 14 21:56:32 2016 1

Name Vis

/in
/out
/V0/PLUS
/in
/out
/V0/PLUS
/in
/out
/V0/PLUS

V (V)

1.3 1.2 1.1 1.0 0.9 0.8 0.7 0.6 0.5 0.4 0.3 0.2 0.1 0.0 -0.1

I (uA)

120.0 100.0 80.0 60.0 40.0 20.0 0.0 -20.0 -40.0 -60.0 -80.0 -100.0 -120.0 -140.0 -160.0 -180.0 -200.0 -220.0 -240.0 -260.0 -280.0

0.99 1.0 1.01 1.02 1.03 1.04 1.05 1.06 1.07 1.08 1.09

time (ns)

mouse L: M: R:

12(25) Trace: /V0/PLUS; Context: /chalmers/users/lenap/test2016/simulation/invFO4-tb/spectre/schematic/psf; Dataset: tran-tran

Virtuoso (R) Visualization & Analysis XL

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cadence

Subwindows: 1

Data Point .348669200p

family

Classic

lab1 invFO4-tb schematic

Transient Response

Wed Sep 14 21:56:32 2016 1

Name Vis

/in
/out
/V0/PLUS
/in
/out
/V0/PLUS
/in
/out
/V0/PLUS

/V0/PLUS
510.3718ps
-81.2626uA

V (V)

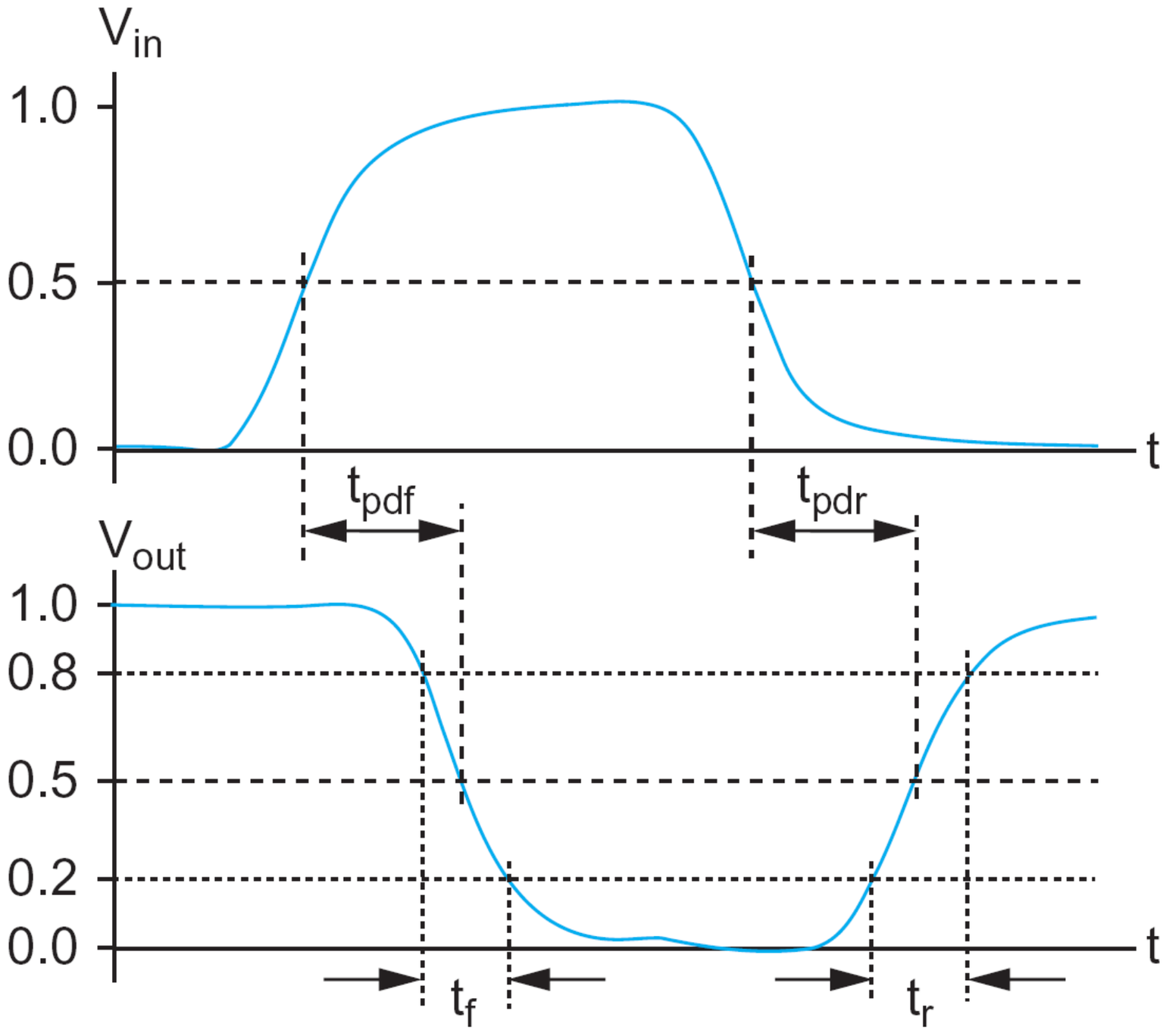
I (uA)

time (ps)

mouse L: M: R:

12(25) Trace: /V0/PLUS; Context: /chalmers/users/lenap/test2016/simulation/invFO4-tb/spectre/schematic/psf; Dataset: tran-tran

Rise/fall time and delay



Analysis types

- Transient analysis
  - In time, nonlinear and with capacitances
- DC analysis
  - No time, no capacitances (but still nonlinear)
  - Changes wrt some parameter, for example a source voltage

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cadence

Subwindows: 1 | Data Point 155934833m | family | Classic

lab1 inv-tb schematic

DC Response

Wed Sep 14 21:29:32 2016 1

Name | Vis

/net4
/net1
/gnd!
/vdd!

M4: 559.227m 935.813mV

M5: 627.156m 363.042mV

Δ dx: 67.929m
dy: 572.771mV
s: 8.43192V/

V (V)

1.3 1.2 1.1 1.0 0.9 0.8 0.7 0.6 0.5 0.4 0.3 0.2 0.1 0.0 -0.1

0.0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0 1.1 1.2

VIN

mouse L: M: R:

Virtuoso (R) Visualization & Analysis XL

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cadence

Subwindows: 1 | Data Point | 936470588m | family | Classic

lab1 inv-tb schematic

DC Response

Wed Sep 14 21:29:32 2016 1

Name | Vis

/net4

/net1

/gnd!

/vdd!

M6: 566.8597m 881.6961mV

M7: 626.9365m 364.8655mV

dx: 60.07674m
dy: 516.831mV
s: 8.602841V/

max gain is only around -8.5
Why?

V (V)

1.3 1.2 1.1 1.0 0.9 0.8 0.7 0.6 0.5 0.4 0.3 0.2 0.1 0.0 -0.1

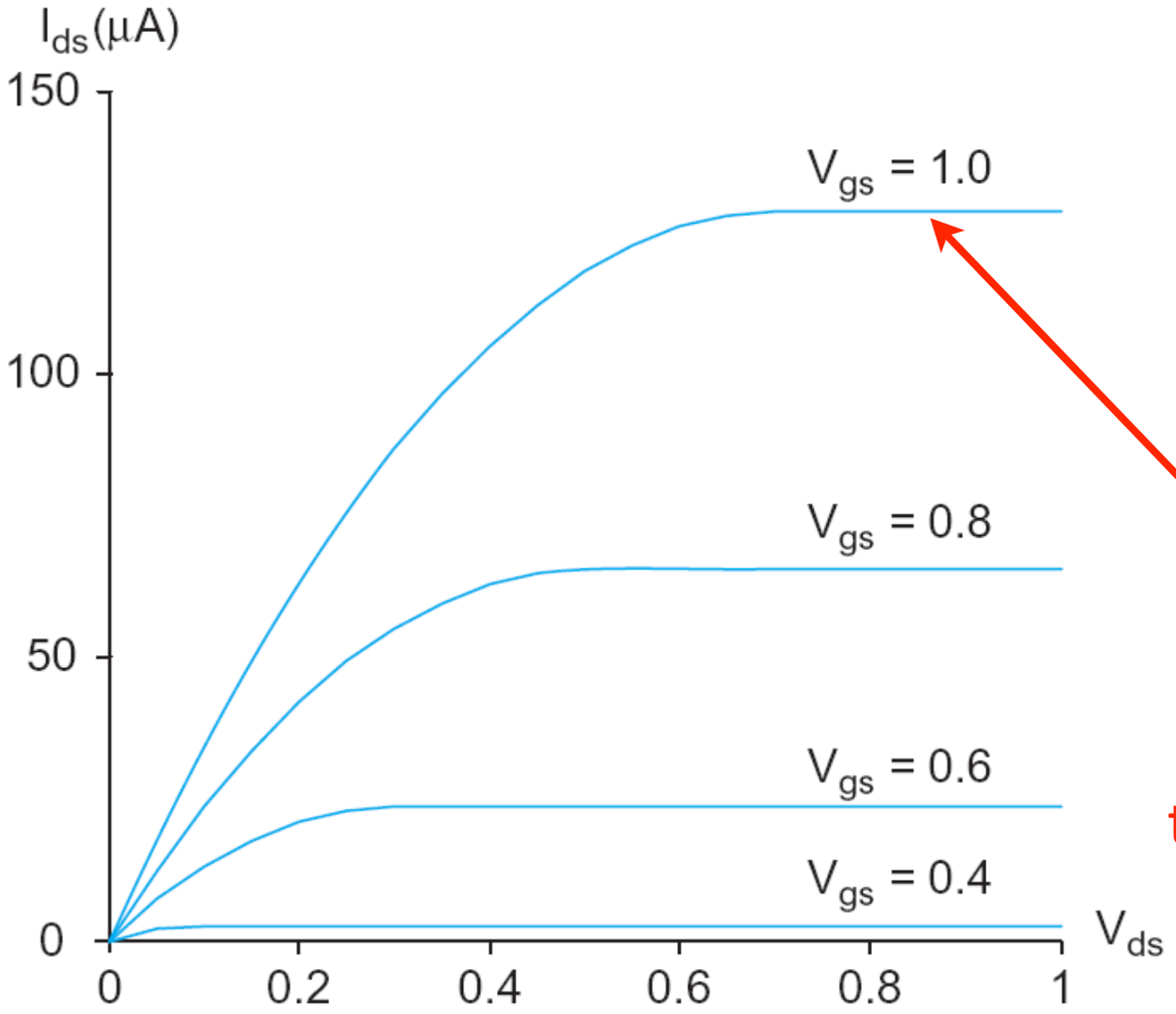
440.0 460.0 480.0 500.0 520.0 540.0 560.0 580.0 600.0 620.0 640.0 660.0 680.0 700.0 720.0 740.0

VIN (m)

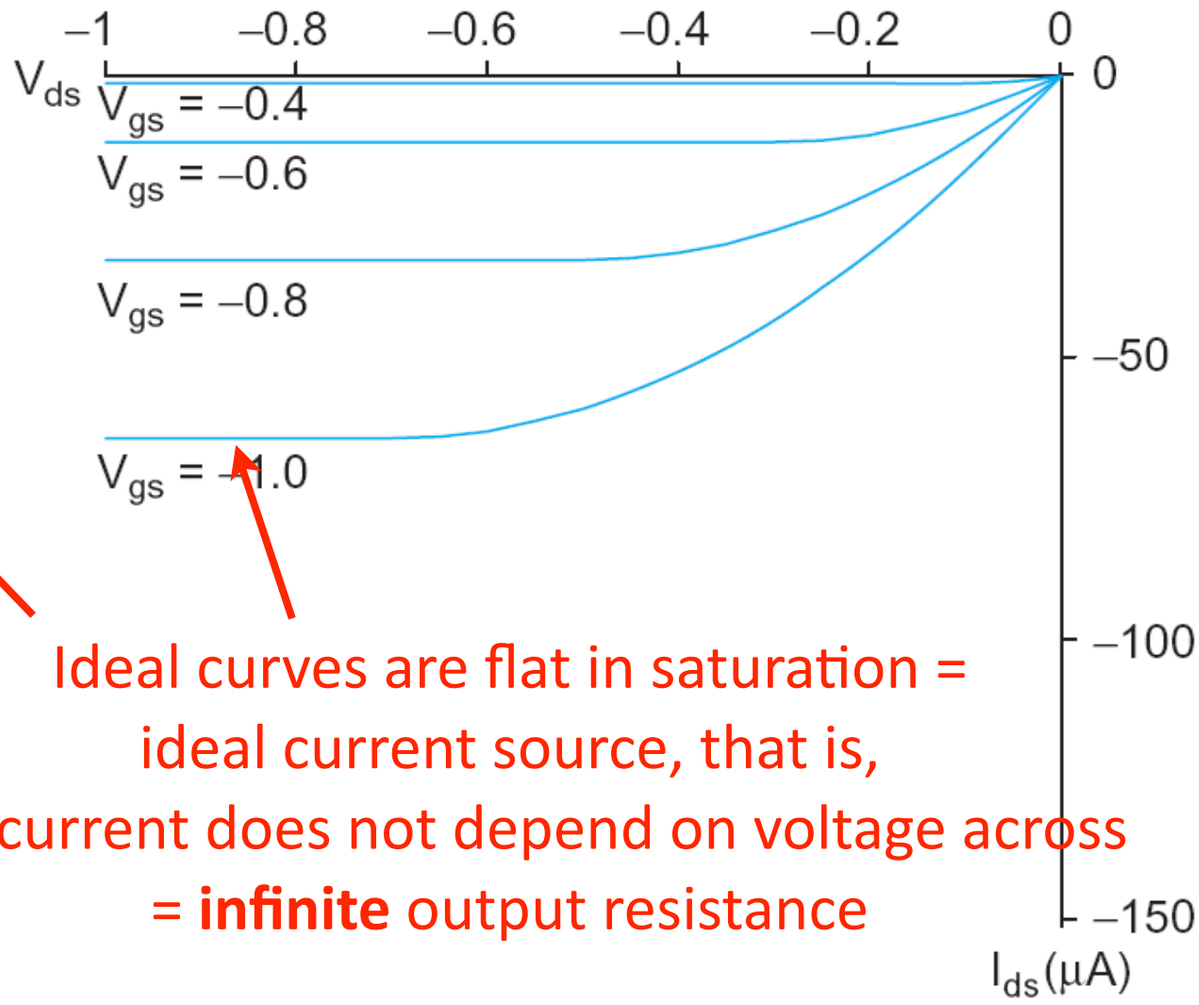
mouse L: M: R:

3(4) no error

Ideal Ids curves



(a)



(b)

Ideal curves are flat in saturation = ideal current source, that is, the current does not depend on voltage across = **infinite** output resistance

Realistic Ids curves

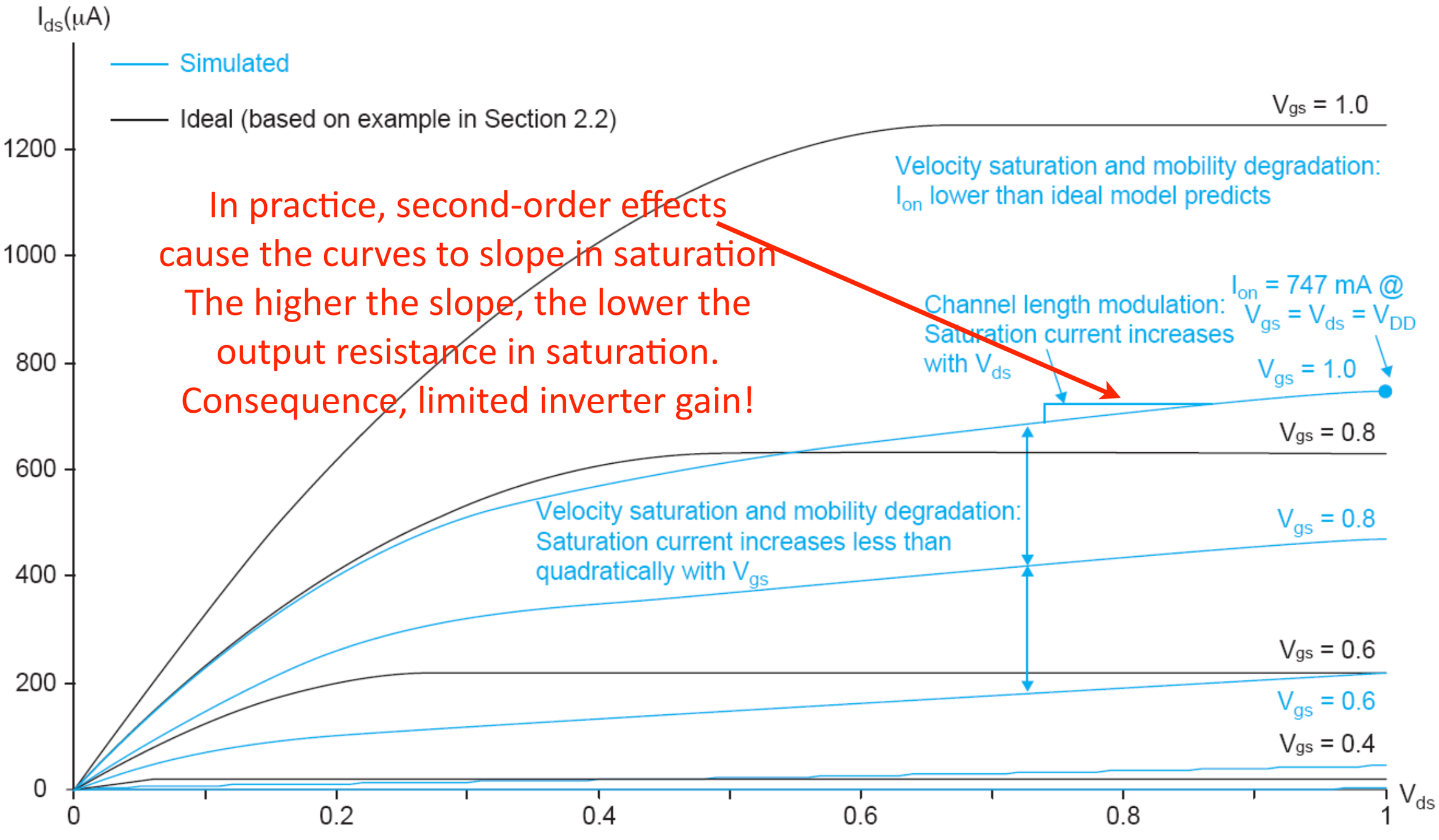


FIGURE 2.14 Simulated and ideal I-V characteristics