The CMOS Inverter

Lecture 3
Static properties
= voltage transfer curves (VTC)
and noise margins

Week 2: The CMOS inverter

- Tuesday
  - Static properties
    - Voltage transfer curves (VTC)
    - Noise margins
  - Exercise (Kjell, 1 hour)
- Thursday
  - Dynamic properties
    - Propagation delay
    - Driving large capacitive loads w. optimal propagation delay
  - Exercise POTW (Victor, 2 hours)
- Friday
  - Prelab 1 deadline 1PM

What happened last week?

- Let's do a quiz about the transistor:
  - Go to socrative.com
  - Select Student login
  - Go to room: "MCC0922018"

Where are we?

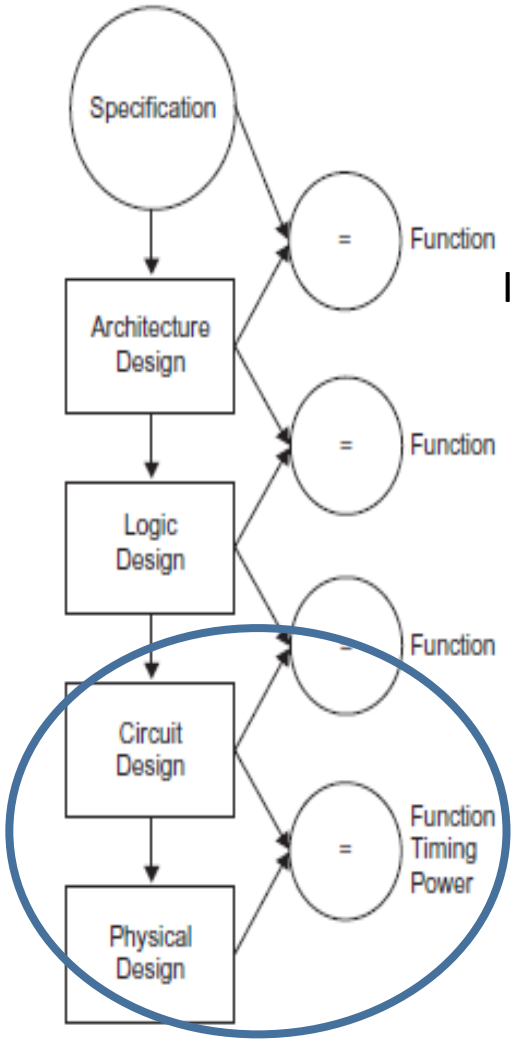
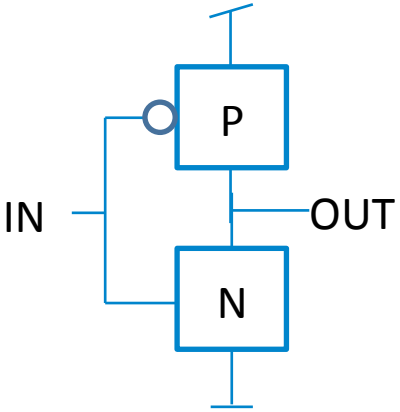
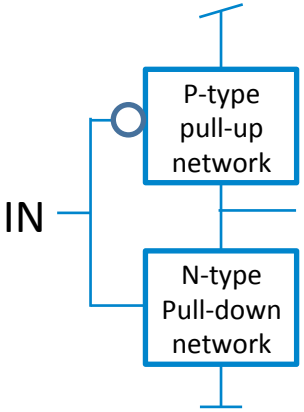


FIGURE 1.70 Design and verification sequence

Inverter

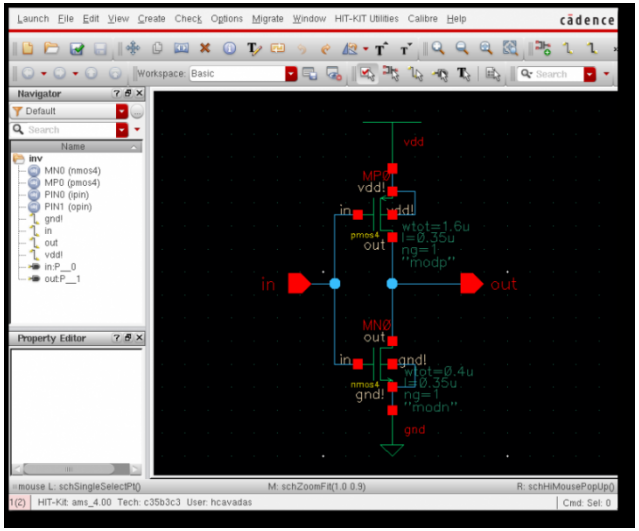


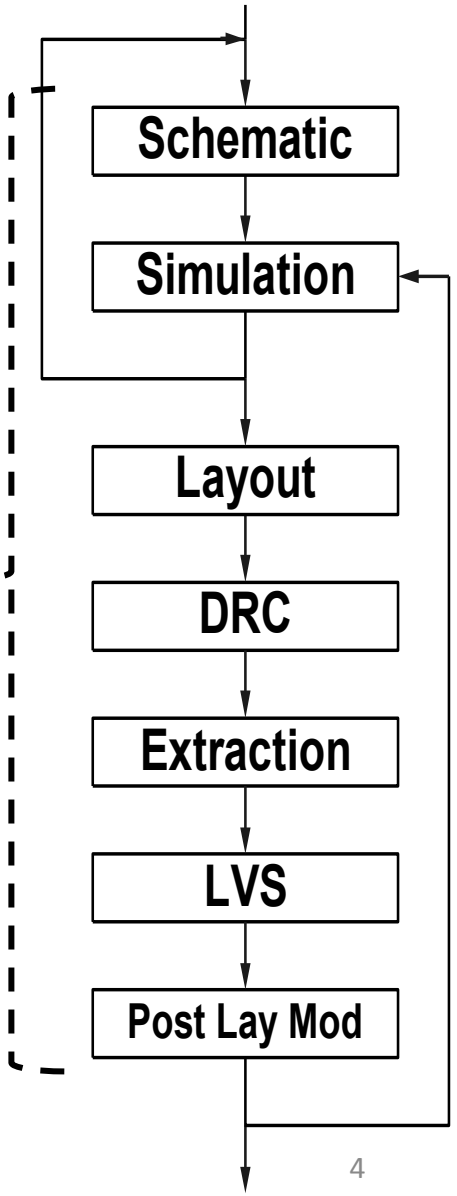
Logic gates



Designing w switches

Hands-on lab session





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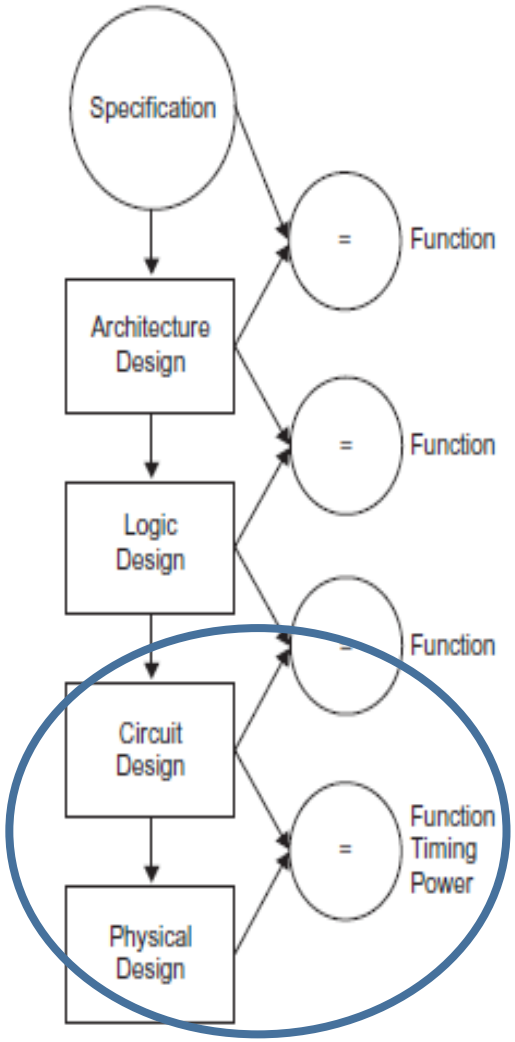

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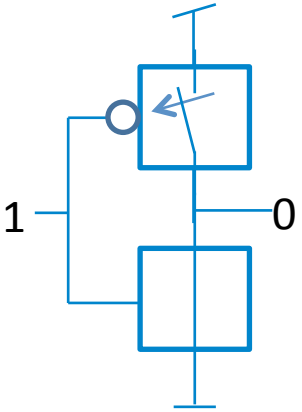

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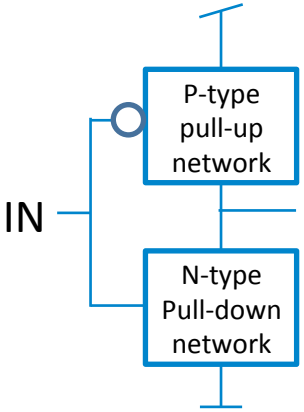

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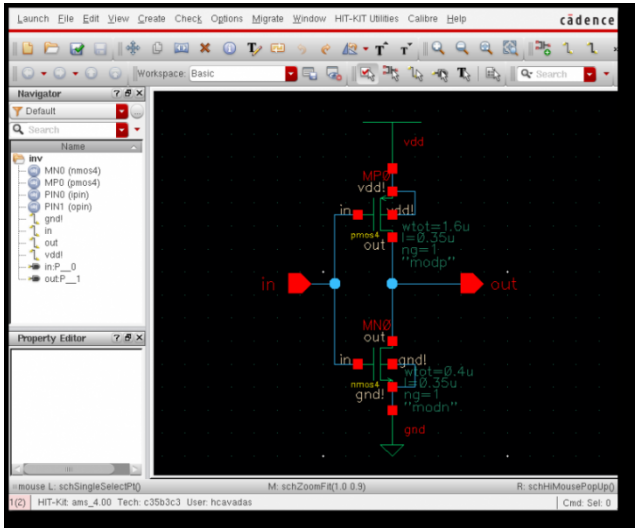

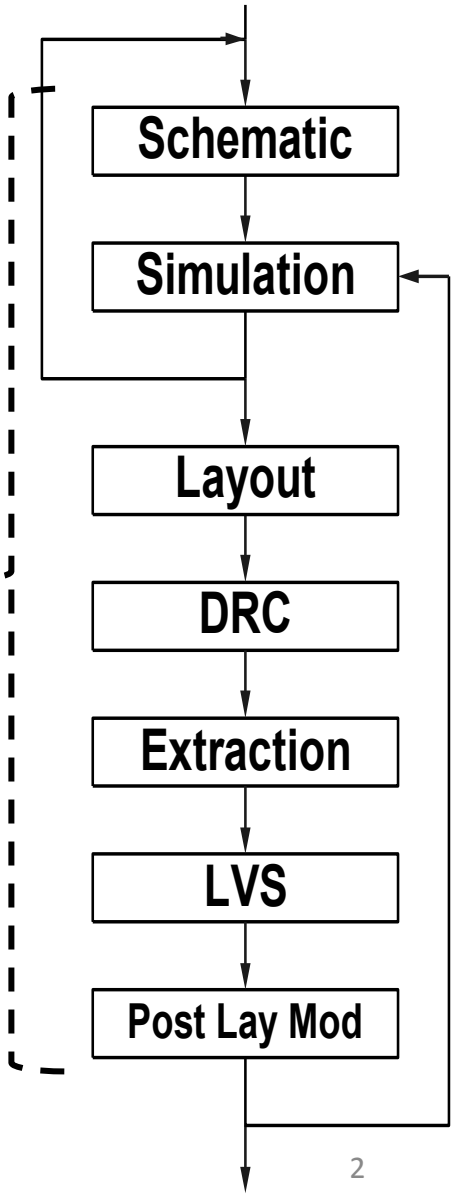

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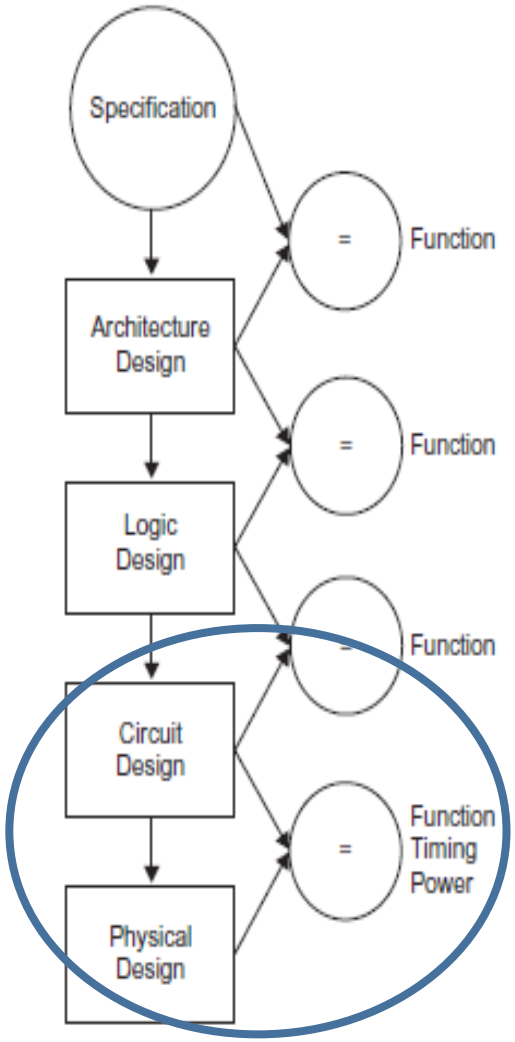

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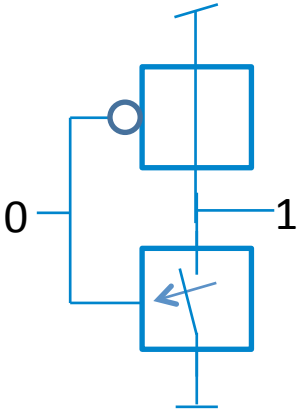

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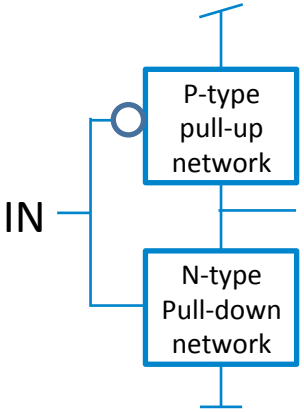

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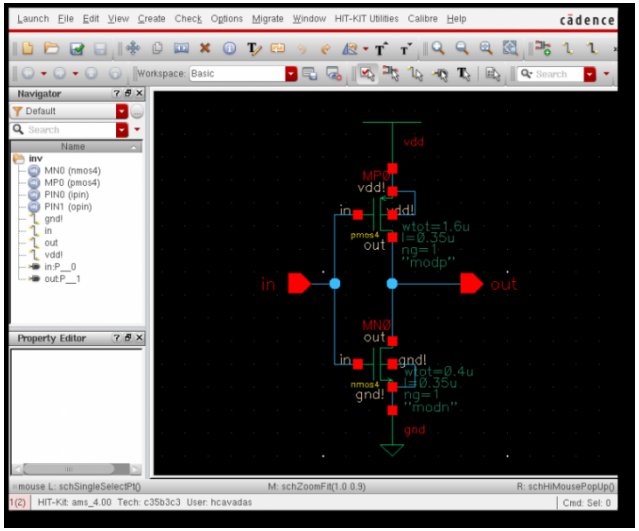

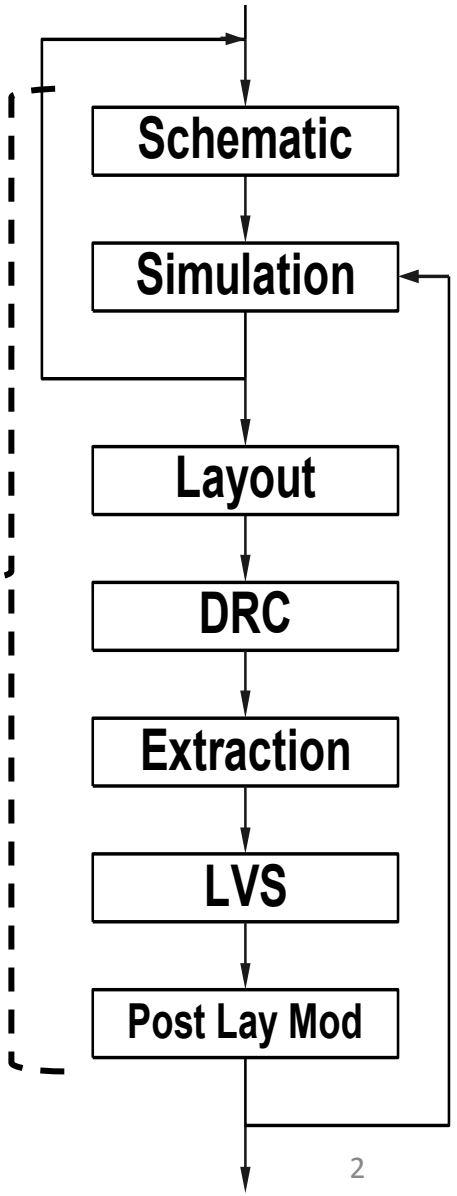

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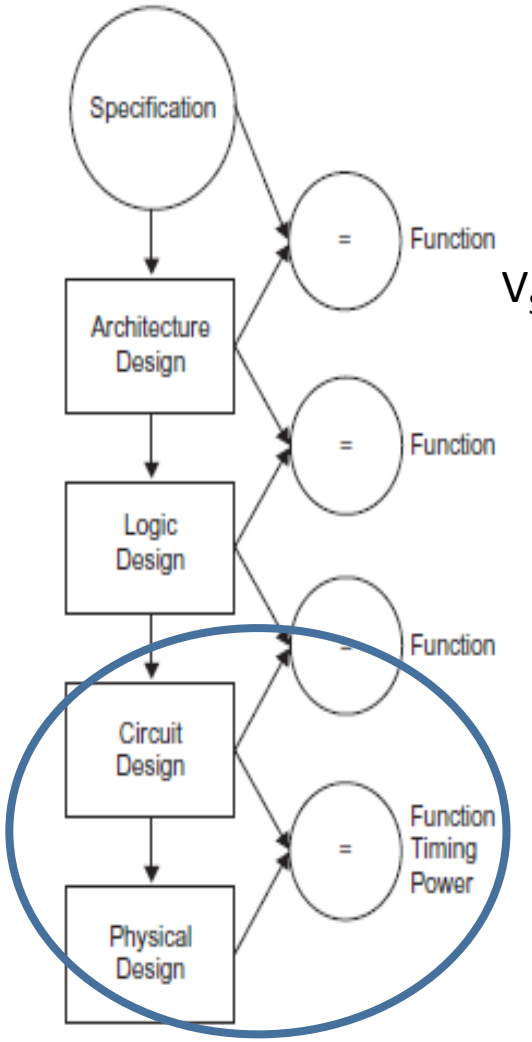

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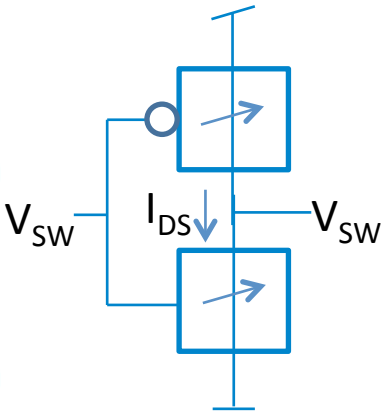

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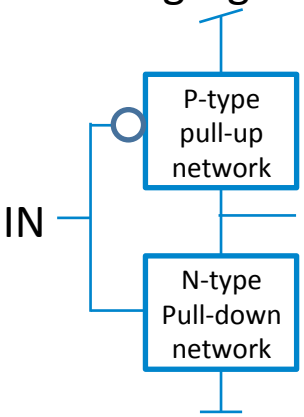

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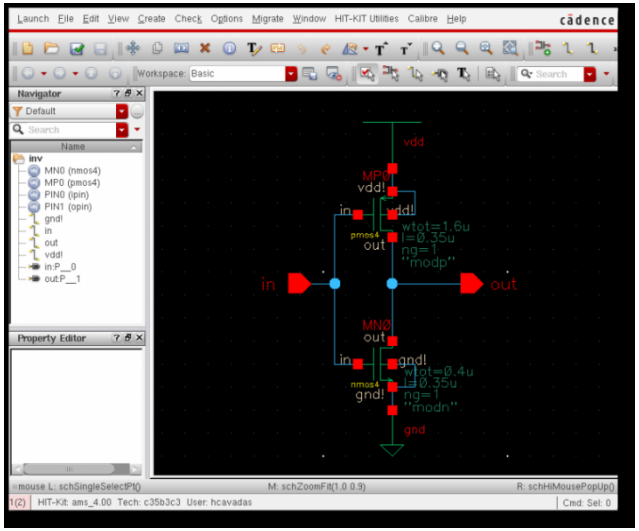
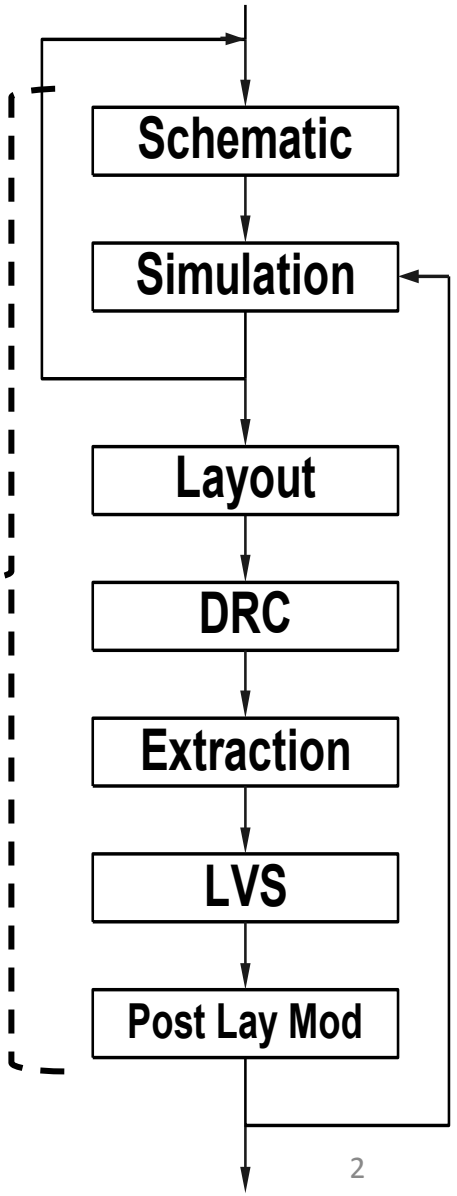
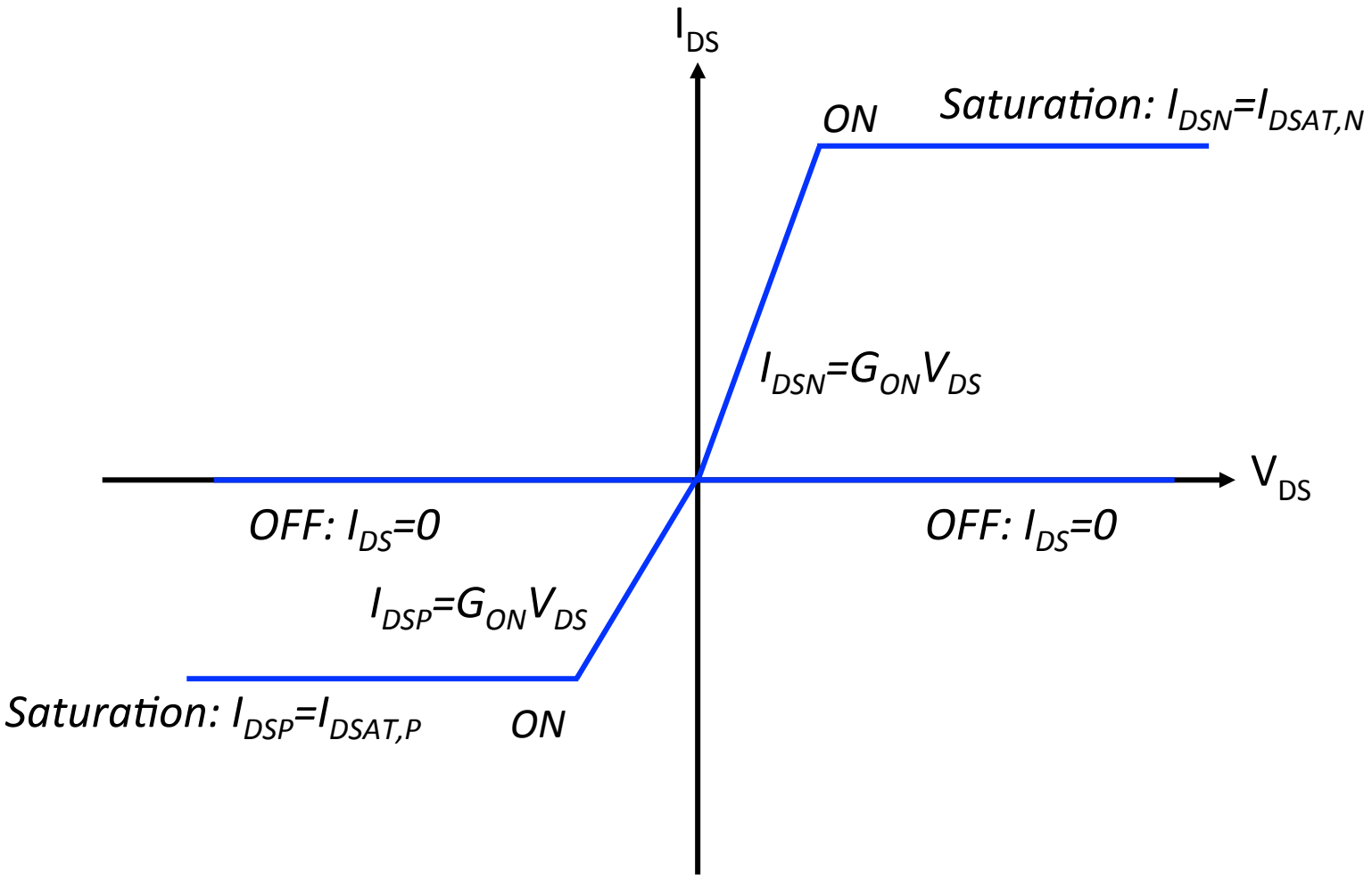




MOSFET I/V Characteristics



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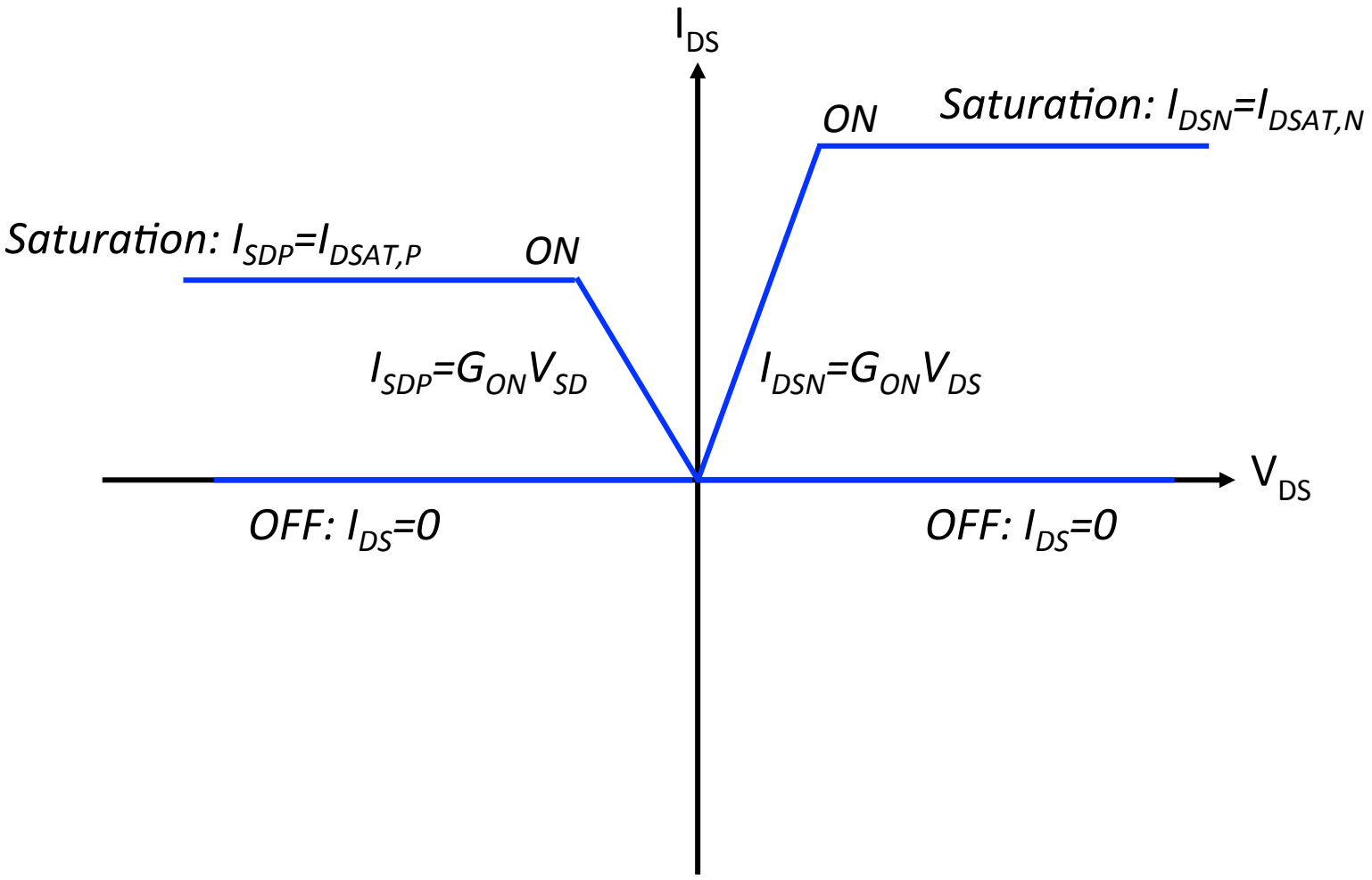

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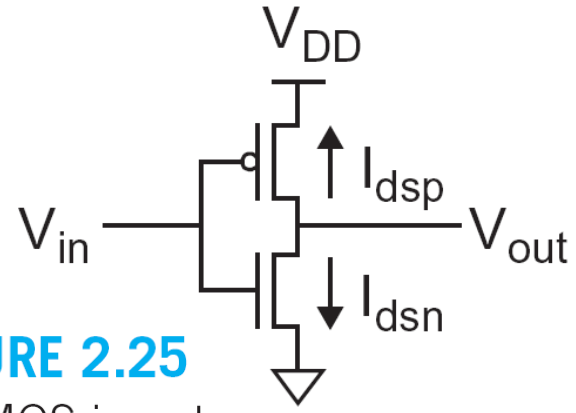
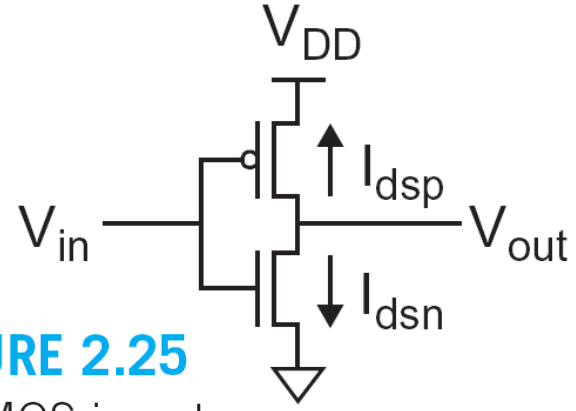


FIGURE 2.25
A CMOS inverter

V_{IN}/V_{OUT} voltage plane



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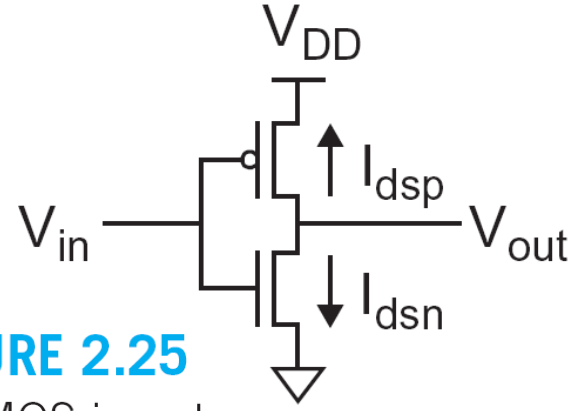

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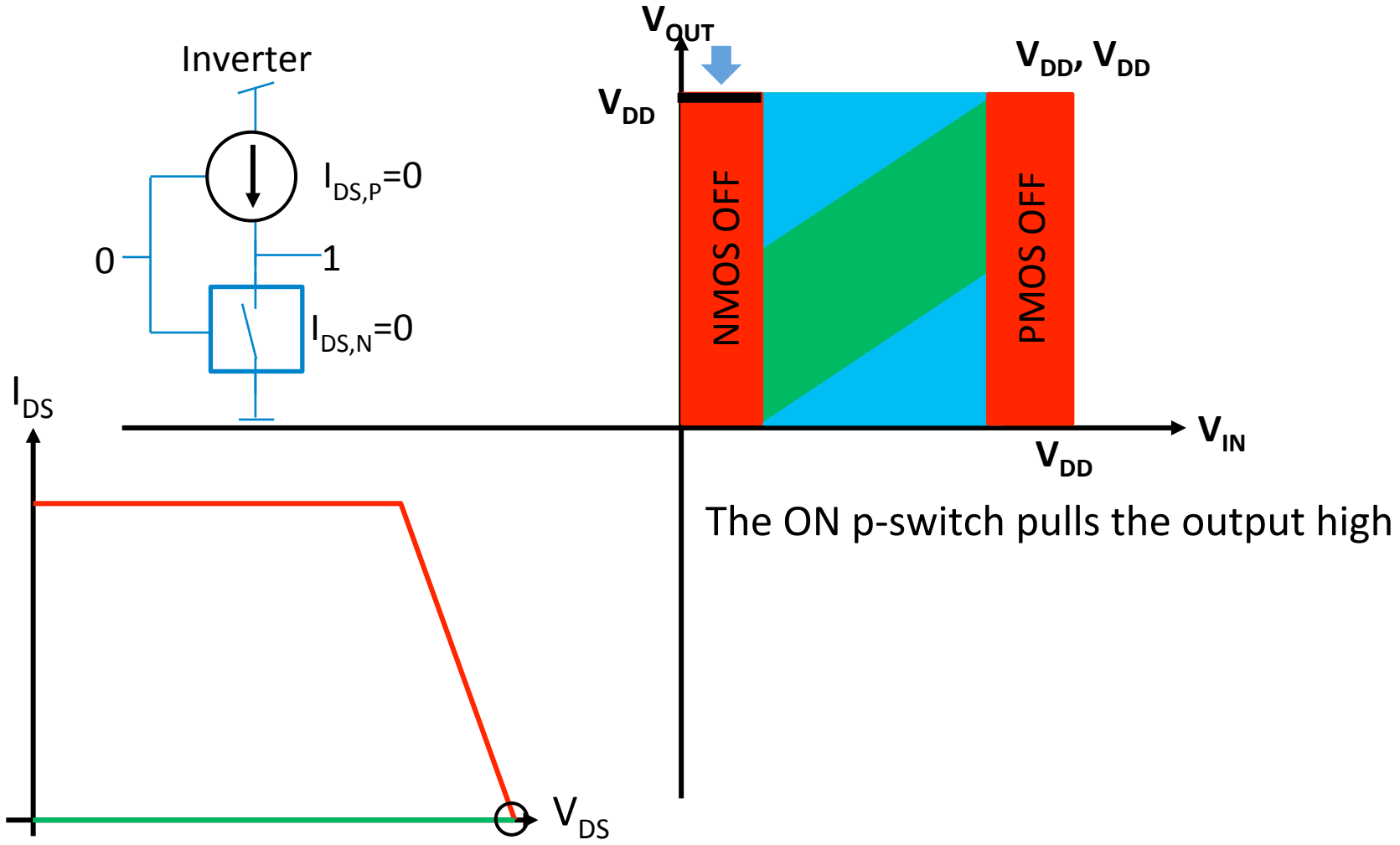
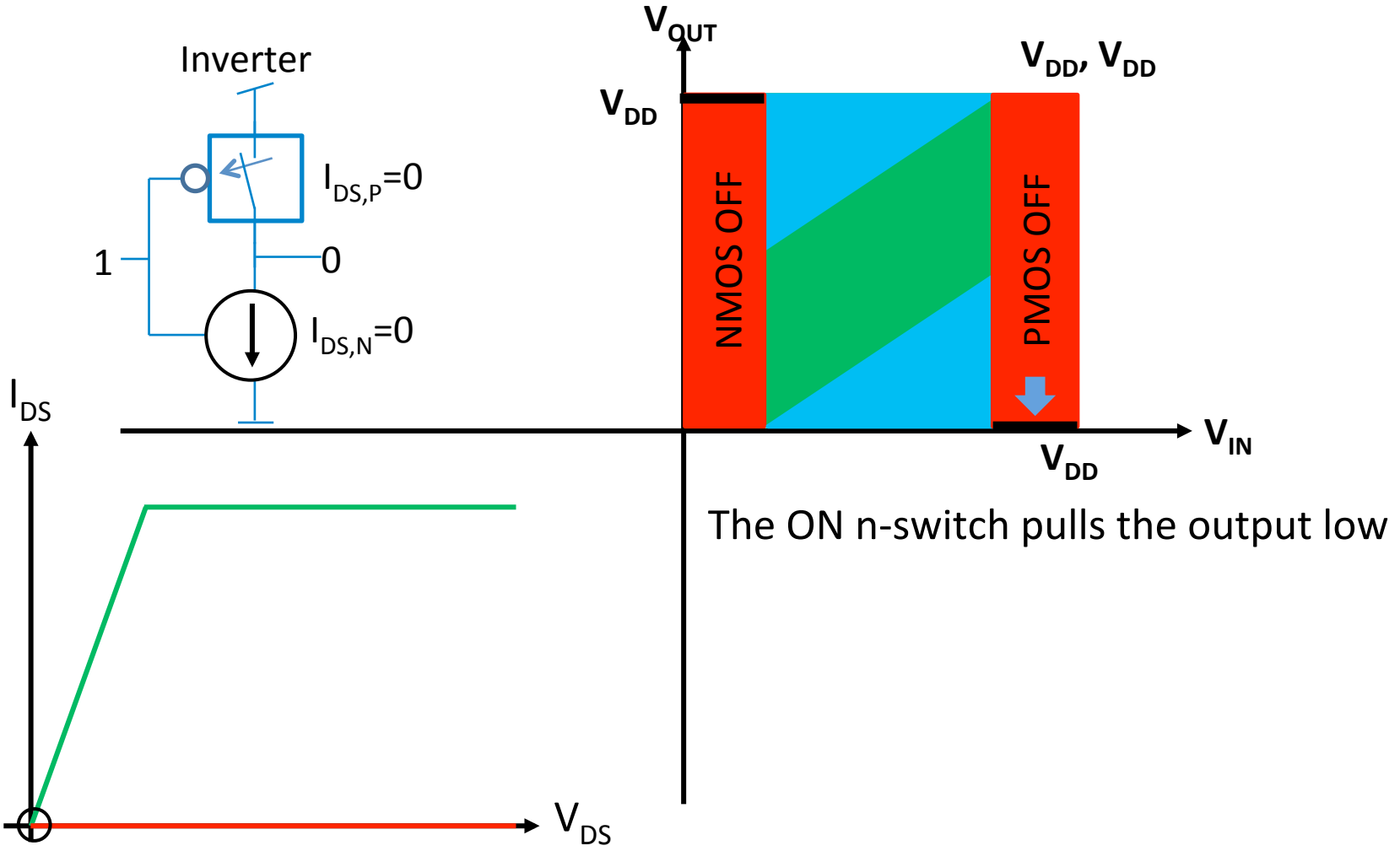
Voltage Transfer Characteristic - VTC



The ON p-switch pulls the output high

Voltage Transfer Characteristic - VTC



The ON n-switch pulls the output low

An aside about MOSFET current equations

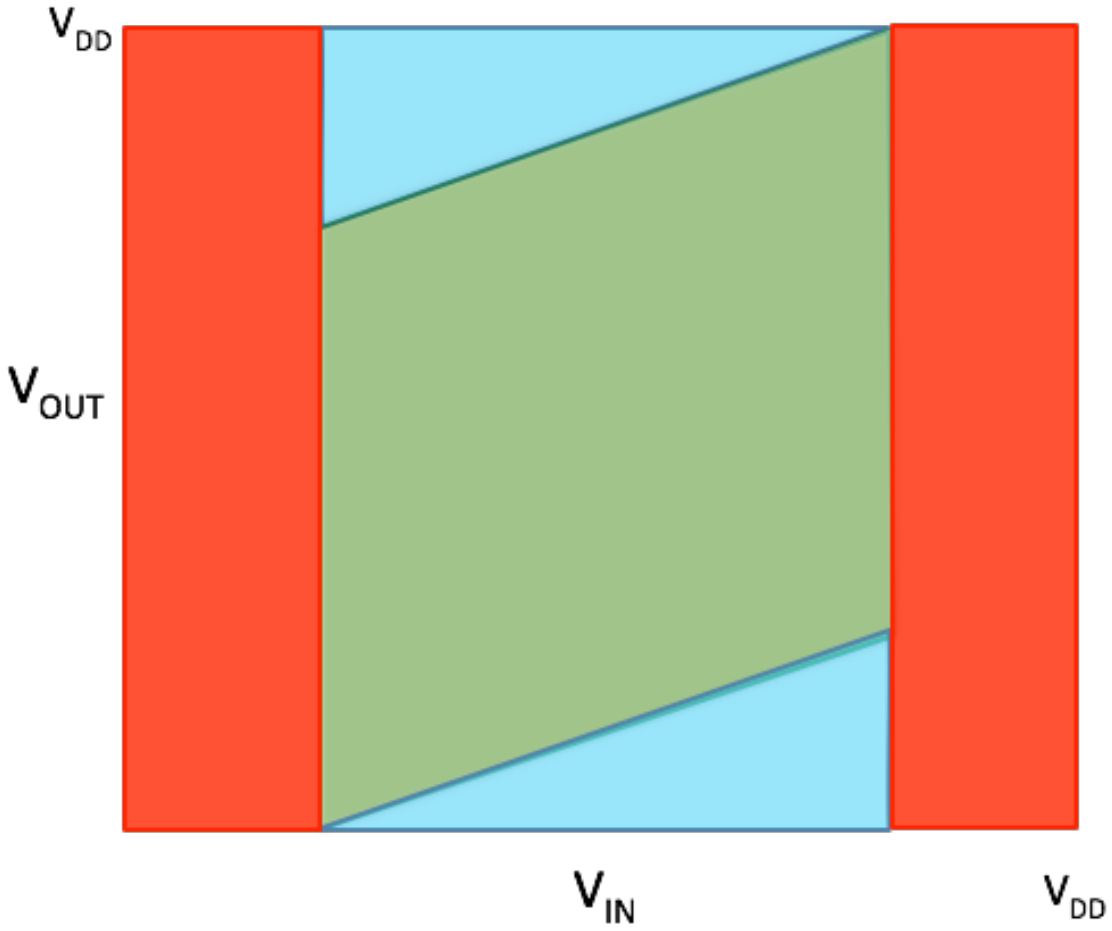
Shockley's continuous model:

$$I_{DS} = \begin{cases} 0 & V_{GS} < V_T \quad \text{Cutoff} \\ k_N(V_{GT} - \frac{V_{DS}}{2})V_{DS} & V_{DS} < V_{GT} \quad \text{Linear} \\ \frac{k_N}{2}V_{GT}^2 & V_{DS} > V_{GT} \quad \text{Saturation} \end{cases}$$

Our piecewise linear model:

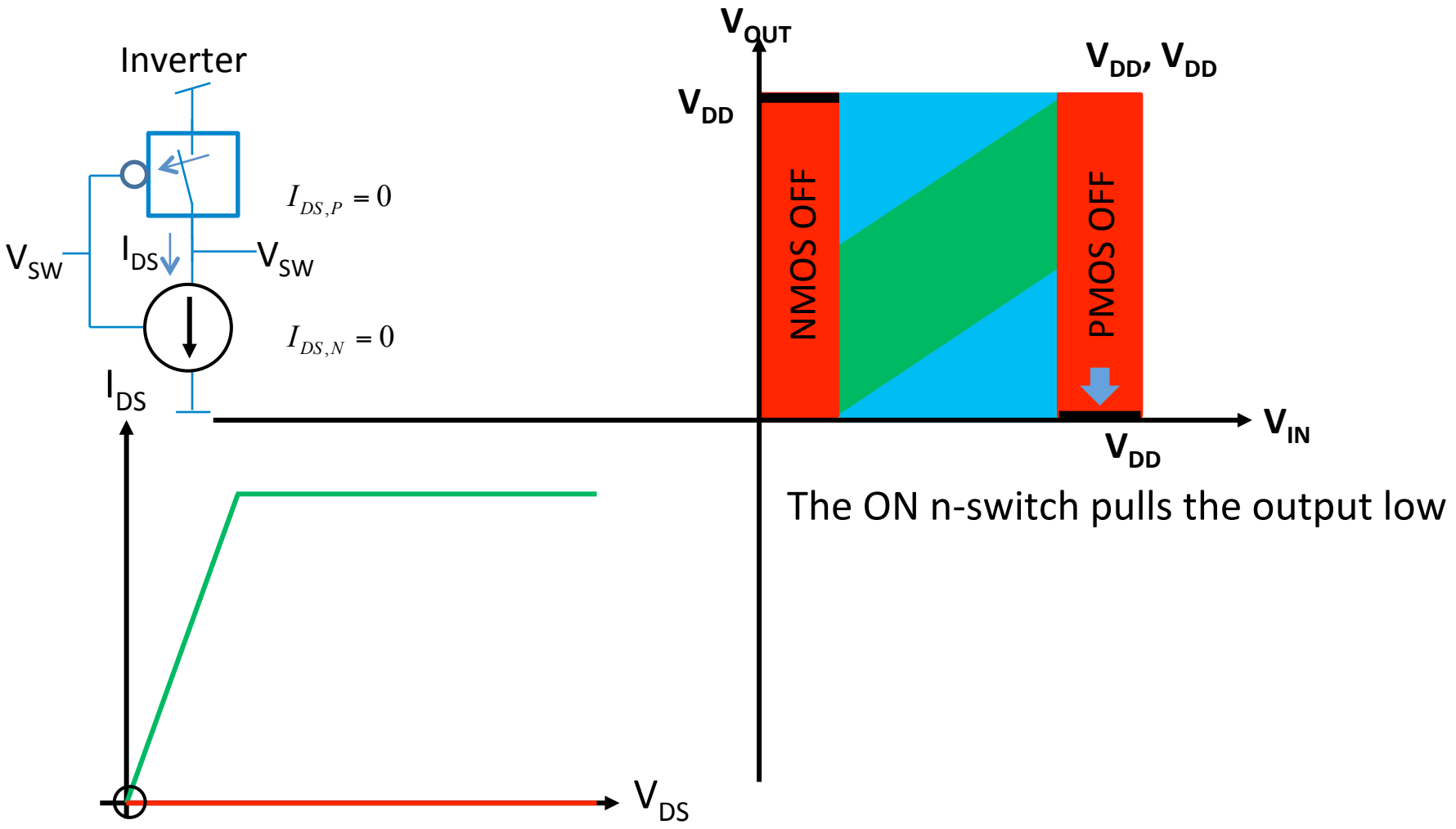
$$I_{DS} = \begin{cases} 0 & V_{GS} < V_T \quad \text{Cutoff} \\ k_N V_{GT} V_{DS} & V_{DS} < V_{GT}/2 \quad \text{Linear} \\ \frac{k_N}{2}V_{GT}^2 & V_{DS} > V_{GT}/2 \quad \text{Saturation} \end{cases}$$

So with piecewise linear MOS model the inverter diagram is this:



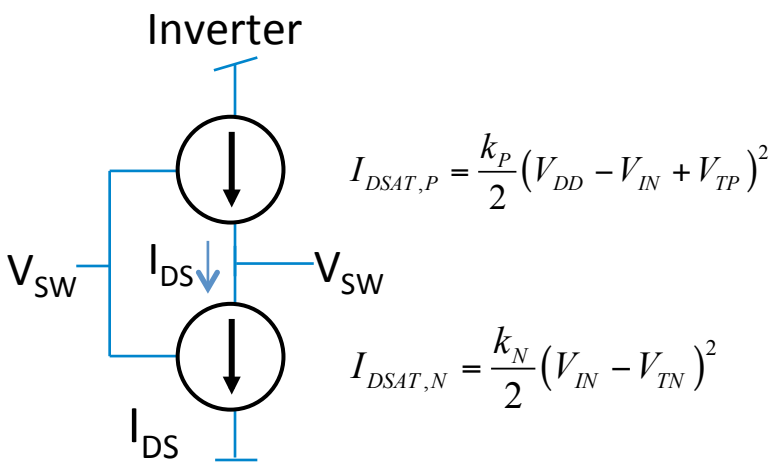
Notice
different slopes
between green
and blue regions!
Transition voltage is
VGT/2 rather than VGT

Voltage Transfer Characteristic - VTC



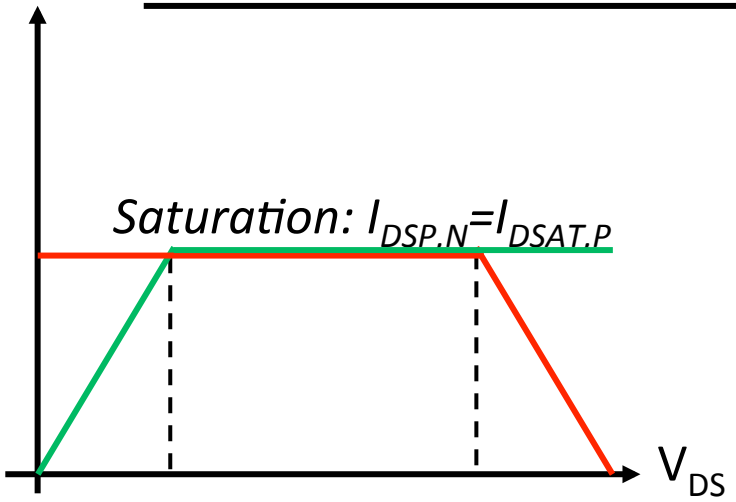
The ON n-switch pulls the output low

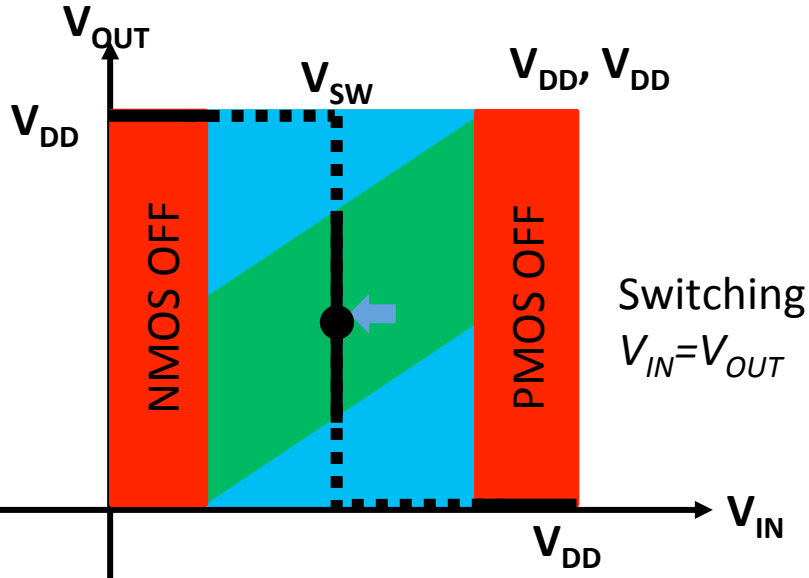
Voltage Transfer Characteristic - VTC



$$I_{DSAT,P} = \frac{k_P}{2}\left(V_{DD} - V_{IN} + V_{TP}\right)^2$$

$$I_{DSAT,N} = \frac{k_N}{2}\left(V_{IN} - V_{TN}\right)^2$$





Switching means:
$V_{IN}=V_{OUT}$

Switching occurs in the **green region** where both MOSFETs are saturated...

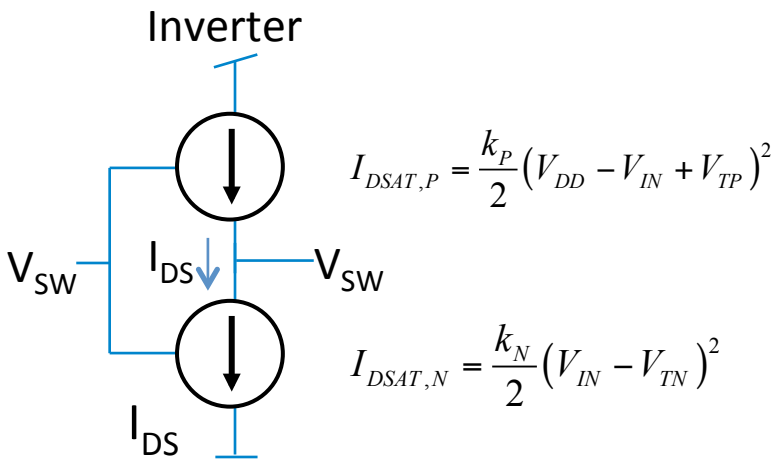
...and saturation currents are equal:

$$\frac{k_N}{2}\left(V_{IN} - V_{TN}\right)^2 = \frac{k_P}{2}\left(V_{DD} - V_{IN} + V_{TP}\right)^2$$

Solving for V_{IN} using $x=k_N/k_P$ yields

$$V_{sw} = \frac{V_{DD} + V_{TP} + \sqrt{x}V_{TN}}{1+\sqrt{x}}$$

Voltage Transfer Characteristic - VTC



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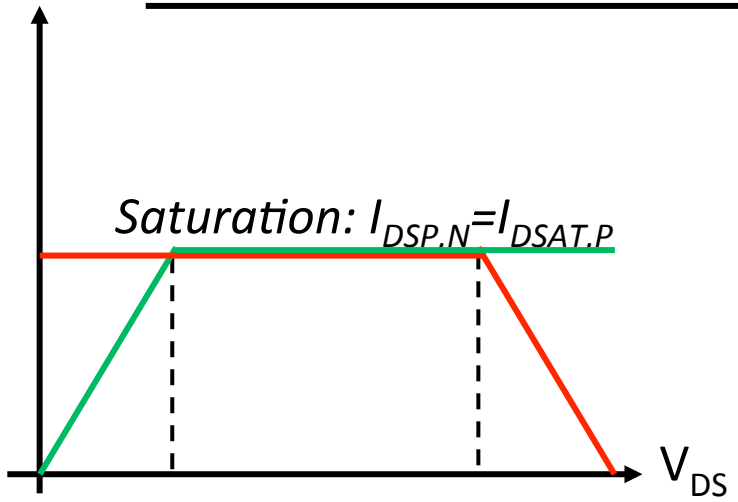
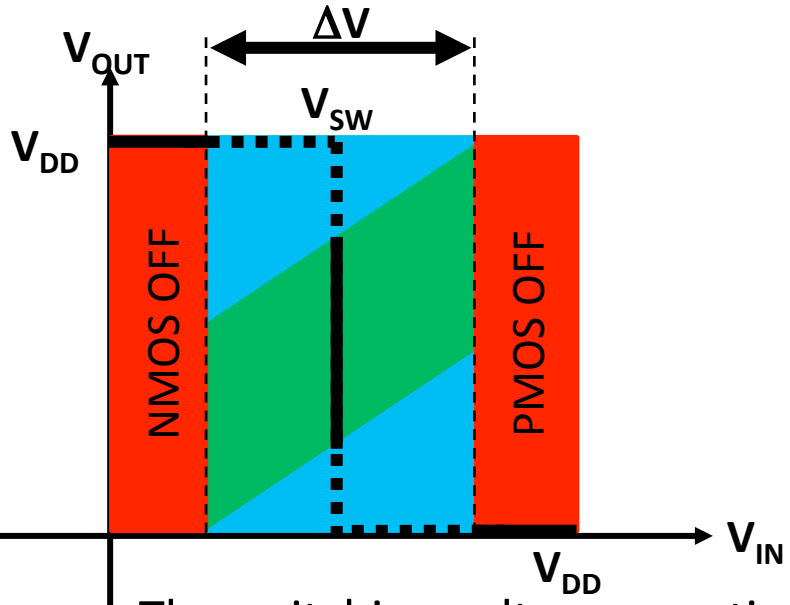




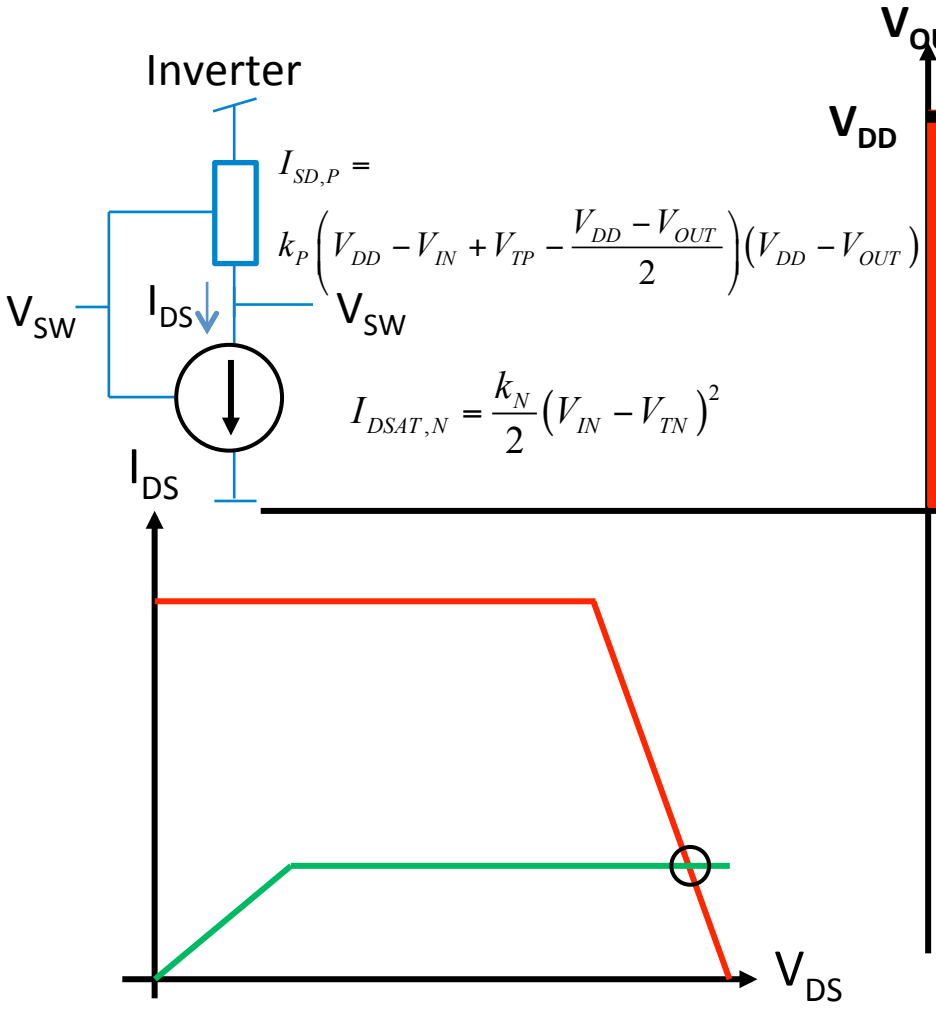
The switching voltage equation

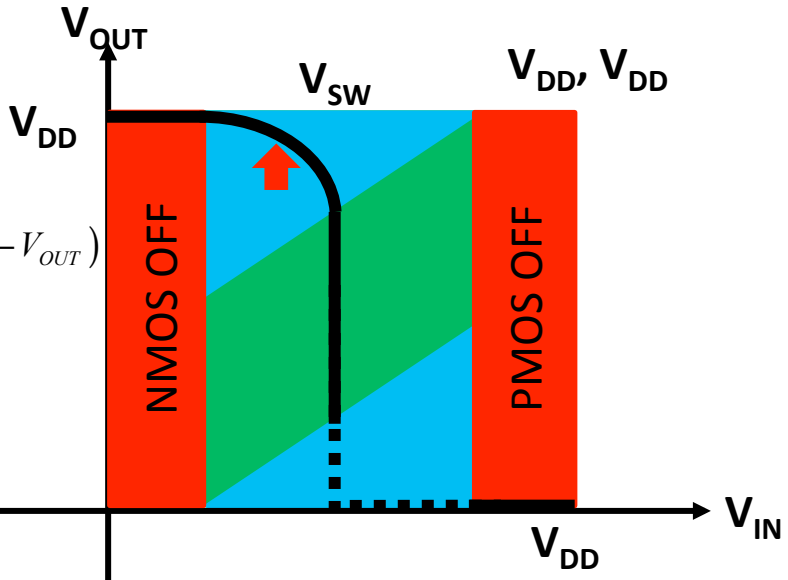
$$V_{sw} = \frac{V_{DD} + V_{TP} + \sqrt{x}V_{TN}}{1 + \sqrt{x}}$$

can be rewritten on a form easier to grasp if we introduce $\Delta V = V_{DD} + V_{TP} - V_{TN}$

$$V_{sw} = V_{TN} + \frac{\Delta V}{1 + \sqrt{x}}$$

Voltage Transfer Characteristic - VTC



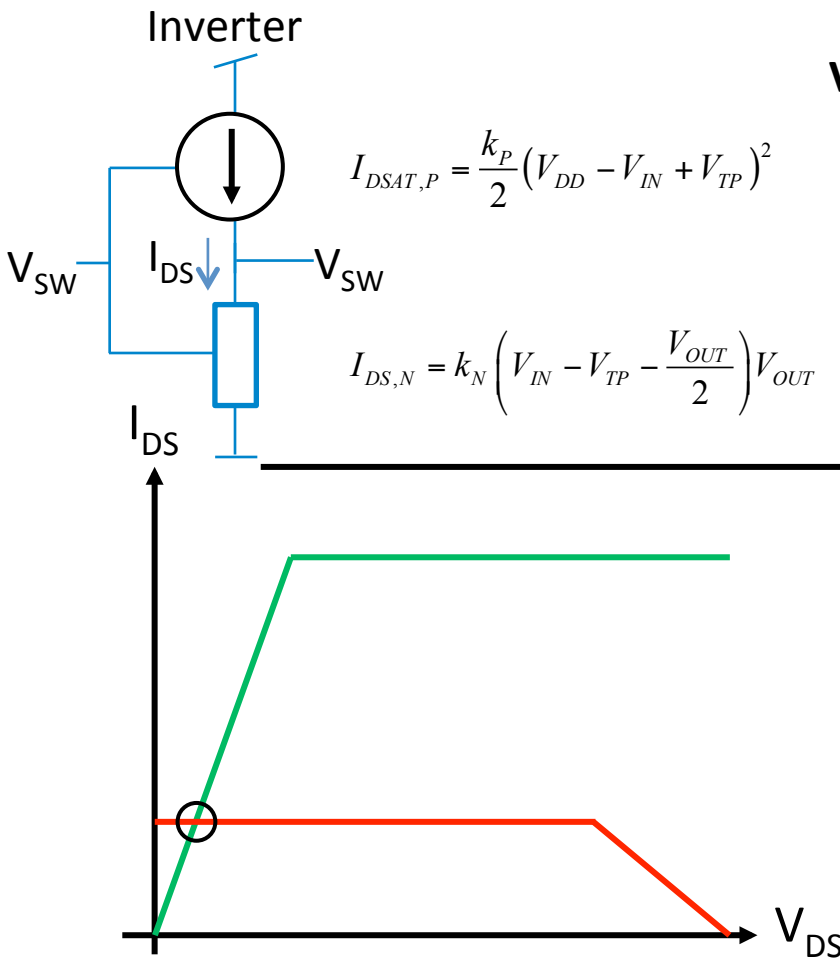


Equal currents in top blue region where p-MOSFET is in linear region

$$\frac{k_N}{2}(V_{IN}-V_{TN})^2 = k_P\left(V_{DD}-V_{IN}+V_{TP}-\frac{V_{DD}-V_{OUT}}{2}\right)(V_{DD}-V_{OUT})$$

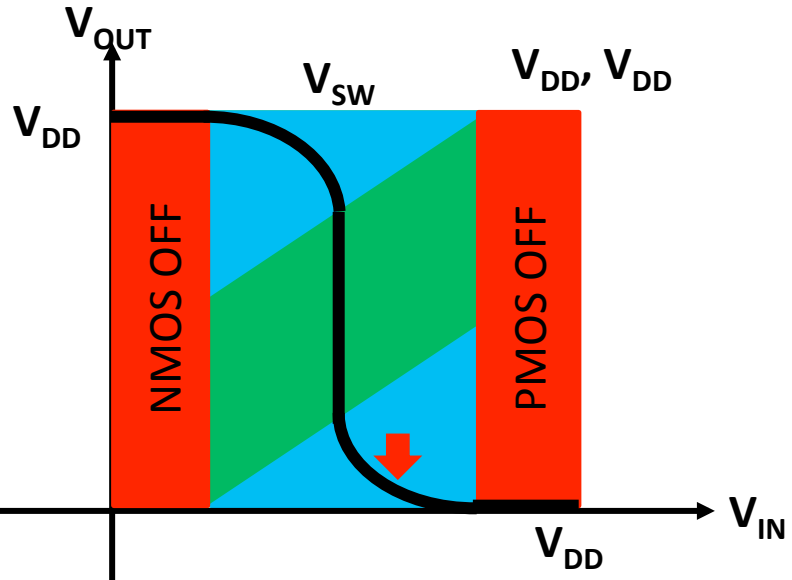
yields V_{OUT} *vs.* V_{IN}*!*

Voltage Transfer Characteristic - VTC



$$I_{DSAT,P} = \frac{k_P}{2}\left(V_{DD} - V_{IN} + V_{TP}\right)^2$$

$$I_{DS,N} = k_N\left(V_{IN} - V_{TP} - \frac{V_{OUT}}{2}\right)V_{OUT}$$



Equal currents in bottom blue region where n-MOSFET is linear region

$$k_N\left(V_{IN} - V_{TN}\right)V_{OUT} = \frac{k_P}{2}\left(V_{DD} - V_{IN} + V_{TP}\right)^2$$

yields V_{OUT} *vs.* V_{IN}*!*

The voltage characteristic (VTC)

For $x=k_N/k_P=1$ we have

$$V_{sw} = V_{TN} + \frac{\Delta V}{1+\sqrt{x}} = V_{TN} + \frac{\Delta V}{2}$$

What if we make n-channel MOSFET wider, i.e. for $x>1$?

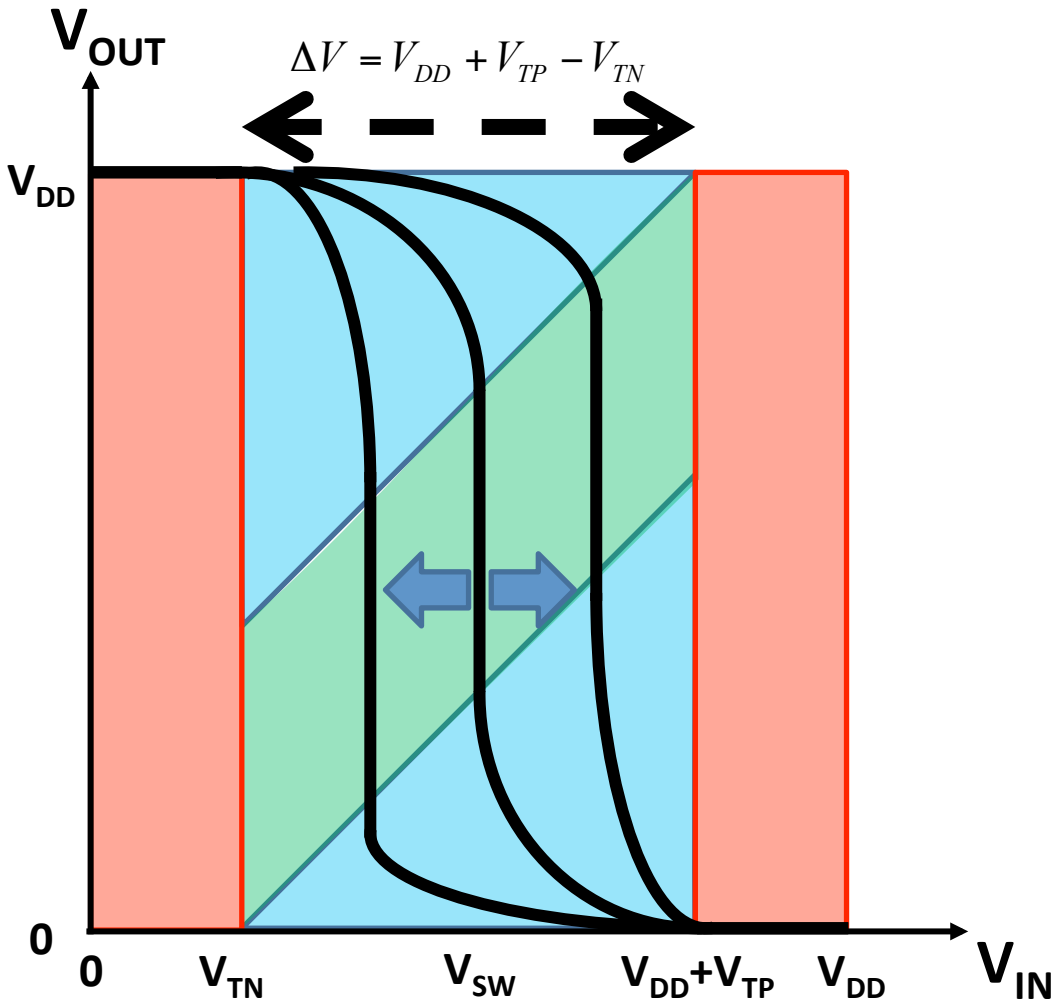
What happens to VTC? Will switching voltage V_{SW} increase or decrease?

Assume $x=4$ and we have

$$V_{sw} = V_{TN} + \frac{1}{3}\Delta V < V_{TN} + \frac{\Delta V}{2}$$

Assume $x=1/4$ and we have

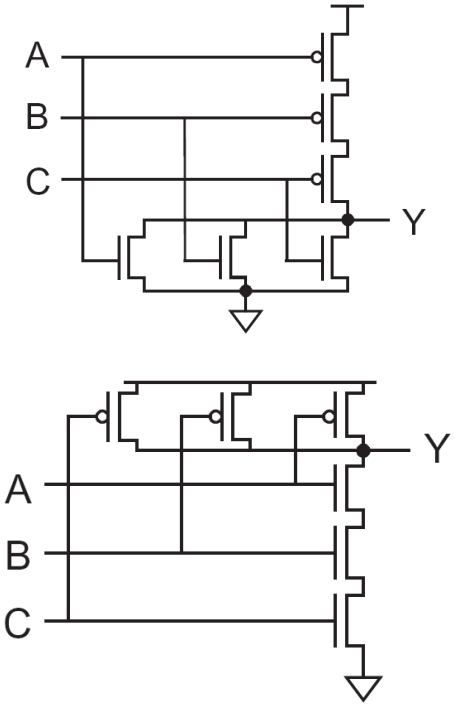
$$V_{sw} = V_{TN} + \frac{2}{3}\Delta V > V_{TN} + \frac{\Delta V}{2}$$

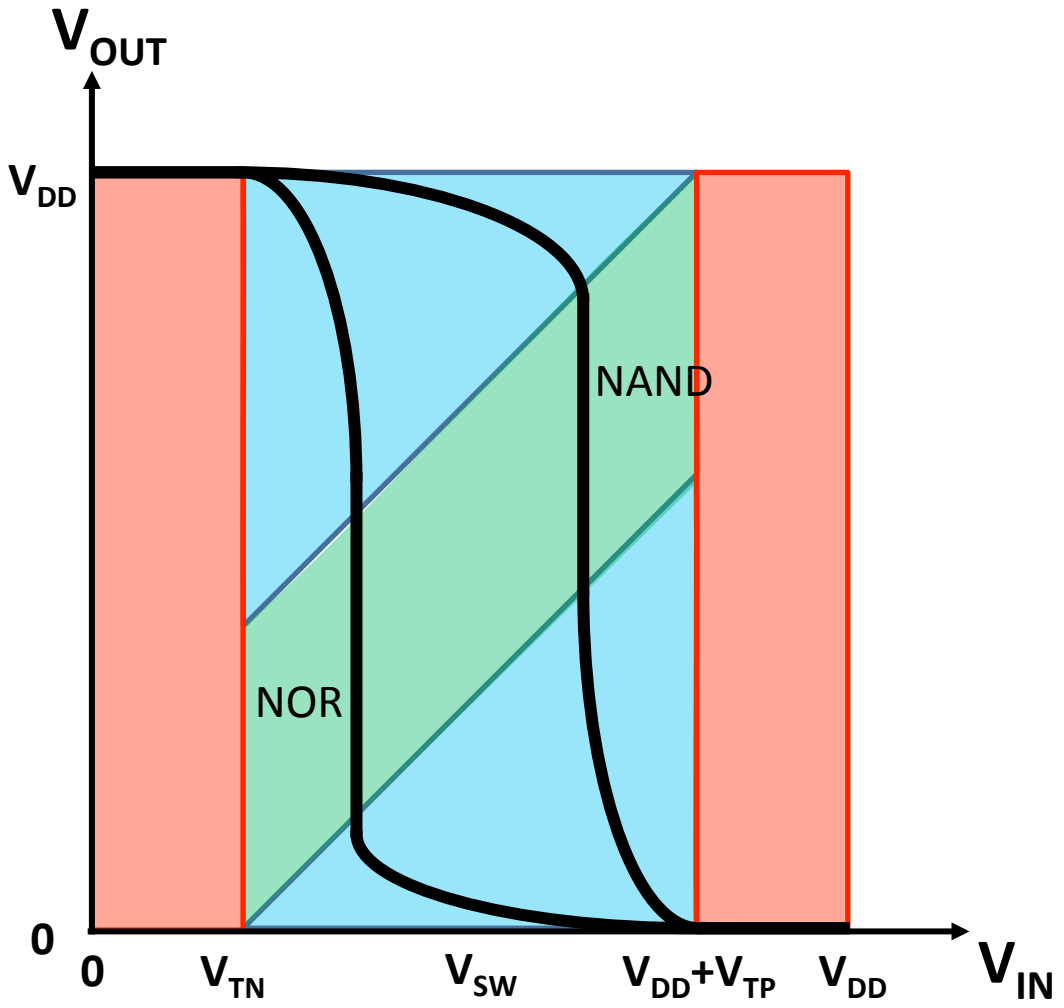


The voltage characteristic (VTC)

Which VTC is NAND and which VTC is NOR?

Assume all transistor same width



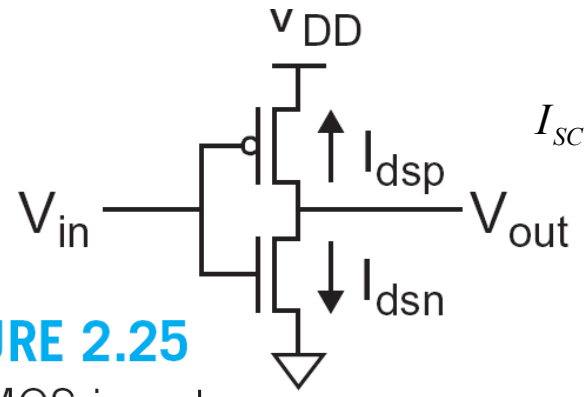


The voltage characteristic (VTC)

How about current flow?

No current flow in red regions!

”short-circuit” current I_{SC} flows in blue/green regions



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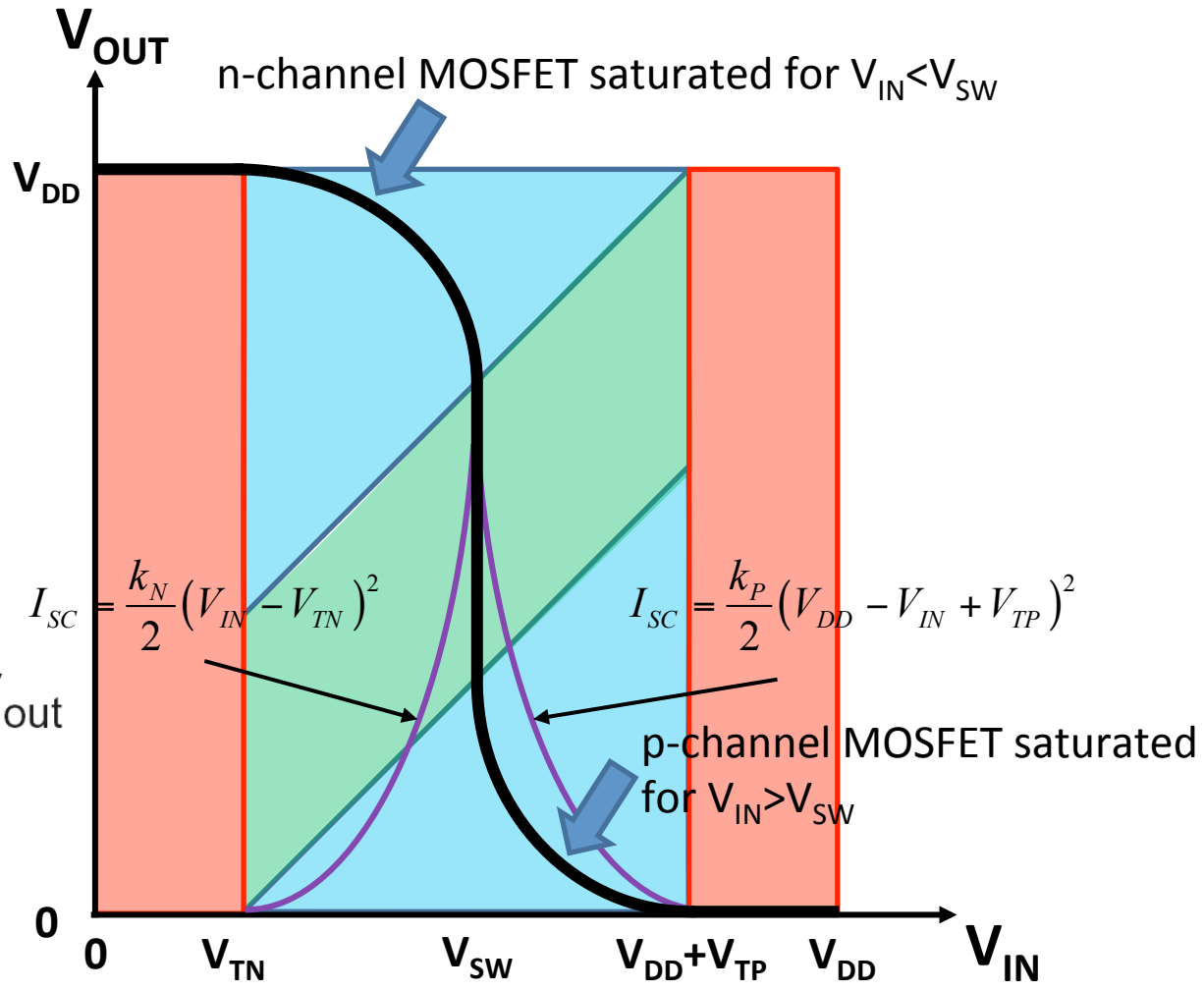
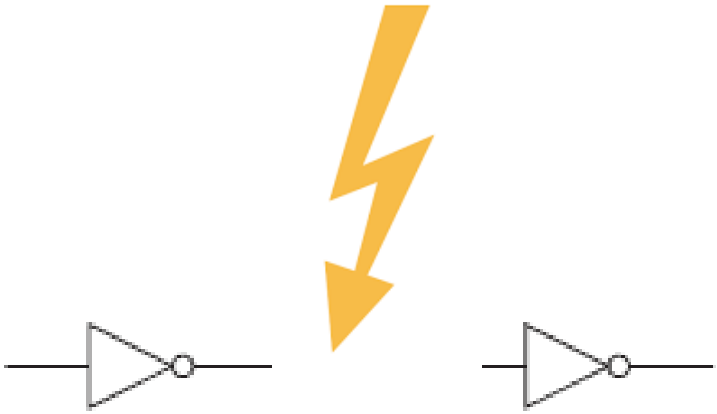


Noise margins

- What are they?
- Why are they important?



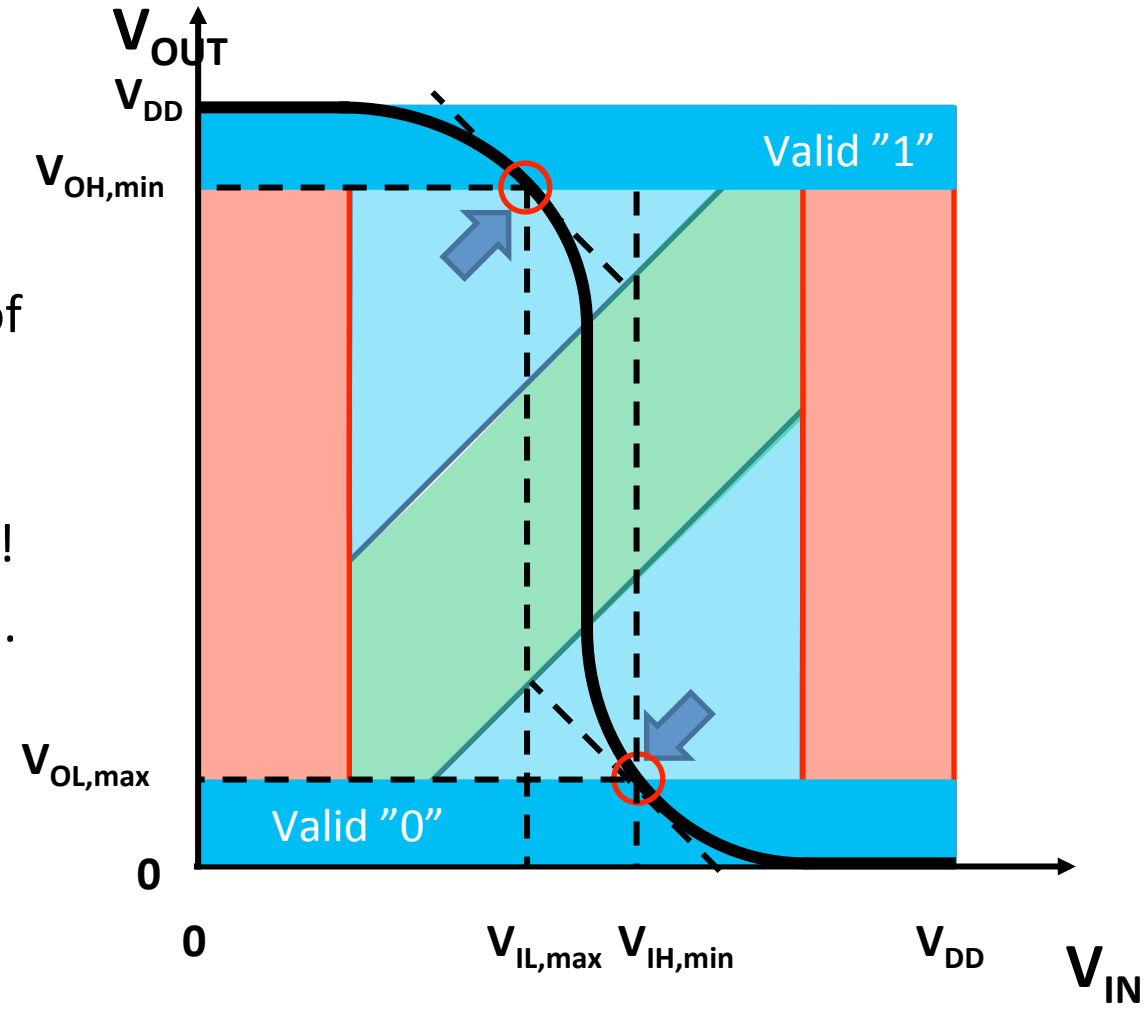
Answers the question: How much noise can the circuit tolerate?

Noise Margins - preliminairies

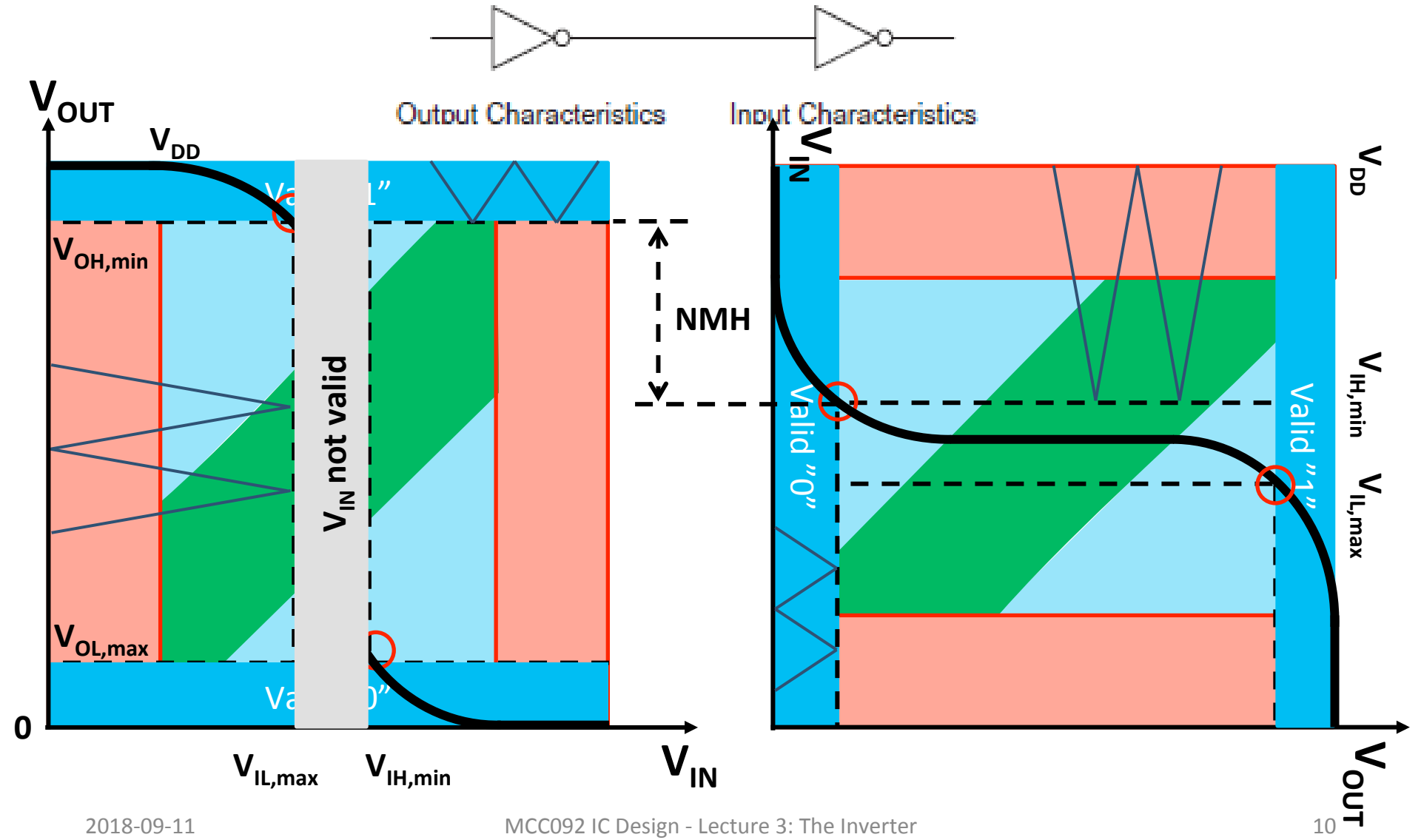
Let´s define valid input and output voltage regions from points where slope of VTC is -1;

That is where $A_V = -1$!

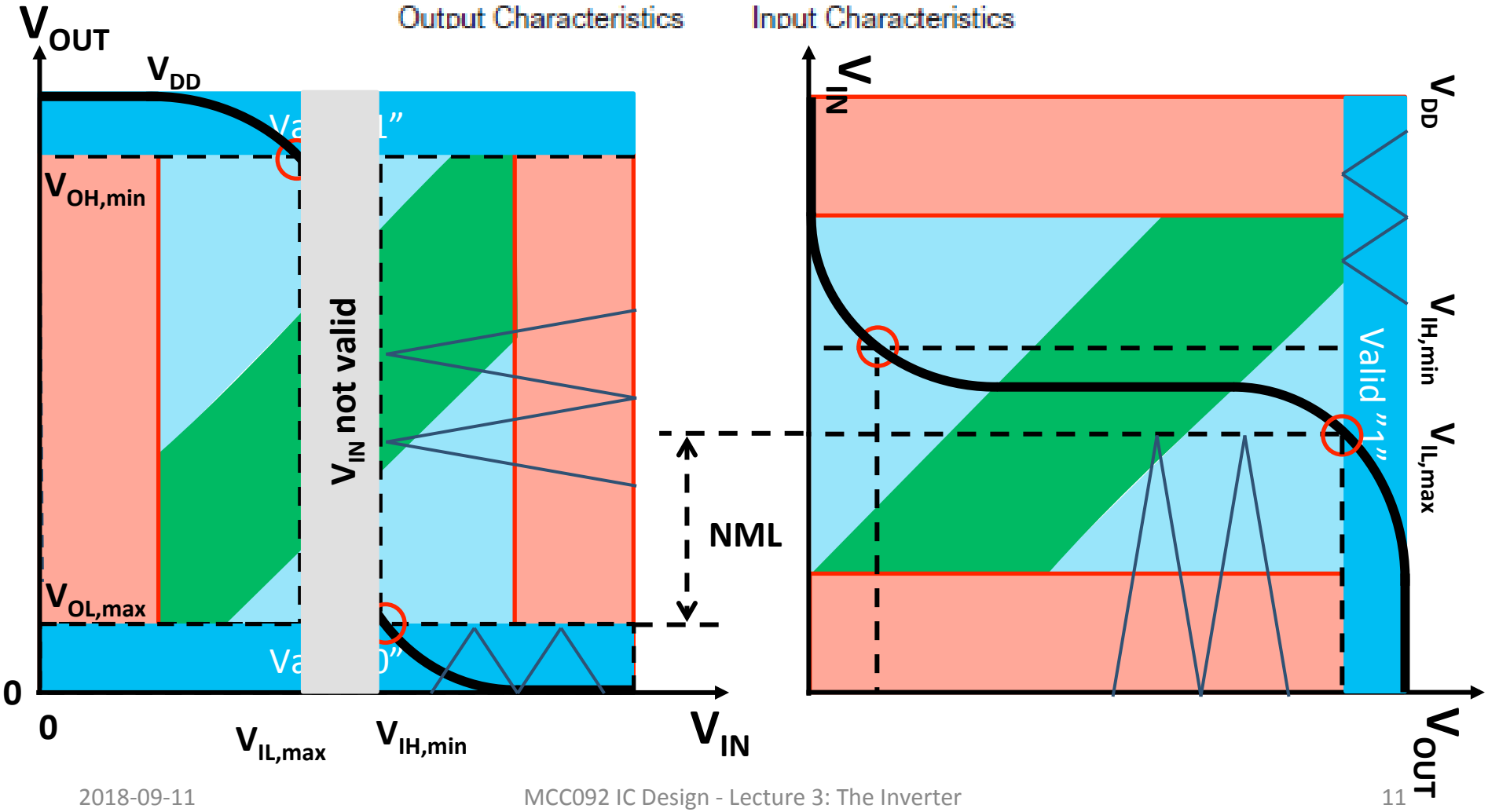
A_V is the voltage gain.



Noise margins - NMH



Noise Margins- NML



Regenerative effect

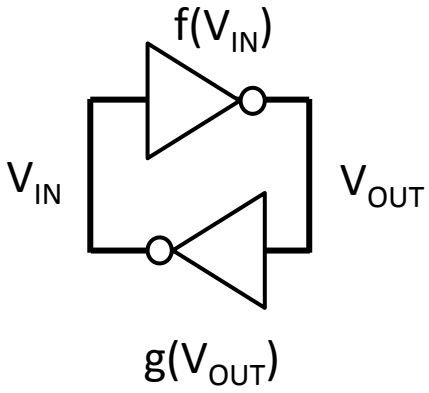
= How well the signal is regenerated from input to output

Consider a pair of cross-coupled inverters

$$V_{\mathrm{OUT}} = f(V_{\mathrm{IN}})$$
$$V_{\mathrm{IN}} = g(V_{\mathrm{OUT}})$$

that is

$$V_{\mathrm{IN}} = g(f(V_{\mathrm{IN}}))$$



We take the partial derivate of this function w.r.t V_{IN} (using the chain rule):

$$1 = \frac{\partial g(f(V_{\mathrm{IN}}))}{\partial f(V_{\mathrm{IN}})} \cdot \frac{\partial f(V_{\mathrm{IN}})}{\partial V_{\mathrm{IN}}} = \frac{\partial g(V_{\mathrm{OUT}})}{\partial V_{\mathrm{OUT}}} \cdot \frac{\partial f(V_{\mathrm{IN}})}{\partial V_{\mathrm{IN}}}$$

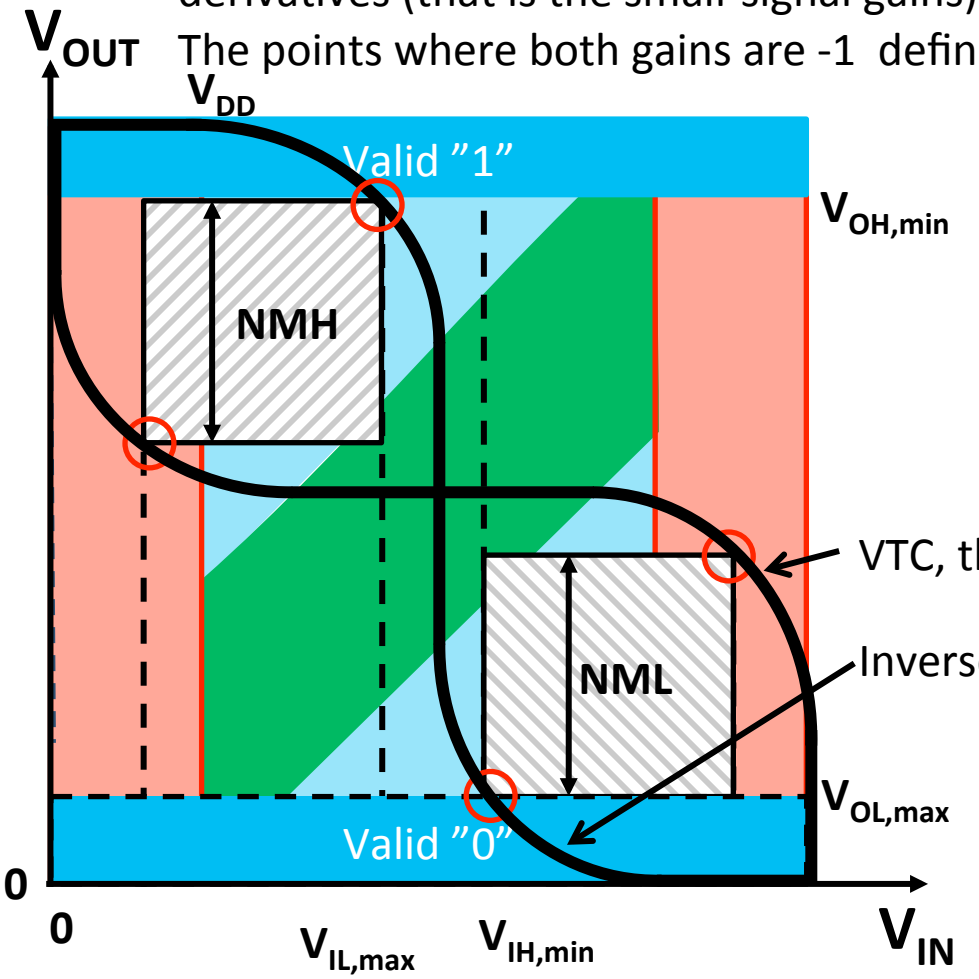
Slopes, that is, small-signal gains

So we see that the inverse of f (the VTC) is g in each pair of corresponding voltage points. Only if the VTC has a region of gain magnitude > 1 bordered by two regions of gain magnitude < 1 is the circuit regenerative. Then there are two stable operating points. The VTC and its inverse are illustrated in the butterfly diagram.

Butterfly Diagram

In each pair of corresponding voltage points (V_{IN}, V_{OUT}) the product of the derivatives (that is the small-signal gains) of the two curves is 1

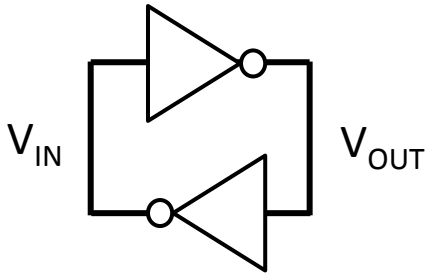
The points where both gains are -1 defines the voltages of interest for noise margins



VTC, that is f

Inverse of VTC, that is g

Memory cell characterization



See W&H section 12.2.1.3 for more info if you want to.

Noise Margins – skewed inverters

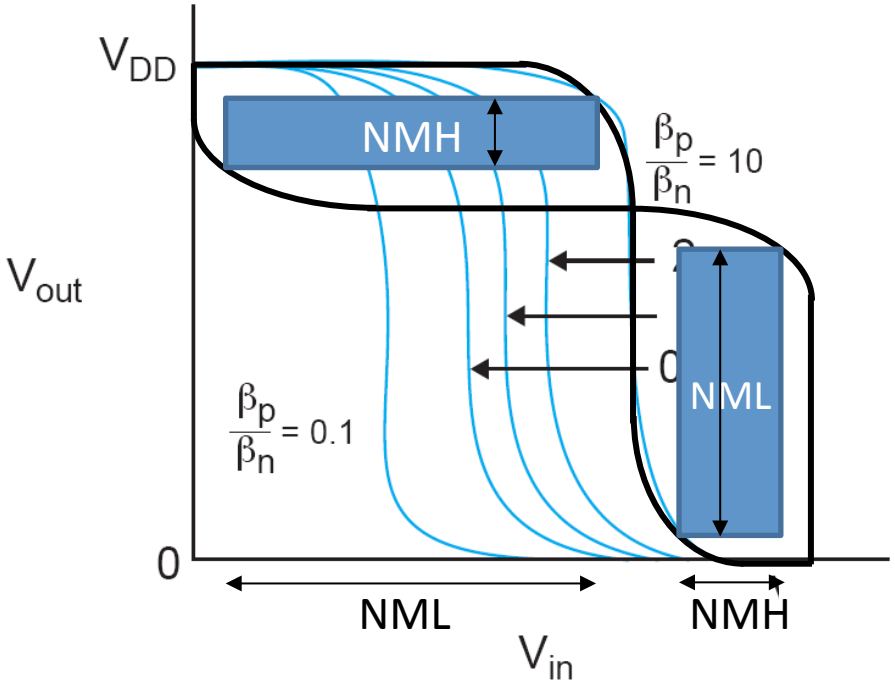


FIGURE 2.28 Transfer characteristics of skewed inverters

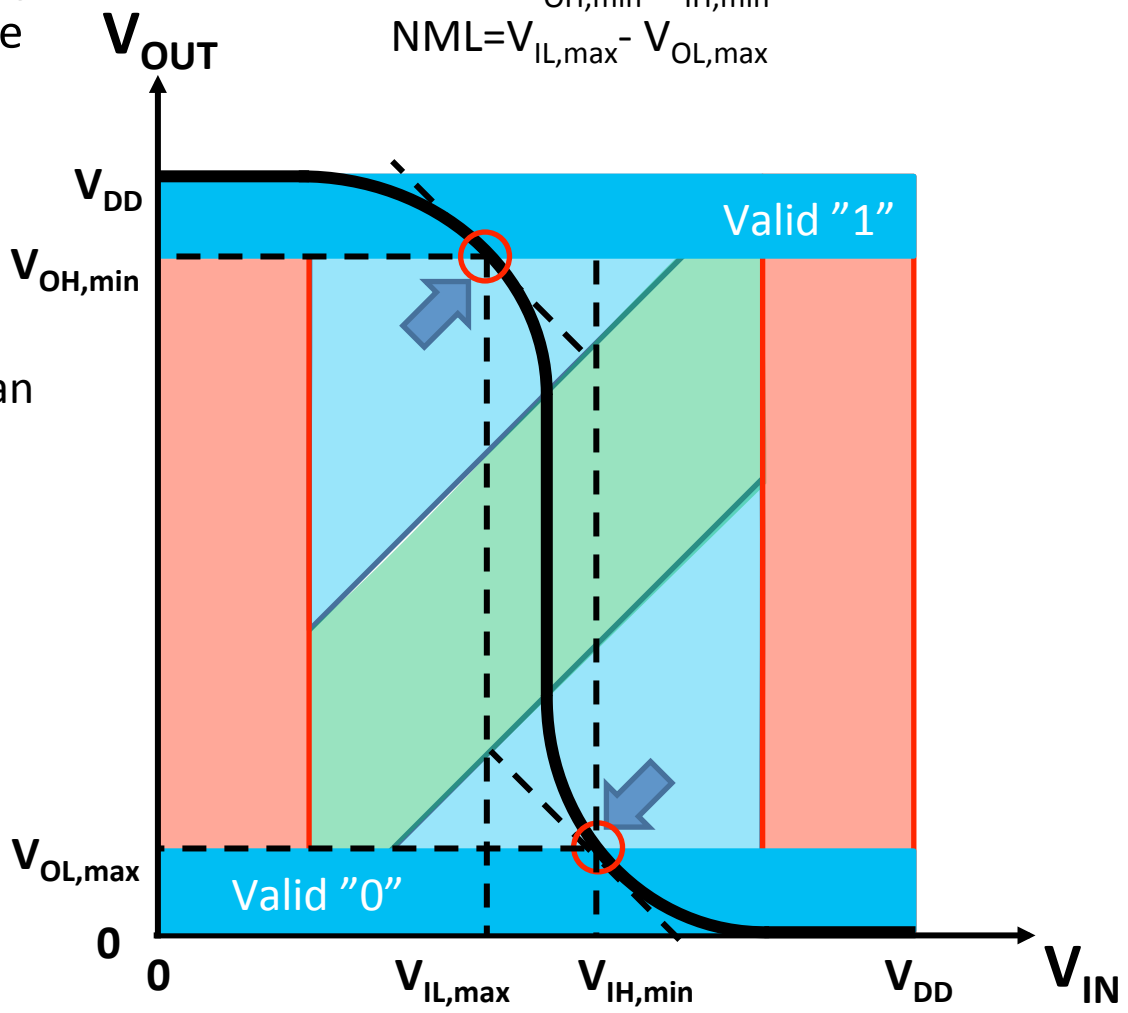
Noise Margins – an example

Let´s define valid regions from points where slope $A_V = -1$!

These points yields numbers for ($V_{OH,min}$, $V_{IL,max}$) and ($V_{OL,max}$, $V_{IH,min}$) so that NMH and NML can be calculated!

$NMH = V_{OH,min} - V_{IH,min}$

$NML = V_{IL,max} - V_{OL,max}$



Noise Margins – an example

Let´s define valid regions from points where slope $A_V = -1$!

These points yields numbers for ($V_{OH,min}$, $V_{IL,max}$) and ($V_{OL,max}$, $V_{IH,min}$) so that NMH and NML can be calculated!

For x=1, V_{TN}=0.28 V and V_{TP}=-0.28 V we have V_{SW}=0.28+0.64/2=0.60 V and ΔV=0.64 V

Formulas can be derived (for x=1):

$V_{OH,min}=V_{DD}-\Delta V/8=1.12$ V

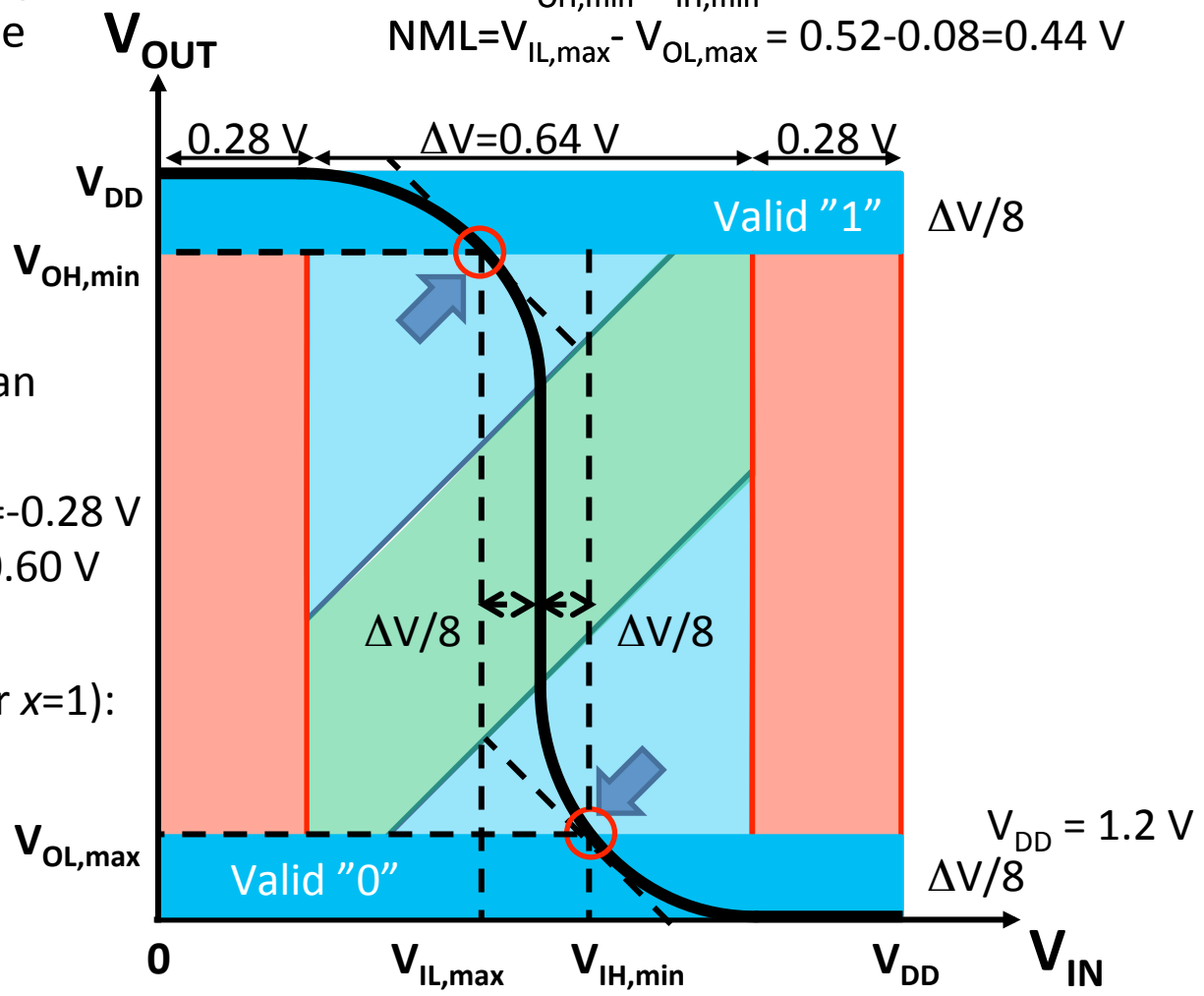
$V_{OL,max}=\Delta V/8=80$ mV

$V_{IL,max}=V_{SW}-\Delta V/8=0.52$ V

$V_{IH,min}=V_{SW}+\Delta V/8=0.68$ V

$NMH=V_{OH,min}-V_{IH,min}$ 1.12-0.68=0.44 V

$NML=V_{IL,max}-V_{OL,max}$ = 0.52-0.08=0.44 V



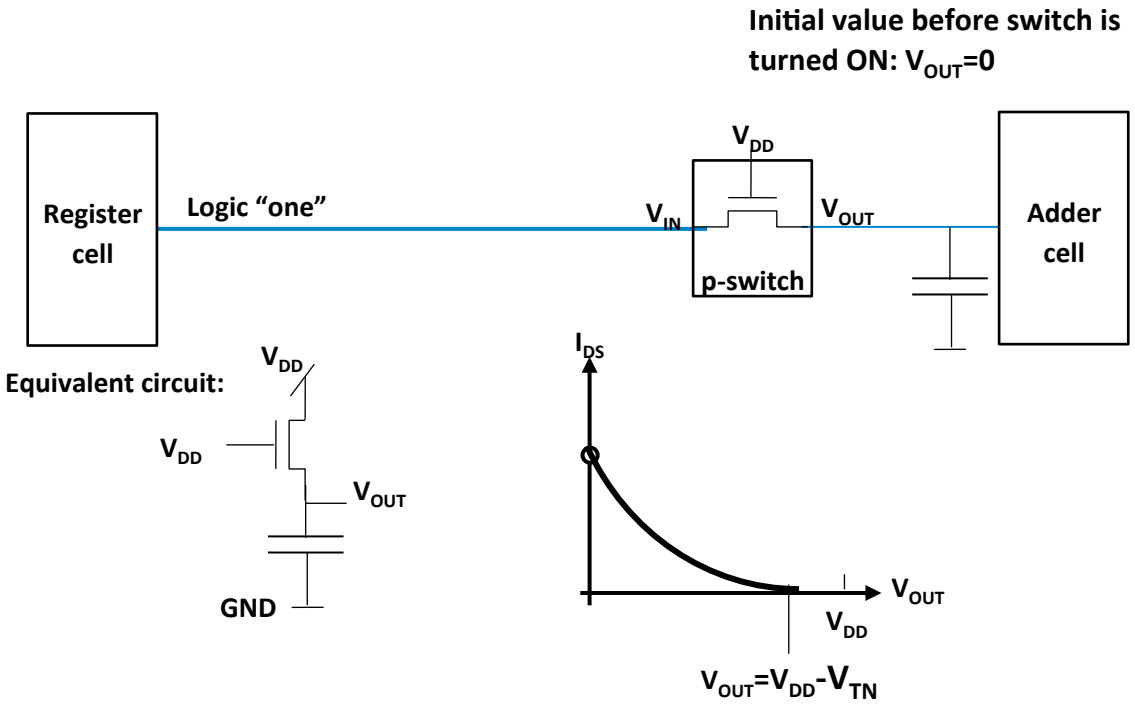
What about lab 1

- Calculate VSW and find from simulation in lab
- Calculate noise margins and find from simulation

Summary

- CMOS inverter – schematic
- Voltage transfer characteristics (VTC)
  - Regions of operation
  - How to calculate switching voltage V_{SW}
  - V_{SW} dependence on k_N/k_P (that is, transistor widths)
  - Understand switching current (I_{SC}) flow
- Noise margins: NMH and NML
  - Why important?
  - Definition
  - Butterfly diagram

Why not n-switches in pull-up networks?



Why not p-switches in pull-down networks?