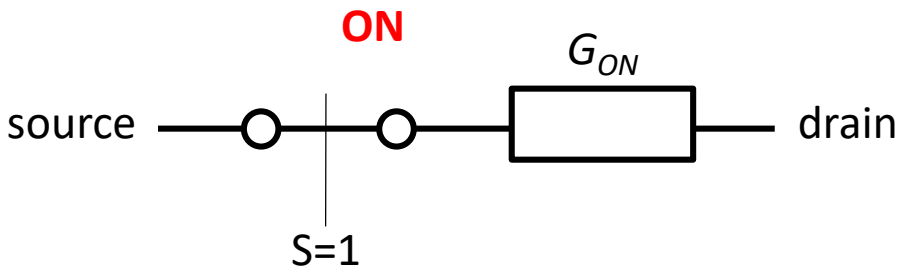
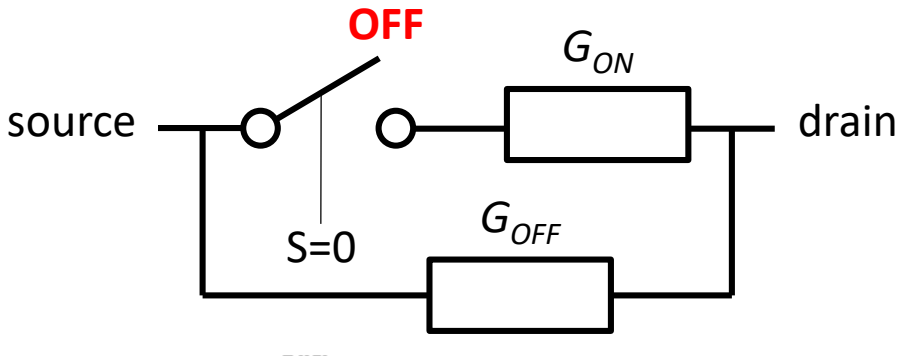
Lecture 2

The MOSFET

The MOSFET as a switch

In the digital world, the MOSFET is a switch that is either *ON* with conductance G_{ON}, or *OFF* with zero conductance, G_{OFF}=0





Lecture outline

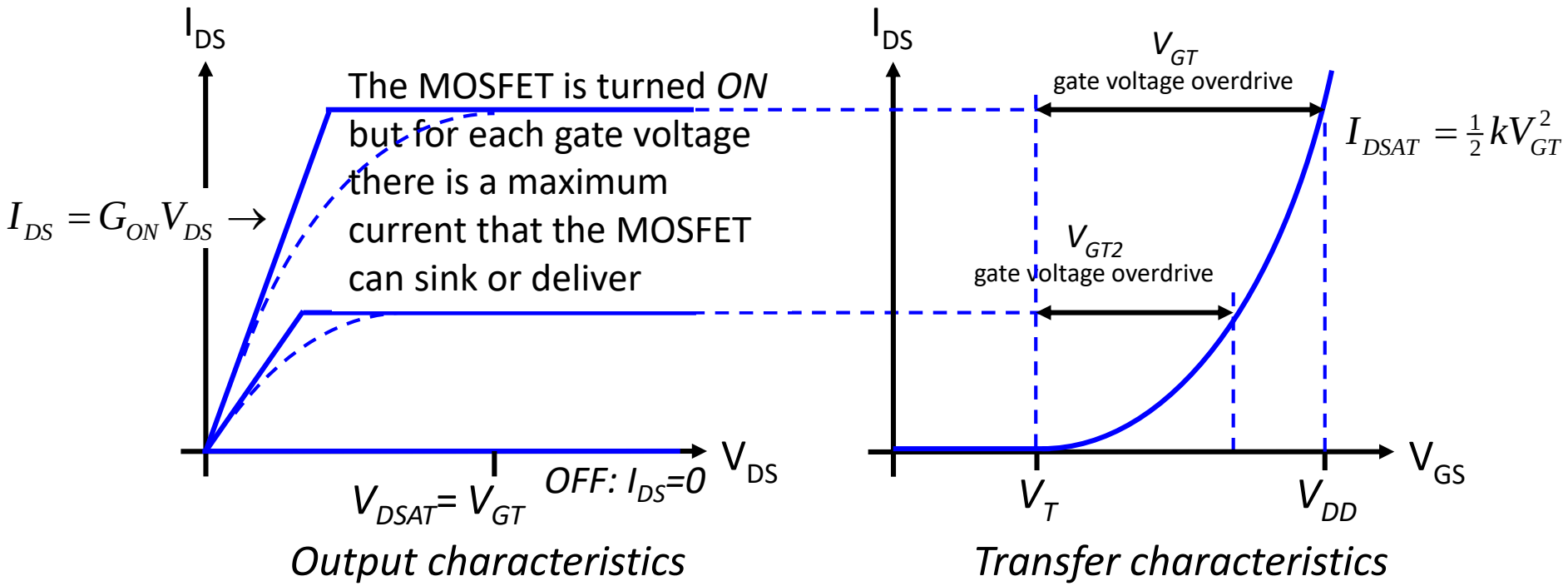
In this lecture we are going to have a closer look at some basic properties of the MOSFET beyond the switch model

- Why?
- Because, even if the switch model is good enough for designing logic CMOS gates based on their functionality . . .
- . . . it is not good enough for determining the performance in terms of switching speed and power dissipation

Lecture outline

- First we are going to learn how to calculate the voltage dependence of the ON resistance (or rather the ON conductance) of the MOSFET based on the principles of the field-effect.
- Then we are going to learn why, for any gate voltage, there is a maximum current that a MOSFET switch can deliver or sink.

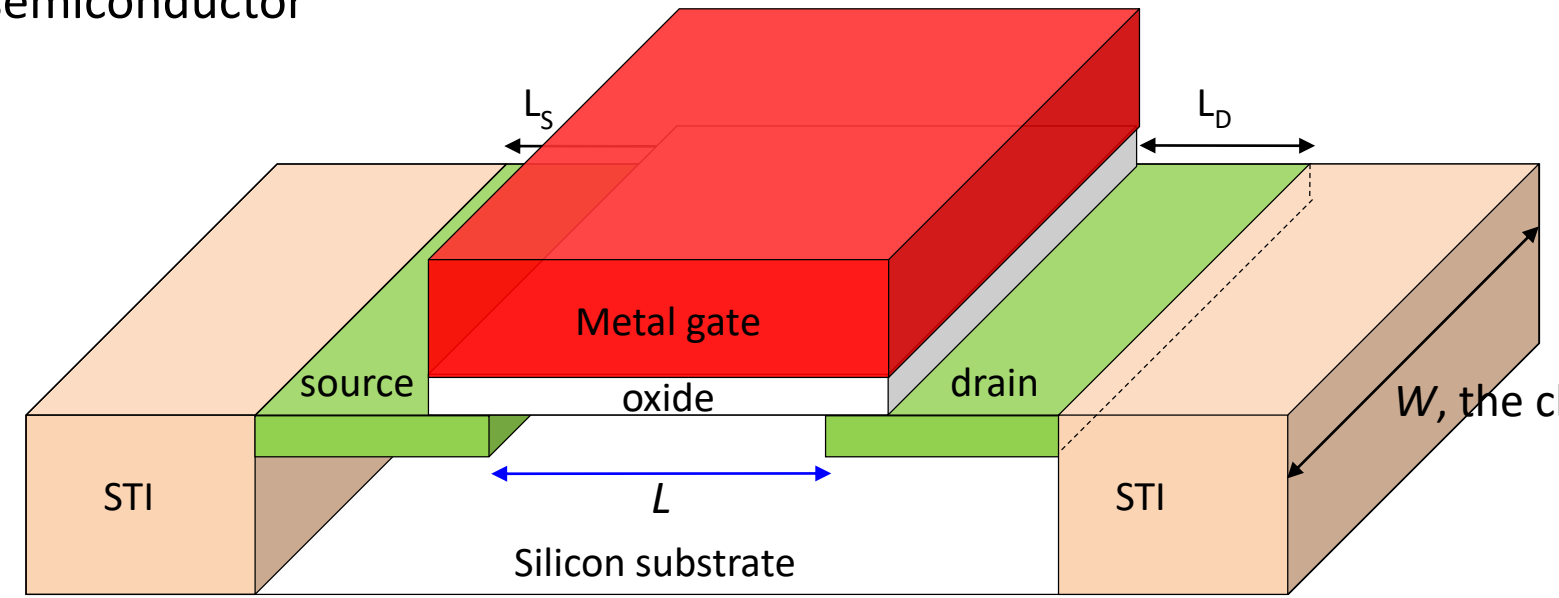
MOSFET output and transfer characteristics



The MOSFET is basically a "square-law" device!

The MOSFET structure

The metal-oxide-semiconductor structure

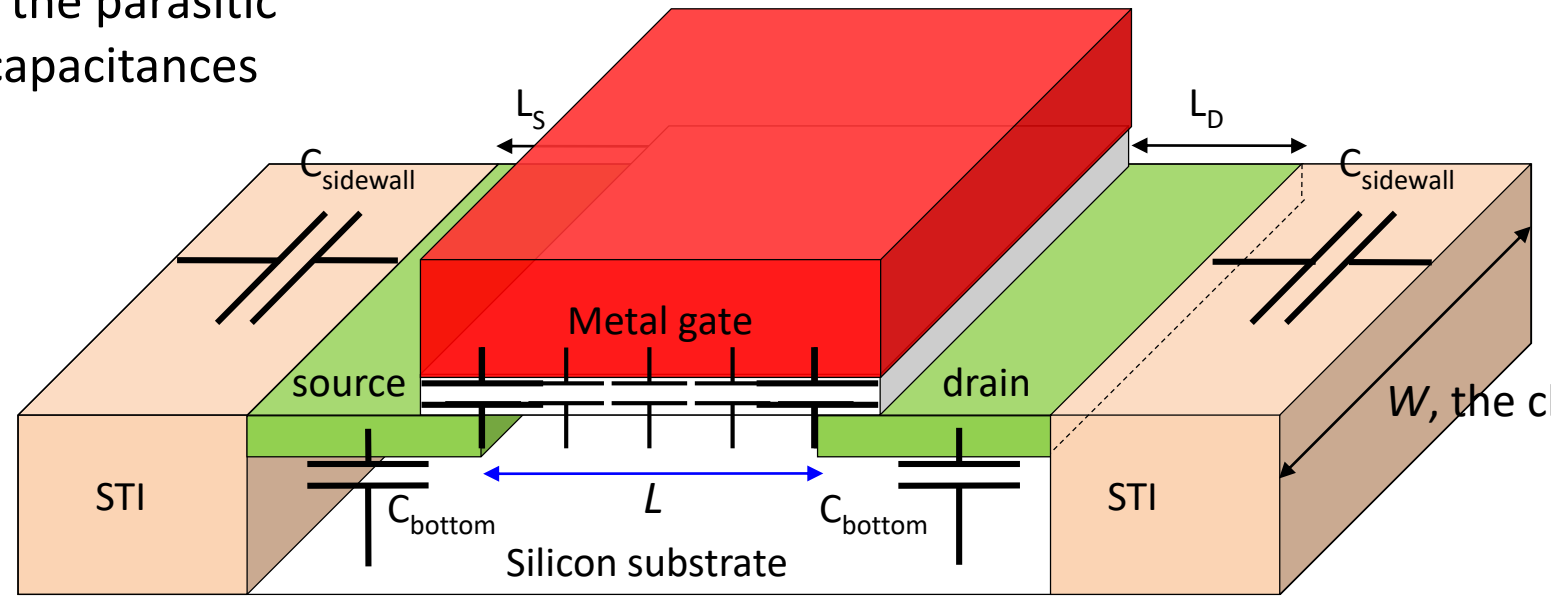


L is the channel length

The MOSFET capacitances

There is a distributed gate capacitance
that must be lumped to the available ckt nodes,
i.e. to source and drain

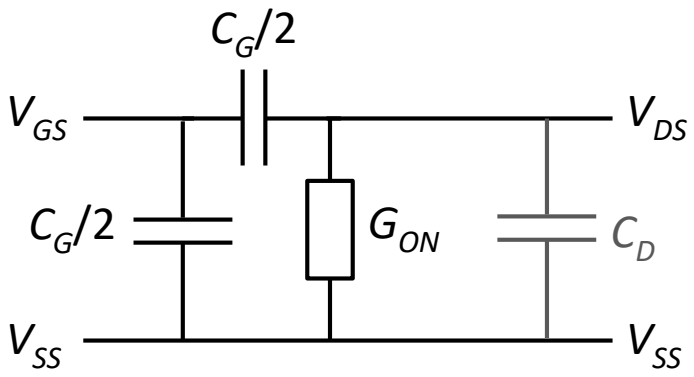
And then we have the parasitic
source and drain capacitances



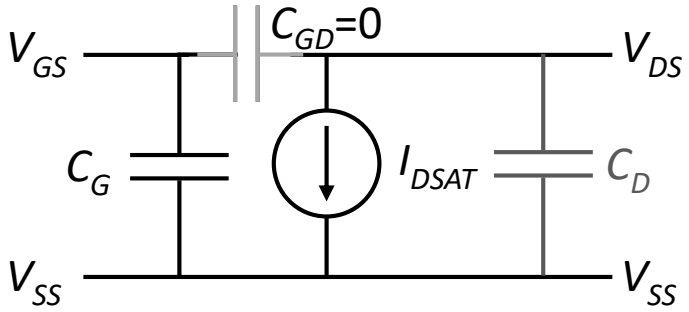
W, the channel width

L is the channel length

Equivalent electrical two-port circuit model

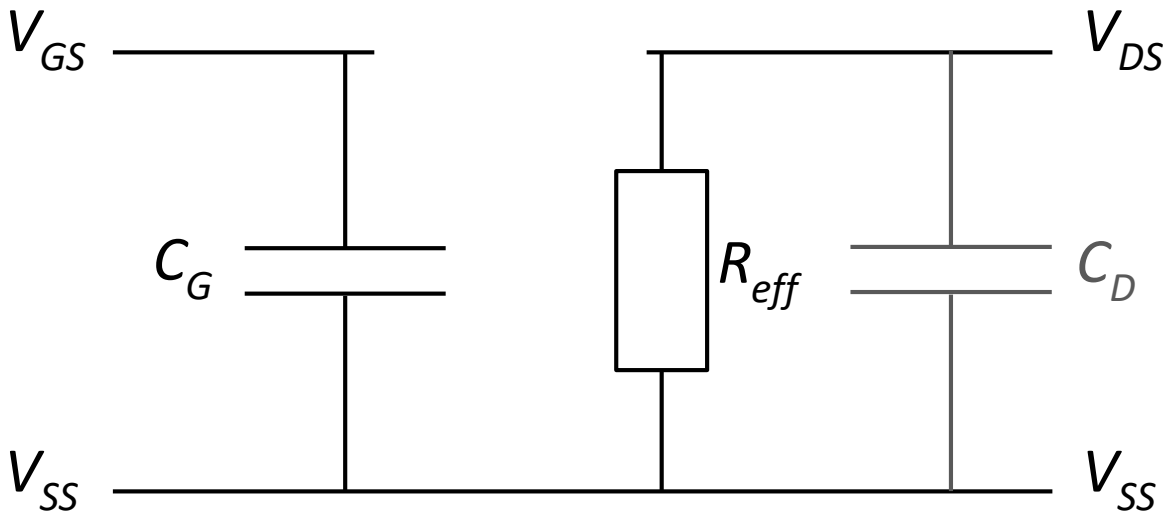


Model for linear device



Model for saturated device

The distributed gate to channel capacitance must be lumped to the available ckt nodes, i.e. to source and drain

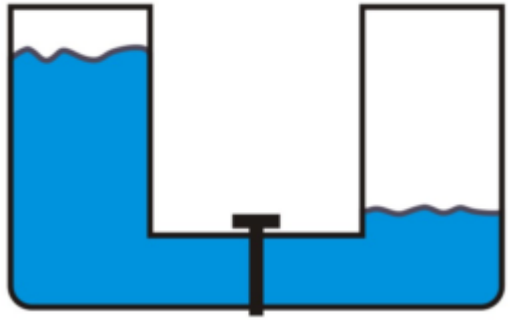


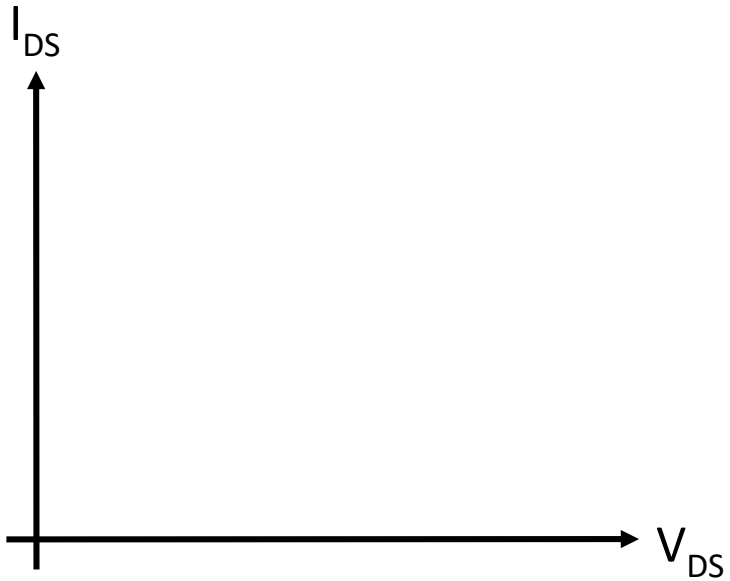
"Average" model during switching of device output

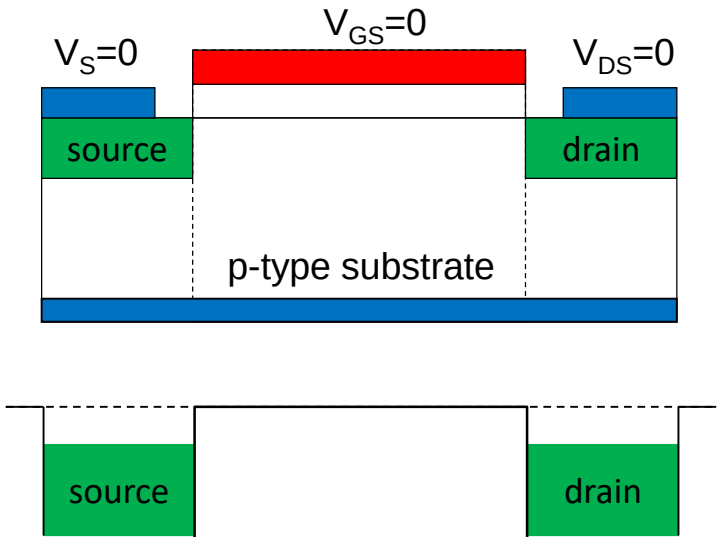
$C_G = WLC_{ox}$, where C_{ox} is the gate insulator capacitance per unit area, typically 20 fF/μm^2

$C_D = pC_G$, where p is a certain fraction of the gate capacitance, typically p=1

ON/OFF MOSFET operation







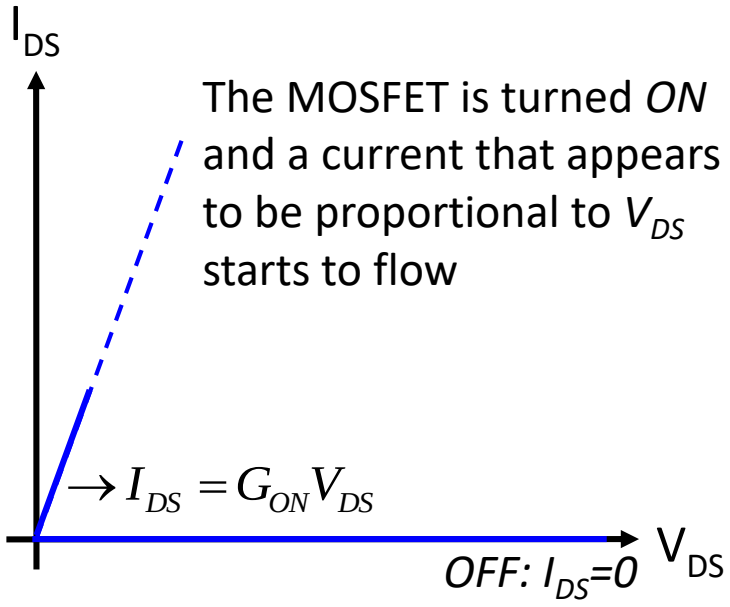
In this illustration of the MOSFET operation, the source and drain will be considered like two oceans of charge carriers isolated from each other through a potential barrier.

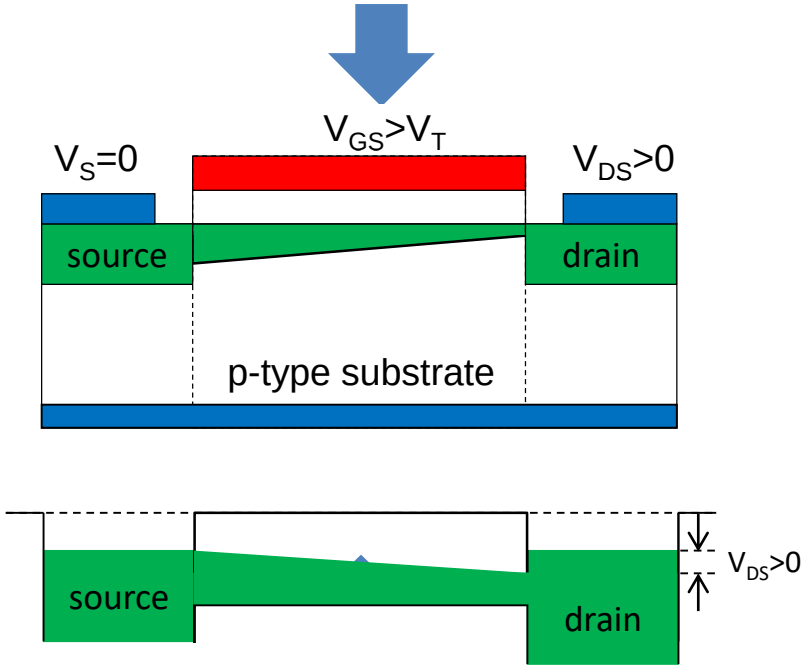
ON/OFF MOSFET operation

What if we apply small drain voltage? – The drain level is lowered, but the source is still isolated by the potential barrier!

However, applying a certain gate voltage called the threshold voltage V_T will just about remove the barrier.

Increasing the gate voltage beyond the threshold voltage will lower the potential barrier at the source even further and form a conducting channel between source and drain.





In this illustration of the MOSFET operation, the source and drain will be considered like two oceans of charge carriers isolated from each other through a potential barrier.

Calculating the ON conductance, G_{ON}

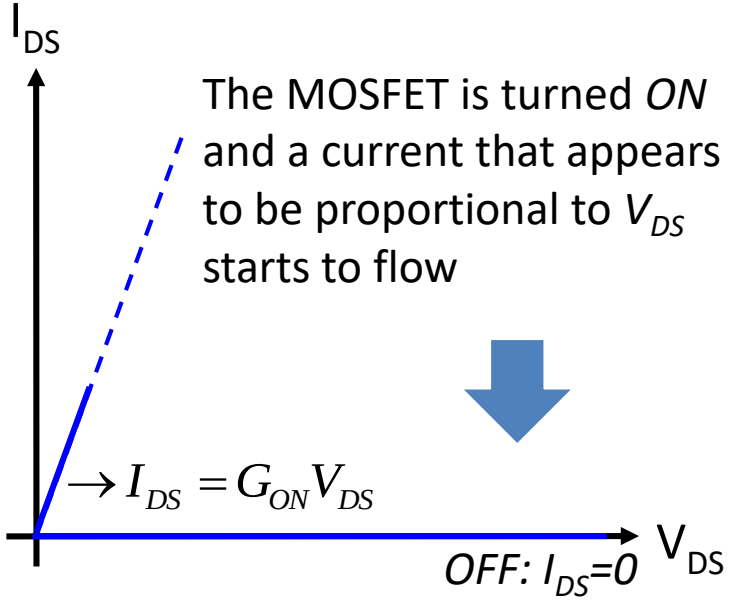
For calculating the ON conductance G_{ON}, let´s have a look at the mobile charge in the channel!

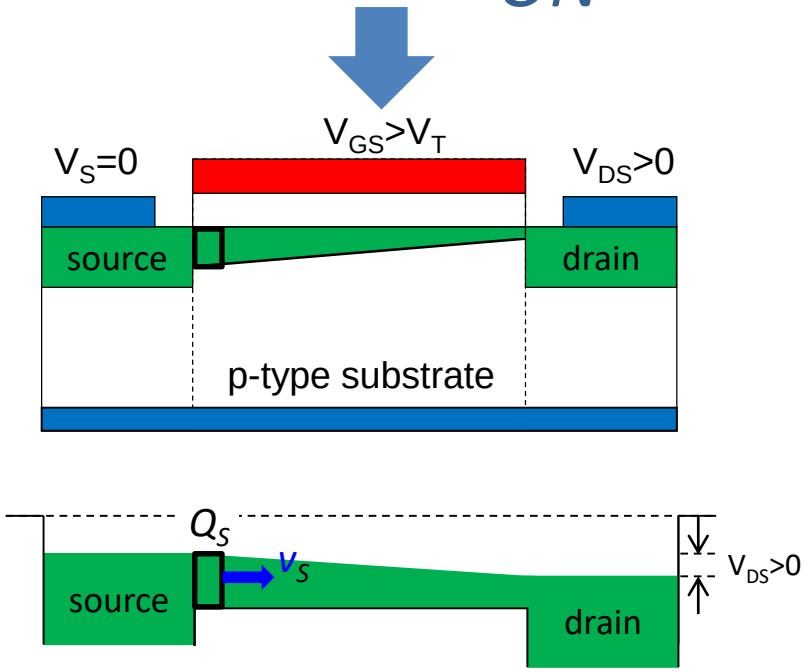
Mobile charge Q_S at source (per unit length):

$$Q_S = WC_{ox}\left(V_{GS} - V_T\right) = WC_{ox}V_{GT}$$

Charge carrier drift velocity at the source: $v_S=\mu E$, $E=V_{DS}/L$

Drain current: $I_{DS}=Q_S \times v_S$





If we introduce the conductance parameter $k = \frac{W}{L}\mu C_{ox}$

The drain current can be written $I_{DS} = kV_{GT}V_{DS}$

In this illustration of the MOSFET operation, the source and drain will be considered like two oceans of charge carriers isolated from each other through a potential barrier.

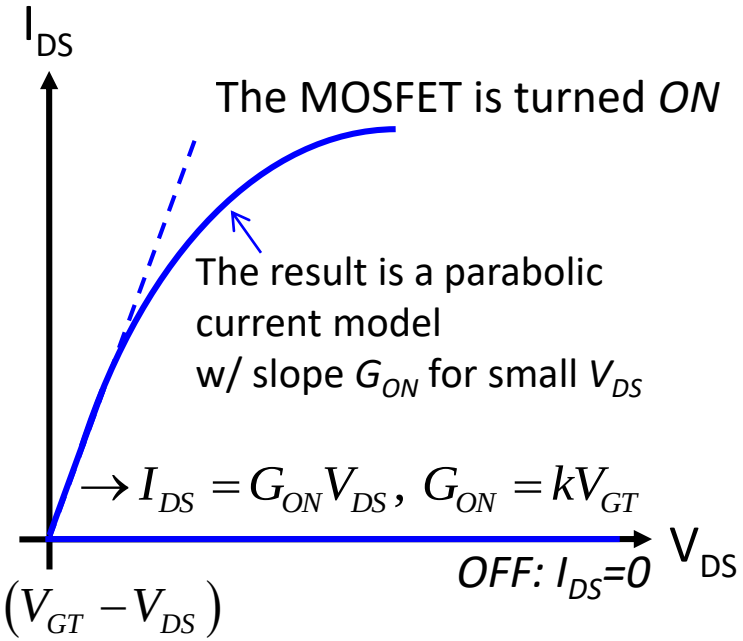
Having a closer look along the channel

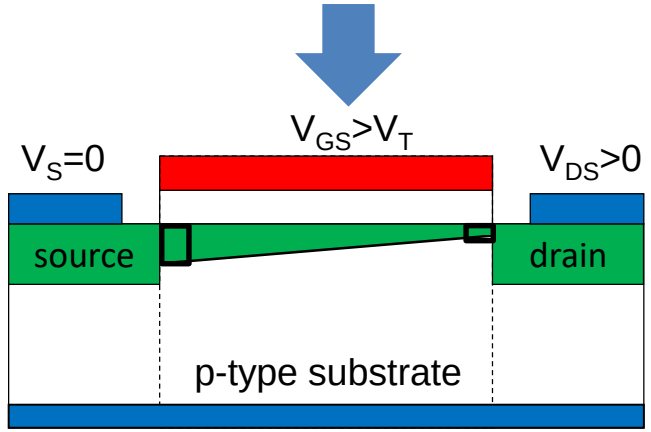
Mobile charge Q_S at source (per unit length):

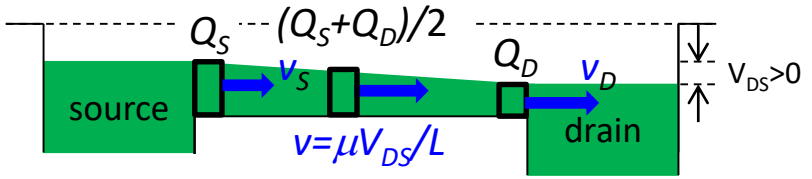
$$Q_S = WC_{ox}\left(V_{GS} - V_T\right) = WC_{ox}V_{GT}$$

Mobile charge Q_D at drain (per unit length):

$$Q_D = WC_{ox}\left(V_{GS} - V_{DS} - V_T\right) = WC_{ox}\left(V_{GT} - V_{DS}\right)$$







Here, $Q_D < Q_S$ because of the drain voltage.
Hence, drift velocity is higher at drain than at source, $v_D > v_S$,
This follows from the current being constant along the channel.

C_{ox} is the gate capacitance per unit area
W is the channel width
$V_{GT}=V_{GS}-V_T$ is the gate voltage overdrive
μ is the charge carrier mobility [cm^2/Vs]
$E=V_{DS}/L$ is the electric field along the channel

A thorough analysis based on the classical "gradual channel approximation" shows that the drain current is given by the average mobile charge density $(Q_S+Q_D)/2$ times the average drift velocity $v=\mu V_{DS}/L$

Understanding current saturation

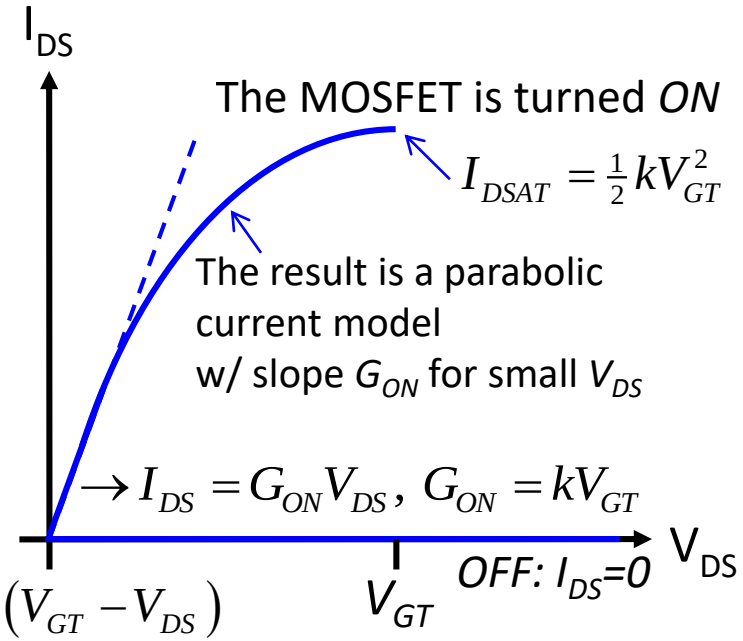
The drain current seems to saturate as $V_{DS} \rightarrow V_{GT}$

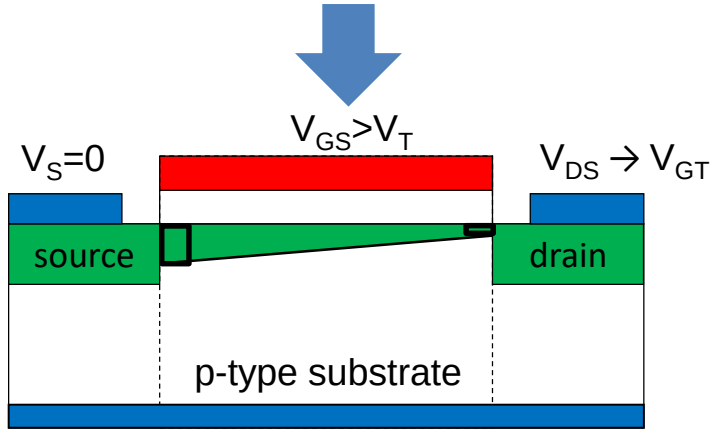
Mobile charge Q_S at source (per unit length):

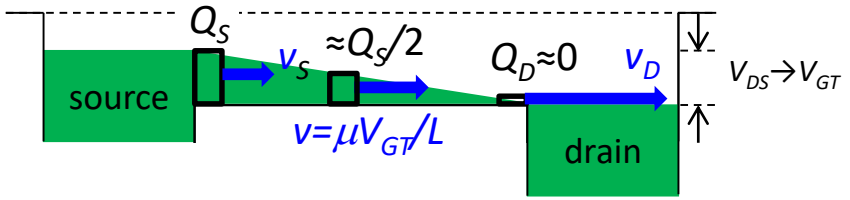
$$Q_S = WC_{ox}\left(V_{GS} - V_T\right) = WC_{ox}V_{GT}$$

Mobile charge Q_D at drain (per unit length):

$$Q_D = WC_{ox}\left(V_{GS} - V_{DS} - V_T\right) = WC_{ox}\left(V_{GT} - V_{DS}\right)$$







C_{ox} is the gate capacitance per unit area
W is the channel width
$V_{GT}=V_{GS}-V_T$ is the gate voltage overdrive
μ is the charge carrier mobility [cm²/Vs]
$E=V_{DS}/L$ is the electric field along the channel

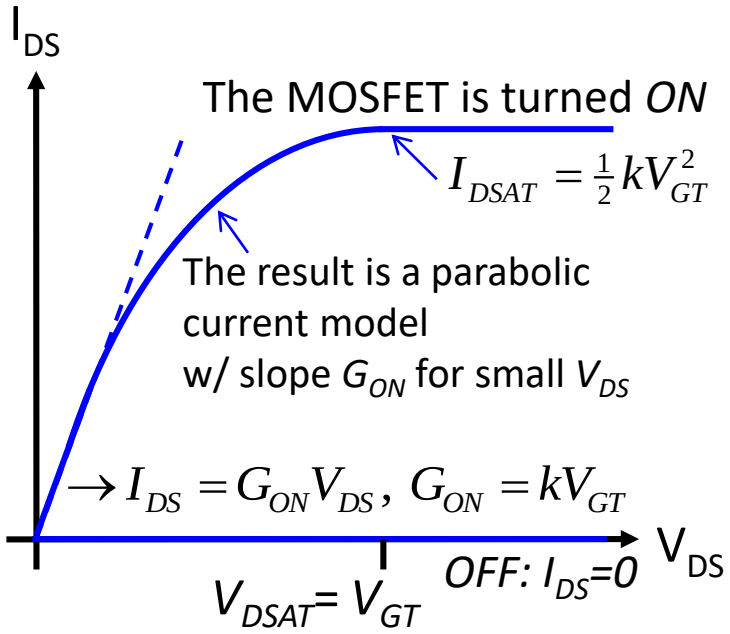
Here, $Q_D \rightarrow 0$ when $V_{DS} \rightarrow V_{GT}$
Hence, drift velocity at drain approaches "infinity", i.e. $v_D \rightarrow \infty$.
This follows from the current being constant along the channel.

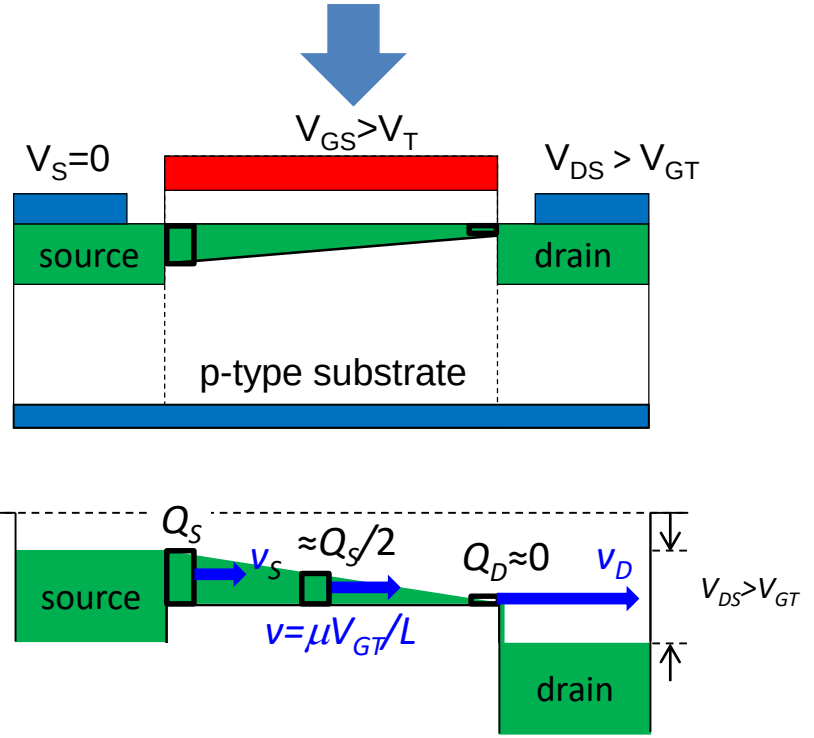
Hence, the drain current I_{DS}→ charge $Q_S/2$ × drift velocity $\mu V_{GT}/L$ as $V_{DS} \rightarrow V_{GT}$.

Understanding current saturation

What if we increase the drain voltage beyond the gate voltage overdrive, i.e. $V_{DS}>V_{GT}$

Actually, the conditions within the channel does not change with the height of the "water fall" between the drain end of the channel and the drain!





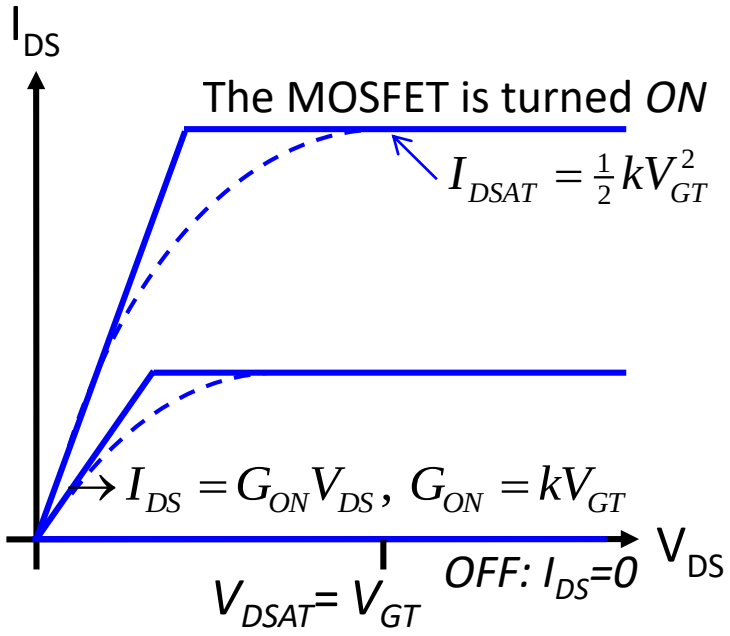
Drain current stays constant! → The saturation current I_{DSAT} is given by the gate voltage overdrive V_{GT} squared! → The saturation voltage V_{DSAT} is given by Q_D=0, → $V_{DSAT}=V_{GS}-V_T$, i.e. the gate voltage overdrive V_{GT}

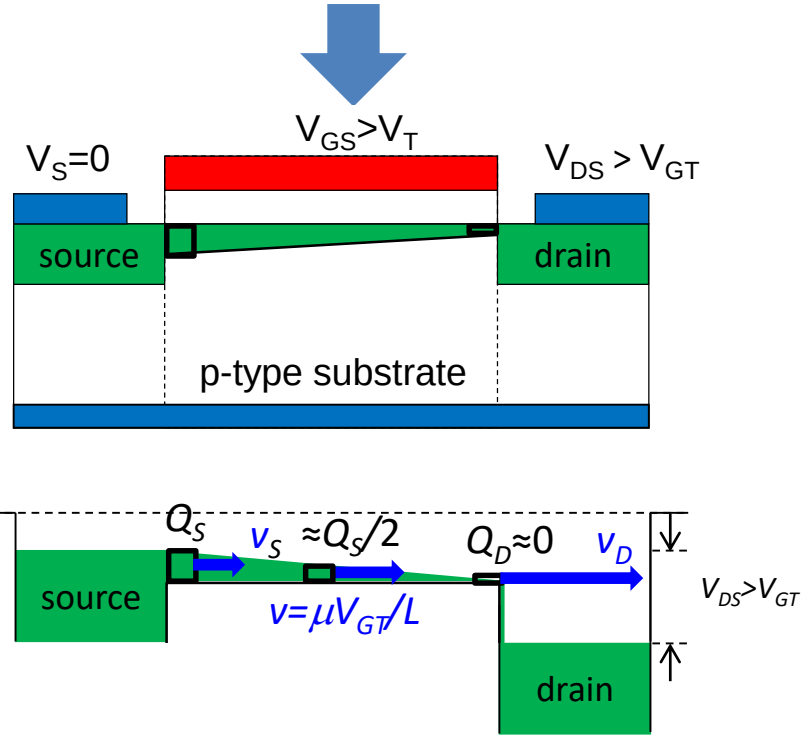
Piecewise linear MOSFET Model

What if we simplify the model, focusing on the two main behaviors of the MOSFET?

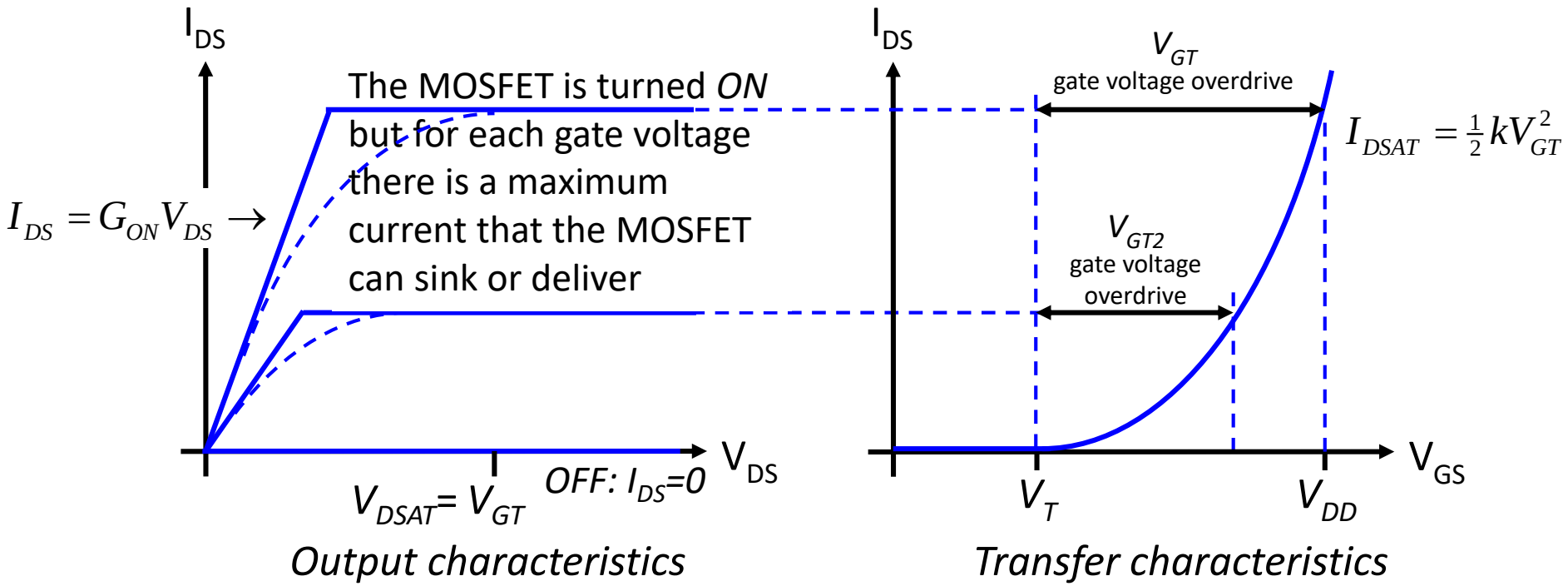
Linear behavior for small drain voltages - G_{ON}
Saturated behavior for large drain voltages - I_{DSAT}

What if we decrease the gate voltage overdrive?





MOSFET output and transfer characteristics



The MOSFET is basically a "square-law" device!

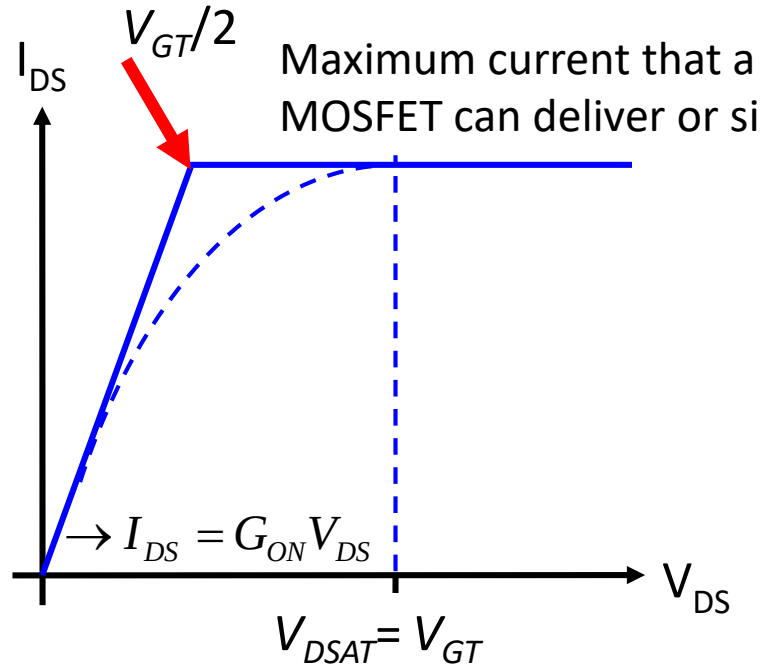
Example

A fully turned on MOSFET has an on resistance of 1 kΩ. What is the maximum current that this device can deliver or sink? Assume V_{DD}=1.2 V, and V_T=0.3 V.

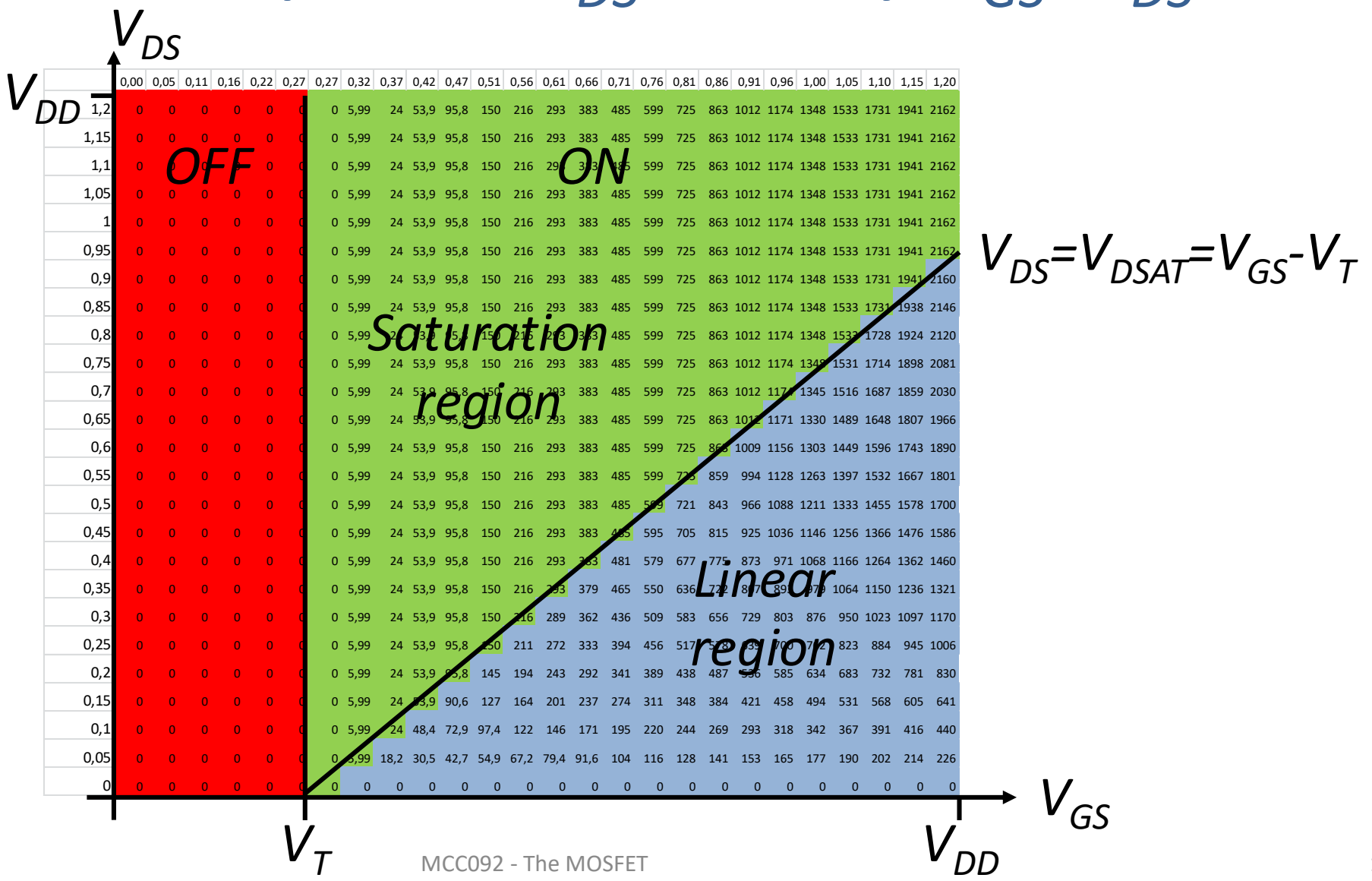
Solution: We know that a long-channel MOSFET saturates for $V_{DSAT}=V_{GT}=V_{GS}-V_T$. Hence, in this case we have V_{DSAT}=0.9 V.

Since the MOSFET is a square-law device (w/ parabolic I-V model) we know that the piecewise linear model breakpoint occurs at $V_{GT}/2$.

Hence, maximum current is given by $I_{DS} = G_{ON} V_{DS} = \frac{V_{GT}/2}{R_{ON}} = \frac{0.45}{1} = 450\ \mu A$

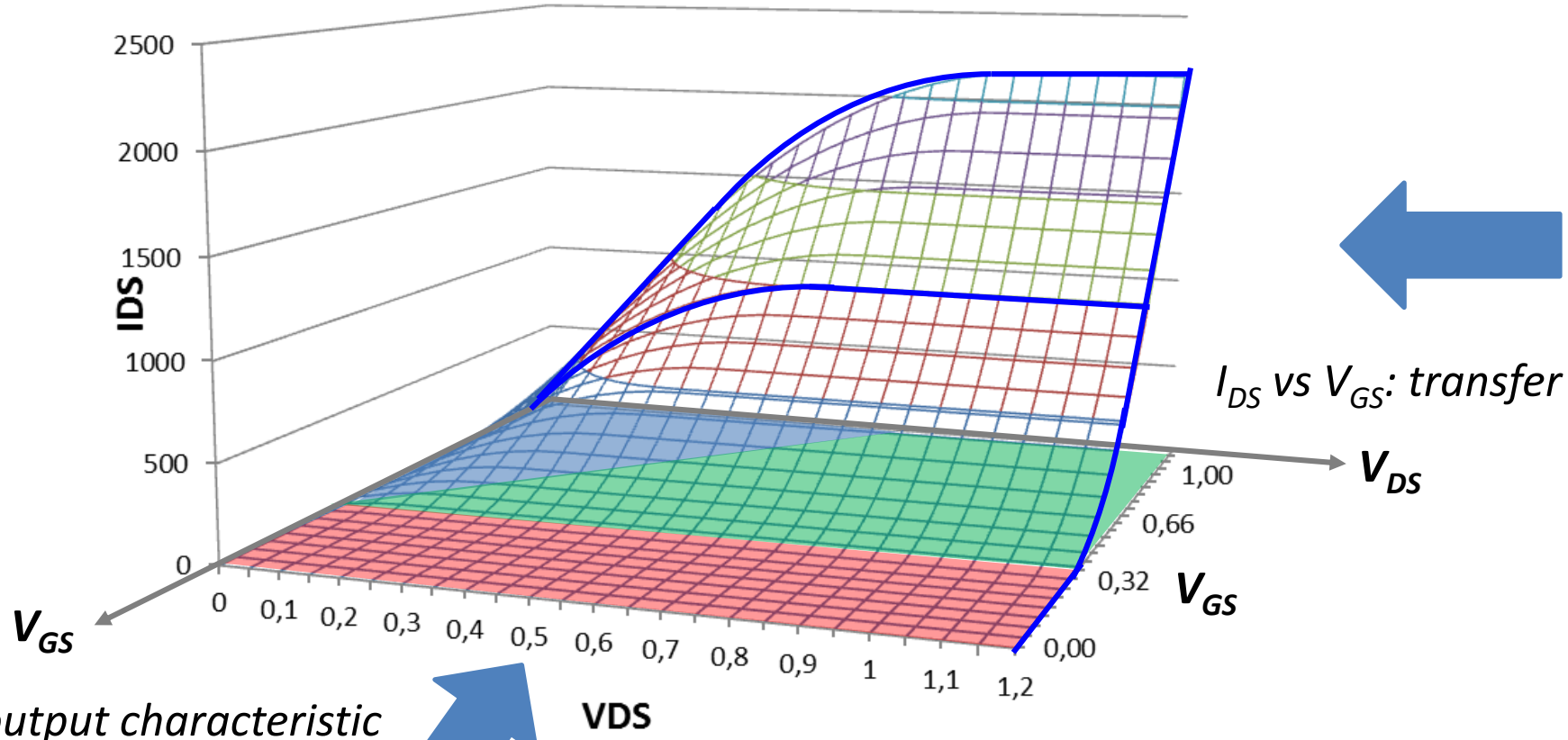


Model can predict I_{DS} for any V_{GS}/V_{DS}



V_{DS} / V_{GS}	0,00	0,05	0,11	0,16	0,22	0,27	0,27	0,32	0,37	0,42	0,47	0,51	0,56	0,61	0,66	0,71	0,76	0,81	0,86	0,91	0,96	1,00	1,05	1,10	1,15	1,20
1,2	0	0	0	0	0	0	0	5,99	24	53,9	95,8	150	216	293	383	485	599	725	863	1012	1174	1348	1533	1731	1941	2162
1,15	0	0	0	0	0	0	0	5,99	24	53,9	95,8	150	216	293	383	485	599	725	863	1012	1174	1348	1533	1731	1941	2162
1,1	0	0	0	0	0	0	0	5,99	24	53,9	95,8	150	216	293	383	485	599	725	863	1012	1174	1348	1533	1731	1941	2162
1,05	0	0	0	0	0	0	0	5,99	24	53,9	95,8	150	216	293	383	485	599	725	863	1012	1174	1348	1533	1731	1941	2162
1	0	0	0	0	0	0	0	5,99	24	53,9	95,8	150	216	293	383	485	599	725	863	1012	1174	1348	1533	1731	1941	2162
0,95	0	0	0	0	0	0	0	5,99	24	53,9	95,8	150	216	293	383	485	599	725	863	1012	1174	1348	1533	1731	1941	2162
0,9	0	0	0	0	0	0	0	5,99	24	53,9	95,8	150	216	293	383	485	599	725	863	1012	1174	1348	1533	1731	1941	2160
0,85	0	0	0	0	0	0	0	5,99	24	53,9	95,8	150	216	293	383	485	599	725	863	1012	1174	1348	1533	1731	1938	2146
0,8	0	0	0	0	0	0	0	5,99	24	53,9	95,8	150	216	293	383	485	599	725	863	1012	1174	1348	1533	1728	1924	2120
0,75	0	0	0	0	0	0	0	5,99	24	53,9	95,8	150	216	293	383	485	599	725	863	1012	1174	1348	1531	1714	1898	2081
0,7	0	0	0	0	0	0	0	5,99	24	53,9	95,8	150	216	293	383	485	599	725	863	1012	1174	1345	1516	1687	1859	2030
0,65	0	0	0	0	0	0	0	5,99	24	53,9	95,8	150	216	293	383	485	599	725	863	1012	1171	1330	1489	1648	1807	1966
0,6	0	0	0	0	0	0	0	5,99	24	53,9	95,8	150	216	293	383	485	599	725	863	1009	1156	1303	1449	1596	1743	1890
0,55	0	0	0	0	0	0	0	5,99	24	53,9	95,8	150	216	293	383	485	599	725	859	994	1128	1263	1397	1532	1667	1801
0,5	0	0	0	0	0	0	0	5,99	24	53,9	95,8	150	216	293	383	485	599	721	843	966	1088	1211	1333	1455	1578	1700
0,45	0	0	0	0	0	0	0	5,99	24	53,9	95,8	150	216	293	383	485	595	705	815	925	1036	1146	1256	1366	1476	1586
0,4	0	0	0	0	0	0	0	5,99	24	53,9	95,8	150	216	293	383	481	579	677	775	873	971	1068	1166	1264	1362	1460
0,35	0	0	0	0	0	0	0	5,99	24	53,9	95,8	150	216	293	379	465	550	636	722	807	893	979	1064	1150	1236	1321
0,3	0	0	0	0	0	0	0	5,99	24	53,9	95,8	150	216	289	362	436	509	583	656	729	803	876	950	1023	1097	1170
0,25	0	0	0	0	0	0	0	5,99	24	53,9	95,8	150	211	272	333	394	456	517	578	639	700	761	823	884	945	1006
0,2	0	0	0	0	0	0	0	5,99	24	53,9	95,8	145	194	243	292	341	389	438	487	536	585	634	683	732	781	830
0,15	0	0	0	0	0	0	0	5,99	24	53,9	90,6	127	164	201	237	274	311	348	384	421	458	494	531	568	605	641
0,1	0	0	0	0	0	0	0	5,99	24	48,4	72,9	97,4	122	146	171	195	220	244	269	293	318	342	367	391	416	440
0,05	0	0	0	0	0	0	0	5,99	18,2	30,5	42,7	54,9	67,2	79,4	91,6	104	116	128	141	153	165	177	190	202	214	226
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

I_{DS} can be plotted in 3D vs. V_{GS}&V_{DS}



I_{DS} vs V_{GS}: transfer characteristic

I_{DS} vs V_{DS}: output characteristic

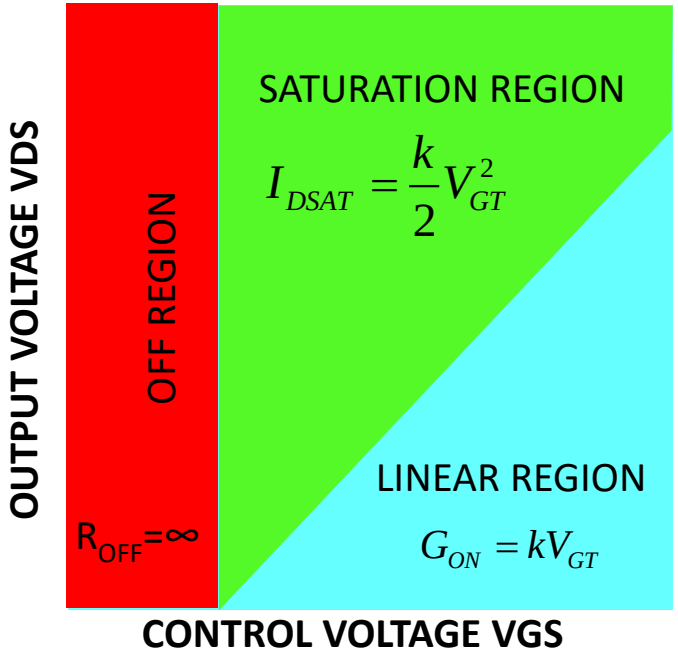
MOSFET regions of operation

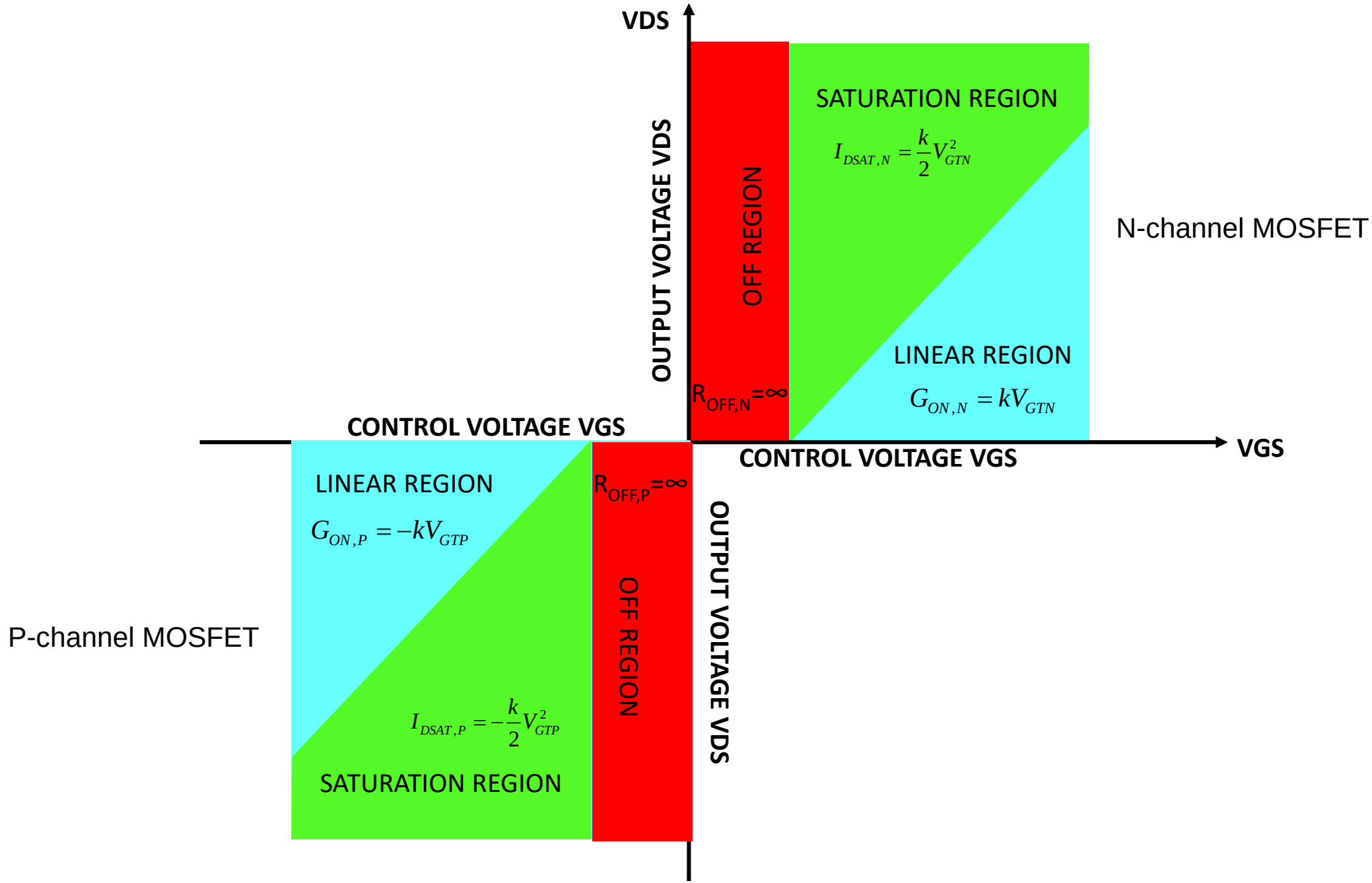
- Why are colored MOSFET regions of operation important?
- Because they visualize the formula to use for estimating the drain durrent

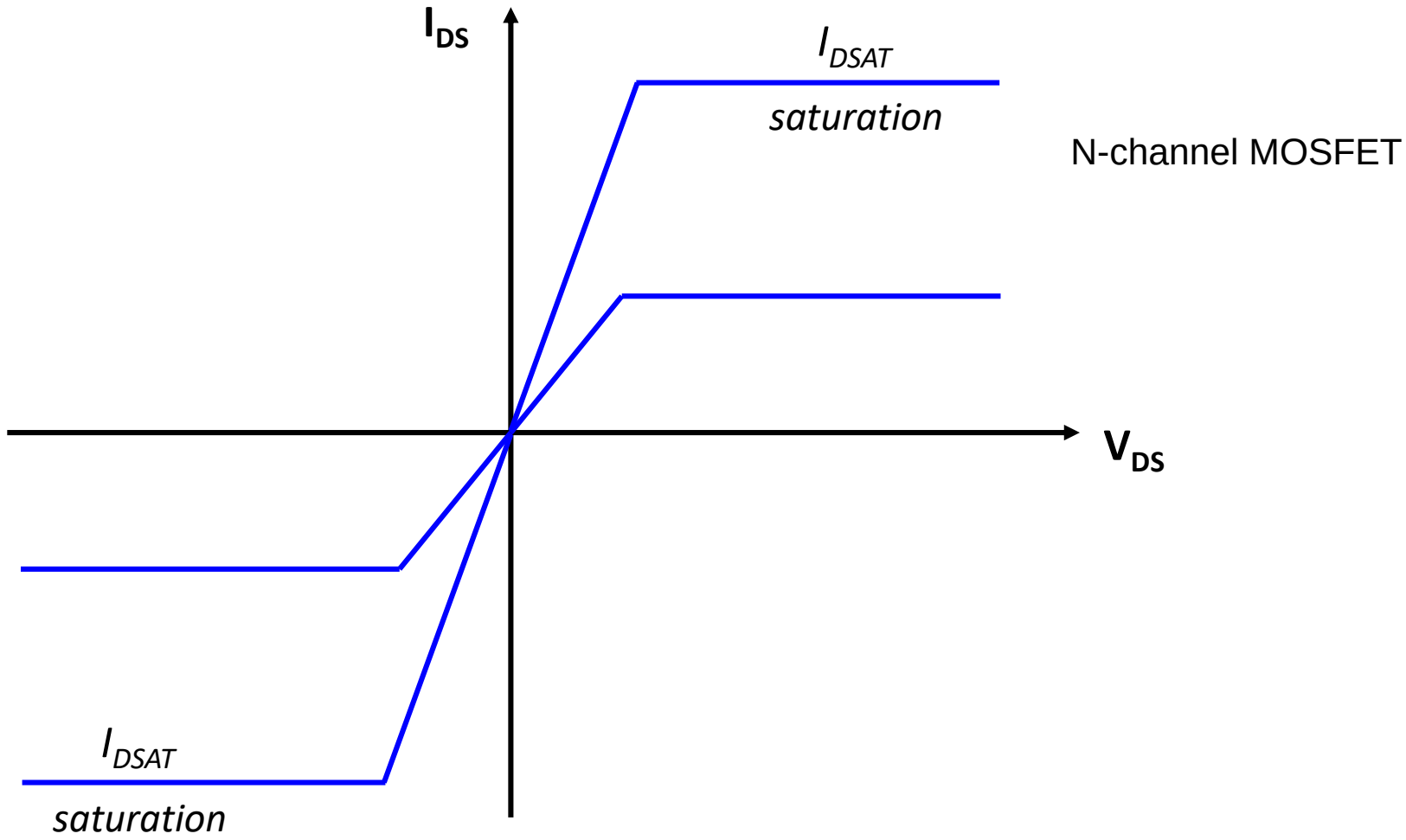
$$I_{DSUB} = 0$$

$$I_{DS} = k\left(V_{GT} - \frac{V_{DS}}{2}\right)V_{DS} = G_{ON}V_{DS}\left(1 - \frac{V_{DS}}{2V_{GT}}\right)$$

$$I_{DSAT} = \frac{k}{2}V_{GT}^2$$



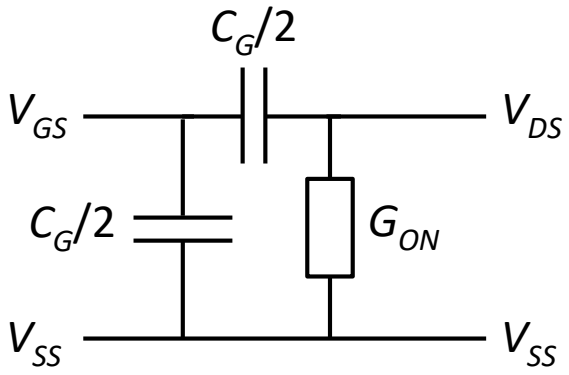

VDS
OUTPUT VOLTAGE VDS
OFF REGION
SATURATION REGION
$I_{DSAT,N} = \frac{k}{2} V_{GTN}^2$
LINEAR REGION
$G_{ON,N} = kV_{GTN}$
N-channel MOSFET
$R_{OFF,N}=\infty$
CONTROL VOLTAGE VGS
CONTROL VOLTAGE VGS
VGS
LINEAR REGION
$G_{ON,P} = -kV_{GTP}$
$R_{OFF,P}=\infty$
OUTPUT VOLTAGE VDS
OFF REGION
P-channel MOSFET
$I_{DSAT,P} = -\frac{k}{2} V_{GTP}^2$
SATURATION REGION


I_{DS}
I_{DSAT}
saturation
N-channel MOSFET
V_{DS}
P-channel MOSFET
I_{DSAT}
saturation

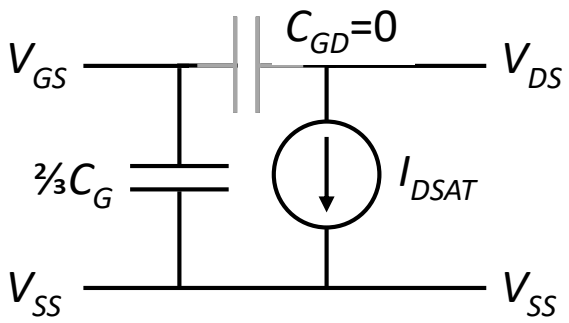
Summary

- In this lecture, The MOSFET has been regarded as an electrically controlled ON/OFF switch.
- Input and output voltages are referred to source
  - Current controlling gate voltage V_{GS}.
  - The output drain voltage V_{DS}.
- The MOSFET current is a function of both voltages, V_{GS} and V_{DS}.
- When ON, the MOSFET behaves
  - like a resistor R_{ON} in its linear region,
  - like a constant-current source I_{DSAT} in its saturation region.
- First-order approximation yields a square-law model for I_{DSAT}=f(V_{GT}^2)
- When OFF, there is a subthreshold leakage current, I_{SUB}.
- Very useful to color code the three regions of operation
  - Red for OFF
  - Green for ON and saturated (and blue for ON and linear operation)

Equivalent electrical two-port circuit model



Model for linear device

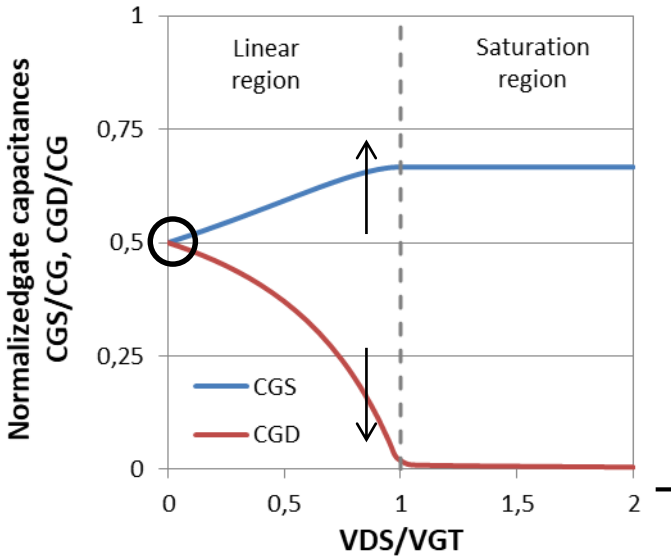


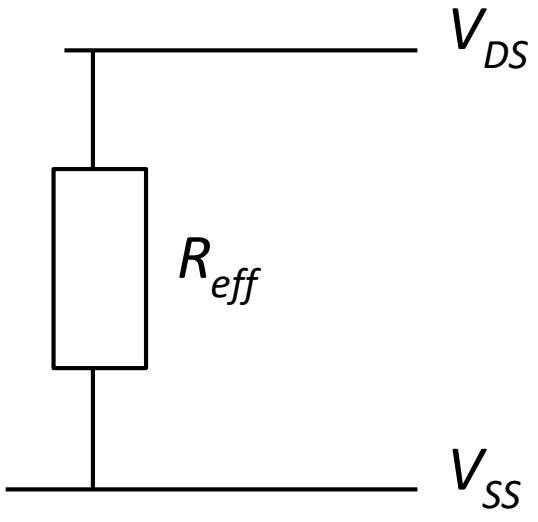
Model for saturated device

In the linear region, the capacitance splits equally between source and drain

In the saturation region, the capacitance tilts towards the source!

The distributed gate to channel capacitance must be lumped to the available ckt nodes, i.e. to source and drain





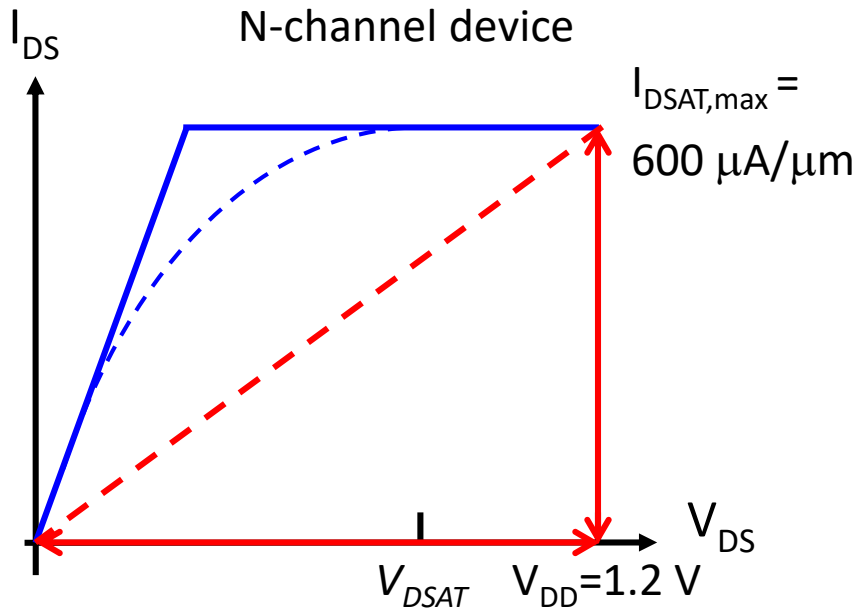
"Average" model during switching of device output

Q: Why use $C_{GS}=C_G$ and not $C_{GS}=⅔C_G$?
A: Integers are easier to handle and there are parasitic overlap and fringing field caps there to motivate the approximation!

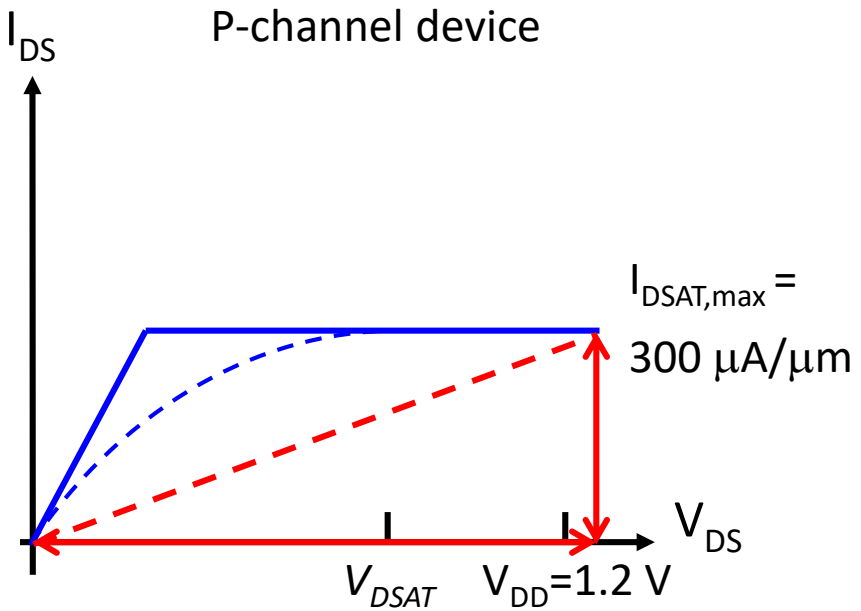
The field-effect upon which the operation of a MOSFET relies, gives the MOSFET a capacitive input!

Effective resistances: 65 nm MOSFETs

$R_{N,eff}$=2 kΩ·μm



$R_{P,eff}$=4 kΩ·μm

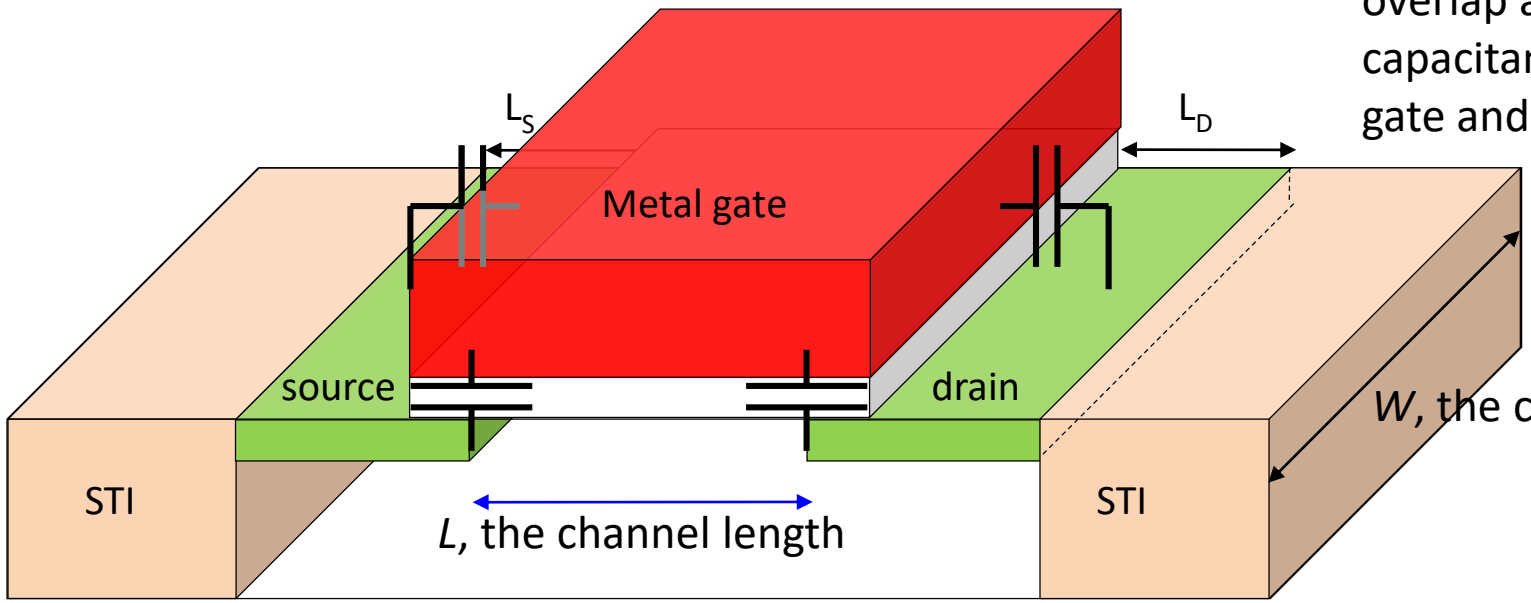


Q: Why is there a difference between n- and p-channel effective resistances?

A: Hole mobility in p-channel device is only half of electron mobility in n-channel device!

MOSFET gate capacitance

FYI, there are also parasitic overlap and fringing field capacitances between the gate and source/drain

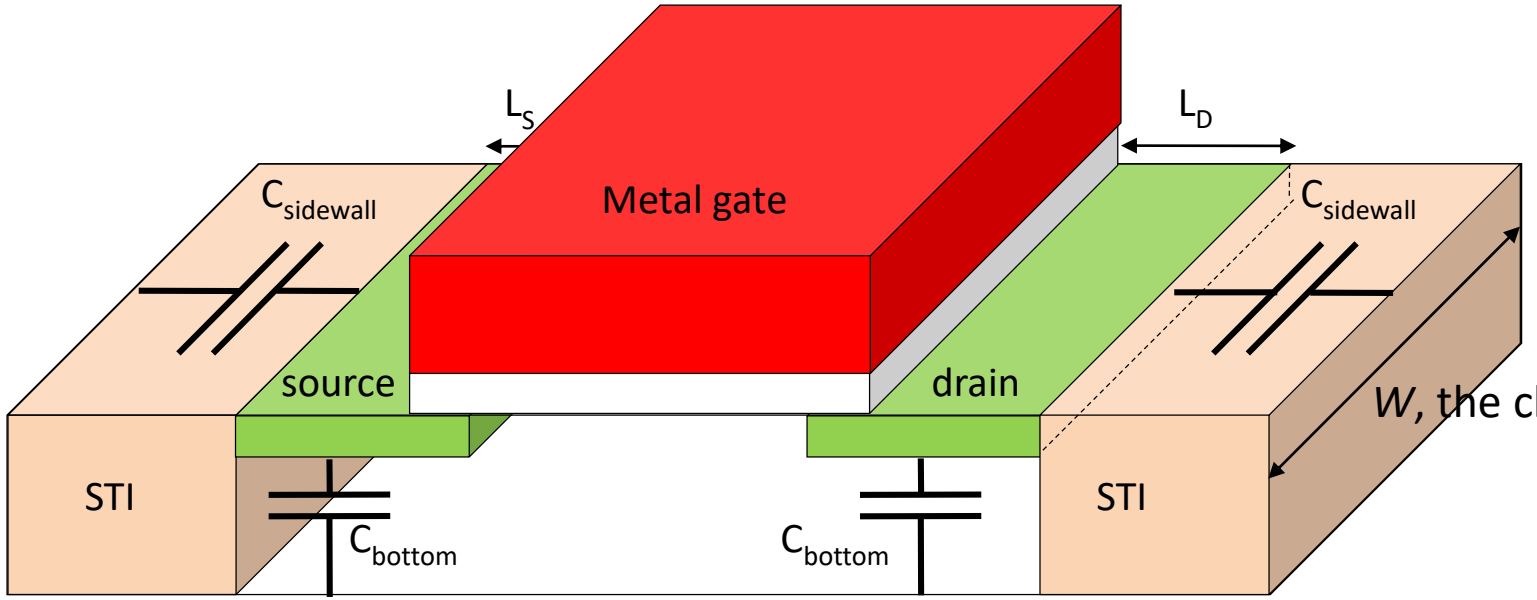


The capacitance between gate and channel, $C_G=WLC_{ox}$, is intrinsic to the field effect!

In a 65 nm CMOS process, typically C_{ox}=20 fF/μm^2

When using fixed channel lengths, L=65 nm, as in digital designs, gate cap C_G scales with channel width

Source/drain parasitic capacitances



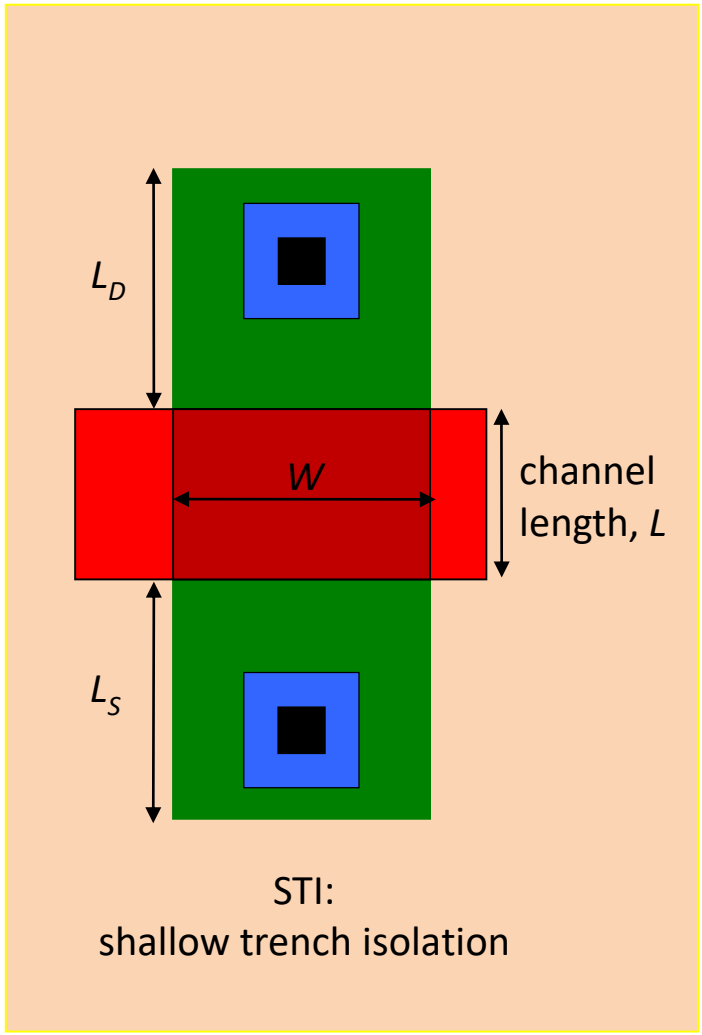
The source and drain capacitances are extrinsic to the field effect!

Therefore regarded as parasitic capacitances, but are non-negligible, i.e. $C_D = pC_G$, where $p \approx 1$.

Sidewall caps due to source/drain lateral dimensions L_S and L_D, are usually small

➡ Just as for the gate cap, we will consider source/drain caps scalable with channel width

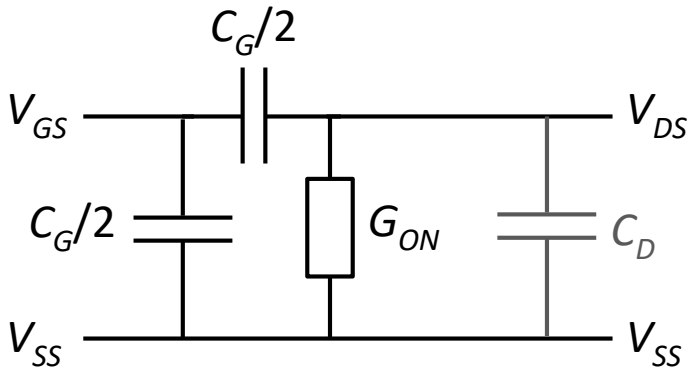
65 nm CMOS capacitances



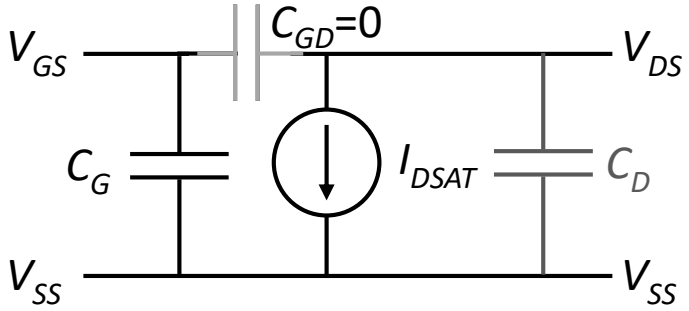
C_{ox}≈20 fF/um^2
(corresponds to 1.2 nm effective oxide thickness)
60 nm effective channel length yields: C_G=1.2 fF/um

Drain/source parasitic caps
The parasitic caps are of the same order of magnitude as the gate capacitance, C_S=C_D=pC_G
Generic approach is to use p=1 for simplicity
But sometimes p=0.5 or p=0.8!

Equivalent electrical two-port circuit model

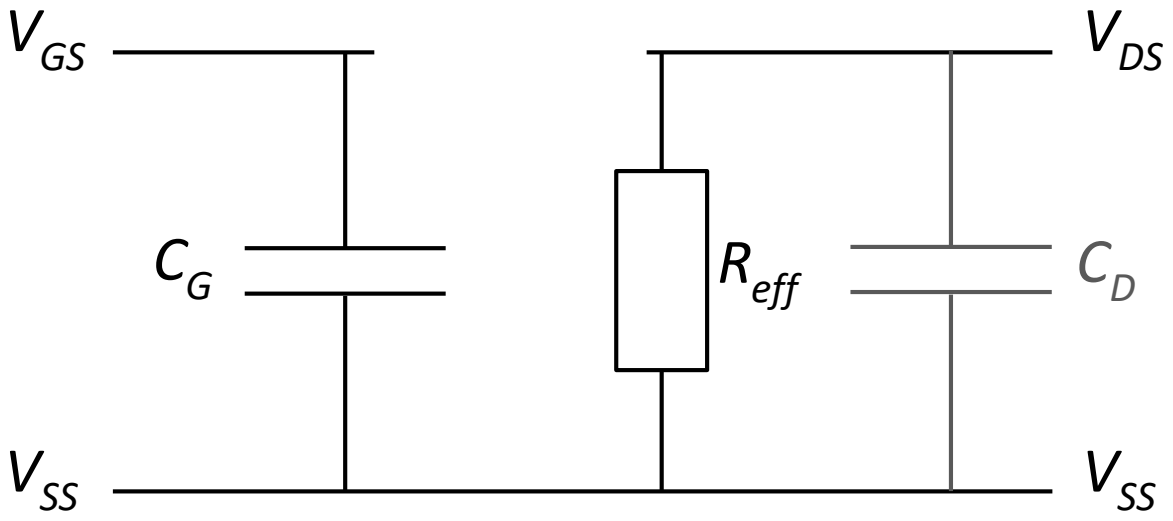


Model for linear device



Model for saturated device

The distributed gate to channel capacitance must be lumped to the available ckt nodes, i.e. source and drain



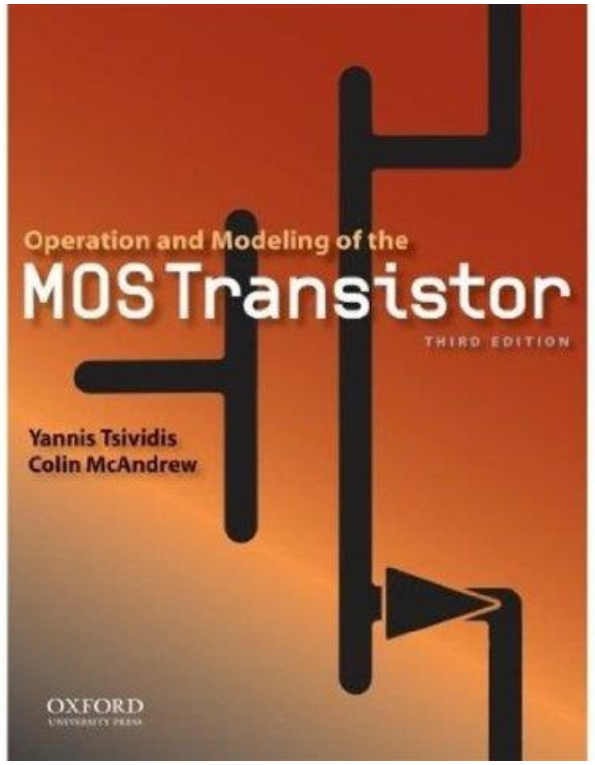
"Average" model during switching of device output

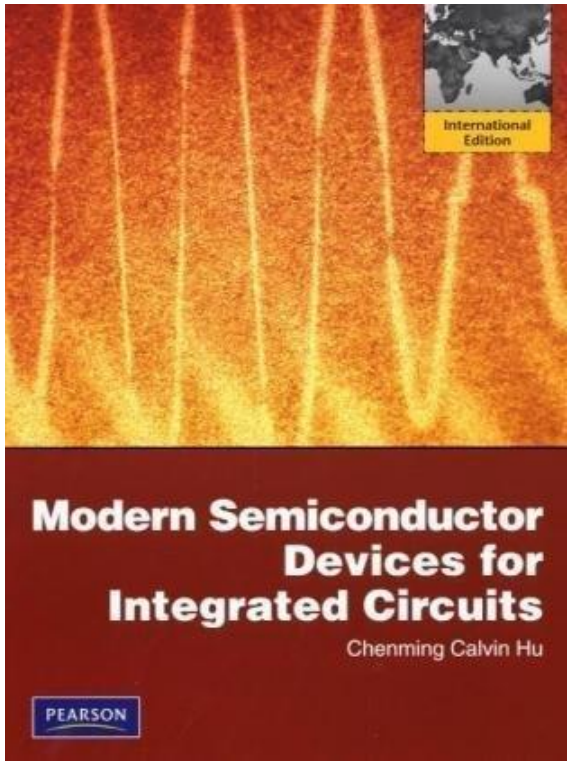
$C_G = WLC_{ox}$, where C_{ox} is the gate insulator capacitance per unit area, typically 20 fF/μm^2

$C_D = pC_G$, where p is a certain fraction of the gate capacitance, typically p=1

The MOSFET in detail

- A number of textbooks treat MOSFET models in great detail, including their physical background and short-comings due to short-channel effects in nanoscale devices






BSIM4v4.7 MOSFET Model

-User's Manual

Tanvir Hasan Morshed, Darsen D. Lu, Wenwei (Morgan) Yang, Mohan V. Dunga, Xuemei (Jane) Xi, Jin He,

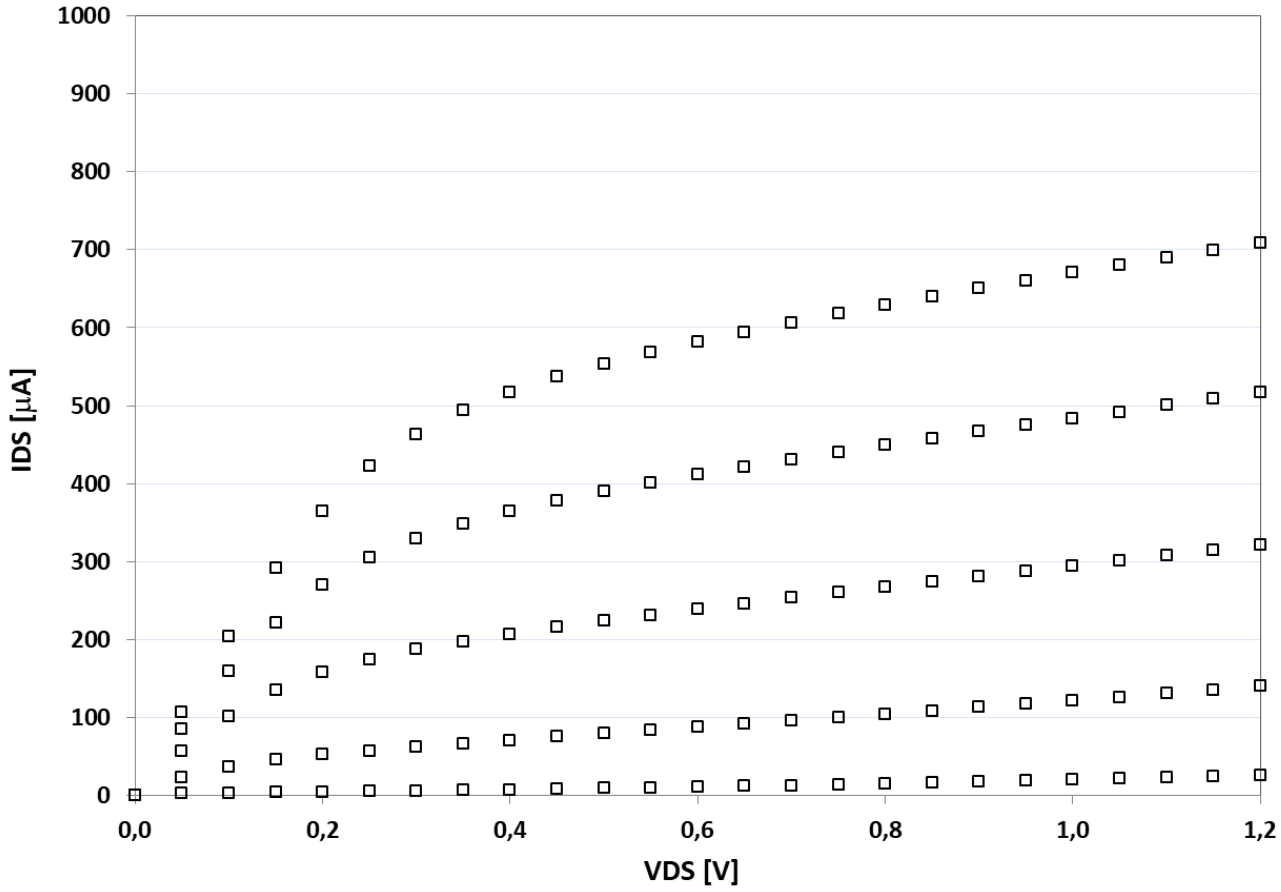
Weidong Liu, Kanyu, M. Cao, Xiaodong Jin, Jeff J. Ou, Mansun Chan,

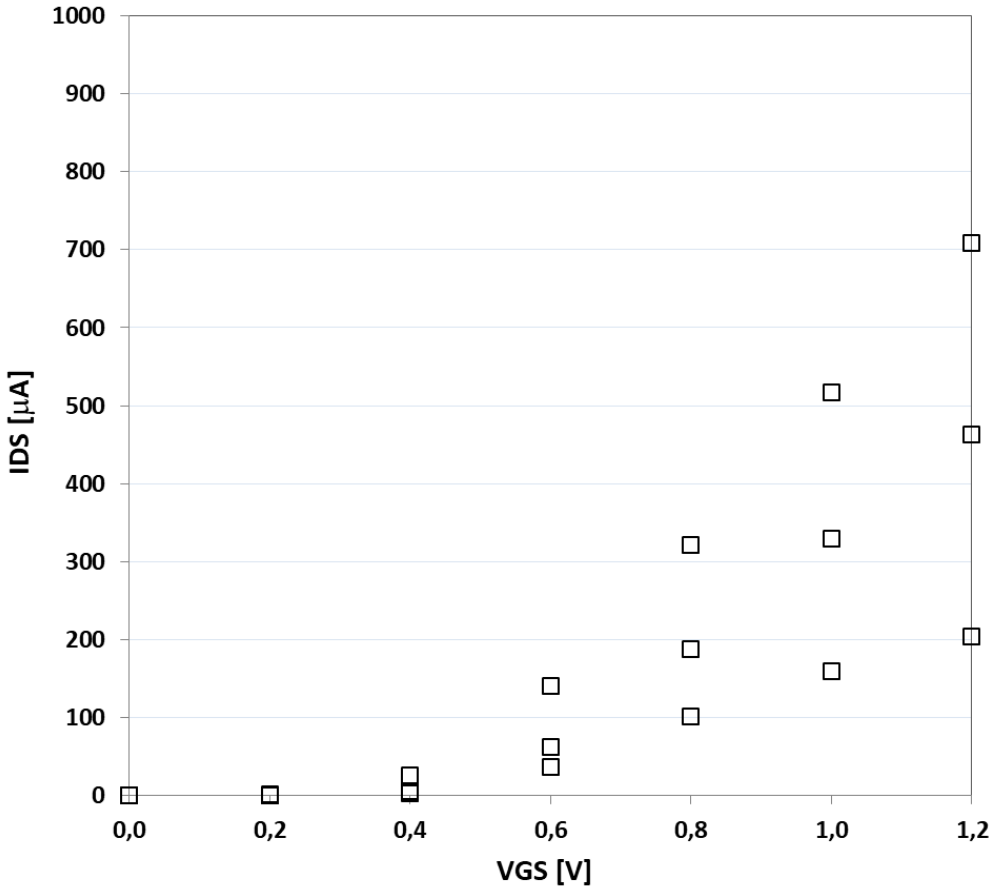
Ali M. Niknejad, Chenming Hu

Department of Electrical Engineering and Computer Sciences
University of California, Berkeley, CA 94720

How good is my model?

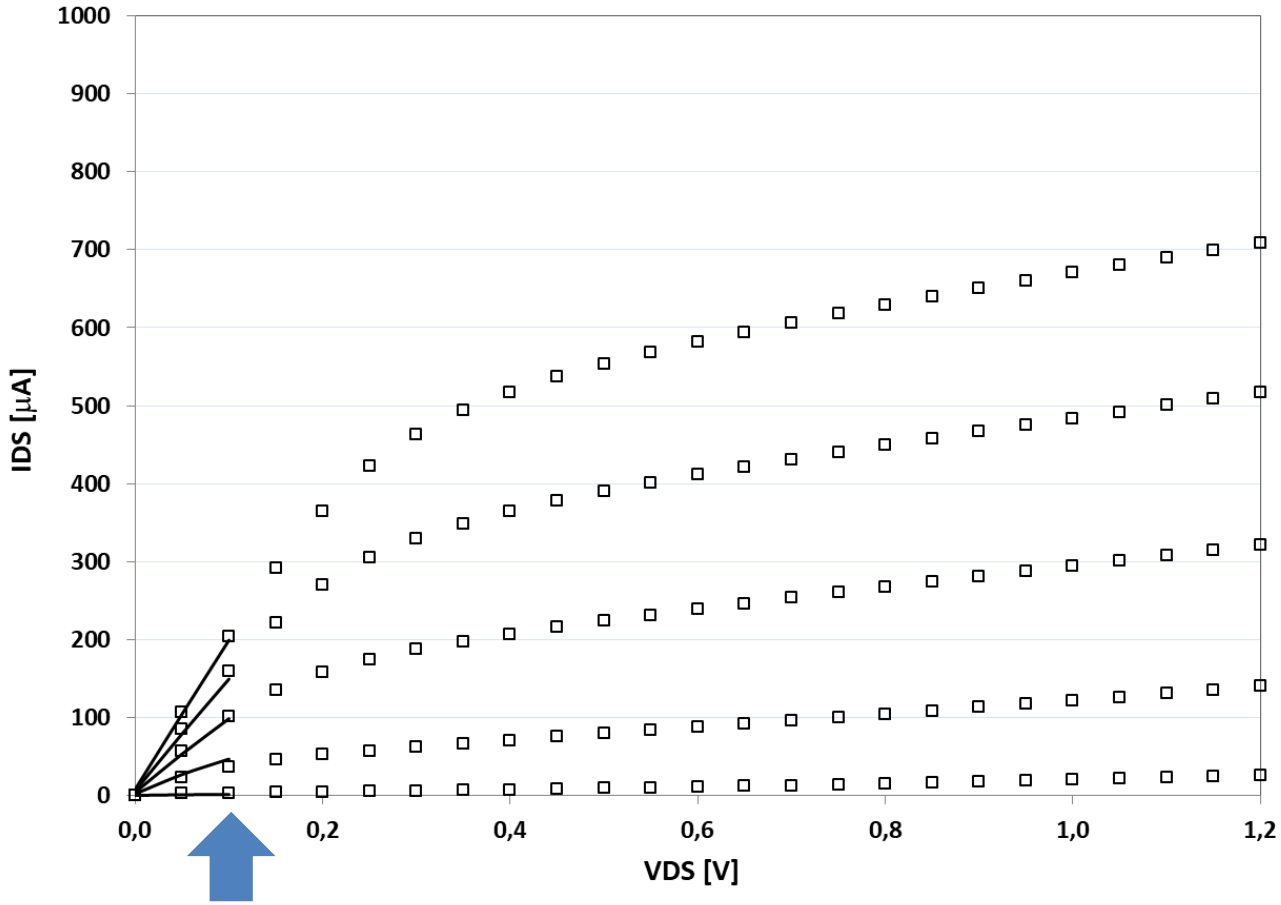
More parameters considering second-order effects must be included for fitting model to experimental data

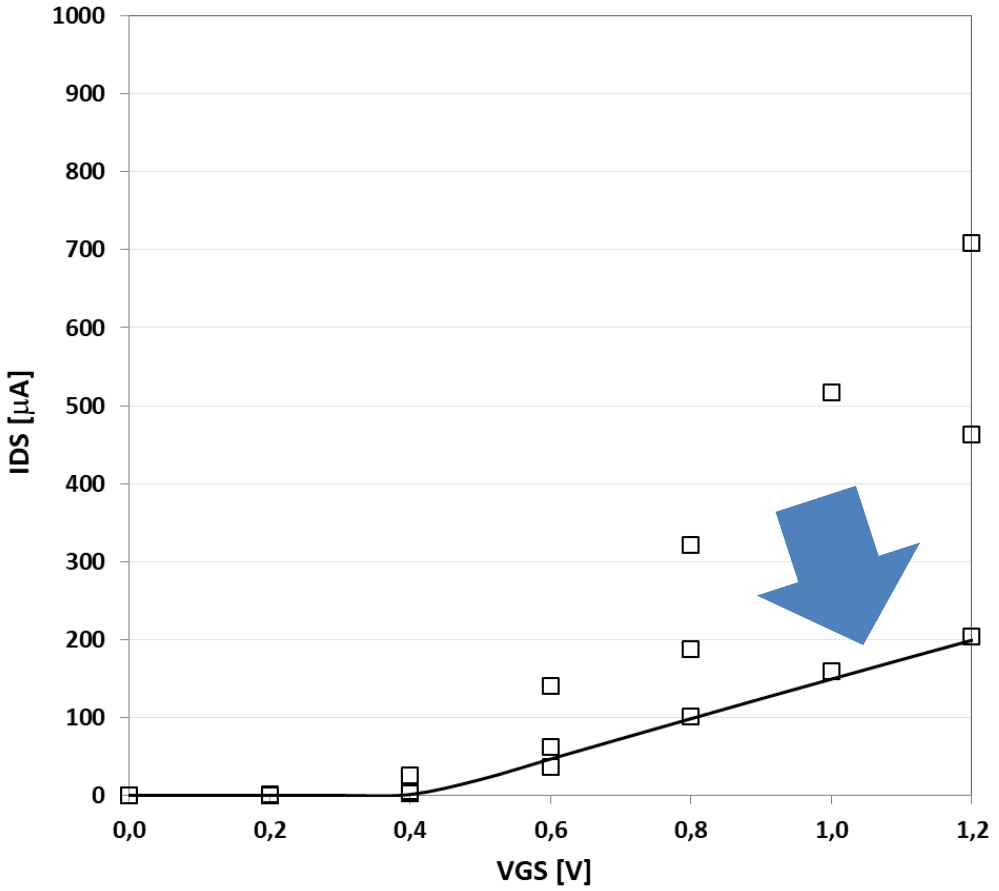




Determine k and V_T @ V_{DS}=100 mV

More parameters considering second-order effects must be included for fitting model to experimental data





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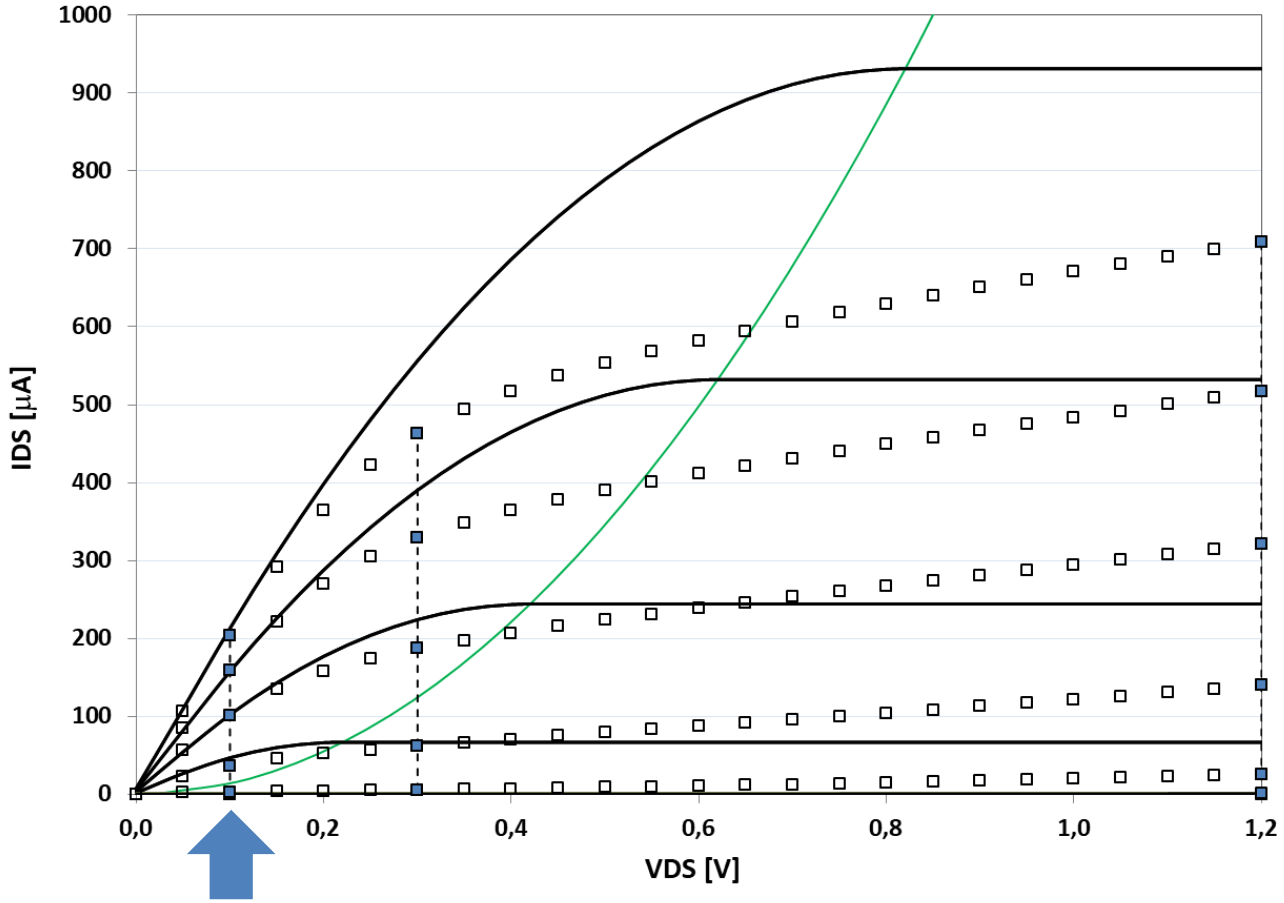
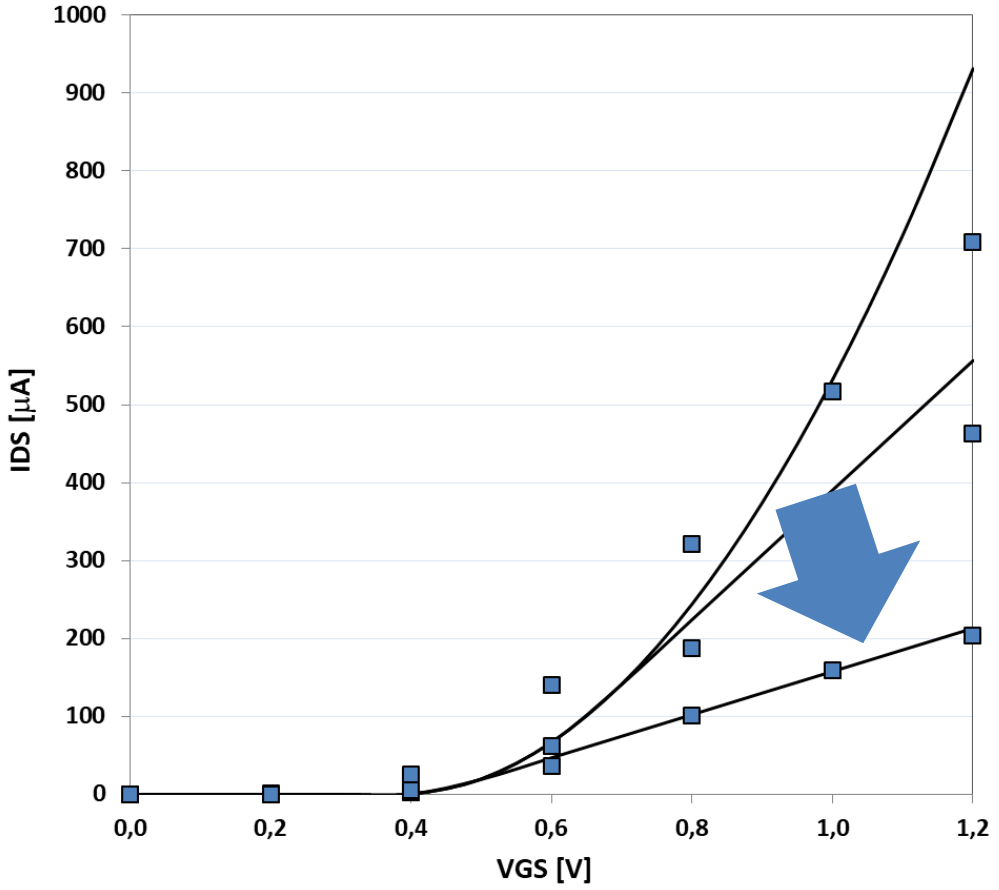
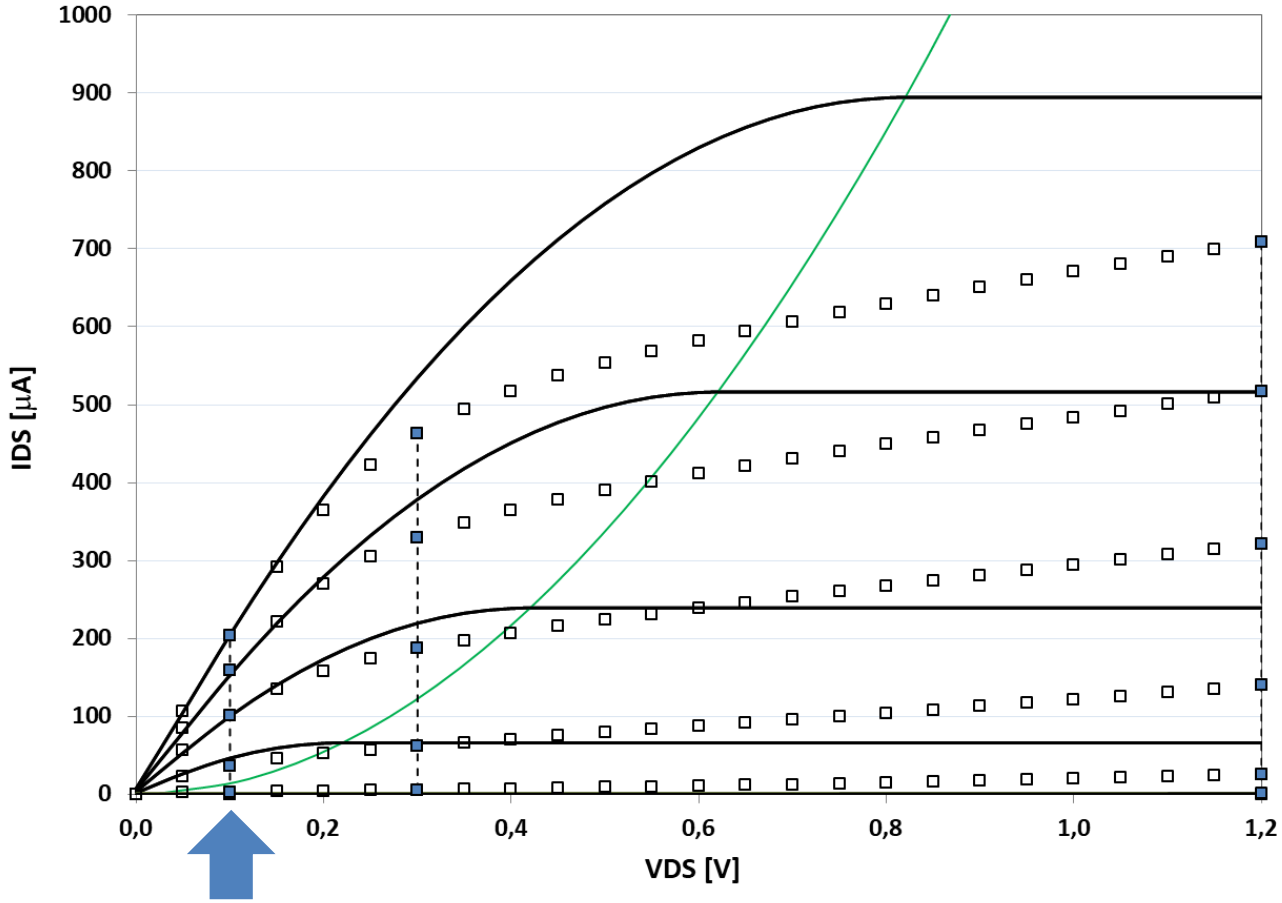
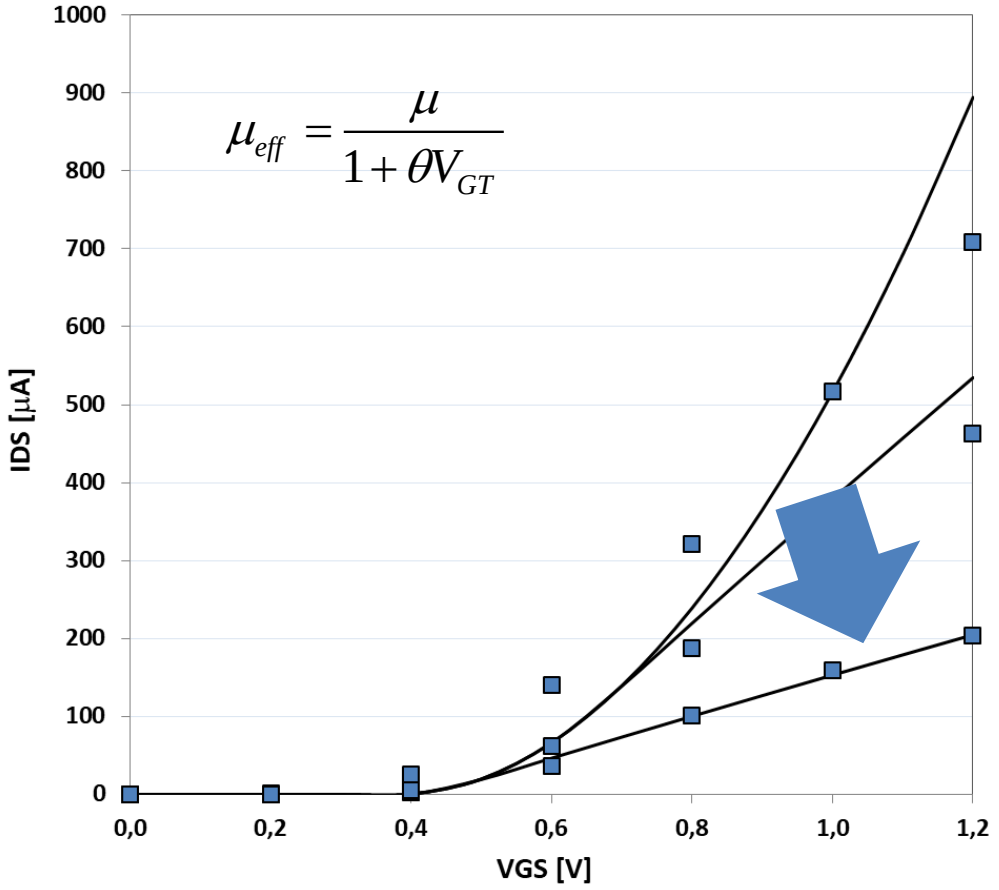


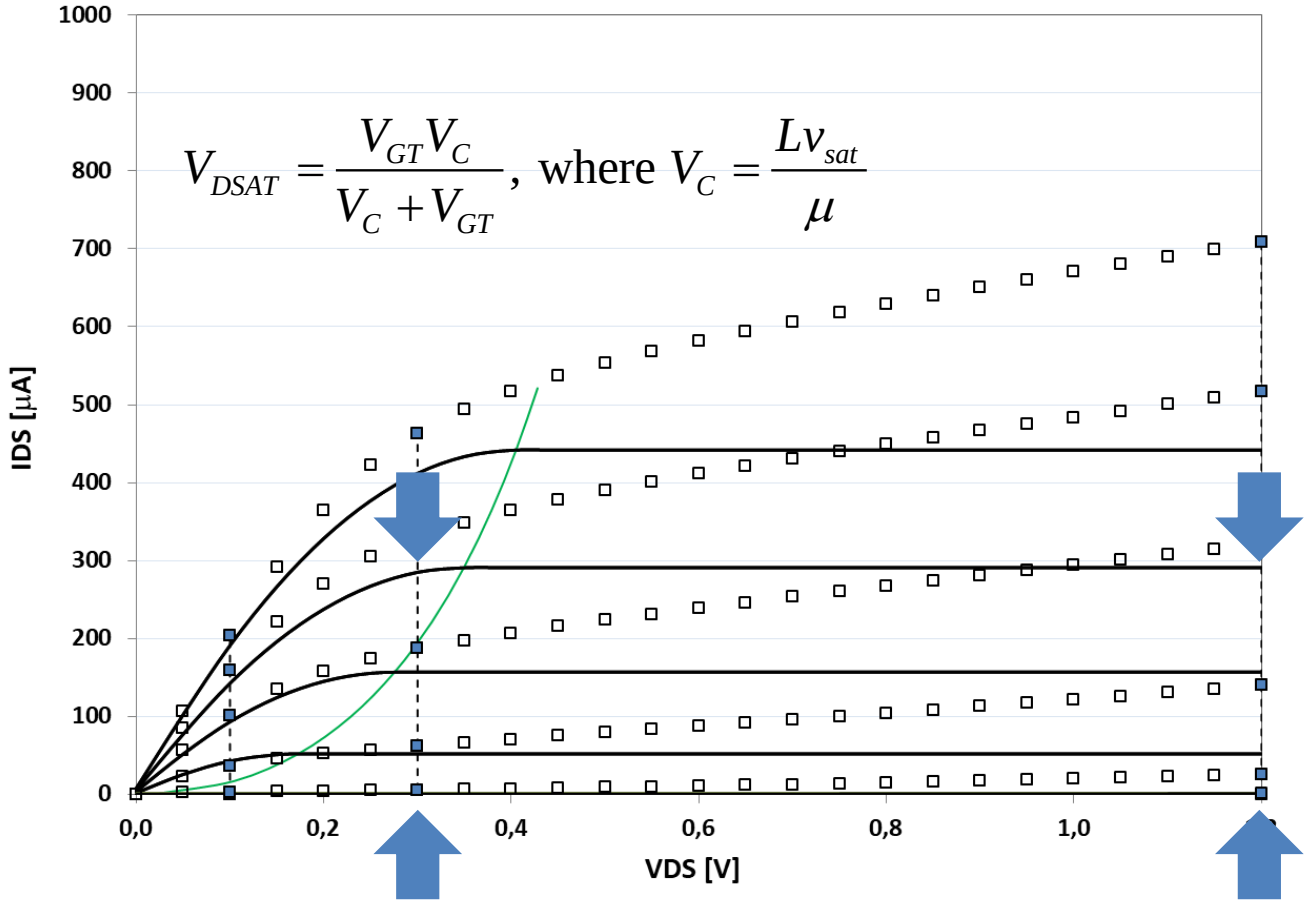


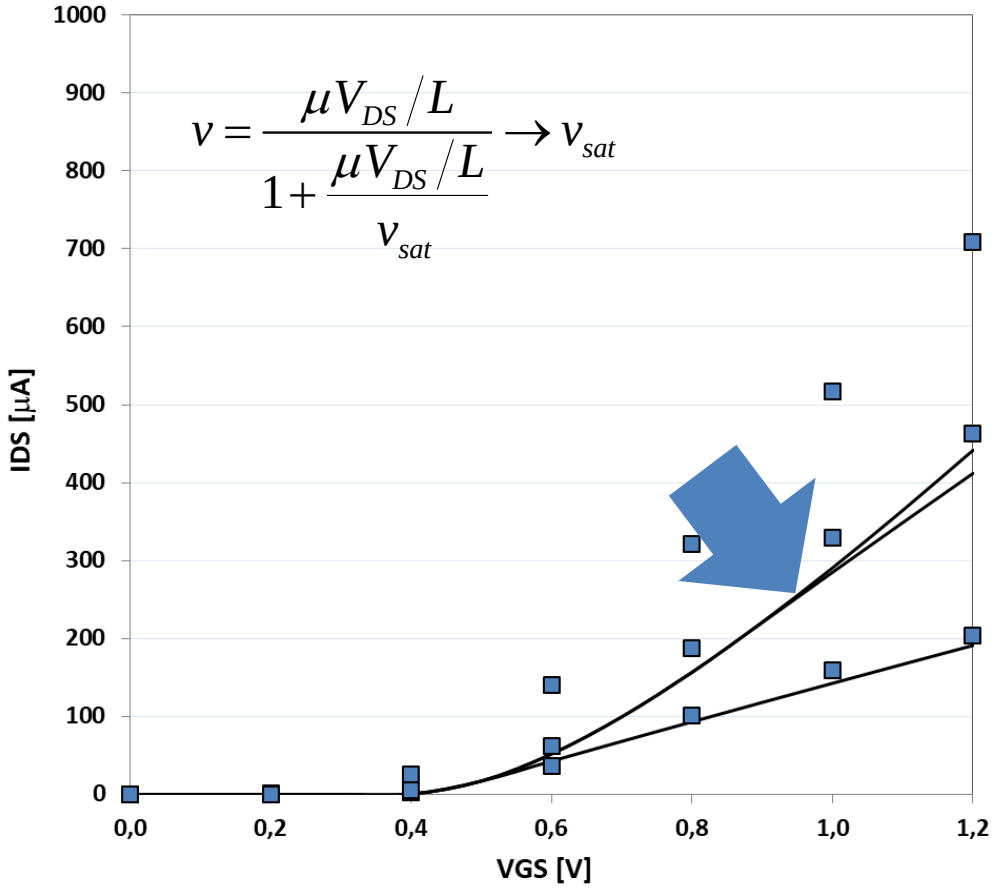
Include mobility roll-off



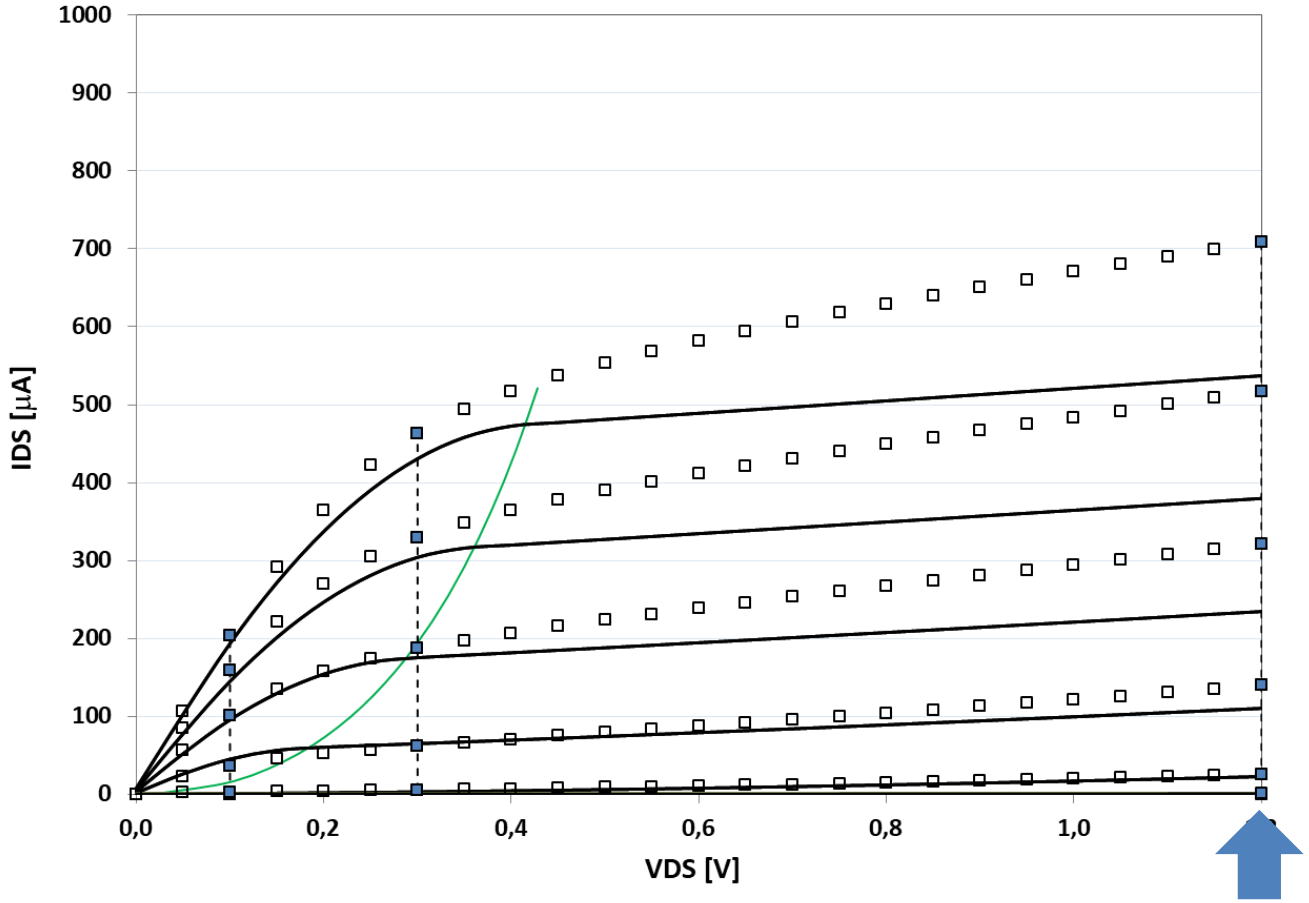


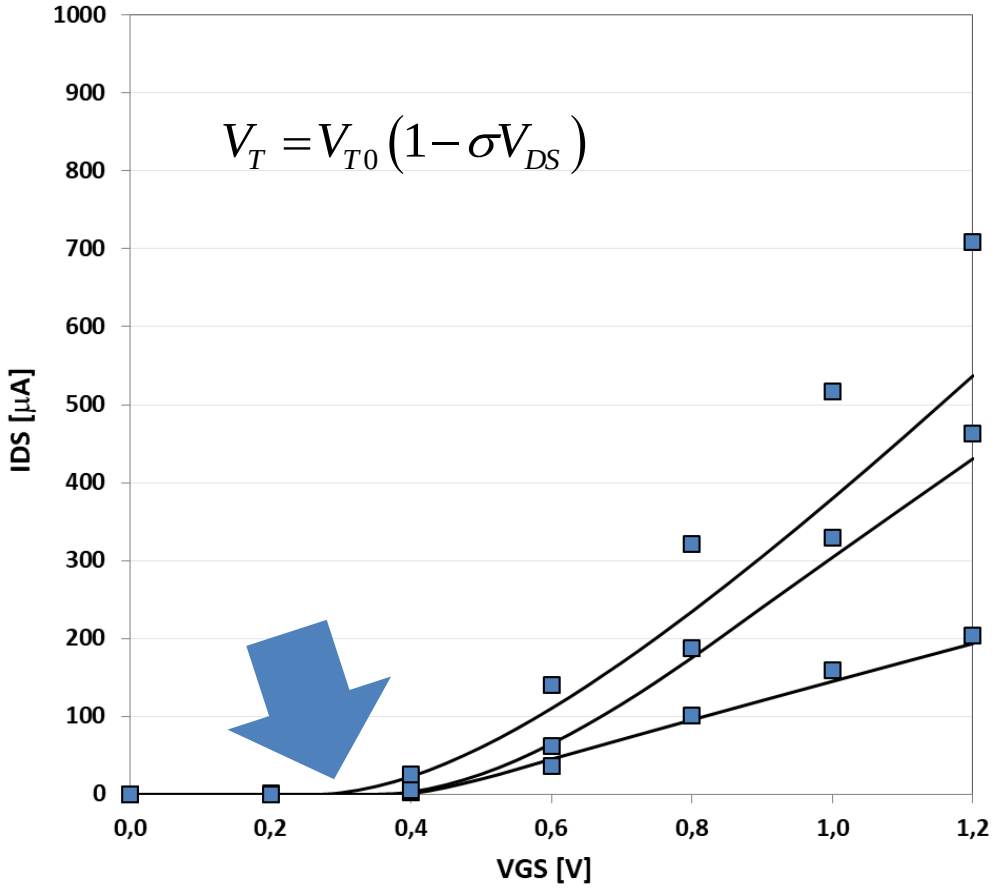
Consider velocity saturation





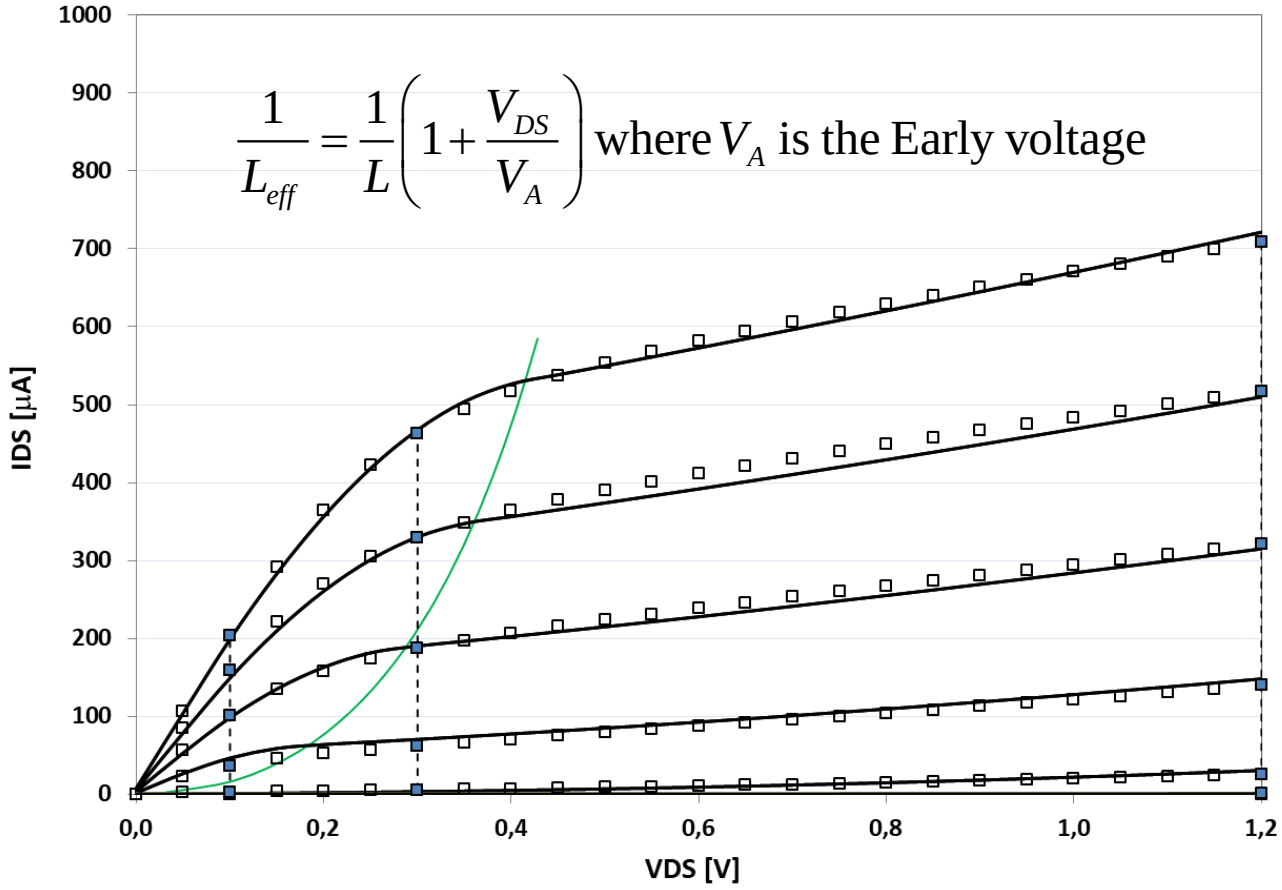
Consider drain-induced barrier-lowering (DIBL)

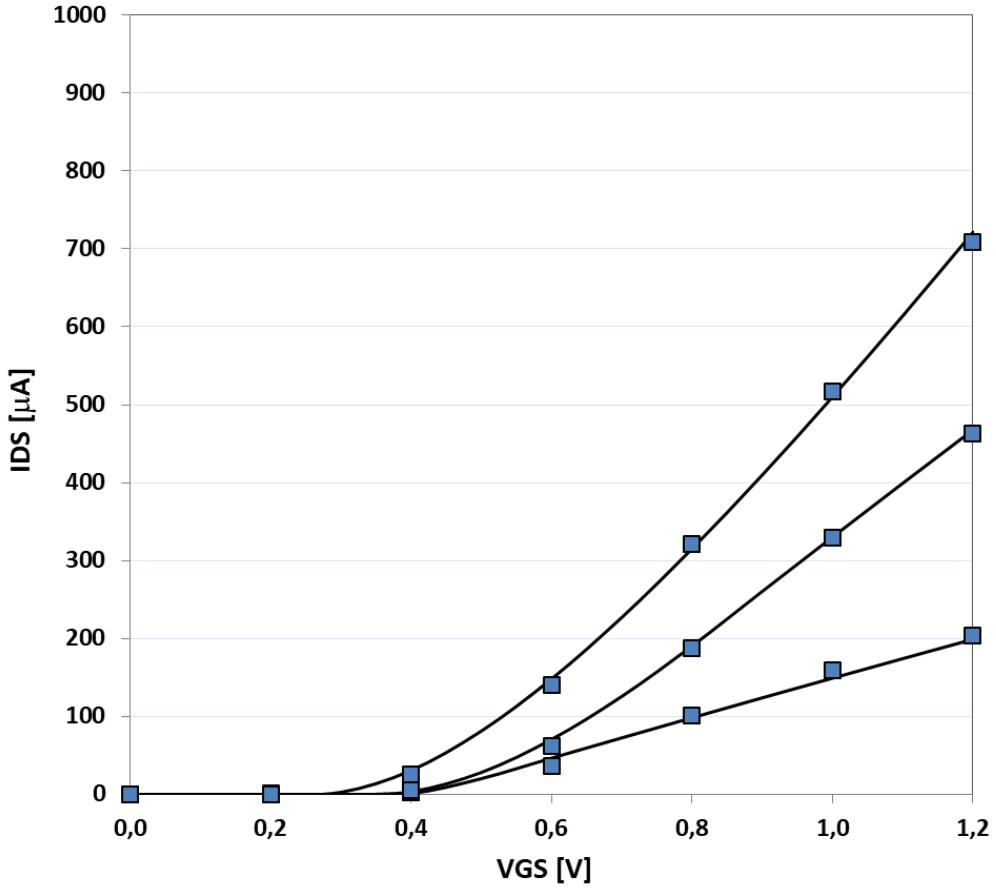




Consider channel length modulation (CLM)

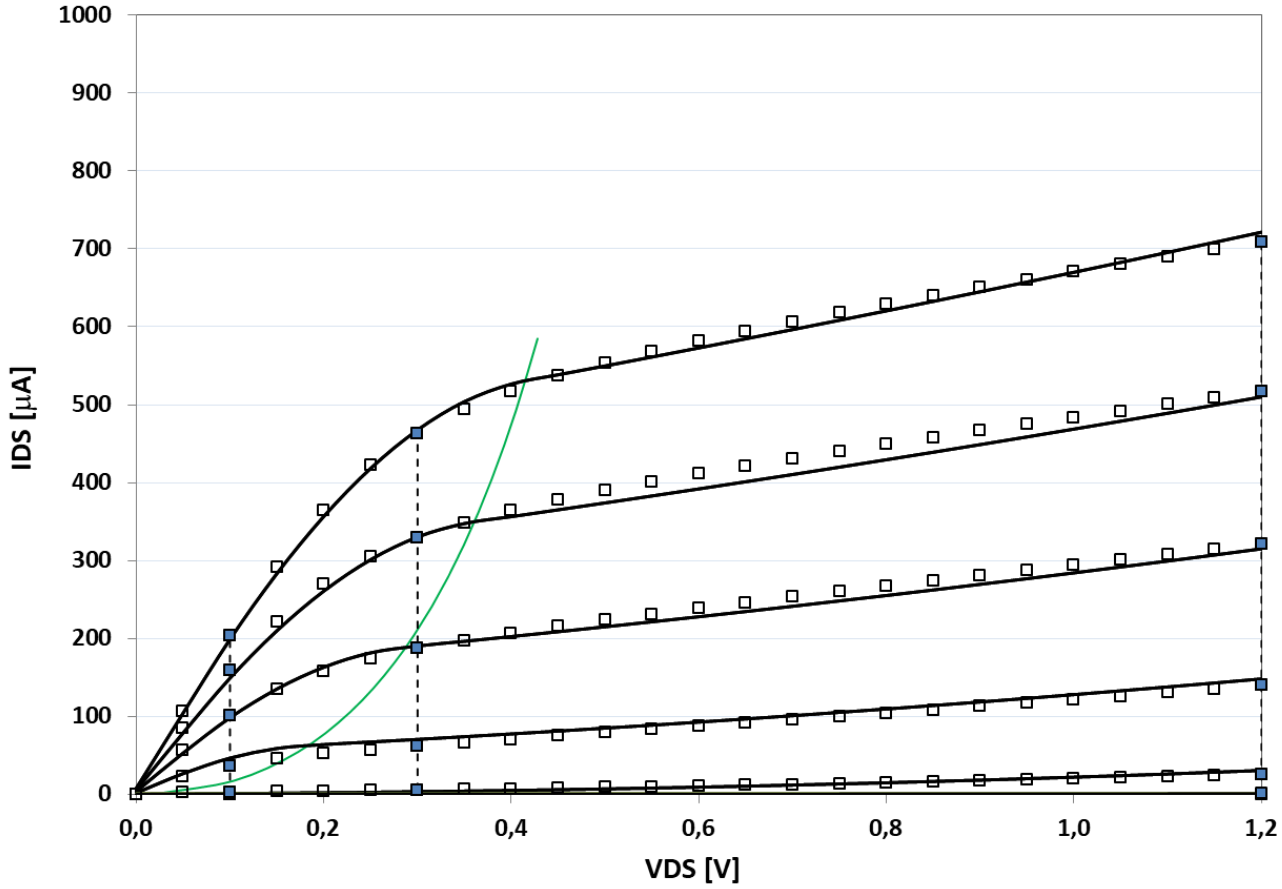
$$\frac{1}{L_{eff}} = \frac{1}{L}\left(1 + \frac{V_{DS}}{V_A}\right) \text{ where } V_A \text{ is the Early voltage}$$

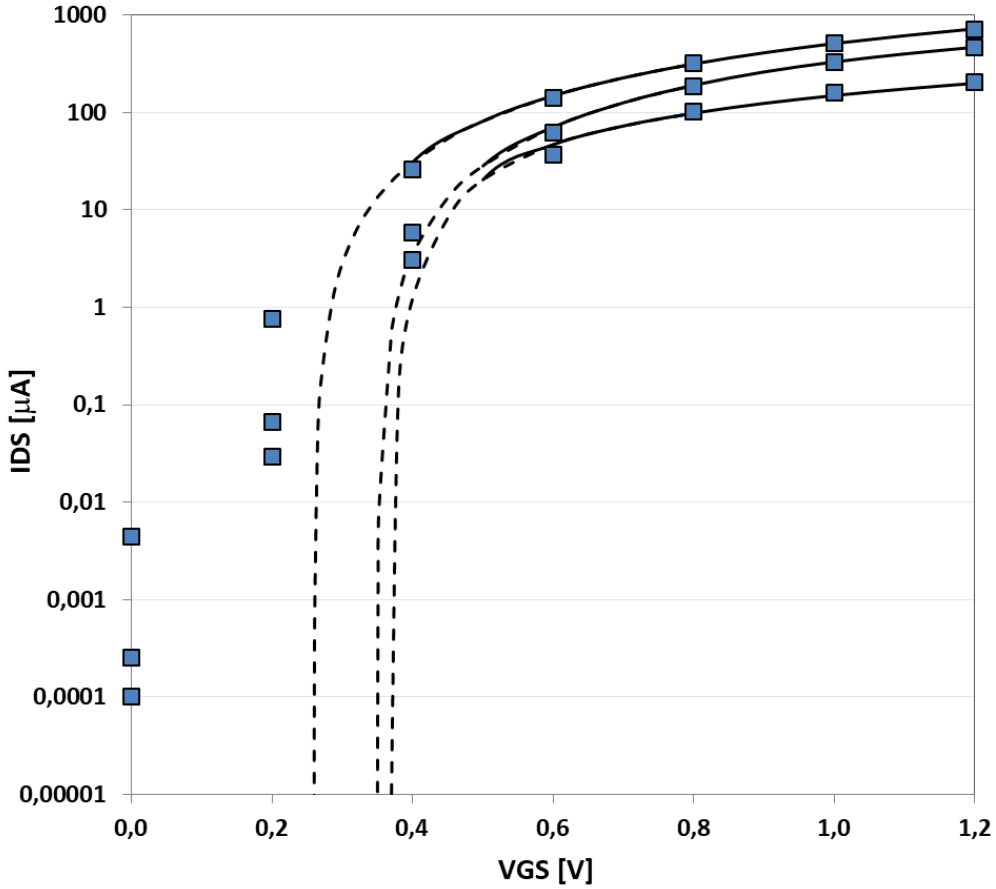




Subthreshold leakage

Replot transfer characteristic on a semilogarithmic scale!





Subthreshold leakage

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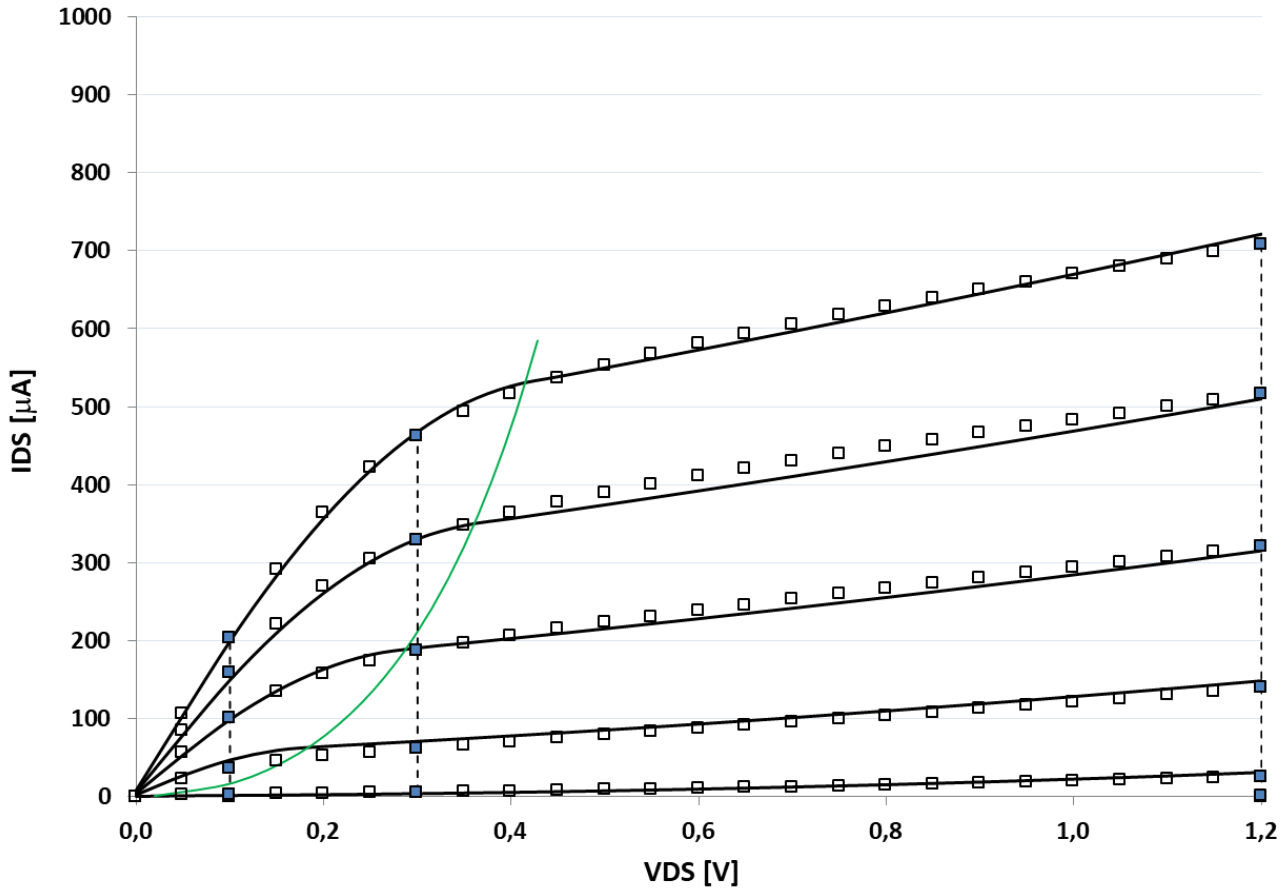

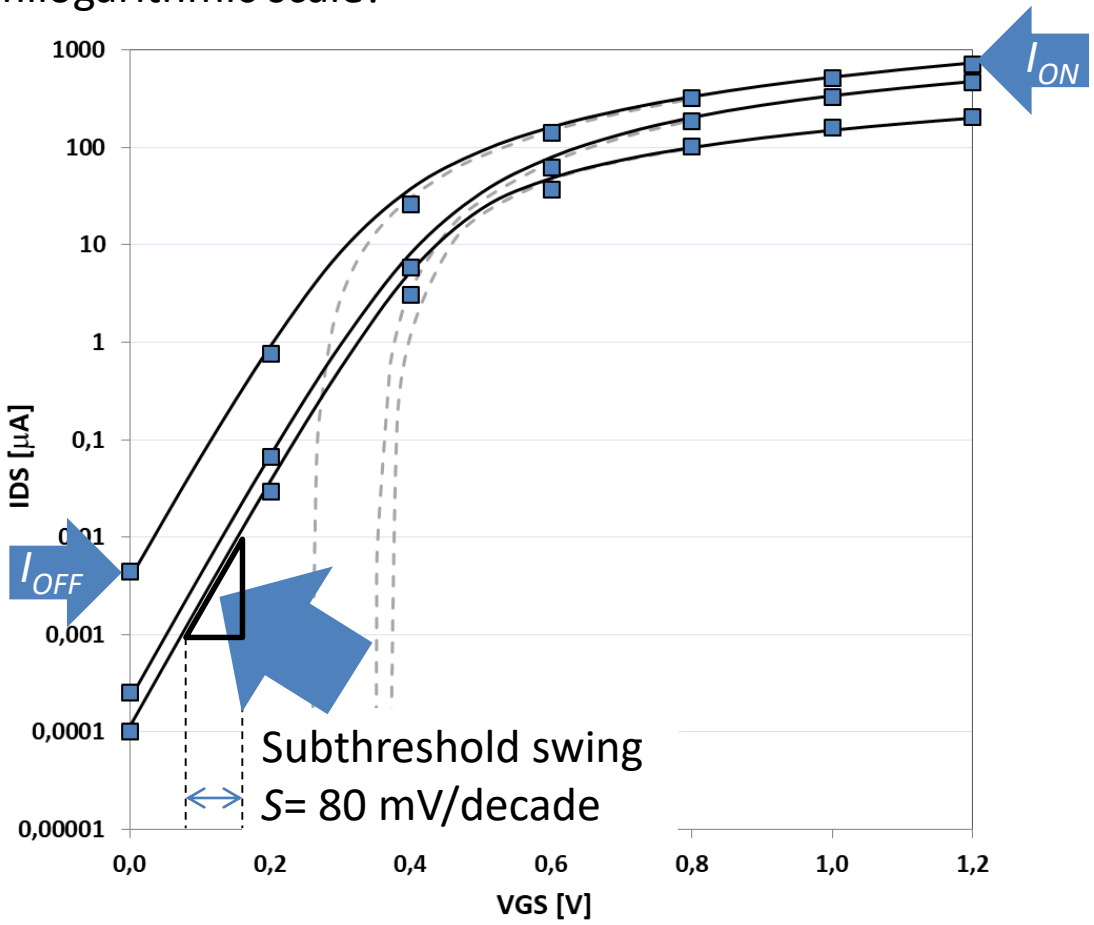

Conclusion

In this lecture, we started considering MOSFET static properties

- Three regions of operation
  - Two ON regions: linear or saturated
  - One OFF region: subthreshold

In second half of lecture we also considered dynamic properties

- The intrinsic gate capacitance
- The extrinsic, or parasitic drain capacitance

We came up with a two-port model including both static circuit elements (resistor or current-source), and dynamic elements, i.e. capacitances!