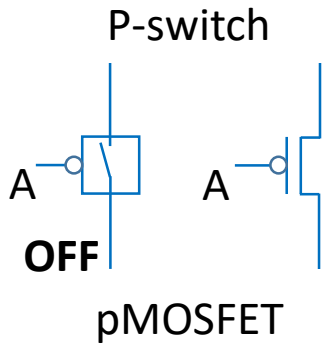
Lecture 16

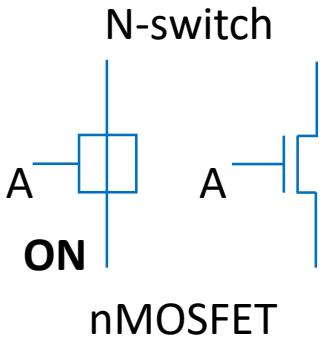
Introduction to Integrated Circuit Design

Course summary

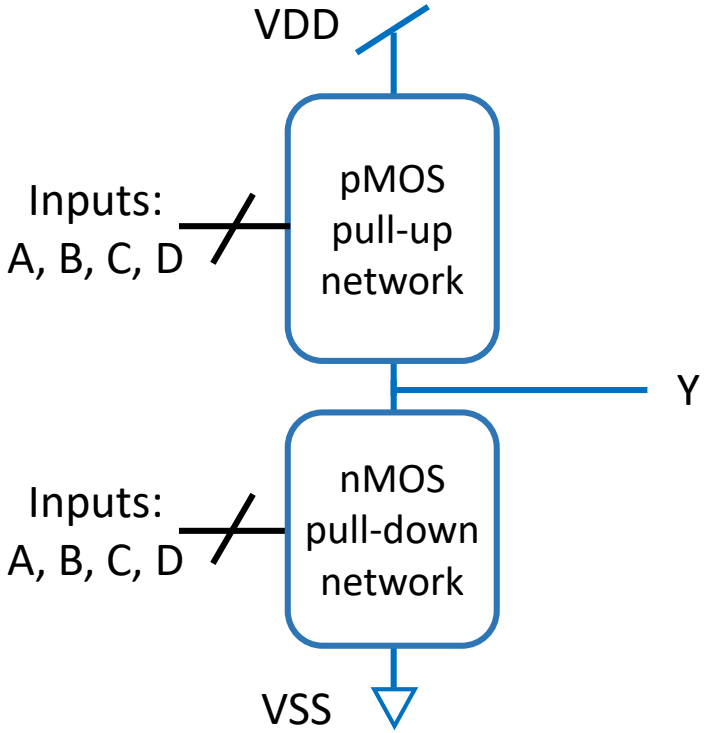
Designing gates with switches

Already the first lecture we learnt how to design gates with switches and in CMOS there are two complementary switches

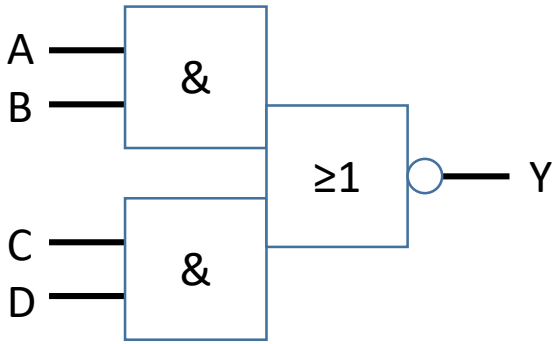




input A is HIGH



$$Y = \overline{AB + CD}$$



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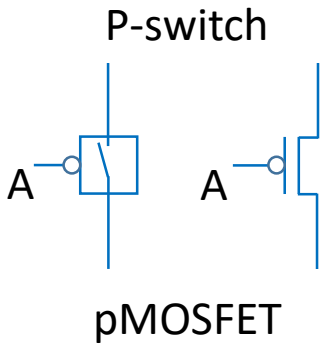
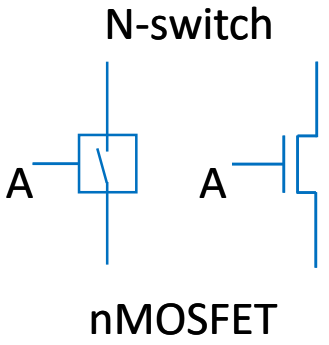
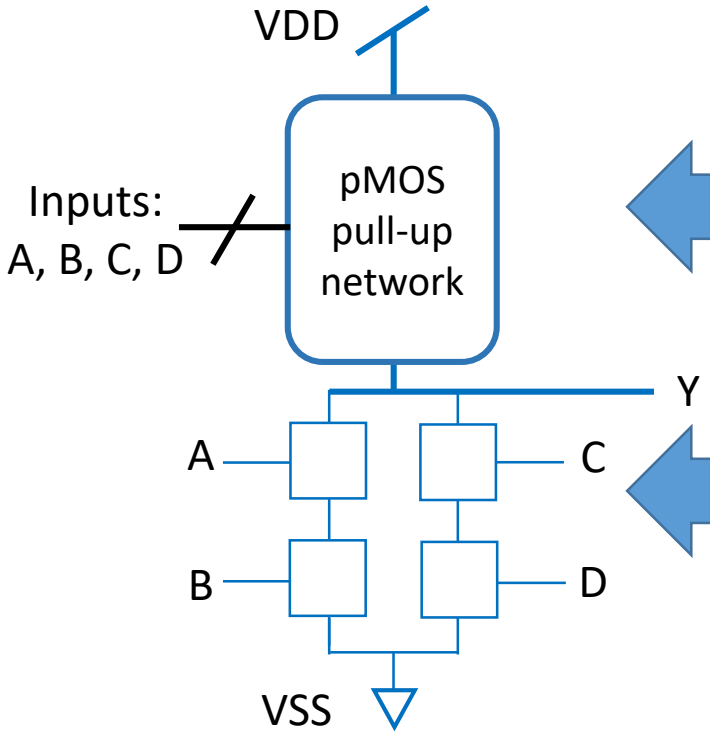


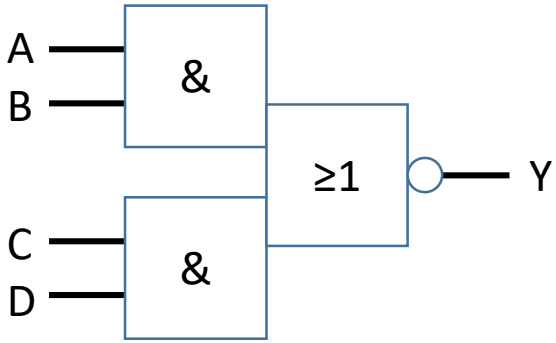




According to de Morgan´s theorem

$$Y = \left(\overline{A} + \overline{B}\right)\left(\overline{C} + \overline{D}\right)$$

$$Y = \overline{AB + CD}$$



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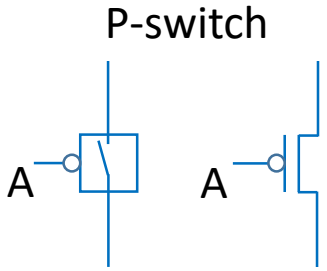

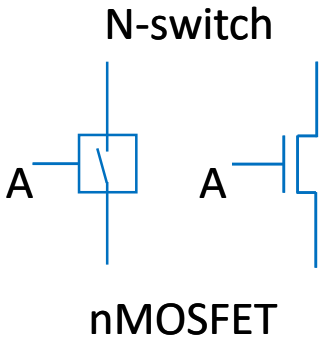

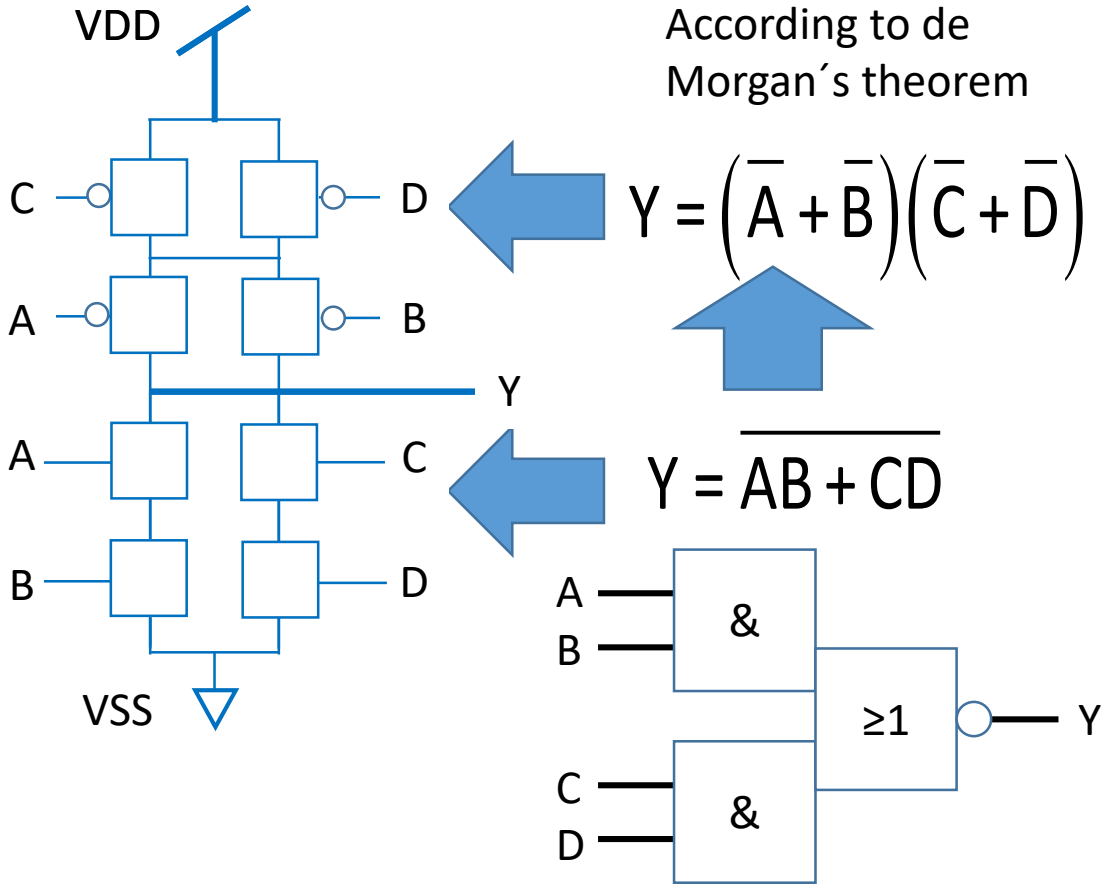

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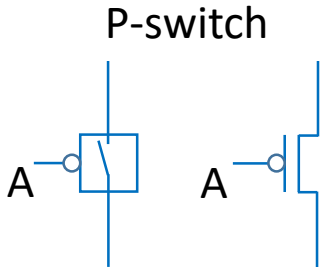

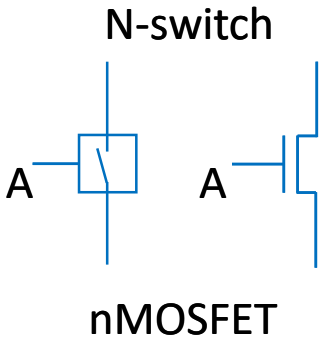

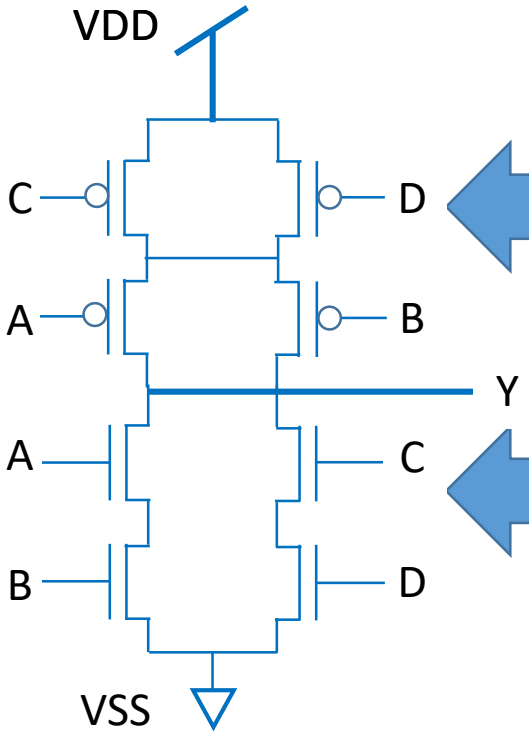

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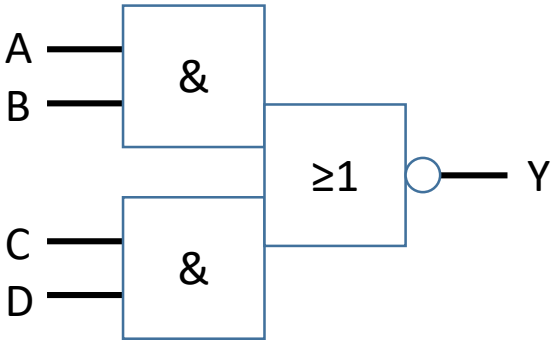
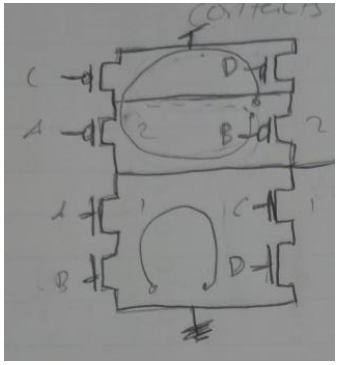
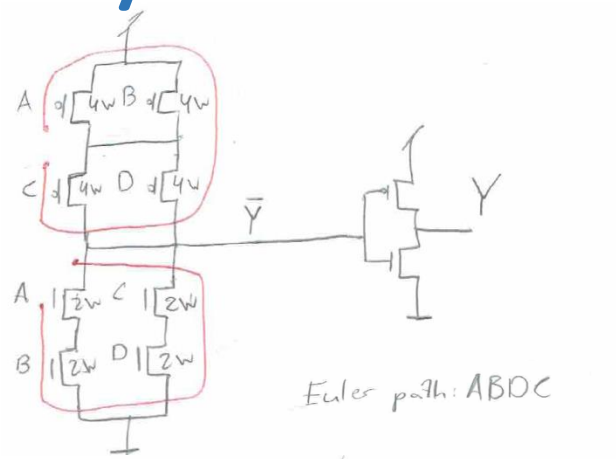
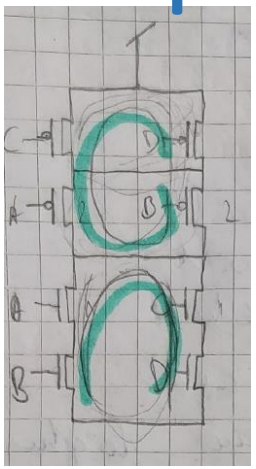
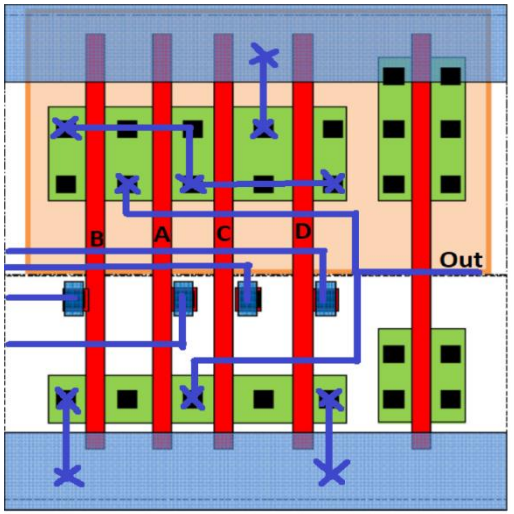


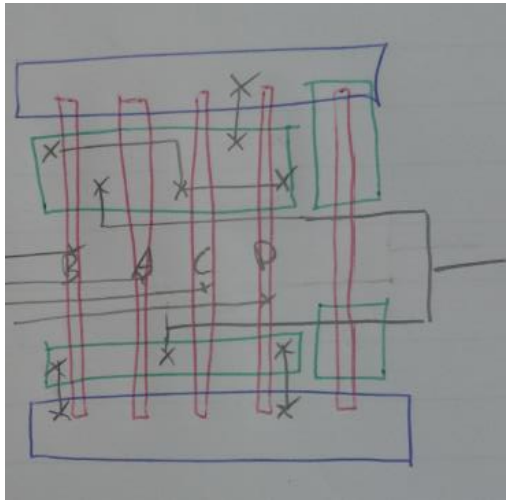
Layout and Euler paths

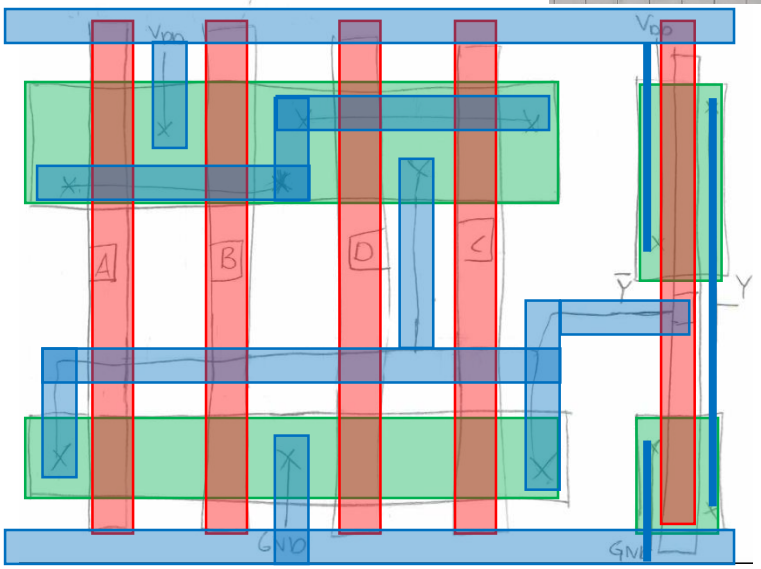


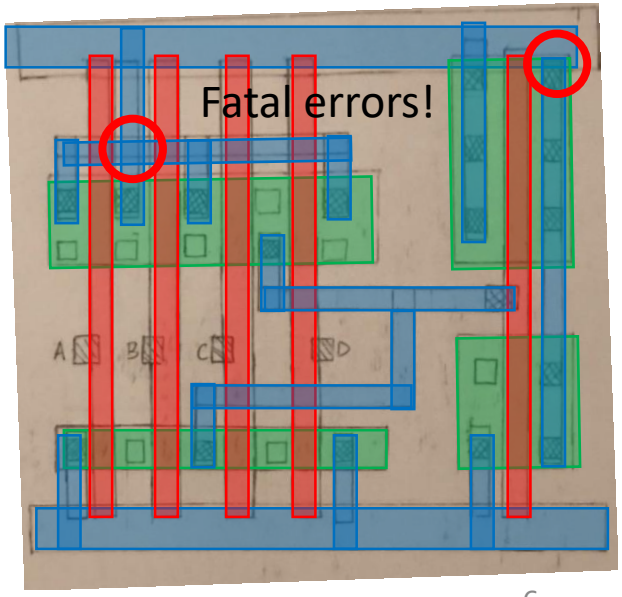








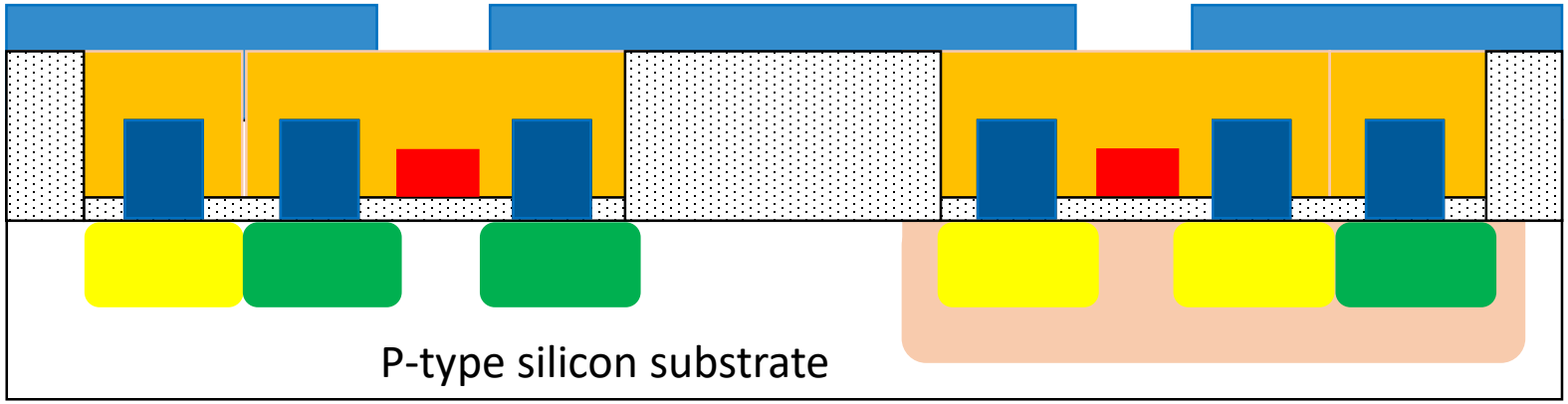


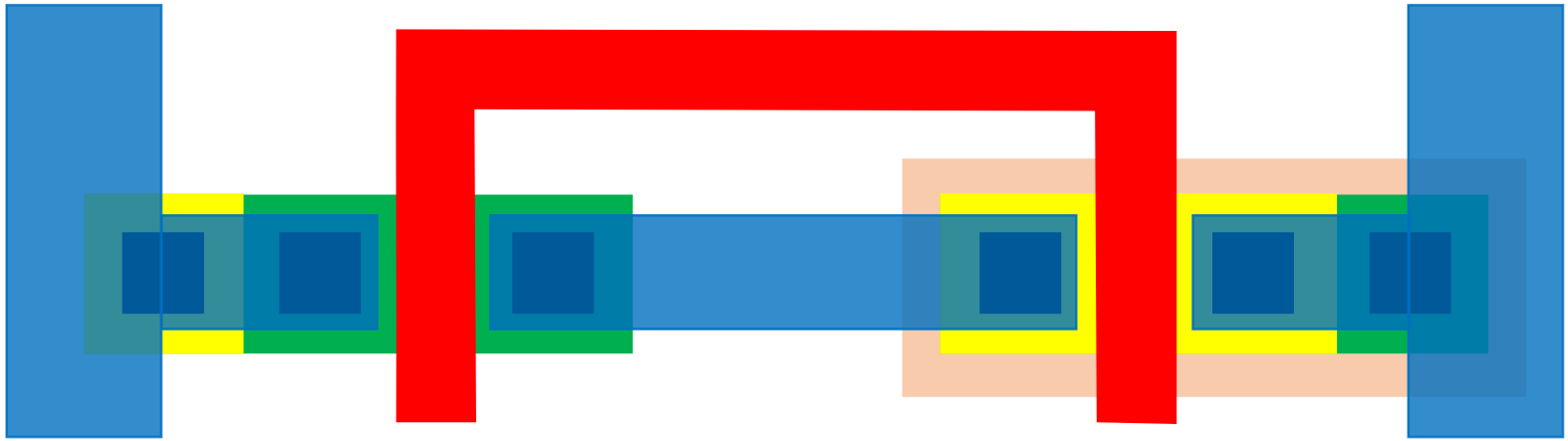


Fabrication

- Chips are built in huge factories called fabs
- Contain clean rooms as large as football fields

Inverter mask set and fabrication





P+ select

Contact cuts

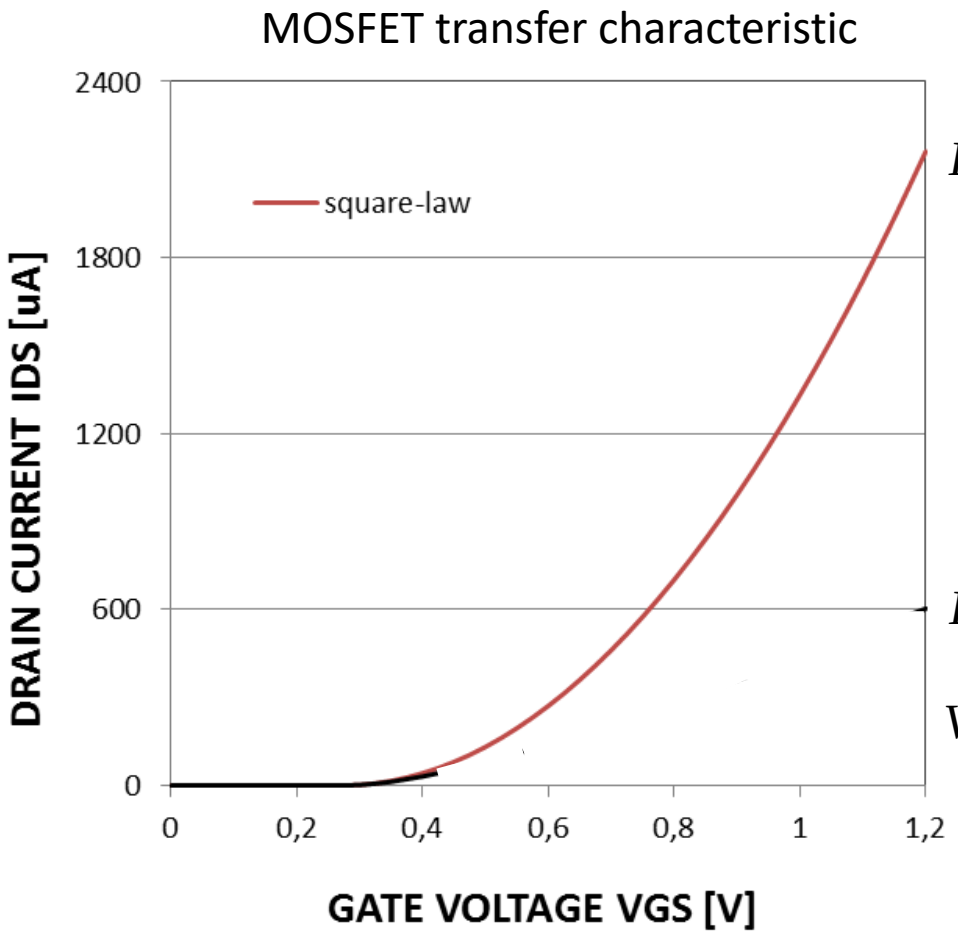
Metal wires

Poly gate

Active areas

N-well

MOSFET – a square-law device



$$I_{DSAT} = \frac{k}{2}(V_{GS} - V_T)^2$$

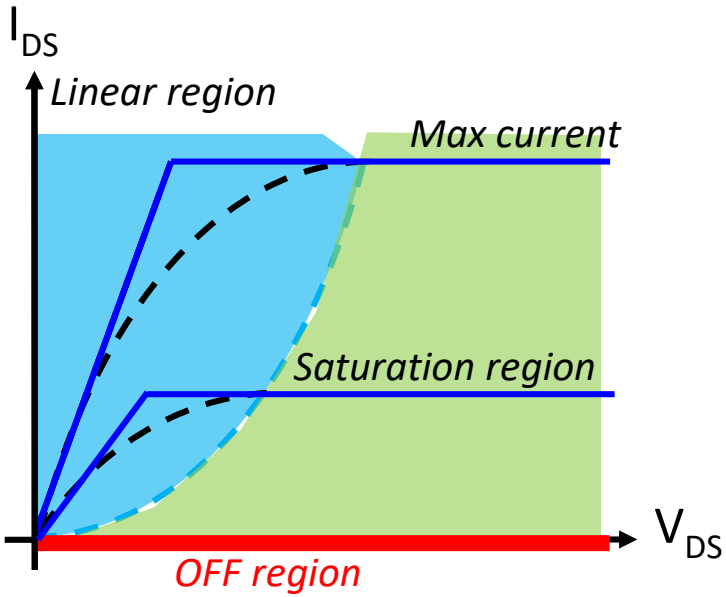
$$V_{DSAT} = V_{GS} - V_T$$

$$I_{DSAT} = \frac{k}{2}(V_{GS} - V_T)V_{DSAT}$$

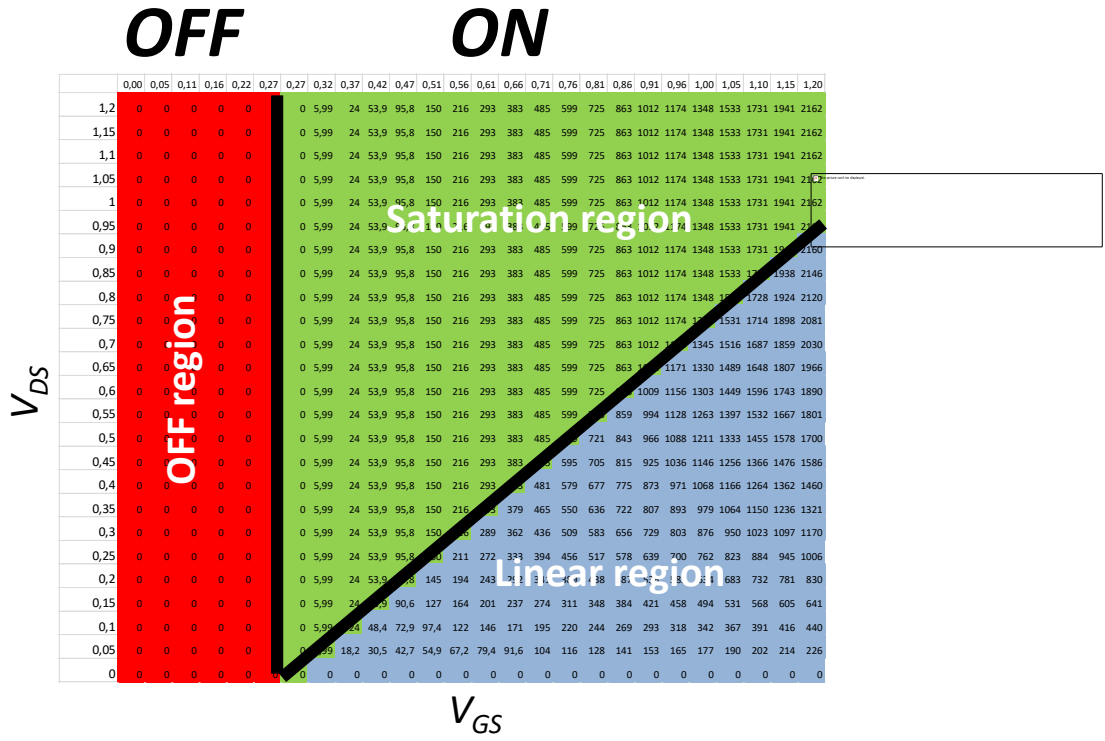
$$V_{DSAT} < V_{GS} - V_T$$

MOSFET models

Models can predict I_{DS} for any V_{GS}/V_{DS}



Output characteristic



CMOS Inverter

Equal saturation currents yields the switching voltage

$$I_{dsp} = \frac{k_P}{2}\left(V_{DD} - V_{IN} + V_{TP}\right)^2$$

$$I_{dsn} = \frac{k_N}{2}\left(V_{IN} - V_{TN}\right)^2$$

$$V_{sw} = V_{TN} + \frac{\Delta V}{1+\sqrt{x}},\ x = \frac{k_N}{k_P}$$

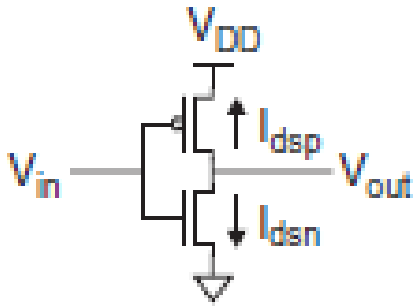
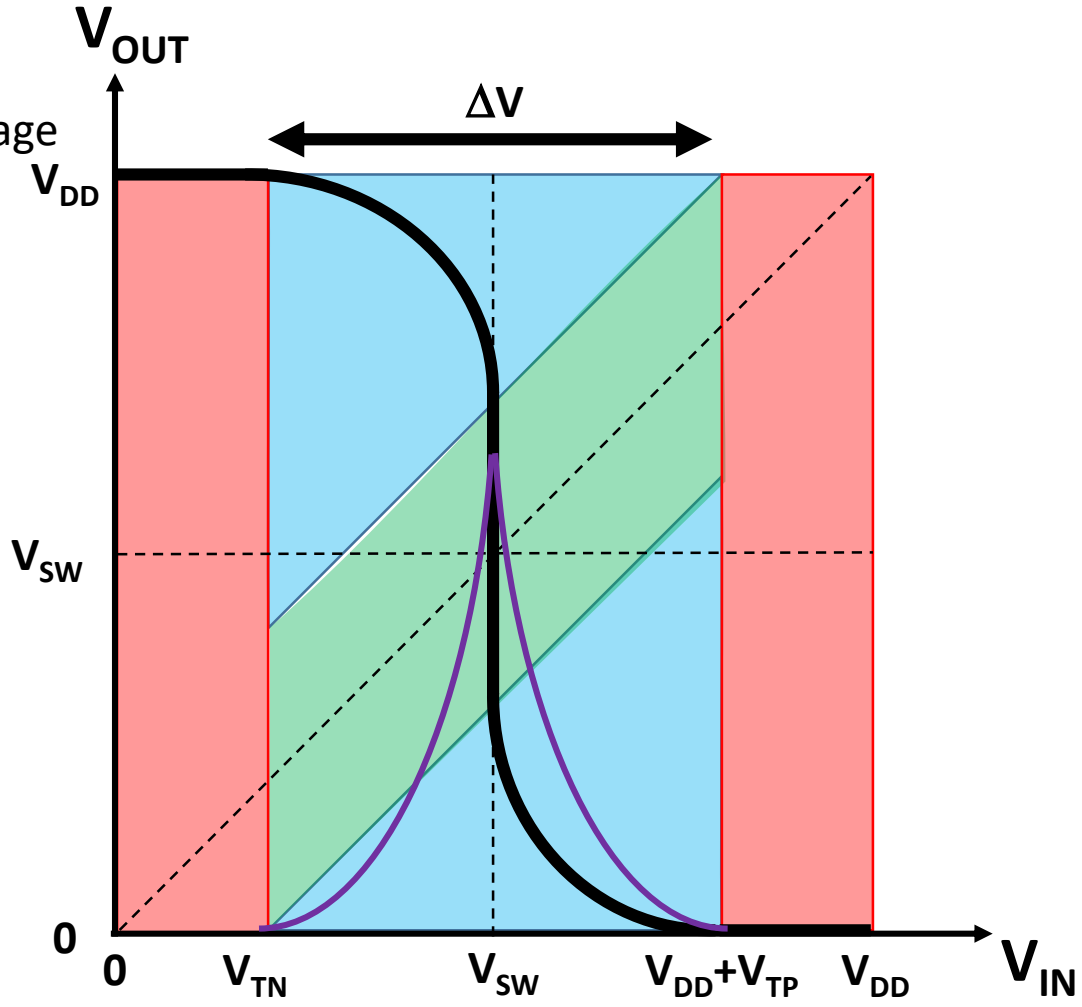


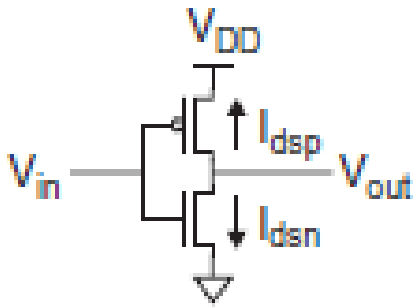
FIGURE 2.25
A CMOS inverter



CMOS Inverter

Simplify and assume $V_{TN}=-V_{TP}=V_{DD}/4$

$$V_{sw} = \frac{1}{4} + \frac{1/2}{2} = \frac{1}{2},\ x = 1$$



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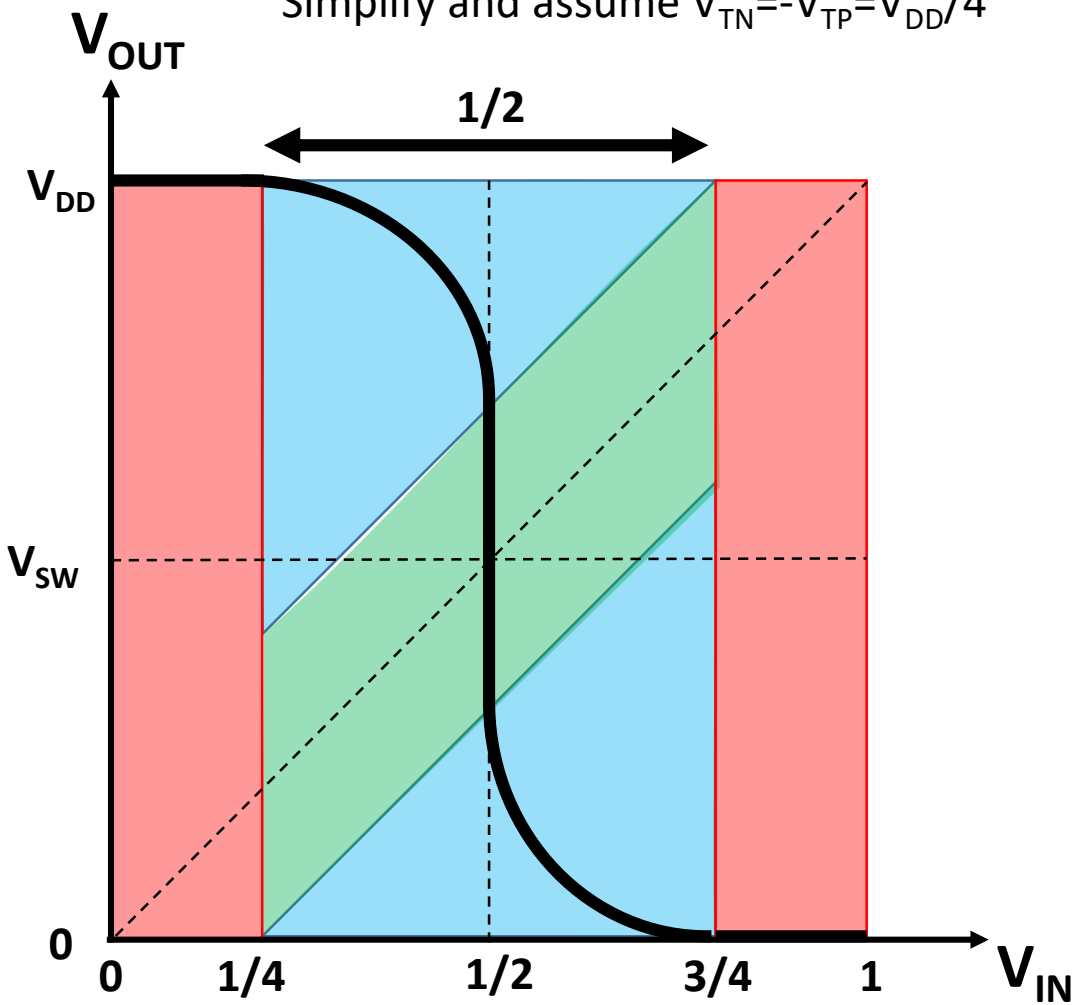
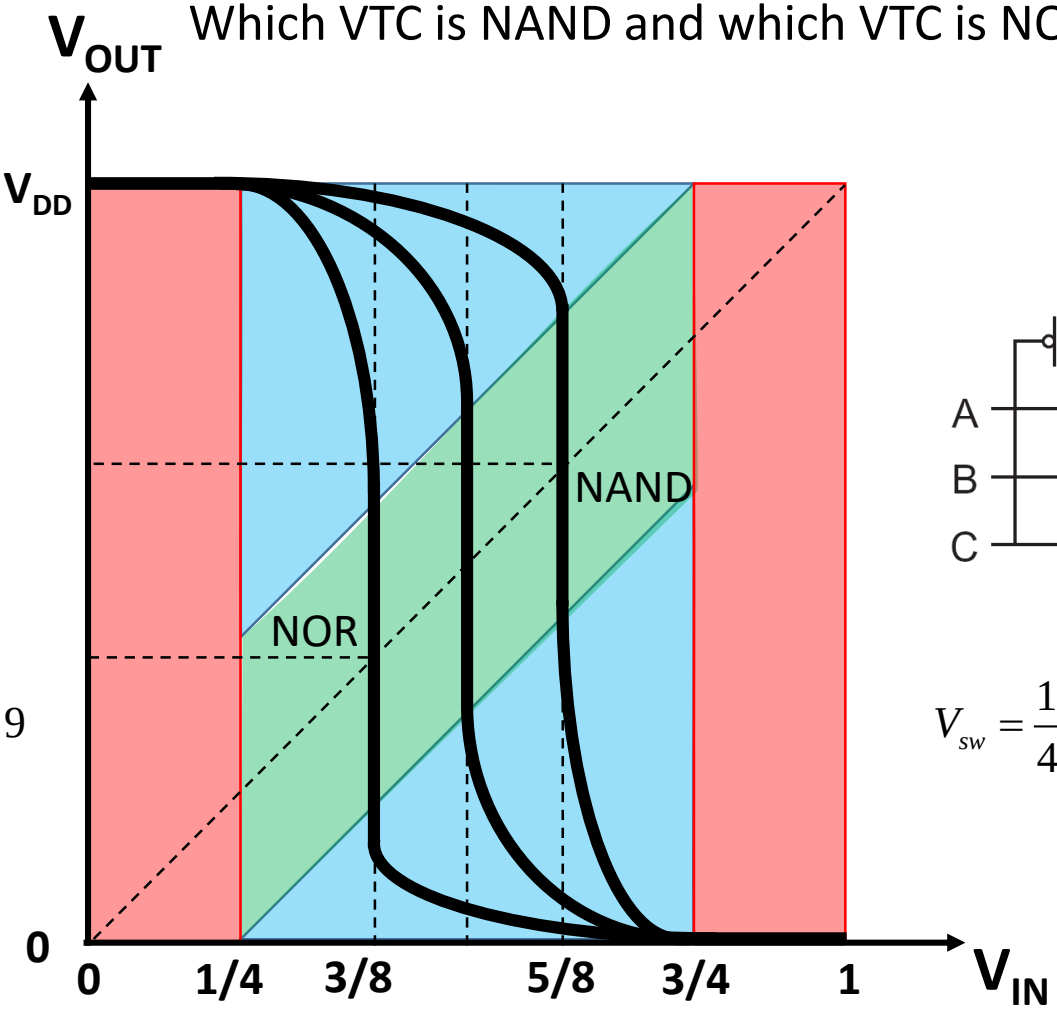
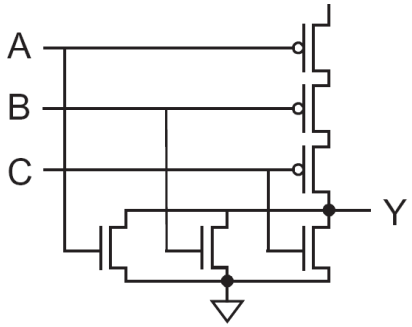


NAND/NOR VTC

Which VTC is NAND and which VTC is NOR?

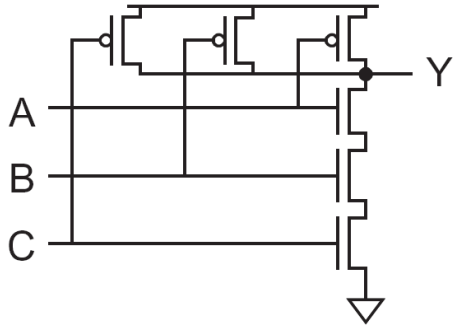


NOR3



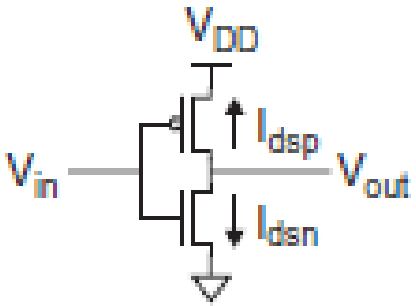
$$V_{sw} = \frac{1}{4} + \frac{1/2}{1+\sqrt{9}} = \frac{3}{8},\ x = 9$$

NAND3



$$V_{sw} = \frac{1}{4} + \frac{1/2}{1+\sqrt{\frac{1}{9}}} = \frac{5}{8},\ x = \frac{1}{9}$$

CMOS Inverter – Noise margins



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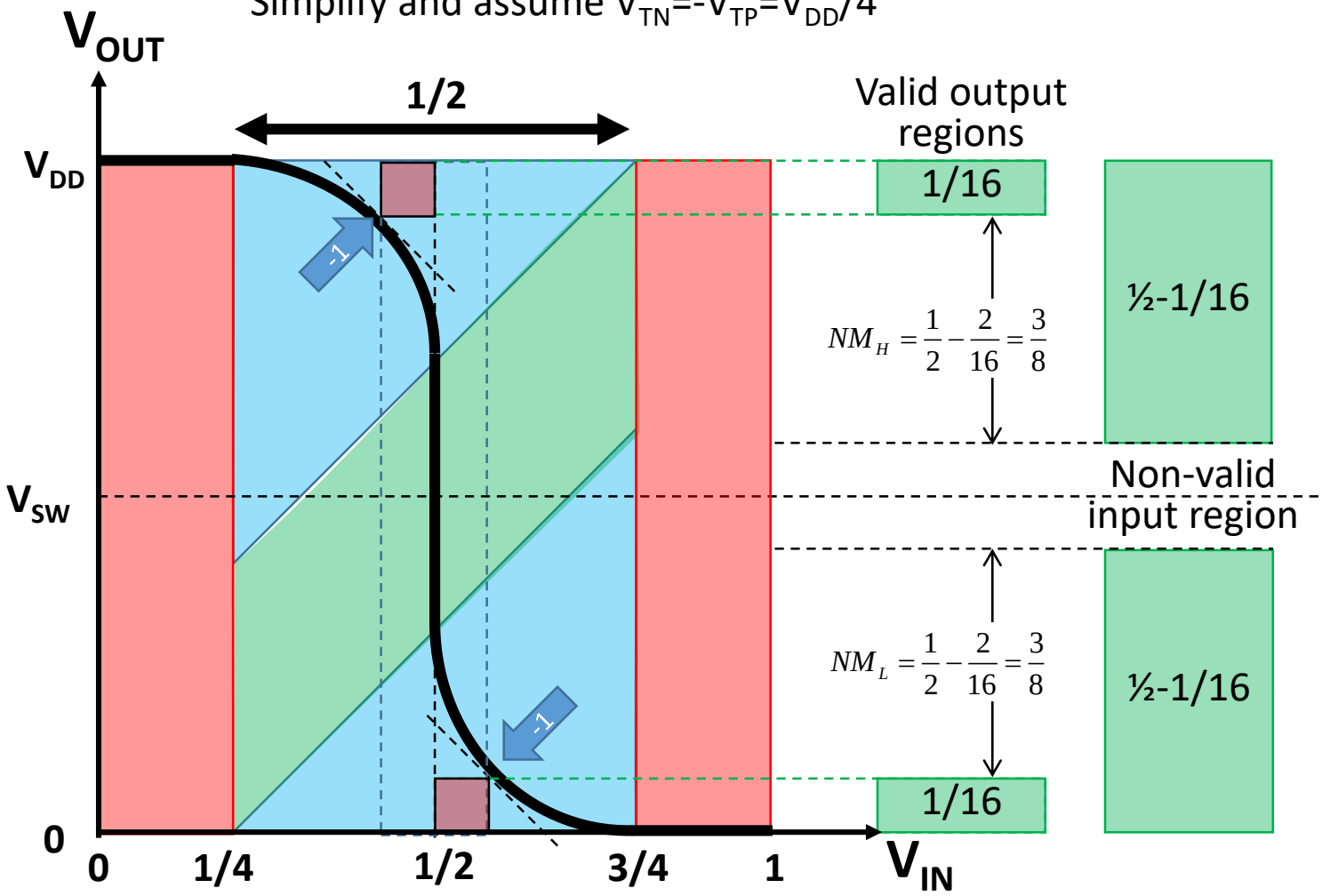
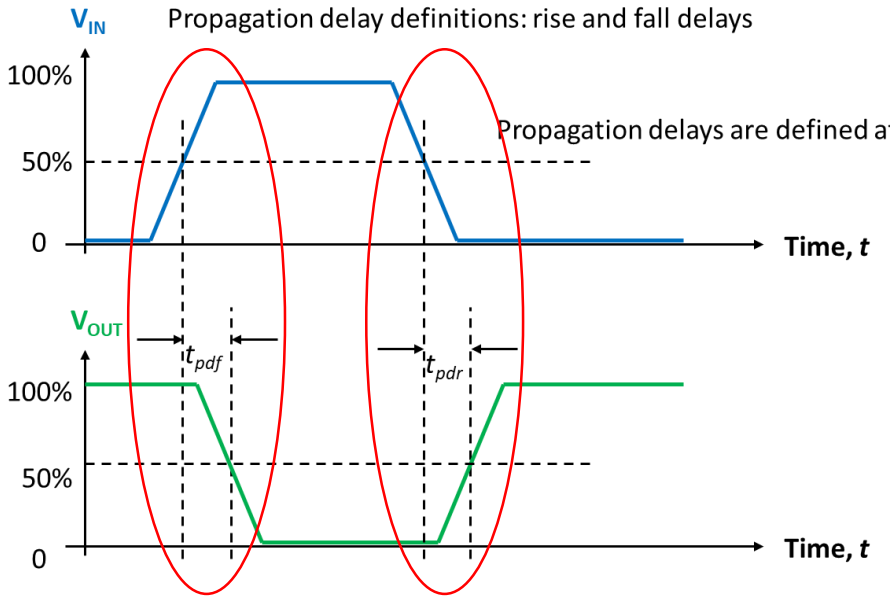
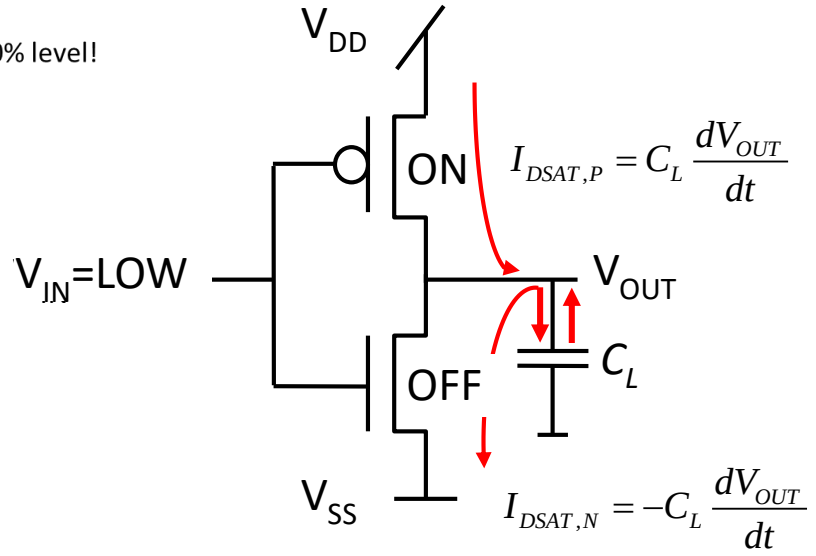
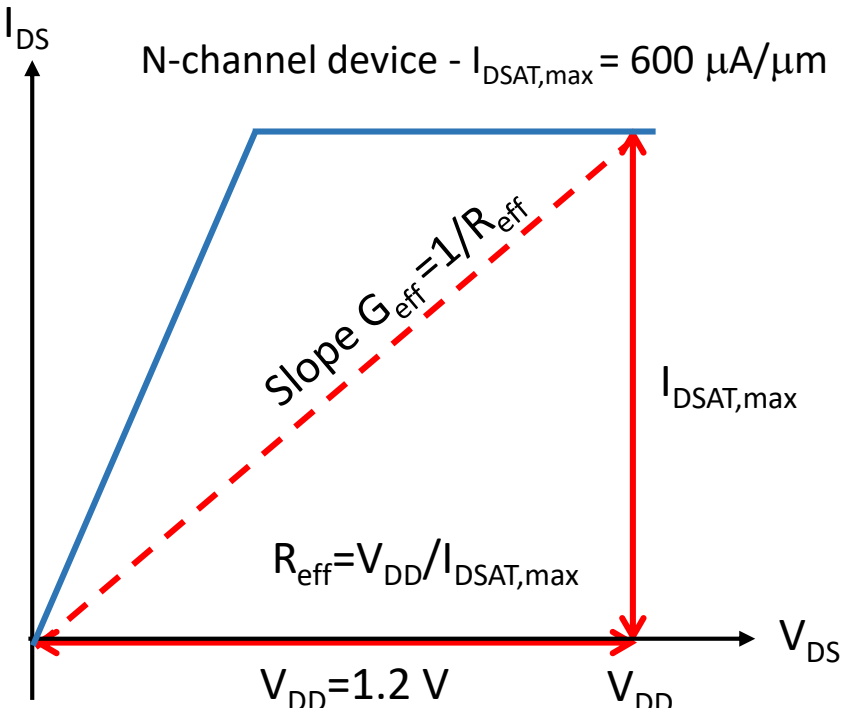


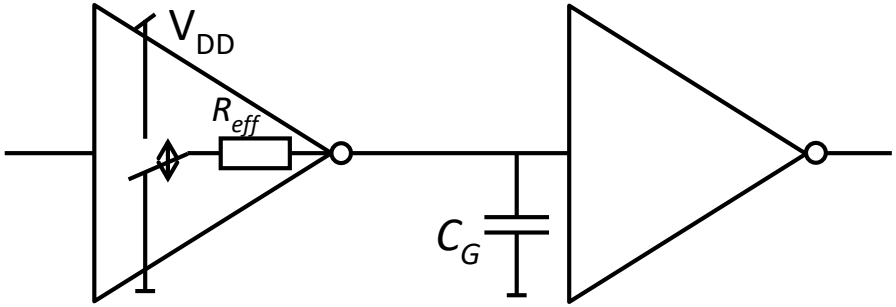
Switching the inverter





Defining the effective resistance . . .

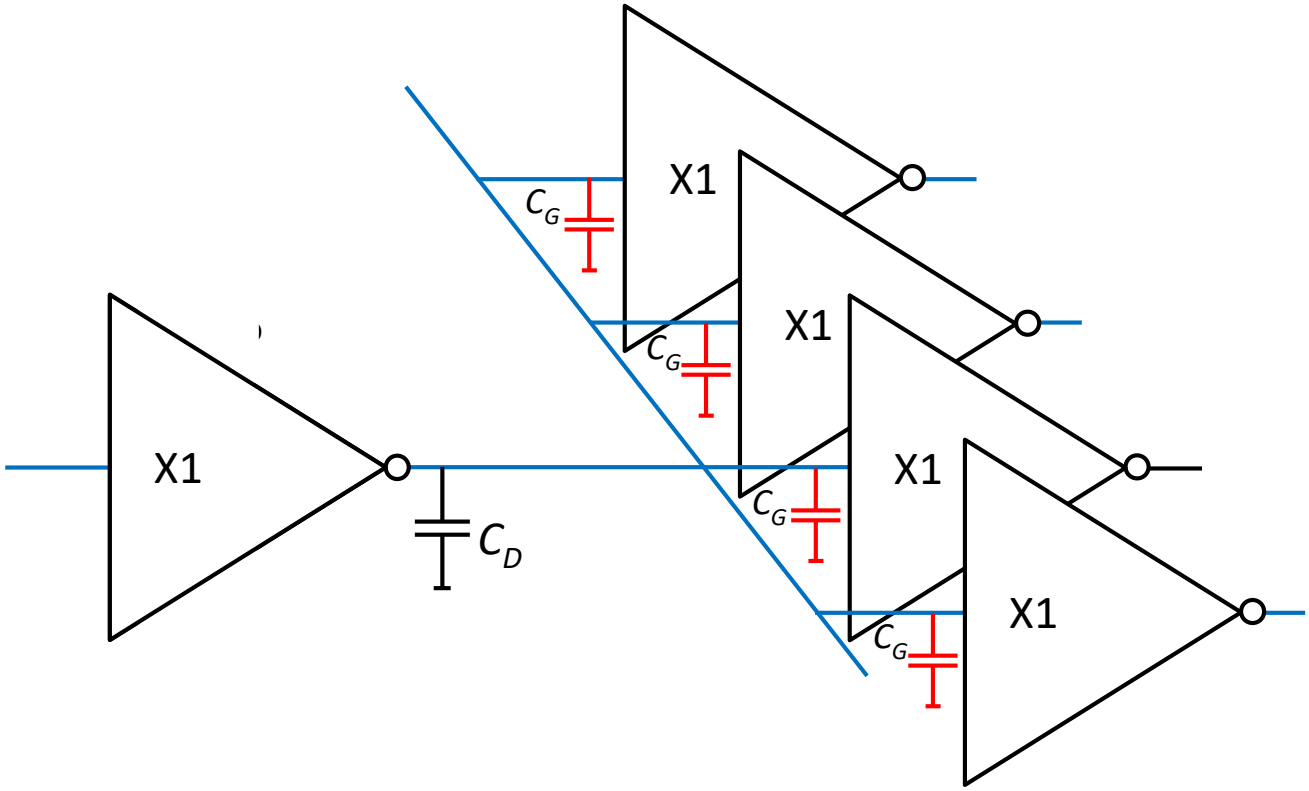




Defining the ideal, non-parasitic delay
tau = $0.7R_{eff}C_G$= 5 ps in 65 nm CMOS

. . . and reference delay tau

FO4 delay

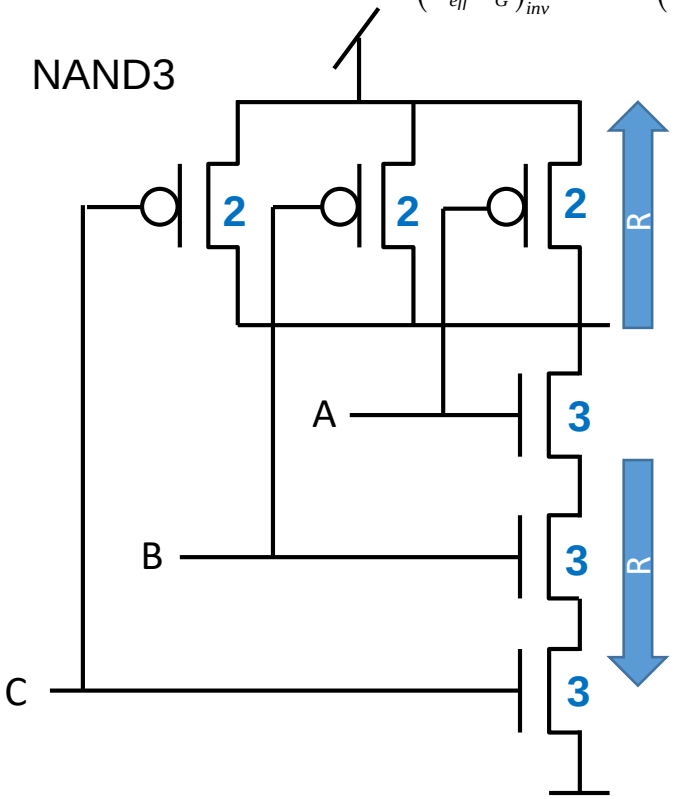


The FO4 propagation delay becomes $t_{pd} = 0.7R_{eff}\left(C_D + 4C_G\right) = \underbrace{0.7R_{eff}C_G}_{\tau au}\left(p_{inv} + 4\right) = 5\text{ ps} \times 5 = 25\text{ ps}$

Defining logical effort

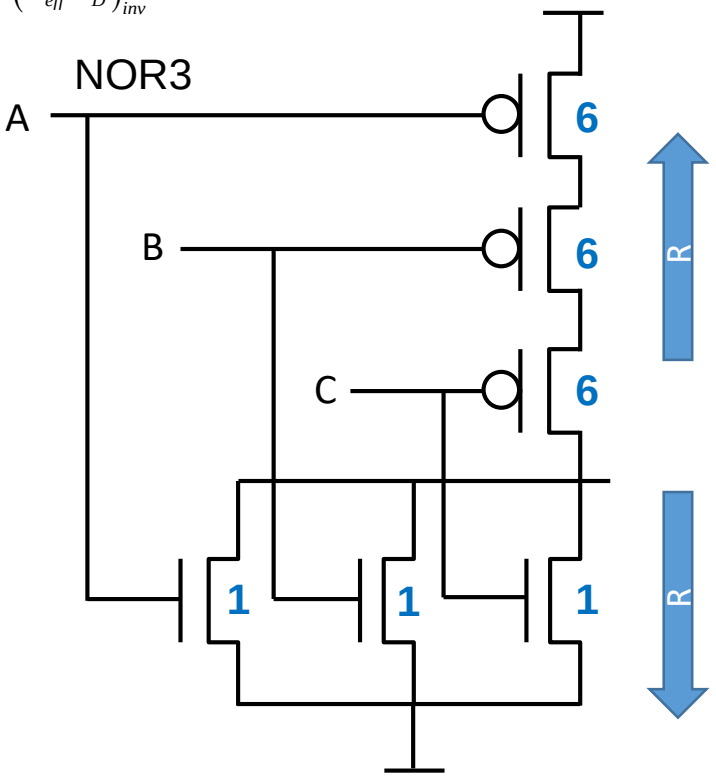
$$g = \frac{\left(R_{eff} C_{IN}\right)_{gate}}{\left(R_{eff} C_G\right)_{inv}} \qquad p = \frac{\left(R_{eff} C_D\right)_{gate}}{\left(R_{eff} C_G\right)_{inv}} = p_{inv} \frac{\left(R_{eff} C_D\right)_{gate}}{\left(R_{eff} C_D\right)_{inv}}$$

NAND3



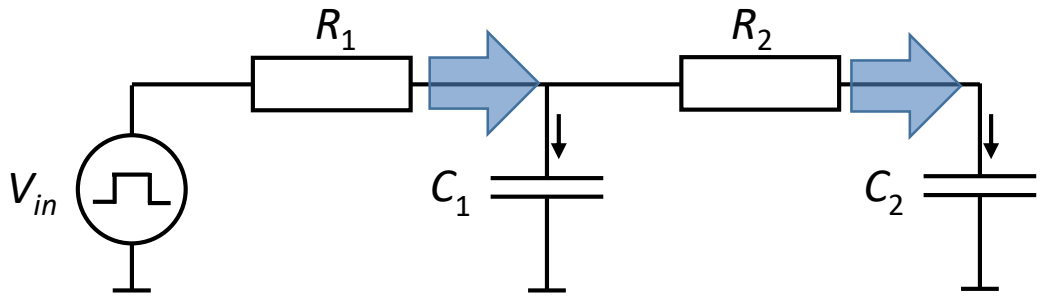
$$g = \frac{R_{eff} 5C}{R_{eff} 3C} = \frac{5}{3} \qquad p = \frac{R_{eff} 9C_D}{R_{eff} 3C} = 3p_{inv}$$

NOR3



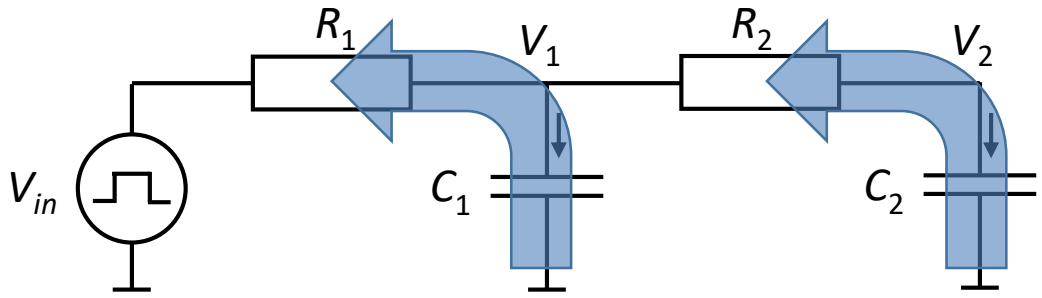
$$g = \frac{R_{eff} 7C}{R_{eff} 3C} = \frac{7}{3} \qquad p = \frac{R_{eff} 9C_D}{R_{eff} 3C} = 3p_{inv}$$

Wire delay



Each resistance is multiplied by its downstream capacitance!

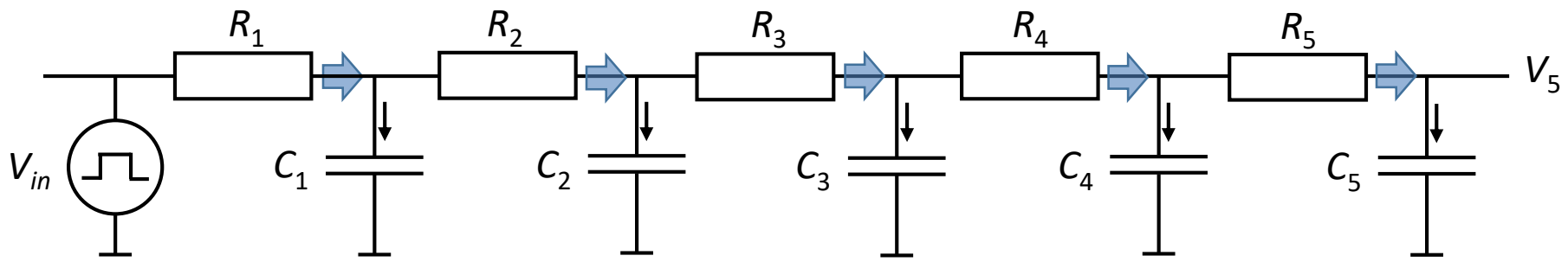
$$T_E = R_1\left(C_1 + C_2\right) + R_2 C_2$$



Or: Each capacitance is multiplied by its upstream capacitance!

$$T_E = R_1 C_1 + \left(R_1 + R_2\right) C_2$$

Elmore delay model



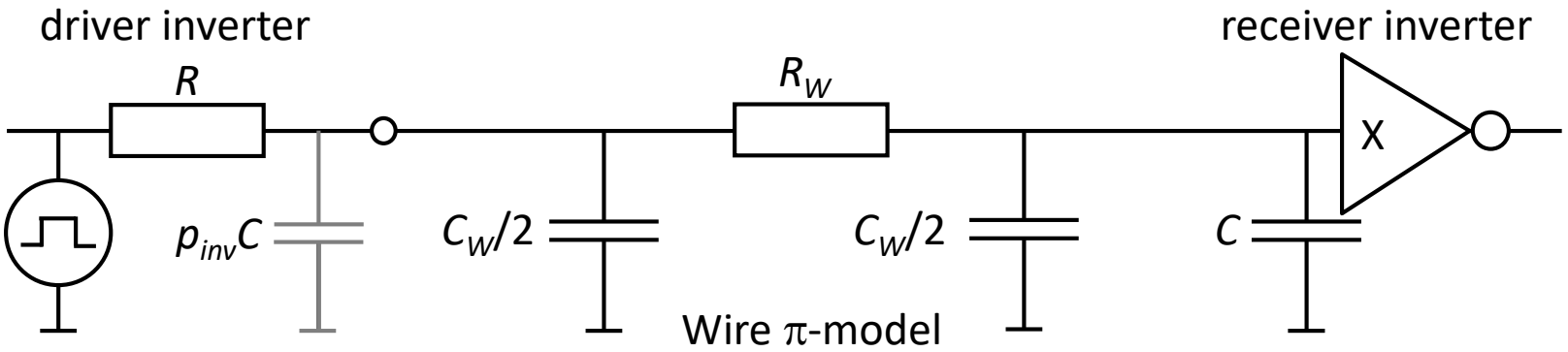
Estimate the propagation delay through the RC ladder knowing that the output voltage is given by

$$V_5 = V_{50} + V_{51}e^{-t/\tau_1} + V_{52}e^{-t/\tau_2} + V_{53}e^{-t/\tau_3} + V_{54}e^{-t/\tau_4} + V_{55}e^{-t/\tau_5}$$

and realizing that we cannot determine any of the parameters involved analytically!
Hence, we use the Elmore delay model based on the assumption that one of the five time constants is dominant!
If so, the dominant time constant T_E (after W. C. Elmore) can be obtained by multiplying each of the resistances with its downstream capacitance!

$$T_E = R_1\left(C_1 + C_2 + C_3 + C_4 + C_5\right) + R_2\left(C_2 + C_3 + C_4 + C_5\right) + R_3\left(C_3 + C_4 + C_5\right) + R_4\left(C_4 + C_5\right) + R_5C_5$$

Sizing the driver



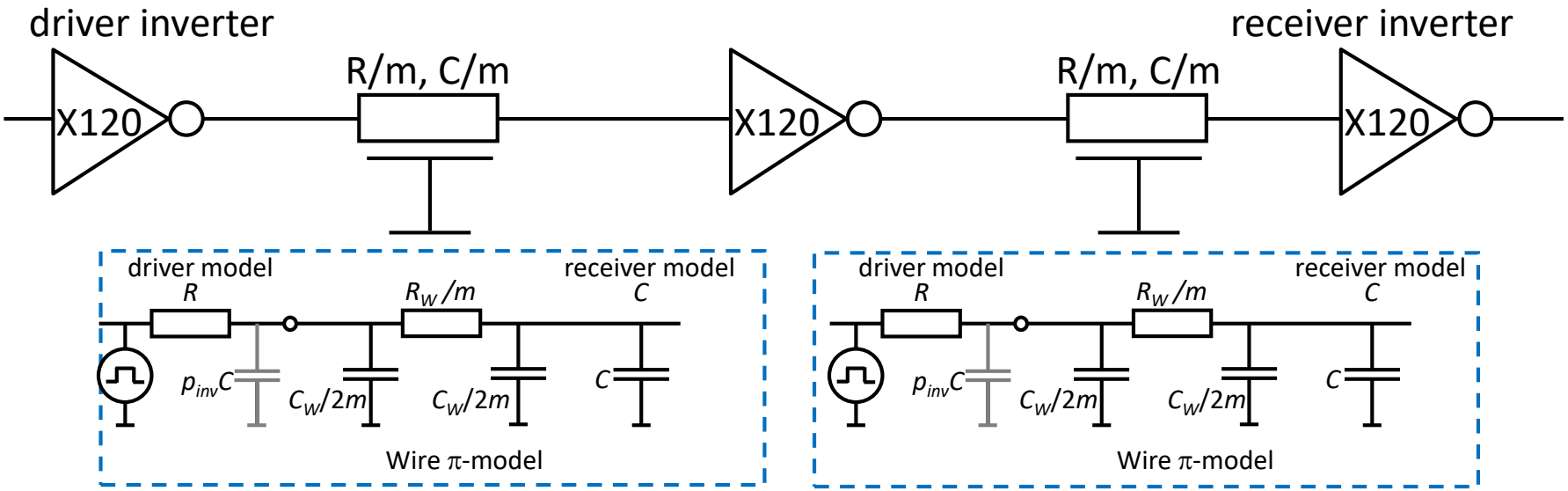
1. Start by defining wire effort $W_E = \frac{R_W C_W}{RC_{inv}}$

2. Elmore $T_E = RC\left(p_{inv}+1\right) + RC_W + R_W C + \frac{R_W C_W}{2}$

3. Normalize $d = p_{inv} + 1 + W_E \frac{R}{R_W} + \frac{R_W}{R} + \frac{W_E}{2}$

4. Find minimum $\frac{\partial d}{\partial R} = \frac{W_E}{R_W} - \frac{R_W}{R^2} = 0 \rightarrow R = \frac{R_W}{\sqrt{W_E}}$

Repeater insertion

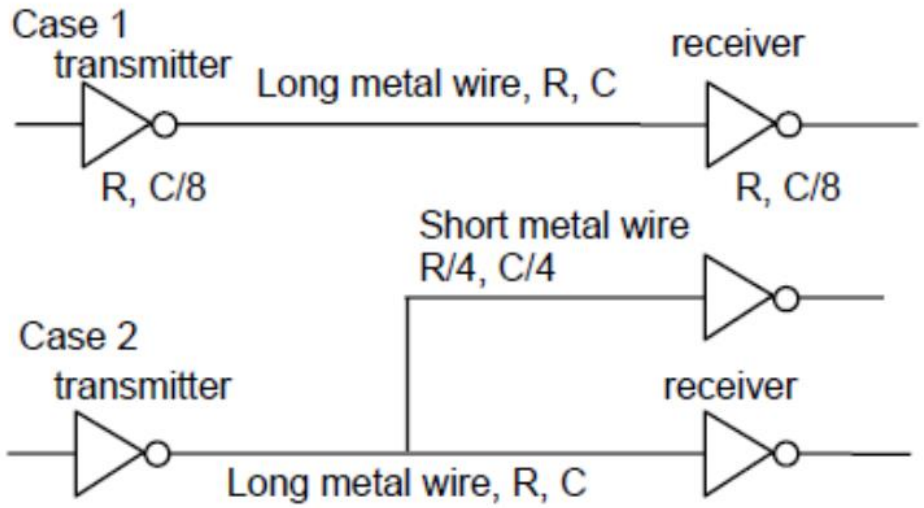


Normalized delay m segments $d = m\left(1 + p_{inv} + \frac{W_E}{m^2}\frac{mR}{R_W} + \frac{R_W}{mR} + \frac{W_E}{2m^2}\right)$

Find minimum, i.e. $\partial d/\partial m = 0$, i.e. for $m = \frac{1}{2}\sqrt{W_E}$

Minimum normalized delay is $d = 4\sqrt{W_E}$.

Divide and conquer

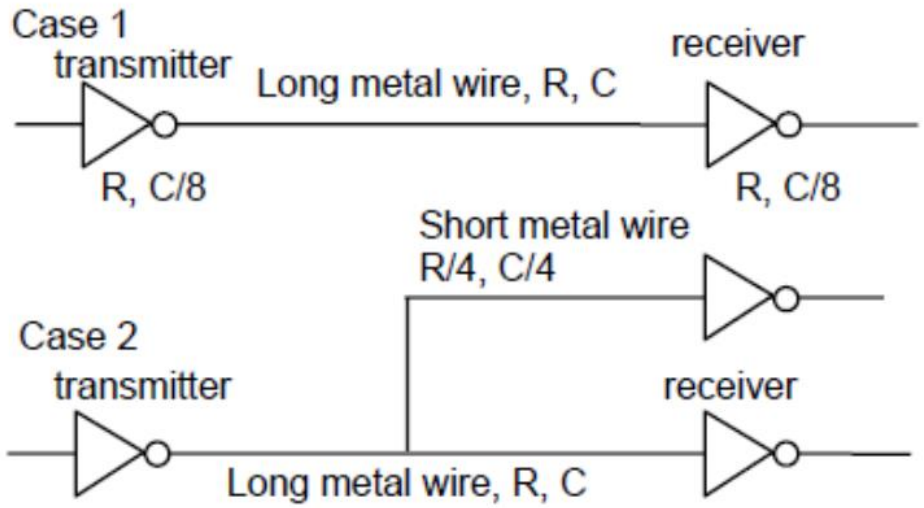


If they ask for the difference between *x*+*a* and *x*+*b*, i.e. *a*-*b*, we do not need to calculate *x*!
Branch contribution to delay is branch capacitance times upstream resistance

$$T_{E,branch} = \left(\frac{C}{4} + \frac{C}{8}\right)\left(R + \frac{R}{2}\right) = \frac{9}{16}RC$$

Total Elmore time constant is then 39*RC*/16≈2.5*RC*

Divide and conquer



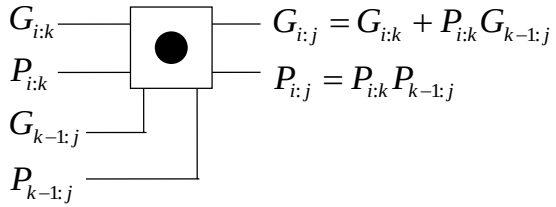
The wire to the other receiver is shorter, only ¾ of the other wire length
Hence, the main path to the other receiver has resistance 3*R*/4 and capacitance 3*C*/4
Main path delay contribution is found to be 22RC/16, and branch contribution is 15RC/16

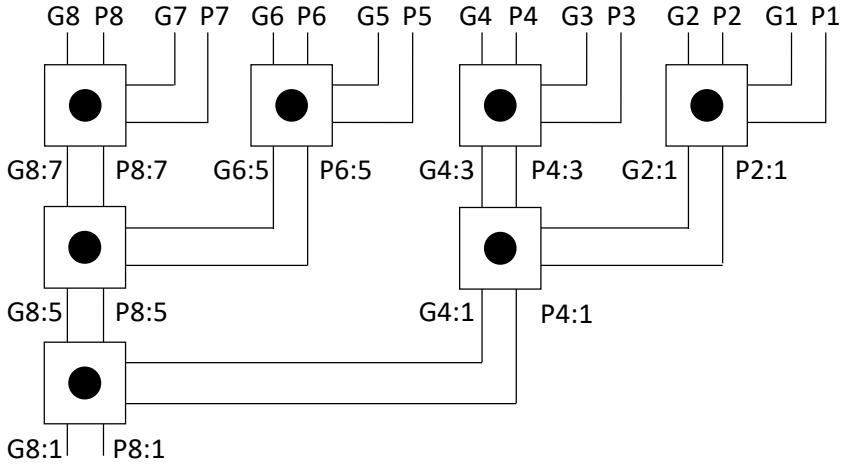
$$T_{E,branch} = \left(\frac{C}{2} + \frac{C}{8}\right)\left(R + \frac{R}{2}\right) = \frac{15}{16}RC$$

Total Elmore time constant is then 37*RC*/16≈2.3*RC*

The dot operator

The “dot operator” is associative and idempotent





Show that $(G_{4:3}, P_{4:3}) \bullet (G_{2:1}, P_{2:1}) = G_4 + P_4\left(G_3 + P_3\left(G_2 + P_2G_1\right)\right), P_4P_3P_2P_1$

Show that $(G_{4:2}, P_{4:2}) \bullet (G_{3:1}, P_{3:1}) = G_4 + P_4\left(G_3 + P_3\left(G_2 + P_2G_1\right)\right), P_4P_3P_2P_1$

The dot operator

- Properties of the dot operator
  - Associativity i.e. parallelization
    - Easy to prove since logical OR and AND operations are associative
    - With the definition $G_{i:i-1}, P_{i:i-1} = (G_i, P_i) \bullet (G_{i-1}, P_{i-1})$ G_i becomes the carry-out signal at stage *i* of an adder
  - The operation is idempotent

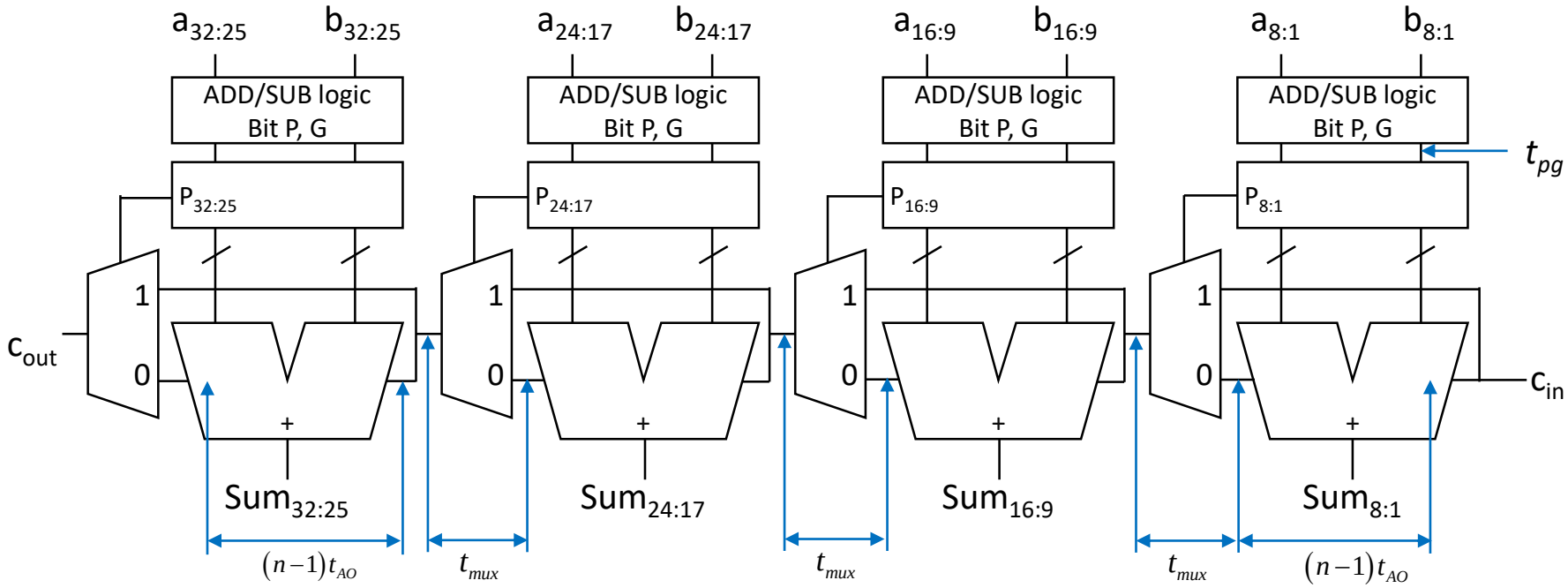
$$(G_{i:i-1}, P_{i:i-1}) \bullet (G_{i:i-1}, P_{i:i-1}) = (G_{i:i-1} + P_{i;i-1} G_{i:i-1}, P_{i;i-1} P_{i;i-1}) = (G_{i:i-1}, P_{i:i-1})$$

  - which implies

$G_{i:j}, P_{i:j} = (G_{i:n}, P_{i:n}) \bullet (G_{m:j}, P_{m:j})$ where $i \geq j$ and $m \geq n$

32-bit carry skip adder

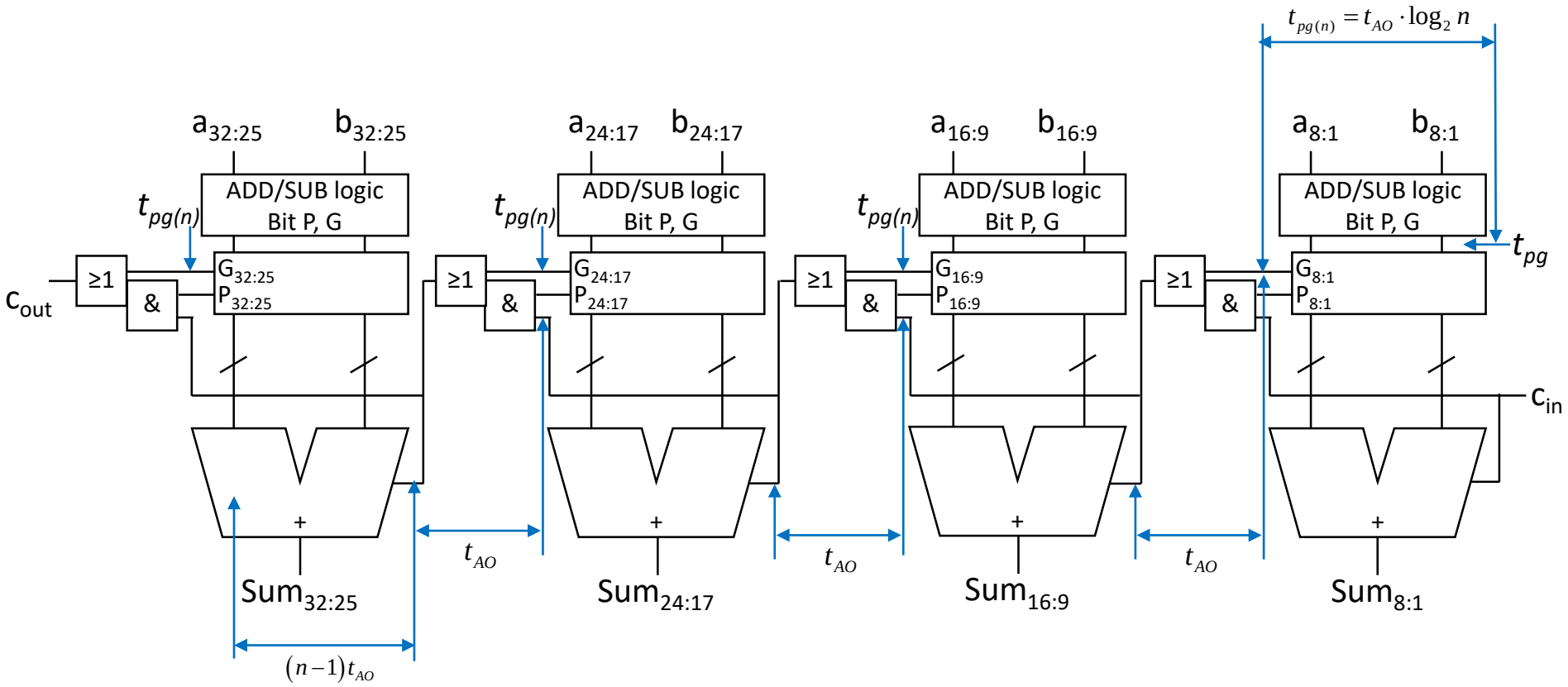
- Identify worst-case propagation delay for 32-bit adder!
- For N-bit adder built with *k* *n*-bit blocks!



Determine the worst case delay!

$$t_{skip} = t_{pg} + 2(n-1)t_{AO} + (k-1)t_{mux} + t_{XOR}$$

32-bit carry-lookahead adder



$$t_{CLA} = t_{pg} + t_{pg(n)} + (n-1+k-1)t_{AO} + t_{XOR}$$

Sklansky adder

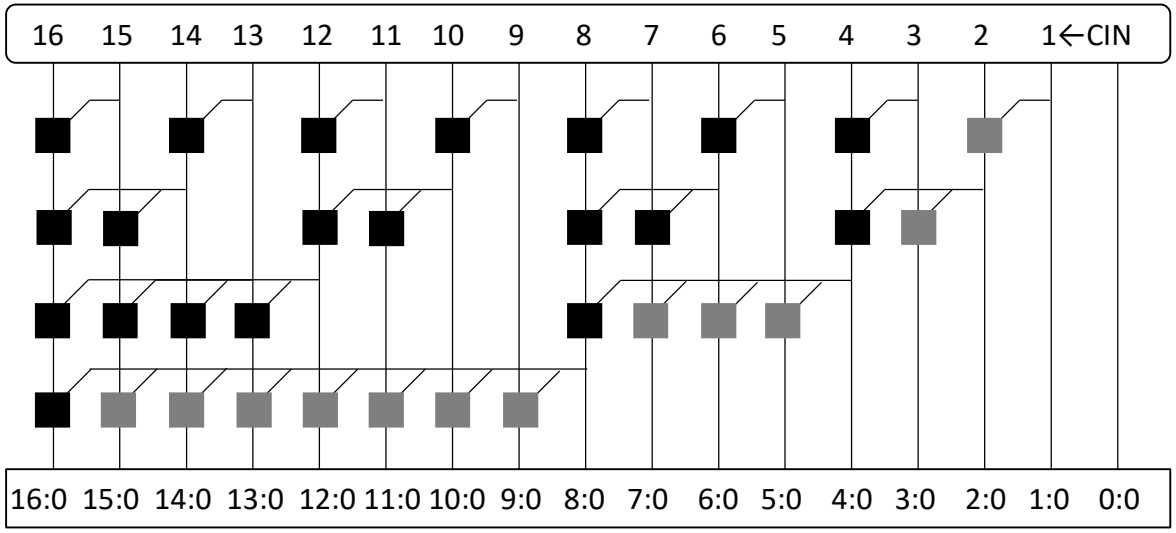


FIGURE 11.29 Tree adder PG networks

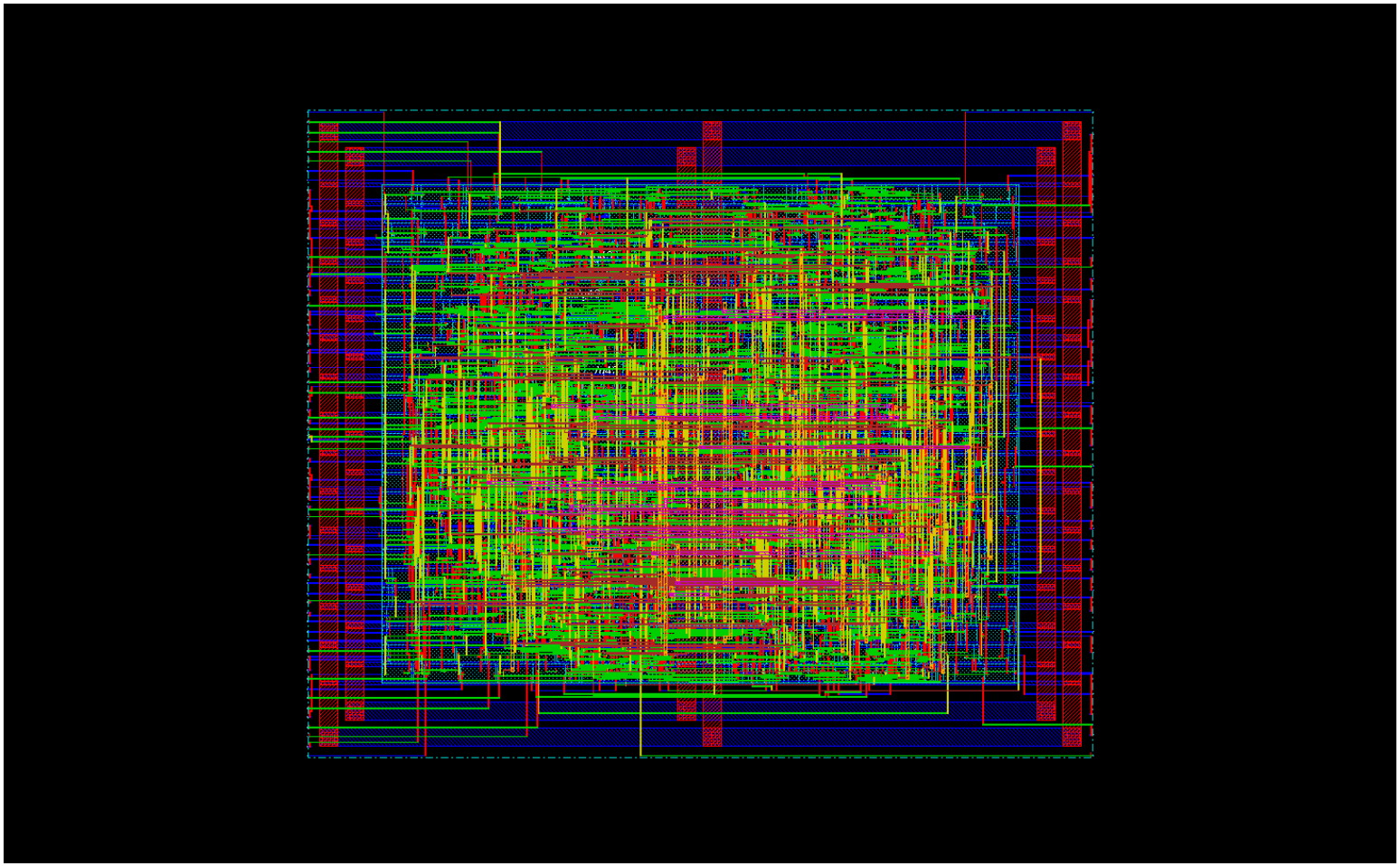
Logic levels L=4
Extra levels l=0
Fanout 2^f+1=9
f=3
Wire tracks 2^t=1
t=0
$l+f+t=L-1=3$
(0, 3, 0)

Determine the worst case delay!

$$t_{tree} = t_{pg} + t_{pg(n)} + t_{XOR}$$

$$t_{pg(n)} = \lceil \log_2 N \rceil t_{AO}$$

Example: synthesized 32-bit ALU layout



End of course wrap-up lecture!

Q & A?