Recap wires & interconnect incl. Prelab 4
Intro to adder exercise

Week 5

- Monday lab3
  - Carry gate layout
- Tuesday
  - Lecture Wires and interconnect (Kjell)
  - Postlab 3 + prelab 4
- Thursday
  - Recap wires + preparation for adder exercise 1
  - Tutorial POTW Wires
- Friday Deadline prelab 4
  - Clock tree simulation

Week 6

- Monday lab 4
  - Clock tree
- Tuesday
  - Adder exercise 1 in E-studion (Kjell)
  - Lecture Power Note in EA! (Kjell)
- Thursday
  - Postlab 4 + Recap power + adder preparation 2
  - Tutorial POTW Power

Week 7

- Monday Deadline Hand-in problem set 2
  - Wires, adders, power
- Tuesday
  - Adder exercise 2 in E-studion (Lena)
  - Lecture Sequential + metastability EA! (Lena)
- Thursday
  - Guest lecture – putting it all together (Erik Ryman)
  - Consolidation adders + recap sequential (Lena)
  - Exercise POTW (?)

Week 8

- Monday Deadline Hand-in problem set 3
  - Sequential, adders + some more
- Tuesday
  - Conclusion (Lena)
  - Lecture Sequential + metastability EA! (Lena)
- Thursday
  - Guest lecture – putting it all together (Erik Ryman)
  - Consolidation adders + recap sequential (Lena)
  - Exercise POTW (?)

From MUD cards

- Elmore delay:
  - How to find the main path for calculating Elmore delay?
  - Calculating Elmore delay.
  - Didn't quite get Elmore.
- Buffer insertion
  - How do we reduce the delay equation after manipulating the R with driving capacitances?
  - What about model of RC wire if pinv isn't1 1?
- Clock tree
  - Is clock tree symmetry the norm?
  - Formula derivation for the H tree.
  - Derivation of the H tree.
- What should we know about wires for the exam?
- + a few "I'm confused".

Elmore delay

- Elmore delay is an approximation
  - It is a pessimistic approximation so you can be sure that the real delay is smaller especially for step responses
  - As rise times of the input signal increases Elmore delay approaches real delay.

Elmore delay in an RC tree

The Elmore delay from the input node to node *i* is:

$$T_{E_i} = \sum_{k=1}^{N} R_{ki} C_k$$

where N is the number of nodes in the RC tree
R_{ki} is the resistance of the portion of the path between the input and node i, that is **common** with the path between the input and node k
C_k is the capacitance at node k

An example

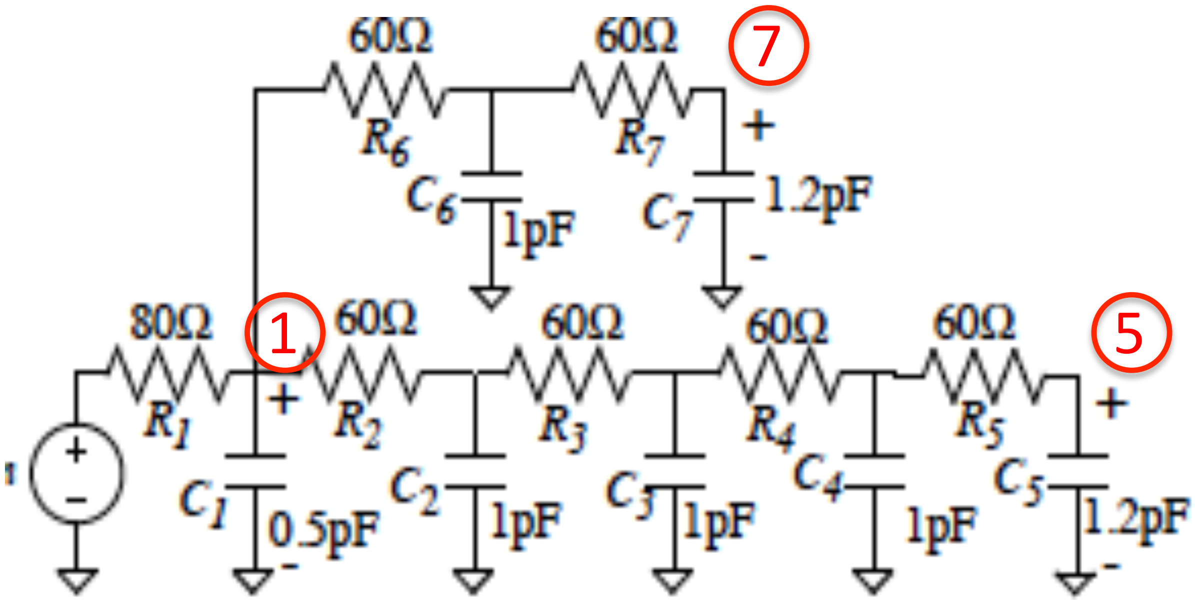


FIGURE 1: A simple RC tree.

What is Elmore delay to node 1, 5, 7?
Give answer in ps

An example

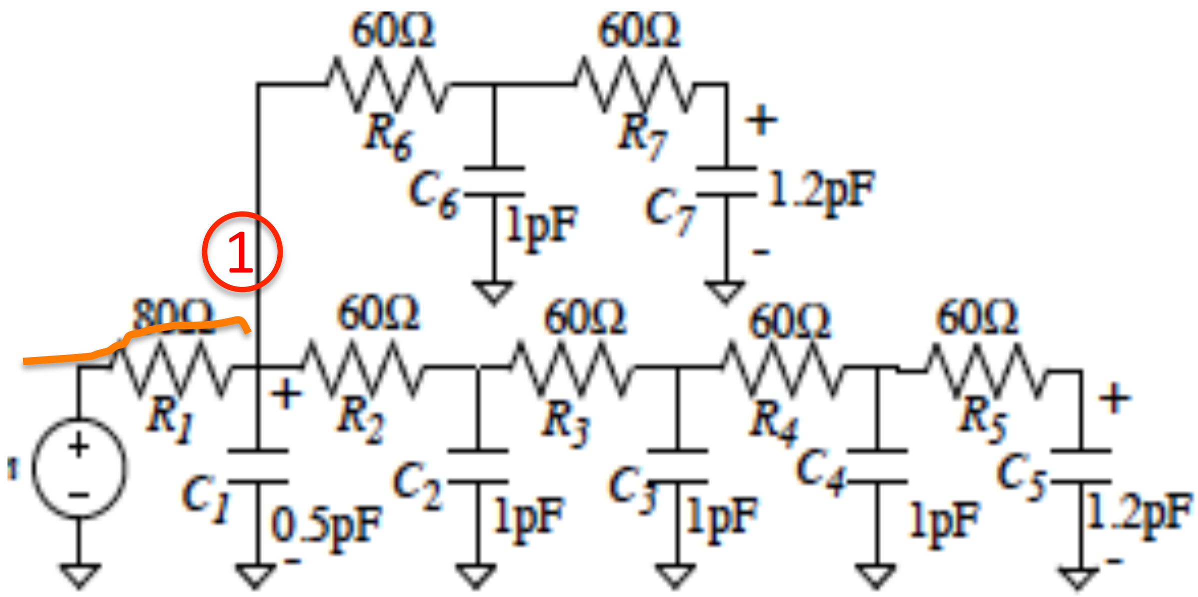


FIGURE 1: A simple RC tree.

Main path to node 1: 80 Ω×0.5 pF = 40 ps
Delay due to all other capacitances not on main path:
Branches: 80 Ω × 6.4 pF = 512 ps

T_{E1} = 40 ps + 608 ps = 552 ps

An example

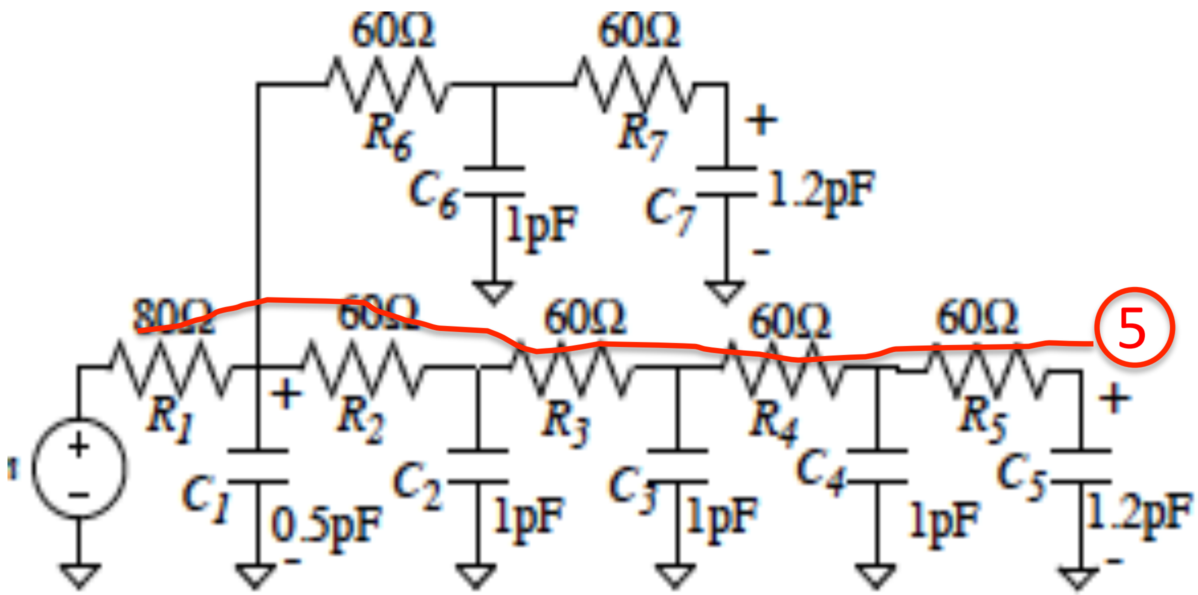


FIGURE 1: A simple RC tree.

Main path to node 5:

80 Ω×0.5 pF + 140 Ω×1 pF+ 200 Ω×1 pF + 260 Ω×1 pF + 320 Ω×1.2 pF =

80 Ω×0.5 pF + 600 Ω×1 pF+ 320 Ω×1.2 pF = 40 + 600 + 384 ps = 1024 ps

Delay due to all other capacitances not on main path:

Branches: 80 Ω × 2.2 pF = 176 ps

T_{E5} = 1024ps + 176 ps = 1200 ps

An example

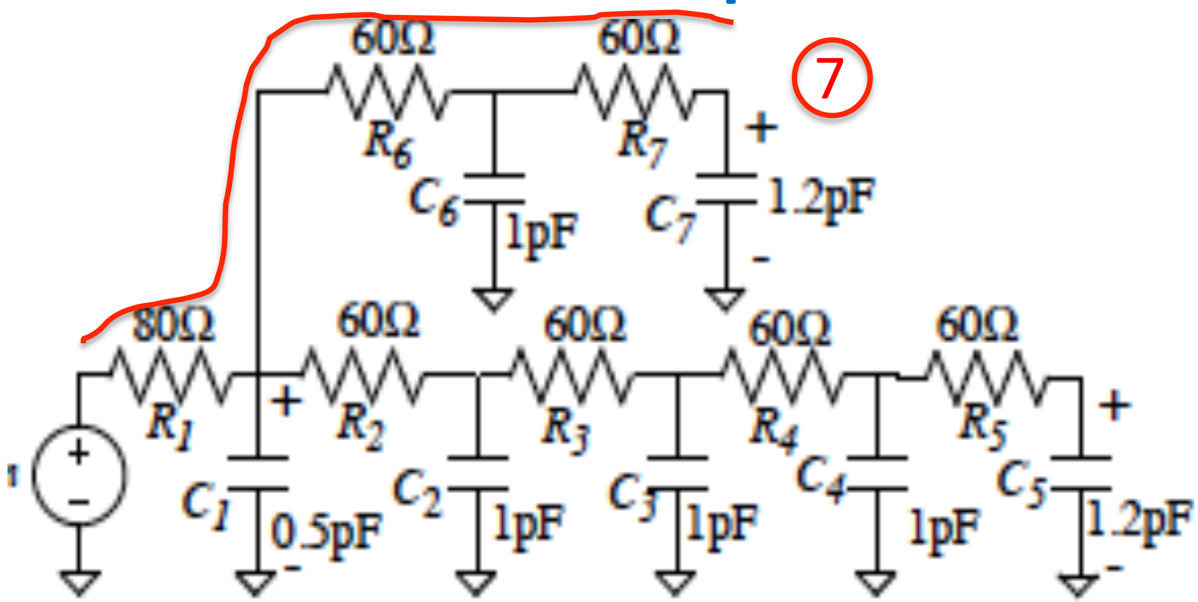


FIGURE 1: A simple RC tree.

Main path to node 5:

80 Ω×0.5 pF + 140 Ω×1 pF+ 200 Ω×1.2 pF = 40 + 140 + 240 ps = 420 ps

Delay due to all other capacitances not on main path:

Branches: 80 Ω × 4.2 pF = 336 ps

T_{E7} = 420 ps + 336 ps = 756 ps

Results

(1)	(2)	(3)	(4)	(5)	(6)	(7)
Node	Actual delay (ns)	Elmore delay, T_D (ns)	Lower bound, T_D-σ (ns)	Single pole, T_D.ln(2) (ns)	RPH upper bound, t_{max} (ns)	RPH lower bound, t_{min} (ns)
C_1	0.196	0.55	0	0.383	0.55	0
C_5	0.919	1.2	0.2	0.83	1.32	0.51
C_7	0.45	0.75	0	0.524	1.02	0.054

TABLE 1: Delay bounds for circuit in Fig.1.

Example and table is taken from:
R. Gupta, B. Krauter, B. Tutuianu, J. Willis and L. Pileggi, "The Elmore Delay as a Bound for RC-Trees with Generalized Input Signals", Proceedings of the Design Automation Conference, 1995.

An inverter driving a wire

Elmore delay for inverter driving wire:

$$T_E = \underbrace{R\left(C_D + C\right)}_{=2\times 7.2\text{ ps if } p_{inv}=1} + \underbrace{RC_w}_{R\text{ is unknown}} + \underbrace{R_w C}_{C\text{ is unknown}} + \underbrace{\frac{R_w C_w}{2}}_{80\text{ ps}} \geq 94.4\text{ ps}$$

Dominating time constant T_E can be normalized wrt technology time constant *RC*!

$$d = \frac{T_E}{\underbrace{RC}_{inverter}} = p_{inv} + 1 + \frac{R_W C_W}{RC}\frac{R}{R_W} + \frac{R_W}{R} + \frac{R_W C_W}{2RC}$$

Introduce wire effort:

$$W_E = \frac{R_W C_W}{RC}$$

$$d = p_{inv} + 1 + W_E \frac{R}{R_W} + \frac{R_W}{R} + \frac{W_E}{2}$$

Buffer insertion – divide wire into *m* segments

$$d_{\text{segment}} = 1 + p_{inv} + \frac{W_E}{m^2}\frac{R}{R_W/m} + \frac{R_W/m}{R} + \frac{W_E}{2m^2}$$

$$d_{\text{total}} = m \times \left[1 + p_{inv} + \frac{W_E}{m^2}\frac{R}{R_W/m} + \frac{R_W/m}{R} + \frac{W_E}{2m^2}\right]$$

Buffer insertion in a nutshell

Wire effort: $$W_E = \frac{R_W C_W}{RC}$$ A large number for a long wire!

Optimal driver resistance: $$R_{opt} = \frac{R_W}{\sqrt{W_E}}$$

Assume p_{inv} = 1 for results below

Optimal number of segments: $$m_{opt} = \frac{\sqrt{W_E}}{2}$$ Note: not number of repeaters!

$$d_{opt} = 4\sqrt{W_E}$$ All 4 parts in delay equation the same

Critical wire length
$$L_{crit} = \frac{L}{m_{opt}}$$

$$L_{crit} = \frac{2L}{\sqrt{W_E}}$$

Finding the optimal inverter resistance

Delay for a wire driven by an inverter

$$d = 1 + p_{inv} + W_E \frac{R}{R_W} + \frac{R_W}{R} + \frac{W_E}{2}$$

Find the inverter resistance R that minimizes delay

Take derivative of d w.r.t R

$$\frac{\partial d}{\partial R} = \frac{W_E}{R_W} - \frac{R_W}{R^2}$$

Set derivative equal to 0

$$\frac{W_E}{R_W} - \frac{R_W}{R^2} = 0$$

Solve for optimal R: R_{opt}

$$R_{opt}^2 = R_W^2 / W_E$$

Note that so far p_{inv} does not matter!

$$R_{opt} = \frac{R_W}{\sqrt{W_E}}$$

Finding an expression for the delay with *m* segments

$$d_{\text{segment}} = 1 + p_{inv} + \frac{W_E}{m^2}\frac{R}{R_W/m} + \frac{R_W/m}{R} + \frac{W_E}{2m^2}$$

$$d_{\text{total}} = m \times \left[1 + p_{inv} + \frac{W_E}{m^2}\frac{R}{R_W/m} + \frac{R_W/m}{R} + \frac{W_E}{2m^2}\right]$$

Insert $R_{opt} = \frac{R_W}{\sqrt{W_E}}$ so that we can see better what we have

$$d_{\text{total}} = m \times \left[1 + p_{inv} + \frac{\sqrt{W_E}}{m} + \frac{\sqrt{W_E}}{m} + \frac{W_E}{2m^2}\right]$$

$$d_{\text{total}} = m(1 + p_{inv}) + 2\sqrt{W_E} + \frac{W_E}{2m}$$

Note that so far p_{inv} does not matter!

Finding the optimal number of stages m_{opt}

$$d_{\text{total}} = m(1 + p_{inv}) + 2\sqrt{W_E} + \frac{W_E}{2m}$$

Find the number of segments *m* that minimizes delay

Take derivative of d_{total} w.r.t. *m*

$$\frac{\partial d_{total}}{\partial m} = 1 + p_{inv} - \frac{W_E}{2m^2}$$

Set derivative equal to 0

$$1 + p_{inv} - \frac{W_E}{2m^2} = 0$$

Solve for m_{opt}:

With pinv = 1: $$m_{opt} = \frac{\sqrt{W_E}}{2}$$

This is where p_{inv} matters!

In general: $$m_{opt} = \sqrt{\frac{W_E}{2(1 + p_{inv})}}$$

Finding the critical length L_{crit}

The critical length for wire insertion; that is the length at which one should consider inserting a buffer

$$L_{crit} = \frac{L}{m_{opt}}$$

With pinv = 1: $$m_{opt} = \frac{\sqrt{W_E}}{2}$$ $$L_{crit} = \frac{2L}{\sqrt{W_E}}$$

In general: $$m_{opt} = \sqrt{\frac{W_E}{2(1+p_{inv})}}$$ $$L_{crit} = \frac{L\sqrt{2(1+p_{inv})}}{\sqrt{W_E}}$$

Buffer insertion in a nutshell

Wire effort: $$W_E = \frac{R_W C_W}{RC}$$

Optimal driver resistance: $$R_{opt} = \frac{R_W}{\sqrt{W_E}}$$

Optimal number of segments: $$m_{opt} = \frac{\sqrt{W_E}}{2}$$

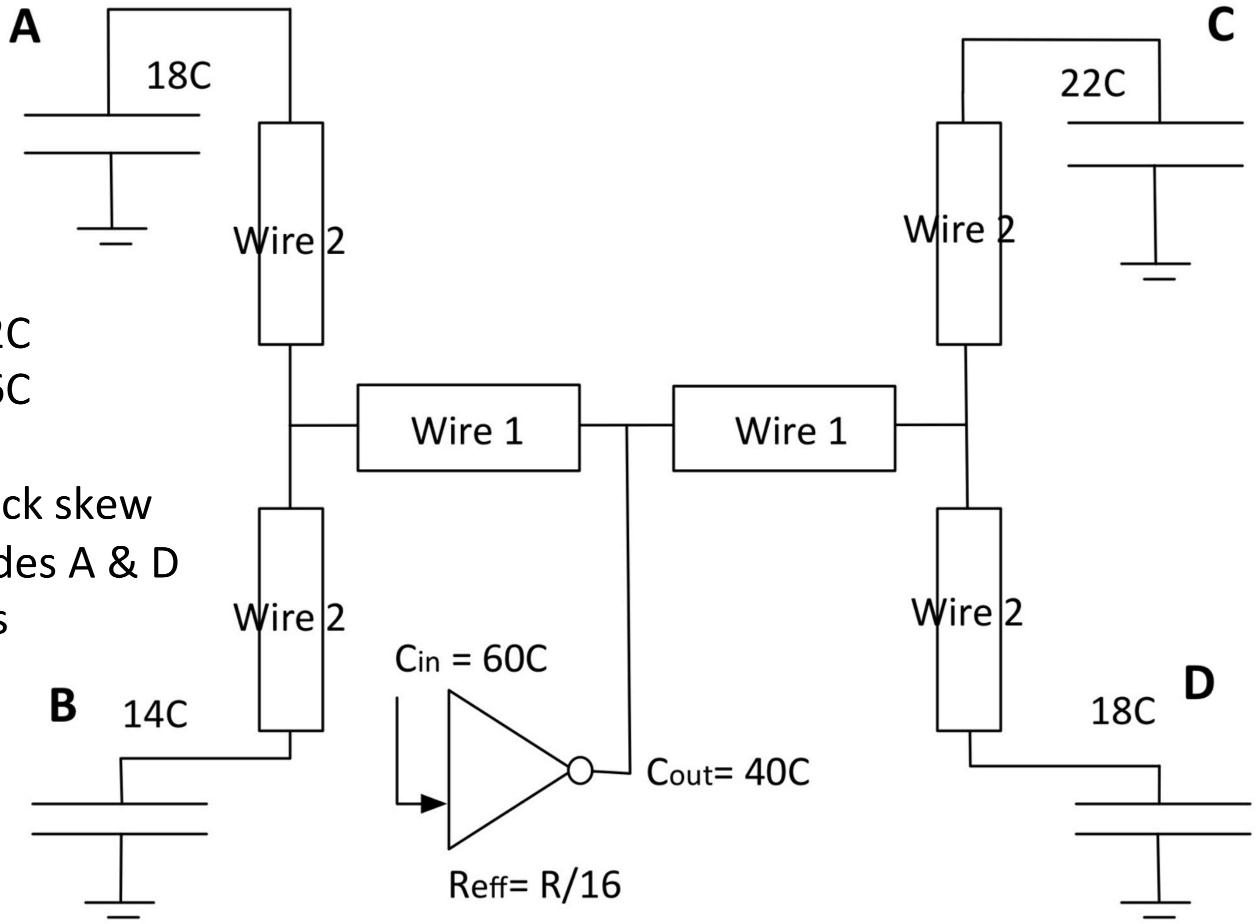
$$d_{opt} = 4\sqrt{W_E}$$

Critical wire length $$L_{crit} = \frac{L}{m_{opt}} \quad L_{crit} = \frac{2L}{\sqrt{W_E}}$$

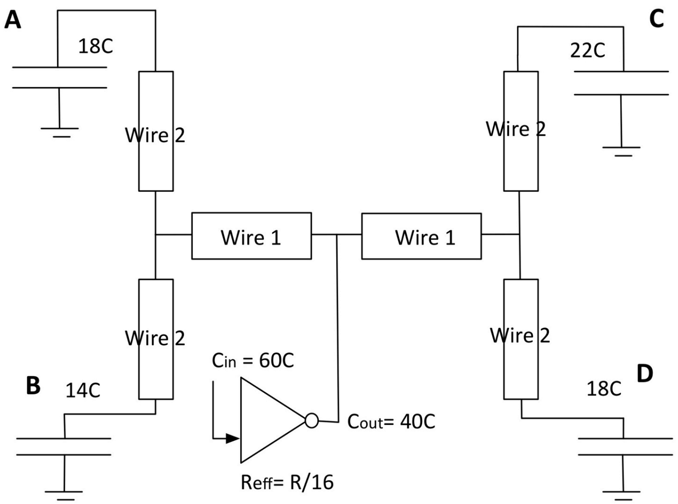
An H tree example

Wire 1: R, 12C
Wire 2: 2R, 6C

Calculate clock skew
Between nodes A & D
Clock skew is
difference
in delay



An H tree example solution



A & D main paths are the same

Also the contribution to the branch delay from the wire segments are the same since the wires are fully symmetrical

Calculate only the impact of the branch leaf capacitances.

For node A: $R/16 \times (22C+18C) + 17R/16 \times 14C$

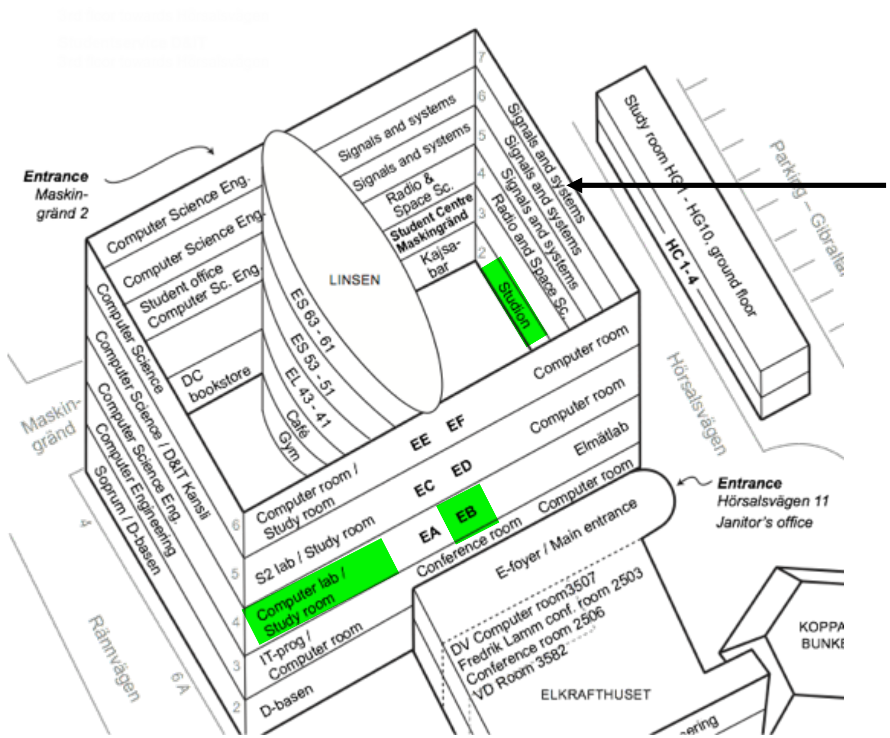
For node D: $R/16 \times (14C+18C) + 17R/16 \times 22C$

Take D-A delay: $- R/16 \times 8C + 17R/16 \times 8C =$ **8RC**

(The sign does not matter here; I just did the subtraction in this order, D-A, to get a positive answer).

Adder lecture/exercises

- Tuesday October 9 13.15-15.00 in E-studion.
- Tuesday October 16 13.15-15.00 in E-studion.



Entry is from Hörsalsvägen

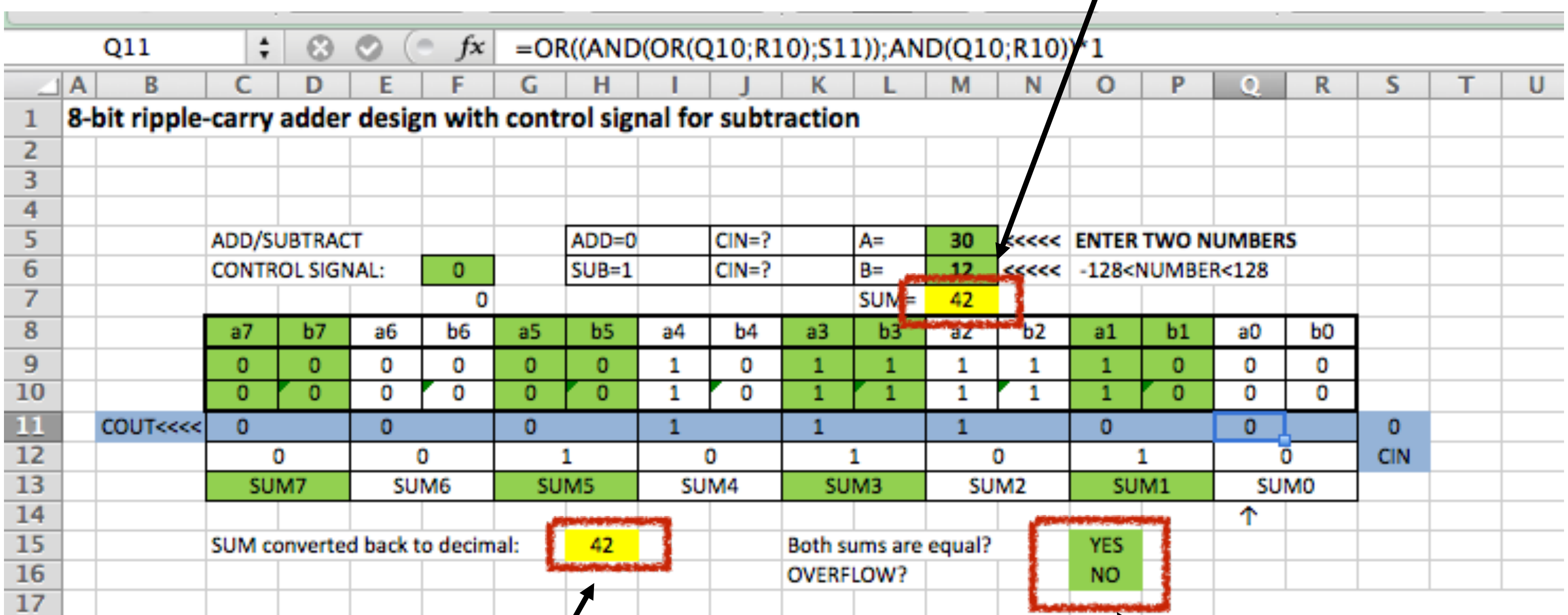
Adder lecture/exercise preparation

- If you do not have access to the book download **chapter 11** of W&H from cmosvlsi.com. Use"Look inside" to the left.
- Read sections 11.2.1, 11.2.2 (for Oct. 9 up to 11.2.2.8 for Oct. 16 the rest of 11.2.2) Skip any optional parts.
- Find excel (either on Chalmers PC:s or download it on your own computer - see later slides).
- Download example file: Excel_examples 2017.xslx and open in Excel. There are three examples:
  1. An 8-bit zero-detect circuit as ILA
  2. An 8-bit comparator circuit as ILA
  3. An 8-bit ripple-carry adder with negation

- The example file is located in Documents -> Old written exams and other problems -> Exercises

Ripple-carry adder

Result from numbers

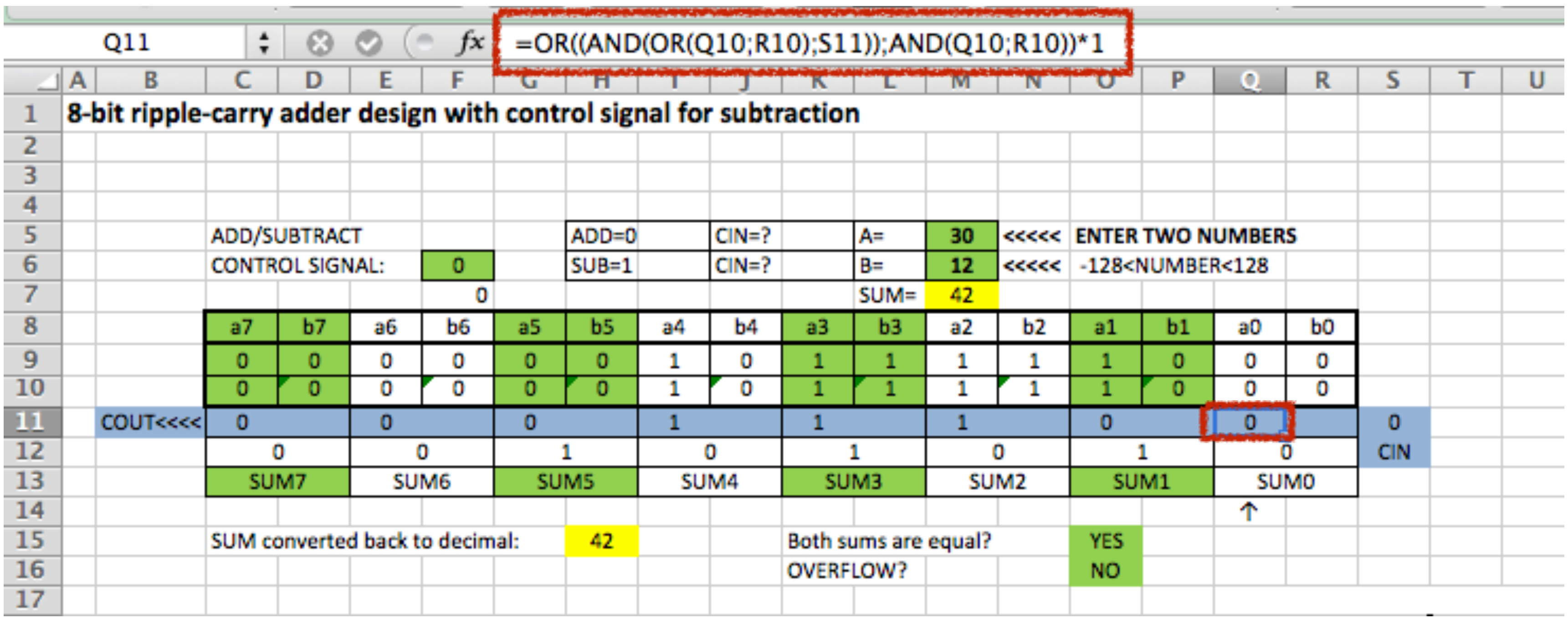


Result from adder

Equal results?

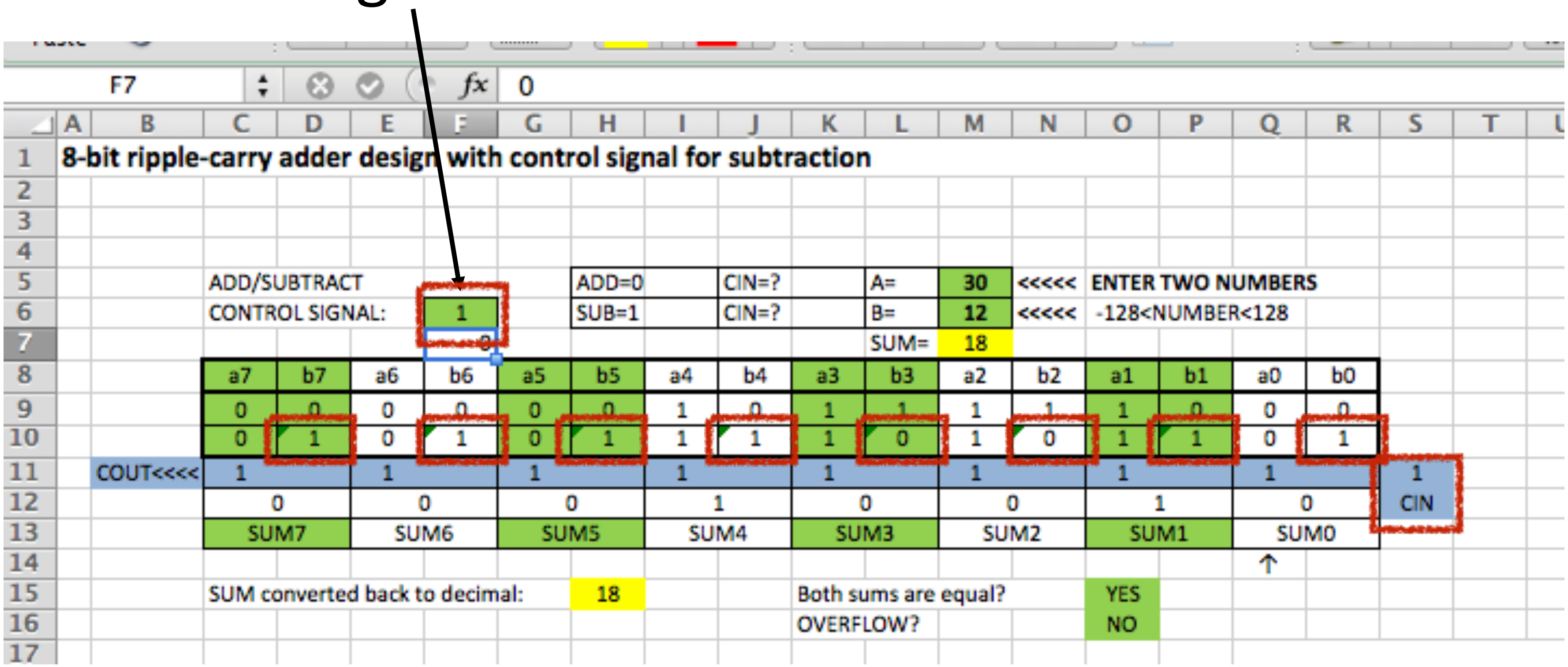
Addition

Expression for C_{out0}



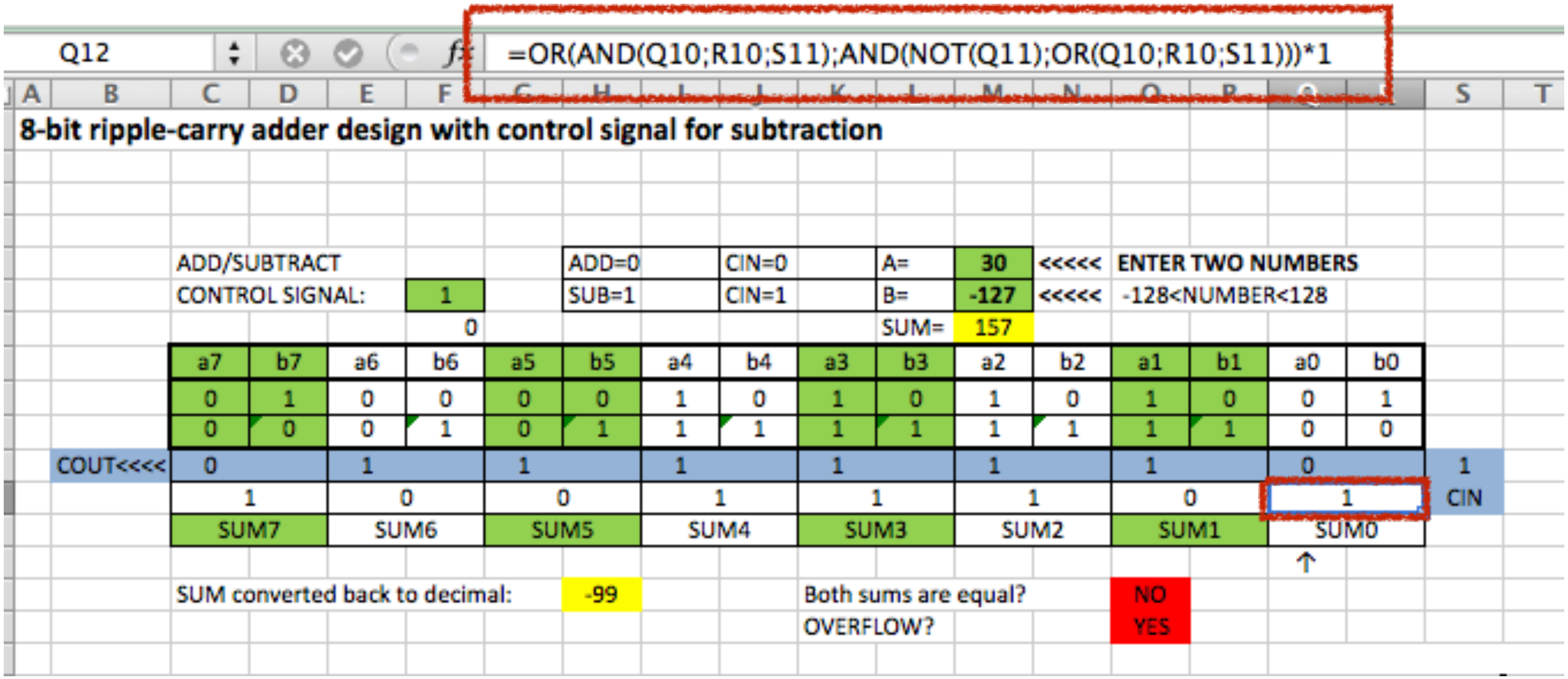
Subtraction

Control signal



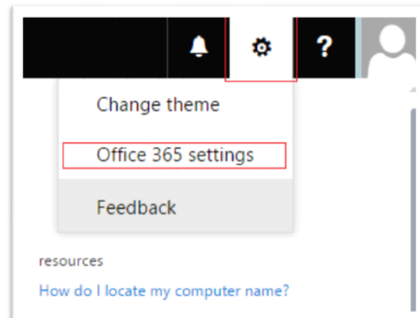
Overflow

Expression for SUM_0

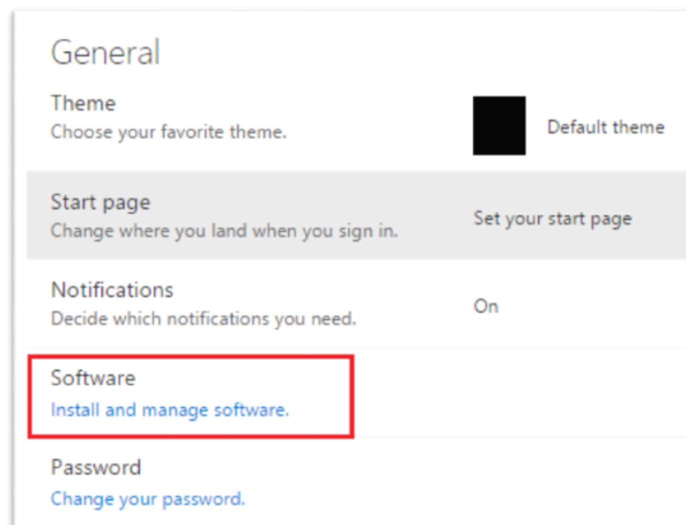


How to download Office 365 on your own PC (1)

1. Go to: https://outlook.com/net.chalmers.se
2. Click on the cogwheel, select "Office 365 settings"

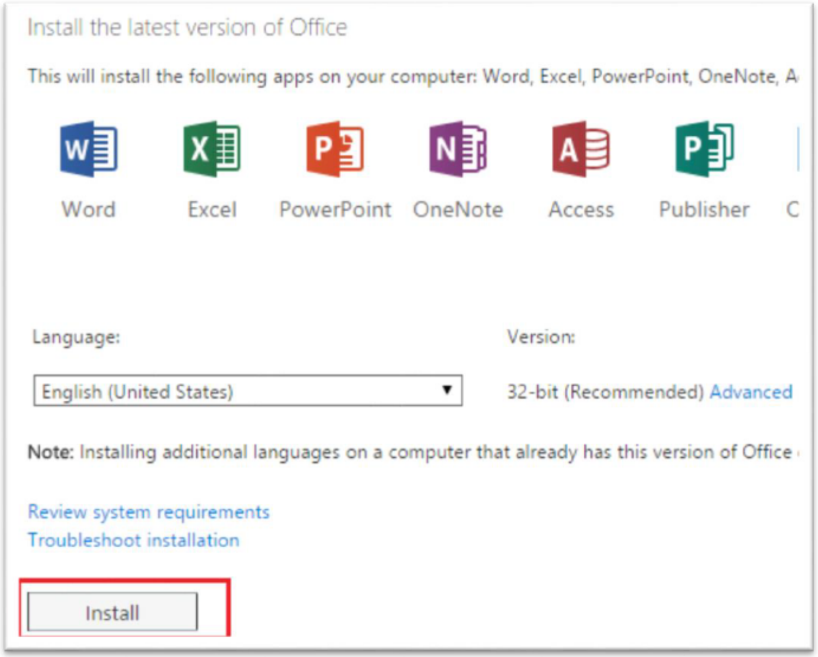


3. Under "Software" click on "Install and manage software" It does not look exactly like this now, I think, but in that case search for "Software".



How to download Office 365 on your own PC (2)

4. Download the installation program:
5. When you are asked to activate the license log in with CID@net.chalmers.se



Note! Only one installation per CID is allowed