Lecture 1

Course subject intro

Designing CMOS gates

2018-09-04

Lecture outline

- CMOS design overview
- Skills developed and knowledge gained from the course
  - Tool handling skills: Cadence Electronic Design Automation (EDA)
  - Theoretical insights –pre-design estimations with pencil on paper
- The design flow – textbook MIPS example
- Iterative Logic Arrays (ILAs)
- Adder designs – custom design vs. synthesis from VHDL
- CMOS Fabrication
- Designing CMOS logic gates using MOSFET switches
- Exercises and
- Summary

Design flow

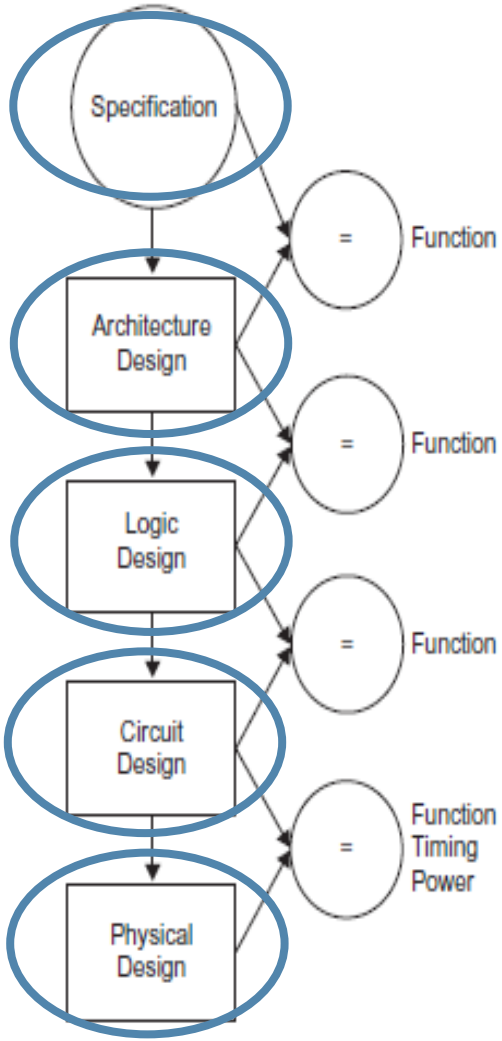
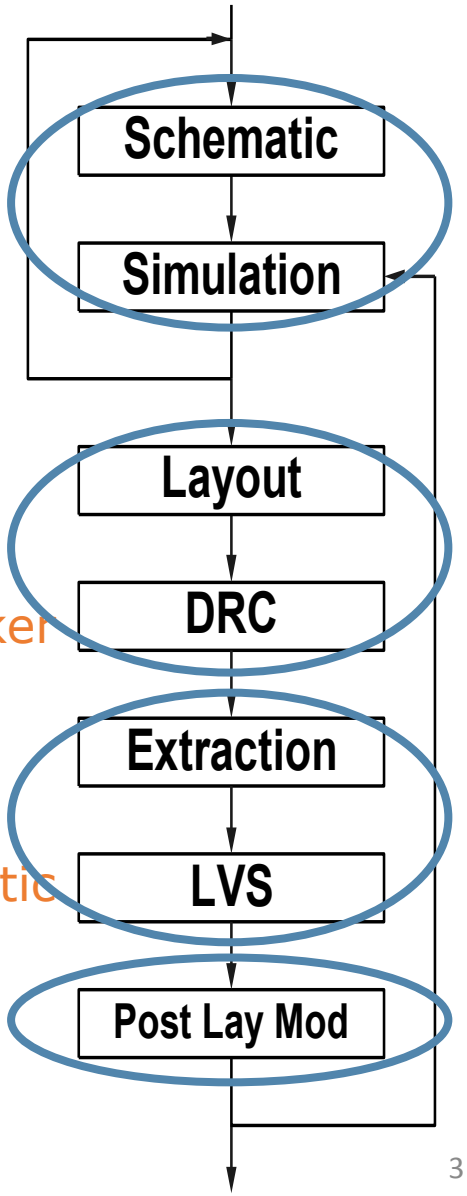


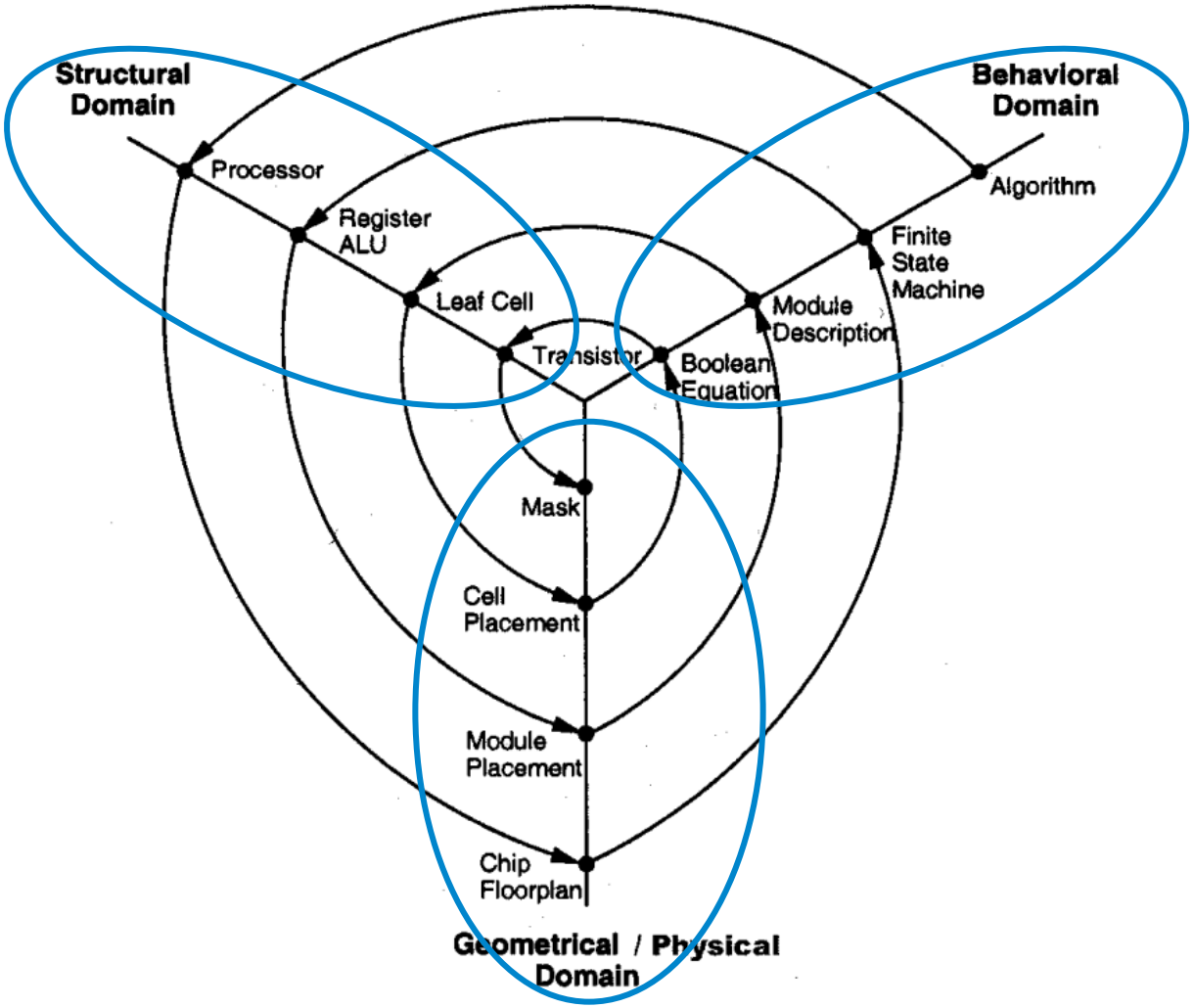
FIGURE 1.70 Design and verification sequence

DRC = Design Rule Checker

LVS = Layout Versus Schematic



Gajski Y-chart



Block Diagram (textbook MIPS example)

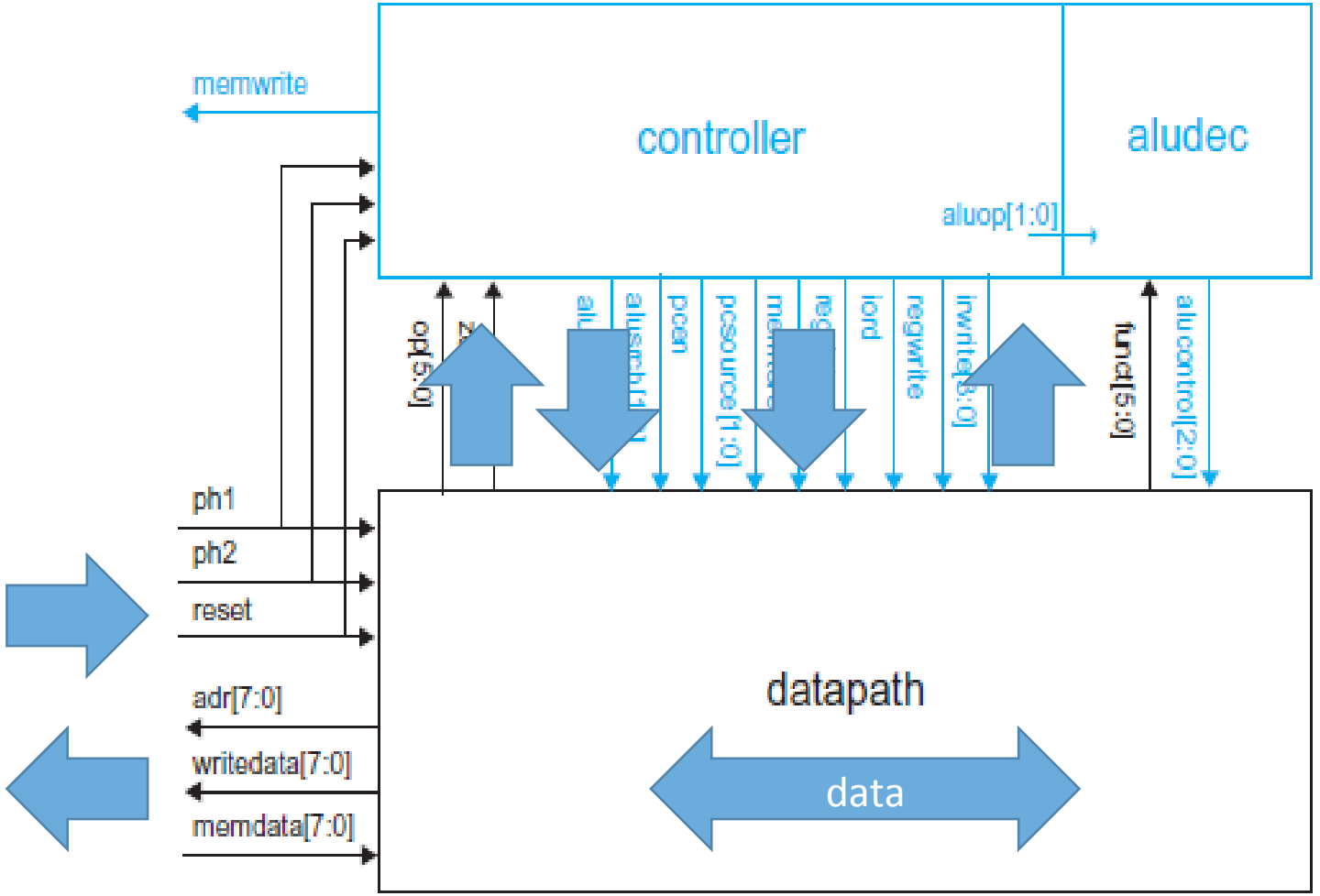
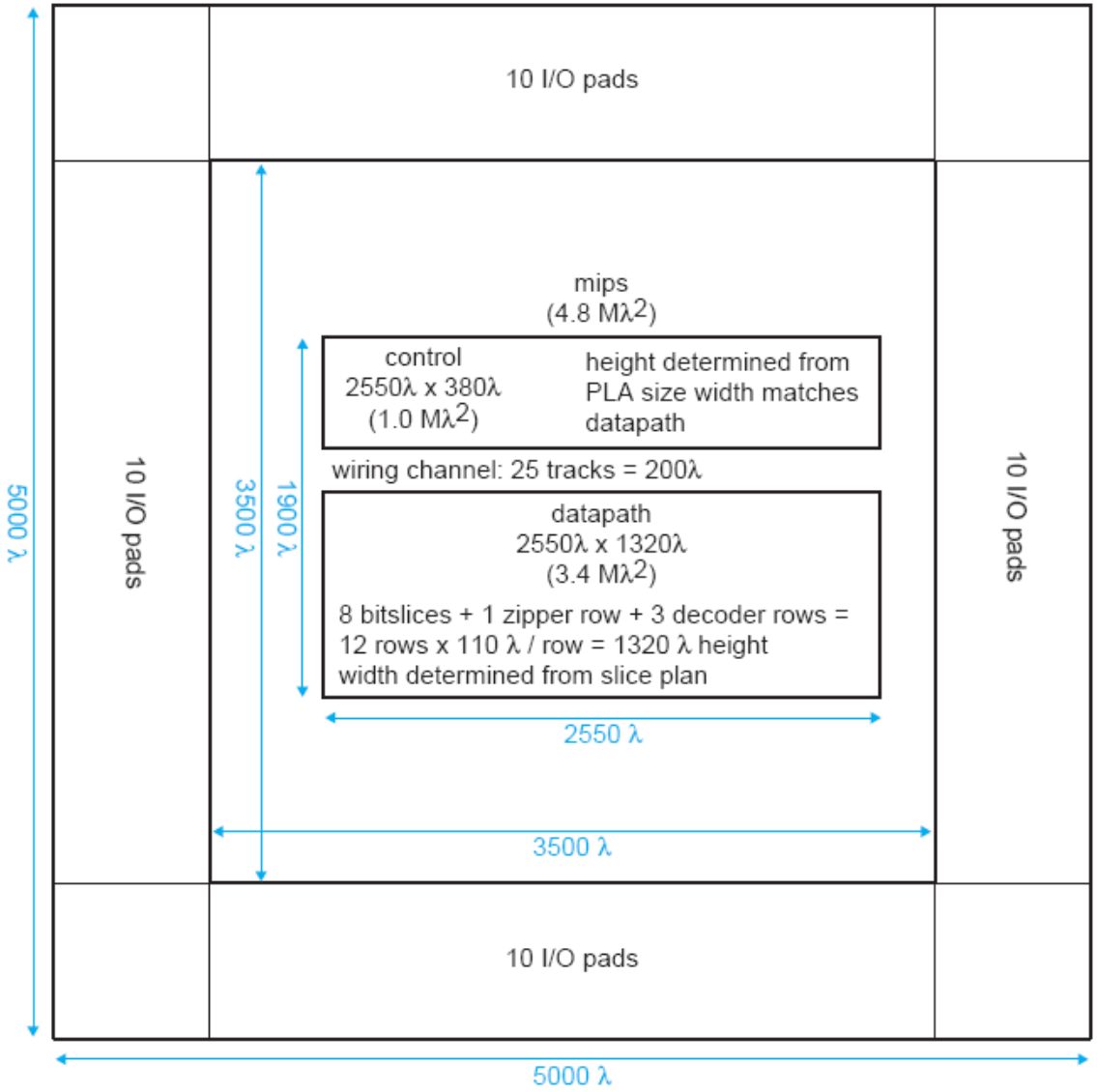
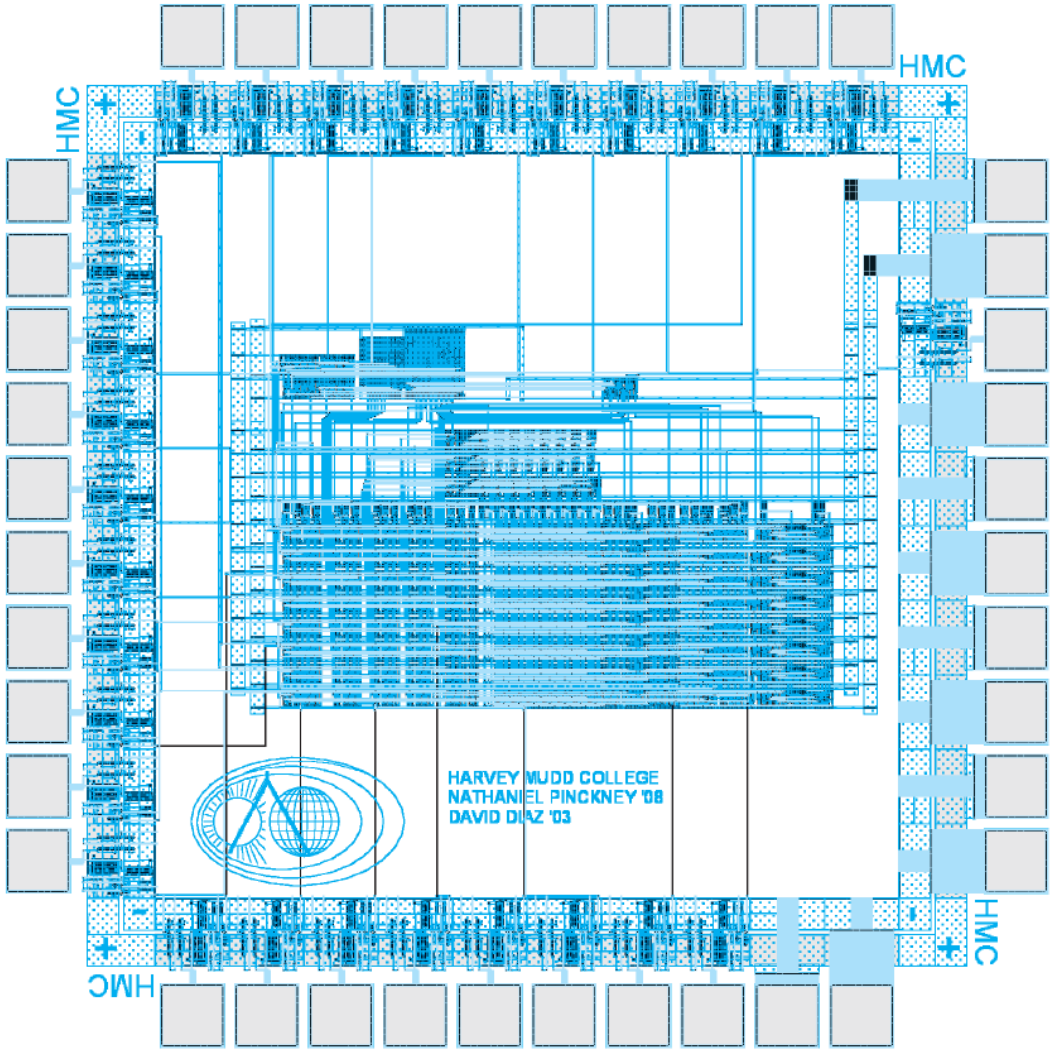


FIGURE 1.56 Top-level MIPS block diagram

Floor planning



MIPS Layout


HMC
HMC
HMC
HMC
HARVEY MUDD COLLEGE
NATHANIEL PINCKNEY '08
DAVID DIAZ '03

Datapath layout

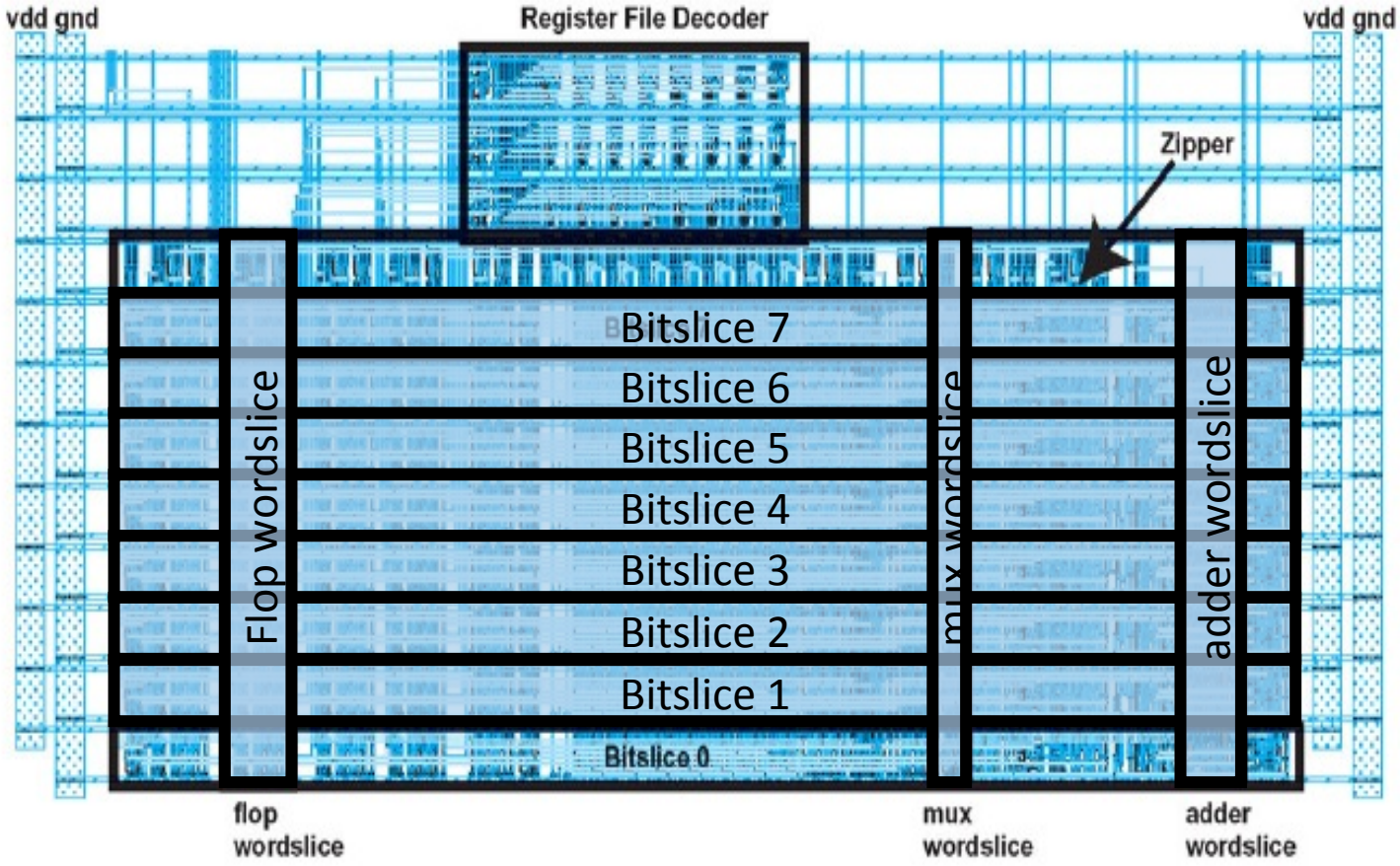
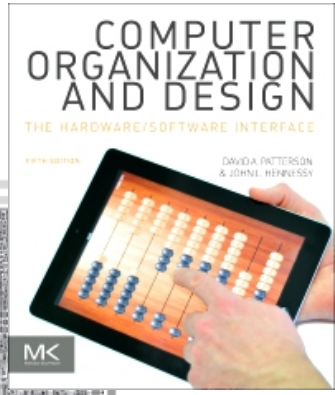


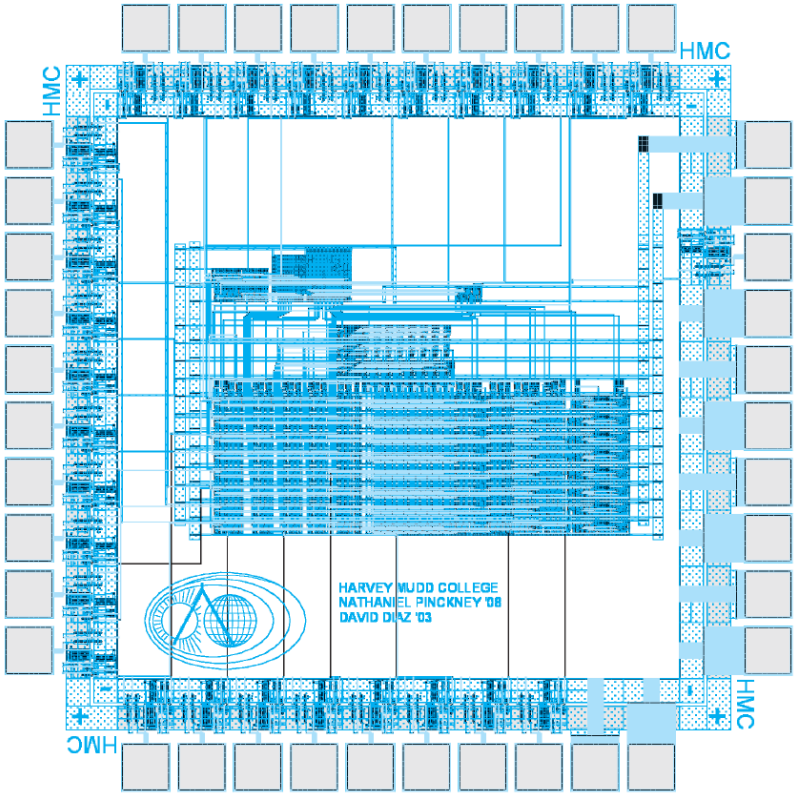
FIGURE 1.67 MIPS datapath layout

Bitslices form iterative logic arrays (ILAs)

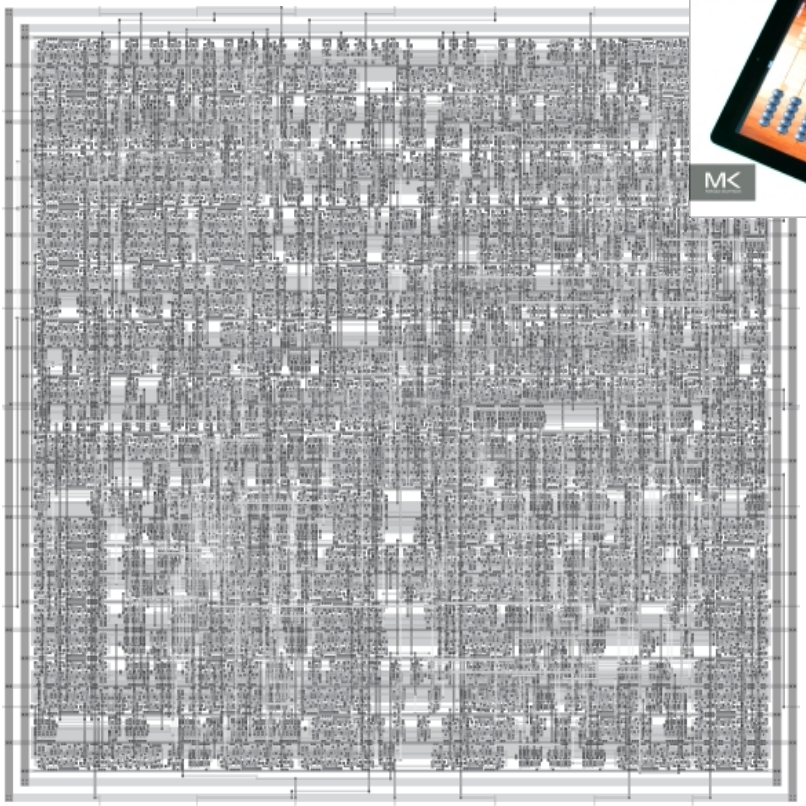
Custom design vs. synthesis from VHDL

8-bit implementations of MIPS from Patterson & Hennessy





Custom design, 0.6 um CMOS, 1.5x1.5 mm die



Standard cells, 130 nm CMOS, 7 metal layers

Iterative Logic Array (ILA)

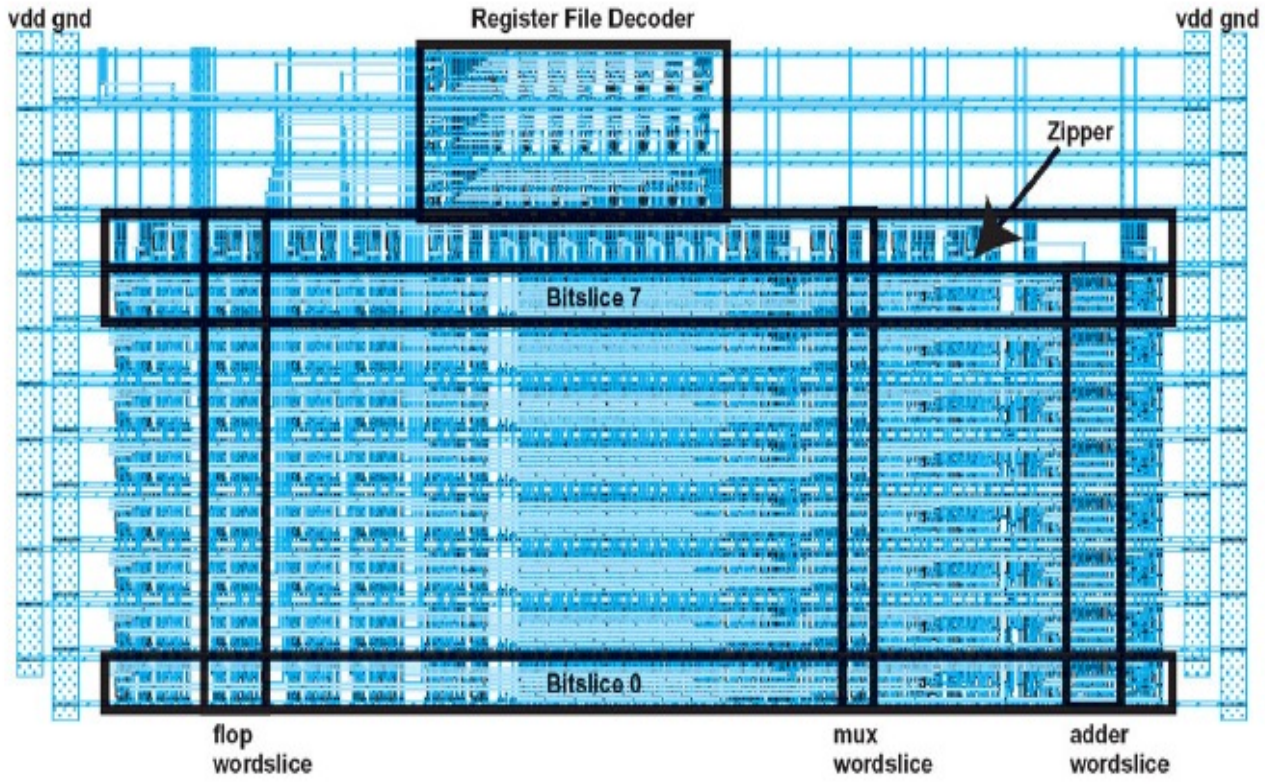
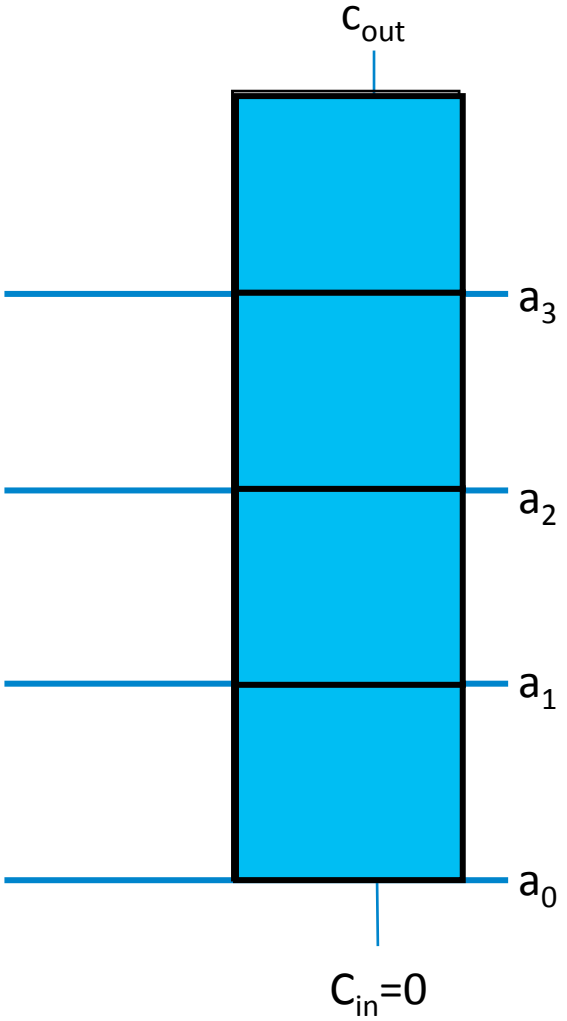
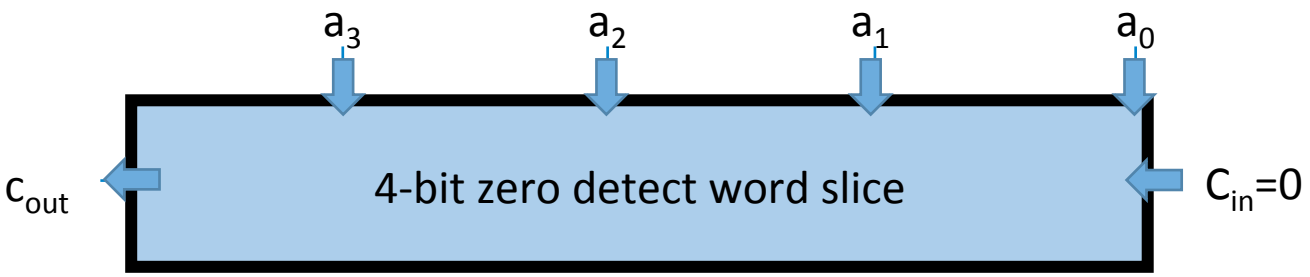


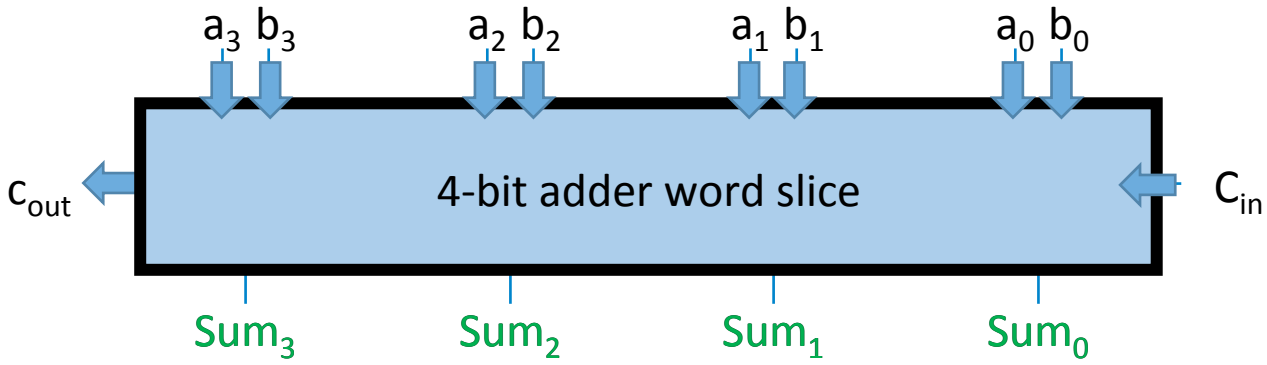
FIGURE 1.67 MIPS datapath layout



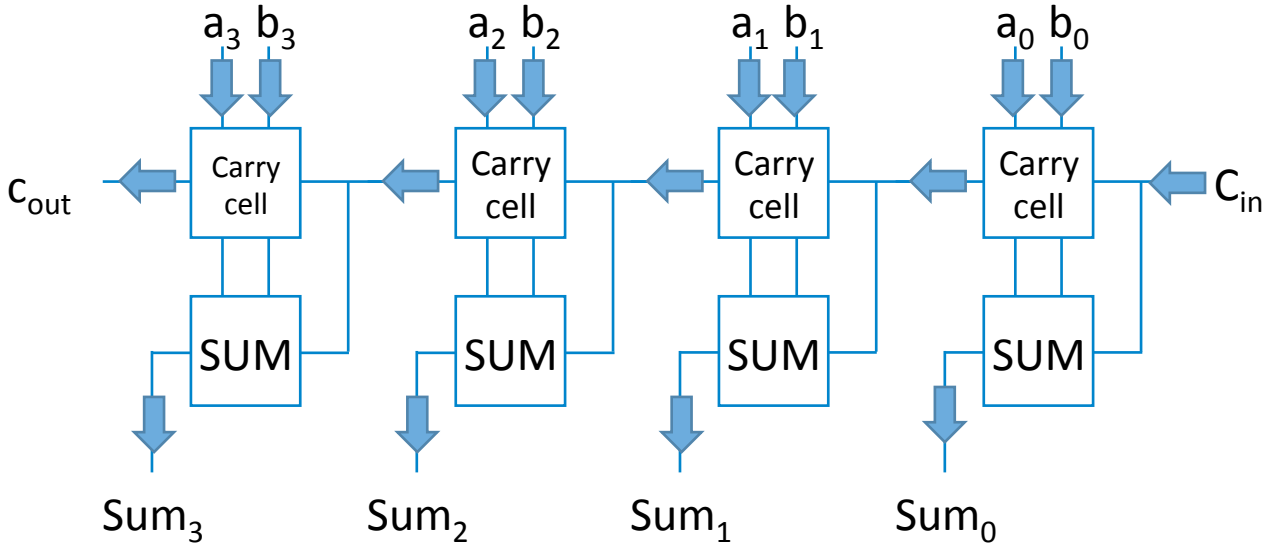
Iterative Logic Array (ILA)



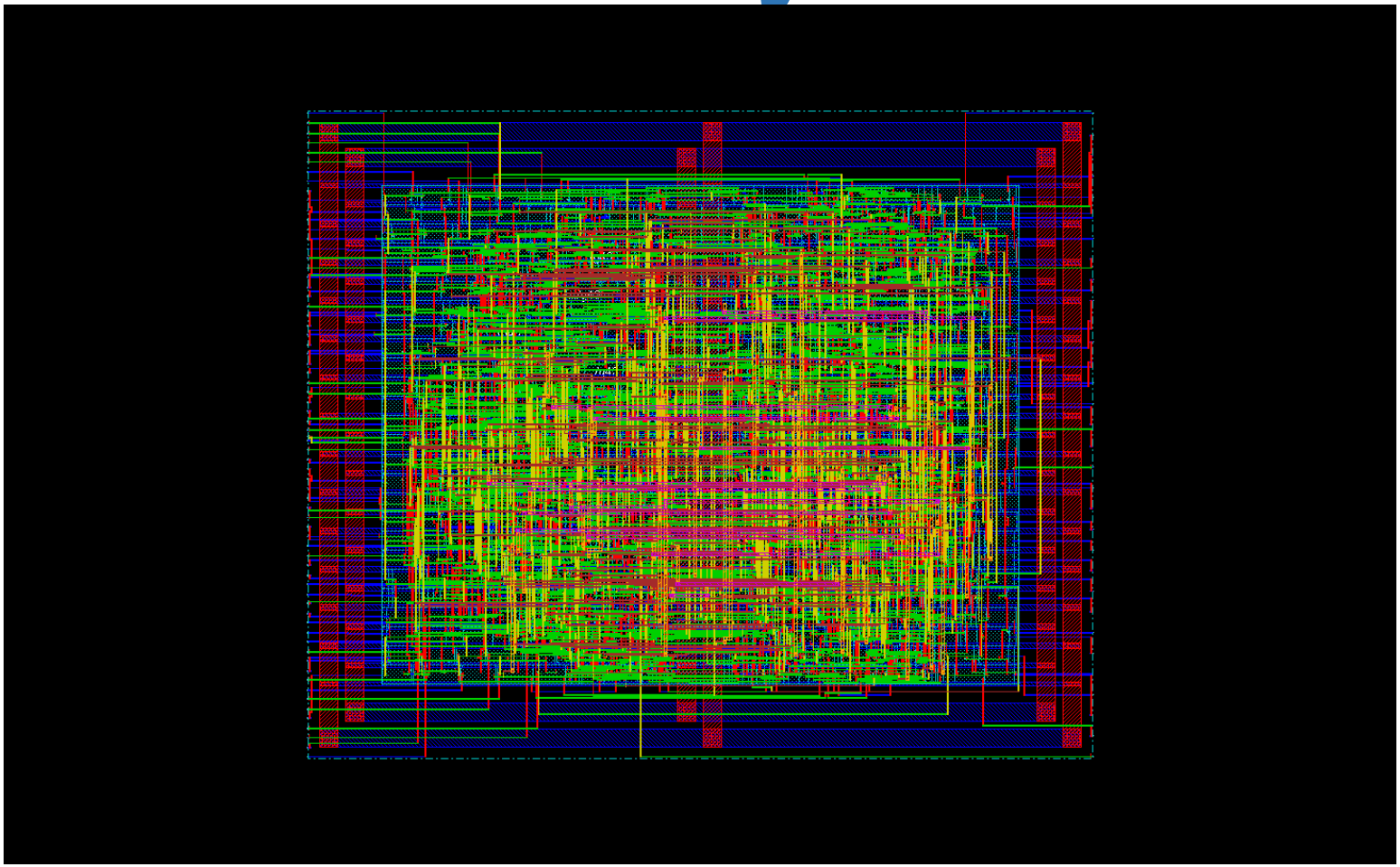
4-bit adder


a3 b3
a2 b2
a1 b1
a0 b0
cout
4-bit adder word slice
Cin
Sum3
Sum2
Sum1
Sum0

4-bit adder


a3 b3
a2 b2
a1 b1
a0 b0
Carry cell
Carry cell
Carry cell
Carry cell
Cout
Cin
SUM
SUM
SUM
SUM
Sum3
Sum2
Sum1
Sum0

Example: synthesized 32-bit ALU layout

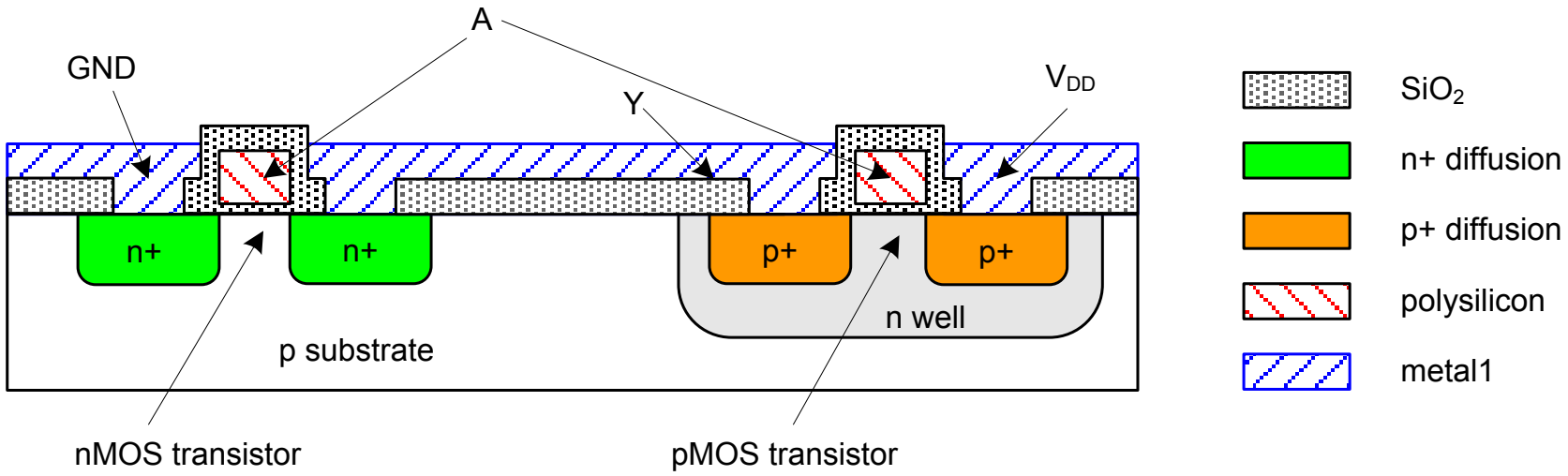


CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

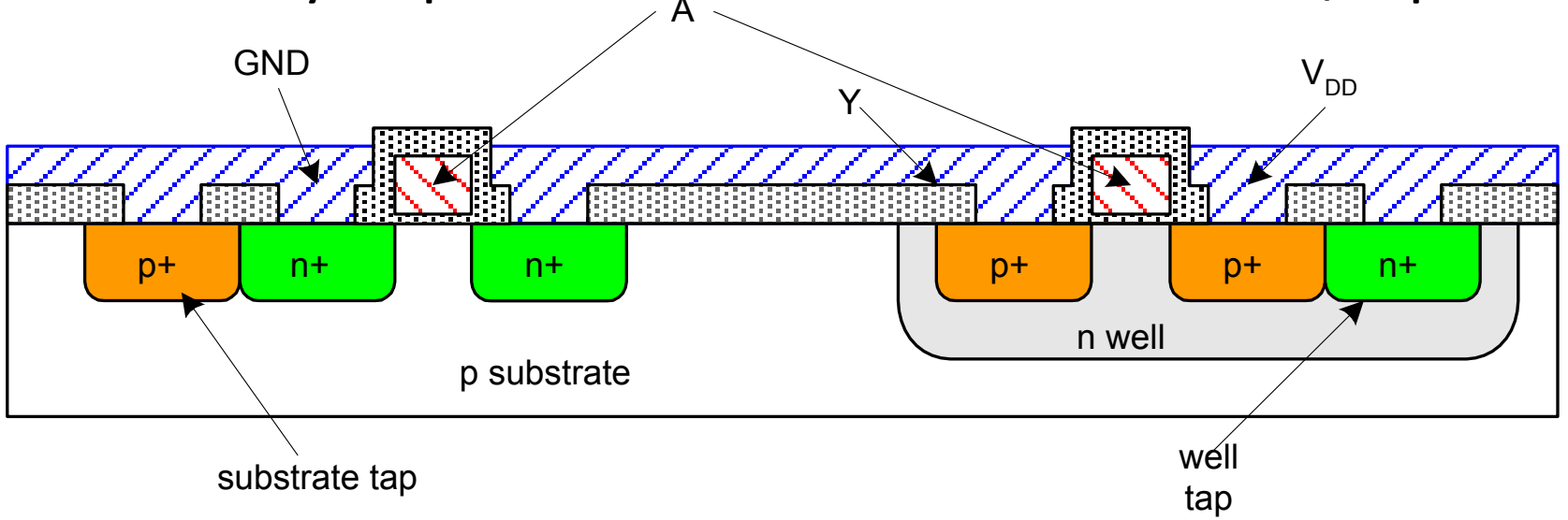
Inverter Cross-section

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors



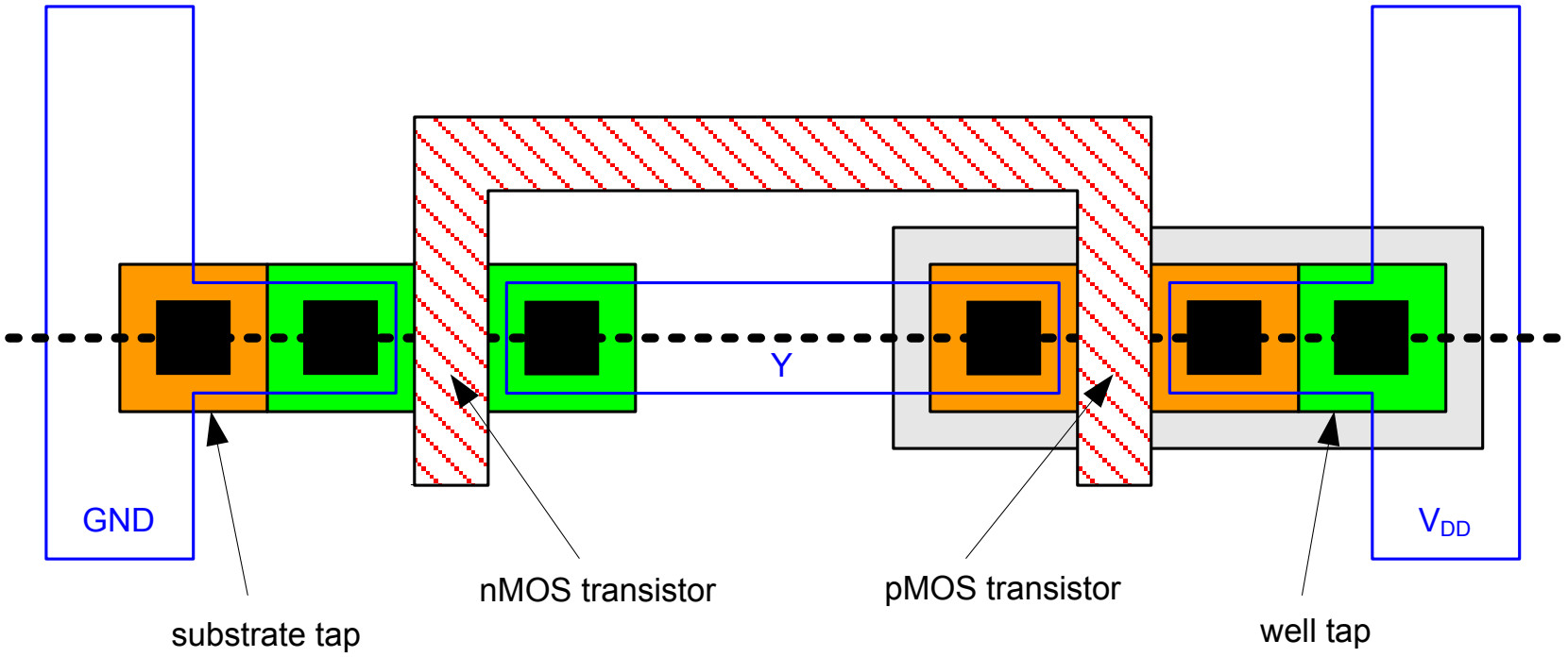
Well and substrate taps

- Substrate must be tied to GND and n-well to V_{DD}
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts/taps

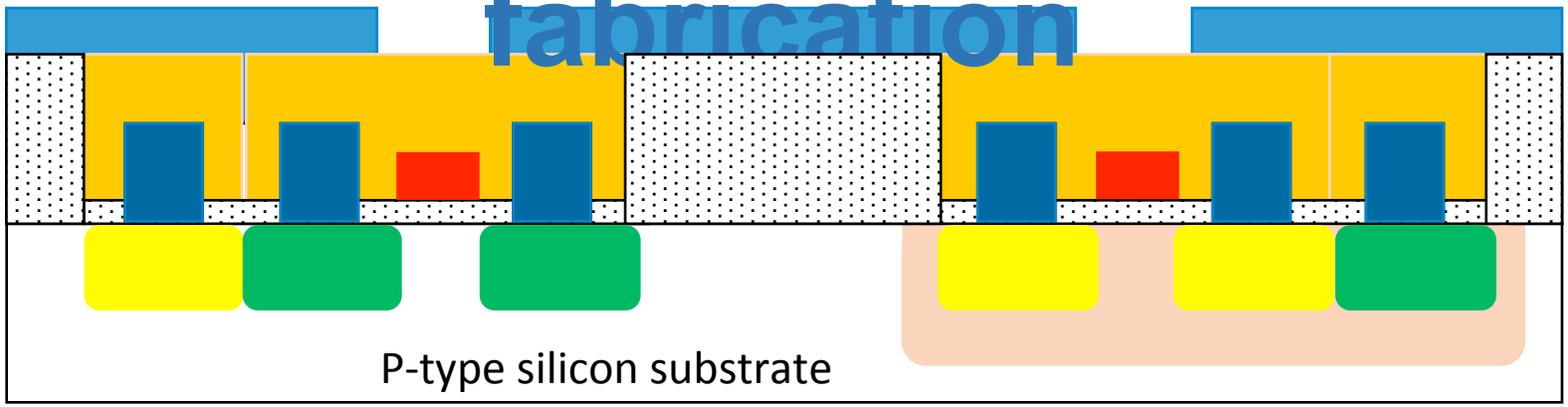


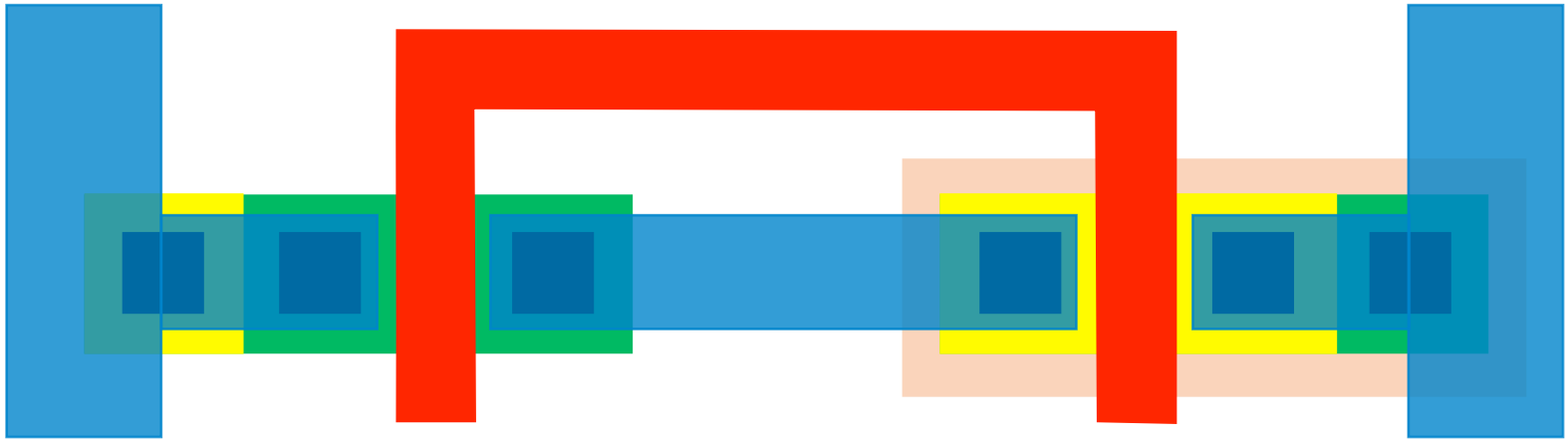
Inverter Mask Set

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



Inverter mask set and fabrication





P+ select

Contact cuts

Metal wires

Poly gate

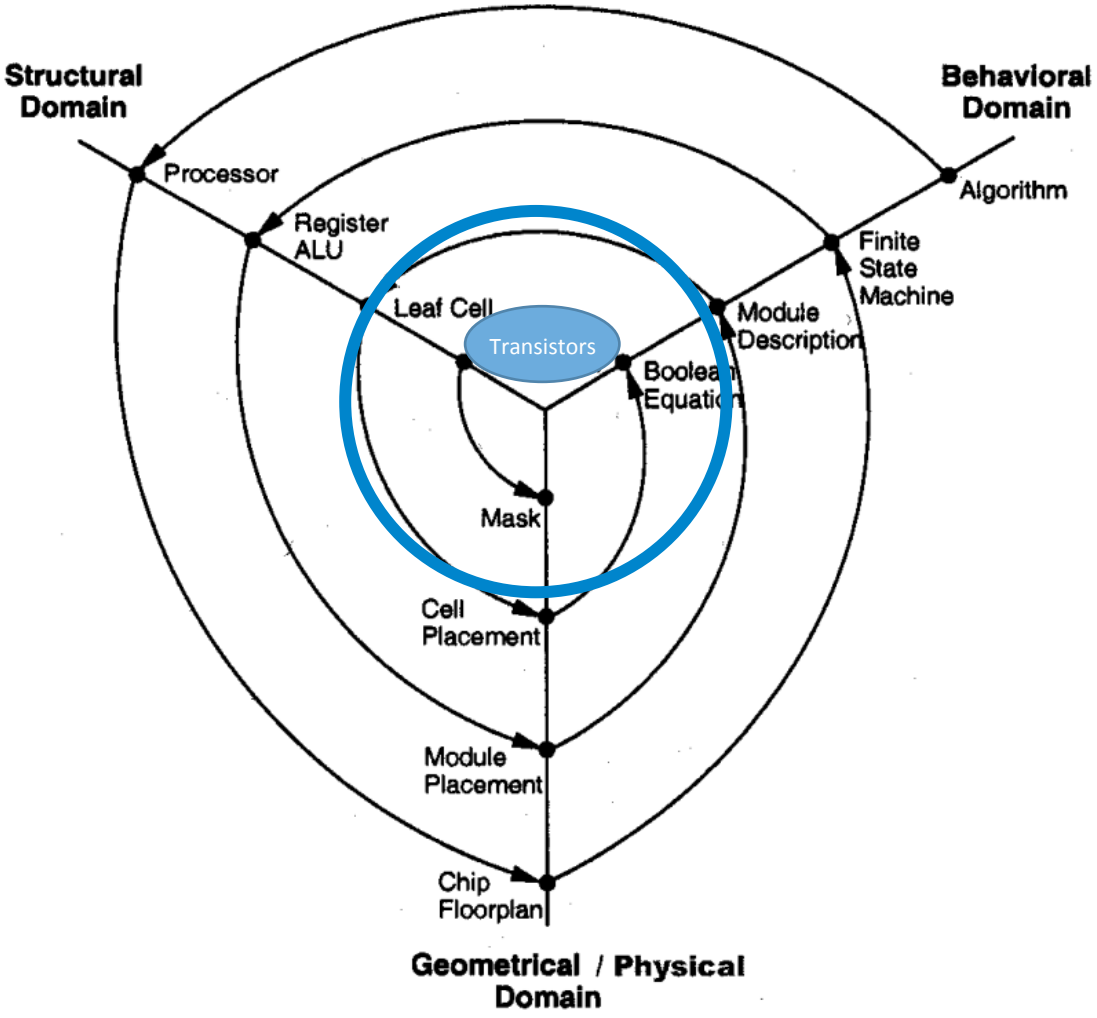
Active areas

N-well

Fabrication

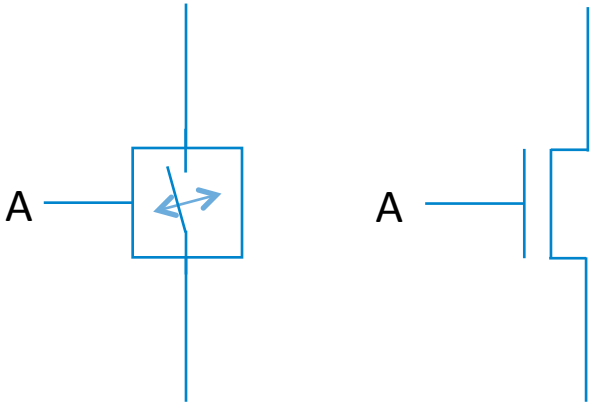
- Chips are built in huge factories called fabs
- Contain clean rooms as large as football fields

Back to the Y-chart



Designing gates with switches

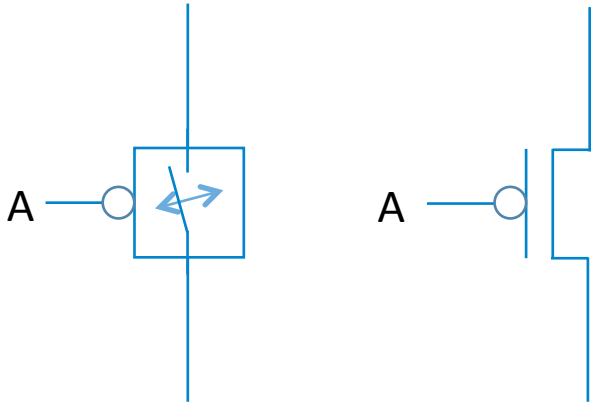
N-switch



nMOSFET

ON when input A is HIGH
OFF when input A is LOW

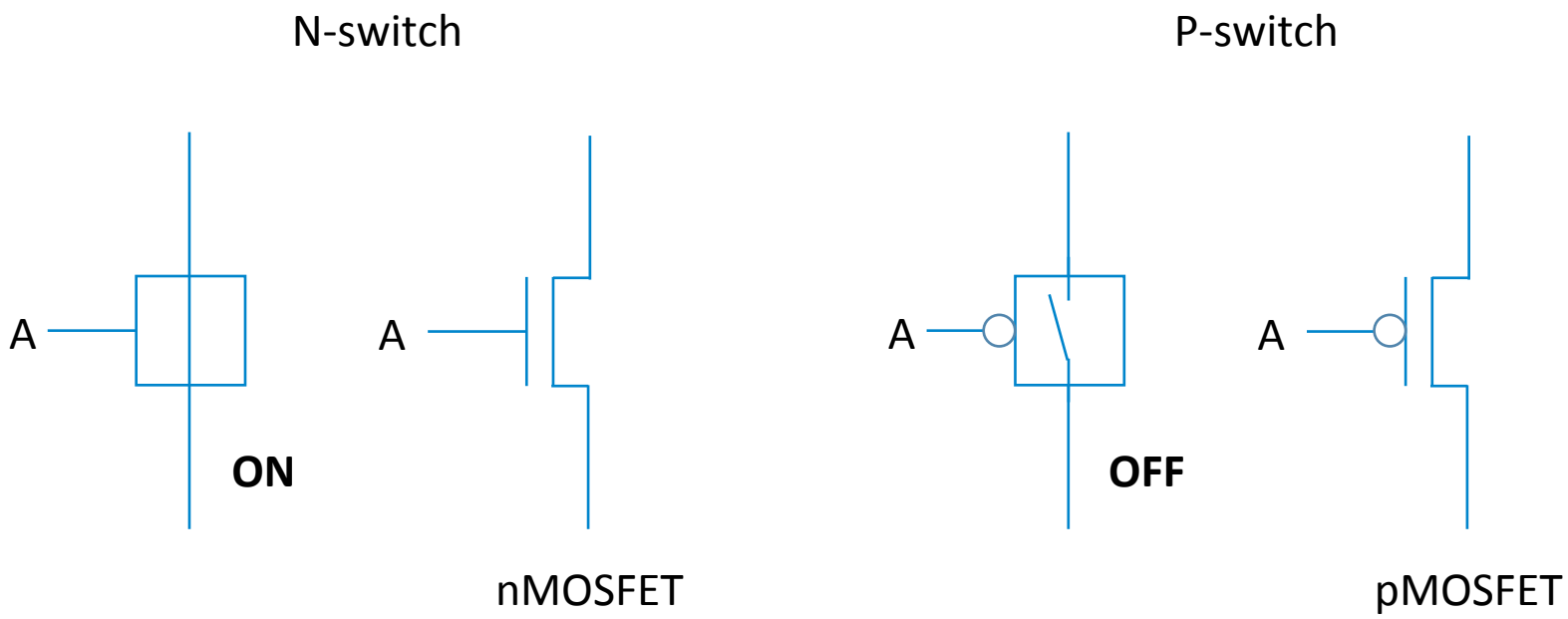
P-switch



pMOSFET

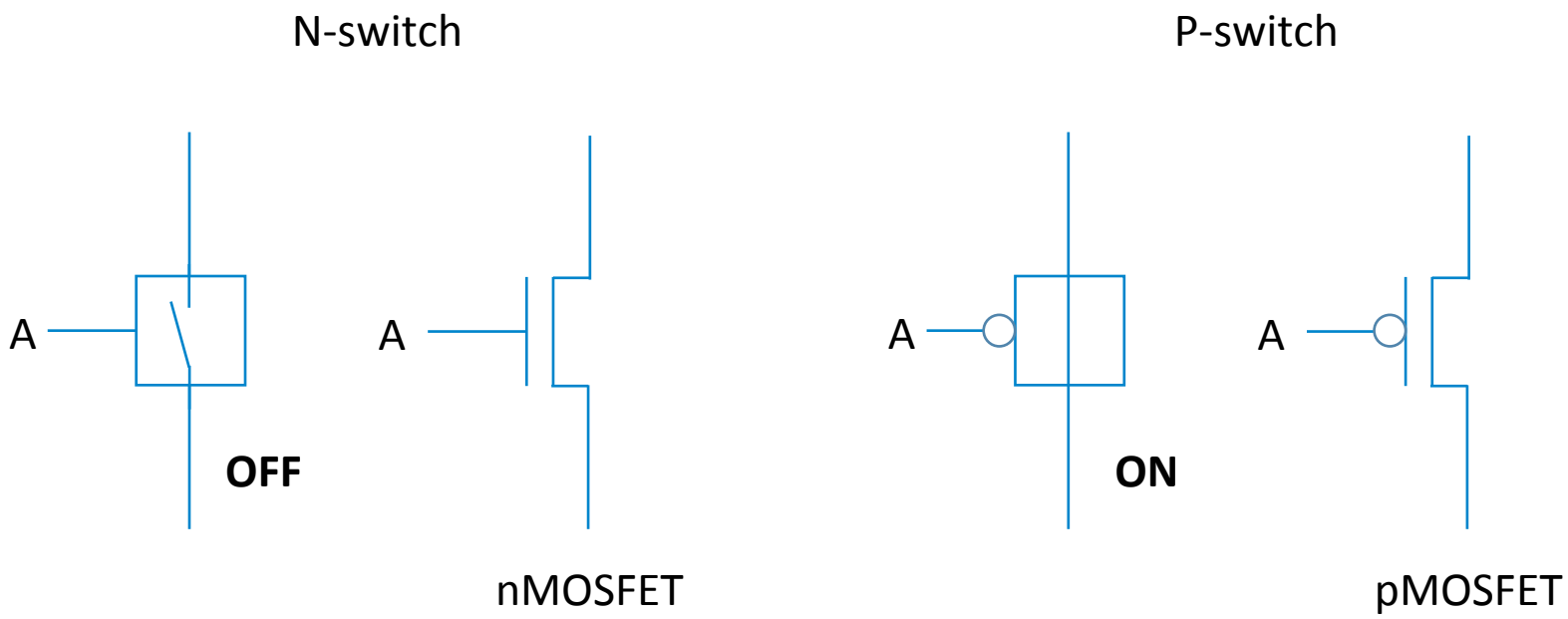
OFF when input A is HIGH
ON when input A is LOW

Designing gates with switches



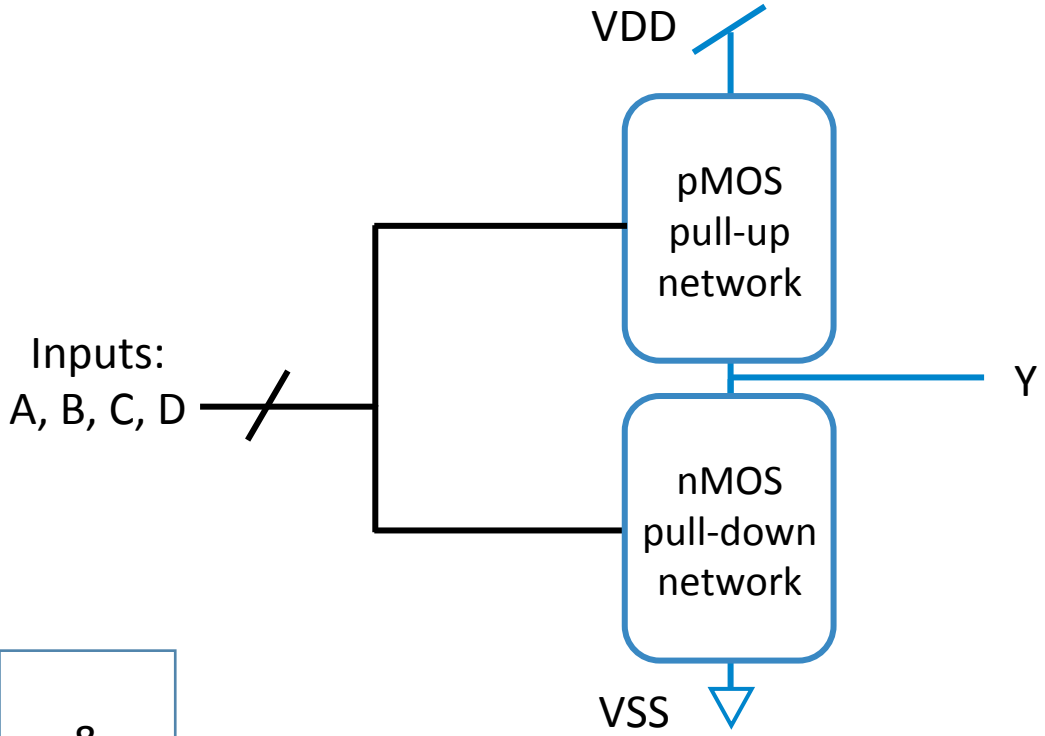
input A is HIGH

Designing gates with switches

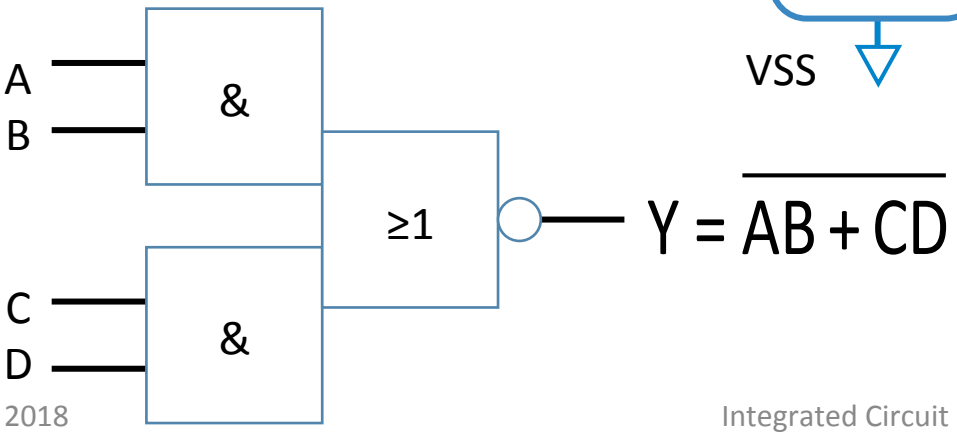


input A is LOW

Designing gates: AOI22

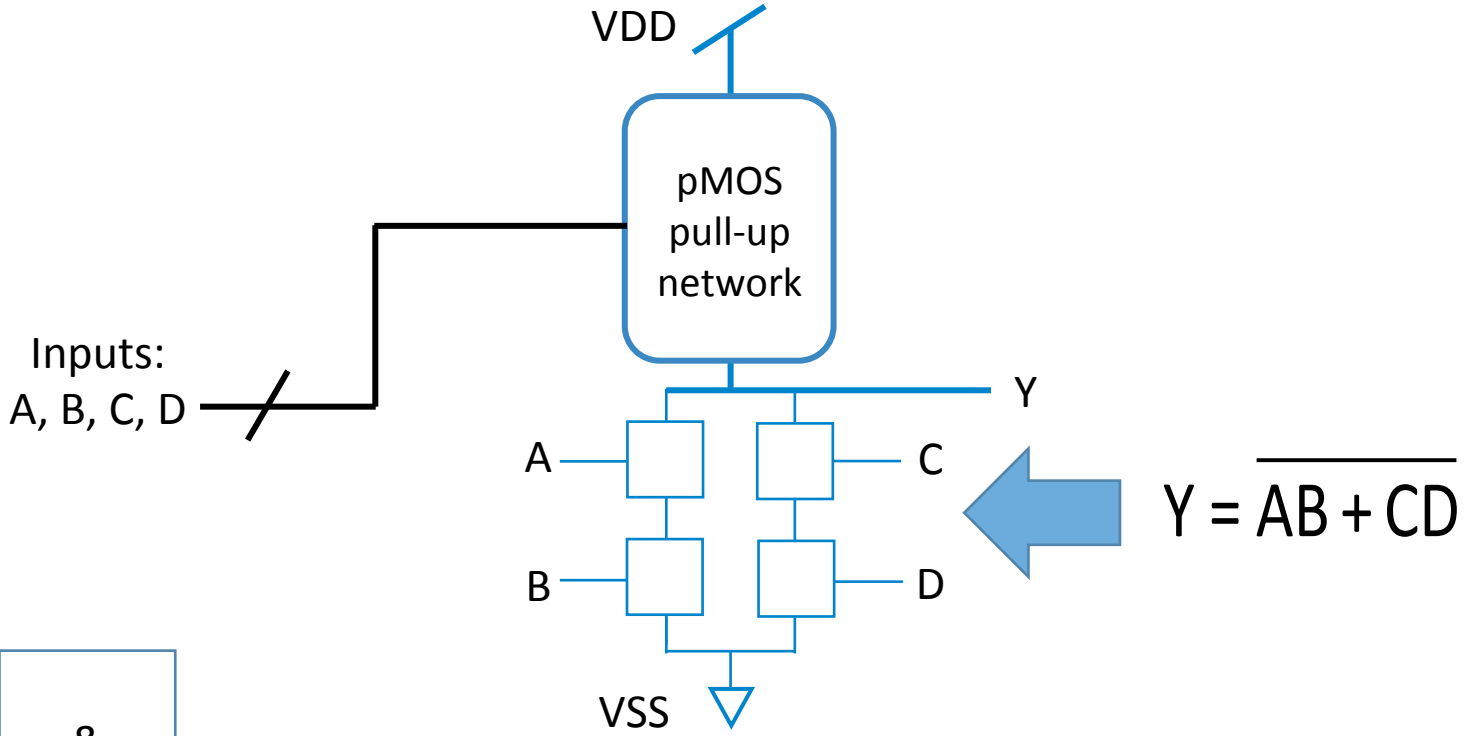


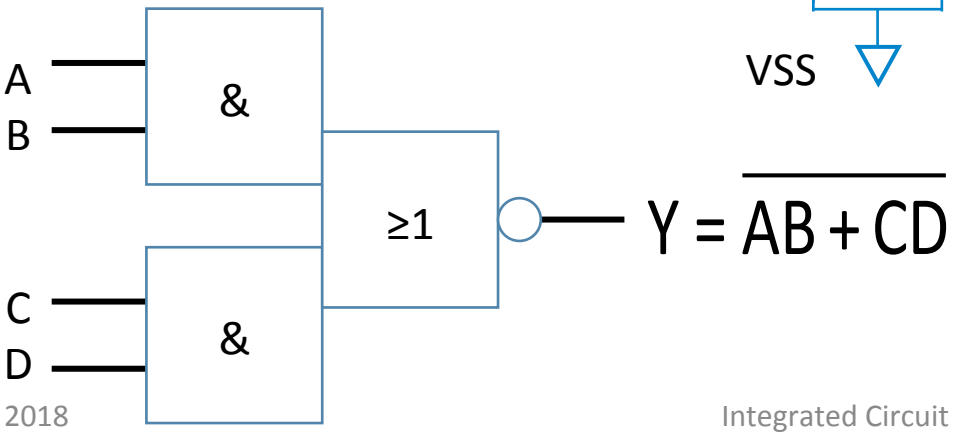
$$Y = \overline{AB + CD}$$



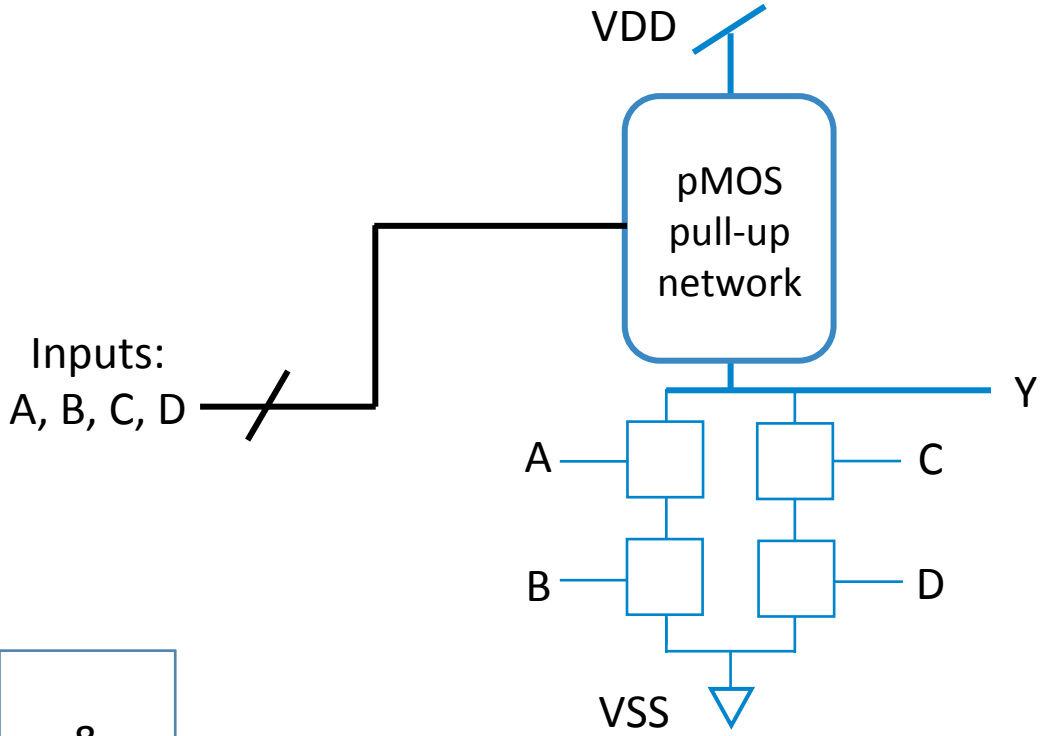
$$Y = \overline{AB + CD}$$

Designing gates: AOI22





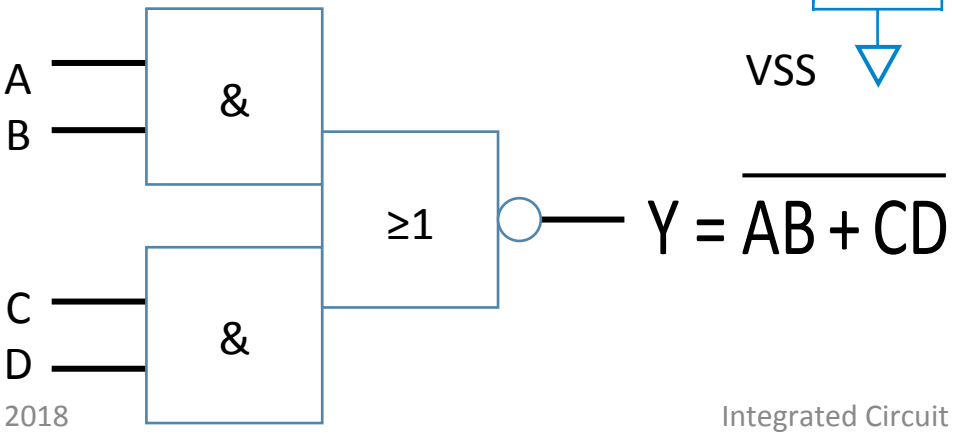
Designing gates: AOI22



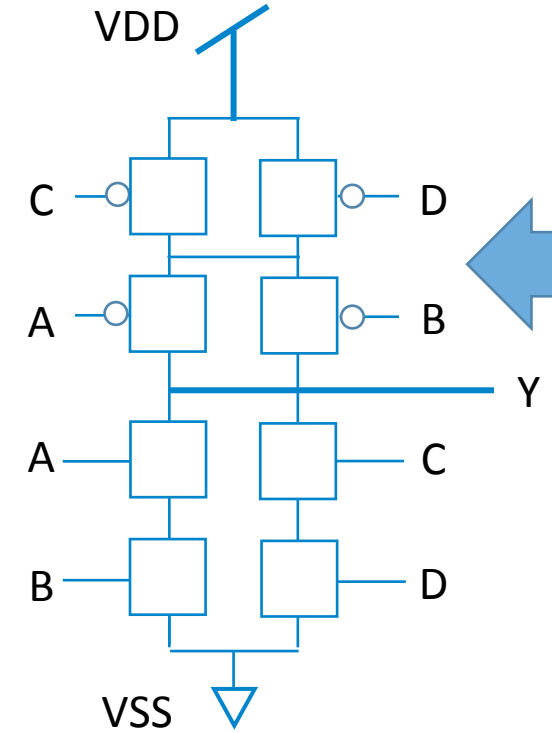
According to de Morgan´s theorem

$$Y = \left(\overline{A} + \overline{B}\right)\left(\overline{C} + \overline{D}\right)$$

$$Y = \overline{AB + CD}$$

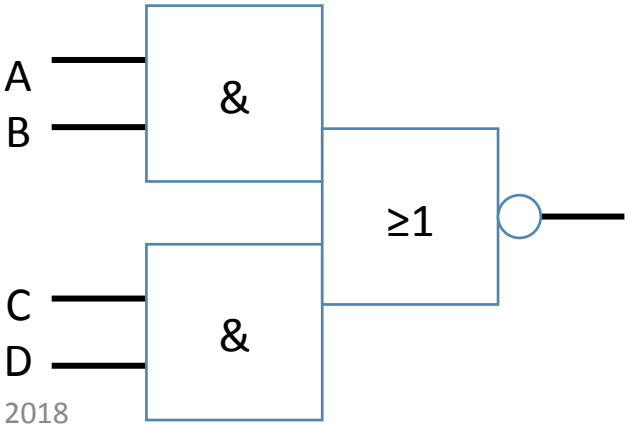


Designing gates: AOI22



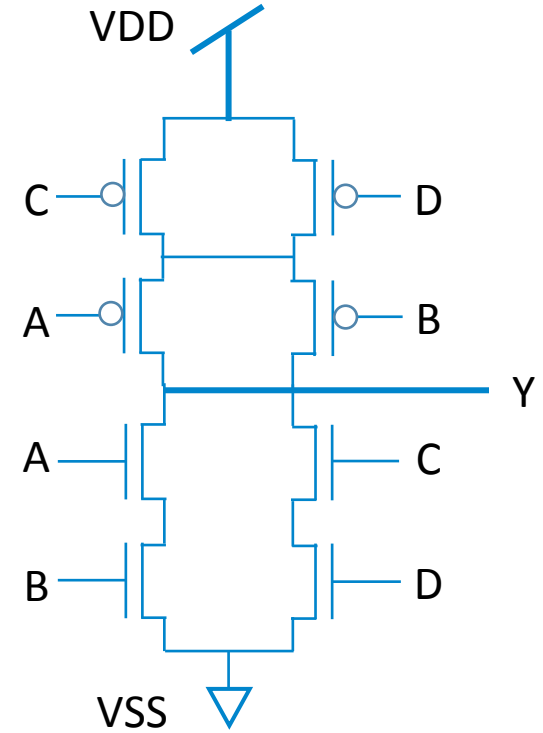
$$Y = \left(\overline{A} + \overline{B}\right)\left(\overline{C} + \overline{D}\right)$$

$$Y = \overline{AB + CD}$$



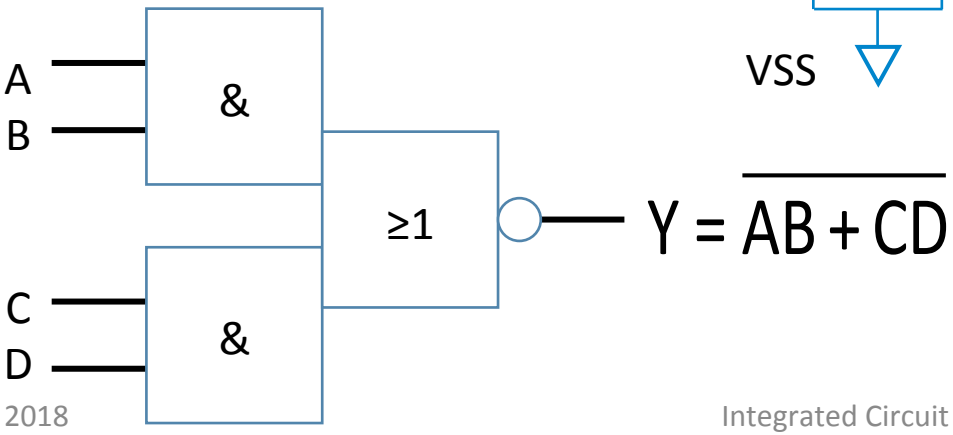
$$Y = \overline{AB + CD}$$

Designing gates: AOI22



$$Y = \left(\overline{A} + \overline{B}\right)\left(\overline{C} + \overline{D}\right)$$

$$Y = \overline{AB + CD}$$



Simple CMOS gates

The Inverter

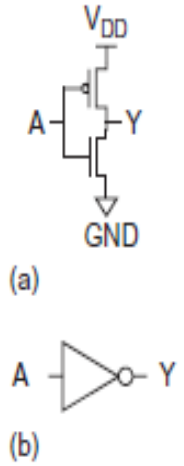


FIGURE 1.11 Inverter schematic (a) and symbol (b) $Y = \overline{A}$

TABLE 1.1 Inverter truth table

A	Y
0	1
1	0

The NAND Gate

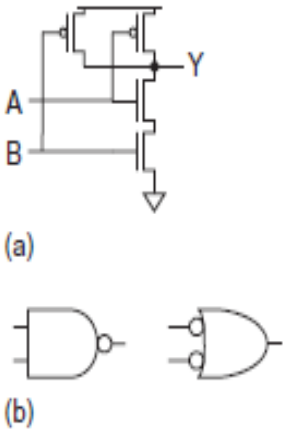


FIGURE 1.12 2-input NAND gate schematic (a) and symbol

$$Y = \overline{AB} = \overline{A} + \overline{B}$$

TABLE 1.2 NAND gate truth table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

The NOR Gate

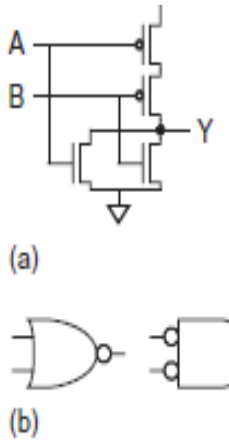


FIGURE 1.16 2-input NOR gate schematic (a) and symbol

$$Y = \overline{A + B} = \overline{A} \, g \overline{B}$$

TABLE 1.4 NOR gate truth table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Exercise: AOI21 AOI31, OAI22
Derive gate from Karnaugh map

End of CMOS design lecture!

Q & A?