Postlab lab 4

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Course evaluation

- We will try "earlier questionnaire" this year to enhance number of replies.
- Questionnaire available Oct 17 - Nov 5
- You will be able to fill it in in class on Oct 19.
  - Laptop or mobile phone both work.
  - Link via e-mail.
- You can adjust your replies until the Nov 5.
- Course evaluation meeting in mid-November.

In context

Learning outcomes

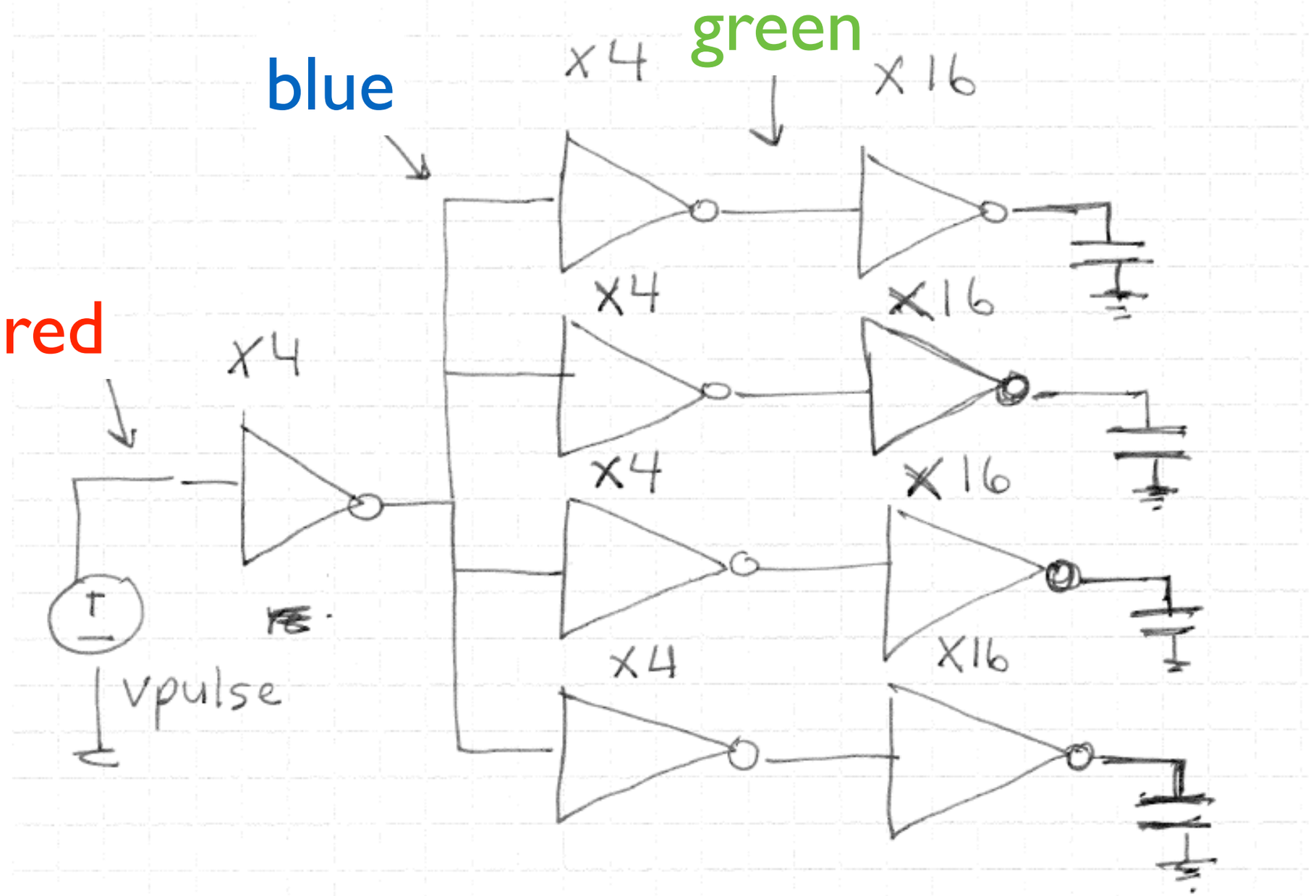
- design static CMOS logic gates (pull-up and pull-down networks) and implement these as standard cells.
- from simple MOS transistor models, estimate static and dynamic properties of CMOS inverters and use these properties to model more complex gates.
- derive logical-effort normalized-delay parameters from circuit diagrams or layout, and use these parameters to estimate and trade off performance measures such as critical-path delays and power dissipation in present and future CMOS technologies.
- find critical paths in more complex combinatorial circuits, such as adders, and determine and minimise their delays.
- analyse wire-delay-dominated cases such as clock distribution and global interconnect, and suggest suitable buffering schemes to minimize delay or delay spread.
- design simple sequential systems that meet set-up and hold time constraints for timing circuits, including the effect of metastability in synchronisation.,
- use industrial-type design automation tools to design, implement and verify basic CMOS circuit elements following the design flow supported by such tools.

What does “in context” mean?

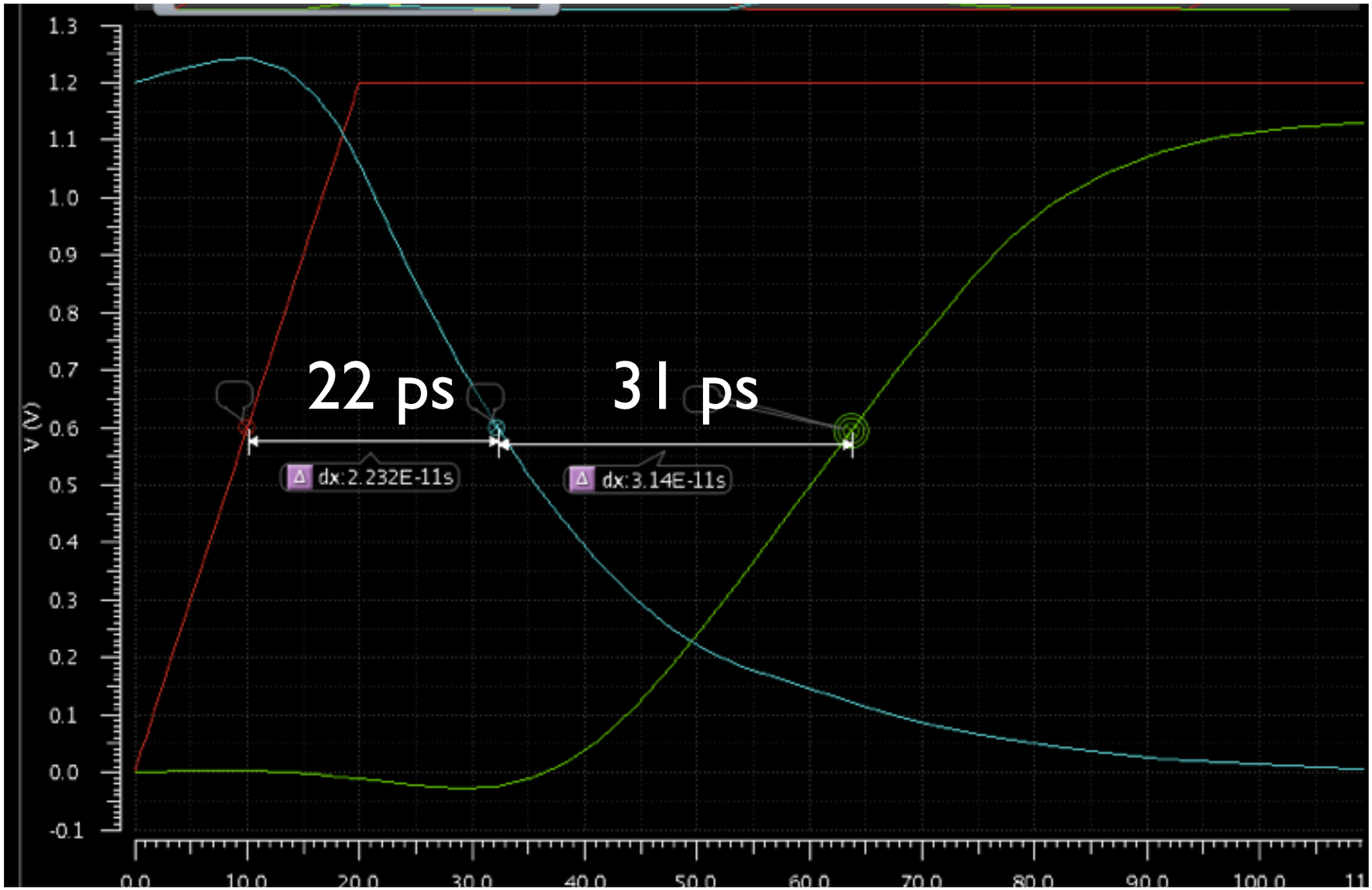
- All information may not be readily available. May have to deduce it from data, graph or assume something reasonable.
- The problem often has to be “extracted” from its context to make it “clean”.
- You have to decide which method to use.
- There may not be one “right answer”.

Why is the measured delay in the tapered buffer longer than the calculated one?

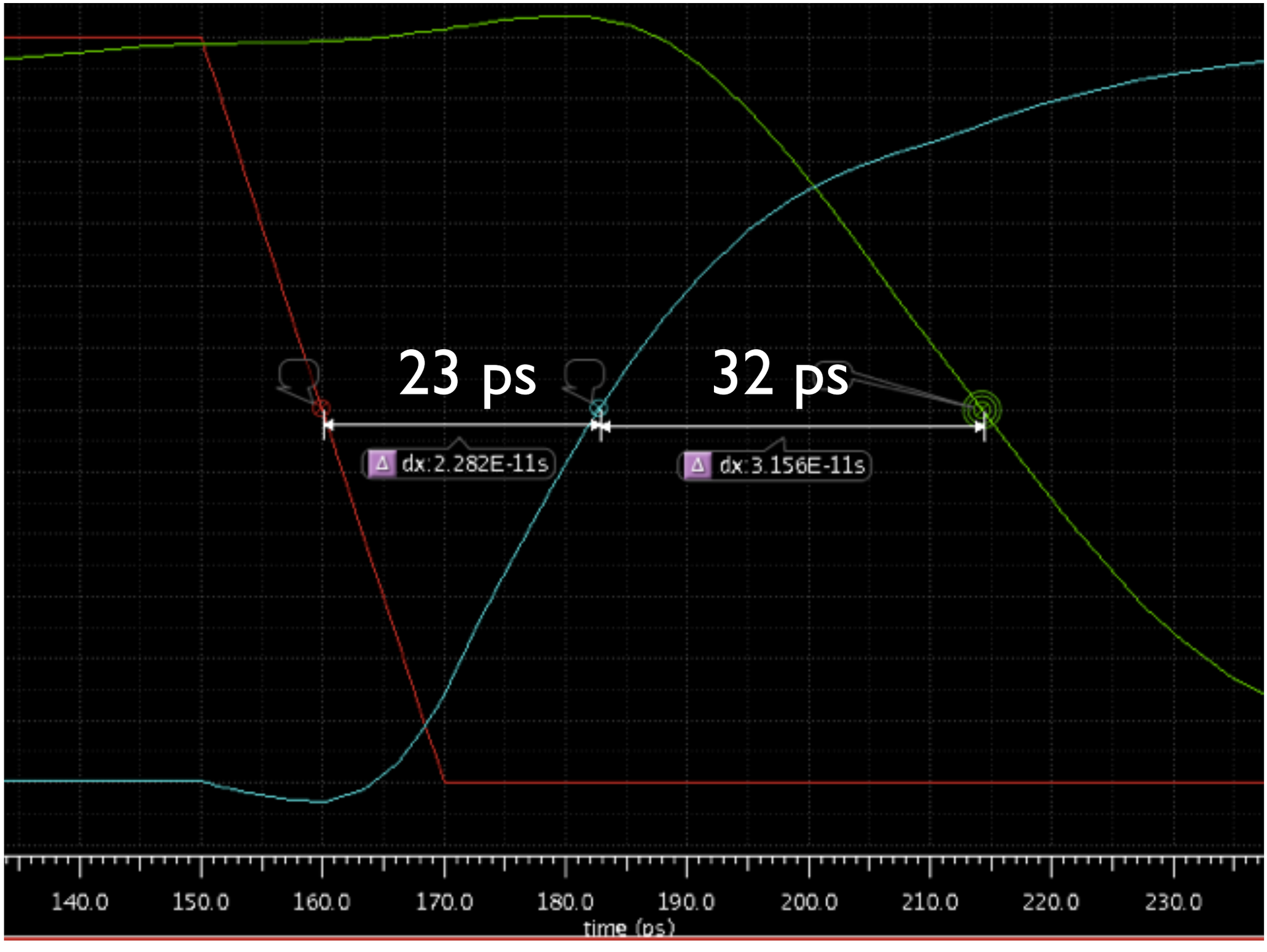
FO4 experiment revisited



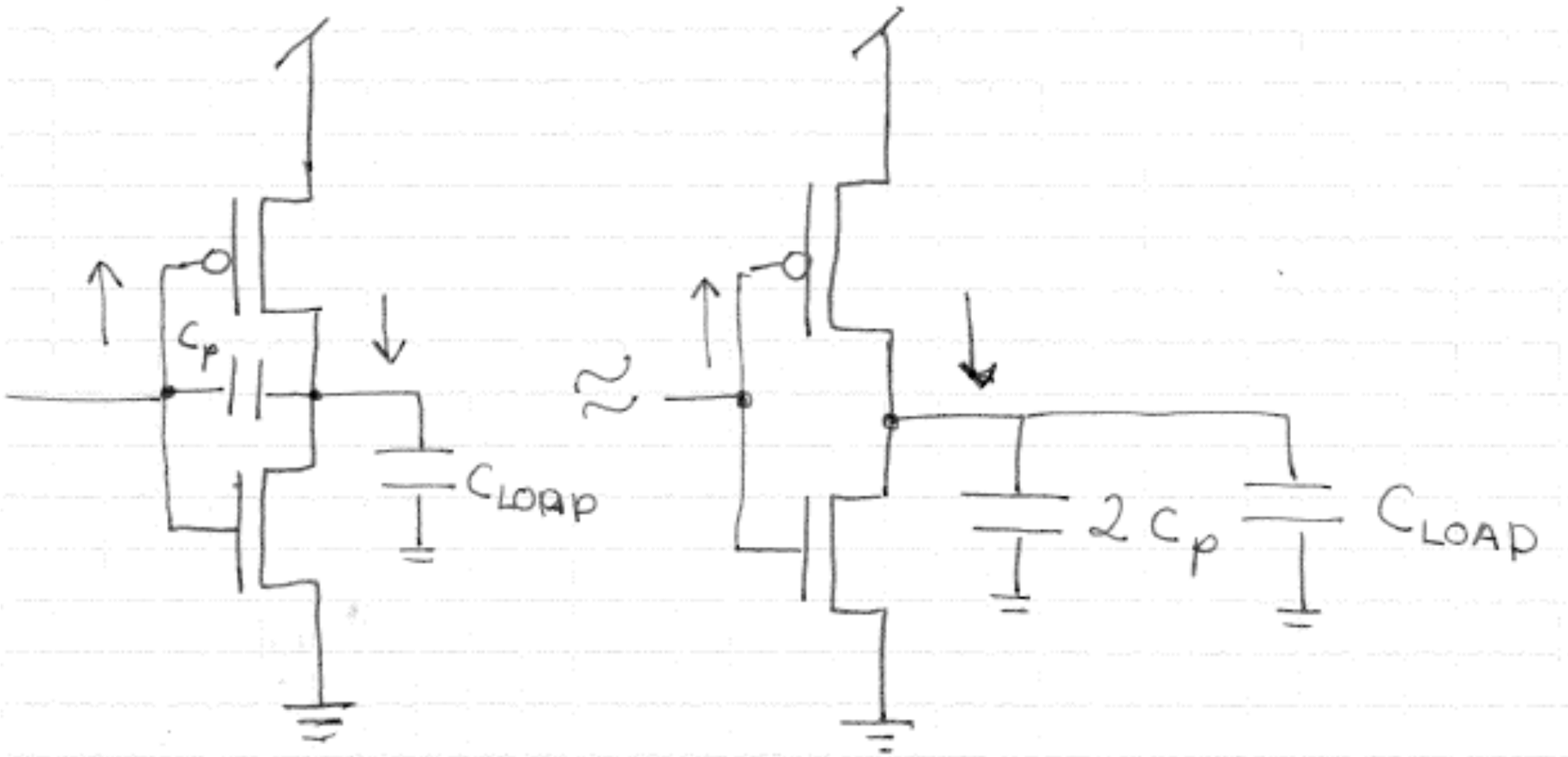
FO4 experiment revisited



FO4 experiment revisited



Miller effect or bootstrapping



When inverter is driven by voltage source which can deliver infinite current this effect does not show.

See W&H section 4.4.6.6

Global clock distribution: H-tree

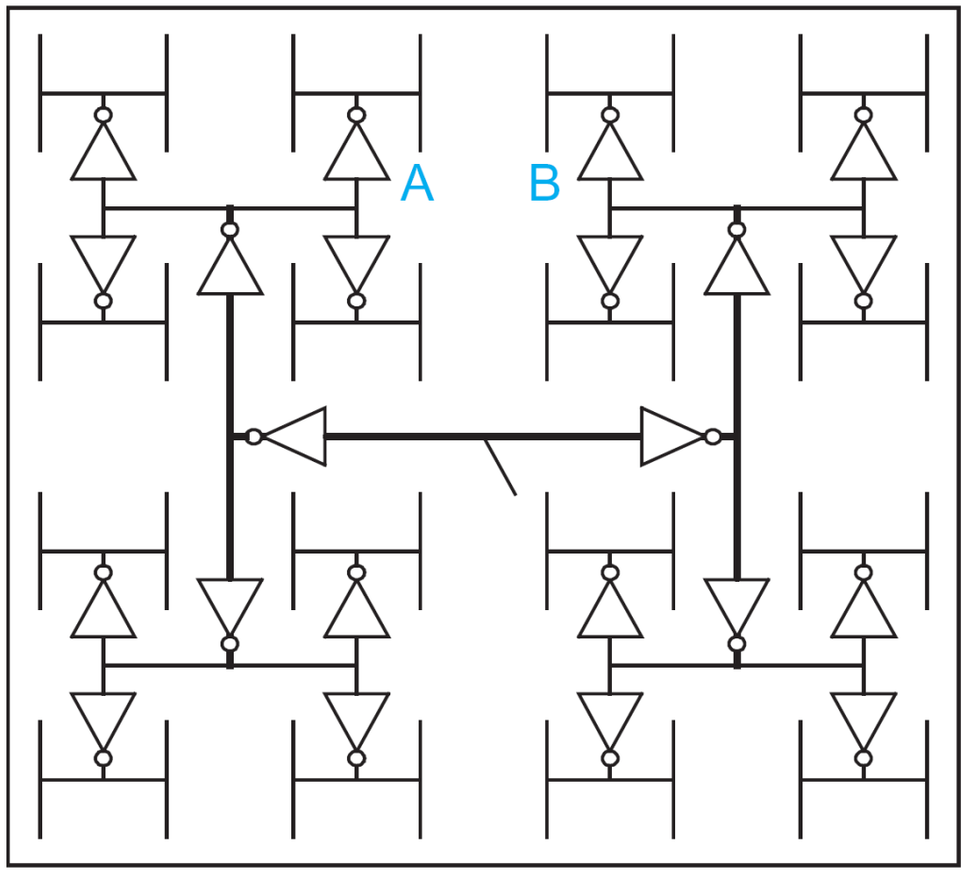


FIGURE 13.24 H-tree

Can you think of a problem for A & B in this H-tree?

A & B can have quite large clock skew due to being in diffrent half trees.