Geometric Design Rules

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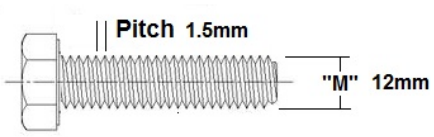
Aim of the lecture

- To give some basic understanding of intralayer and interlayer geometric design rules
  - Intralayer rules concerns minimum dimensions and spacing between objects in **the same** layer
  - Interlayer rules concerns minimum spacing and overlap rules between objects in two **different** layers:
    - MOSFET rules between poly and active
    - Contact and via rules between contacts or vias to their bottom and top contacting layers
- Discuss the prelab assignment for the layout lab session

Why rules?

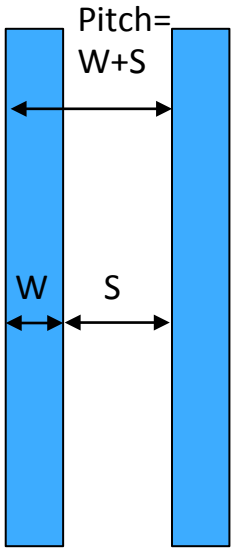
- To minimize the risk of faulty circuits after fabrication.
  - Malfunction due to shorts
  - Improper forming of components or contacts
  - Electrical charging during fabrication.
- More complex nowadays due to:
  - Smaller feature sizes
  - More complex fabrication processes
    - For example polishing for each metal layer

Geometric design rules



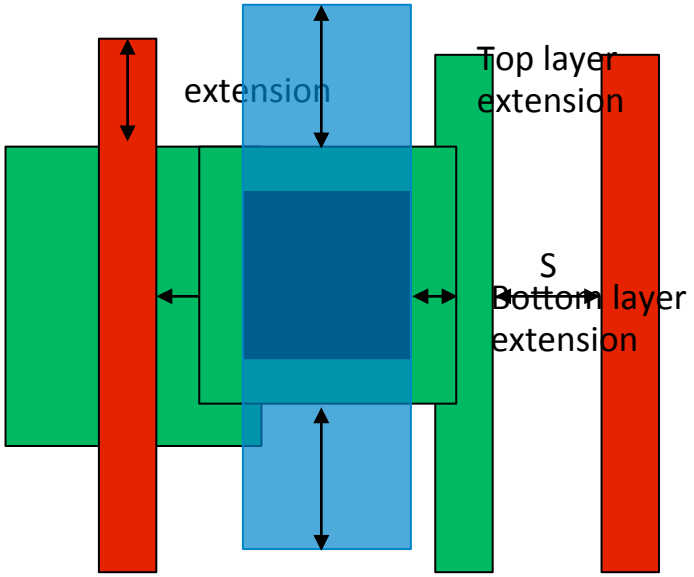
Bolt identification
"M"Dia*Pitch

M12*1.5



Interlayer rules

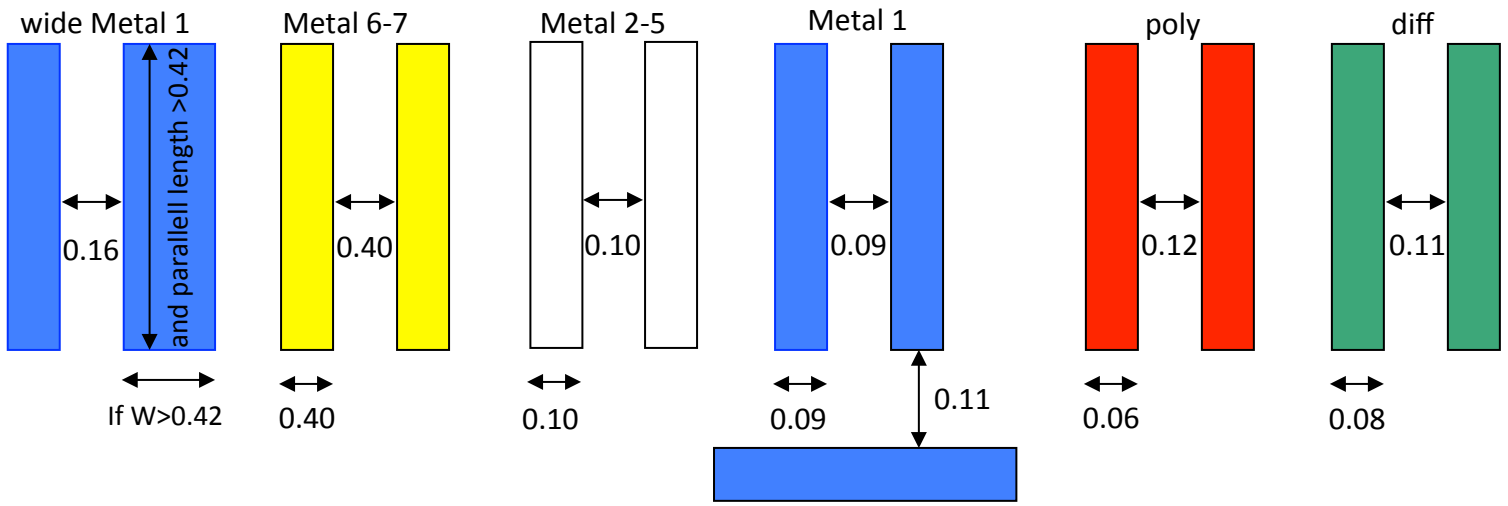
Contacts and vias



pitch = width + separation

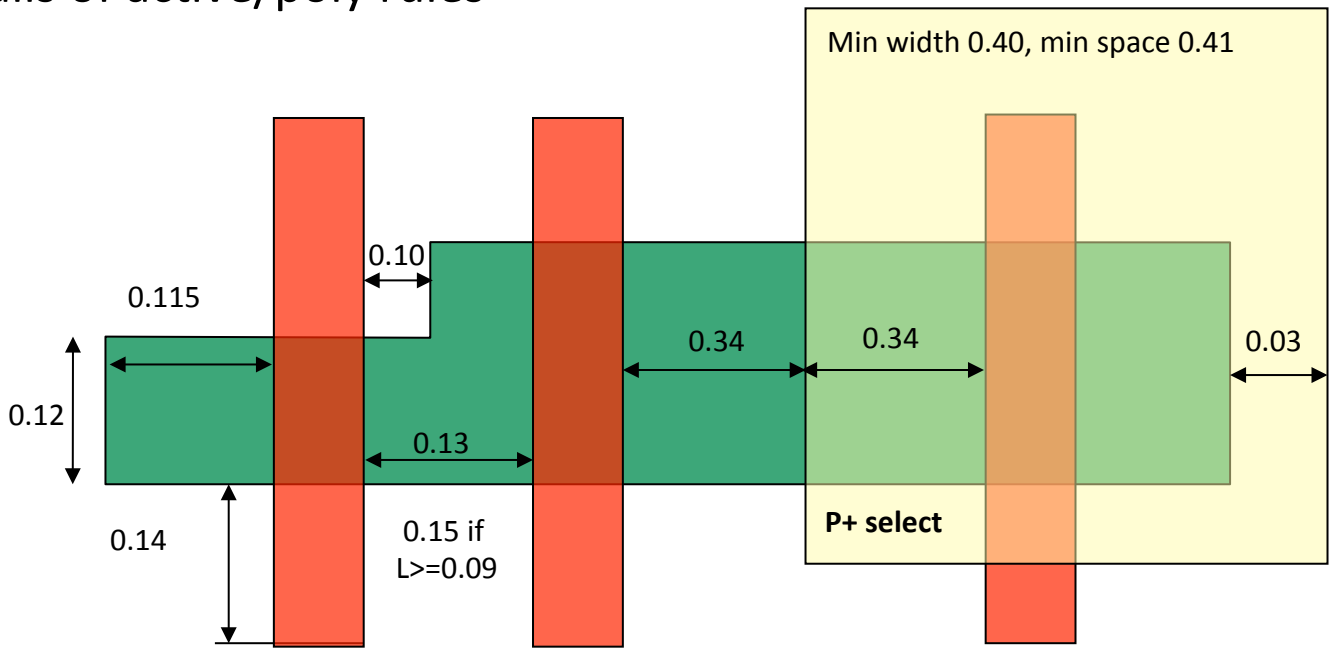
Geometric design rules

Intralayer rules



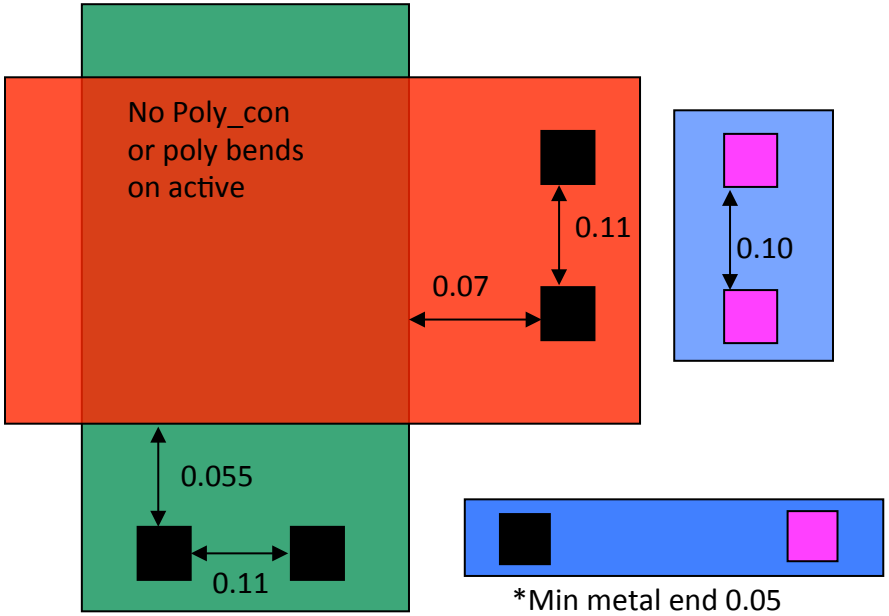
Geometric design rules

Details of active/poly rules



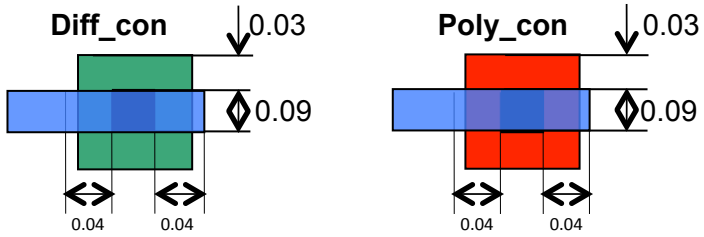
Geometric design rules

Contact and via rules



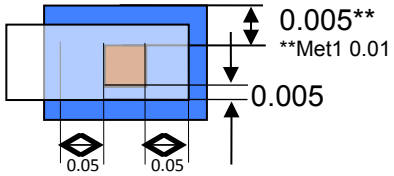
Geometric design rules

Contact and via rules



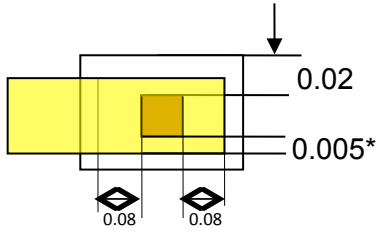
For minimum width metal lines at least 0.04 enclosure is required on two opposite sides (bottom measures).

Via 1-4: 0.10x0.10

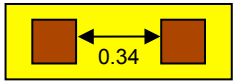


At least two 0.05 metal ends on metal pad

Via 5-6: 0.36x0.36



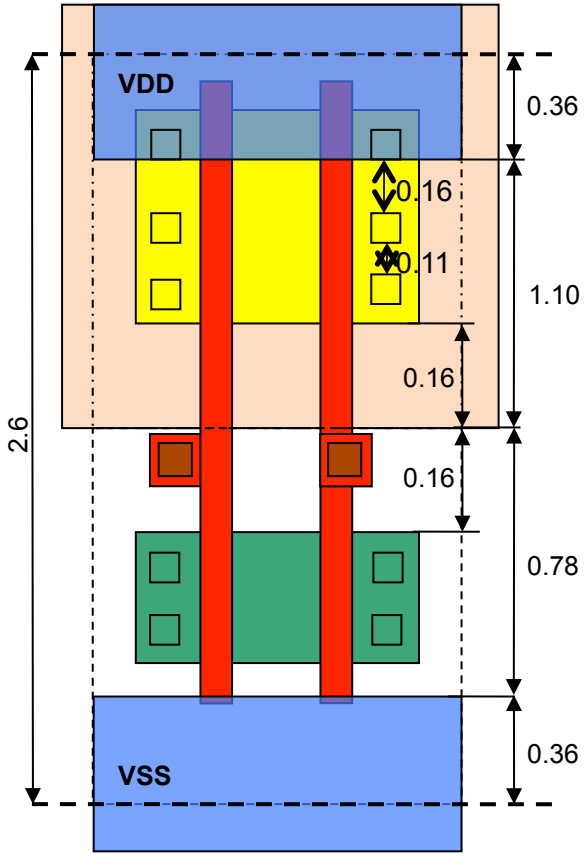
At least two 0.08 metal ends on metal pad



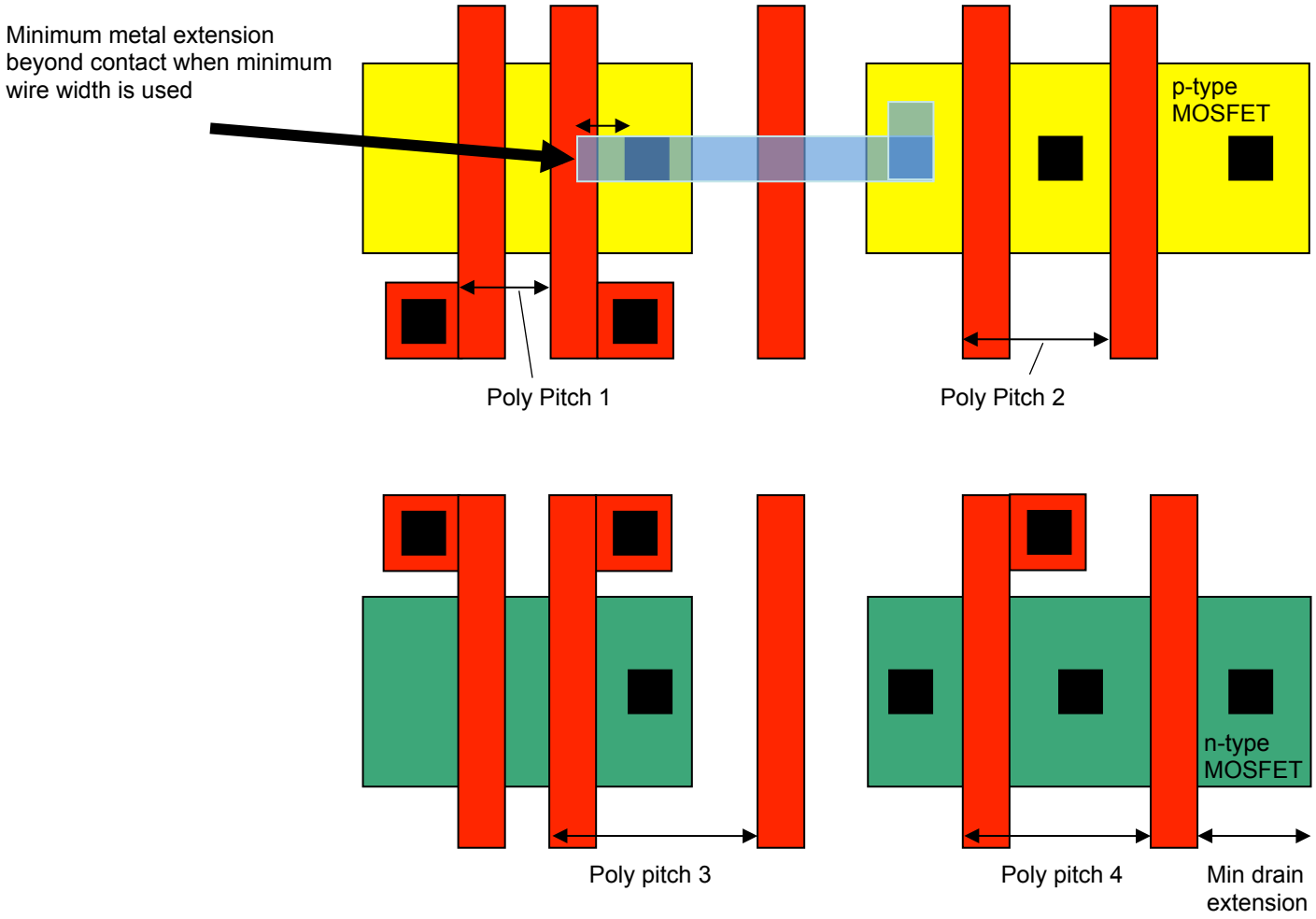
(min 0.54 in array)

Geometric design rules

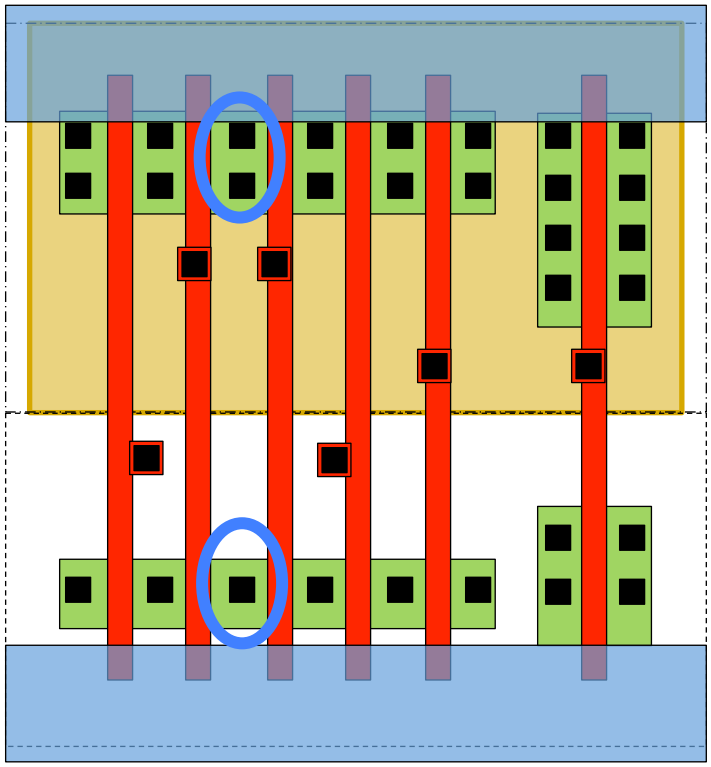
Standard cell template
with rails, n-well, pplus and nplus design rules

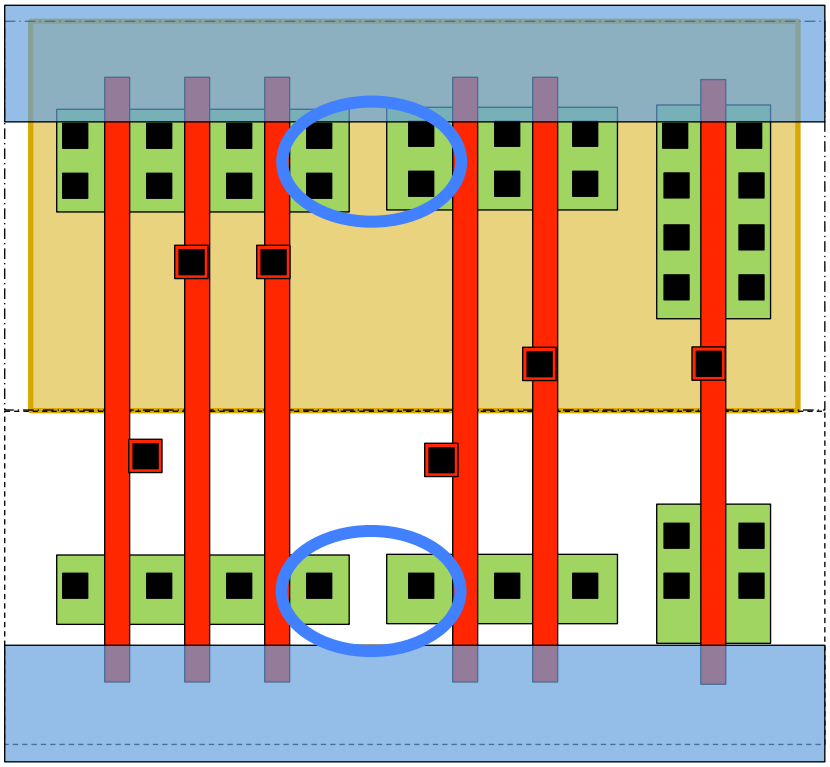


Prelab 3 assignment

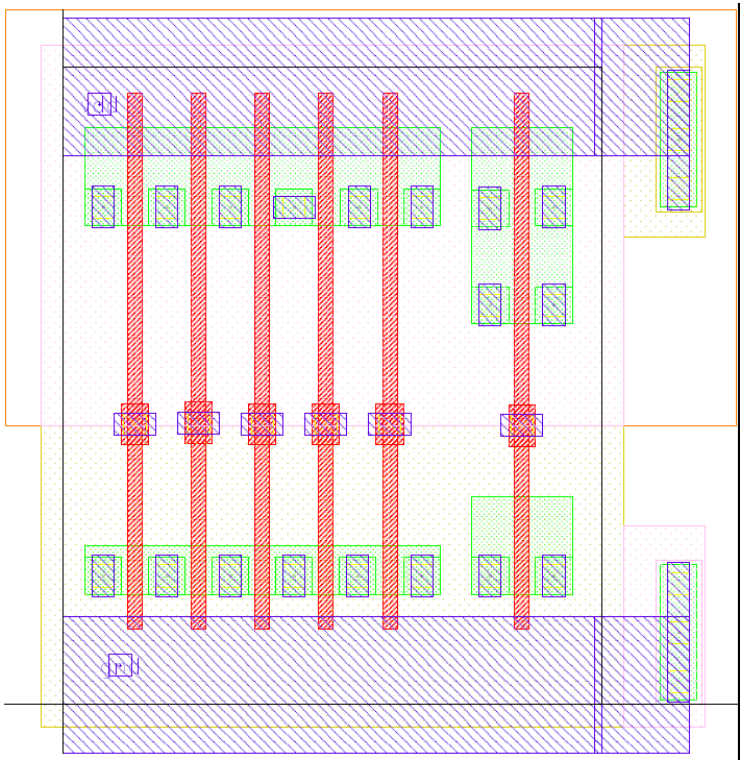


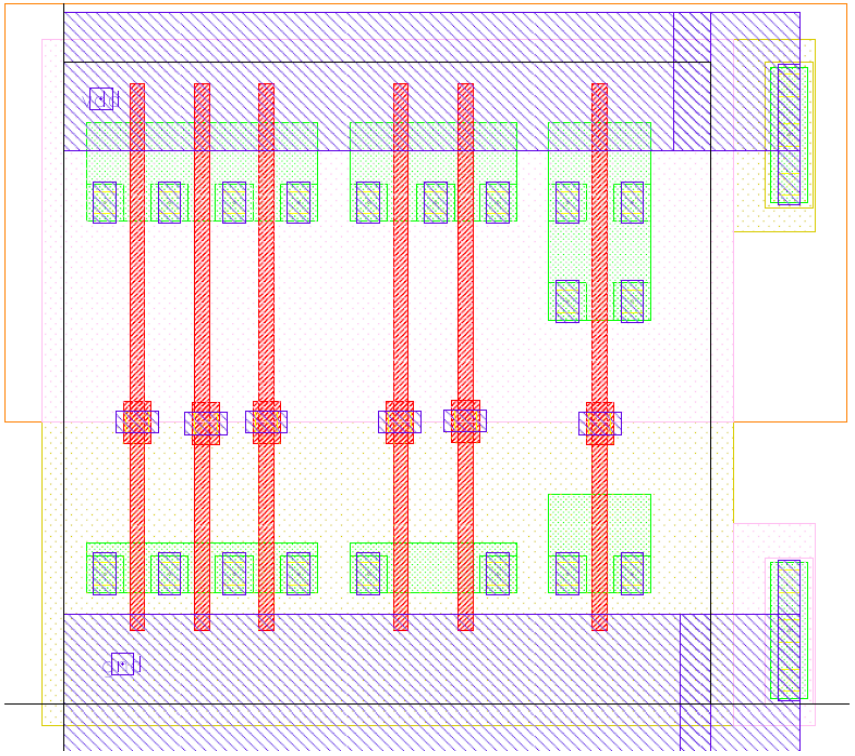
Prelab 3 layout templates





Prelab 3 layout templates

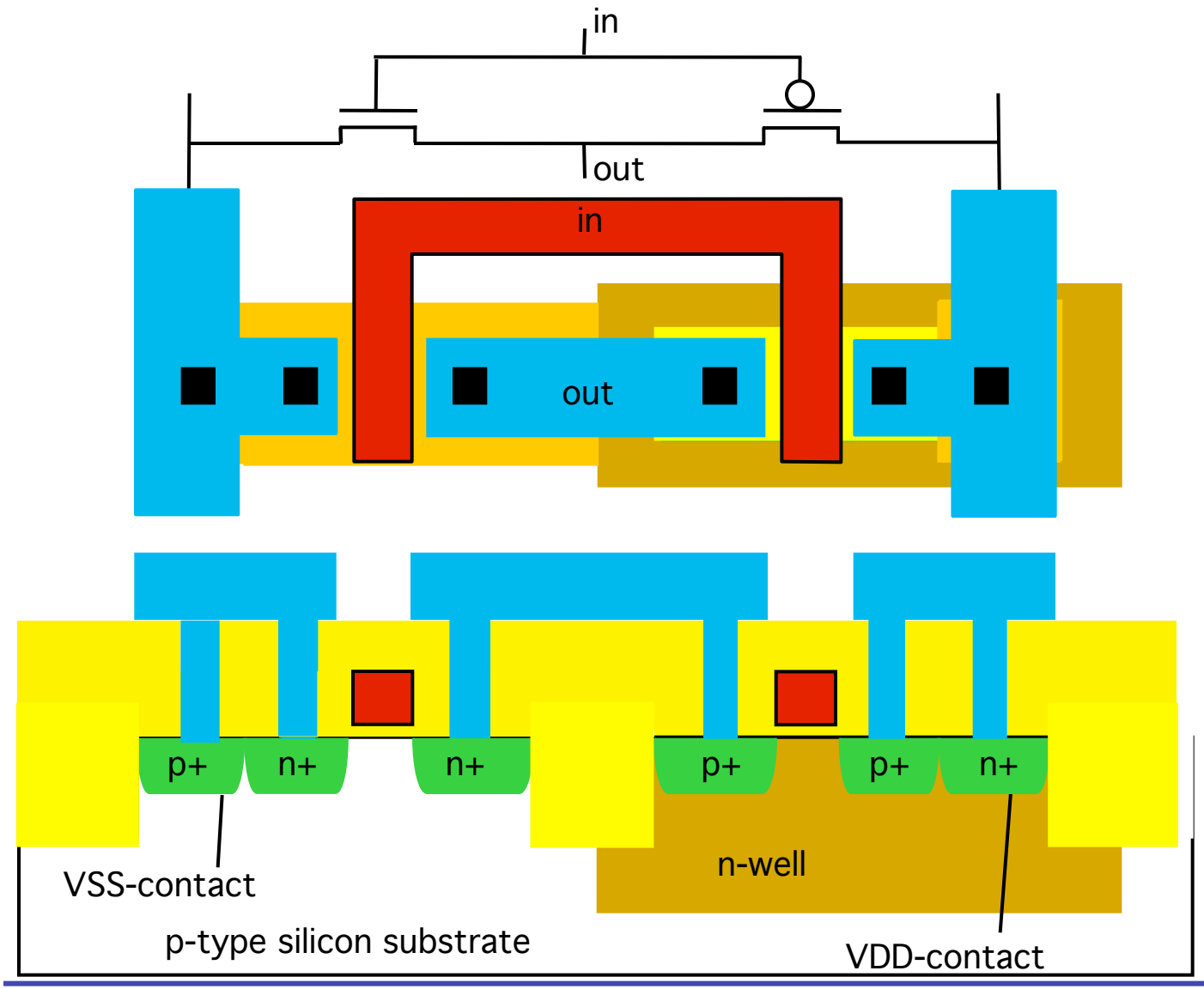




The layers

- **Physical layers** in your layout:
  - N-well (NW)
  - Diffusion/Active (OD)
  - Poly (PO)
  - **Metal-1 (M1)**
  - Contact hole (CO)
- **Non-physical layers** required in your layout:
  - P-select (PPLUS) (pink dots)
  - N-select (NPLUS) (yellow dots)

CMOS Layout



Well-mask

Active-mask

Shallow trench Isolation (STI)

poly-mask

N^+-select-mask

N^+-diffusion

P^+-select-mask

P^+-diffusion

Body-ties

Field oxide

Contact-mask

Contact-etch

Metal-mask

Summary

In this lecture, we have

- introduced intralayer and interlayer geometric design rules
- defined the minimum pitch:
  - the sum of the minimum width and the minimum separation between two objects in the **same** layer
- studied interlayer rules between objects in two different layers, like
  - MOSFET rules between poly and active
  - contact and via rules between contacts or vias to their bottom and top contacting layers
- discussed the prelab assignment to the layout lab session