Lab 2 Summary

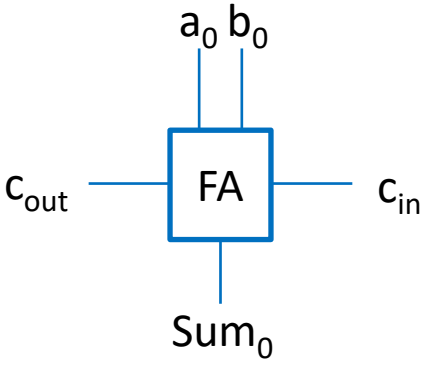
Carry cell design

Prelab 2

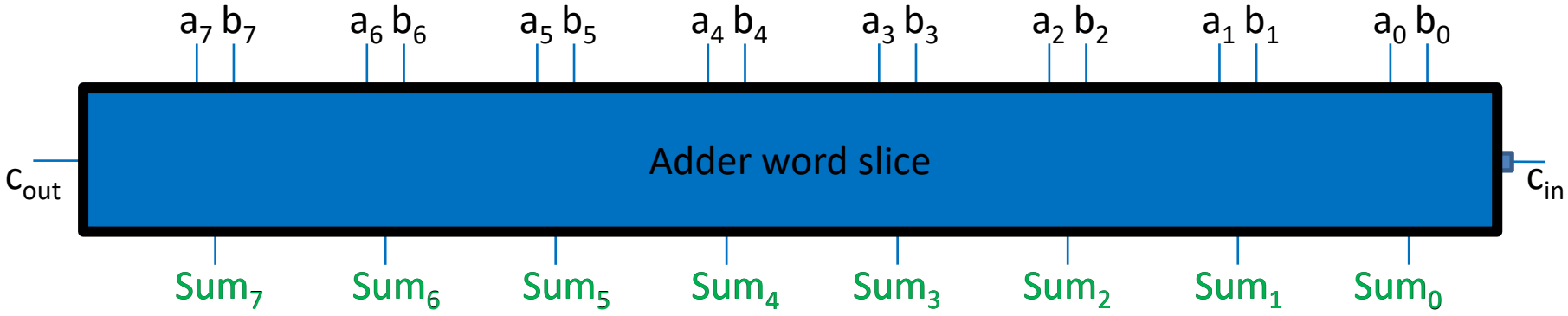
- Design task: design with MOSFETs the carry bit-cell for an 8-bit ripple-carry adder!
- The 8-bit carry logic is to be implemented by an iterative logic array consisting of eight instances of the bit-cell that you have designed.
- The carry bit-cell has three inputs (two bits a, b and a carry-in memory bit), and one output, the carry-out memory bit to the next more significant bit.

Iterative logic arrays: FULL ADDER

Find Boolean equations from truth table!

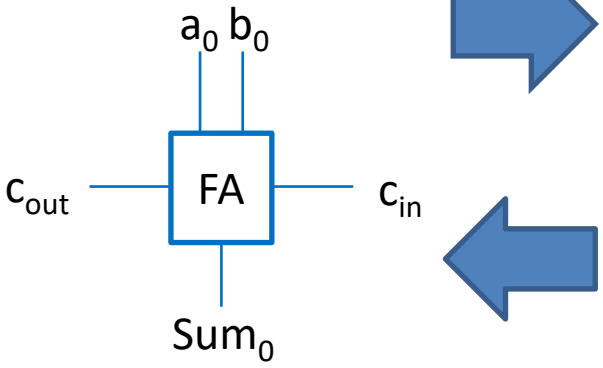


BOOLEAN TRUTHTABLE				
A	B	CIN	COUT	SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



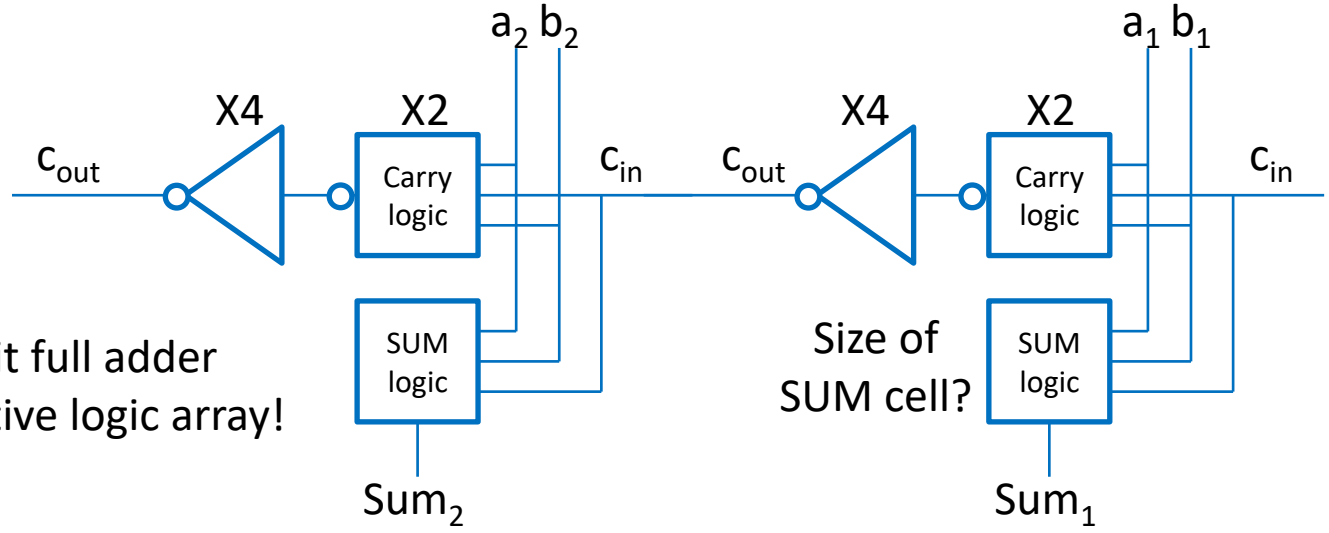
Iterative logic arrays: FULL ADDER

Find Boolean equations from truth table!



BOOLEAN TRUTH TABLE					LOGIC FORMULAS	
A	B	CIN	COUT	SUM	COUT	SUM
0	0	0	0	0	=OR(AND(A;B;CIN);	
0	0	1	0	1	AND(NOT(COUT);OR(A;B;CIN)))*1	
0	1	0	0	1	0	1
0	1	1	1	0	1	0
1	0	0	0	1	0	1
1	0	1	1	0	1	0
1	1	0	1	0	1	0
1	1	1	1	1	1	1

Design full adder by divide and conquer

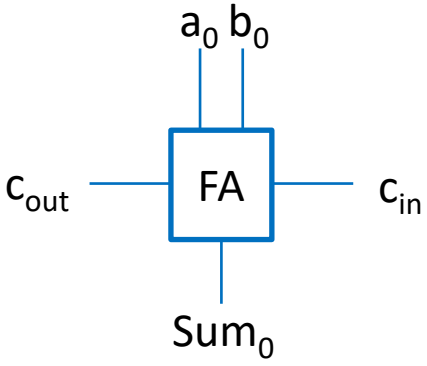


Design 8-bit full adder as an iterative logic array!

Size of SUM cell?

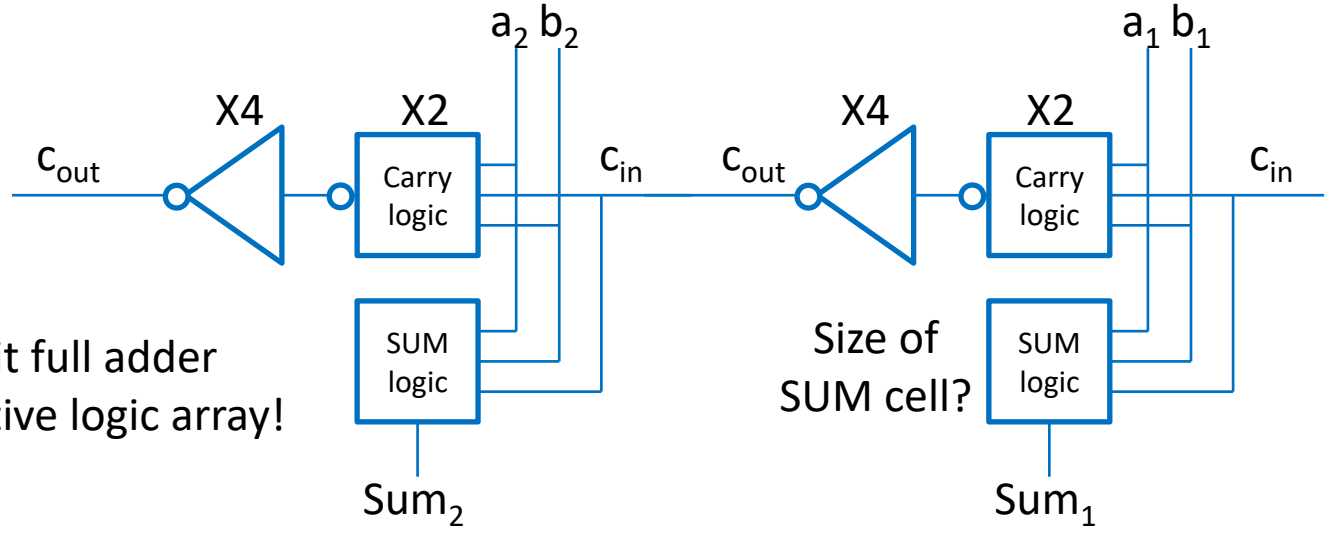
Iterative logic arrays: FULL ADDER

Find Boolean equations from truth table!



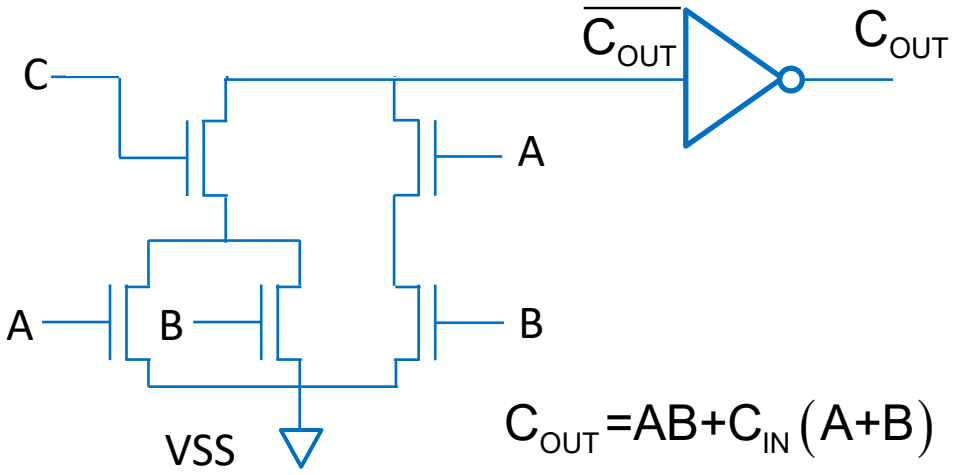
Propagation delay estimation:
Assume carry cell has logical effort *g* and parasitic delay *p.*
8-bit adder delay: A first crude estimate!
$d=8*(p+g*2+p_{inv}+1/2)\approx 8*10=80 \rightarrow t_{pd}= 400$ ps
Corresponding to 1.25 GHz clock frequency
But load from SUM cell was neglected and will slow down the design!

Design 8-bit full adder as an iterative logic array!



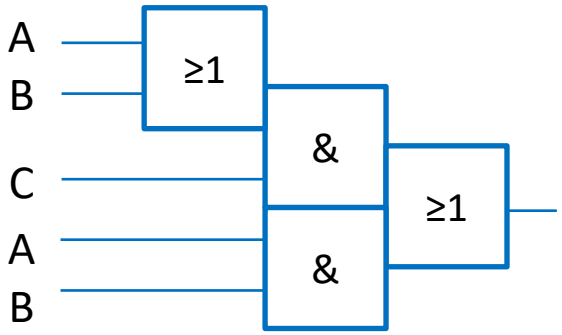
Designing the carry cell

$$\overline{C_{OUT}} = \left(\overline{A} + \overline{B}\right)\left(\overline{C_{IN}} + \overline{A}\,\overline{B}\right) = \overline{A}\,\overline{B} + \overline{C_{IN}}\left(\overline{A} + \overline{B}\right)$$

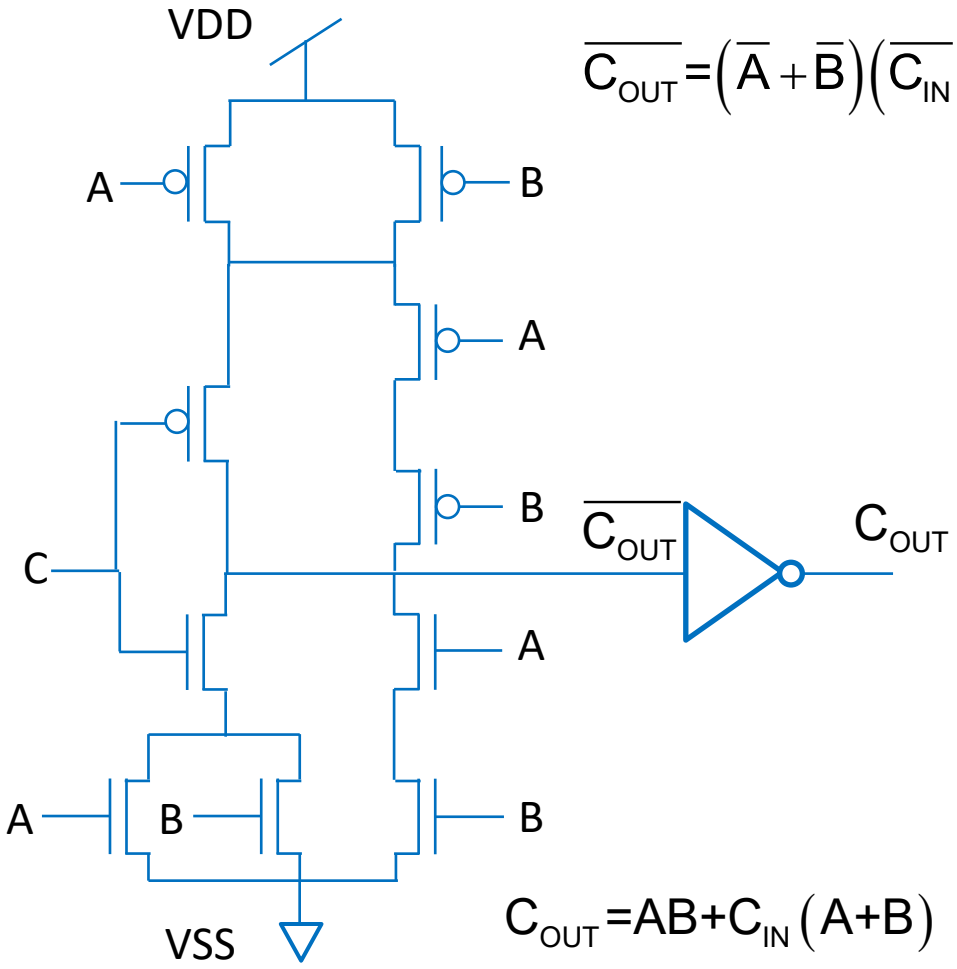


$$C_{OUT} = AB + C_{IN}\left(A + B\right)$$

$$Y = \left(A+B\right)C_{IN} + AB$$



Designing the carry cell



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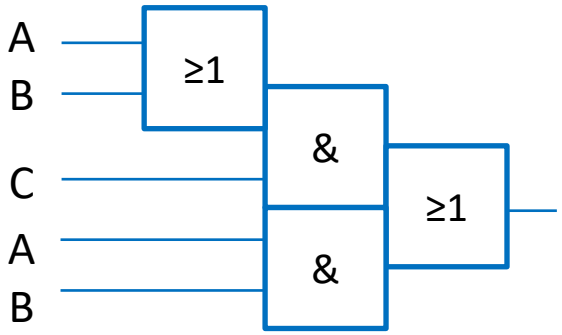
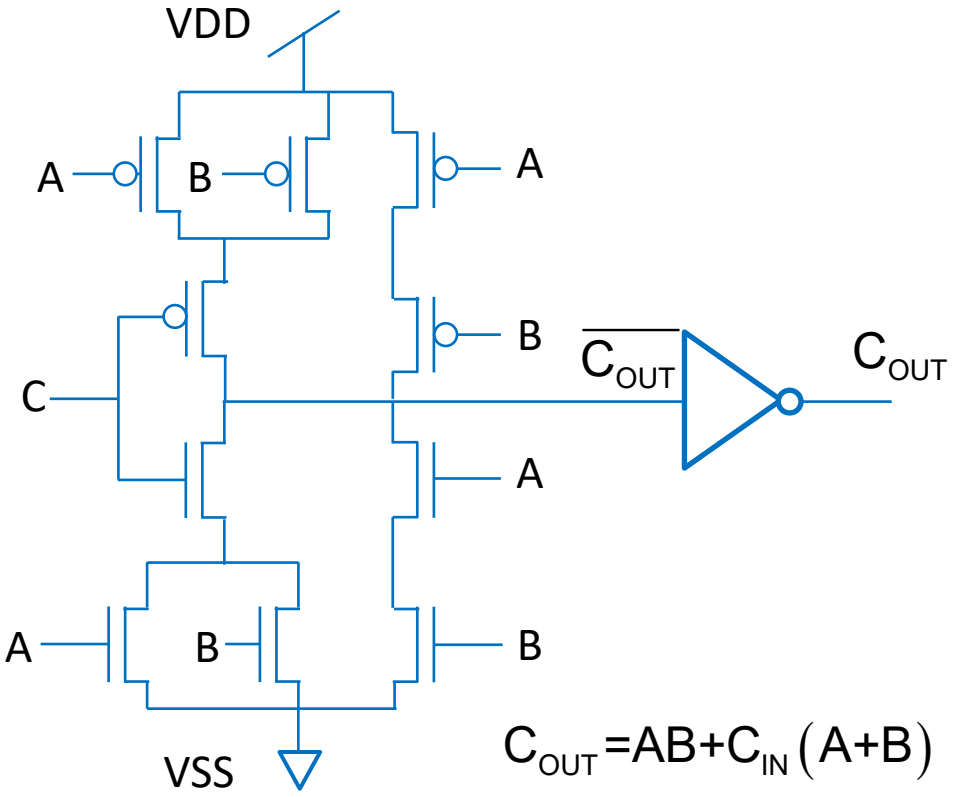
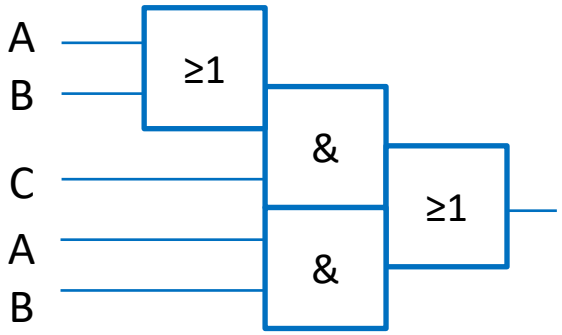


Designing the carry cell

$$\overline{C_{OUT}} = \left(\overline{A} + \overline{B}\right)\left(\overline{C_{IN}} + \overline{A}\,\overline{B}\right) = \overline{A}\,\overline{B} + \overline{C_{IN}}\left(\overline{A} + \overline{B}\right)$$

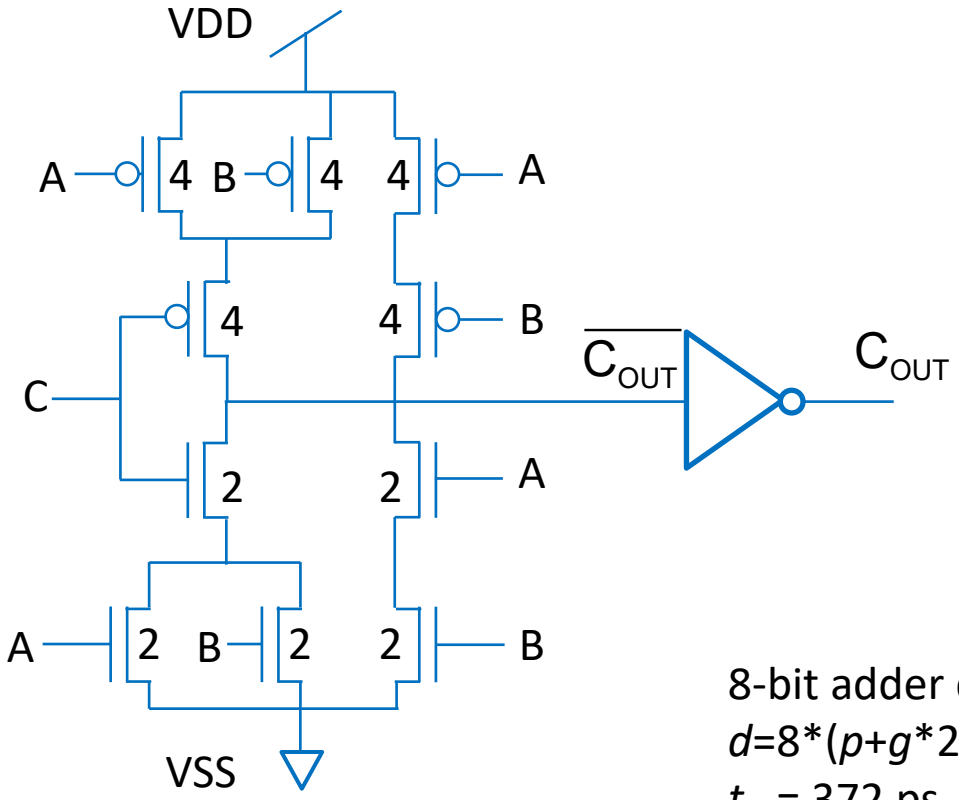




$$C_{OUT} = AB + C_{IN}\left(A + B\right)$$

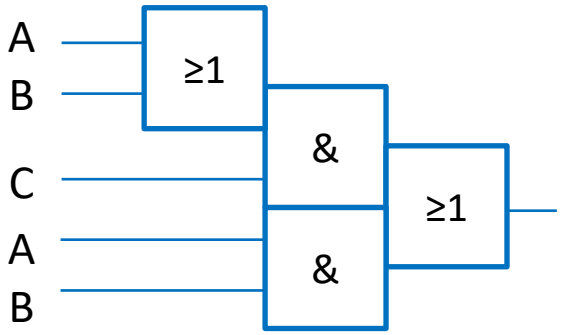
Designing the carry cell

$$\overline{C_{OUT}} = \left(\overline{A} + \overline{B}\right)\left(\overline{C_{IN}} + \overline{A}\,\overline{B}\right) = \overline{A}\,\overline{B} + \overline{C_{IN}}\left(\overline{A} + \overline{B}\right)$$



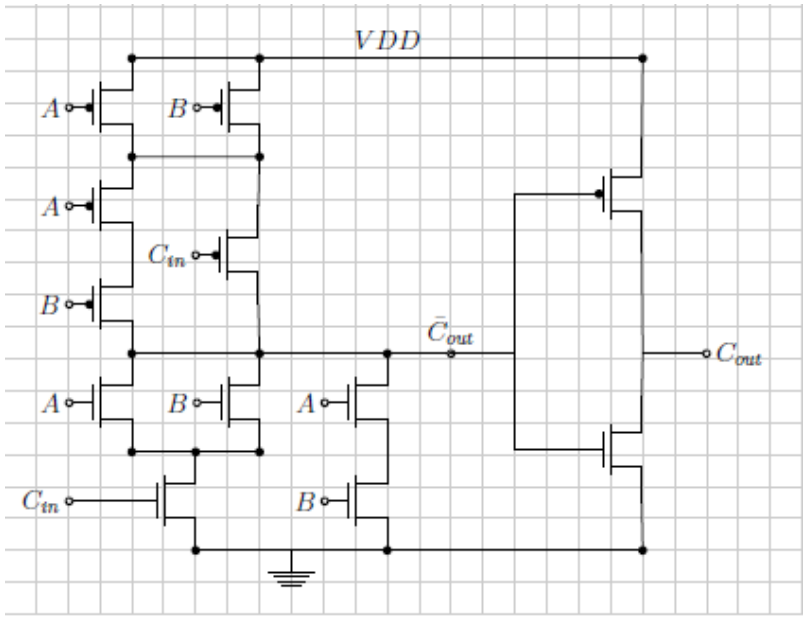
$$C_{OUT} = AB + C_{IN}\left(A + B\right)$$

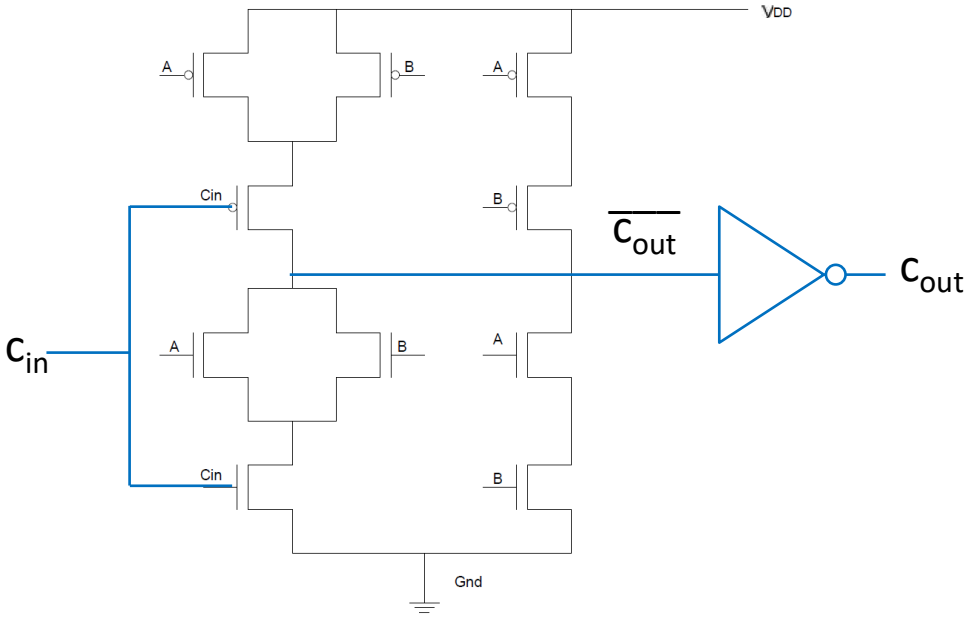
Logical effort g=2,
Parasitic delay p=4



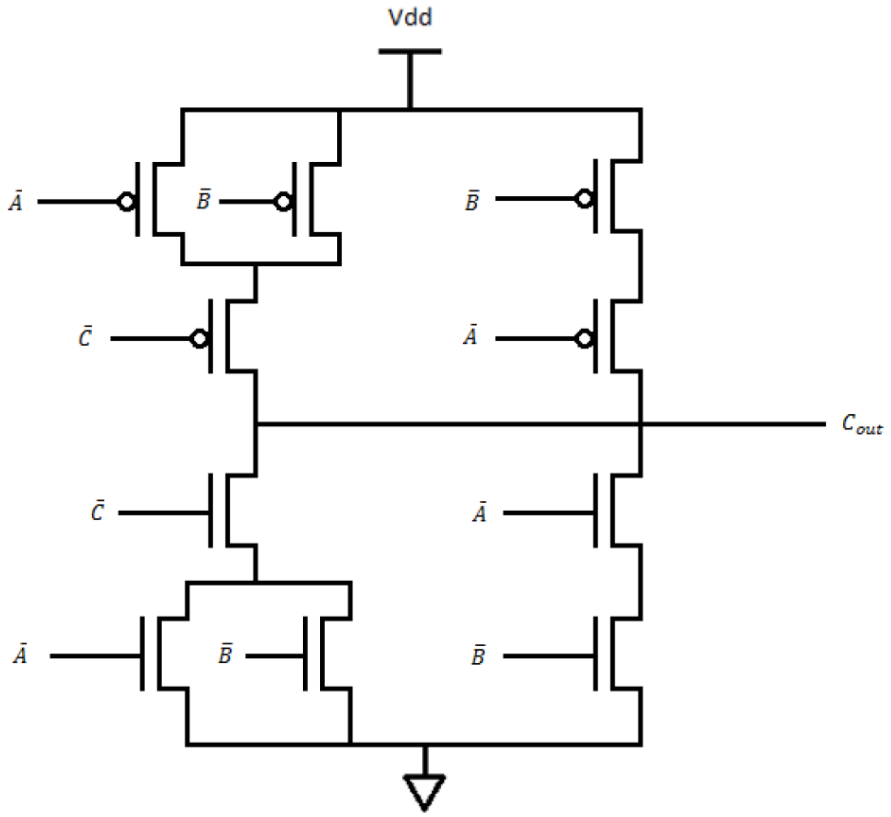
8-bit adder delay: Improved estimate!
$d = 8*(p+g*2+p_{inv}+1/2) \approx 8*(4+2*2+1.3) = 74.4 \rightarrow$
t_{pd}= 372 ps

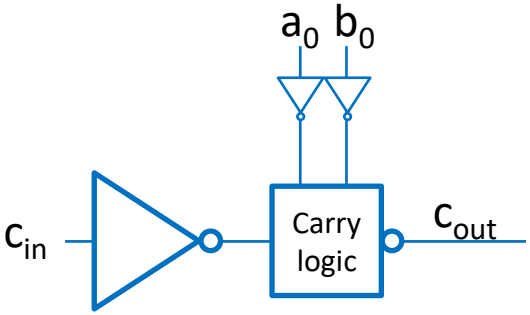
2015 hand-in examples





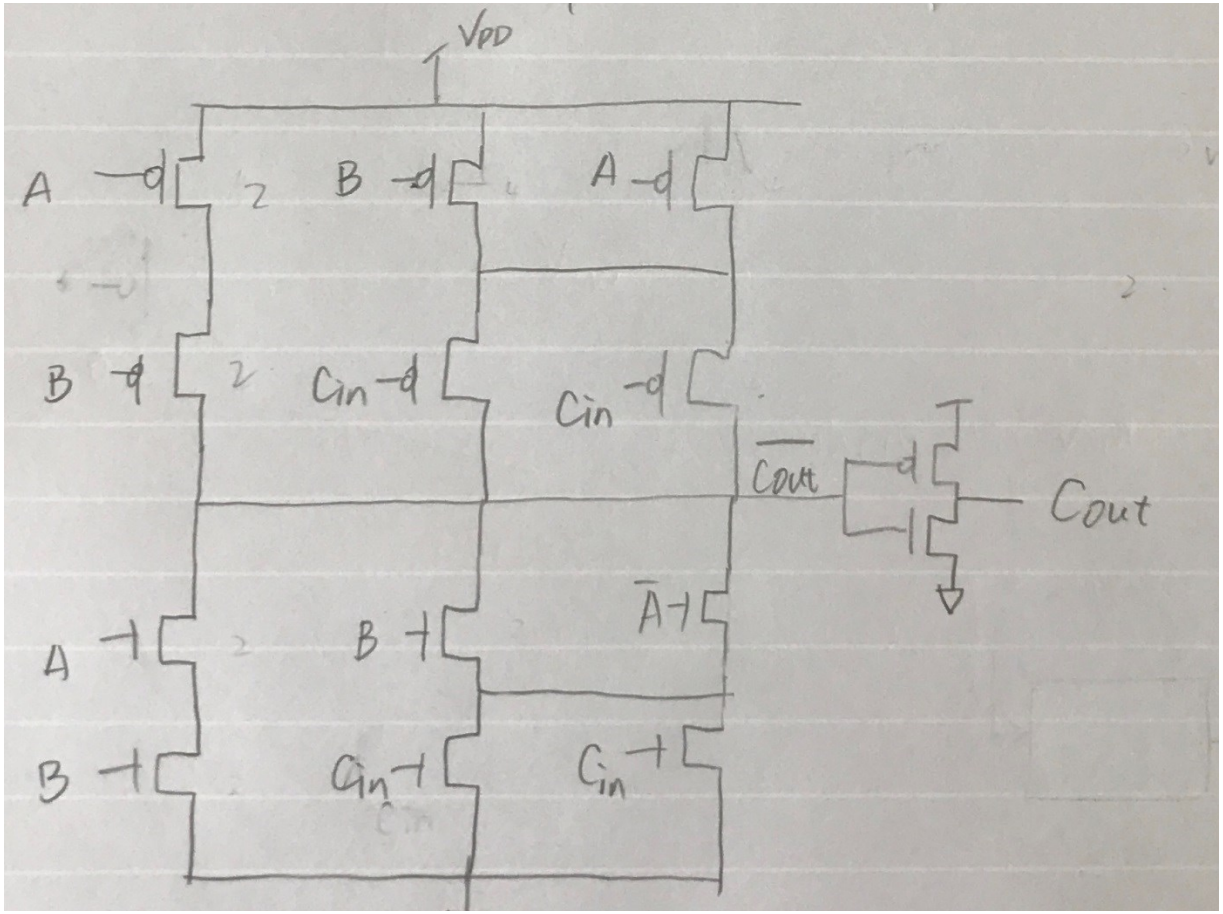
2015 hand-in examples



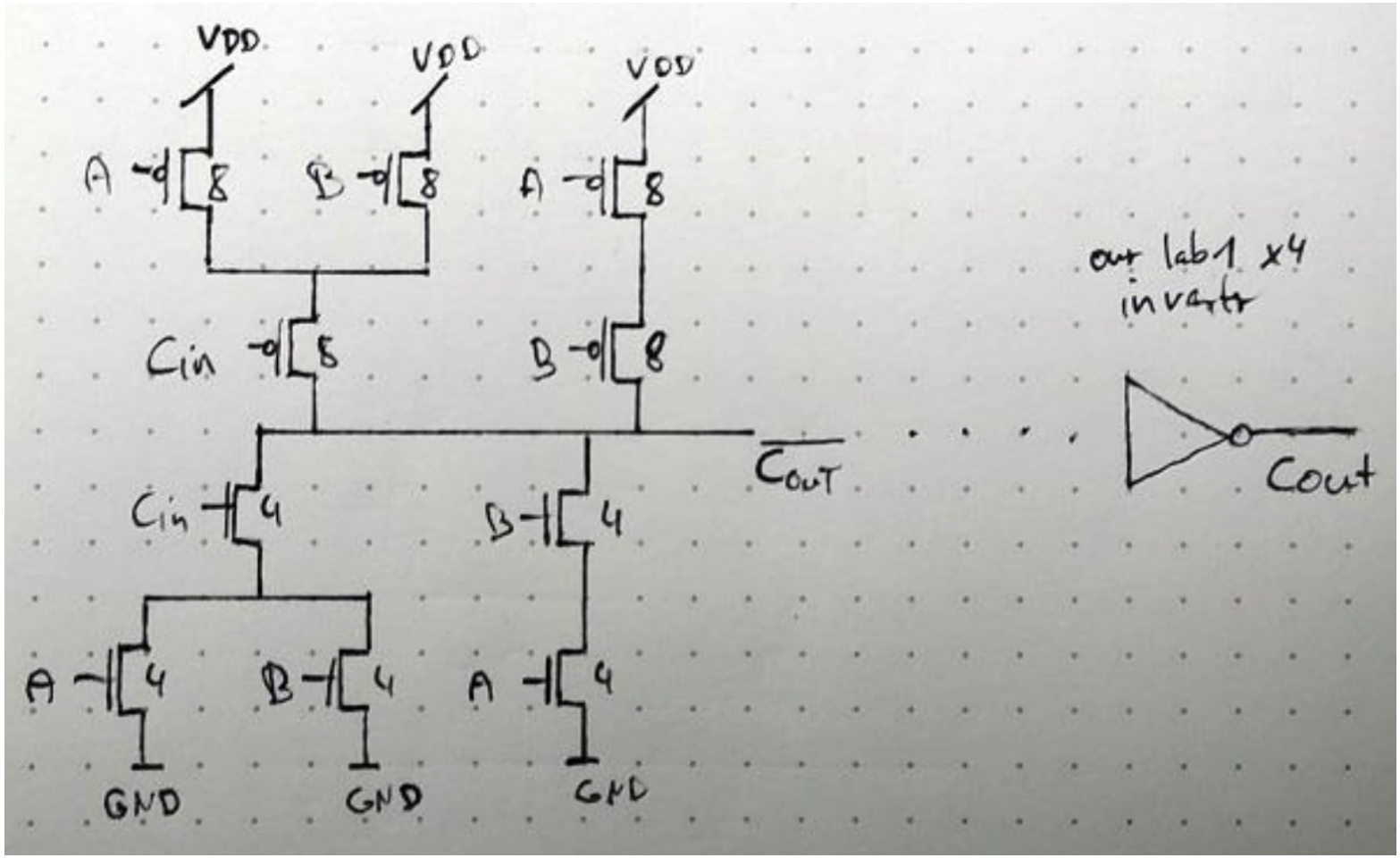


Design structure chosen by a number of 2015 students!

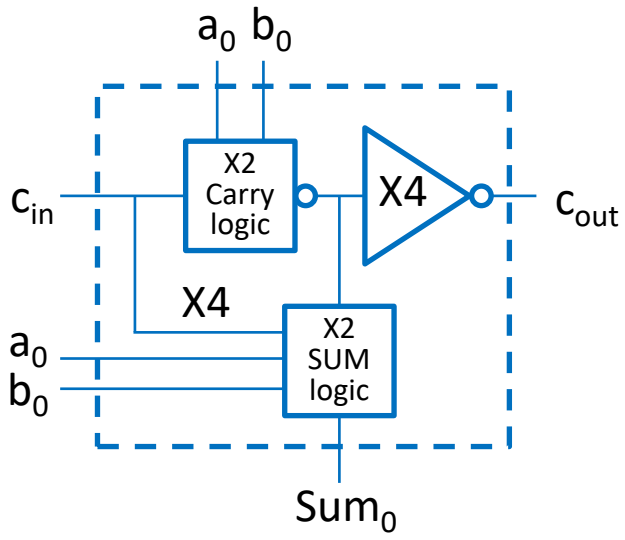
2017 hand-in example



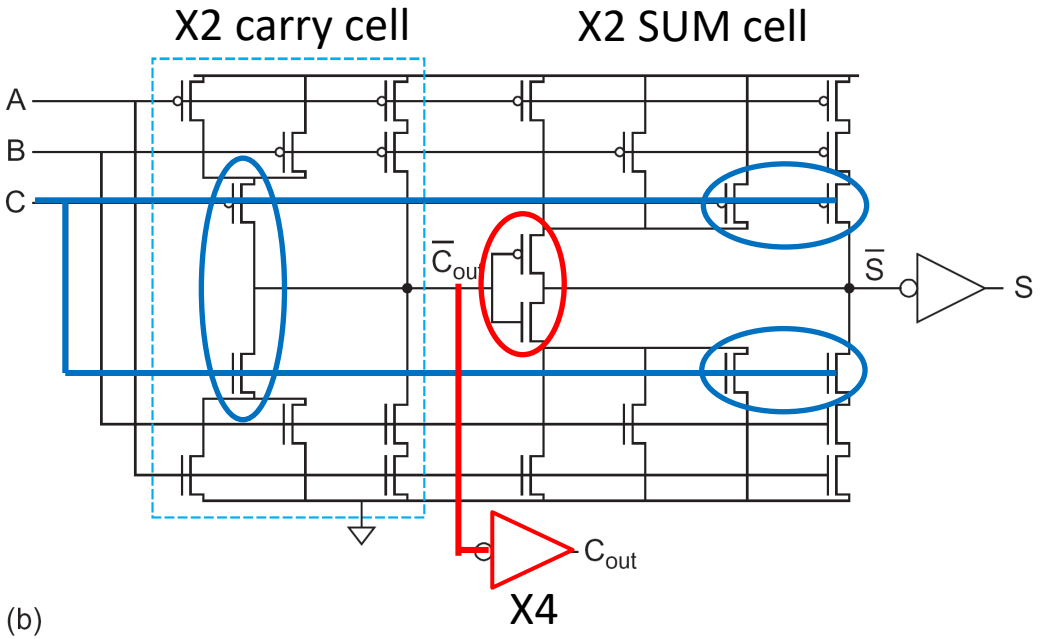
2017 hand-in example



Textbook solution



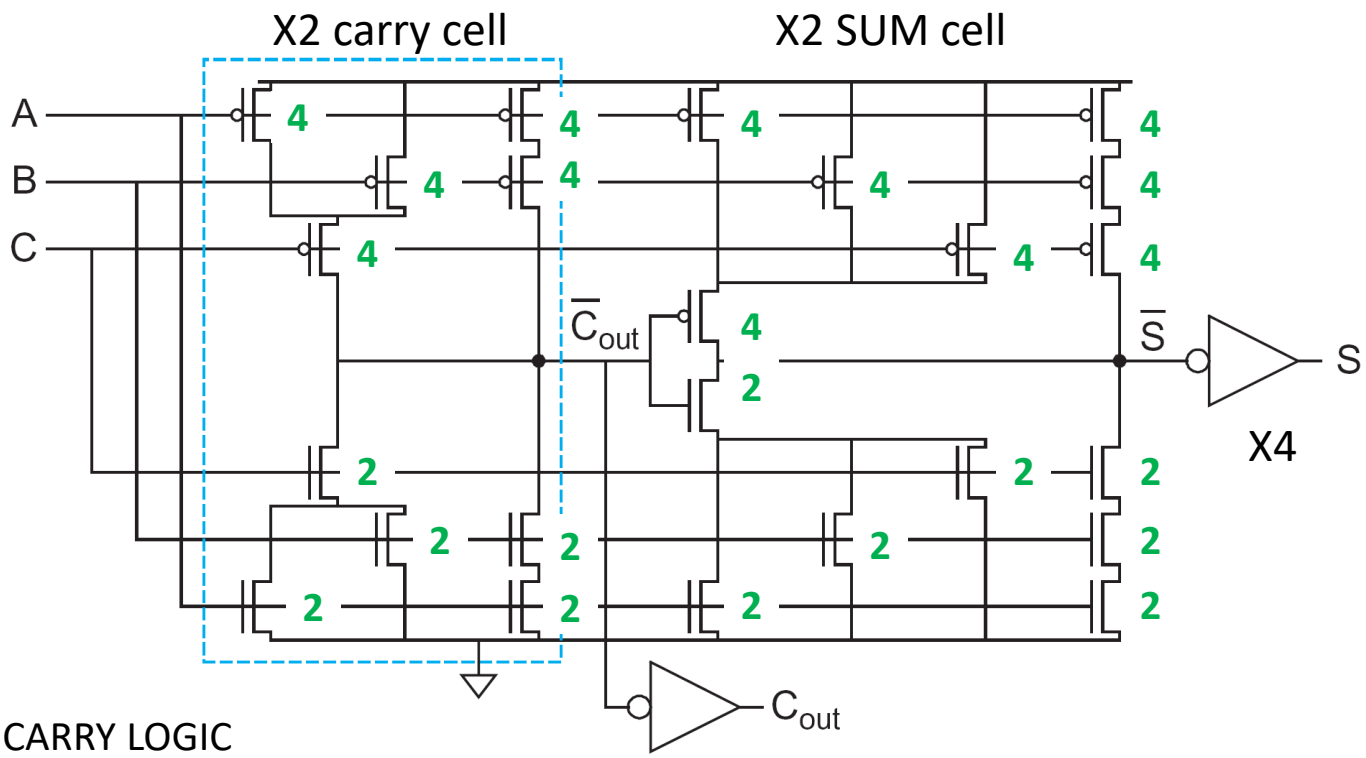
Design structure as proposed in textbook!



Textbook solution

CARRY DELAY (CIN input)

d=4+2x(6+12)/6+1+(6+6+6)/12=4+6+1+1.5=12.5



CARRY LOGIC

(C input)

g=(2+4)/3=2

p=2x(2+4)/3=4

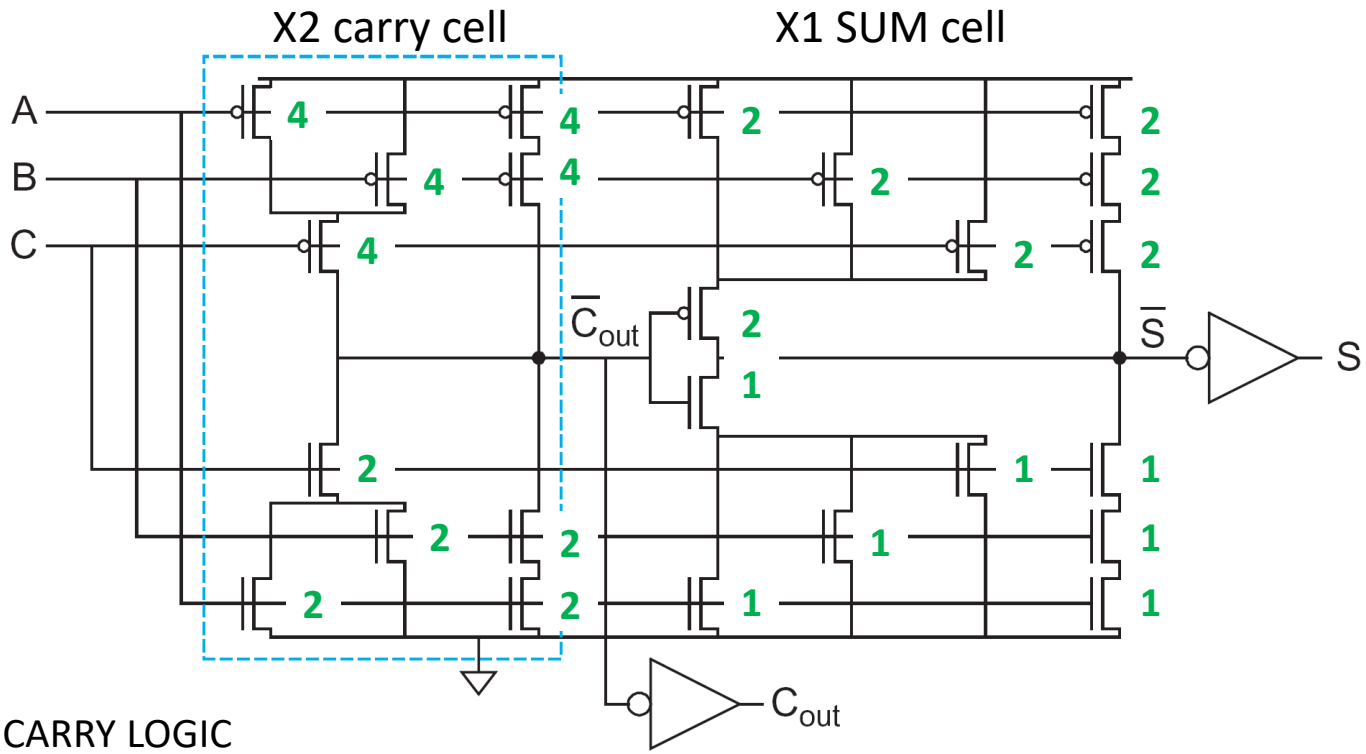
8-bit adder delay: Consider also SUM cell load

$d=8*(p+g*(2+4)/2+p_{inv}+3*2/4)\approx 8*(4+2*3+2.5)=100$

$\rightarrow t_{pd}$= 500 ps

Textbook solution

What if we resize
MOSFETs in SUM cell?

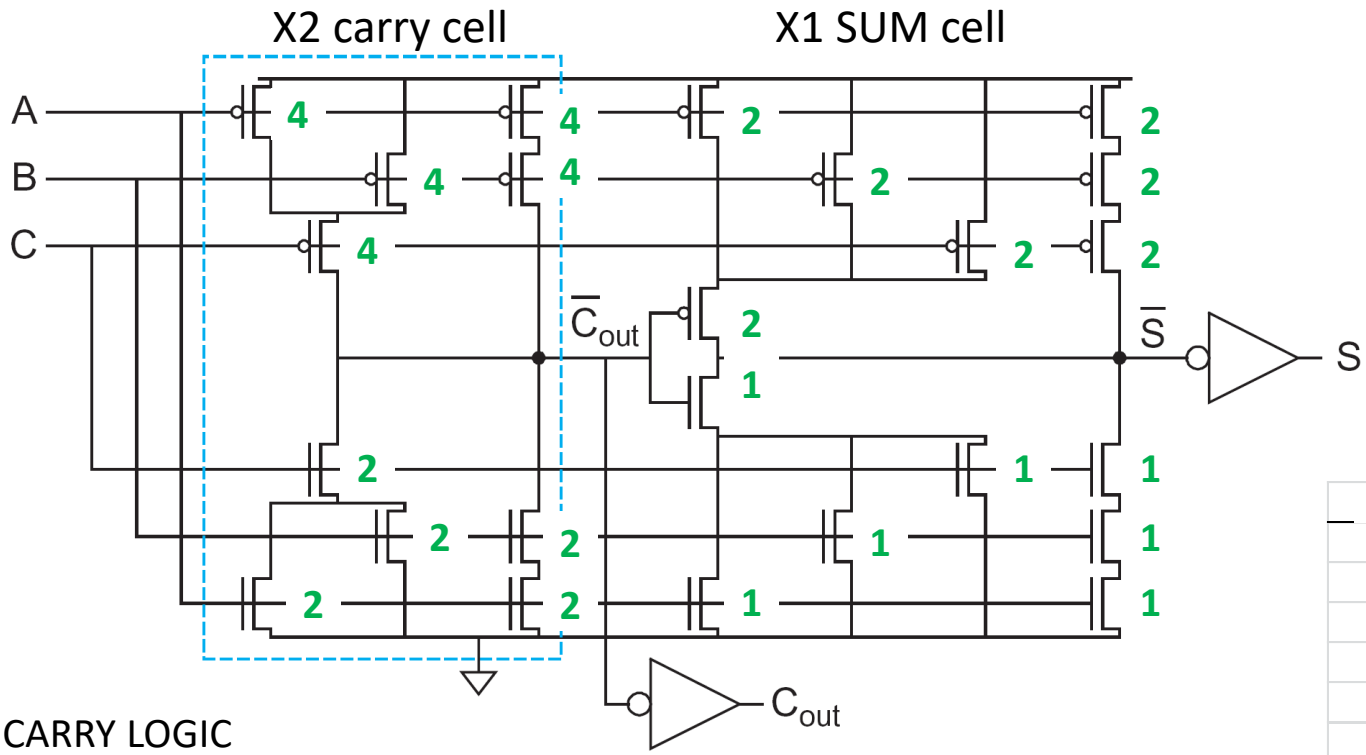


CARRY LOGIC
(C input)
g=(2+4)/3=2
p=2x(2+4)/3=4

8-bit adder delay: Consider also SUM cell load
d=8*(4+2x(1+2)/2+1+(2+1+1))=8*(4+3+1)=8*10=80
→ t_{pd}= 400 ps

Textbook solution

What if we resize
MOSFETs in SUM cell?



CARRY LOGIC
(C input)
g=(2+4)/3=2
p=2x(2+4)/3=4

X2

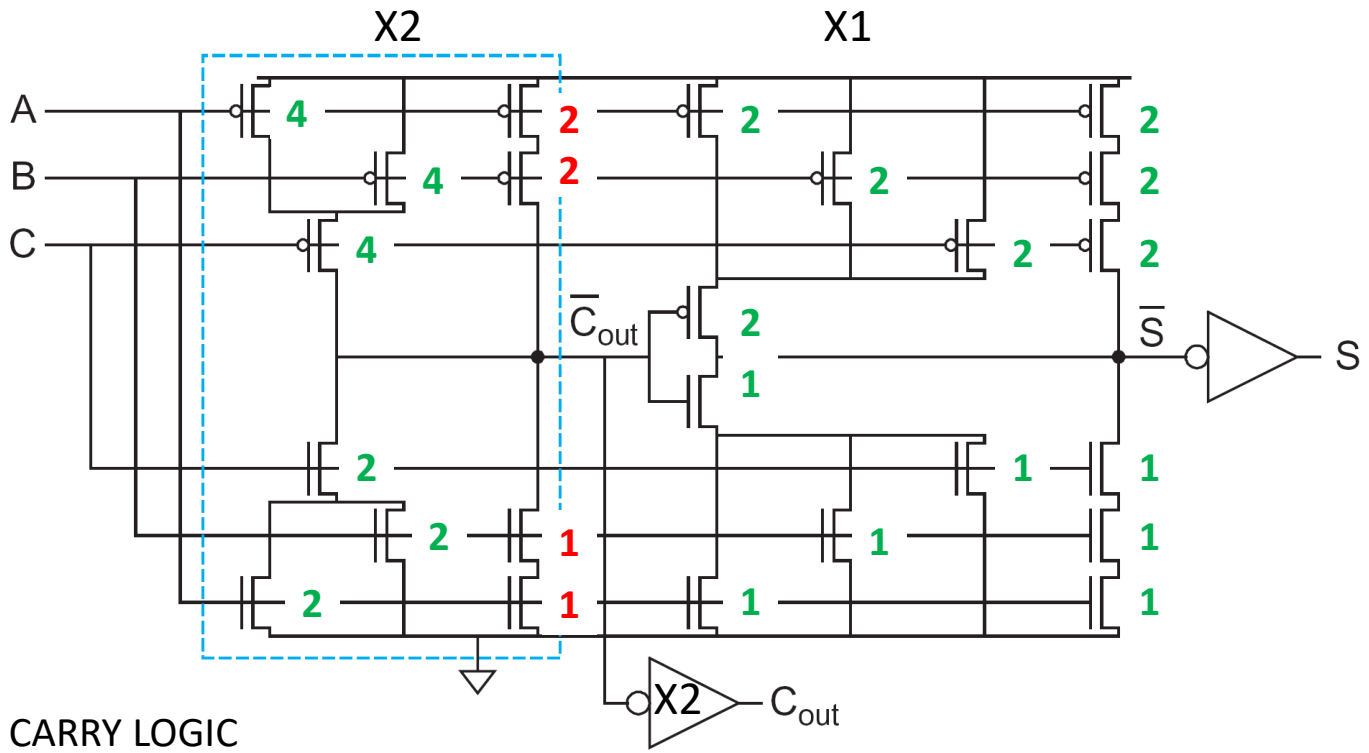
Which size is
optimal? X2? X4?

X	d
1	11
2	10
4	11
5	11,8
8	14,5
10	16,4

Textbook solution

CARRY DELAY (CIN input)

What if we resize the MOSFETs as shown in red, what is the parasitic delay, *p*, now?



CARRY LOGIC

(C input)

g=(2+4)/3=2

p=(2+4+2+1)/3=3

CARRY DELAY (C input)

d=3+2x(1+2)/2+1+(2+1+1)/2=3+3+1+2= 9 units/stage

→ t_{pd}= 360 ps

The End

Q & A session!