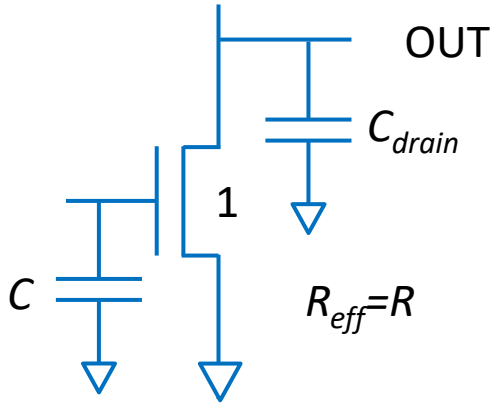
Q & A session

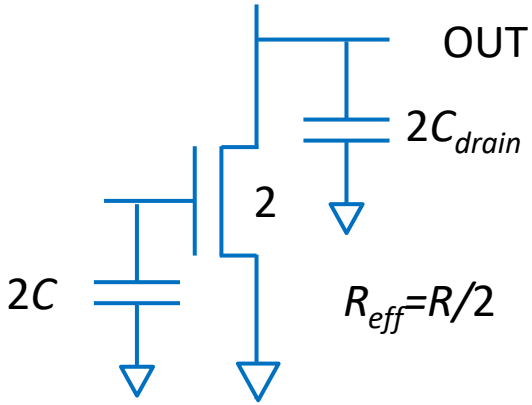
Lecture 5

Transistor sizing

If these are the *R* and *C* parameters of the unit width n-channel MOSFET . . .



. . . what would be the *R* and *C* parameters of a 2 unit width n-channel MOSFET?



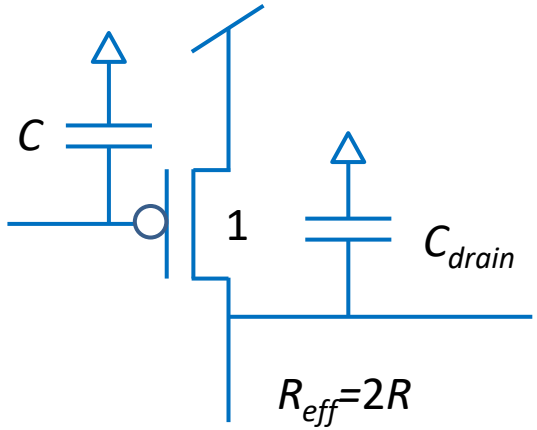
The unit width is just arbitrarily chosen, but for any width *W*, the MOSFET gate capacitance and its effective resistance can be calculated as shown below

$$R_{eff} = \frac{2}{W}\ \frac{[\mathrm{k\Omega}\times\mu\mathrm{m}]}{[\mu\mathrm{m}]},\ C_{gate} = 1.2\times W\ [\mathrm{fF}/\mu\mathrm{m}]\times[\mu\mathrm{m}],\ C_{drain} = p_{inv}C_{gate}$$

CMOS inverter –Transistor sizing

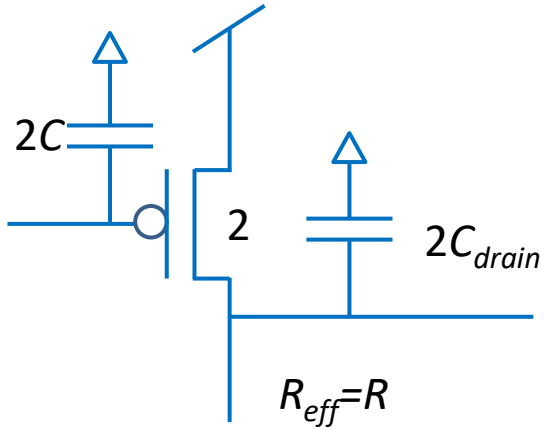
Q: What if the MOSFET is a p-channel device?

The *R* and *C* parameters of the unit width p-channel MOSFET



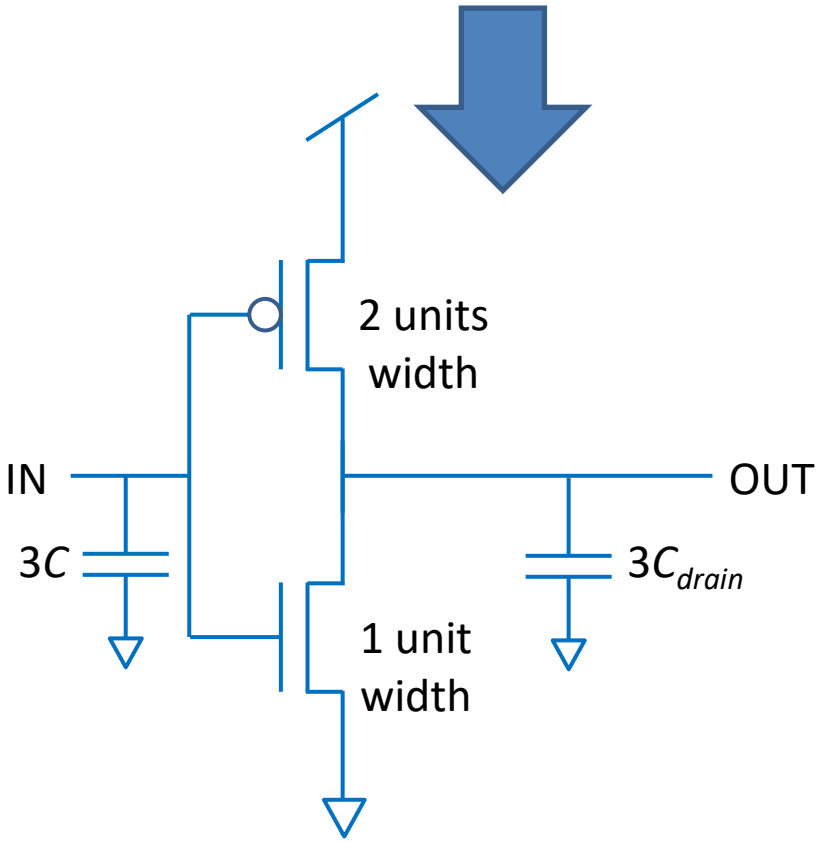
The higher effective resistance is because of the hole mobility in the p-channel being only half of that of the electron mobility in the n-channel.

The *R* and *C* parameters of the 2 unit width p-channel MOSFET



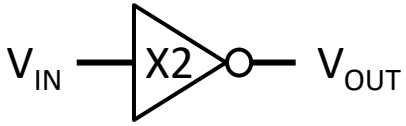
The 2 unit width p-channel device has the same effective resistance as the 1 unit width n-channel device, but twice its capacitances.

So, this is our reference CMOS inverter

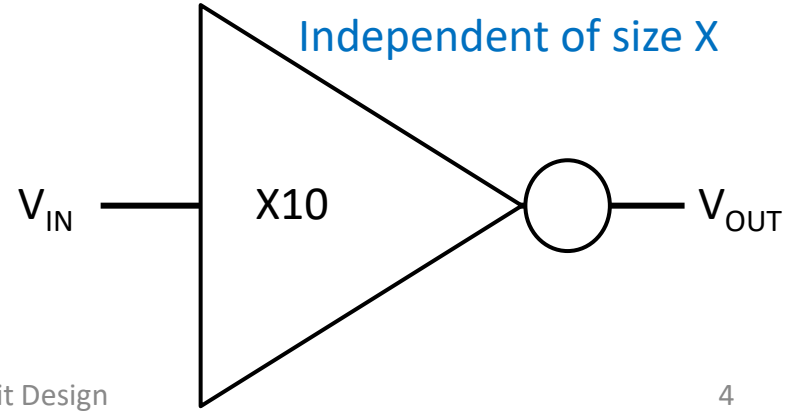


Size X	WN [nm]	WP [nm]
2	200	400
3	280	560
4	370	740
5	510	1020
8	720	1440
10	1000	2000

All inverters in cell library have WP/WN=2

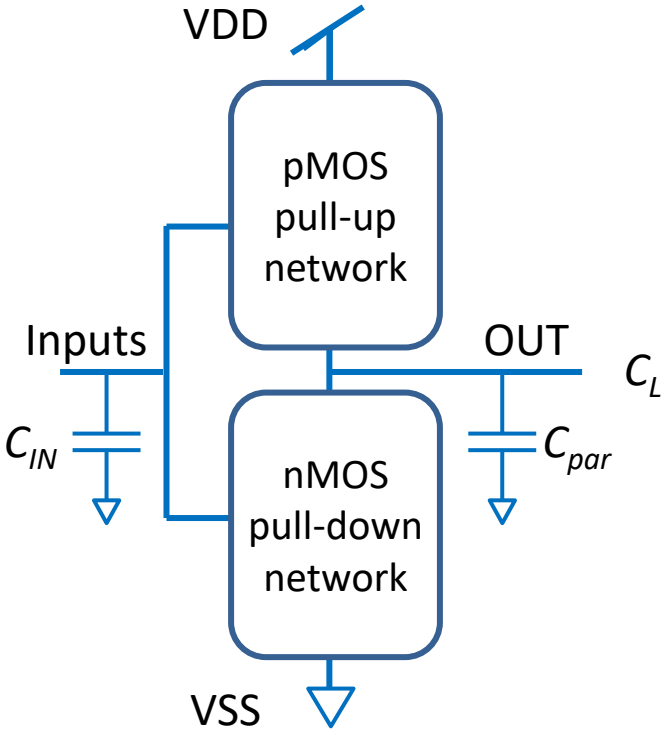


Independent of size X



How to size MOSFETs in a logic gate

Now we want to apply the same model to any CMOS logic gate

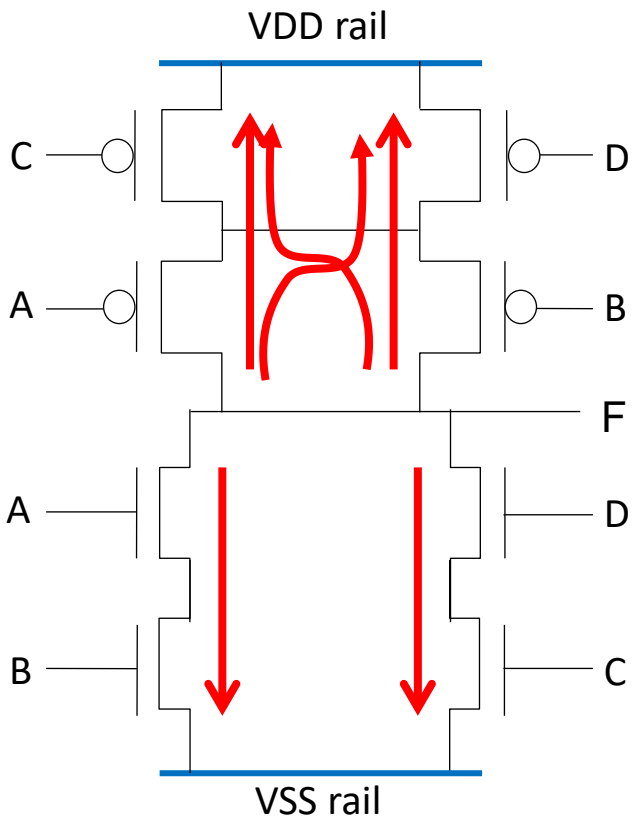


In a logic gate, the pull-up and pull-down networks may have many different resistive paths from the output to the VDD and VSS rails, respectively.

Q: Why do we want all resistive paths to have the same effective resistance?

A: Because it makes life simpler! Just one number to keep track of.
Let the EDA tools keep track of more detailed approaches!

A logic gate example: the AOI22 gate



The AOI22 gate has two pull-down paths to VSS and four pull-up paths to VDD.

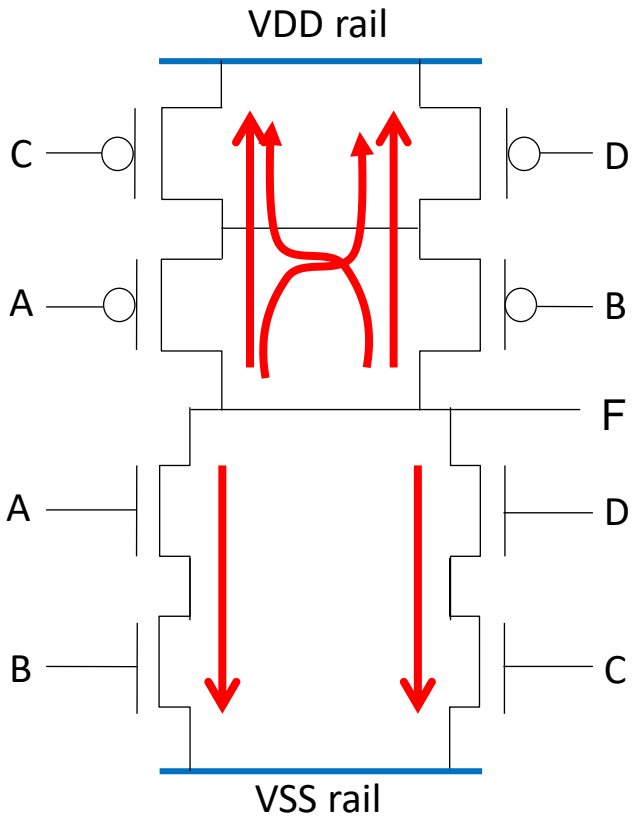
The worst case propagation delay occurs when only one path connects the output to a rail.

When two or more paths are ON, charging/discharging the load capacitor through parallel paths will be faster.

These cases will not be the speed limiting cases potentially violating the timing constraints.

Q: Which input combinations lead to more than one conducting path?
A: This can be deduced from the Boolean truth table. Obviously A=B=C=D=1 opens up 2 paths to ground. 3 or 4 zero inputs will open up two or more conducting paths to VDD.

A logic gate example: the AOI22 gate

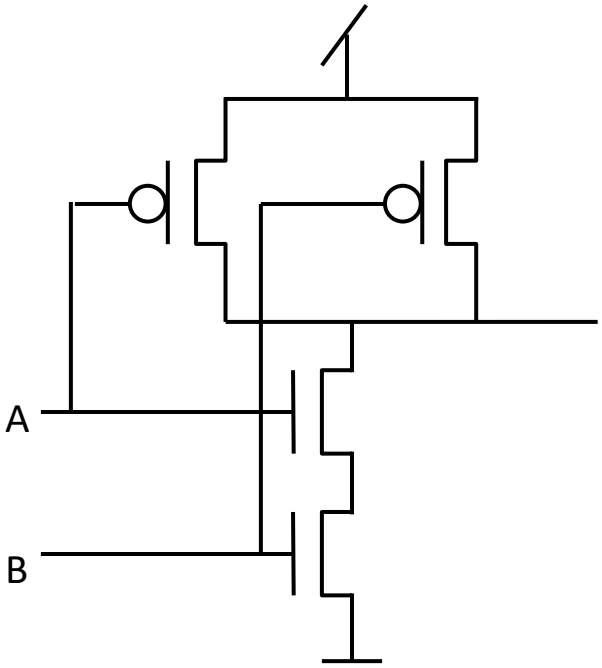


A	B	C	D	OUT	# ON paths
0	0	0	0	1	4↑
0	0	0	1	1	2↑
0	0	1	0	1	2↑
0	0	1	1	0	1↓
0	1	0	0	1	2↑
0	1	0	1	1	1↑
0	1	1	0	1	1↑
0	1	1	1	0	1↓
1	0	0	0	1	2↑
1	0	0	1	1	1↑
1	0	1	0	1	1↑
1	0	1	1	0	1↓
1	1	0	0	0	1↓
1	1	0	1	0	1↓
1	1	1	0	0	1↓
1	1	1	1	0	2↓

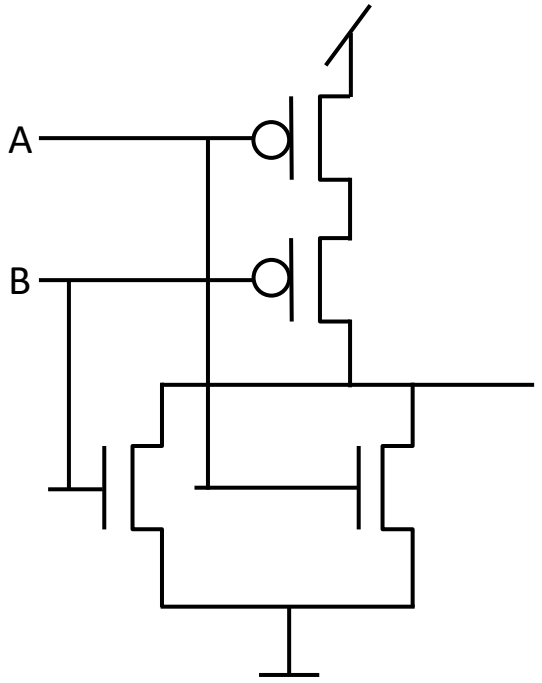
Q: Which input combinations lead to more than one conducting path?

A: This can be deduced from the Boolean truth table. Obviously A=B=C=D=1 leads to 2 paths to ground. 3 or 4 zero inputs lead to 2 or more conducting paths to VDD.

Exercise:
Calculate NAND2 NOR2 logical efforts

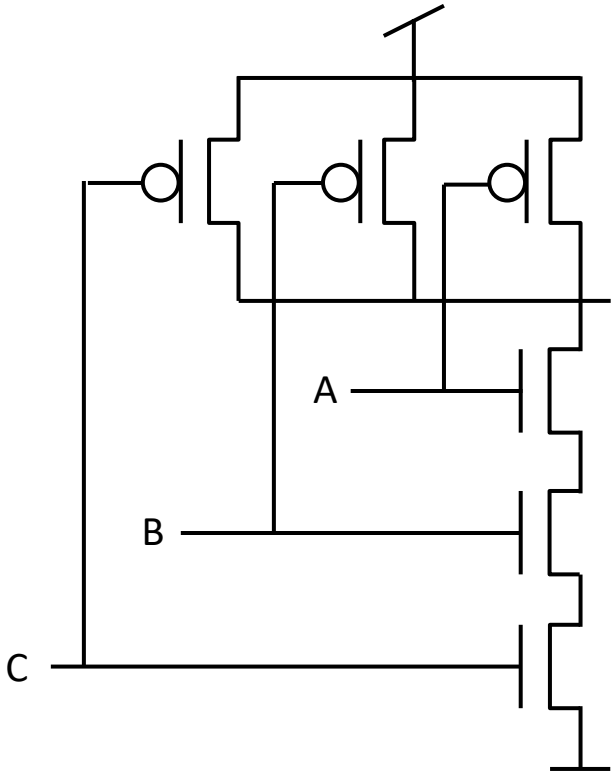


NAND2
Show that g=4/3, and p=2p_{inv}



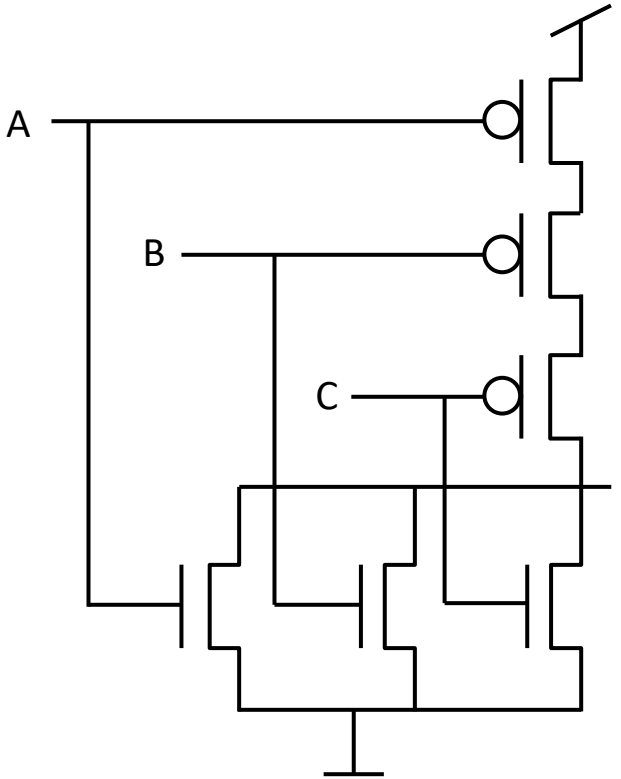
NOR2
Show that g=5/3, and p=2p_{inv}

Exercise:
Calculate NAND3 & NOR3 logical efforts



NAND3

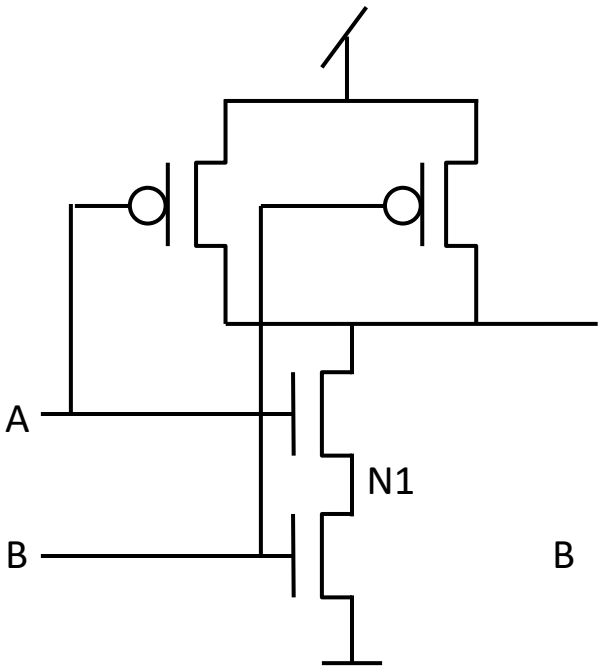
Show that $g=5/3$, and $p=3p_{inv}$



NOR3

Show that $g=7/3$, and $p=3p_{inv}$

Consider the NAND2 logical gate



NAND2

Q: Does it make any difference to the switching properties of the NAND2 gate that the source of the A-input n-channel device is not connected to ground?

A: Interesting question. Actually it does. Consider the case when A=1 and B=0. Both the output and N1 nodes are then at VDD.

The node N1 voltage not being at GND actually increases the threshold voltage of the A-input n-channel device, thereby increasing its effective resistance and making it a bottleneck device once B goes high.

Therefore it is better to arrange inputs so that the B-input goes high before the A input.

When A=0 and B=1, the N1 node is being discharged to GND. Thereby the threshold voltage of the A-input MOSFET is not affected. Furthermore, node N1 is already discharged when the A-input goes high!

VT modulation

- The effect that the MOSFET source potential not being at GND affects the threshold voltage is called VT-modulation.
- Why do I tell you about this?
- Because it is going to be important in your carry cell design!
- When you add two bits, a and b, considering an incoming carry from less significant bits, which is the order of signal arrival? Should be considered while designing your cell for the course lab series!
- Design task: