Prelab 2 Introduction

Iterative Logic

Prelab 2

- Design task: design with MOSFETs the carry bit-cell for an 8-bit ripple-carry adder!
- The 8-bit carry logic is to be implemented by an iterative logic array consisting of eight instances of the bit-cell that you have designed.
- The carry bit-cell has three inputs (two bits a, b and a carry-in memory bit), and one output, the carry-out memory bit to the next more significant bit.

Designing an adder word slice

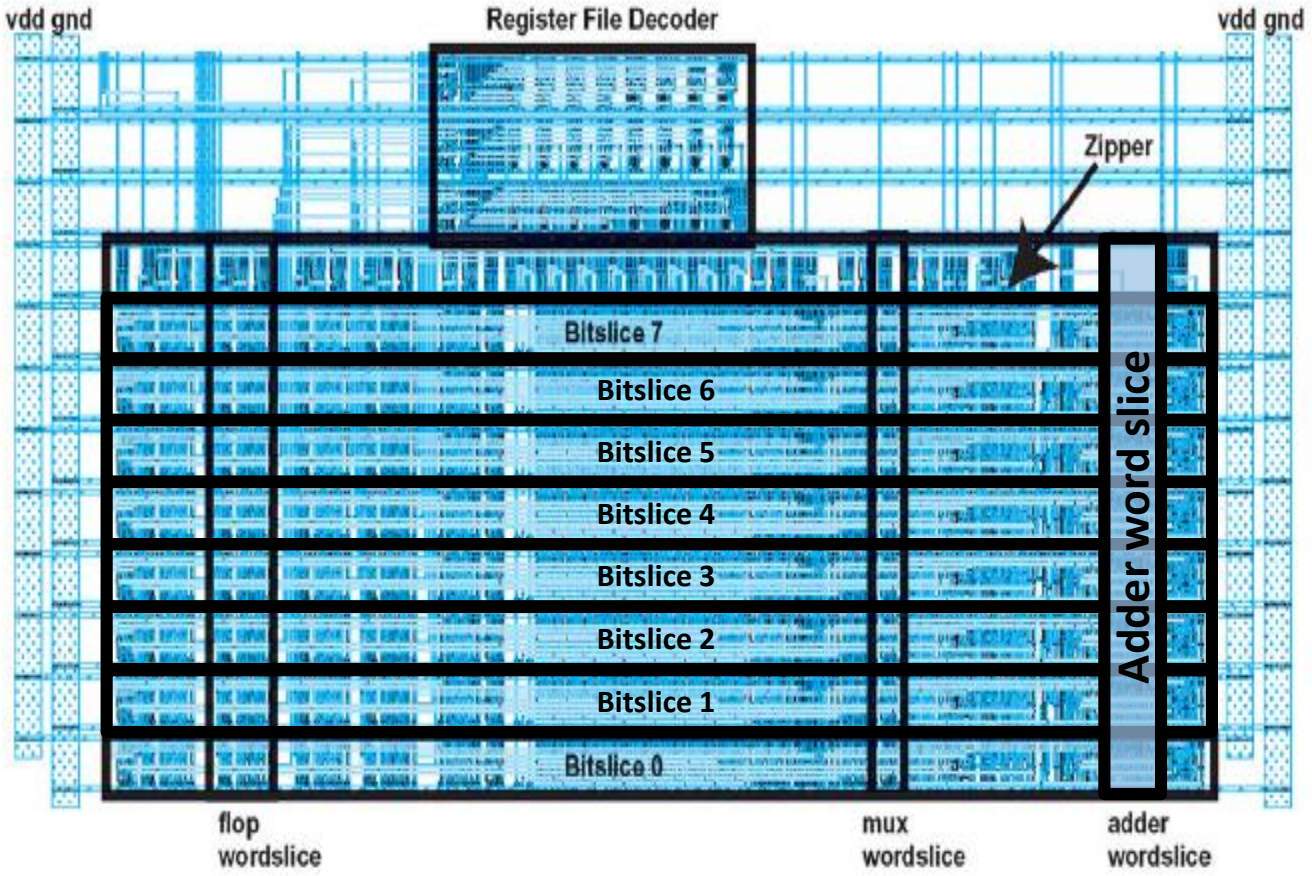
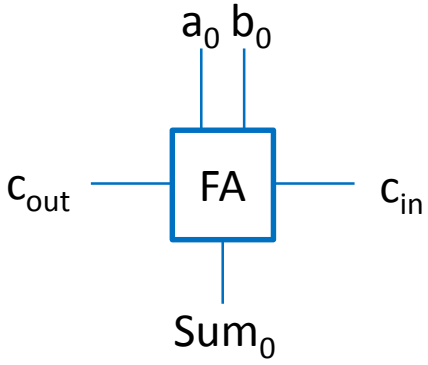
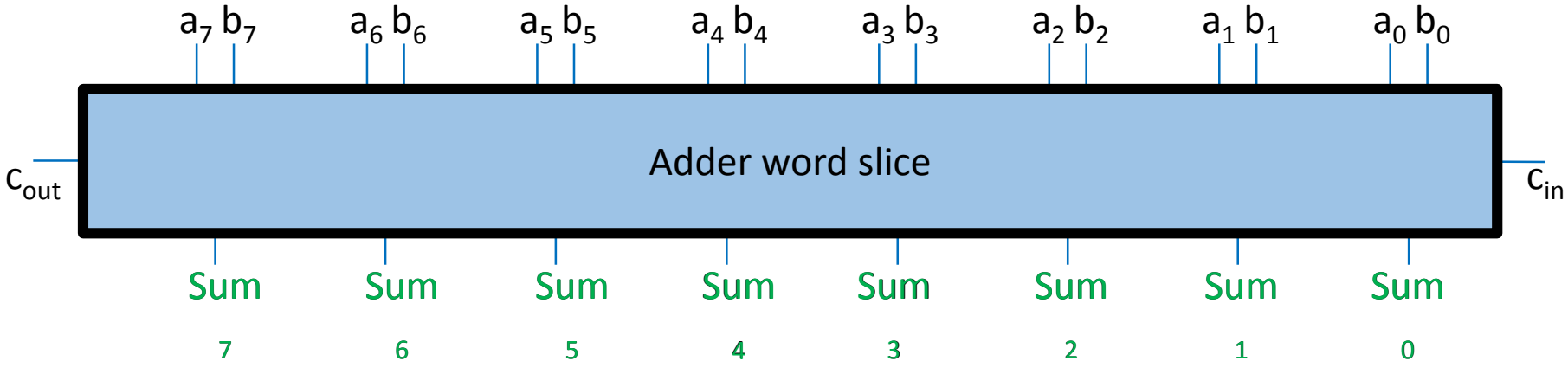


FIGURE 1.67 MIPS datapath layout

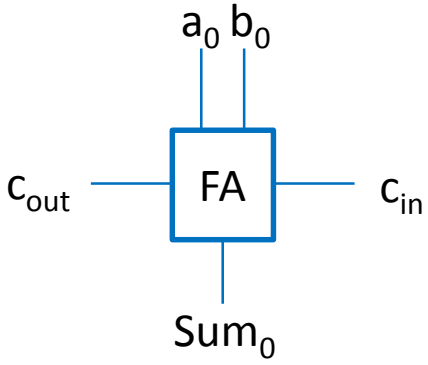
Iterative logic arrays: FULL ADDER



BOOLEAN TRUTH TABLE				
A	B	CIN	COUT	SUM
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		



Iterative logic arrays: FULL ADDER



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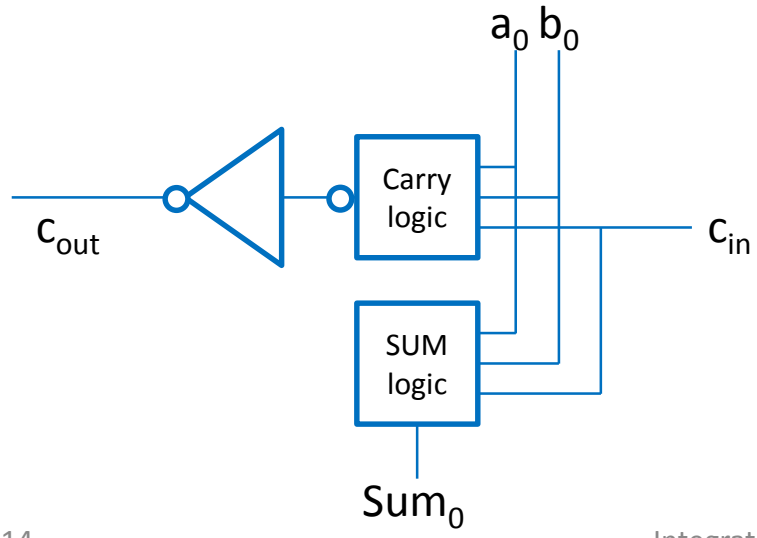

Prelab design tasks (see prelab 2 instructions):

- Design carry logic as a SUM of products!
- Draw MOSFET schematic!
- Calculate logical effort and parasitic delay of the inverting carry-logic cell that you have designed!

The End

Q & A session!