CMOS Logic Gates – a delay model

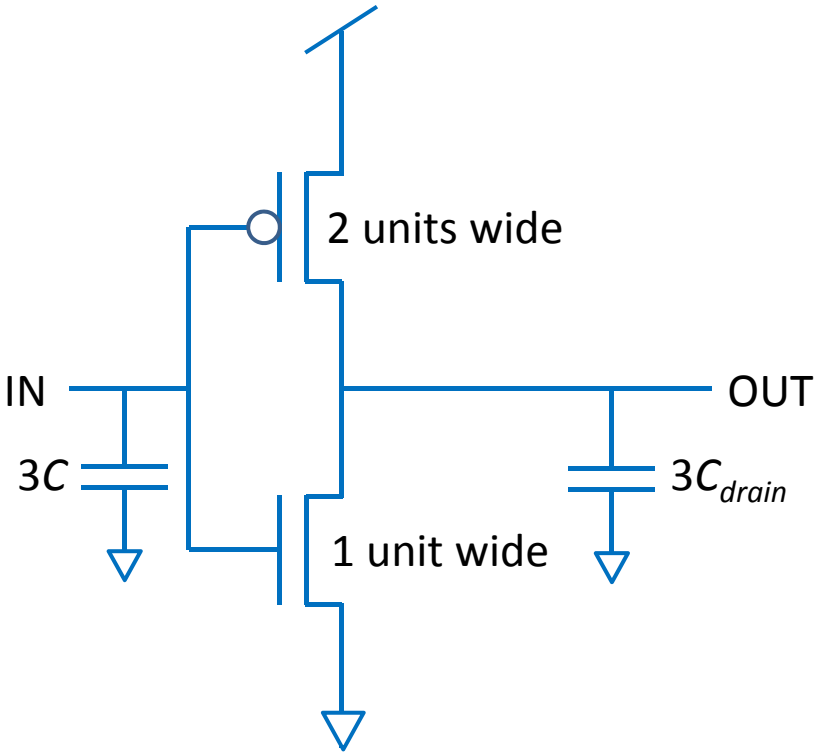
Introducing logical effort

Lecture 5

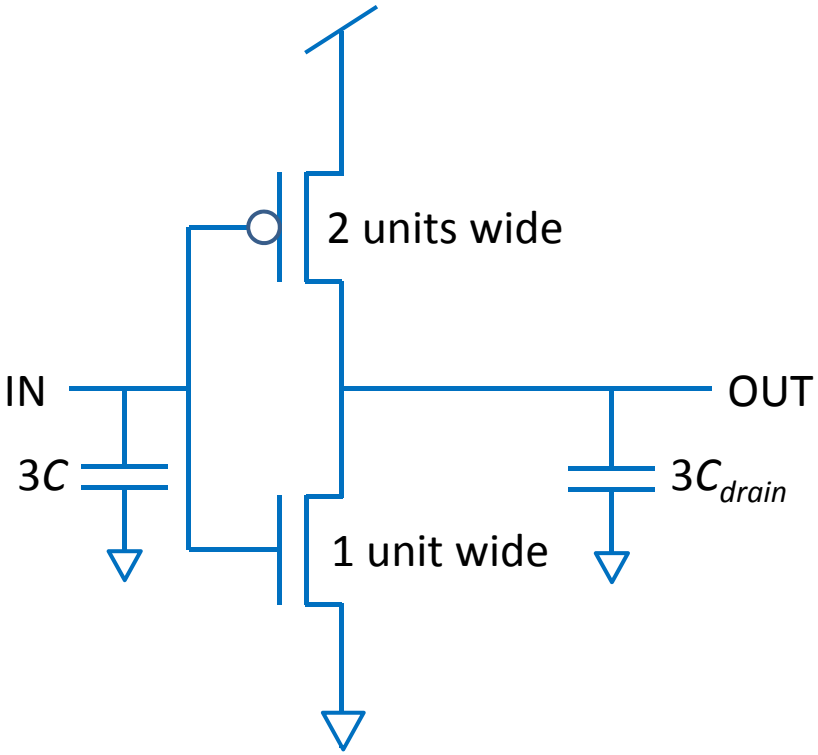
Background

- In previous lecture, lecture 4, we have developed a propagation delay model for CMOS inverters.
- For equal rise and fall delays, we have decided to use p-channel devices twice as wide as the n-channel device.
- An n-channel MOSFET of unit width was assumed to have effective resistance *R* and gate capacitance *C*.
- Hence, a p-channel device of two units width has the same effective resistance *R*, but gate capacitance 2*C*.
- The inverter designed with such MOSFETs has input capacitance 3*C*, and equal pull-up and pull-down resistances.

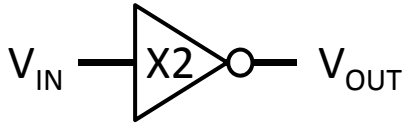
CMOS inverter –Transistor sizing

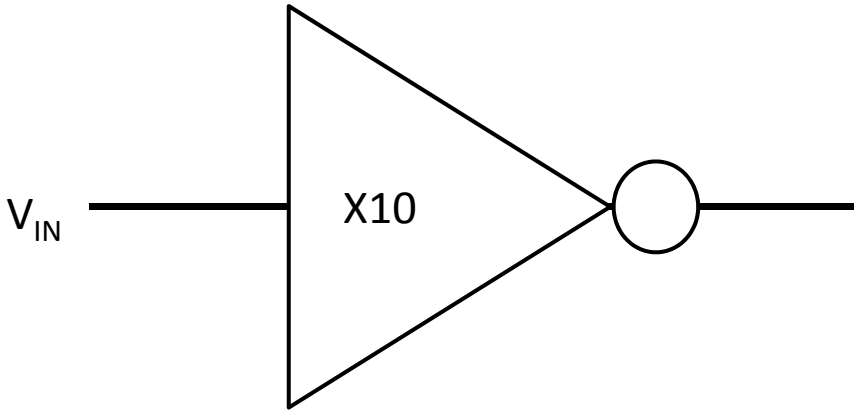


CMOS inverter – cell sizing

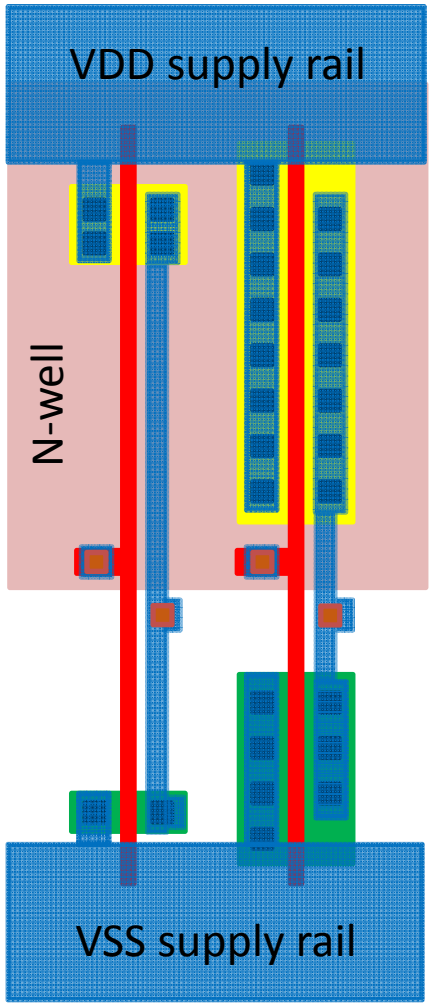


Size X	WN [nm]	WP [nm]
2	200	400
3	280	560
4	370	740
5	510	1020
8	720	1440
10	1000	2000





CMOS inverter – cell sizing



In ST cell library, size X refers to the input cap (and for inverters also to the driving capability)!

Size X	WN [nm]	WP [nm]
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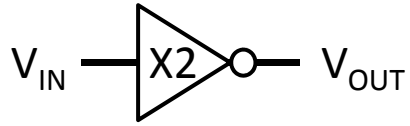
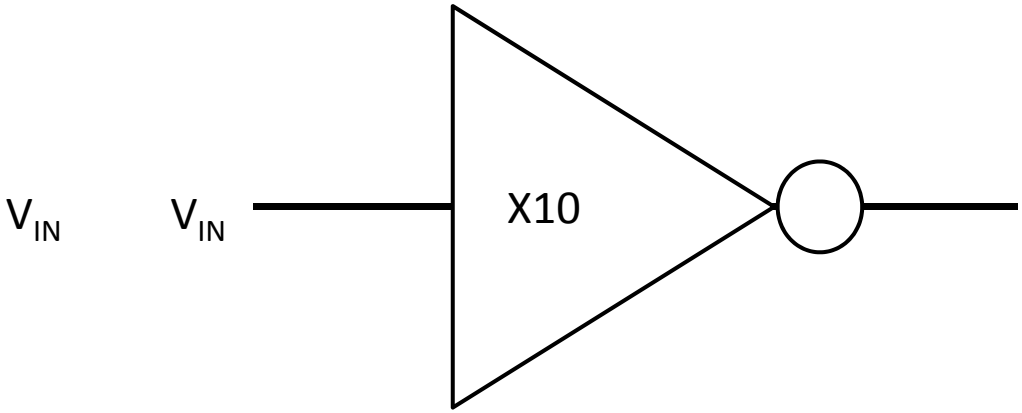
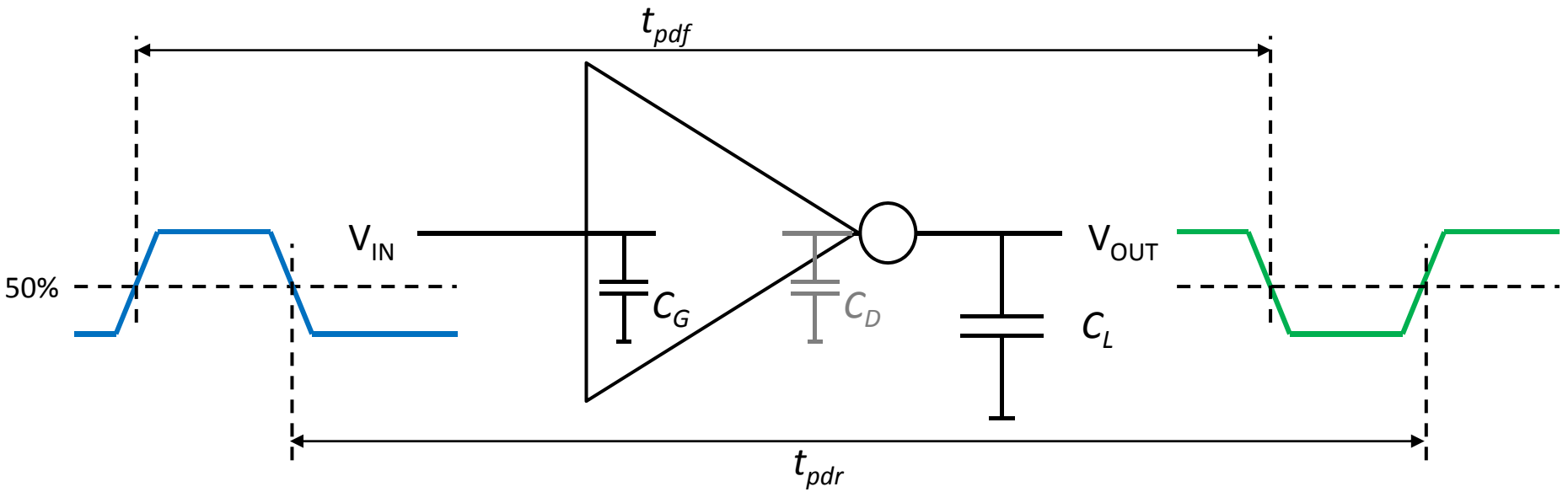




Inverter propagation delay model

Propagation delay definitions: rise and fall delays

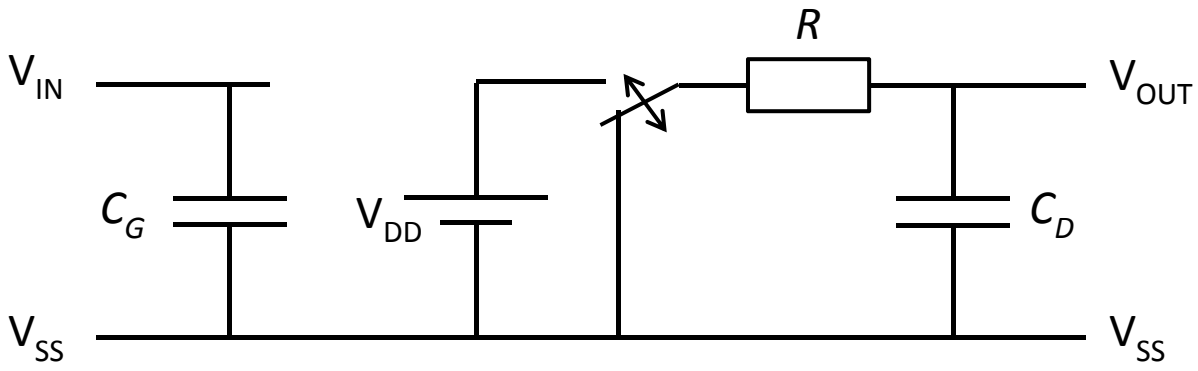


$$t_{pd} = 0.7\left(C_D + C_L\right)\frac{V_{DD}}{I_{DSAT}} = \underbrace{0.7R_{eff}C_G}_{\text{tau}}\left(\frac{C_D}{C_G} + \frac{C_L}{C_G}\right) = \tau\left(p_{inv} + h\right)$$

We defined time constant tau equal to 5 ps in 65 nm CMOS technology. Furthermore, we introduced parasitic delay $p_{inv}=C_D/C_G$, and electrical effort $h=C_L/C_G$.

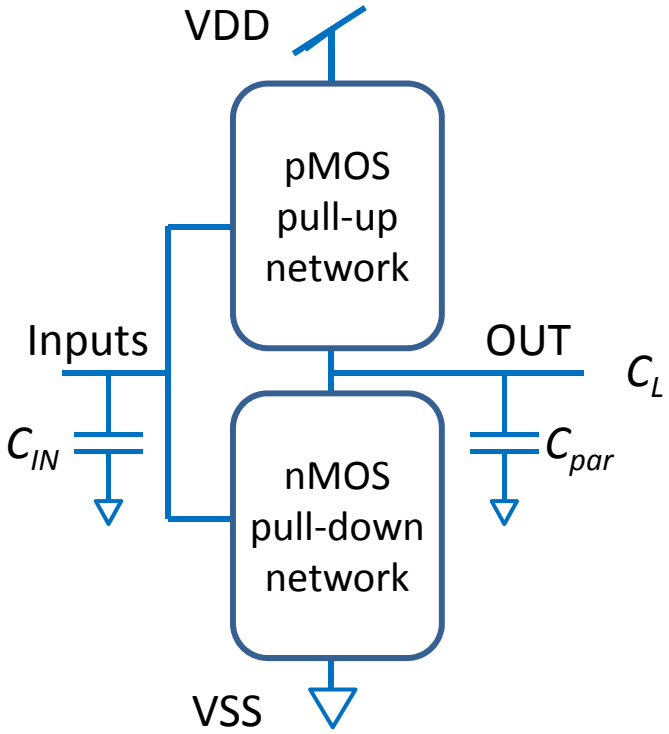
Inverter propagation delay model

Two-port electrical representation of propagation delay model

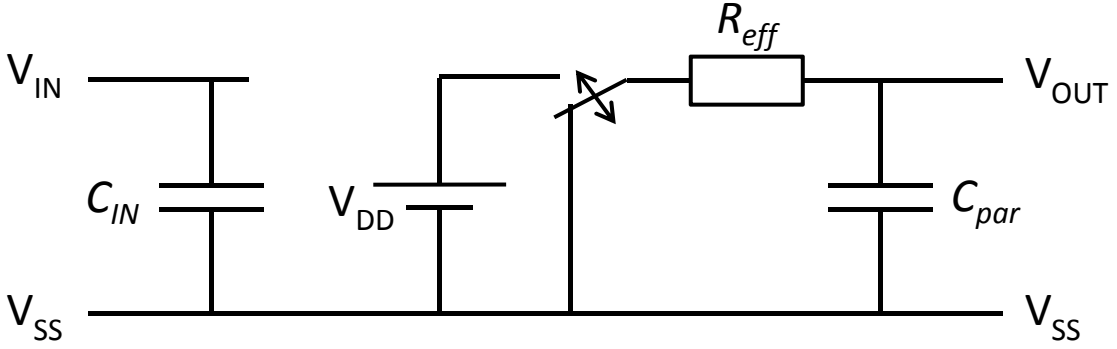


Logic gate propagation delay model

Now we want to apply the same model to any CMOS logic gate



The pull-up and pull-down networks may have many different paths, but we want to design for equal effective resistance R_{eff} in all paths!
But . . . what price do we have to pay for this in terms of input capacitance, C_{IN}?
And in parasitic capacitance, C_{par}?



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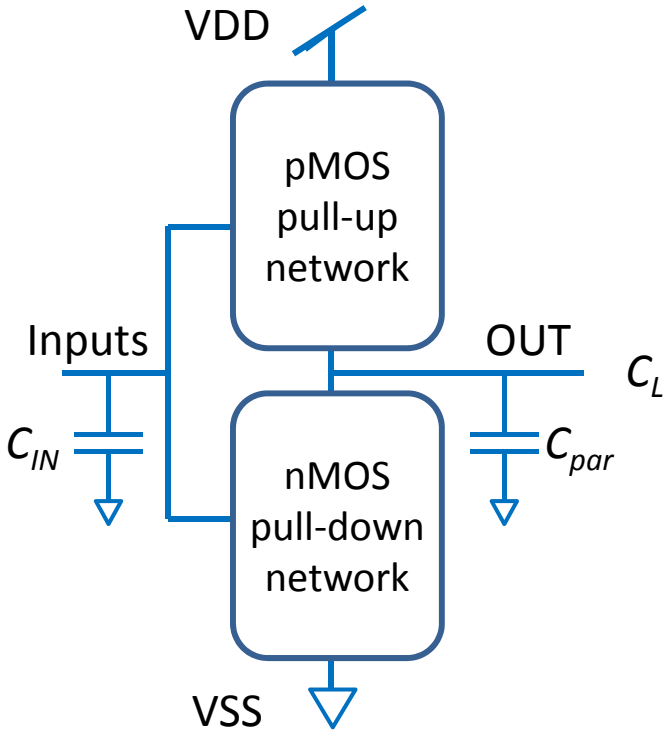
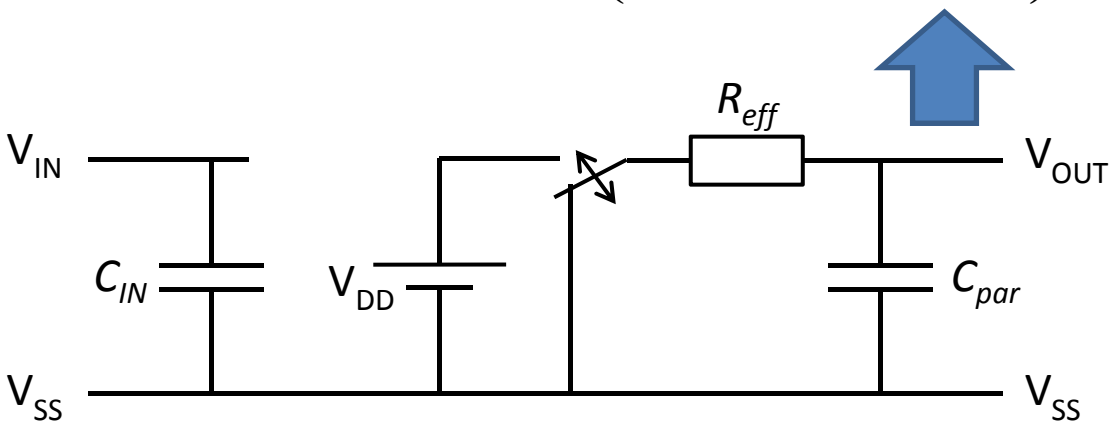


Assume all pull-up/down paths have same resistance R_{eff}.
Obviously, the logic gate will have larger RC product than the inverter! What is the delay with load C_L?
As before, normalize to inverter tau!

$$t_{pd} = 0.7 R_{eff}\left(C_{par} + C_L\right) = \tau\left(\frac{R_{eff}C_{par}}{\left(RC_G\right)_{inv}} + \frac{R_{eff}C_L}{\left(RC_G\right)_{inv}}\right)$$



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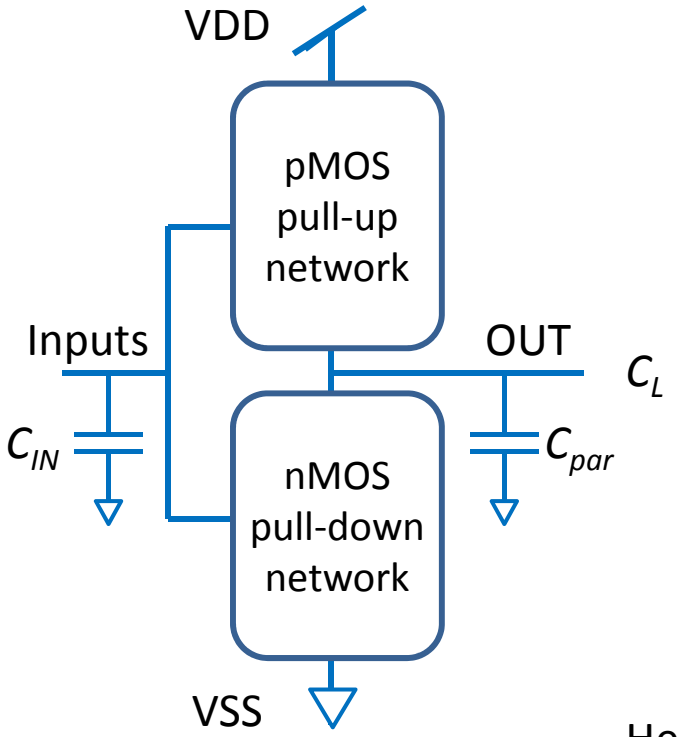


Consider one delay term at a time!

$$t_{pd} = 0.7 R_{eff}\left(C_{par} + C_L\right) = \tau\left(\frac{R_{eff}C_{par}}{\left(RC_G\right)_{inv}} + \frac{R_{eff}C_L}{\left(RC_G\right)_{inv}}\right)$$

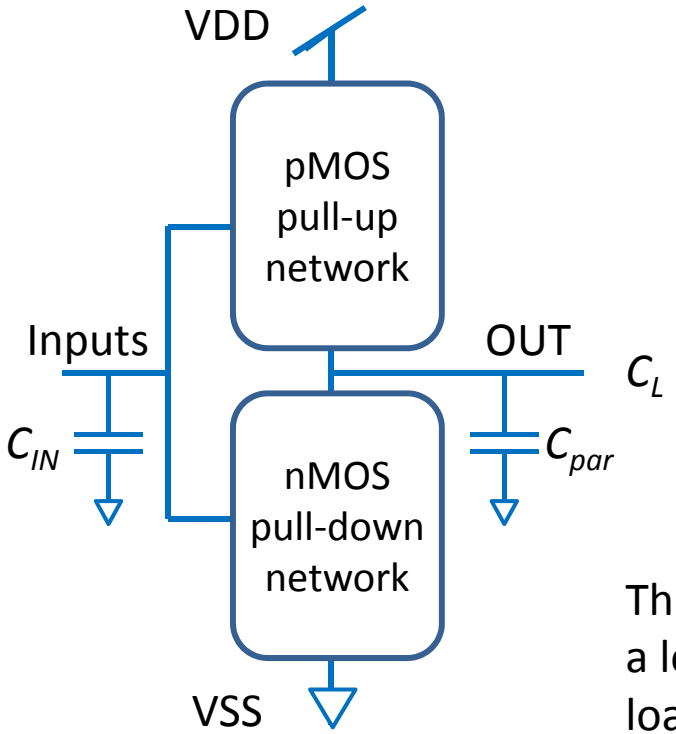
$$\text{parasitic delay: } p = \frac{R_{eff}C_{par}}{\left(RC_G\right)_{inv}} = \frac{R_{eff}C_{par}}{\left(RC_D\right)_{inv}}\underbrace{\frac{C_D}{C_G}}_{p_{inv}}$$

$$\text{stage effort: } f = \frac{R_{eff}C_L}{\left(RC_G\right)_{inv}} = \underbrace{\frac{R_{eff}C_{IN}}{\left(RC_G\right)_{inv}}}_{g}\underbrace{\frac{C_L}{C_{IN}}}_{h} = gh$$

Here, we have defined the logical effort of a logic gate, *g*
The logical effort tells us how much larger the logic gate RC product is wrt inverter RC product!

Logic gate propagation delay model

To simplify, I suggest sizing MOSFETs for equal effective resistances, i.e. $R_{eff}=R$



Consider one delay term at a time!

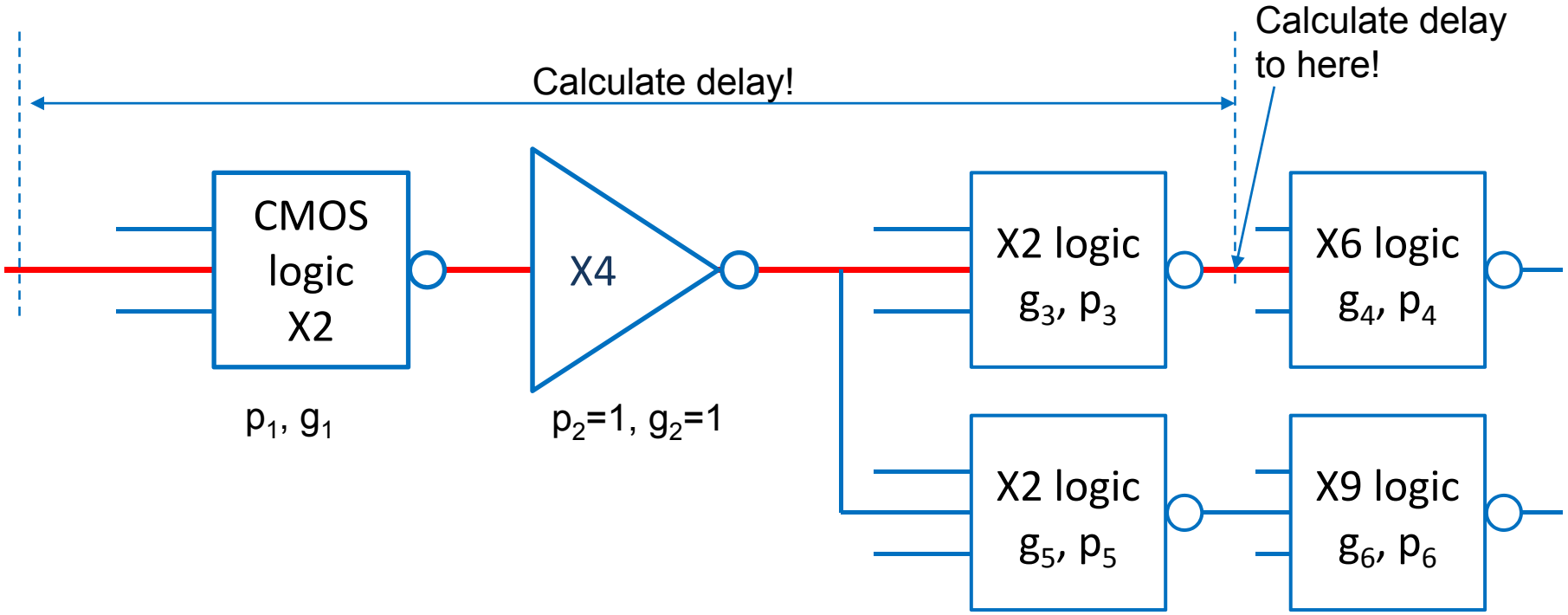
$$\text{parasitic delay: } p = \frac{RC_{par}}{(RC_G)_{inv}} = \frac{C_{par}}{C_D}\underbrace{\frac{C_D}{C_G}}_{p_{inv}}$$

$$\text{stage effort : } f = \frac{RC_L}{(RC_G)_{inv}} = \underbrace{\frac{C_{IN}}{C_G}}_{g}\underbrace{\frac{C_L}{C_{IN}}}_{h} = gh$$

This method conveniently separates the driving strength of a logic gate in terms of its logical effort, and its external load in terms of its electrical effort. And all with respect t to the properties of the inverter.

Delay estimations using logical effort

- Once the logical effort of a logic gate is known we can easily calculate the propagation delay of any critical timing path



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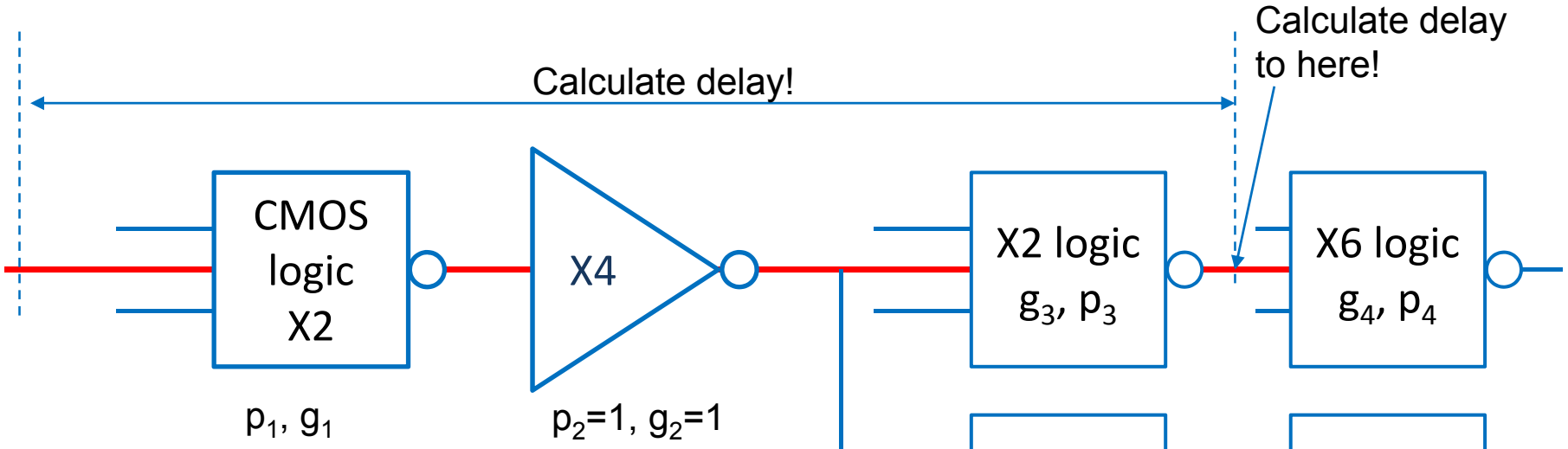
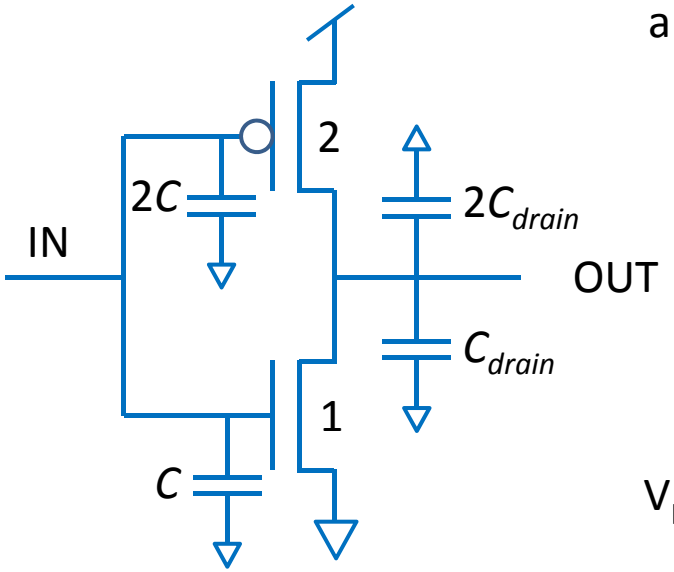


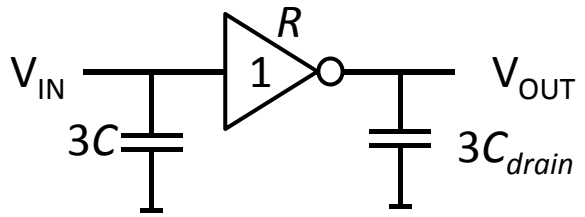
$$d = \underbrace{p_1 + g_1\frac{X4}{X2}}_{\text{1st stage}} + \underbrace{p_2 + \frac{2\times X2}{X4}}_{\text{inverter stage}} + \underbrace{p_3 + g_3\frac{X6}{X2}}_{\text{3rd stage}} =$$

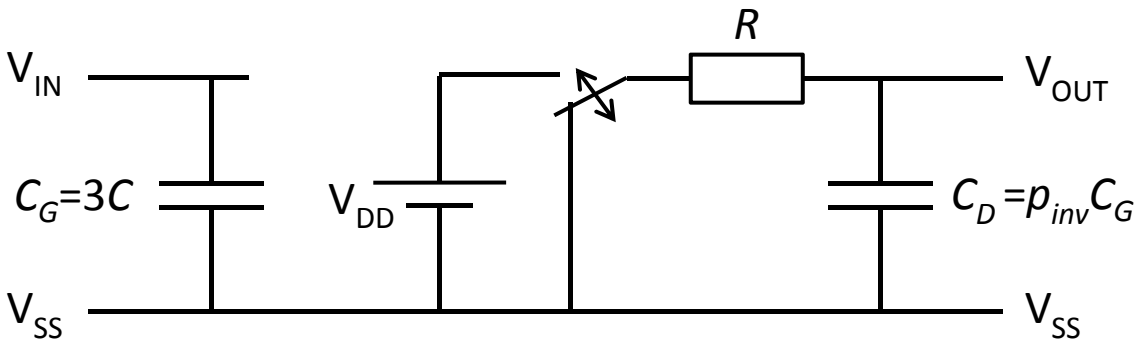
$$= \underbrace{p_1 + p_2 + p_3}_{\sum p} + \underbrace{2g_1 + 1 + 3g_3}_{\sum gh}$$

Inverter propagation delay model

Two-port electrical representation of propagation delay model
Consider a unit size inverter with a unit size n-channel device and a p-channel device of twice that width

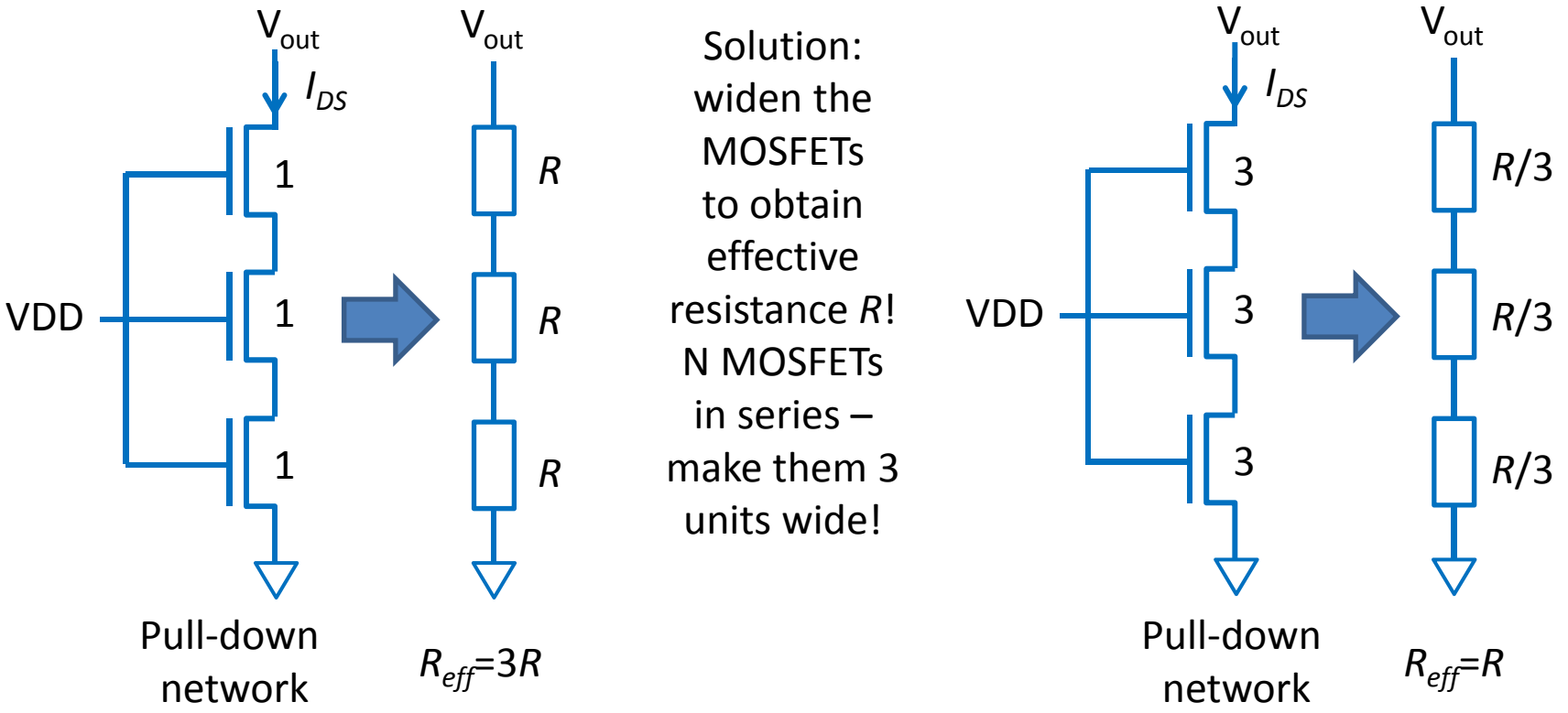






Effective resistance

- Pull-up/down paths may have MOSFETs in series! Effective resistances add up!



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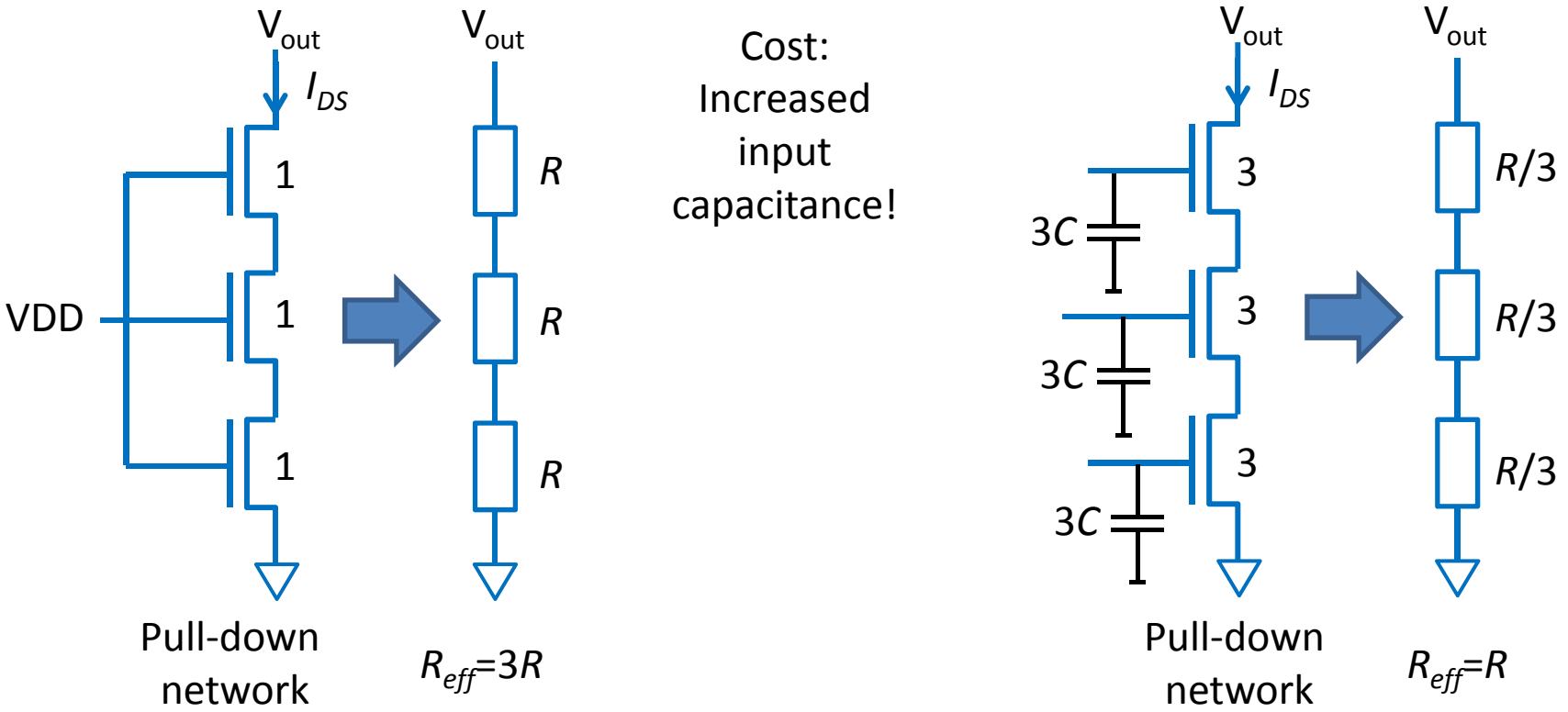
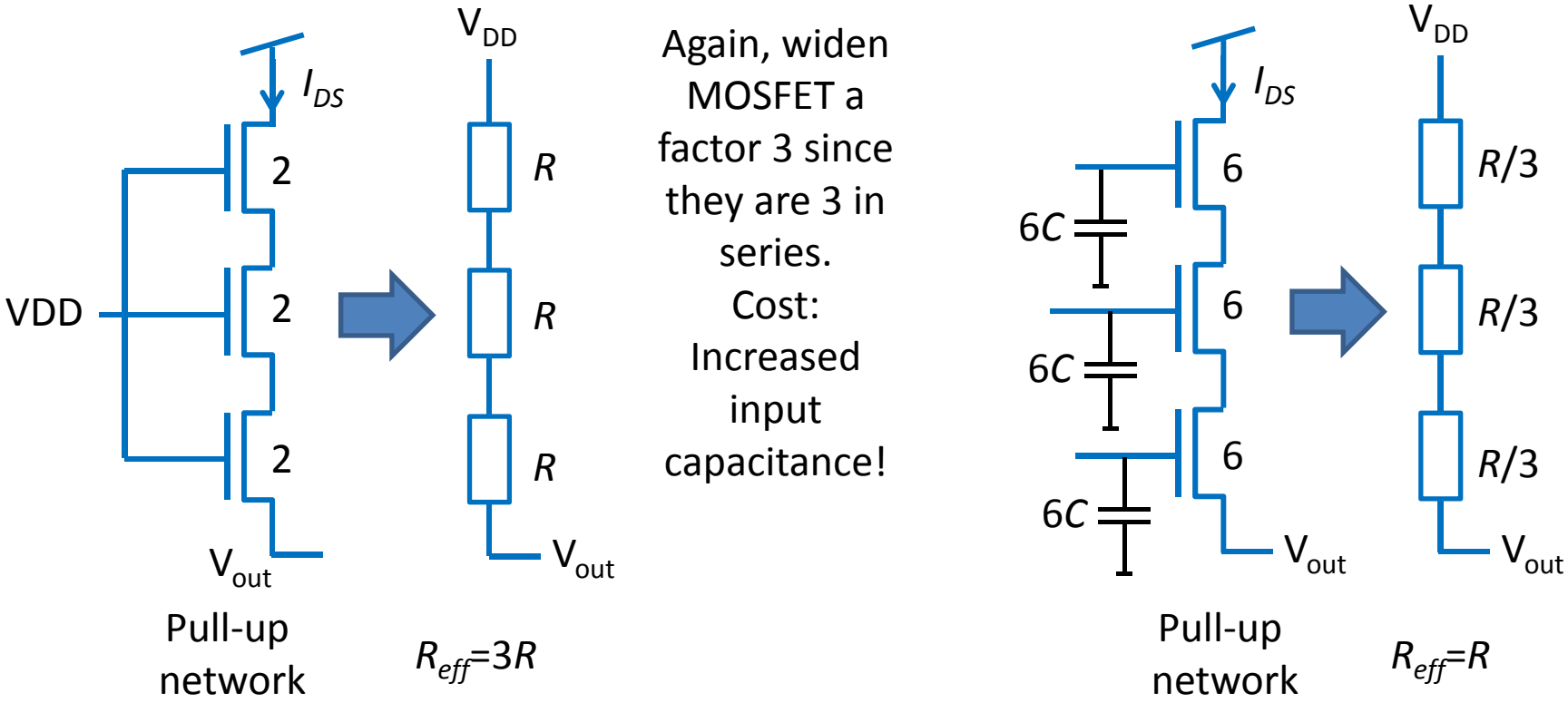


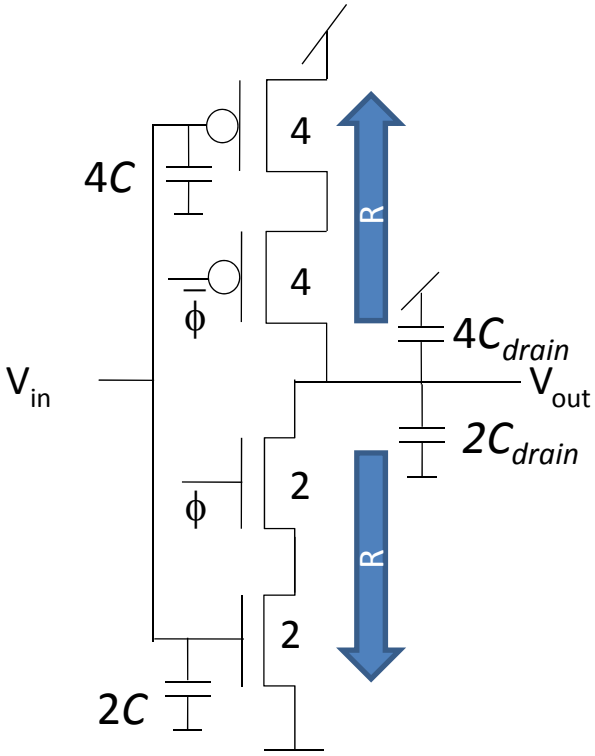
Effective resistance

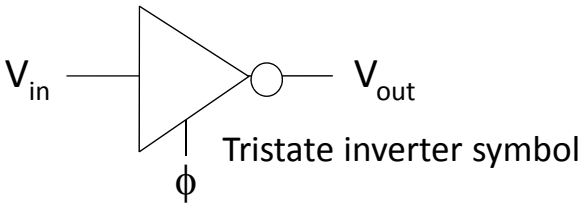
- Pull-up/down paths may have MOSFETs in series! Effective resistances add up! This is for p-channel devices!



Example 1: The tri-state inverter

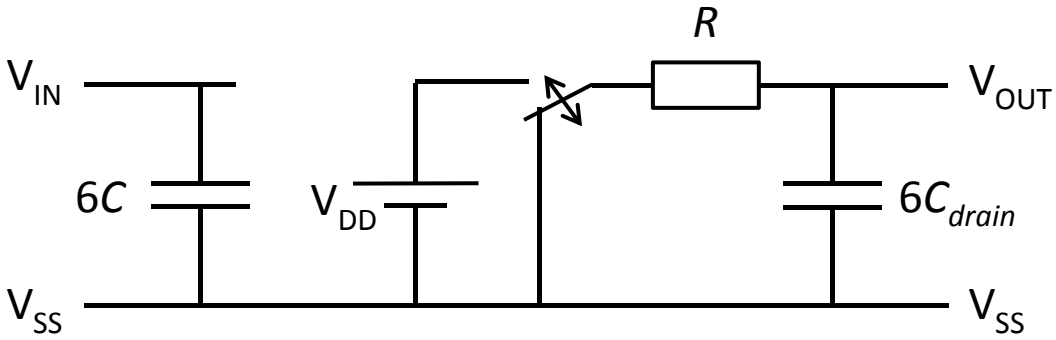
Make all MOSFETs twice as wide to cut effective resistance in half!





Input cap = twice that of reference inverter: $C_G=6C$ where C is gate capacitance of a unit width MOSFET

Parasitic output cap = $6C_{drain}$ which is twice that of the unit inverter



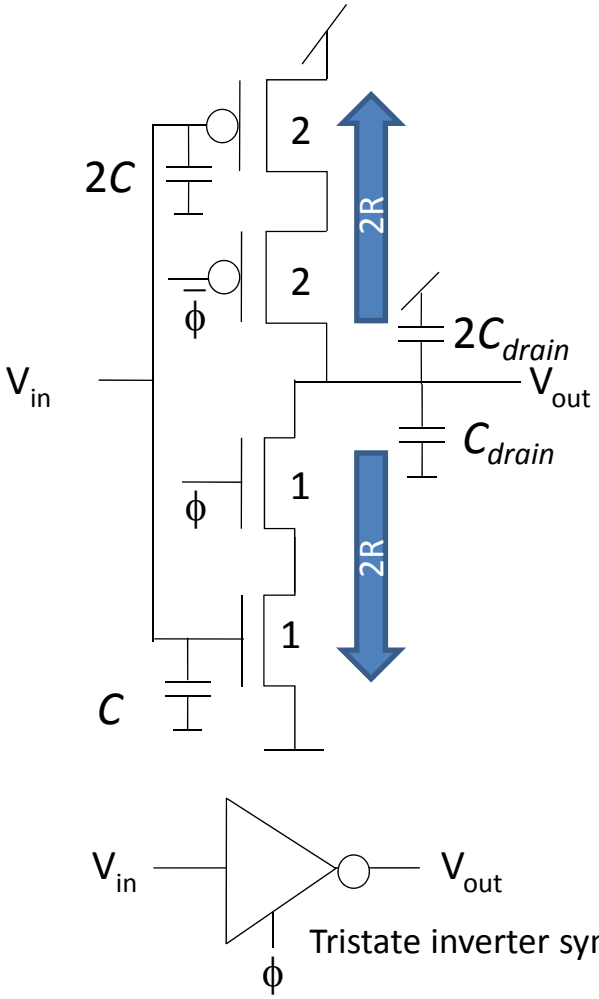
While inverter RC-product is $3RC$, tristate inverter RC-product is $6RC$, i.e. twice that of the inverter!

This ratio is defined as the "logical effort", g, and $g=6C/3C=2$!

Parasitic delay $=6C_{drain}/3C=2p_{inv}$

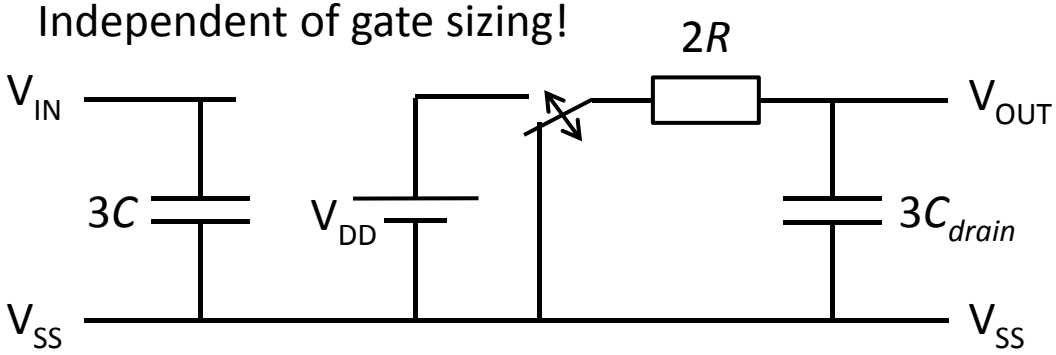
Example 1: The tri-state inverter

Make all MOSFETs at original widths to keep input capacitances @ 3*C*.



Say that we want input capacitance to be same as for the inverter! Then path resistances become 2R!

But parasitic delay and logical effort are the same! Independent of gate sizing!

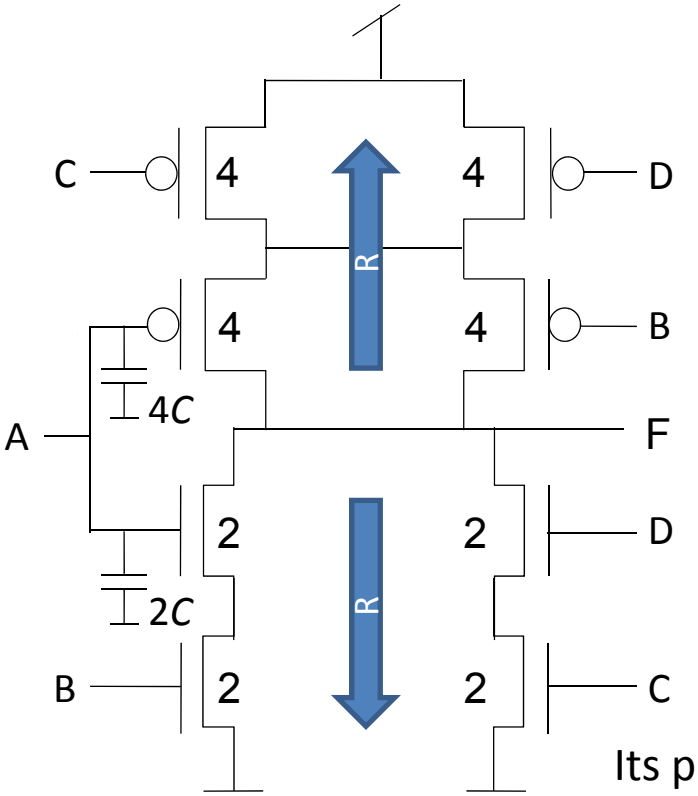


While inverter *RC*-product is 3*RC*, tristate inverter *RC*-product is 6*RC*, i.e. twice that of the inverter!

Because $R \sim \frac{1}{W}$ and $C \sim W$. Hence RC is constant!

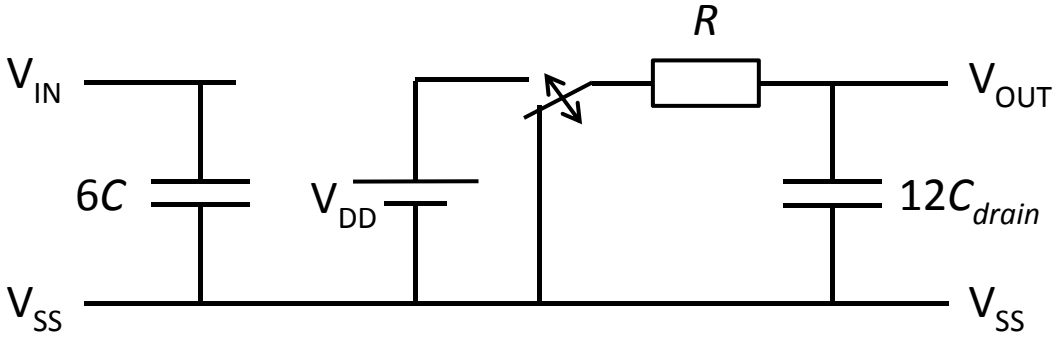
Example 2: 2+2 AND-OR-invert (AOI22)

Make all MOSFETs twice as wide to cut effective resistance in half!



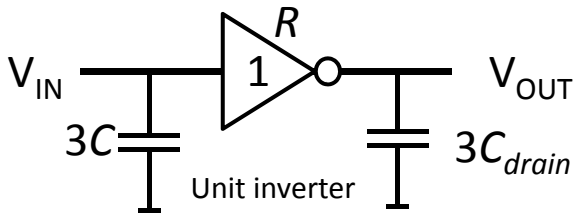
This gate also has logical effort, g=2

$$g = \frac{\left(R_{eff} C_{IN}\right)}{3RC} = \frac{6RC}{3RC} = 2$$

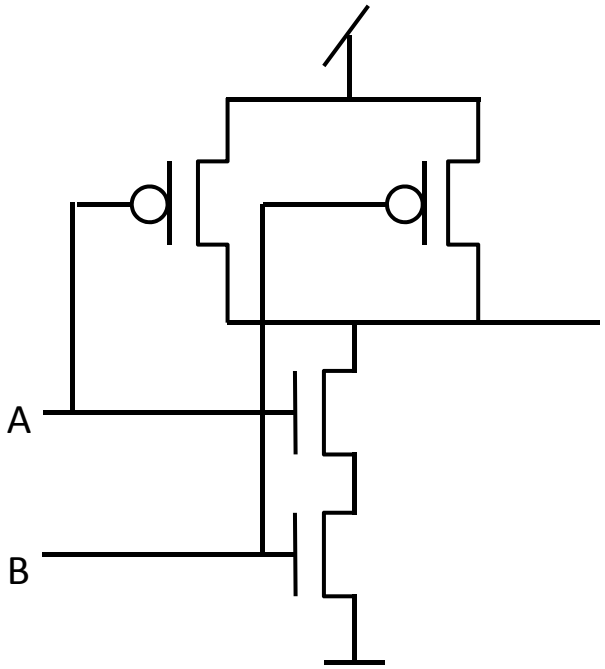


Its parasitic *RC*-product *p, the parasitic delay,* is defined as

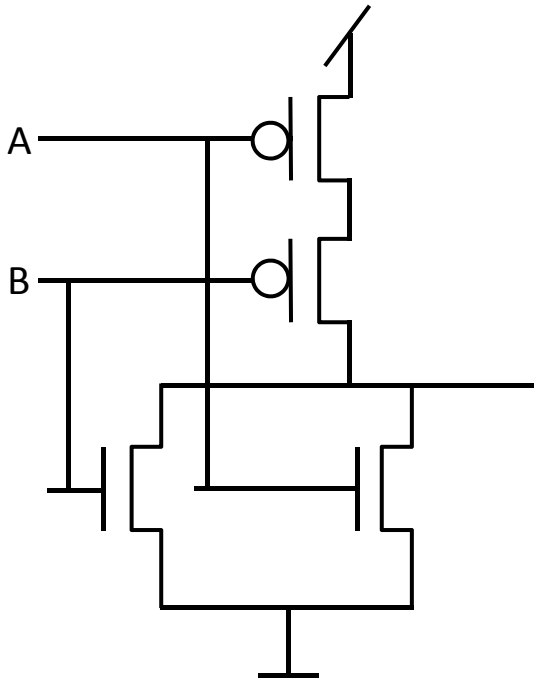
$$p = \frac{\left(R_{eff} C_{par}\right)}{3RC} = \frac{12RC_{drain}}{3RC} = 4\frac{C_{drain}}{C} = \begin{cases} 4 \text{ if } p_{inv} = 1.0 \\ 3.2 \text{ if } p_{inv} = 0.8 \end{cases}$$



Exercise:
Calculate NAND2 NOR2 logical efforts

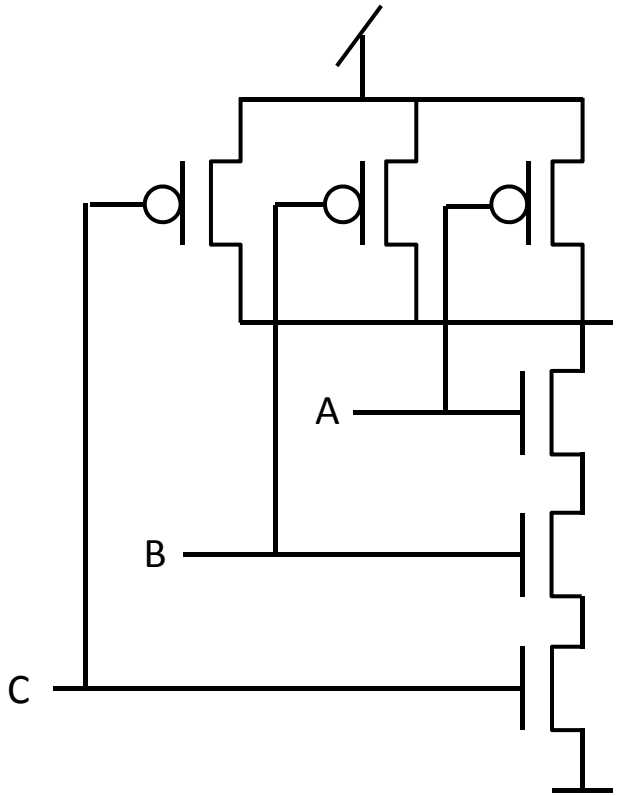


NAND2

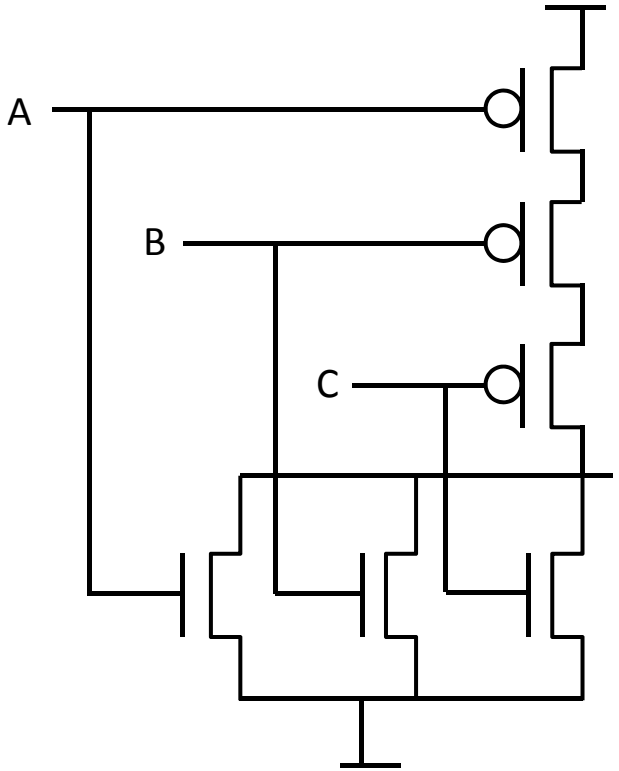


NOR2

Exercise:
Calculate NAND3 & NOR3 logical efforts



NAND3

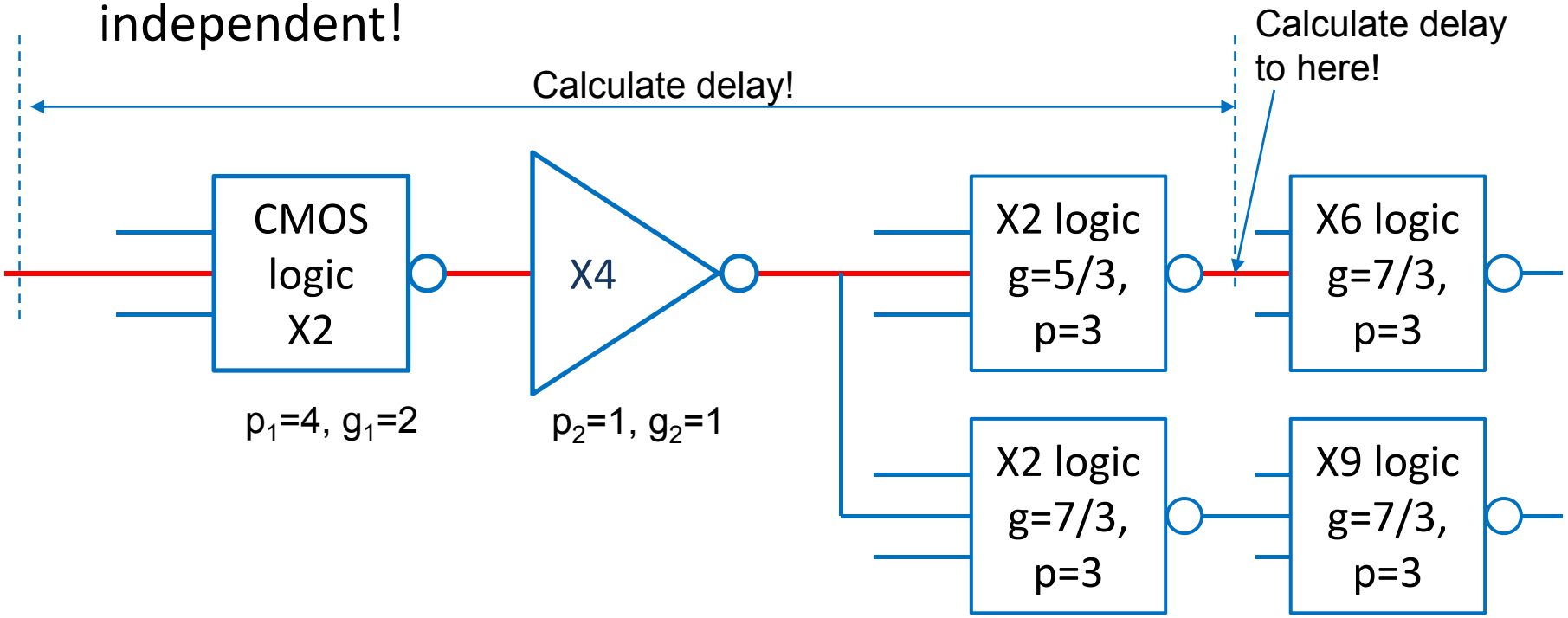


NOR2

Why all this?

In ST cell library, size X refers to the input cap!

- Simplify delay calculations and making them technology independent!



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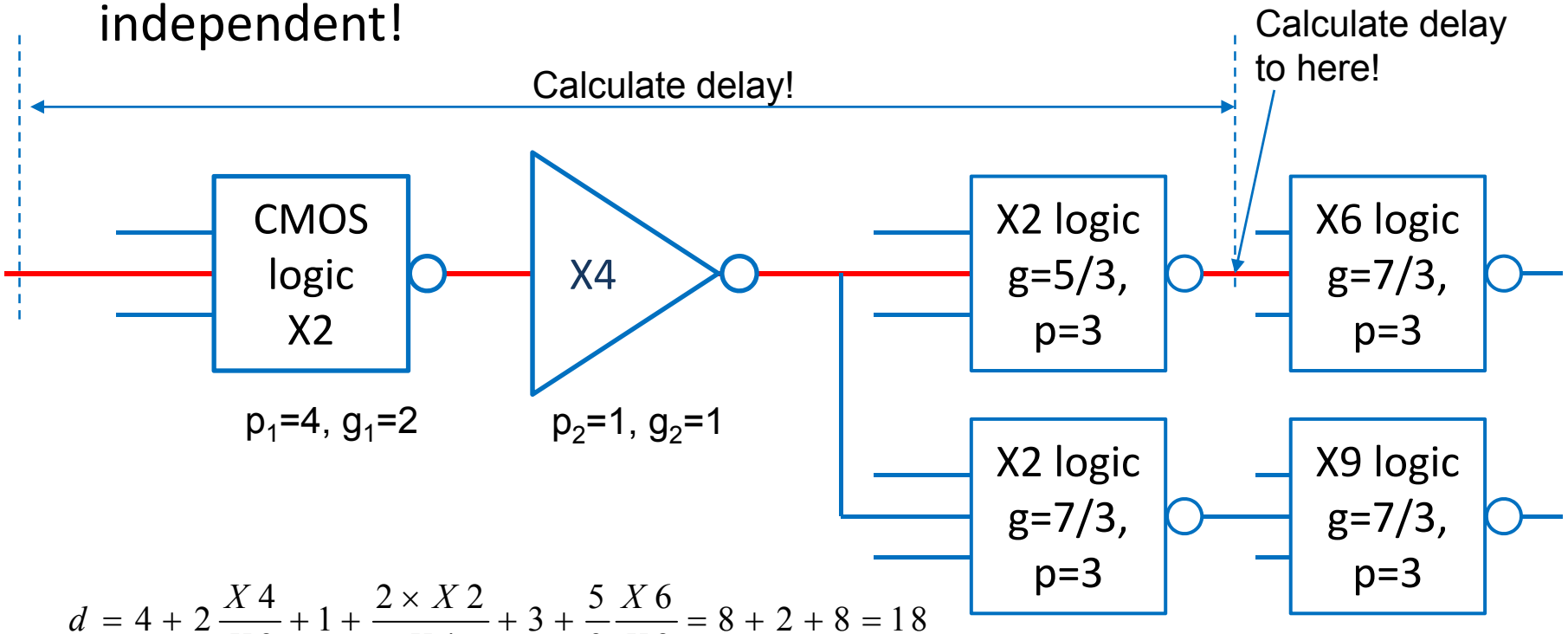
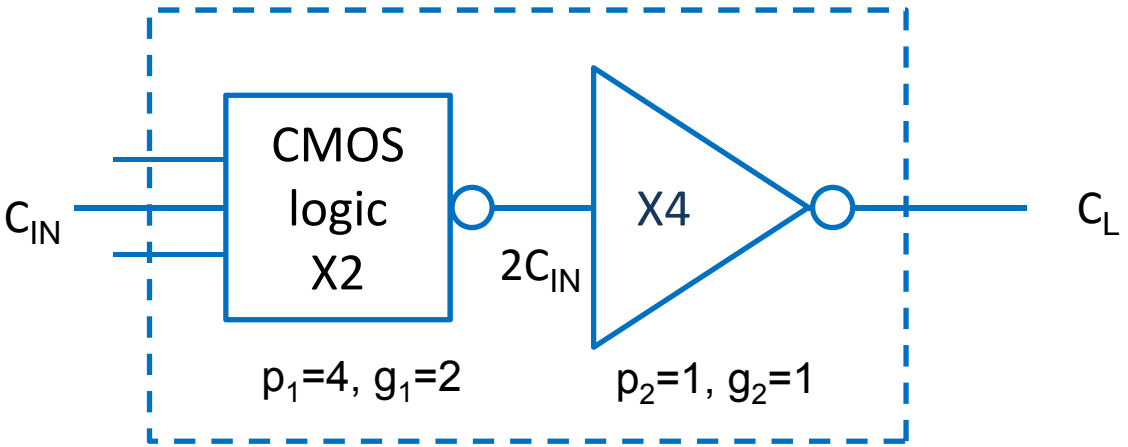


$$d = \underbrace{4 + 2\frac{X4}{X2}}_{\text{1st stage}} + \underbrace{1 + \frac{2 \times X2}{X4}}_{\text{inverter}} + \underbrace{3 + \frac{5}{3}\frac{X6}{X2}}_{\text{3rd stage}} = 8 + 2 + 8 = 18$$

Propagation delay=18*tao=90 ps

Non-inverting gate



$$d = \underbrace{4 + 2\frac{X4}{X2}}_{\text{1st stage}} + \underbrace{1 + \frac{C_L}{2C_{IN}}}_{\text{inverter}} = \underbrace{9}_{p} + \underbrace{\frac{1}{2}}_{g}\underbrace{\frac{C_L}{C_{IN}}}_{h}$$

The parasitic delay p=9
Logical effort g=0.5

Conclusion

In this lecture we have

- Adapted the two-port delay model previously developed for inverters to any CMOS logic gate
- Learnt how to size MOSFETs for equal worst case rise and fall delay
- Noticed that logic gates have larger $R_{eff}C_G$-products than inverters
- Introduced two new concepts: *logical effort* and *parasitic delay*
- Logical effort and parasitic delay quantifies
  - Logical effort: $(R_{eff}C_G)_{gate}$ relative to $(3RC)_{inv}$
  - Parasitic delay: $(R_{eff}C_{par})_{gate}$ relative to $(3RC)_{inv}$
- Learnt how to calculate these parameters of any logic gate
- Learnt how to calculate the electrical effort $h = C_{LOAD}/C_{IN}$
- Learnt to calculate all propagation delays as a multiple of tau, where tau=5 ps in STMicroelectronics 65 nm CMOS process