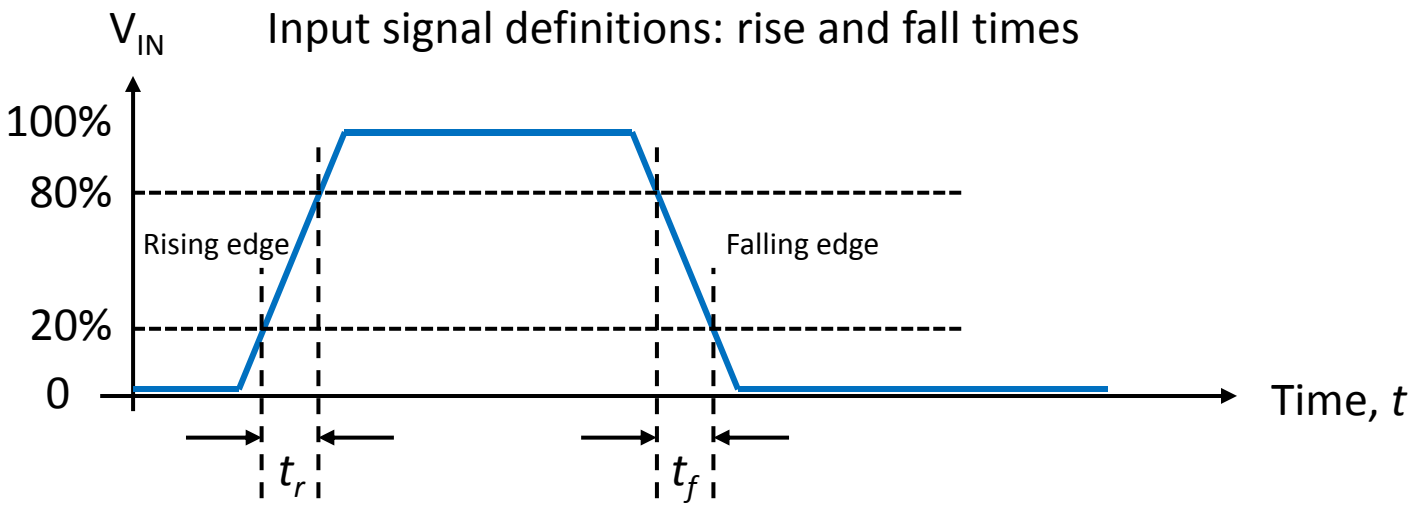
# Lecture 4
# The CMOS Inverter

Dynamic properties

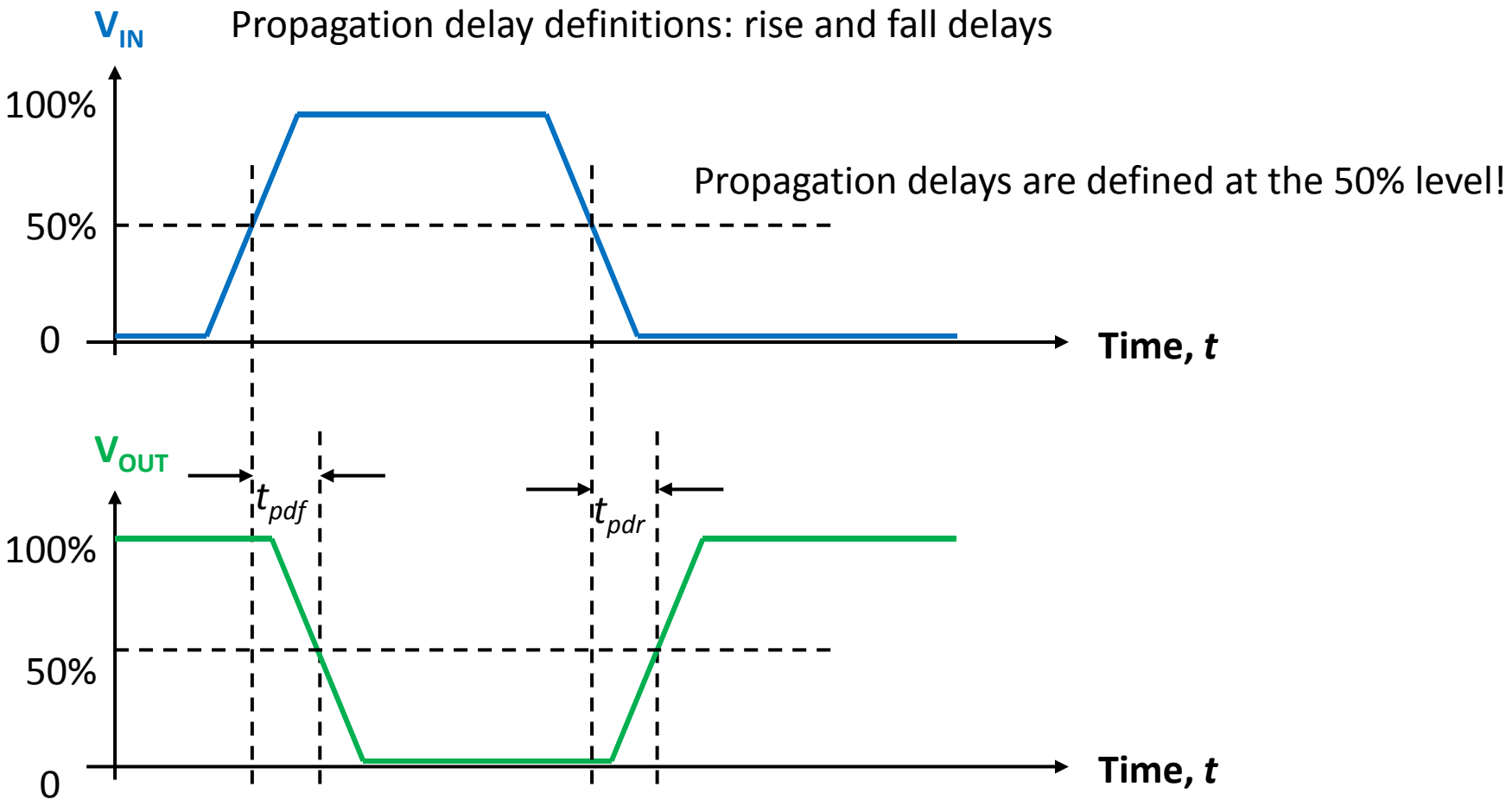
# Outline

- Definitions
  - Static properties (dV/dt=0 ) vs. dynamic properties (dV/dt≠0)
  - Rise time and fall time
  - Propagation delay: Rise delay and fall delay
- Propagation delay estimation
  - Step response model
    - Charging and discharging the load capacitor
  - Ramp response model
    - Introducing the MOSFET effective resistance
- Inverter capacitances
- Normalizing the inverter delay wrt $\tau$=0.7RC
- Inverter pair delay
- The fanout-of-four (FO4) delay
- The tapered buffer

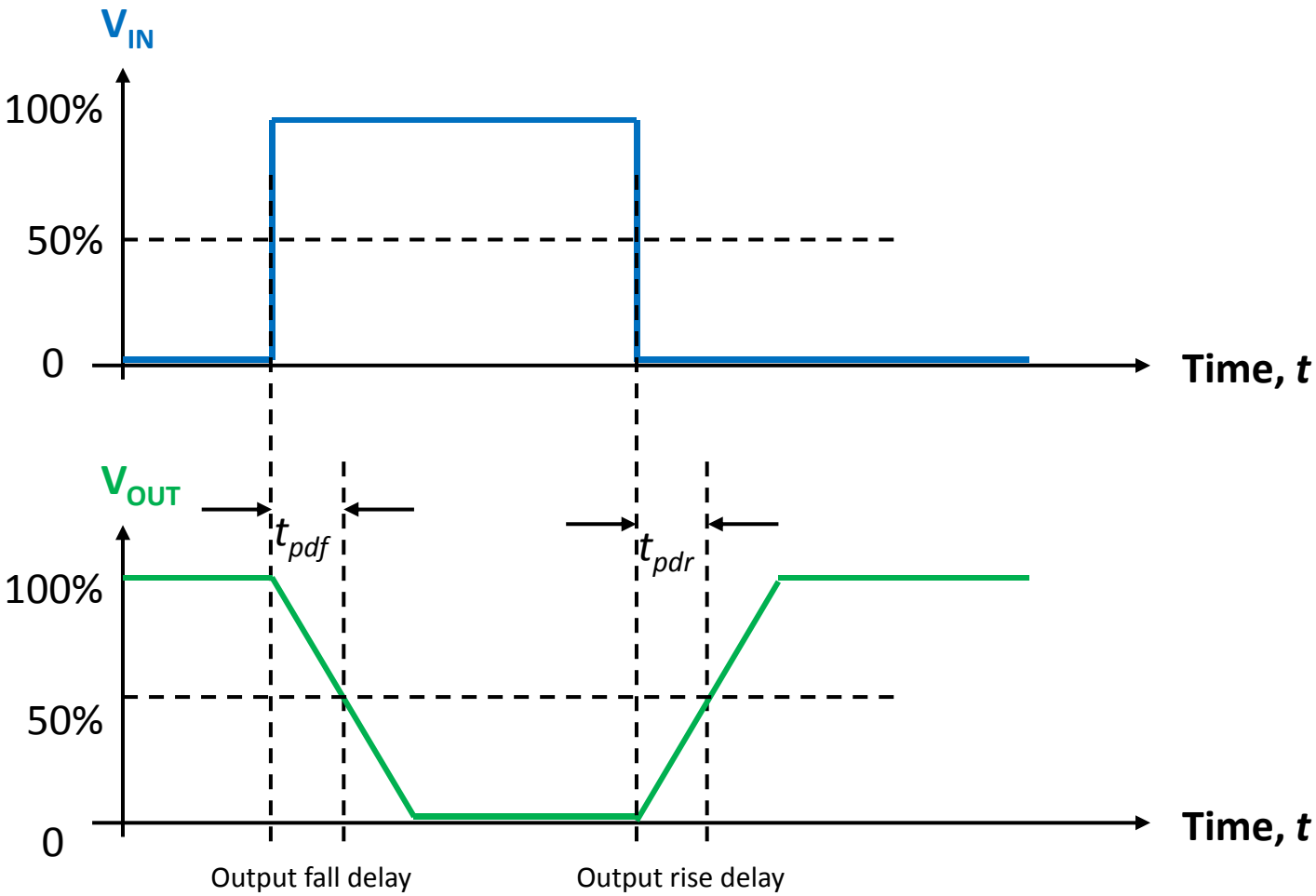
# Definitions



# Definitions

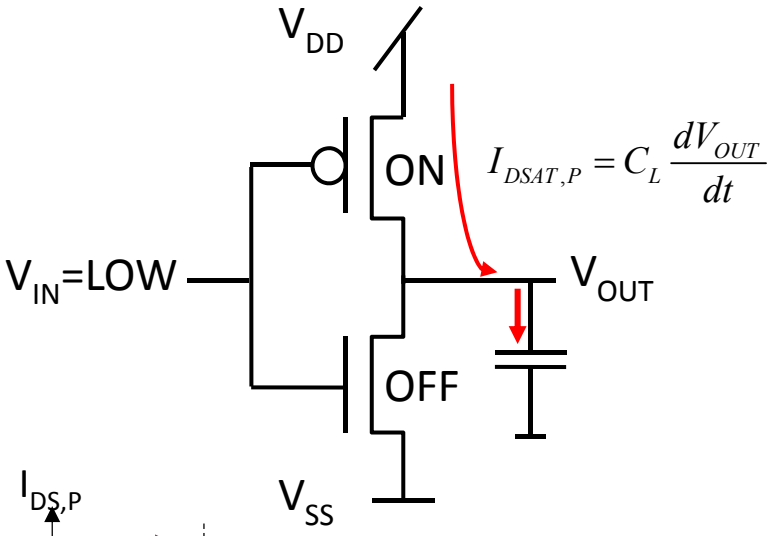


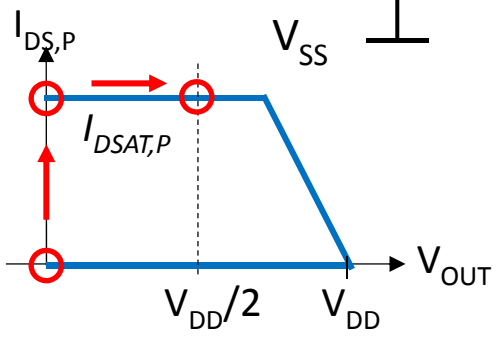
# Step-response model



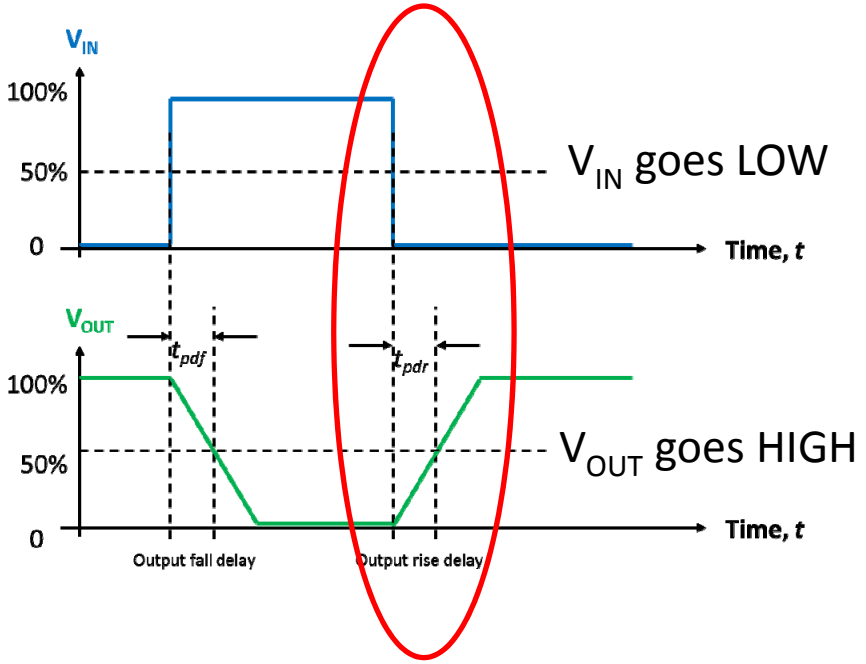
# Step-response model

1. Charging the load capacitor through the p-channel MOSFET



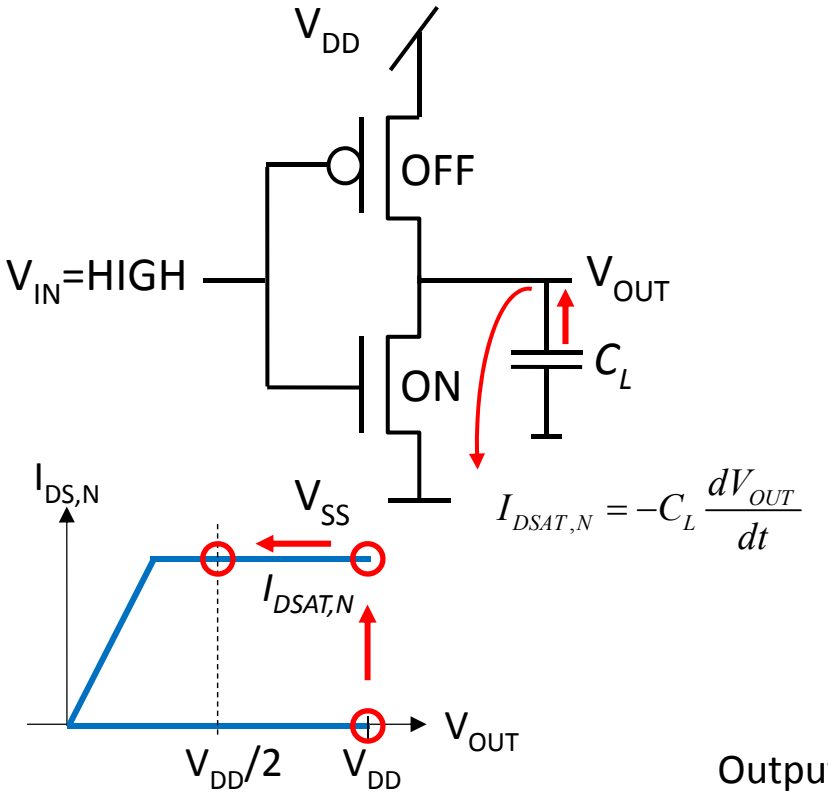

pMOS current flow in detail



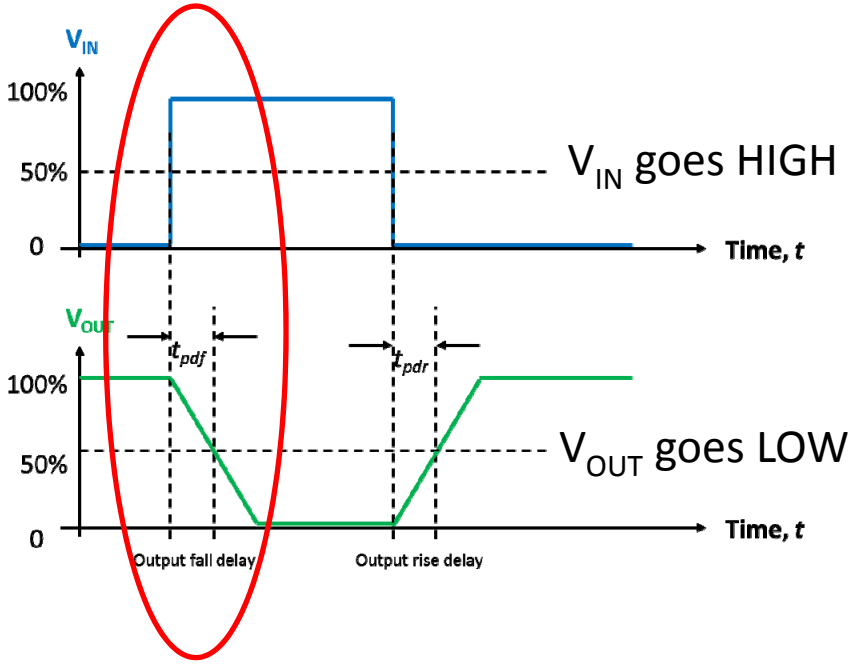

Output rise delay $t_{pdr} = C_L \frac{V_{DD}/2}{I_{DSAT,P}}$

# Step-response model

2. Discharging the load capacitor through the n-channel MOSFET




$$I_{DSAT,N} = -C_L \frac{dV_{OUT}}{dt}$$

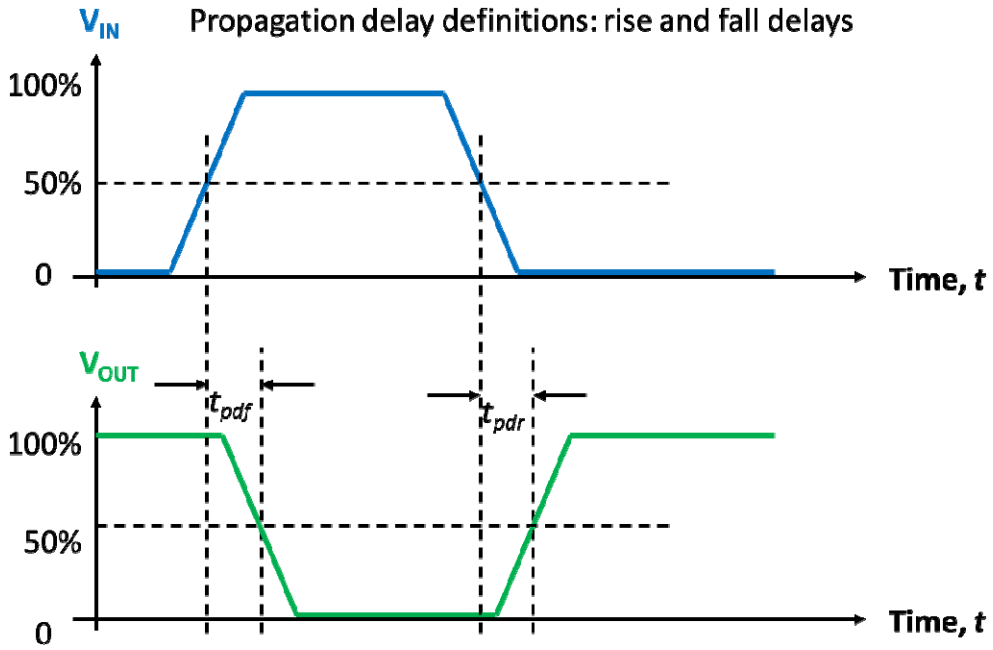



Output fall delay $t_{pdf} = C_L \frac{V_{DD}/2}{I_{DSAT,N}}$

nMOS current flow in detail

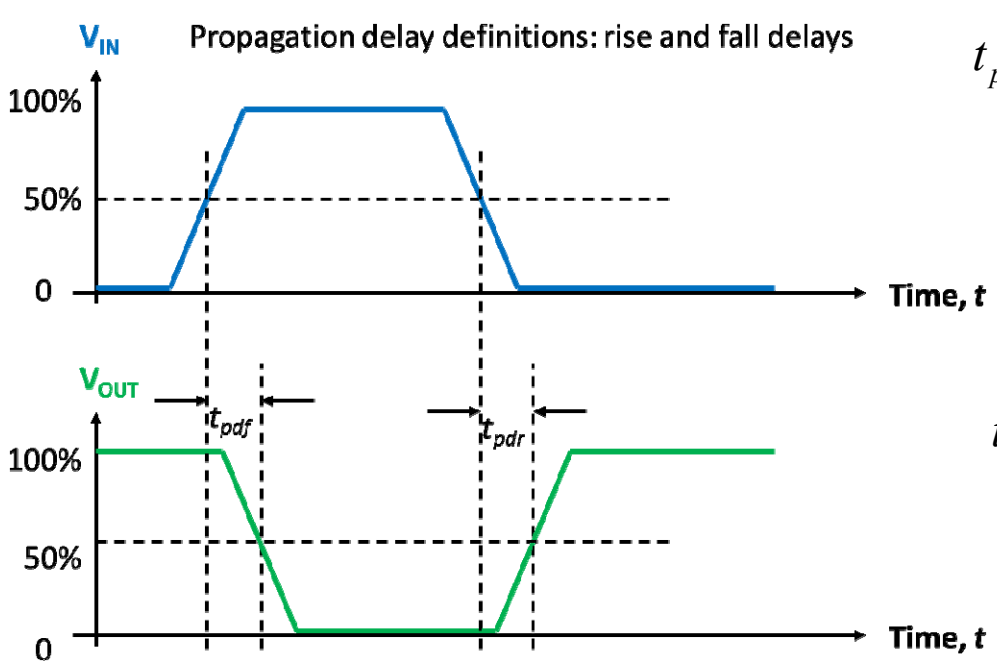
# Step response model accuracy

- How good is the step response model?
- Real world input voltages are not step functions
- They are output voltages from other gates



# Step response model accuracy

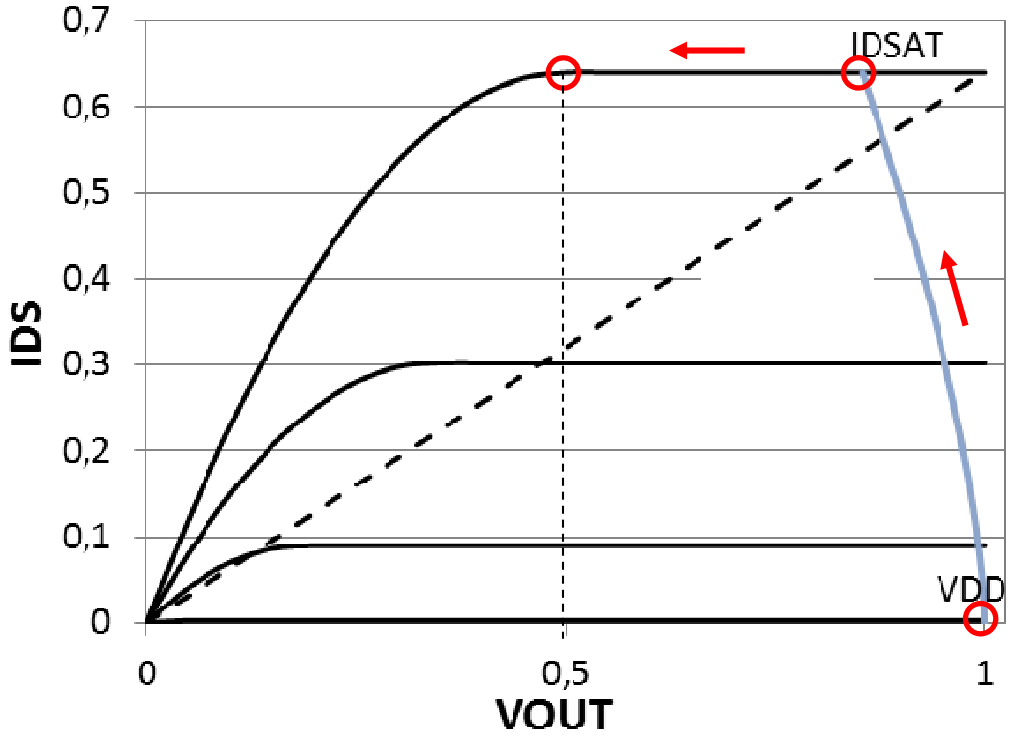
- Experience and hundreds of circuit simulations show that propagation delay are about 40% longer in designs where input and output edge rates are equal




$$t_{pd} = C_L \frac{V_{DD}/2}{I_{DSAT}}$$

$$t_{pd} = 0.7 C_L \frac{V_{DD}}{I_{DSAT}}$$

# Ramp input – output trace



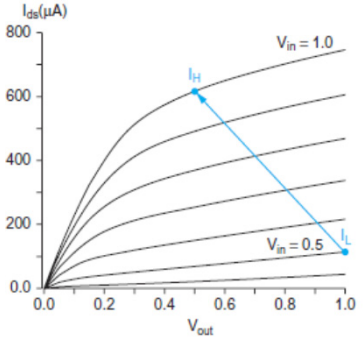
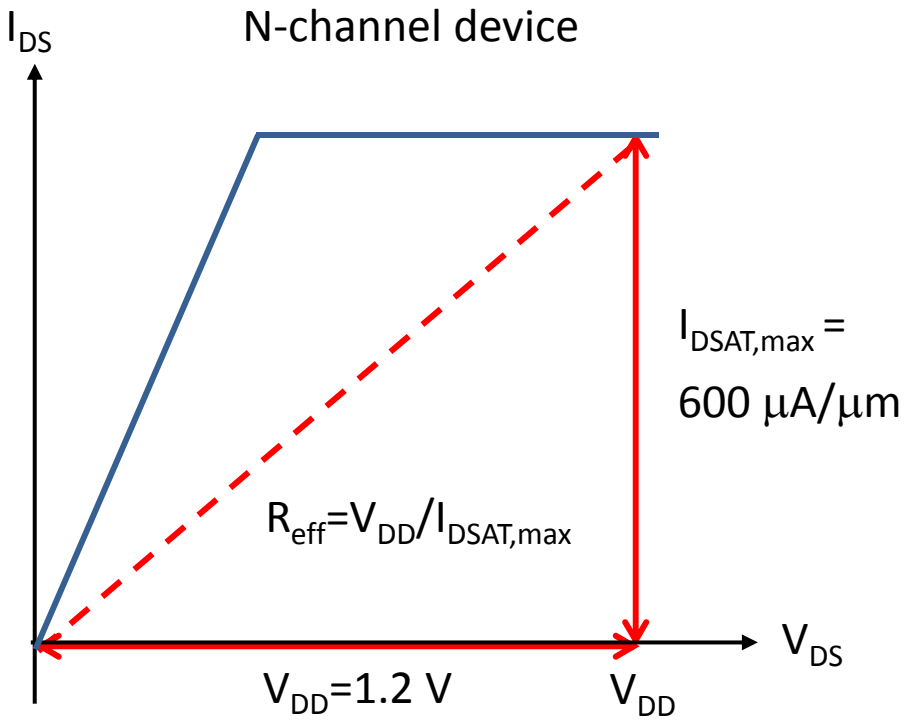



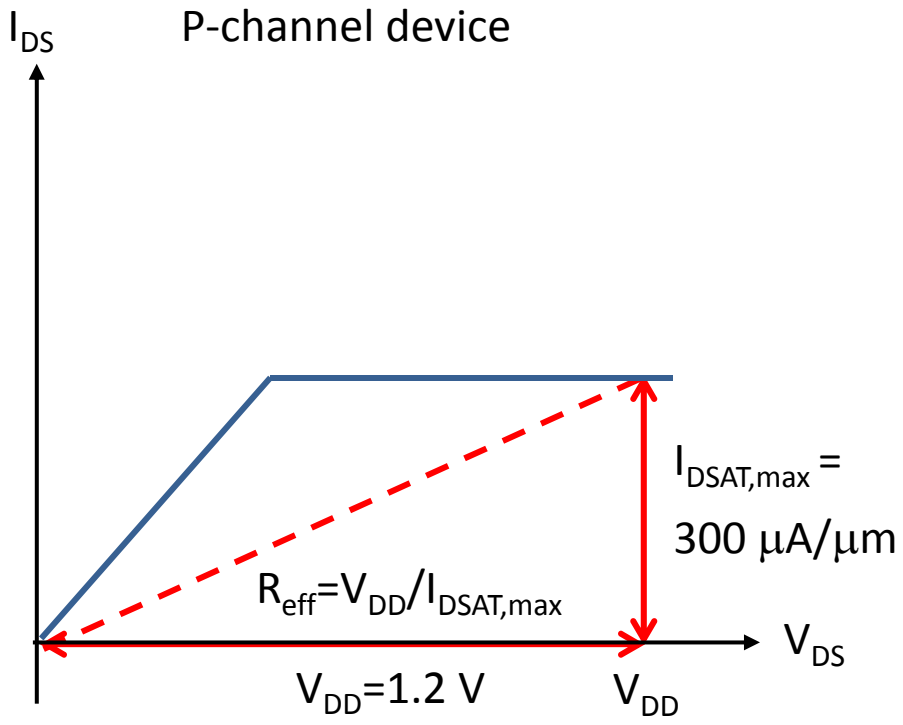

FIGURE 4.20 Approximate switching trajectory

# Effective resistances: 65 nm MOSFETs

$R_{N,eff}$=2 kΩ·µm




$R_{P,eff}$=4 kΩ·µm

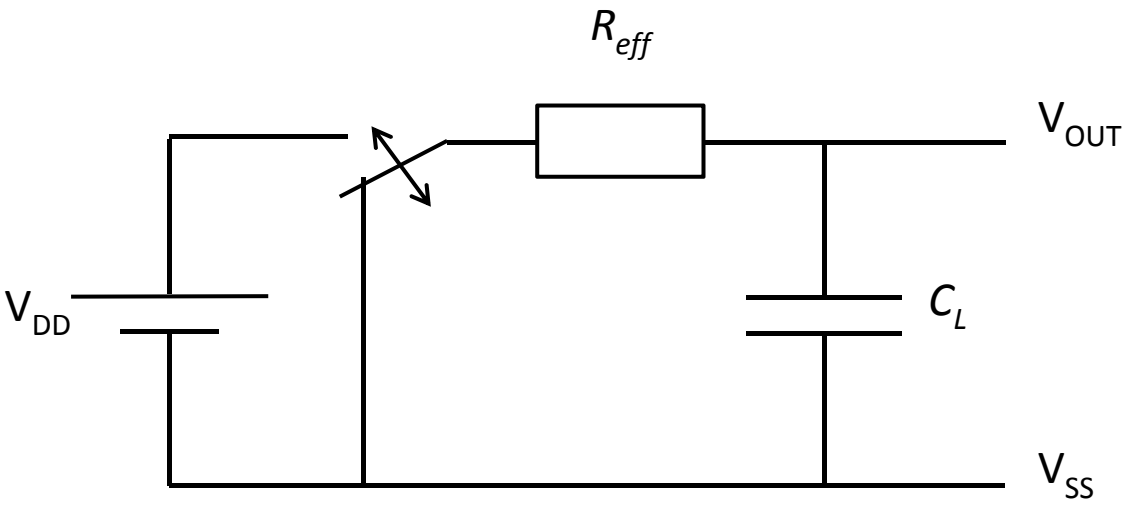



$$t_{pd} = 0.7 C_L \frac{V_{DD}}{I_{DSAT}} \Rightarrow t_{pd} = 0.7 R_{eff} C_L$$

# RC delay

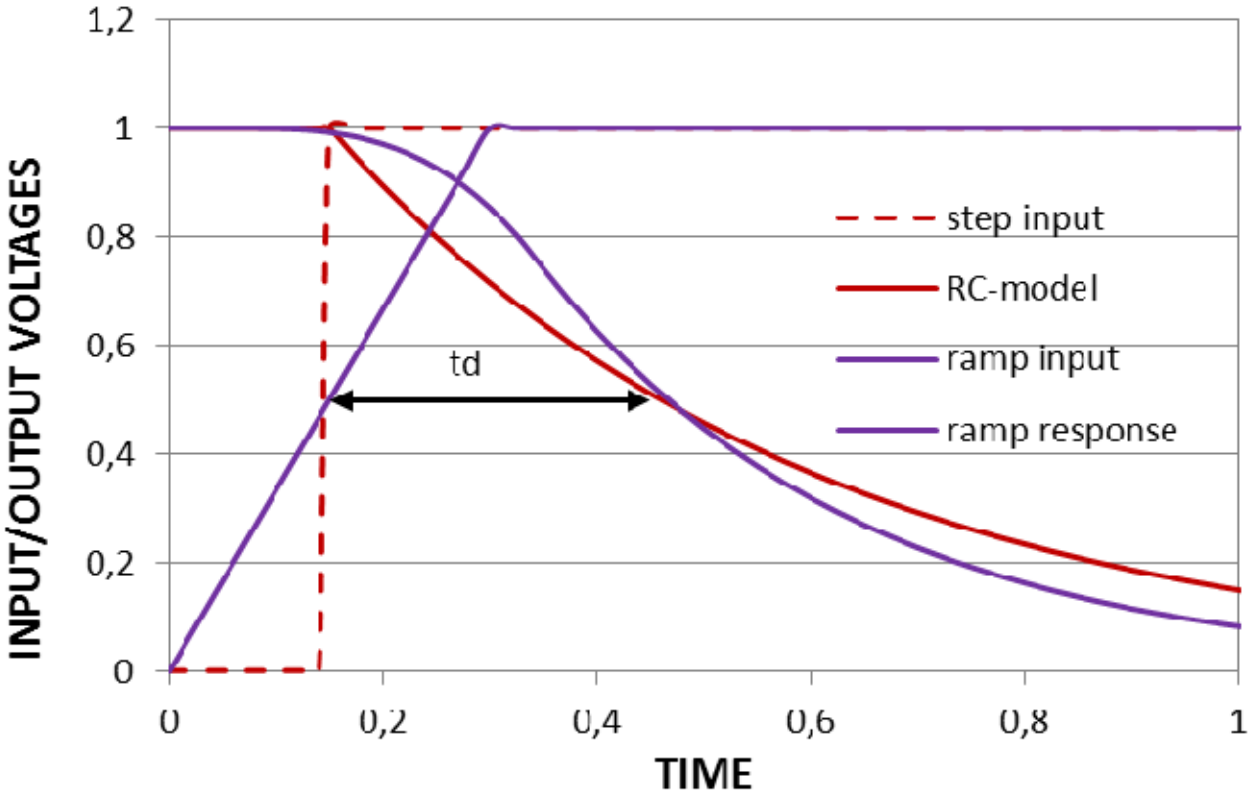
This RC circuit has an output voltage delay given by

$$t_{pd} = 0.7 R_{eff} C_L$$



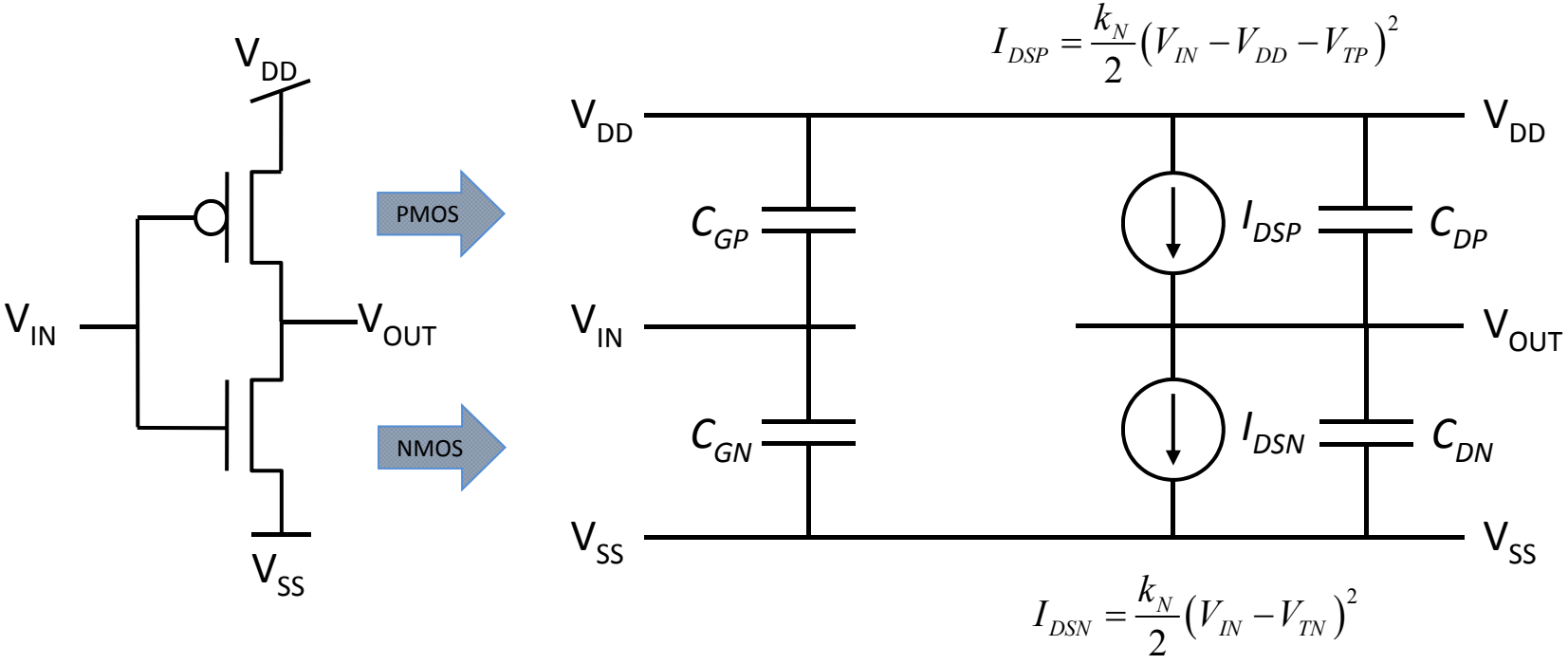
# Ramp input – output response

The two curve forms are not the same, but they yield the same delay!



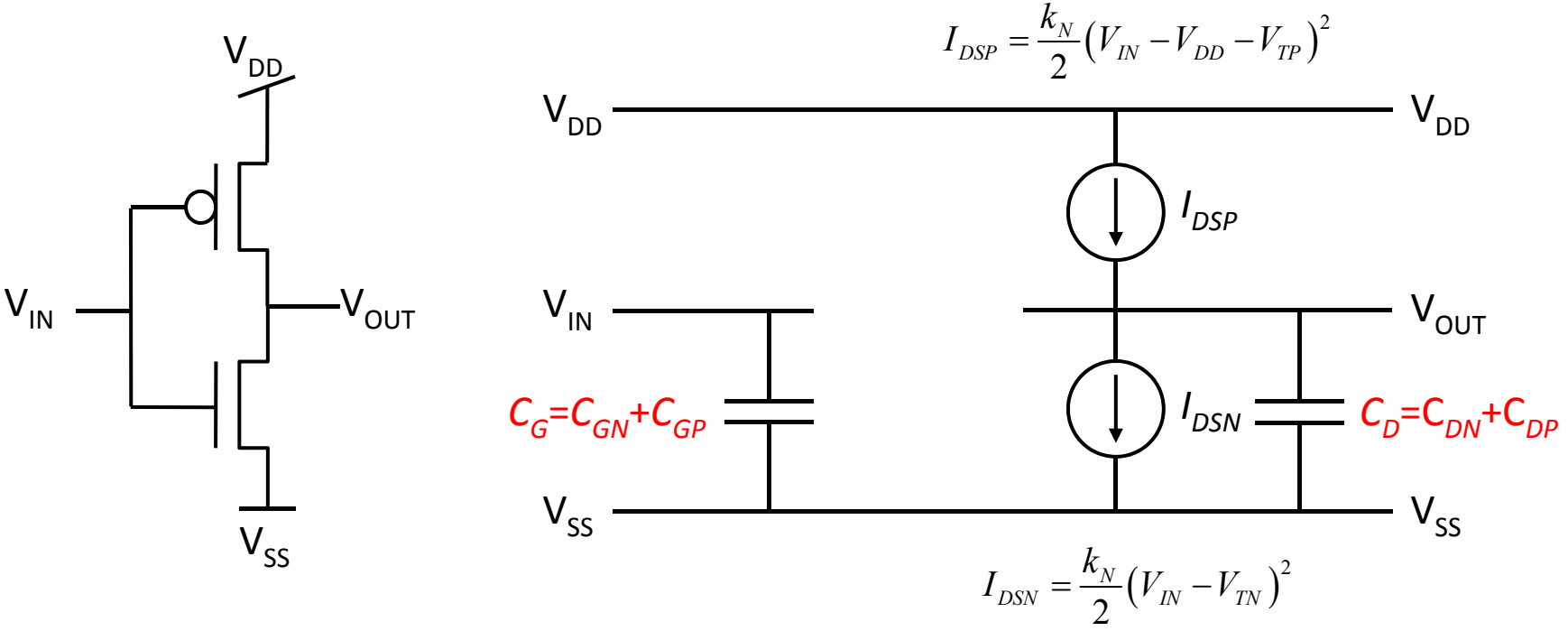
# The inverter and its electrical model

Replace the MOSFETs with their equivalent electrical circuits!



# The inverter and its electrical model

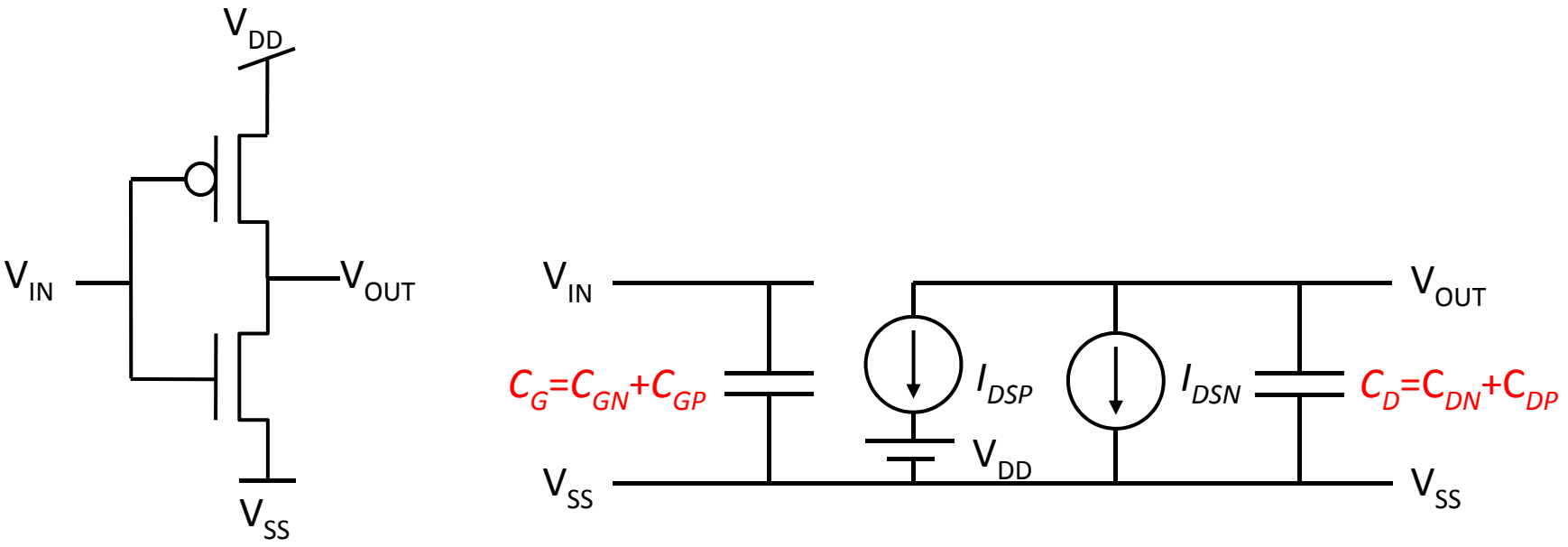
Place all capacitor to signal ground! Both rails are constant voltages, no dV/dt




Inverter input capacitance: $C_G = C_{GN} + C_{GP}$; MOSFET gate capacitances add!
Inverter parasitic output capacitance: $C_D = C_{DN} + C_{DP}$. Drain caps also add!

# The inverter and its electrical model

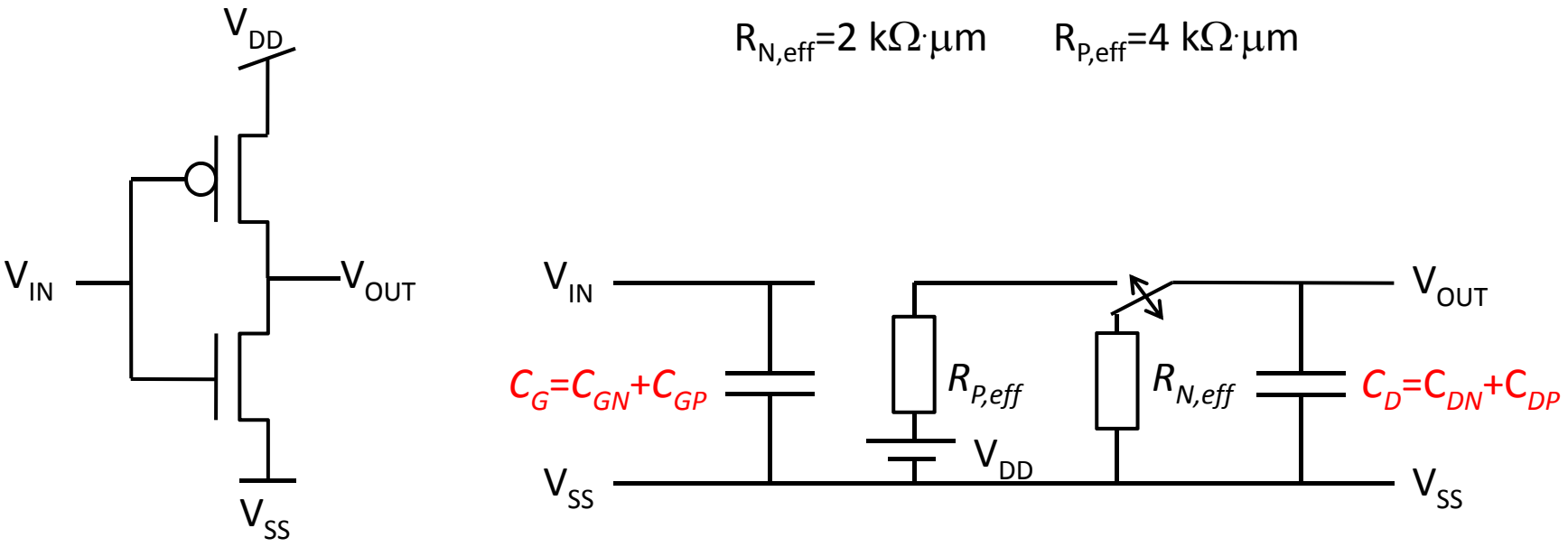
Eliminate VDD rail by inserting power supply to signal ground!




Inverter input capacitance: $C_G=C_{GN}+C_{GP}$; MOSFET gate capacitances add!
Inverter parasitic output capacitance: $C_D=C_{DN}+C_{DP}$. Drain caps also add!

# The inverter and its electrical model

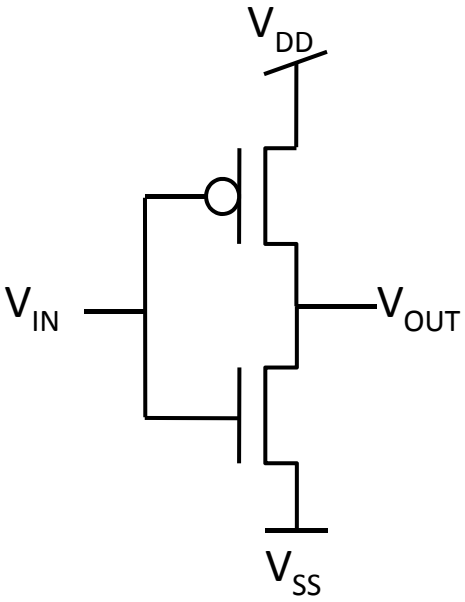
Replace MOSFET constant-current sources with their effective resistances!



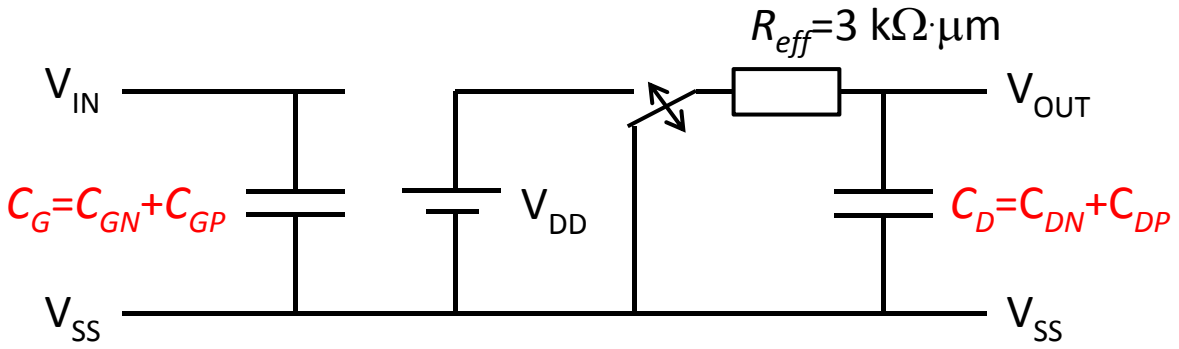

Inverter input capacitance: $C_G=C_{GN}+C_{GP}$; MOSFET gate capacitances add!
Inverter parasitic output capacitance: $C_D=C_{DN}+C_{DP}$. Drain caps also add!

# The inverter and its electrical model

To cumbersome to have different rise and fall delays!
Replace effective resistances with one average effective resistance!




$R_{N,eff}$=2 kΩ·µm $R_{P,eff}$=4 kΩ·µm

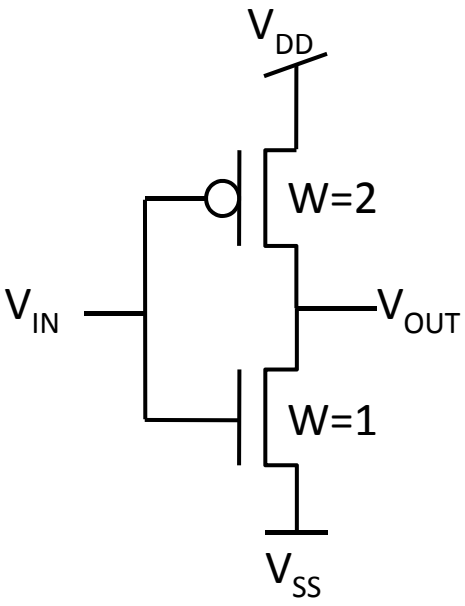


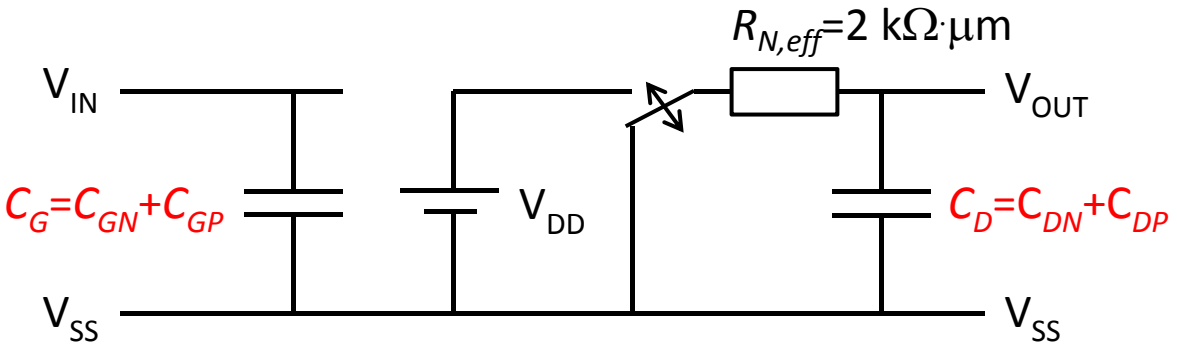

Inverter input capacitance: $C_G=C_{GN}+C_{GP}$; MOSFET gate capacitances add!
Inverter parasitic output capacitance: $C_D=C_{DN}+C_{DP}$. Drain caps also add!

# The inverter and its electrical model

To cumbersome to have different rise and fall delays!
Replace effective resistances with one average effective resistance!

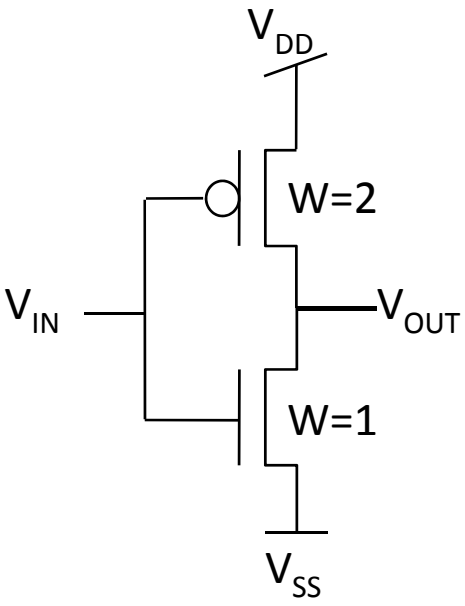
Or even better!
Design the inverter for equal effective resistances, $R_{N,eff}=R_{P,eff}$, by making p-channel MOSFET twice as wide as the n-channel MOSFET to compensate for the lower hole mobility



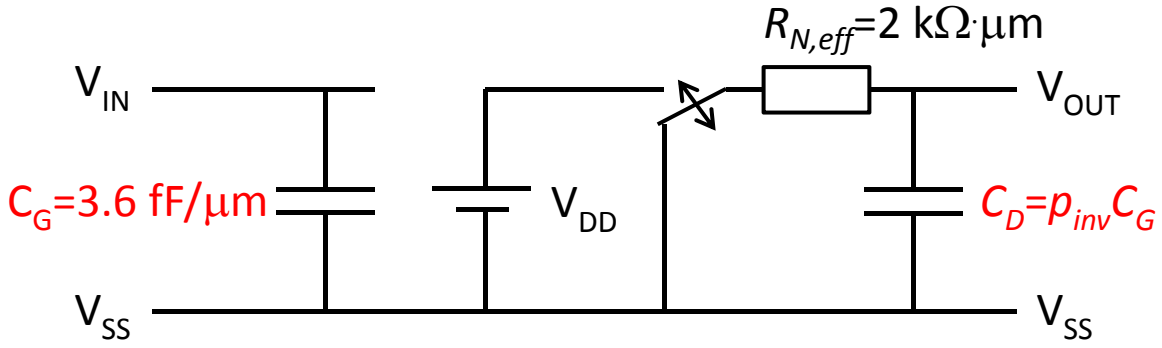




Inverter input capacitance: $C_G=C_{GN}+C_{GP}$; MOSFET gate capacitances add!
Inverter parasitic output capacitance: $C_D=C_{DN}+C_{DP}$. Drain caps also add!

# Inverter capacitances



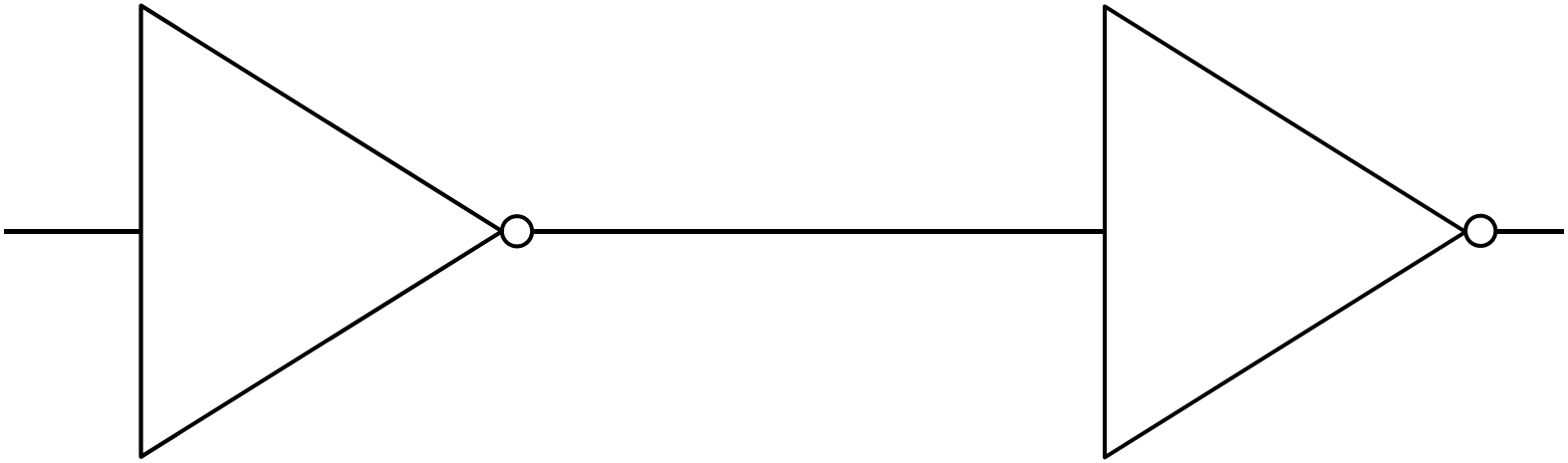

Task: Calculate $C_G$ and $C_D$!




Answer: Assuming L=60 nm and $C_{ox}$=20 fF/µm² we obtain $C_{GN}$=1.2 fF/µm and $C_{GP}$=2.4 fF/µm. Hence $C_G$=3.6 fF/µm.
Concerning $C_D$ we assume $C_D=p_{inv}C_G$=3.6 fF/µm with $p_{inv}$=1.

# Inverter pair delay

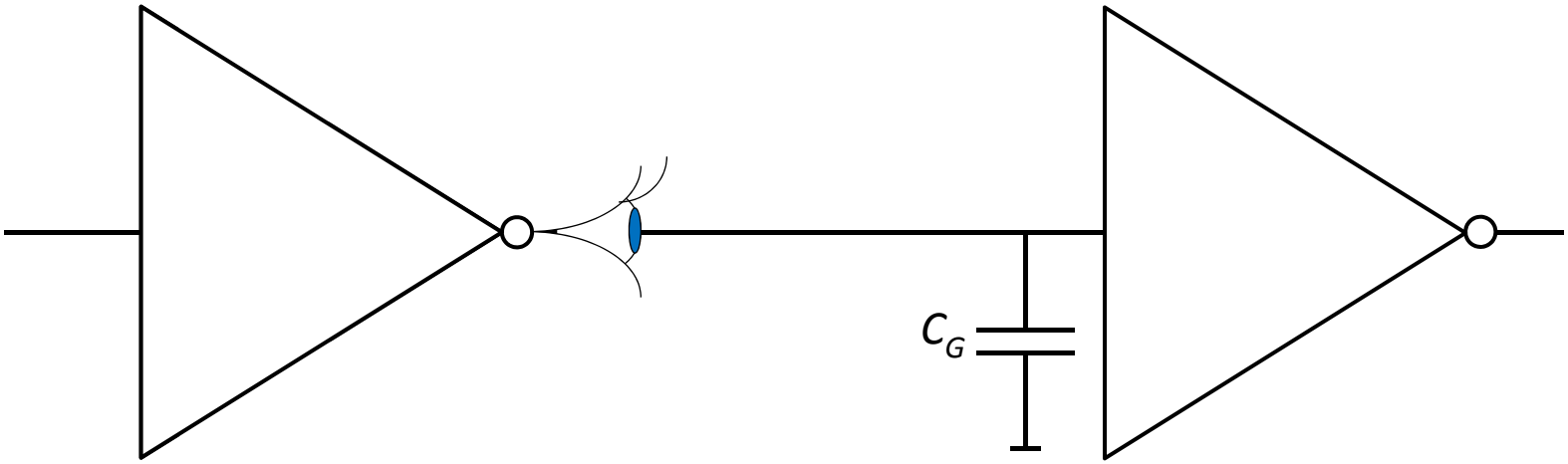
Task: Calculate the inverter pair delay!



# Inverter pair delay

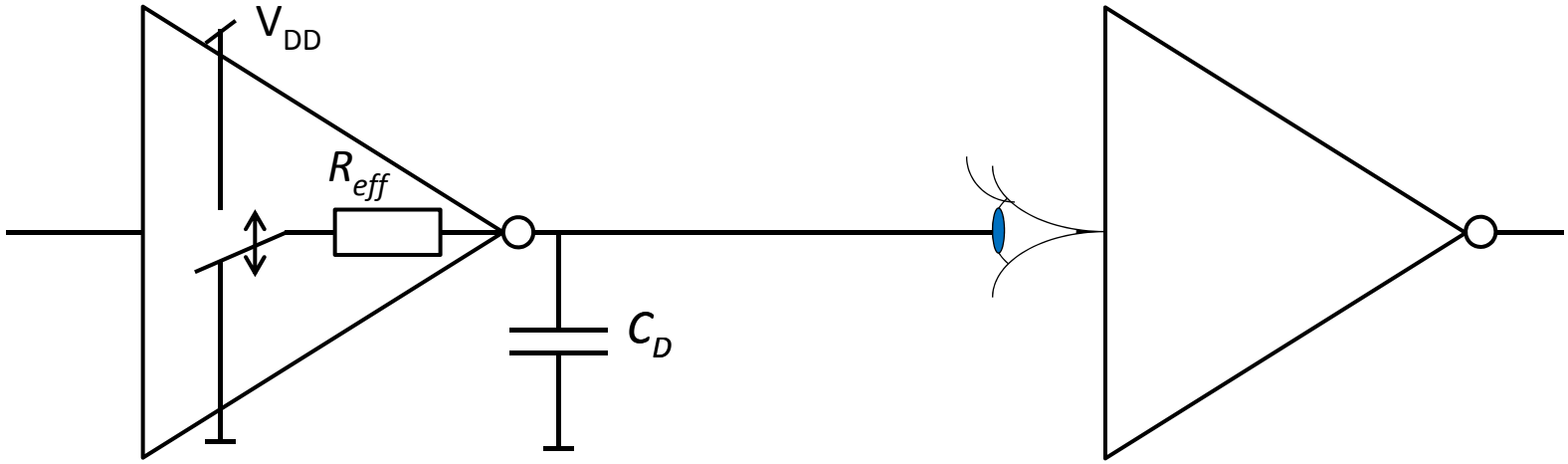
Put on your “two-port glasses” and look towards the loading inverter!

*You will only see the input capacitance of the loading inverter*



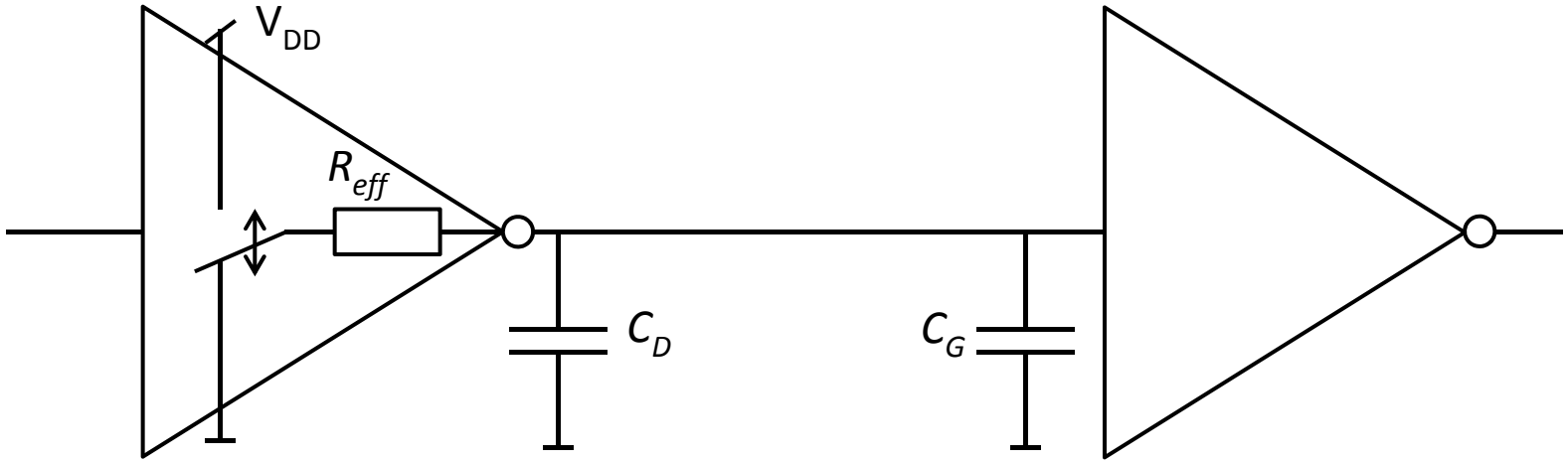
# Inverter pair delay

Have your “two-port glasses” on and look towards the driving inverter!
*You will see a voltage source with a certain source resistance, and you will see the parasitic capacitance of the loading inverter*



# Inverter pair delay

In an ideal inverter the time constant tau is really what the name says, a constant, and that is independent of inverter size (as long as $W_P/W_N=2$).

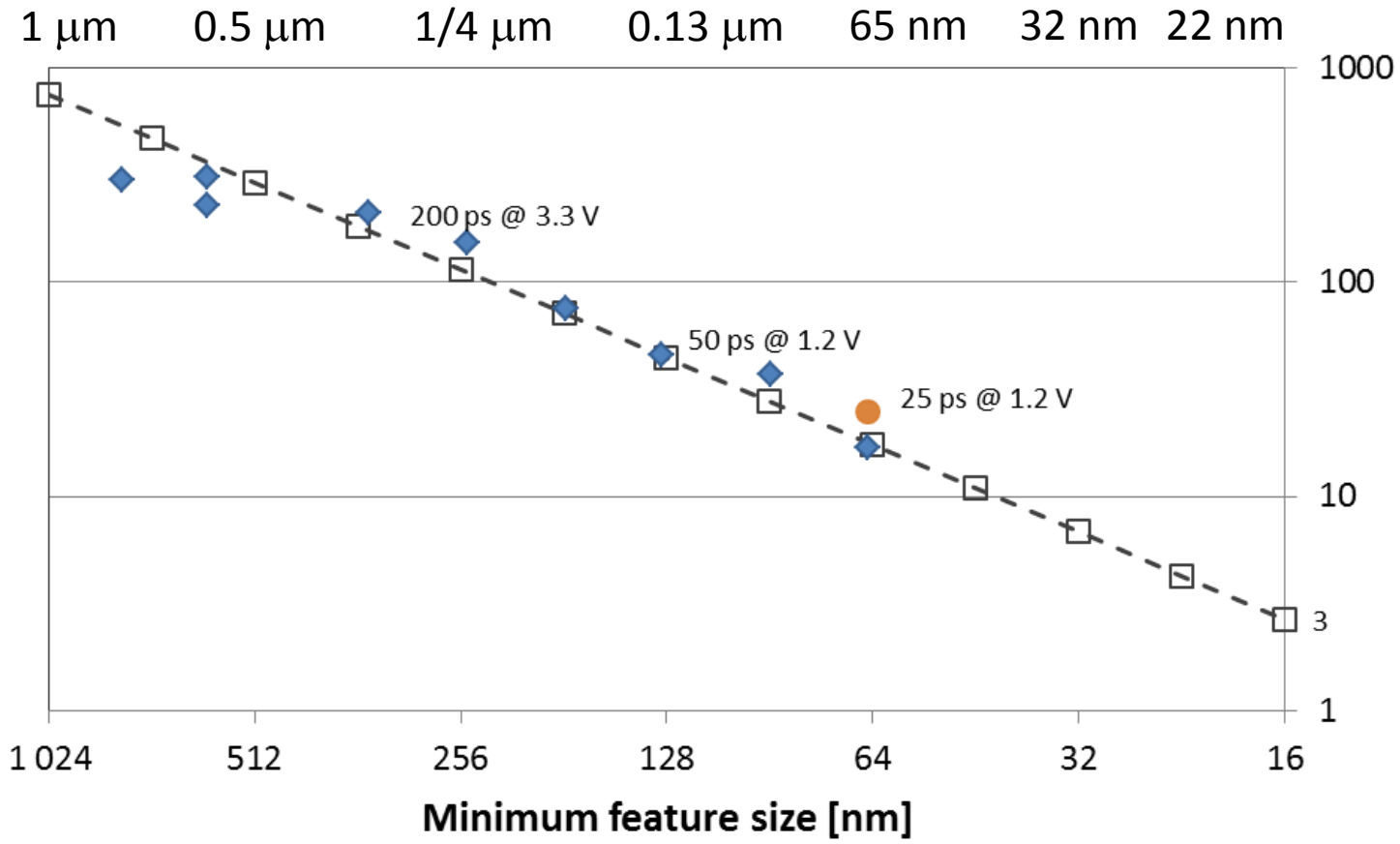



The propagation delay becomes $t_{pd} = 0.7R_{eff}\left(C_D + C_G\right) = 0.7R_{eff}C_G\left(p_{inv}+1\right) = 5\text{ ps}\times 2 = 10\text{ ps}$

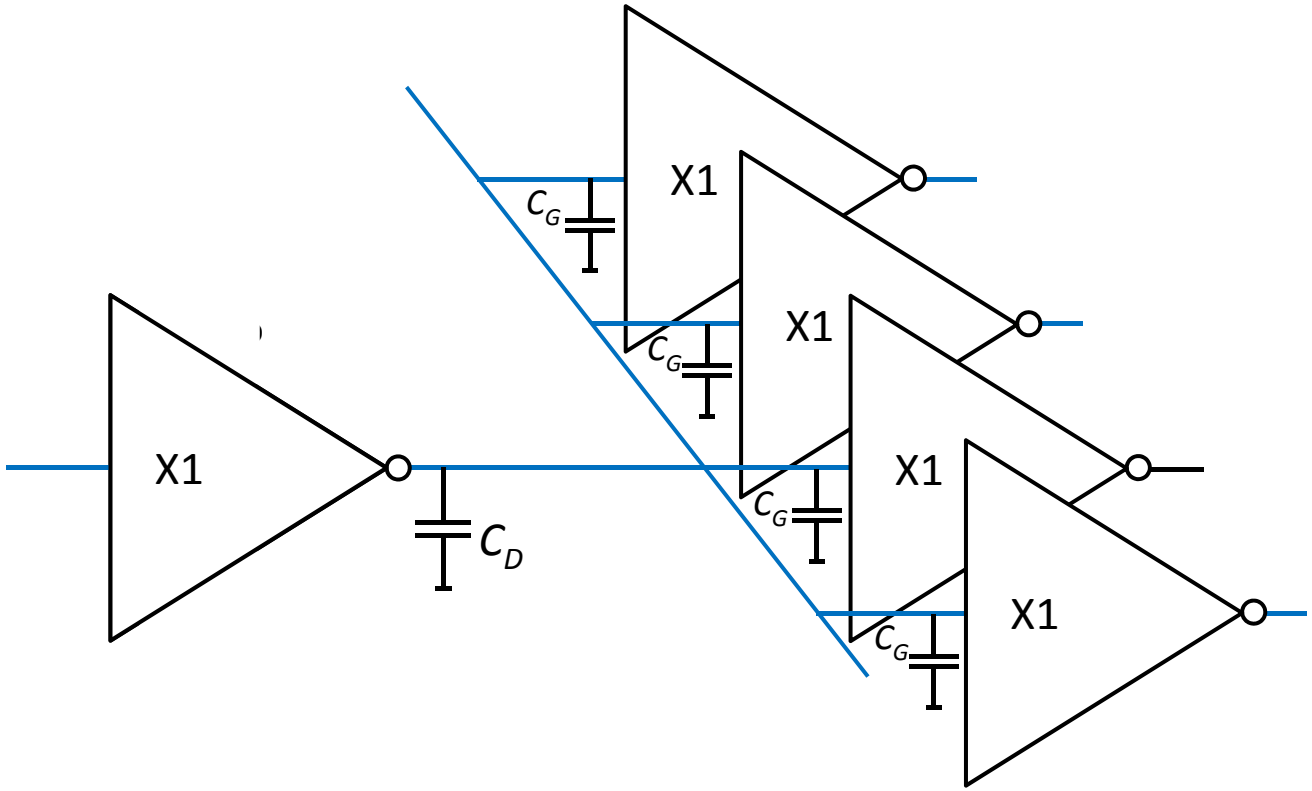
All delay calculations are made wrt to this technology time constant tau

$$\tau = 0.7R_{eff}C_G = 0.7\times\left(2\text{ k}\Omega\times\mu\text{m}\right)\times\left(3.6fF/\mu\text{m}\right) = 5\text{ ps}$$

# FO4 delay vs. feature size



# Inverter FO4 delay



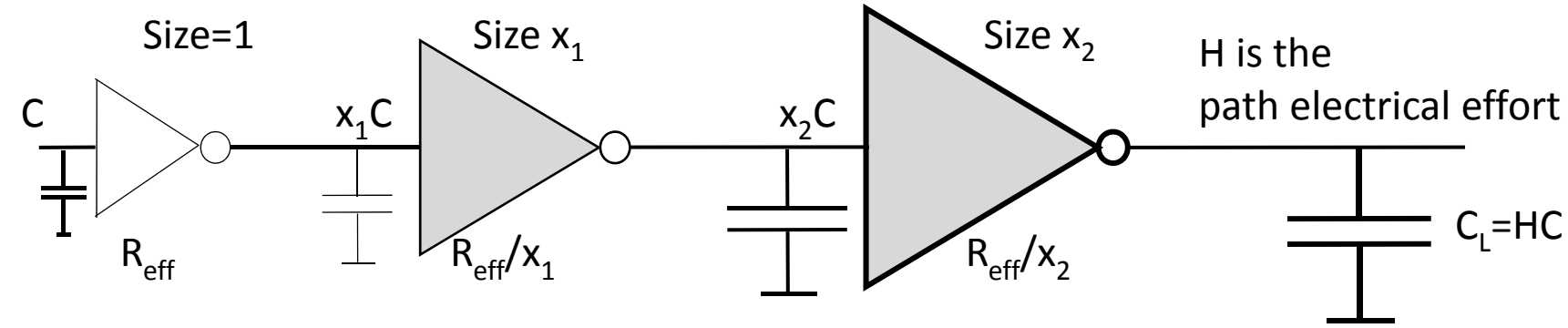

The FO4 propagation delay becomes $t_{pd} = 0.7R_{eff}\left(C_D + 4C_G\right) = \underbrace{0.7R_{eff}C_G}_{\tau au}\left(p+4\right) = 5\text{ ps} \times 5 = 25\text{ ps}$

# Inverter Size

- In most vendor cell libraries, inverters and other logic gates comes in a number of different varieties concerning their driving capability ($R_{eff}$) and input capacitance ($C_G$).
- In the following all inverters and logic gates of a certain size, e.g. size X=8, will have the same input capacitance, and, as an example, this input capacitance will be only half the input capacitance of a gate of size X=16.

# The tapered buffer

Reference inverter . . . and two inserted buffer inverters




With two intermediate buffer inverters we obtain a normalized delay relative to tao:
$d=(p_{inv}+h_1)+(p_{inv}+h_2)+(p_{inv}+H/h_1h_2)$

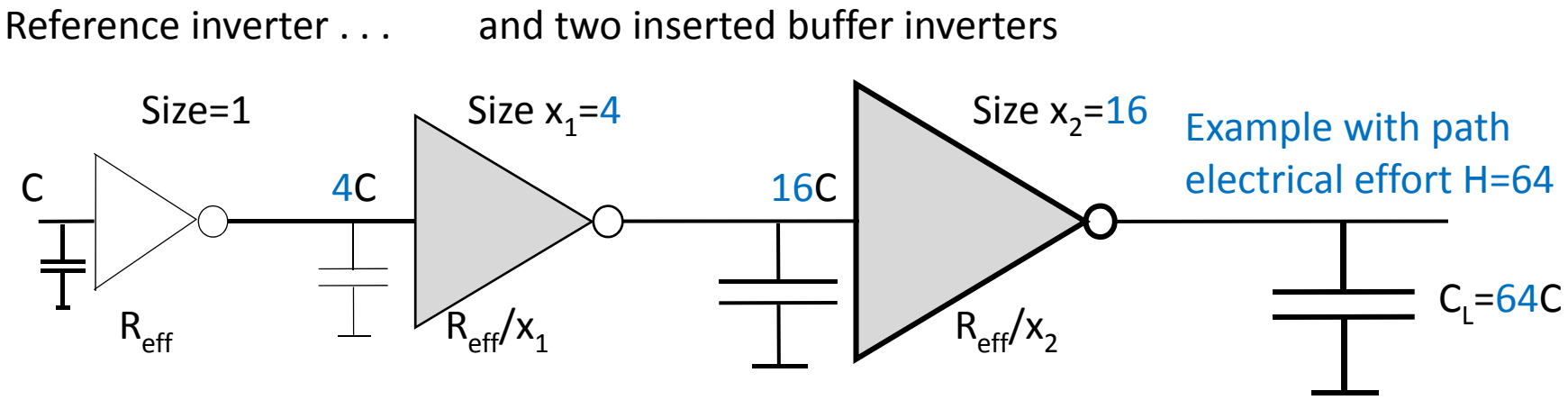
where we have defined the electrical efforts, or fanouts, $h$, where $h_1=x_1$, $h_2=x_2/x_1$ (and $h_3=H/h_1h_2$)

Show that minimum delay is obtained for $h_1=h_2=\sqrt[3]{H}$ >>> $d=3(p_{inv}+\sqrt[3]{H})$

Hint: $\frac{d}{dh_1}d(h_1,h_2)=0$, and $\frac{d}{dh_2}d(h_1,h_2)=0$

yields $h_1=h_2$ and $h_3=H/h_1h_2 \rightarrow h=h_1=h_2=h_3=\sqrt[3]{H}$

# The tapered buffer




With two intermediate buffer inverters we obtain a normalized delay relative to tao:
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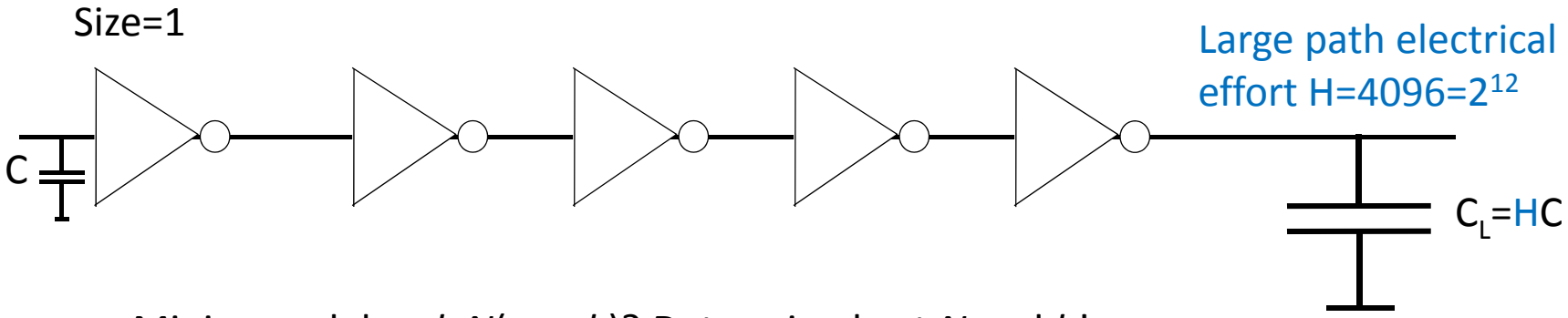
where we have defined the electrical efforts, or fanouts, $h$, where $h_1=x_1$, $h_2=x_2/x_1$ (and $h_3=H/h_1h_2$)

Minimum delay is obtained for $h_1=h_2=\sqrt[3]{64}=4$ >>> $d=3(p_{inv}+4)=15$ for $p_{inv}=1$

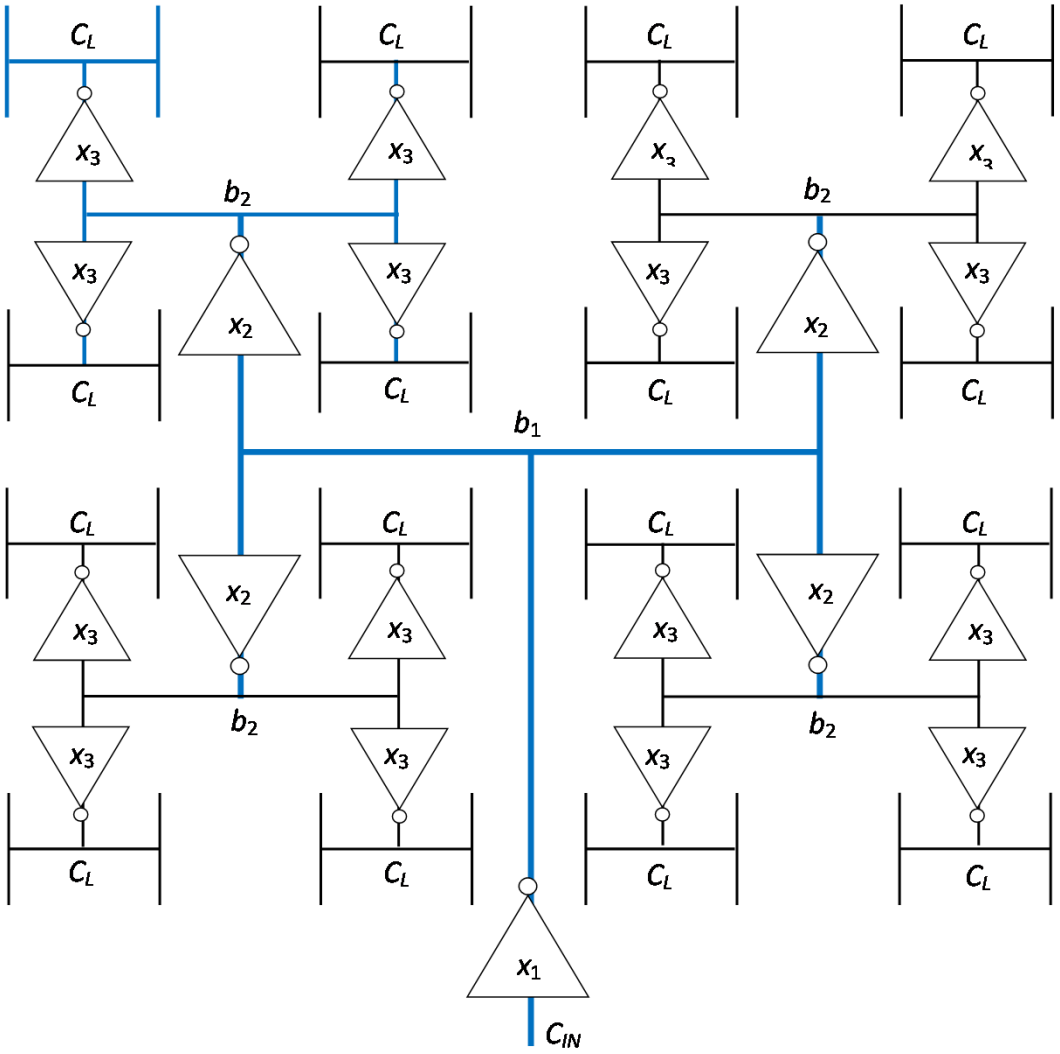
# The Tapered Buffer

- What if the path electrical effort, for some reason, is very large, e.g. H=4096.
- How many inverters, *N*, are needed to minimize the delay?



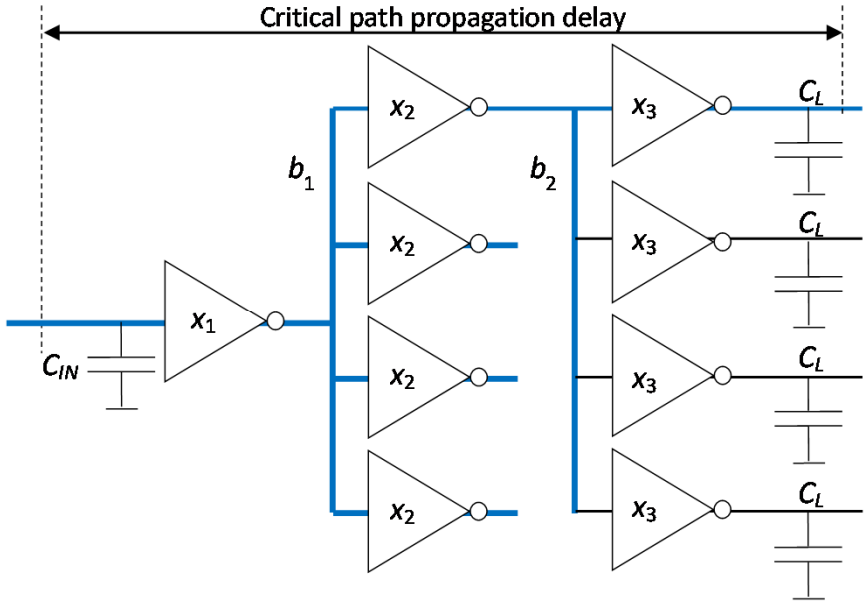

Minimum delay $d=N(p_{inv}+h)$? Determine best *N* and *h*!

# H-tree clock distribution



# H-tree clock distribution

- What is the timing path electrical effort?
- What sizes to choose for inverters in the H-tree?



# Summary

- We defined rise and fall delays at the 50% level ($V_{DD}/2$)
- We defined rise and fall times between 20% and 80% levels
- We calculated propagation delay in response to a square-wave input signal assuming MOSFETs being saturated during delay
- We improved the delay model by adding 40%
  - assuming a ramp input signal and
  - assuming equal input and output edge rates
- We "*heard a bell ring*" and replaced saturation current sources by effective resistances
- We made the p-channel MOSFET twice as wide to compensate for lower hole mobility
  - Both MOSFETs now have the same effective resistance of 2 $k\Omega{\cdot}\mu m$
  - However, p-channel device now has twice the input capacitance of the n-channel MOSFET
- We have obtained an electrical two-port model of the inverter for delay calculations
  - we know what this model looks like seen from the input port, and seen from the output port
- Finally, we calculated the FO4 delay, and we found the $R_{eff}C_G$ product being independent of the inverter size (as long as we keep same ratio between $W_P$ and $W_N$)