The CMOS Inverter

Lecture 3

Static properties

(VTC and noise margins)

Where are we?

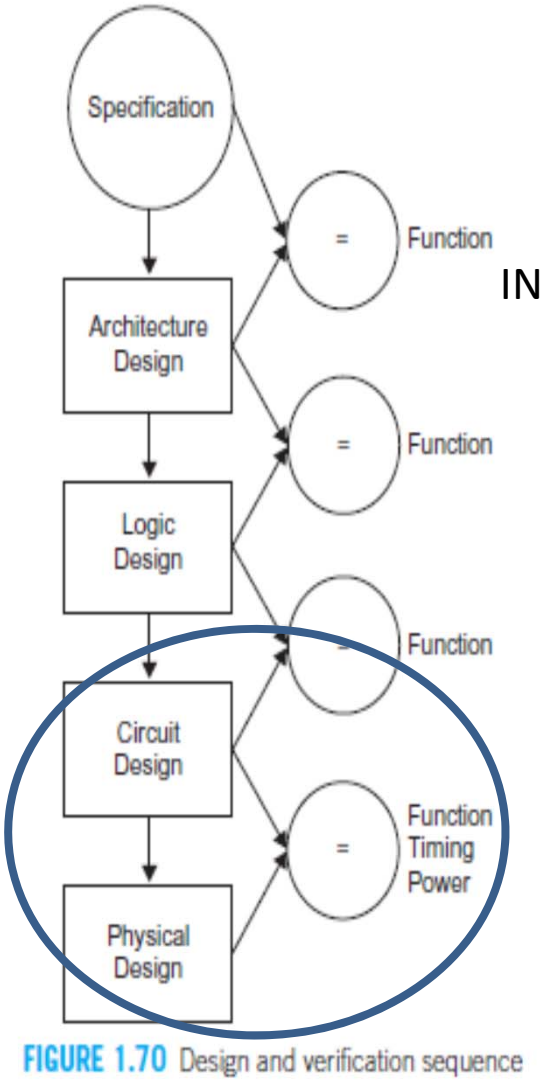
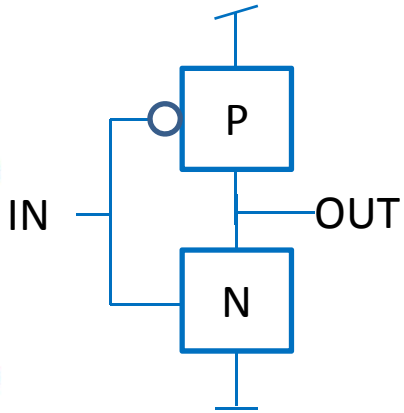
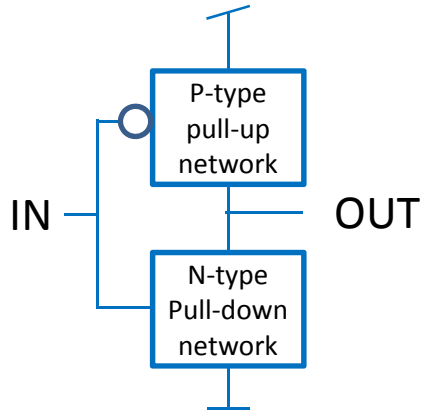


FIGURE 1.70 Design and verification sequence

Inverter

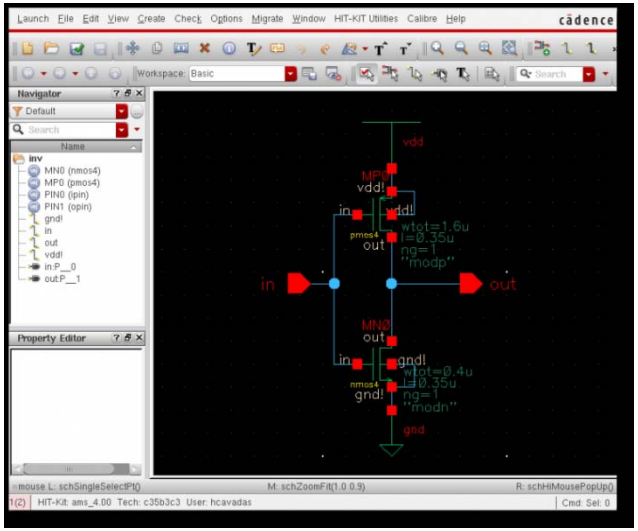


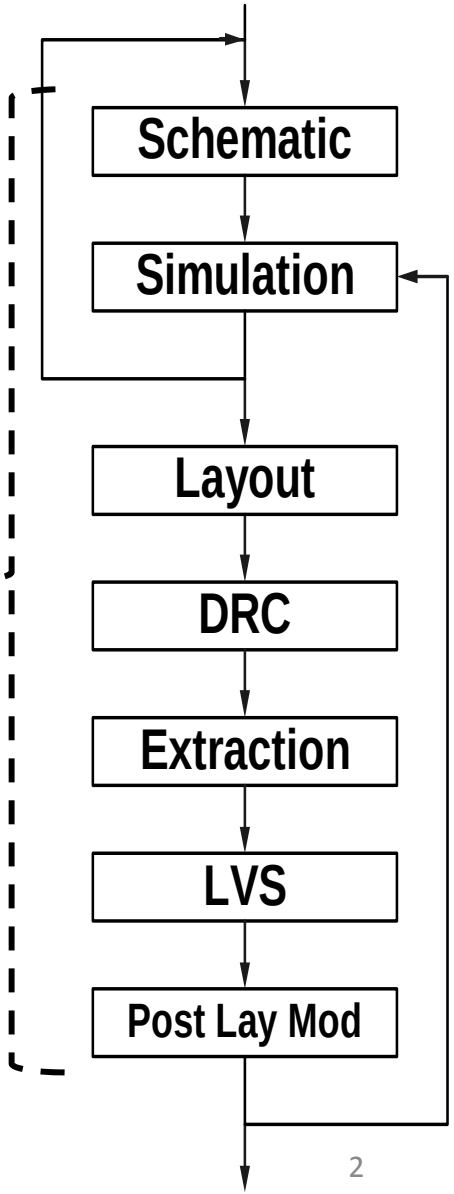
Logic gates



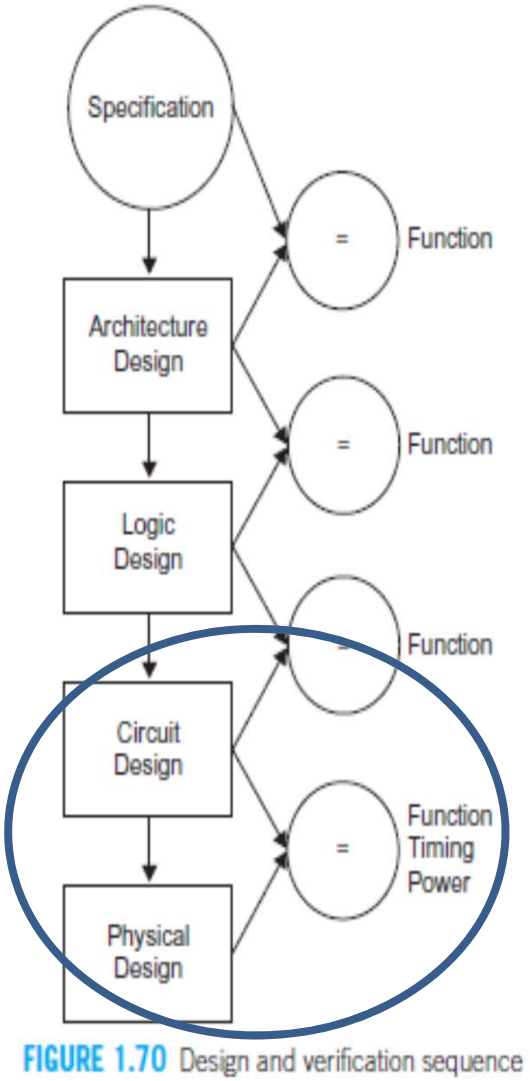
Designing w switches

Hands-on lab session





Where are we?



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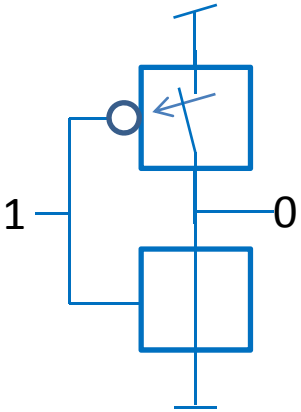
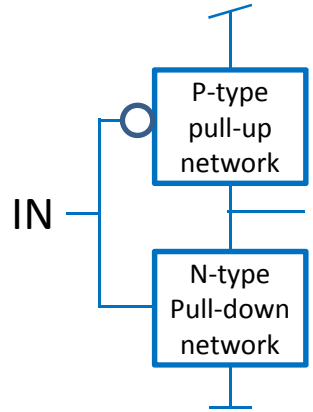
Inverter

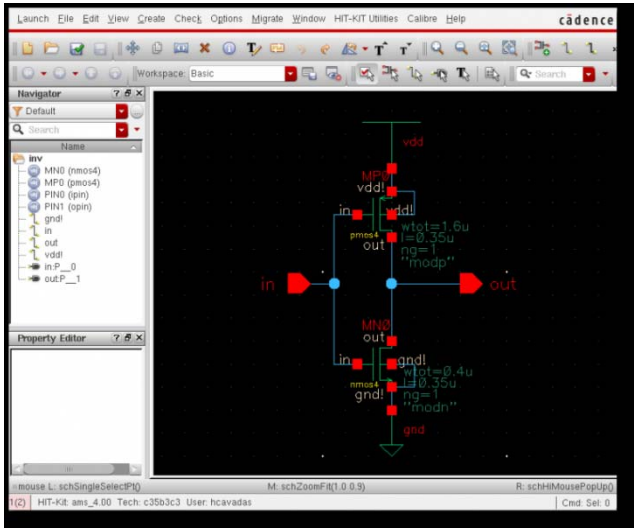


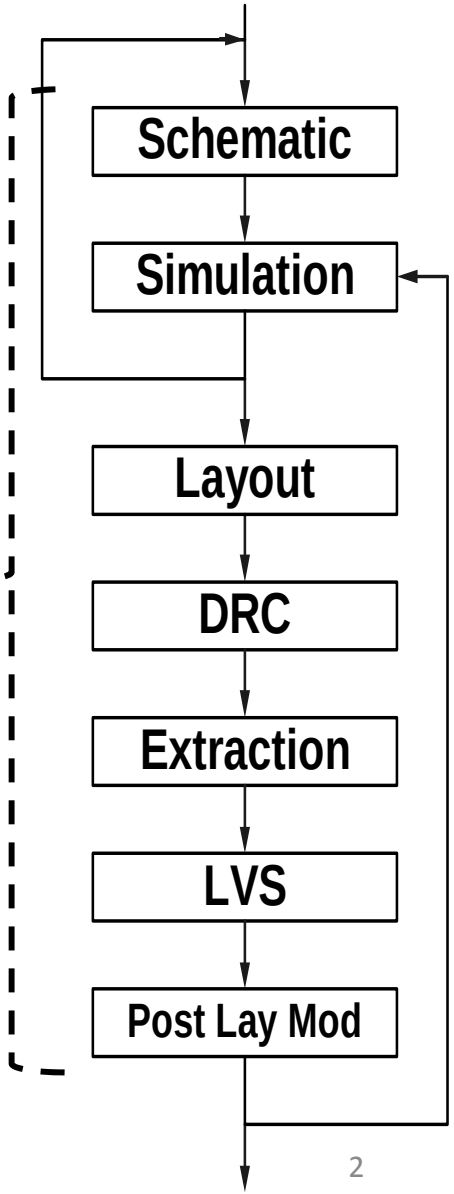
Designing w switches

Logic gates



Hands-on lab session





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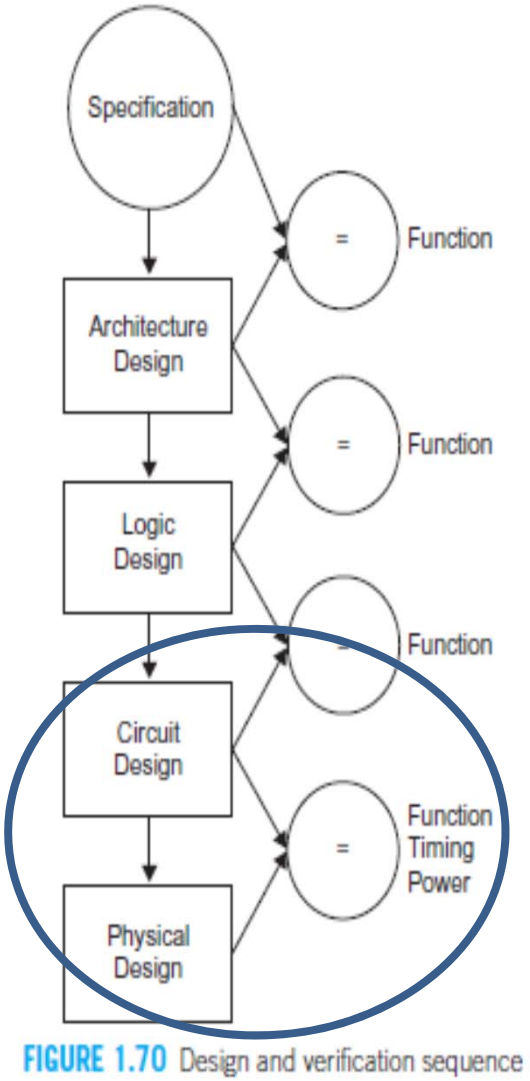

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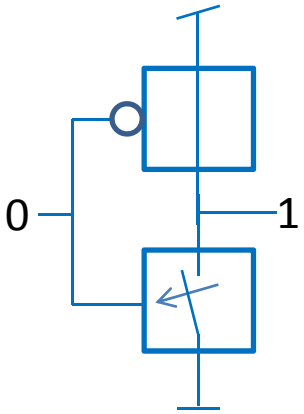
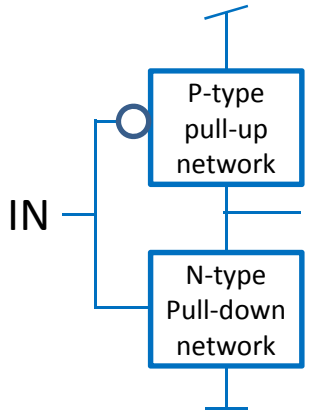
Inverter

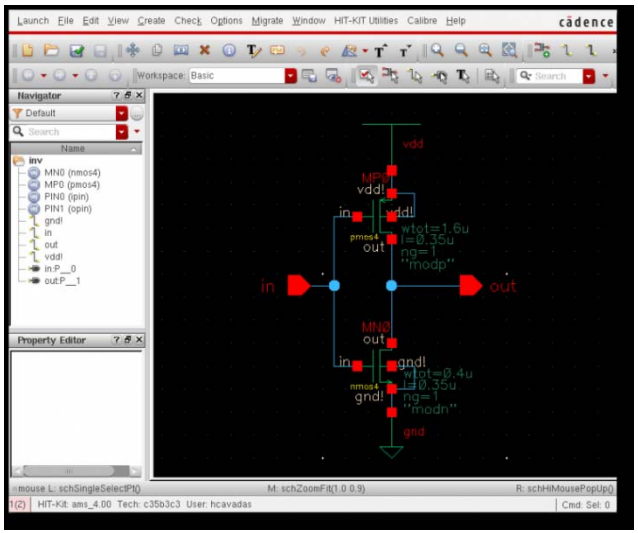


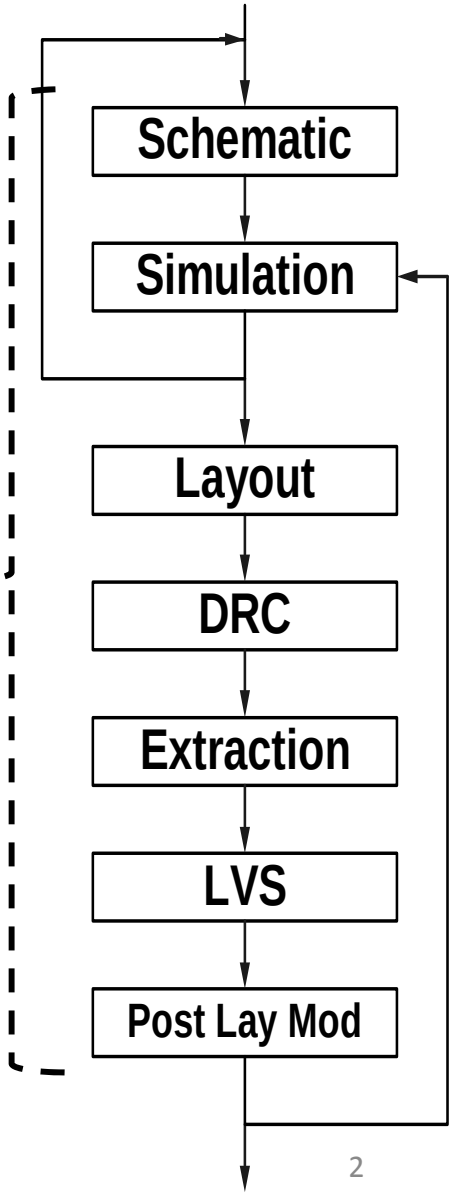
Designing w switches

Logic gates



Hands-on lab session





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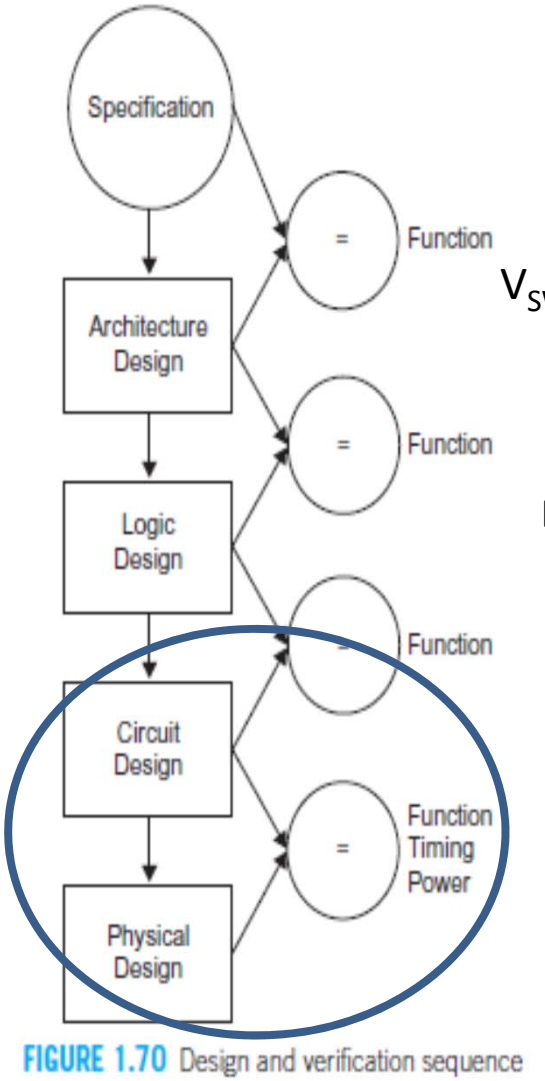

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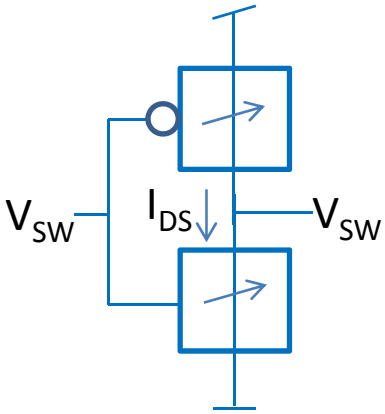
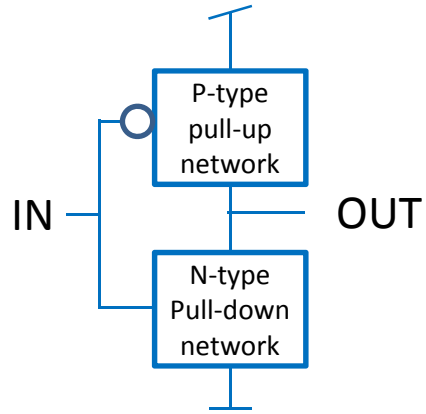
Inverter

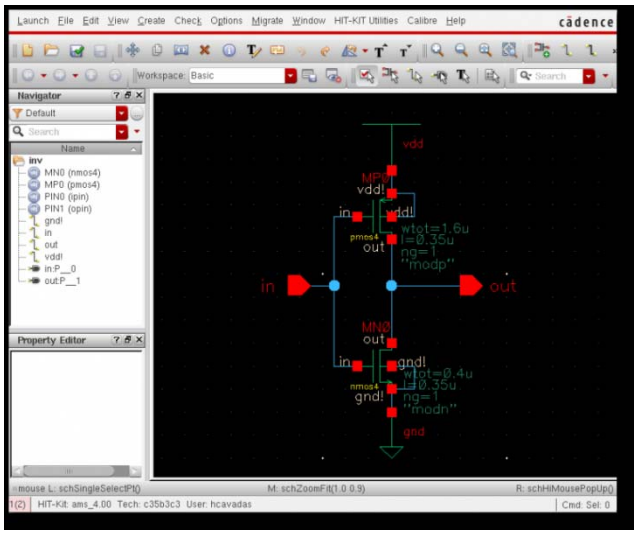


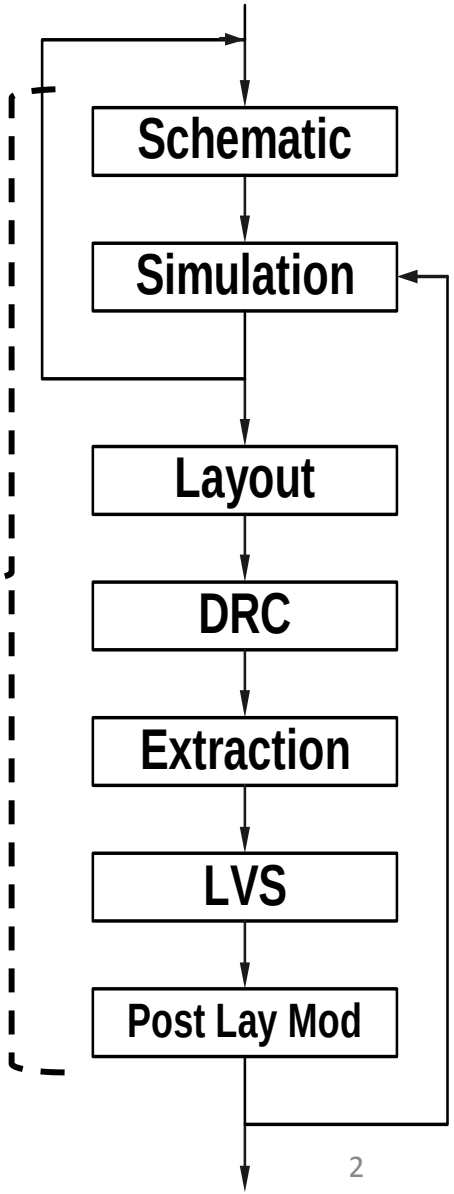
Designing w switches

Logic gates

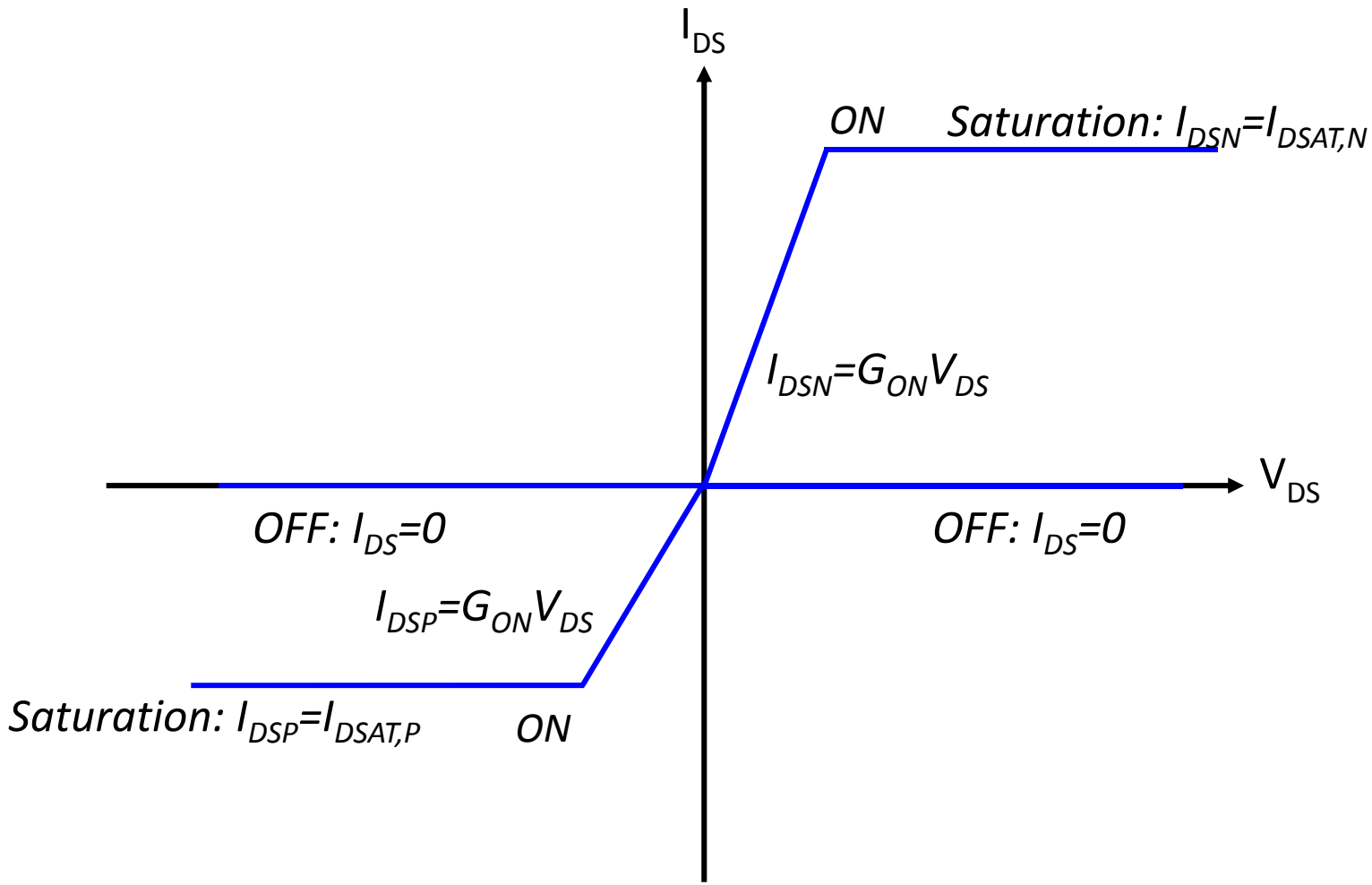


Hands-on lab session

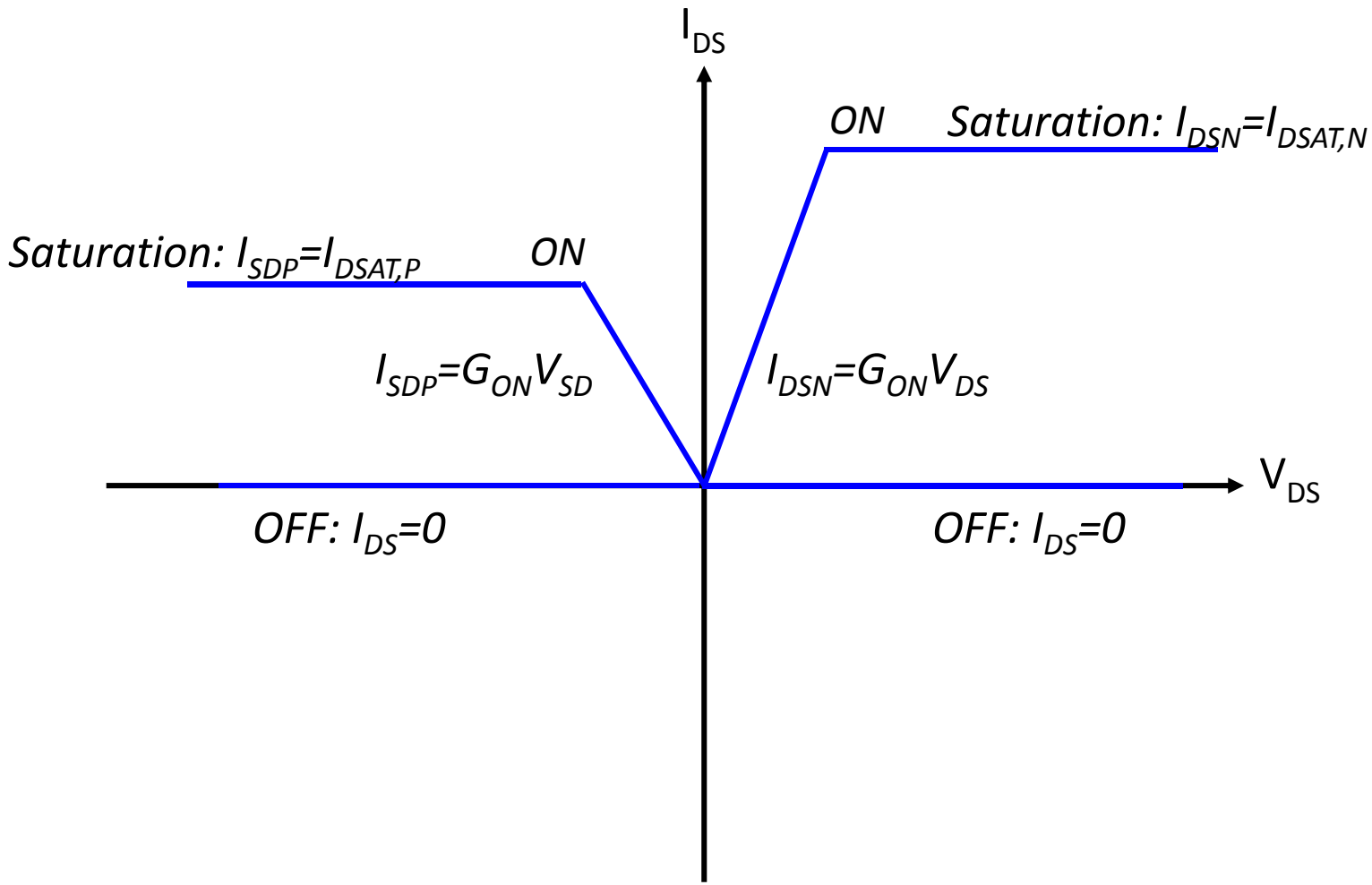




MOSFET I/V Characteristics



MOSFET I/V Characteristics



MOSFET I/V Characteristics

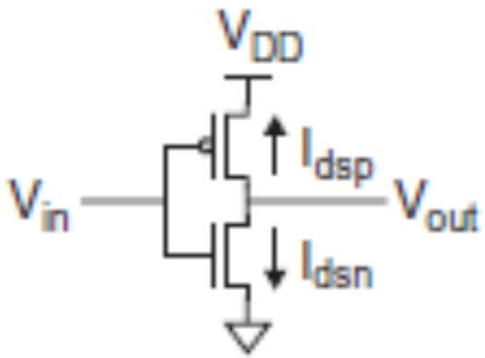
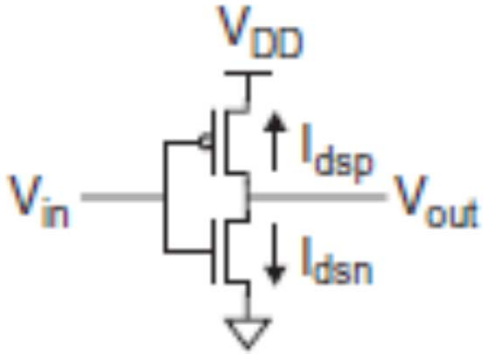


FIGURE 2.25
A CMOS inverter

V_{IN}/V_{OUT} voltage plane



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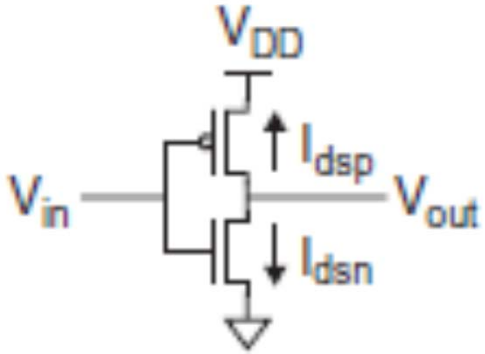
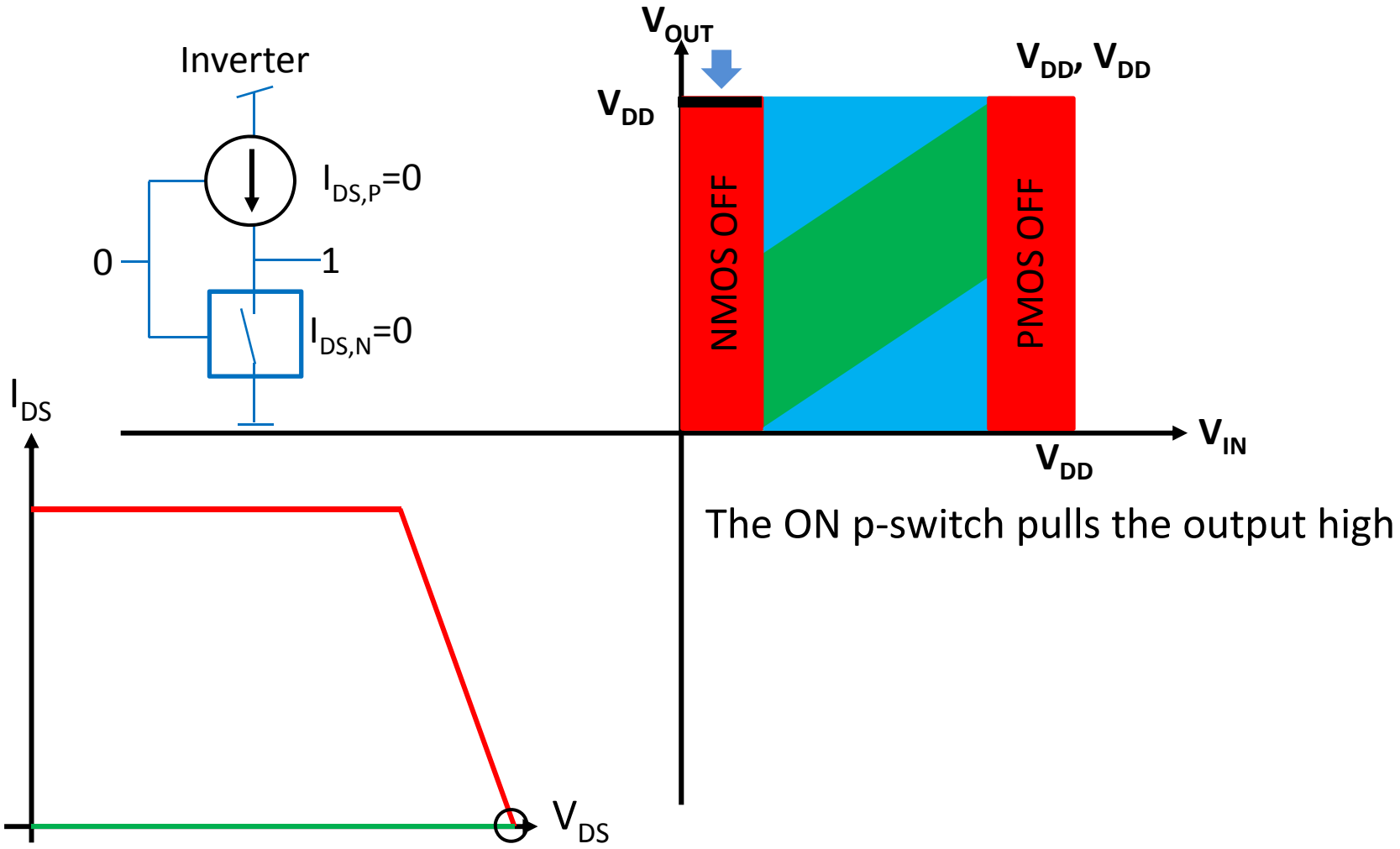


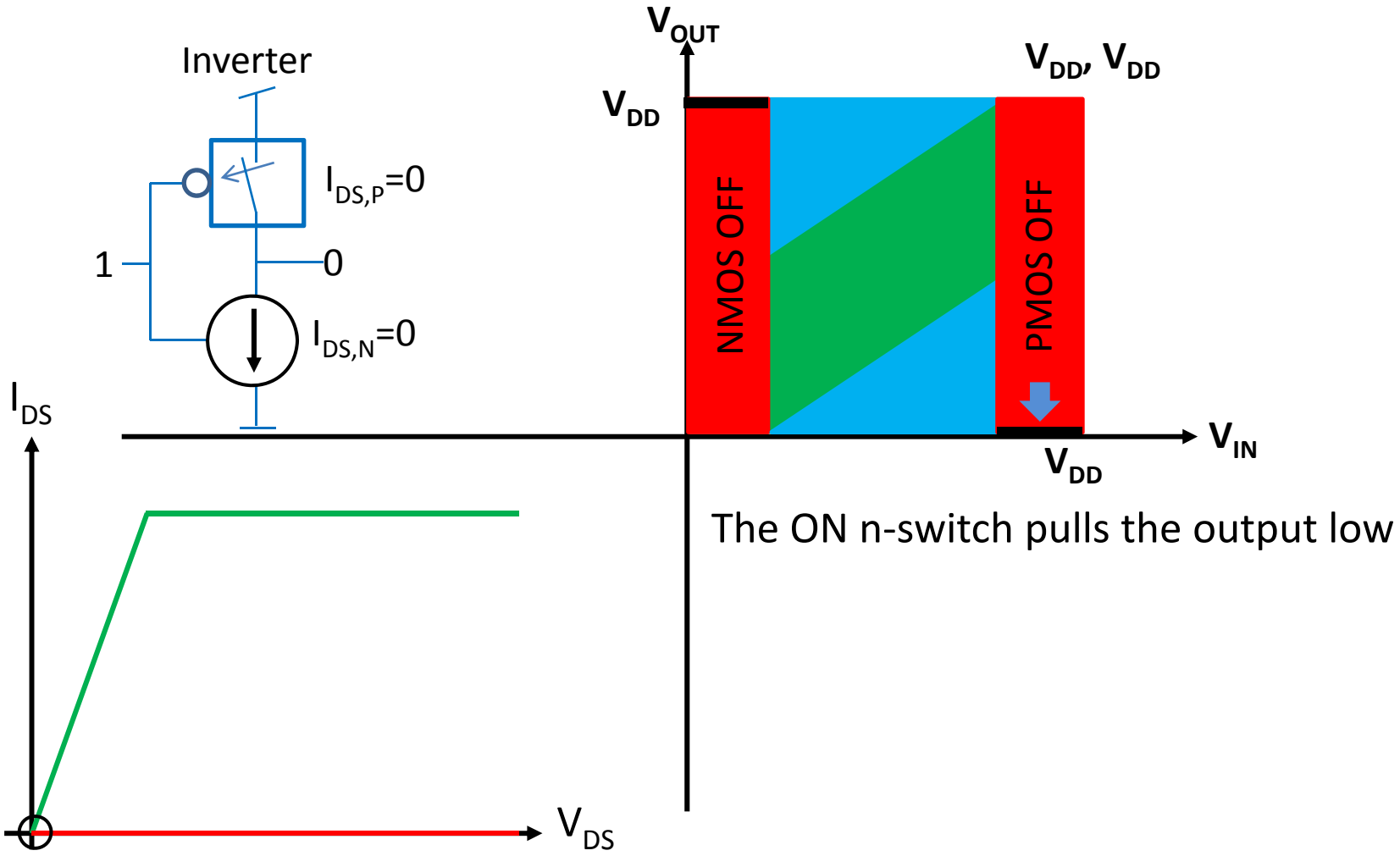
FIGURE 2.25
A CMOS inverter

Voltage Transfer Characteristic - VTC



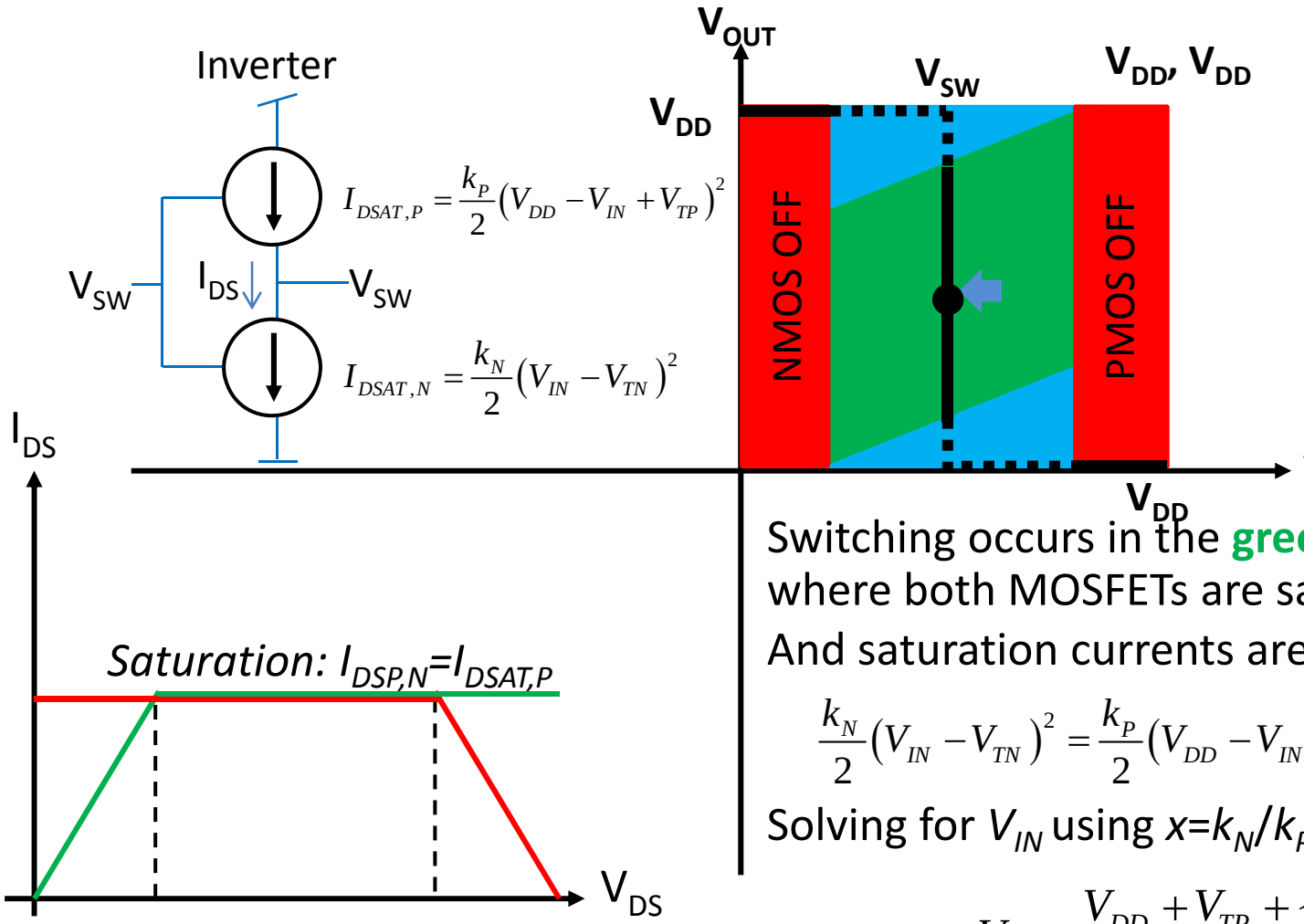
The ON p-switch pulls the output high

Voltage Transfer Characteristic - VTC



The ON n-switch pulls the output low

Voltage Transfer Characteristic - VTC



Switching occurs in the **green region** where both MOSFETs are saturated!

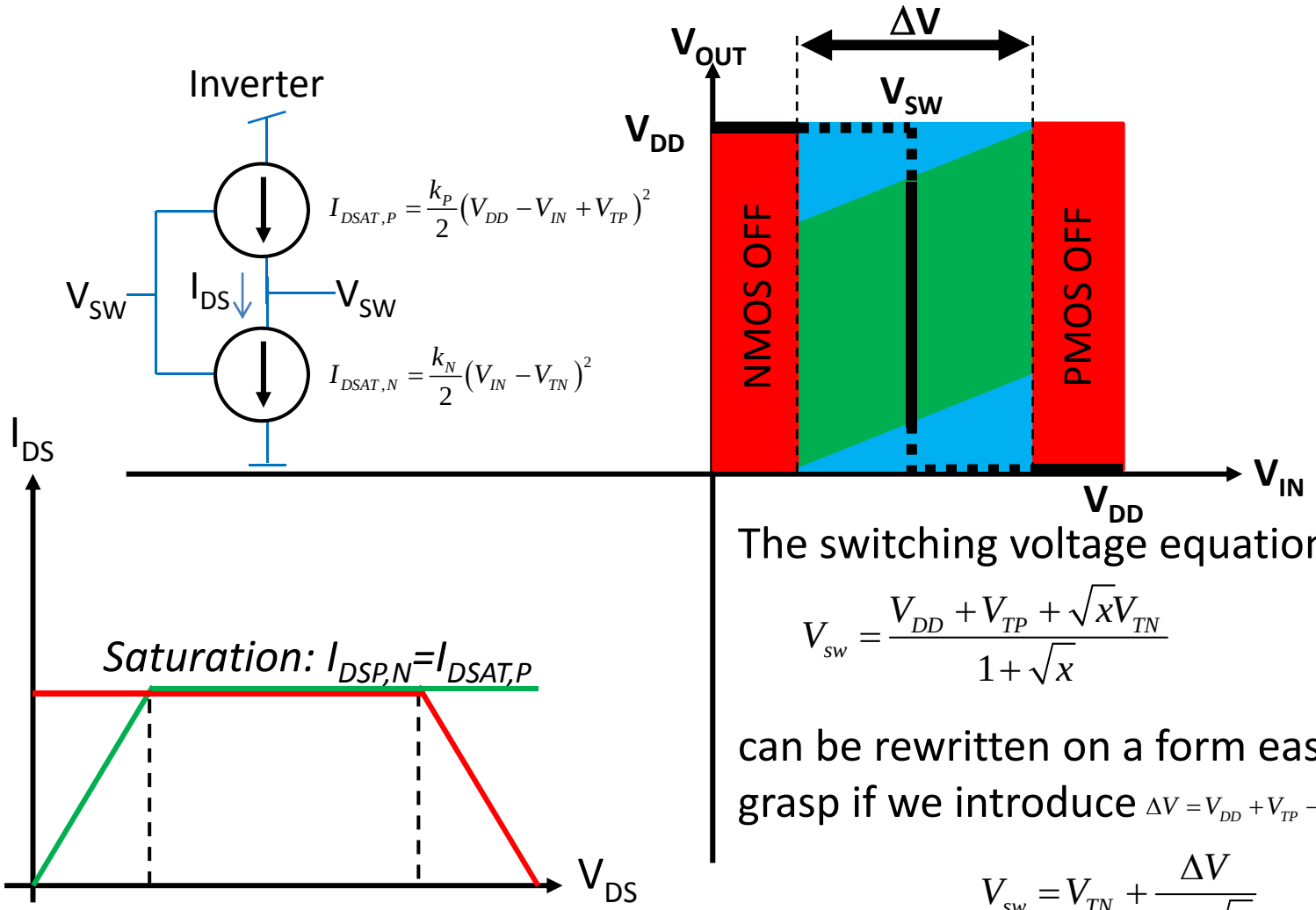
And saturation currents are equal:

$$\frac{k_N}{2}(V_{IN} - V_{TN})^2 = \frac{k_P}{2}(V_{DD} - V_{IN} + V_{TP})^2$$

Solving for V_{IN} using $x=k_N/k_P$ yields

$$V_{sw} = \frac{V_{DD} + V_{TP} + \sqrt{x}V_{TN}}{1+\sqrt{x}}$$

Voltage Transfer Characteristic - VTC



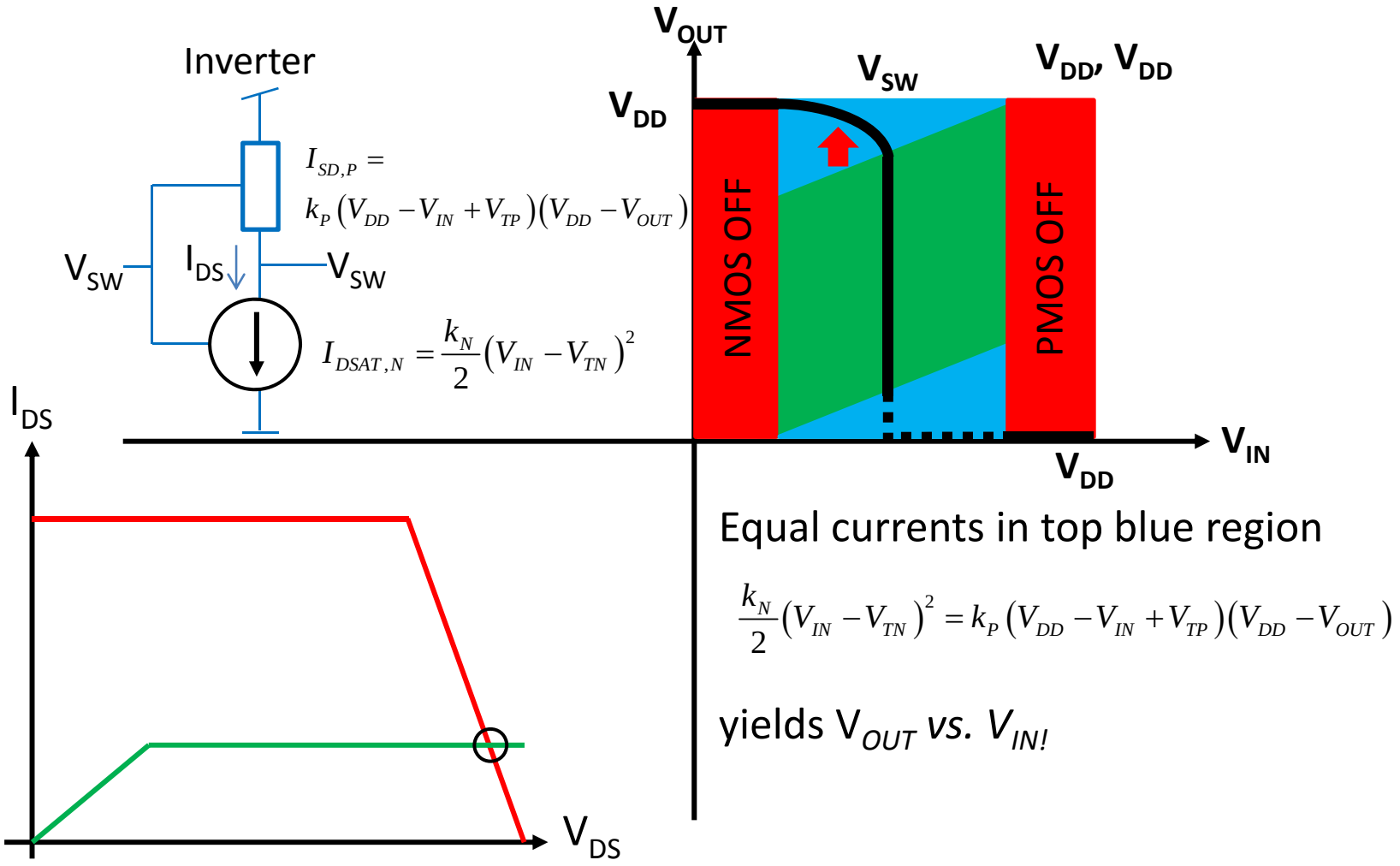
The switching voltage equation

$$V_{sw} = \frac{V_{DD} + V_{TP} + \sqrt{x}V_{TN}}{1+\sqrt{x}}$$

can be rewritten on a form easier to grasp if we introduce $\Delta V = V_{DD} + V_{TP} - V_{TN}$

$$V_{sw} = V_{TN} + \frac{\Delta V}{1+\sqrt{x}}$$

Voltage Transfer Characteristic - VTC

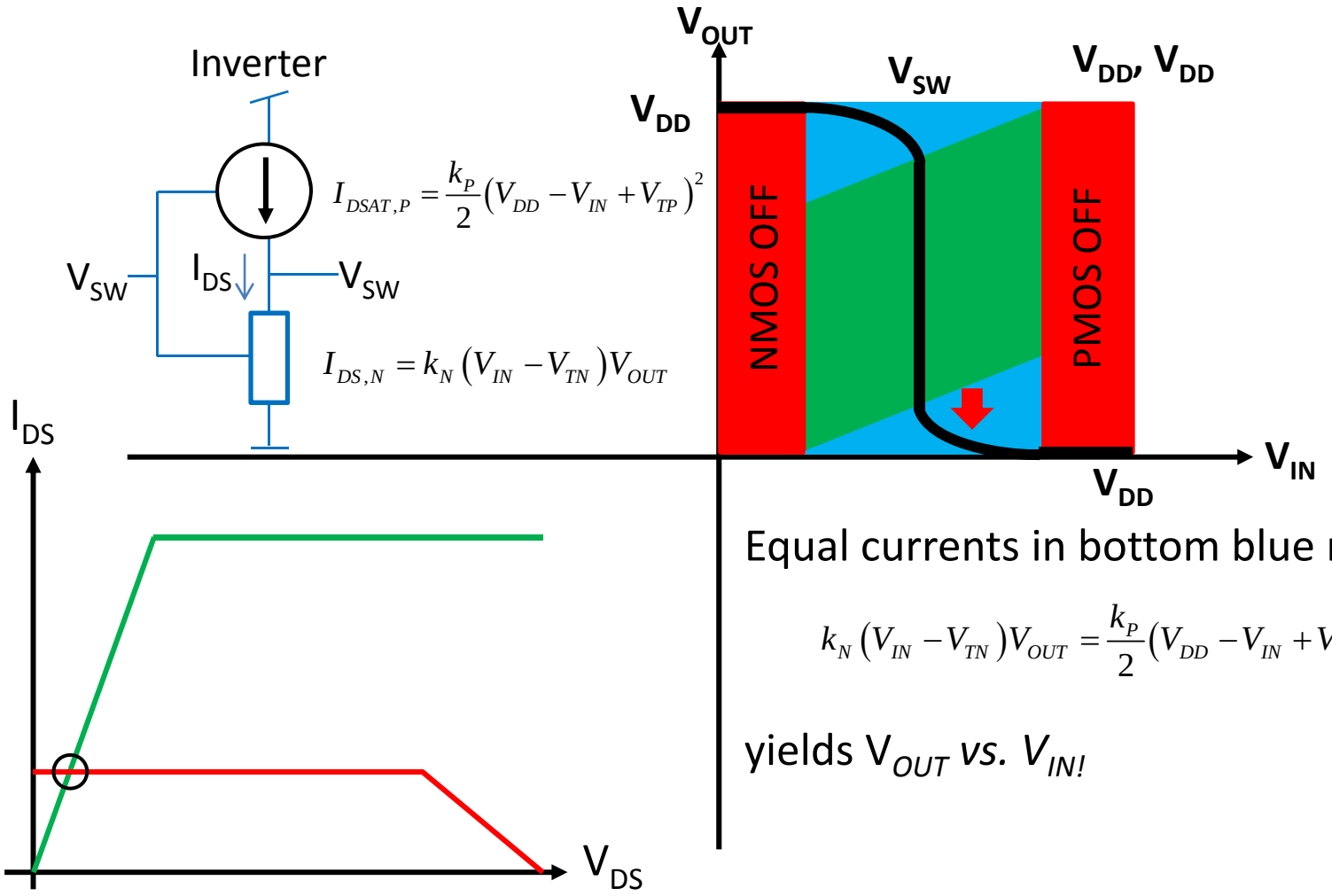


Equal currents in top blue region

$$\frac{k_N}{2}(V_{IN} - V_{TN})^2 = k_P (V_{DD} - V_{IN} + V_{TP})(V_{DD} - V_{OUT})$$

yields V_{OUT} *vs.* V_{IN}*!*

Voltage Transfer Characteristic - VTC



Equal currents in bottom blue region

$$k_N (V_{IN} - V_{TN}) V_{OUT} = \frac{k_P}{2}(V_{DD} - V_{IN} + V_{TP})^2$$

yields V_{OUT} *vs.* V_{IN}*!*

The voltage characteristic (VTC)

For $x=k_N/k_P=1$ we have

$$V_{sw} = V_{TN} + \frac{\Delta V}{1+\sqrt{x}} = V_{TN} + \frac{\Delta V}{2}$$

What if we make n-channel MOSFET wider, i.e. for $x>1$?

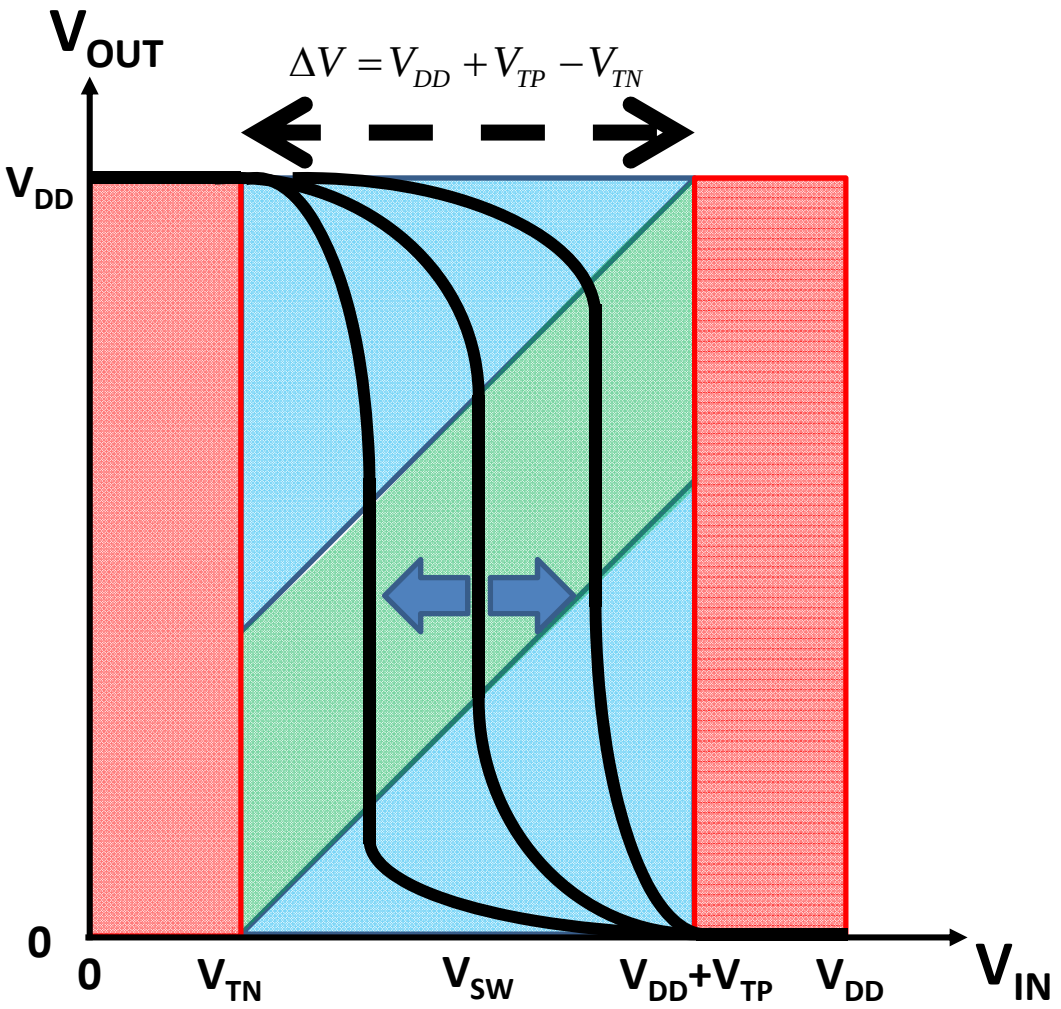
What happens to VTC?
Will switching voltage V_{SW} increase or decrease?

Assume $x=4$ and we have

$$V_{sw} = V_{TN} + \frac{1}{3}\Delta V < V_{TN} + \frac{\Delta V}{2}$$

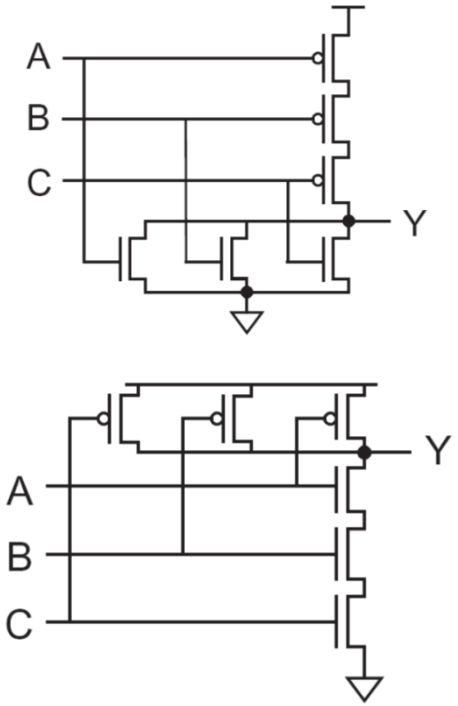
Assume $x=1/4$ and we have

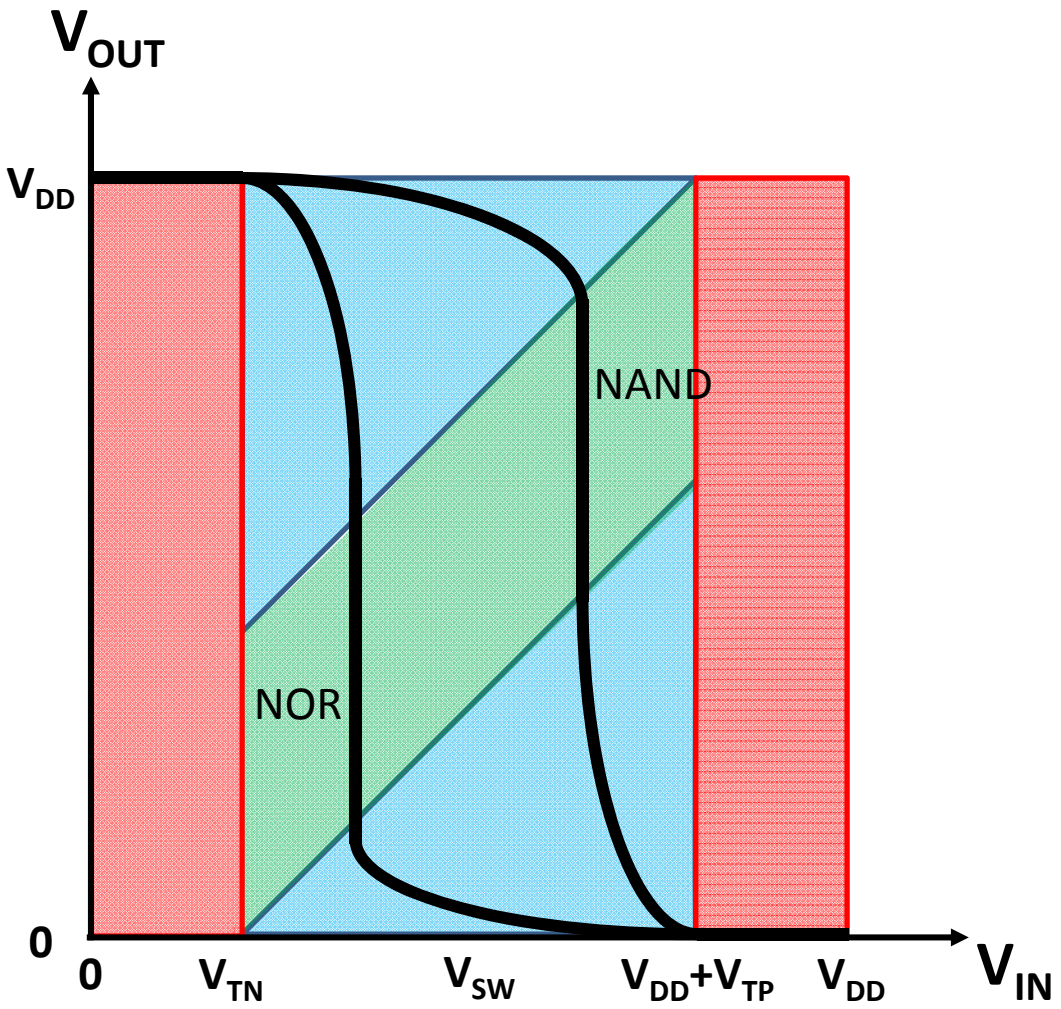
$$V_{sw} = V_{TN} + \frac{2}{3}\Delta V > V_{TN} + \frac{\Delta V}{2}$$



The voltage characteristic (VTC)

Which VTC is NAND and which VTC is NOR?





The voltage characteristic (VTC)

How about current flow?

No current flow in red regions!

”short-circuit” current I_{SC} flows in blue/green regions

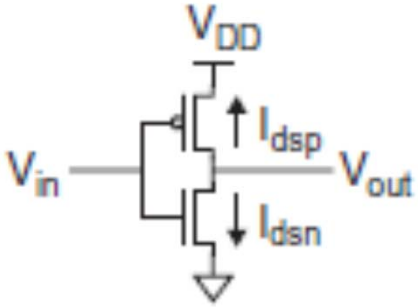
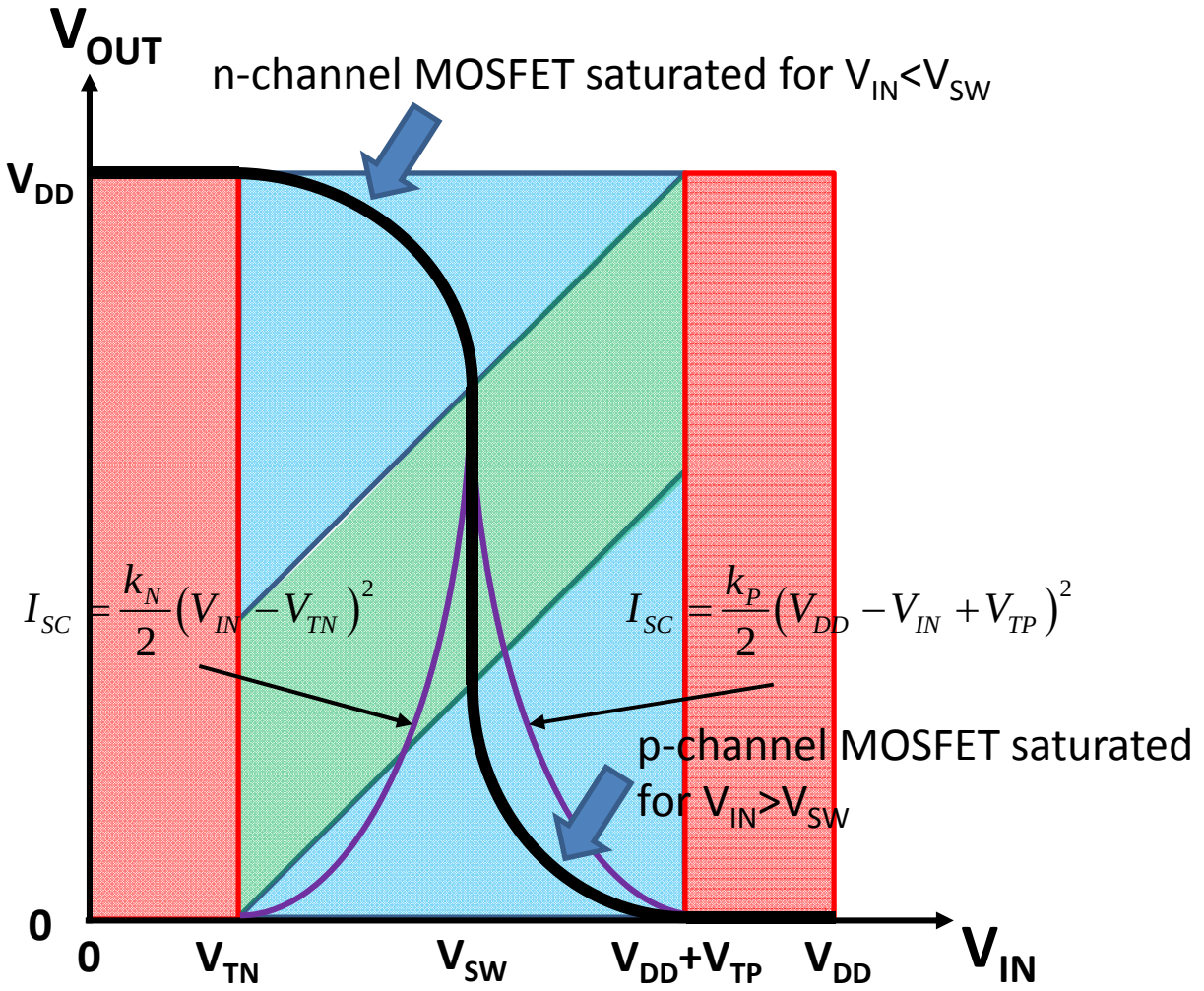
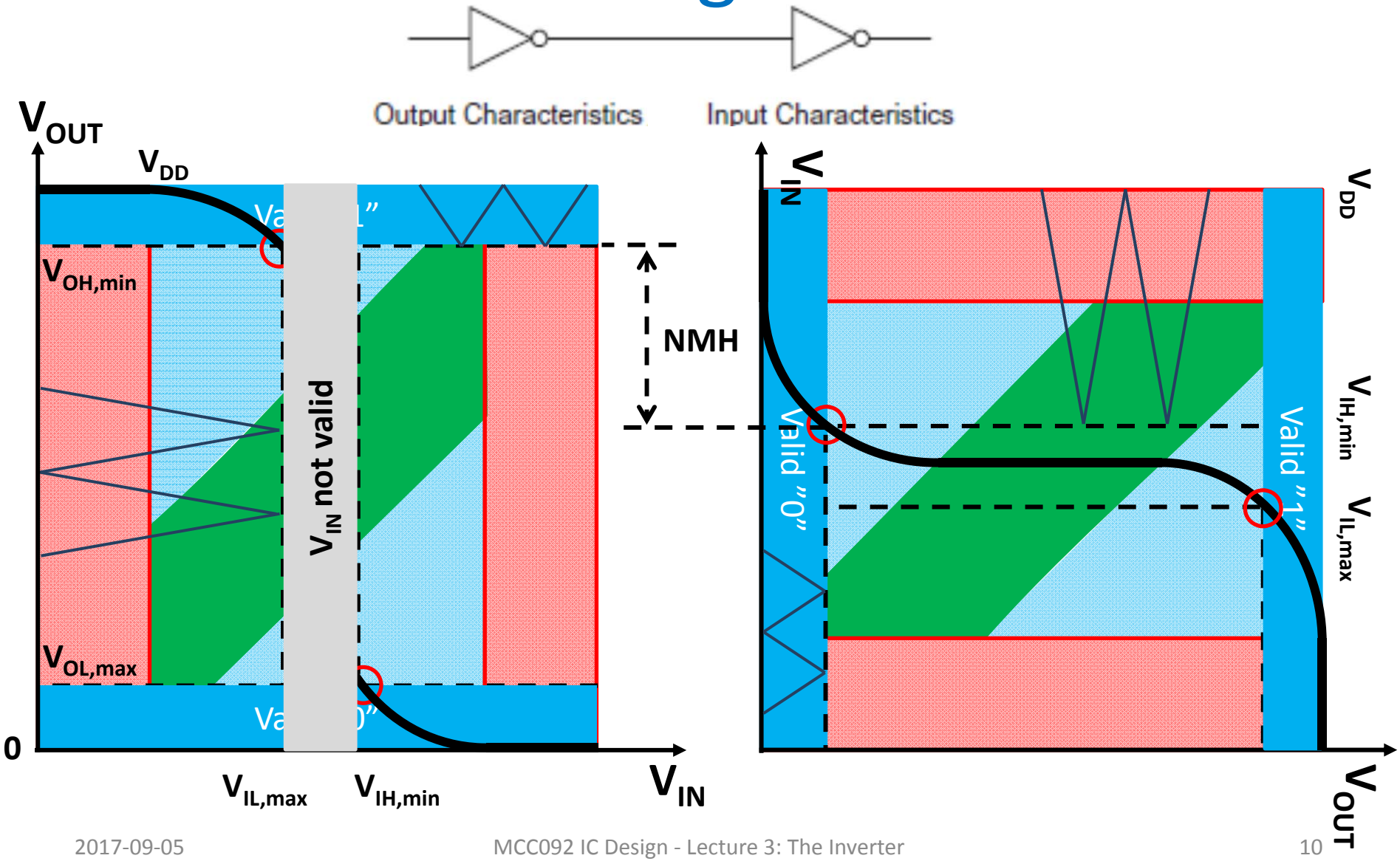


FIGURE 2.25
A CMOS inverter



Noise Margins- NML



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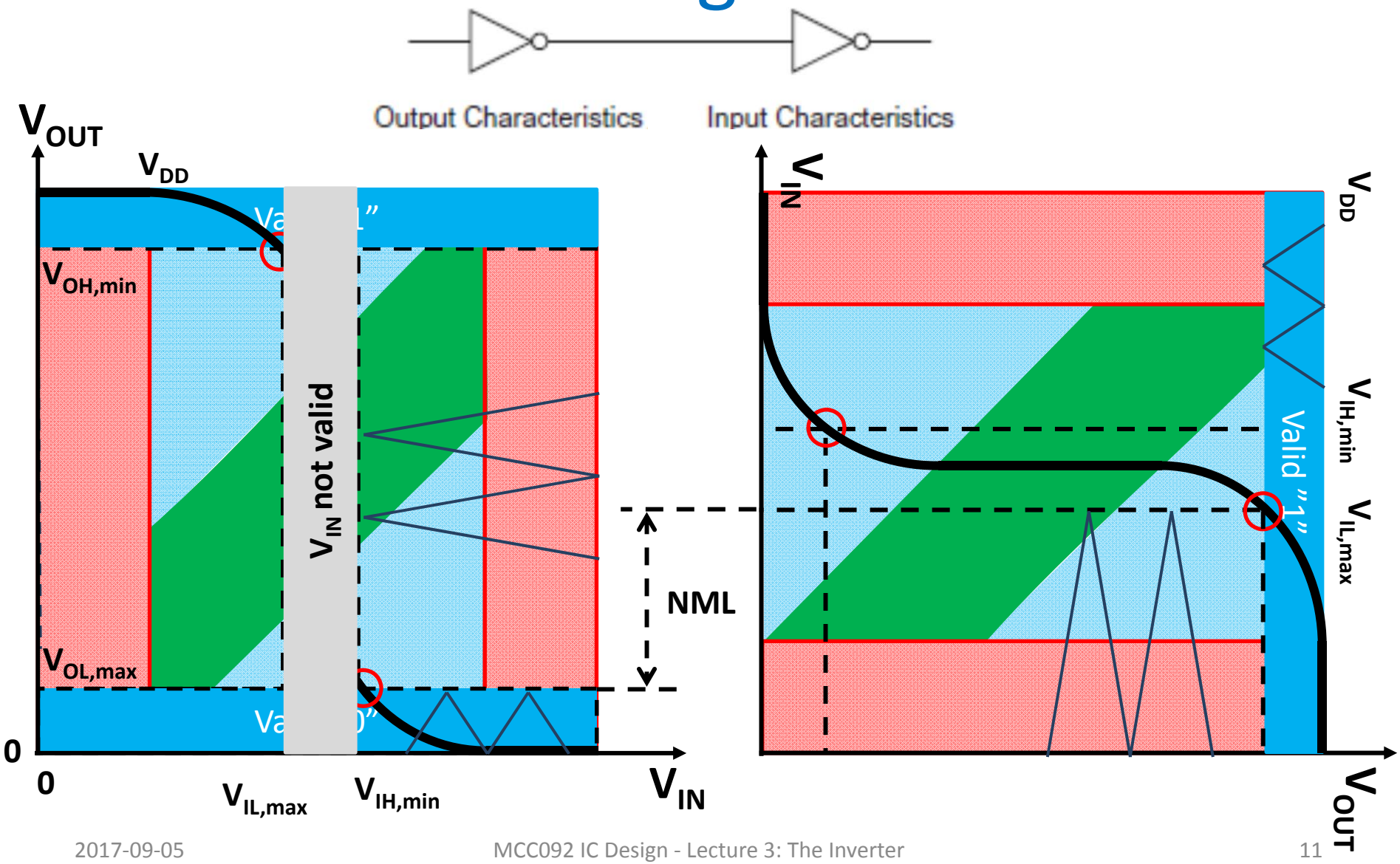
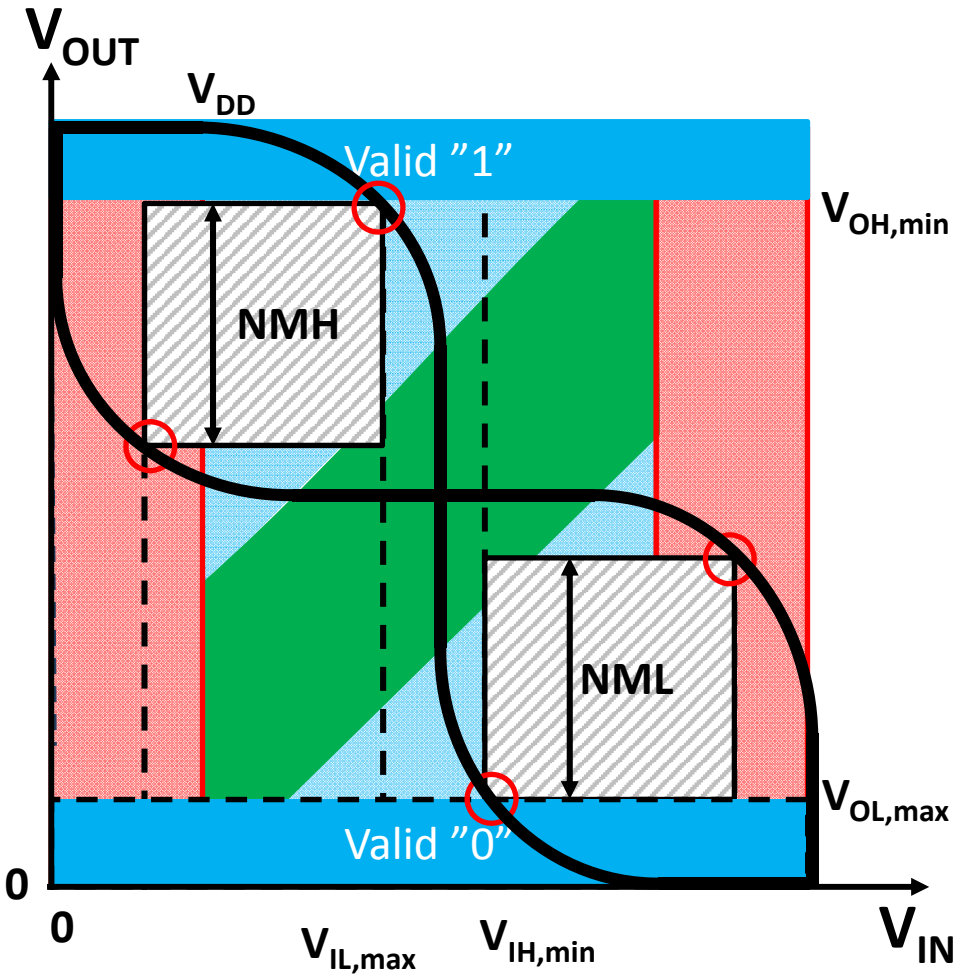
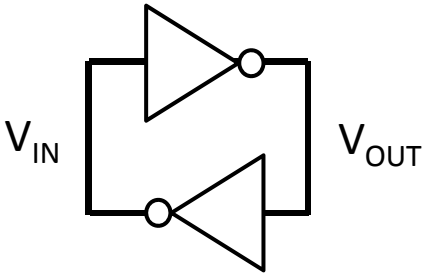


Butterfly Diagram



Memory cell characterization



Noise Margins – skewed inverters

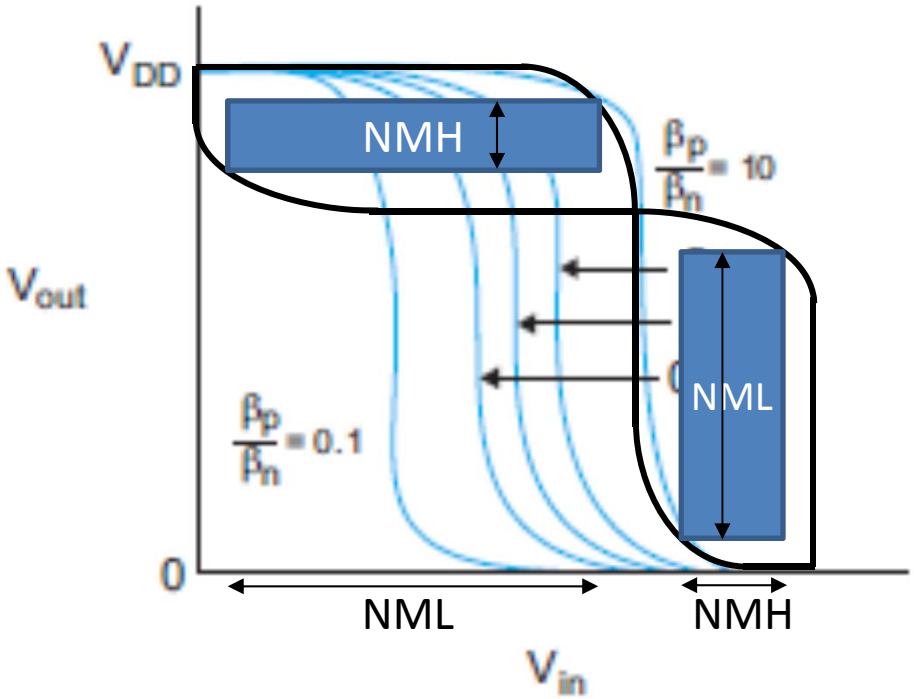


FIGURE 2.28 Transfer characteristics of skewed inverters

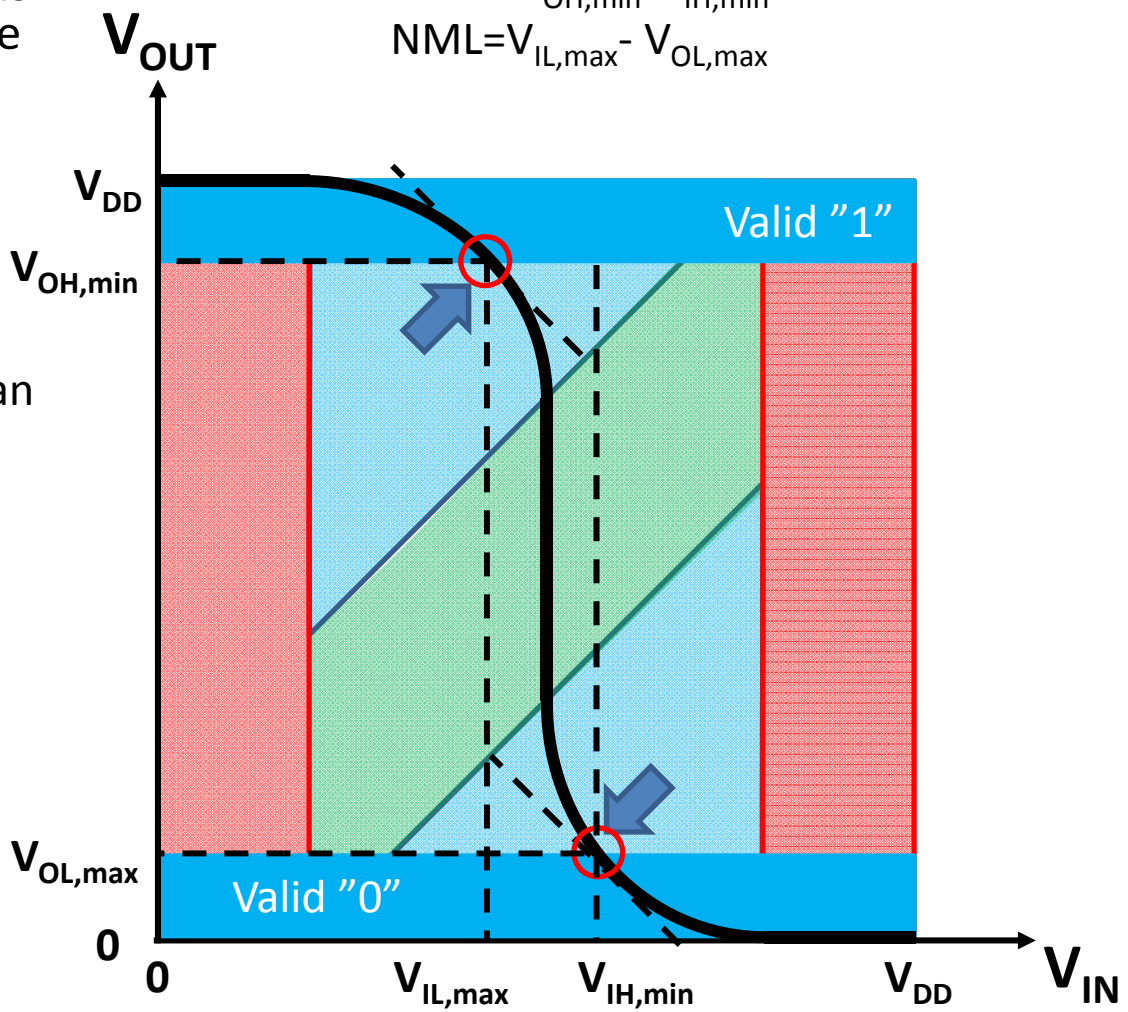
Noise Margins – an example

Let´s define valid regions from points where slope $A_V = -1$!

These points yields numbers for ($V_{OH,min}$, $V_{IL,max}$) and ($V_{OL,max}$, $V_{IH,min}$) so that NMH and NML can be calculated!

$NMH = V_{OH,min} - V_{IH,min}$

$NML = V_{IL,max} - V_{OL,max}$



Noise Margins – an example

Let´s define valid regions from points where slope $A_V = -1$!

These points yields numbers for ($V_{OH,min}$, $V_{IL,max}$) and ($V_{OL,max}$, $V_{IH,min}$) so that NMH and NML can be calculated!

For x=1, V_{TN}=0.28 V and V_{TP}=-0.28 V we have V_{SW}=0.28+0.64/2=0.60 V and ΔV=0.64 V

Formulas can be derived (for x=1):

$V_{OH,min}=V_{DD}-\Delta V/8=1.12$ V

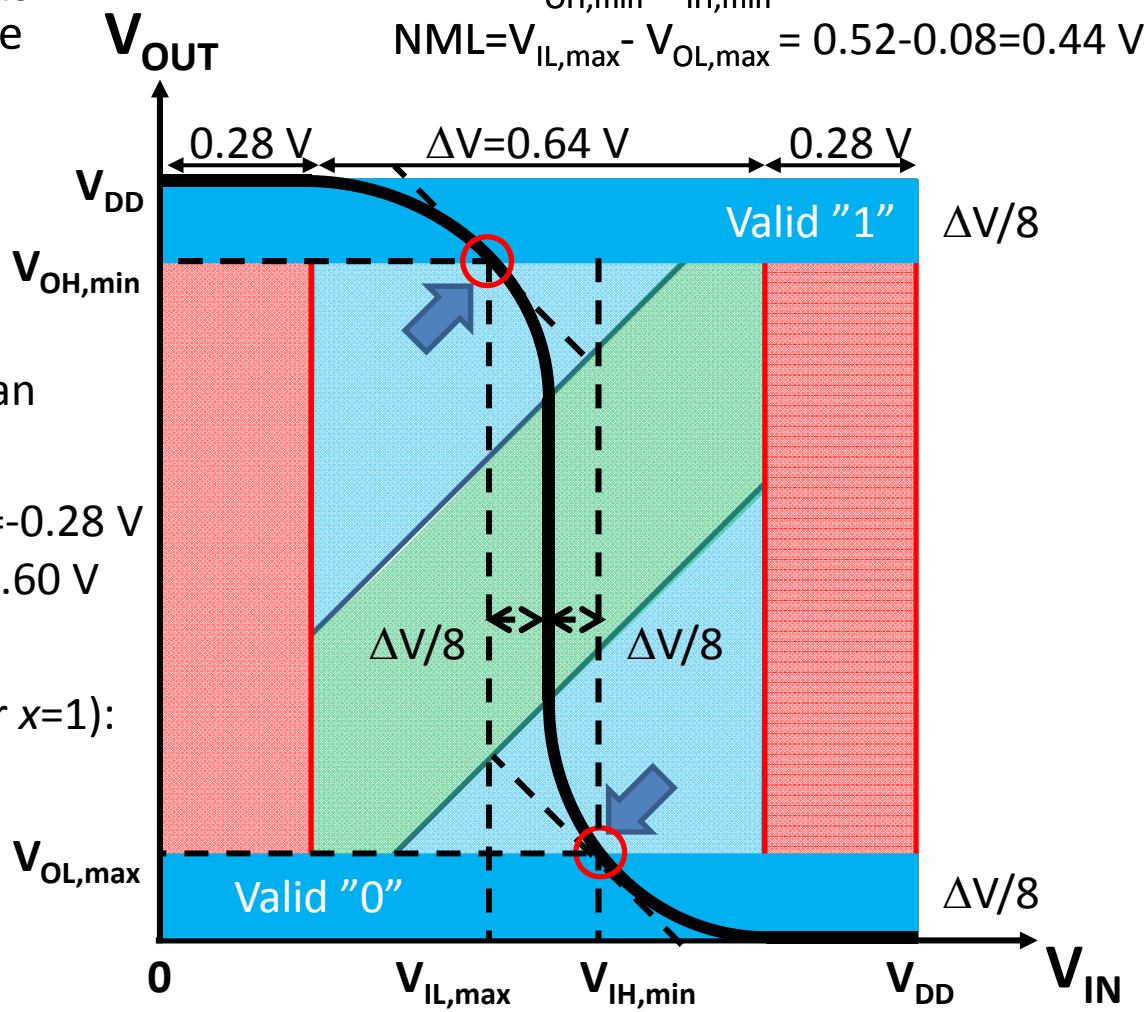
$V_{OL,max}=\Delta V/8=80$ mV

$V_{IL,max}=V_{SW}-\Delta V/8=0.52$ V

$V_{IH,min}=V_{SW}+\Delta V/8=0.68$ V

$NMH=V_{OH,min}-V_{IH,min}$ 1.12-0.68=0.44 V

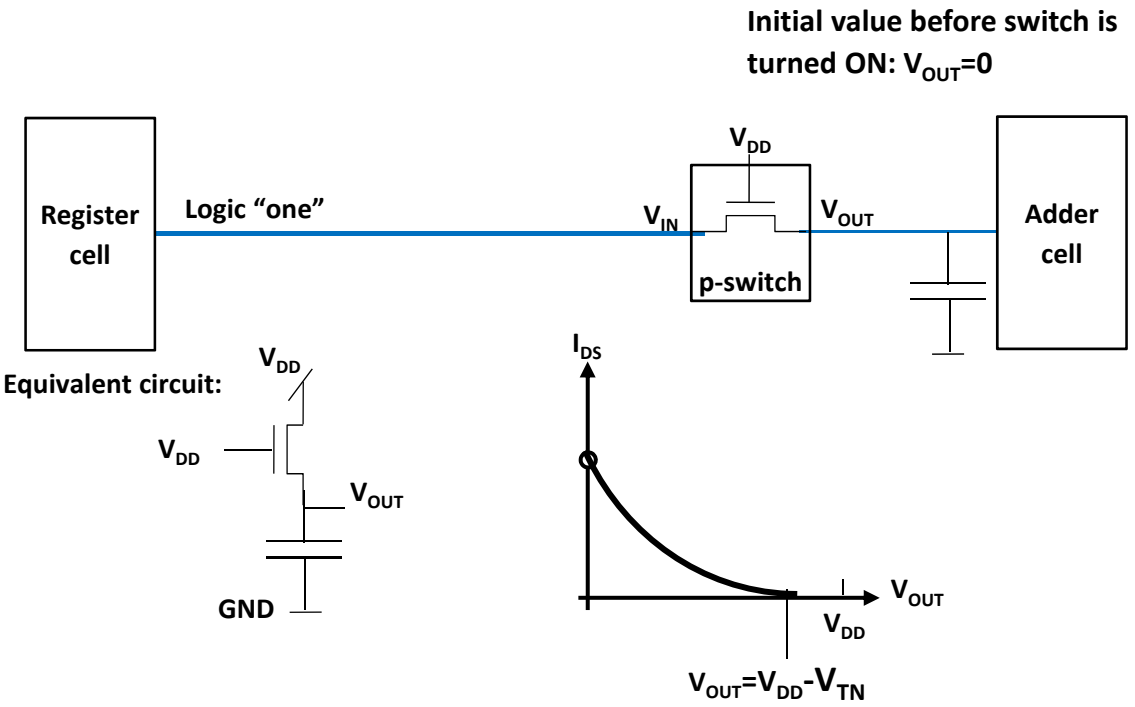
$NML=V_{IL,max}-V_{OL,max}$ = 0.52-0.08=0.44 V



Summary

- CMOS inverter – schematic
- Voltage transfer characteristics (VTC)
- How to calculate switching voltage V_{SW}
- Understand V_{SW} dependence on k_N/k_P
- Understand switching current (I_{SC}) flow
- Noise margins NMH and NML
- Butterfly diagram
- Match current curves

Why not n-switches in pull-up networks?



Why not p-switches in pull-down networks?