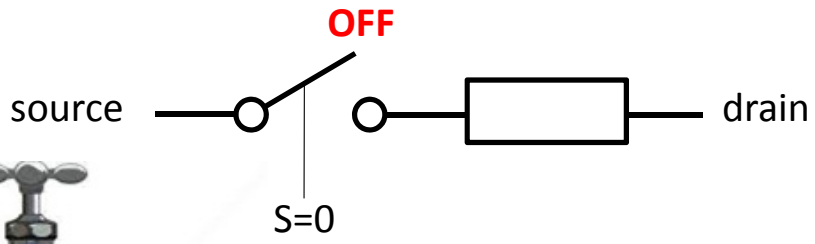
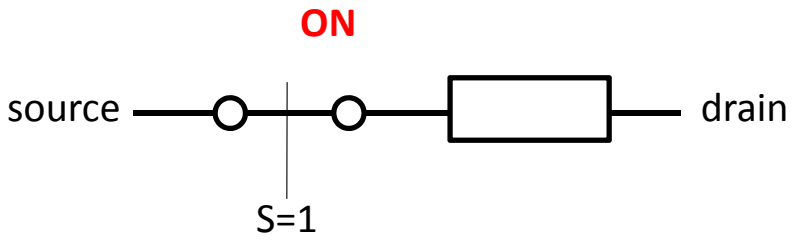
# Lecture 2

## The MOSFET

# The MOSFET as a switch

In the digital world, the MOSFET is a switch that is either *ON* with a conductance $G_{ON}>0$, or *OFF* with no conductance, $G_{OFF}=0$




For now we have assumed that $R_{ON}=0$, but today we´ll learn more about this

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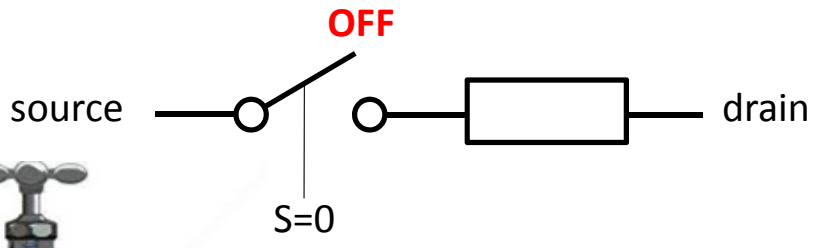
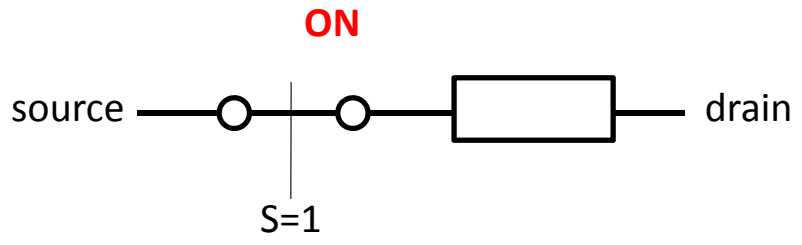
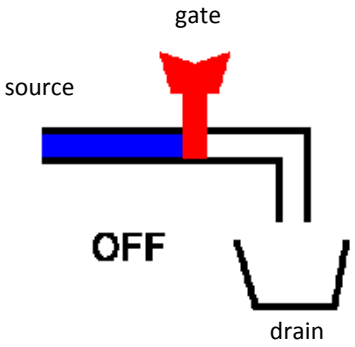
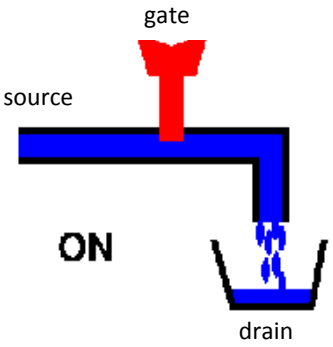


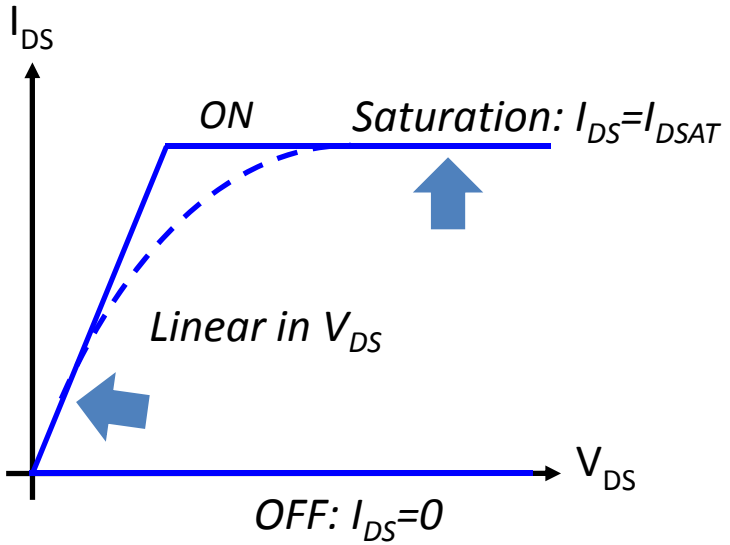




For now we have assumed that $R_{ON}=0$, but today we´ll learn more about this

# ON/OFF piecewise linear MOSFET model

*The piece-wise linear model based on two parameters ($G_{ON}$ and $I_{DSAT}$) is our backbone model*

***Why current saturation?***
*Current saturation is a combination of drain end charge →0, and charge-carrier velocity saturation*




$$I_{DS} = \begin{cases} 0 & \text{OFF} & V_{GS} < V_T \\ G_{ON} V_{DS} & \text{ON} & linear \\ I_{DSAT} & \text{ON} & saturated \end{cases}$$

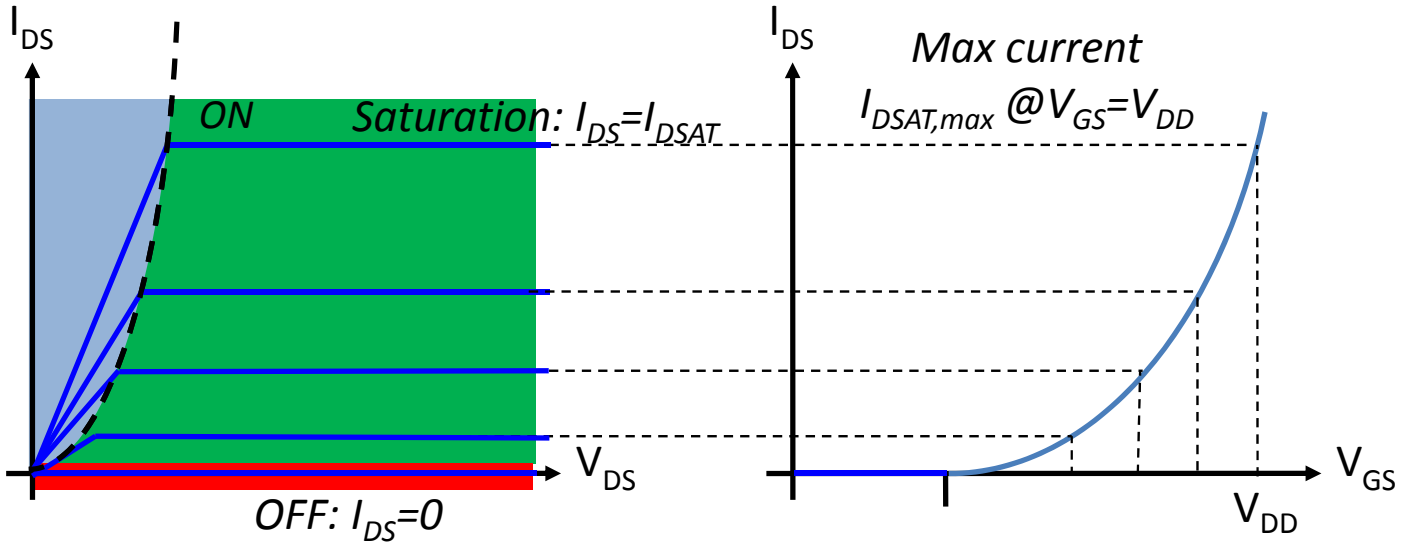
*Why piecewise linear model?*

+ Simple
+ Focus on important behavior
+ Asymptotically correct
- Poor transition region model
- Derivative not continous

# The MOSFET is a square-law device

*The piece-wise linear model based on two parameters ($G_{ON}$ and $I_{DSAT}$) is our backbone model*

***Why current saturation?***
*Current saturation is a combination of drain end charge →0, and charge-carrier velocity saturation*




$$I_{DS} = \begin{cases} 0 & \text{OFF} \quad V_{GS} < V_T \\ G_{ON} V_{DS} & \text{ON} \quad \textit{linear} \\ I_{DSAT} & \text{ON} \quad \textit{saturated} \end{cases}$$

$$I_{DSAT} = \frac{k}{2}\left(V_{GS} - V_T\right)^2$$

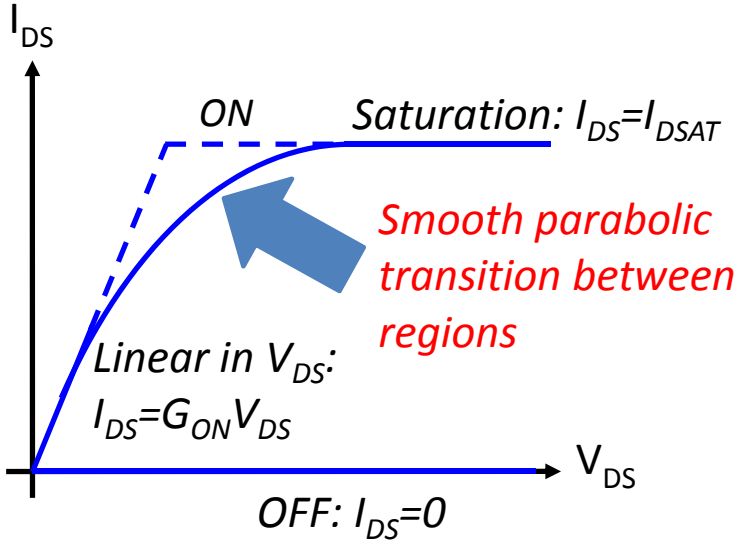
$$G_{ON} = k\left(V_{GS} - V_T\right)$$

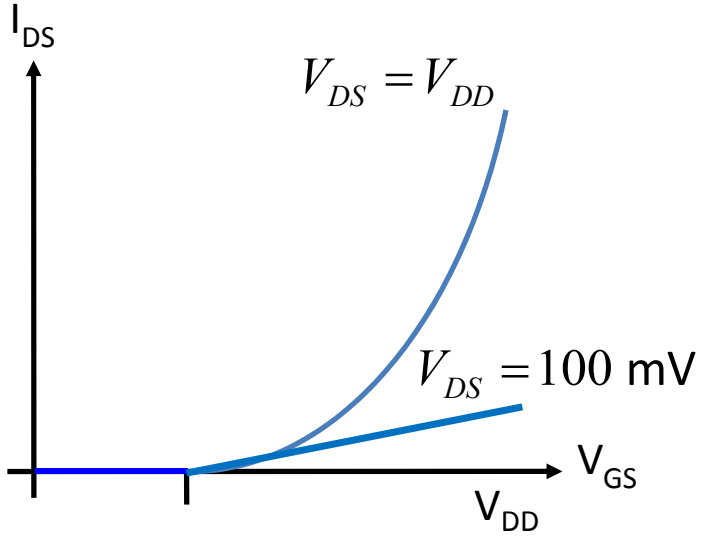
# Classic square-law MOSFET model

*The piece-wise linear model based on two parameters ($G_{ON}$ and $I_{DSAT}$) is our backbone model*

***Why current saturation?***

*Current saturation is a combination of drain end charge →0, and charge-carrier velocity saturation*




$$I_{DS} = \begin{cases} 0 & \text{OFF} \quad V_{GS} < V_T \\ G_{ON} V_{DS}\left(1 - \dfrac{V_{DS}}{2V_{DSAT}}\right) & \text{ON} \quad \textit{linear} \\ I_{DSAT} & \text{ON} \quad \textit{saturated} \end{cases}$$

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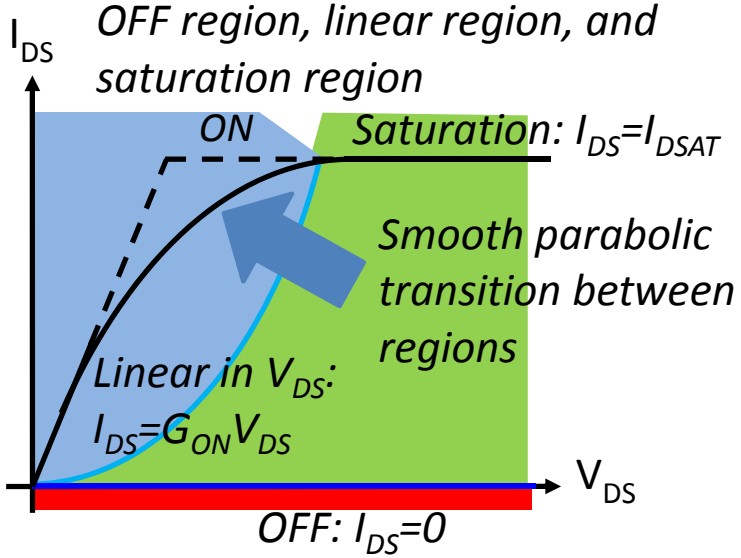
# Classic square-law MOSFET model

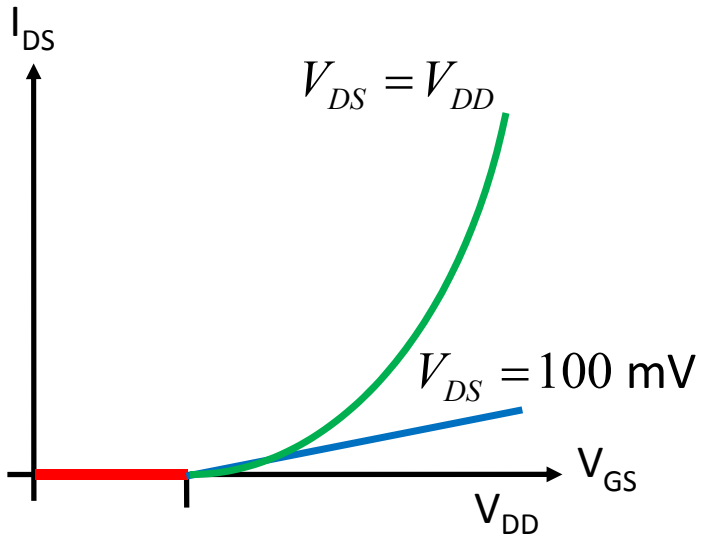
*The piece-wise linear model based on two parameters ($G_{ON}$ and $I_{DSAT}$) is our backbone model*

***Why current saturation?***

*Current saturation is a combination of drain end charge →0, and charge-carrier velocity saturation*

*Introduce color coding for OFF region, linear region, and saturation region*




$$I_{DS} = \begin{cases} 0 & \text{OFF} \quad V_{GS} < V_T \\ G_{ON} V_{DS}\left(1 - \dfrac{V_{DS}}{2V_{DSAT}}\right) & \text{ON} \quad \textit{linear} \\ I_{DSAT} & \text{ON} \quad \textit{saturated} \end{cases}$$

$$I_{DSAT} = \frac{k}{2}\left(V_{GS} - V_T\right)^2$$

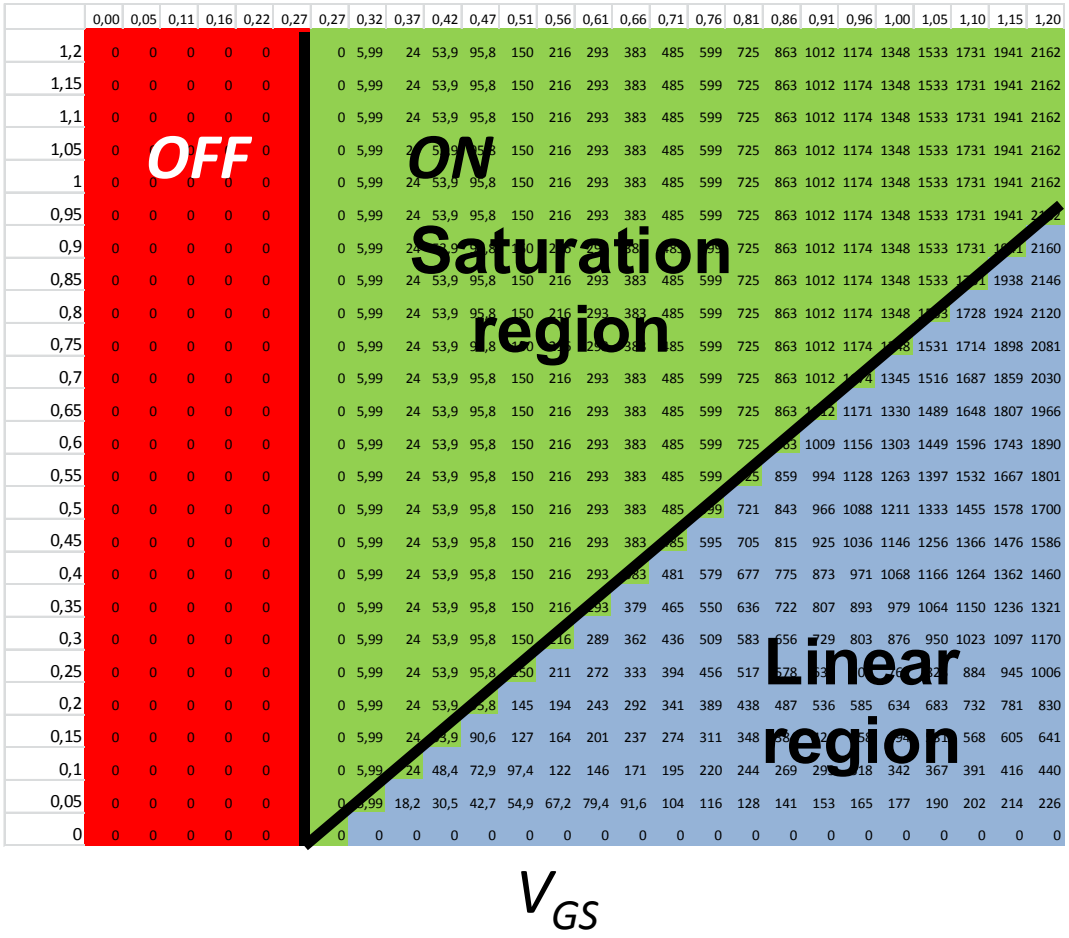
$$G_{ON} = k\left(V_{GS} - V_T\right)$$

Define $V_{GT} = V_{GS} - V_T$

# MOSFET models can predict $I_{DS}$ for any $V_{GS}/V_{DS}$

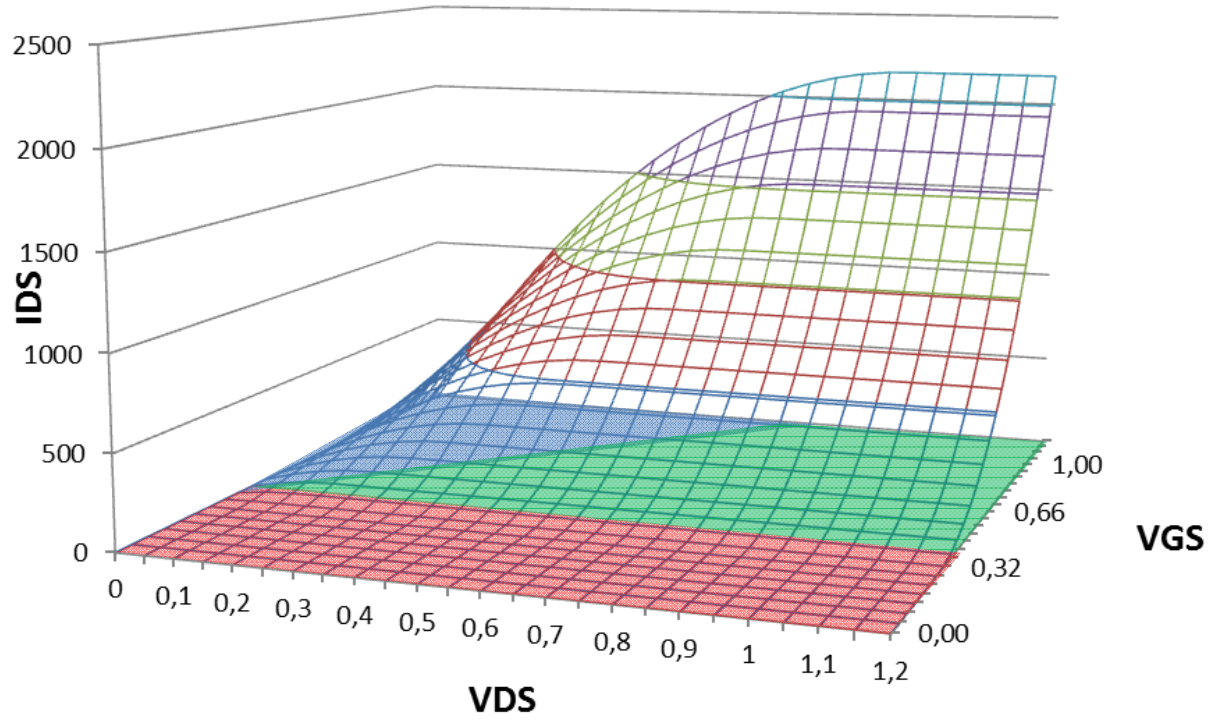
**Focus on saturated region**

Blue and red regions tell us when to be alert for errors in using saturation model




$$V_{DS} = V_{GS} - V_T = V_{GT}$$

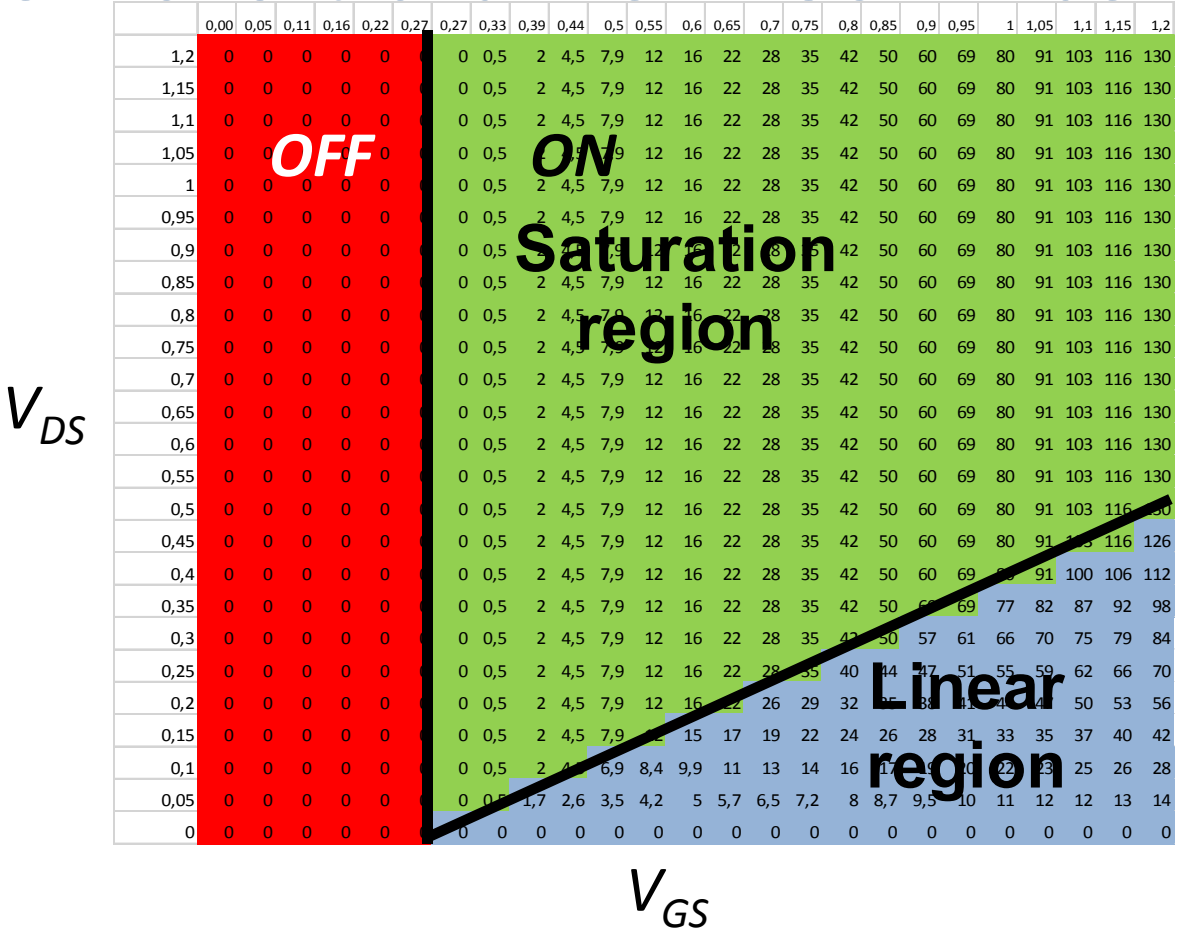
# $I_{DS}$ can be plotted in 3D vs. $V_{GS}$&$V_{DS}$



# Piecewise linear MOSFET model is actually closer to modern short-channel MOSFET behavior

**Focus on saturated region**

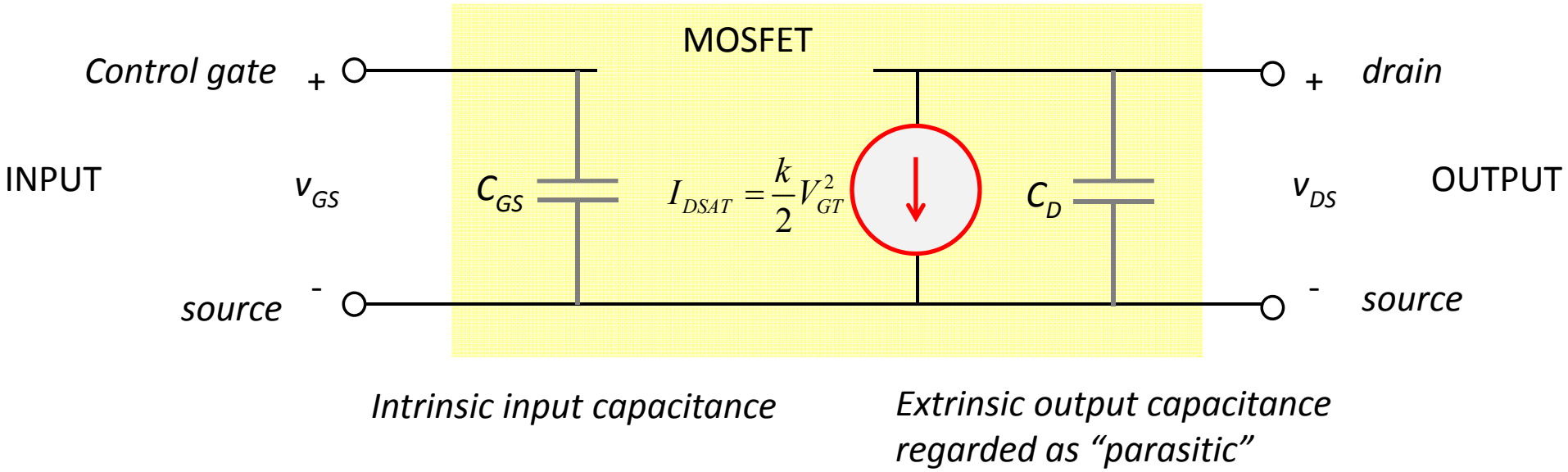
Blue and red regions tell us when to be alert for errors in using saturation model



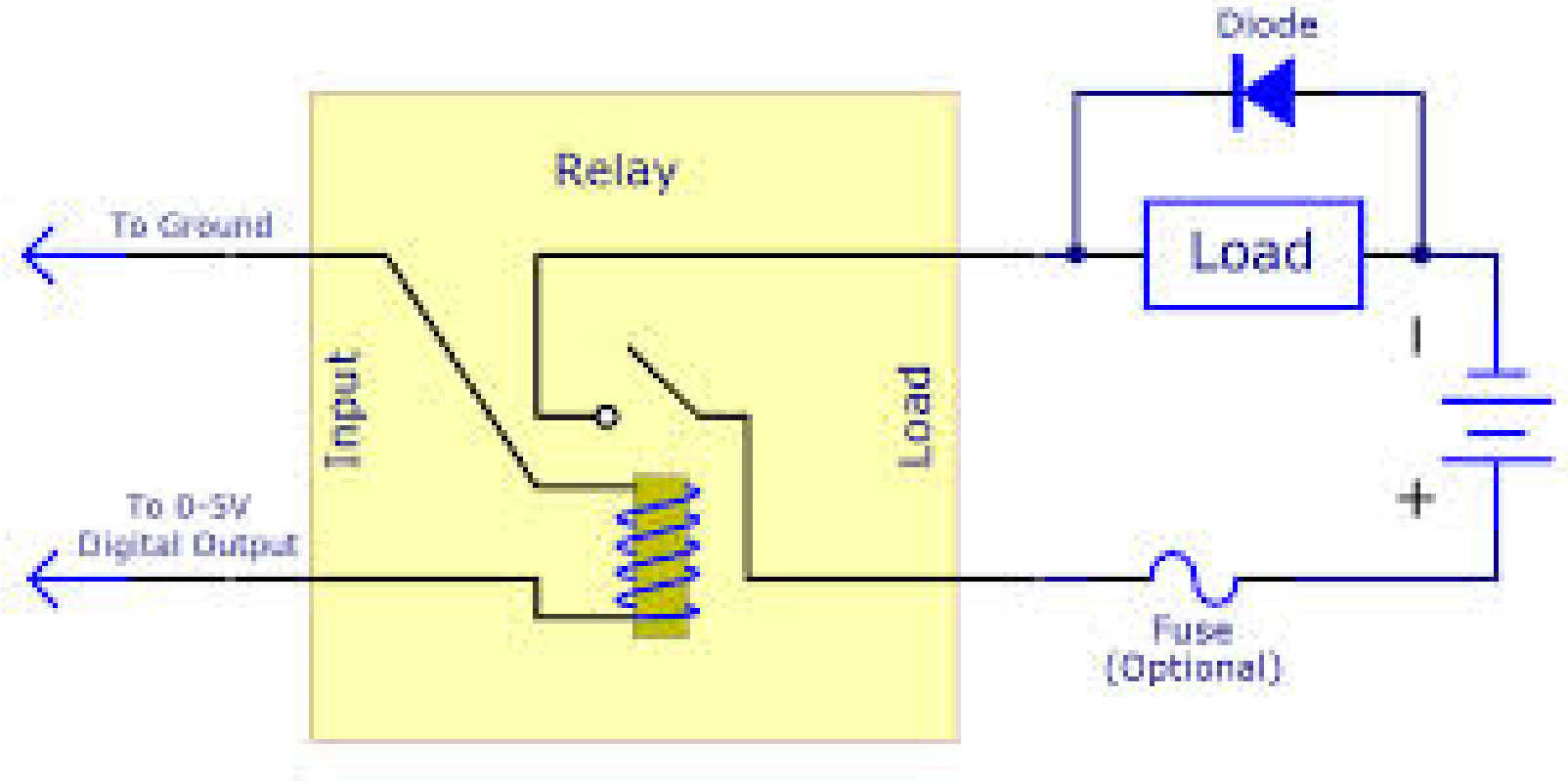

$$V_{DS} = \frac{V_{GS} - V_T}{2} = \frac{V_{GT}}{2}$$

# Electrical two-port MOSFET model

## FOCUS ON THE SATURATED MOSFET

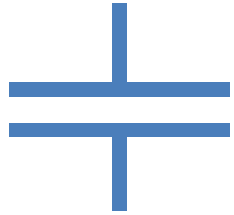


# Electrical relay two-port model



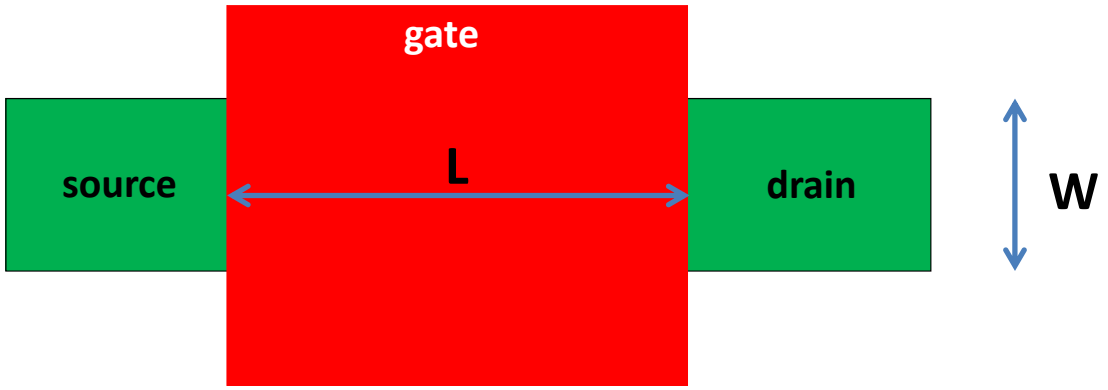
# Some slides on MOSFET theory

- To find out how $G_{ON}$ depends on geometry and voltages we need a little theoretical discussion
- MOSFETs are field effect transistors, i.e. FETs, which means that the ON/OFF function is a capacitive effect
- Capacitor charge = capacitance * voltage: Q=CV
- Parallel plate capacitance per unit area C=$\varepsilon$/thickness, where $\varepsilon$ is the permittivity of the insulator. In a MOSFET $\varepsilon_{ox}=4\varepsilon_0$

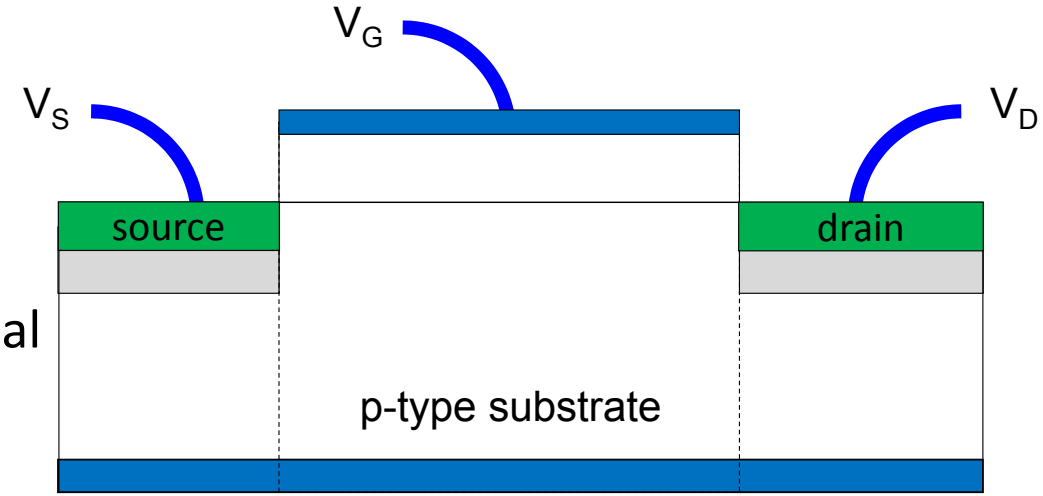


# MOSFET geometry

MOSFET top view



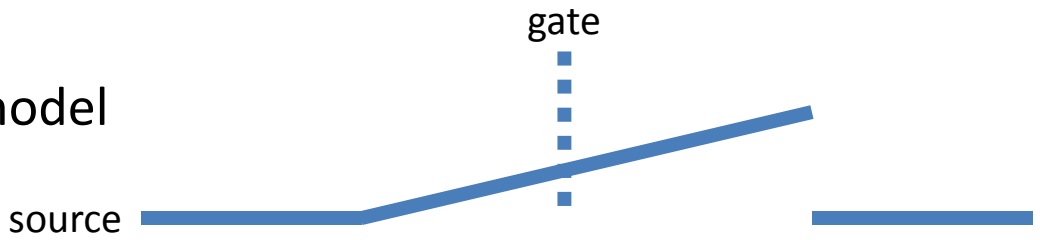

MOSFET cross sectional view




The n-channel MOSFET

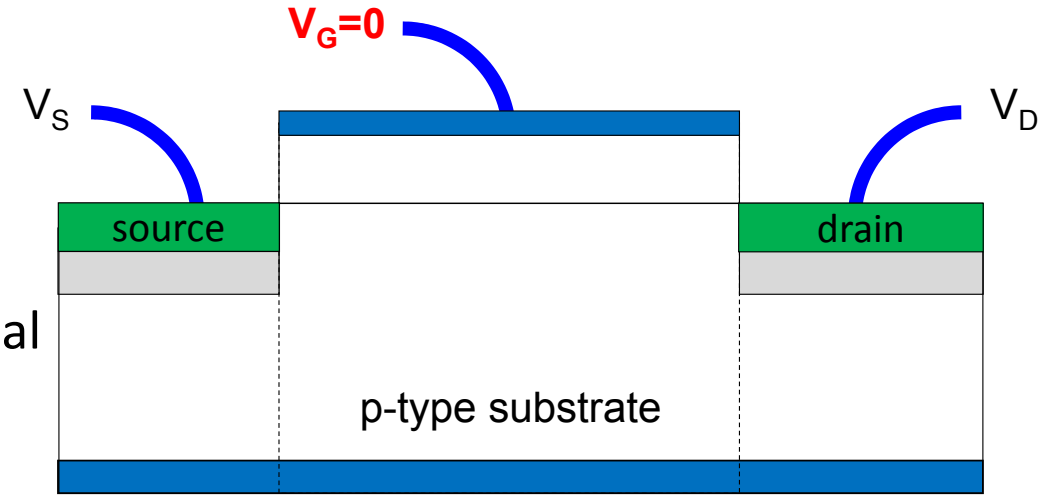
# MOSFET theory – no gate voltage applied

MOSFET switch model




MOSFET switch is OFF

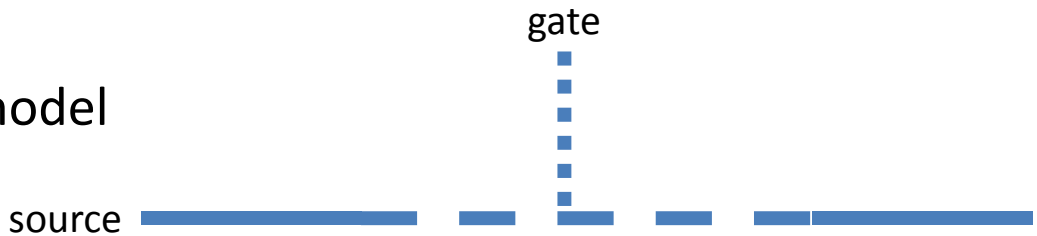
MOSFET cross sectional view




The n-channel MOSFET

# MOSFET theory – applying a gate voltage

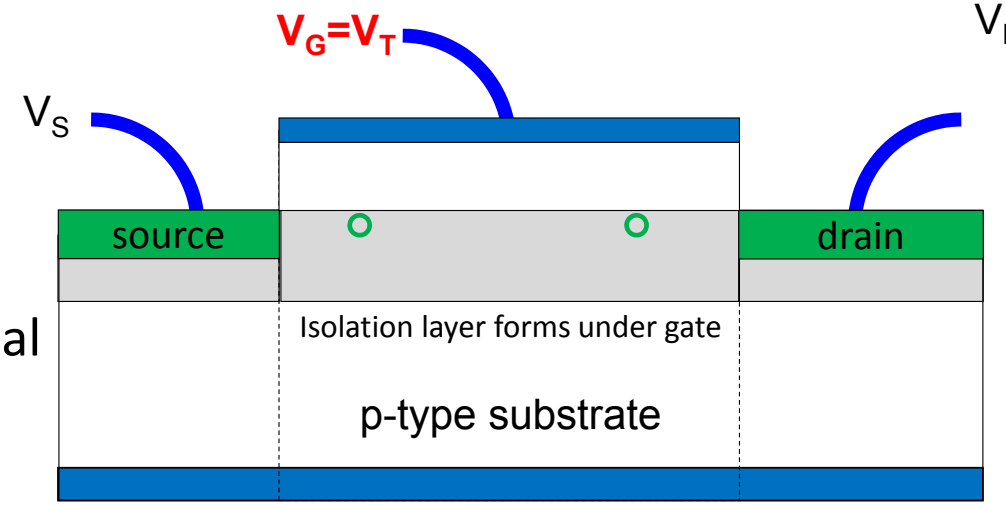
MOSFET switch model




MOSFET switch is leaky

The threshold voltage $V_T$ is the gate voltage needed to form the isolation layer

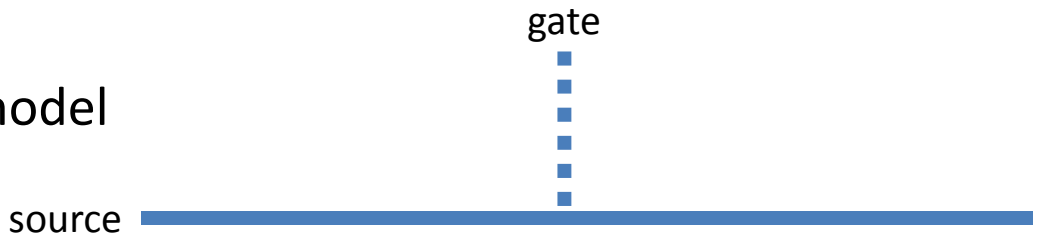
MOSFET cross sectional view




The n-channel MOSFET

# MOSFET theory – applying a gate voltage

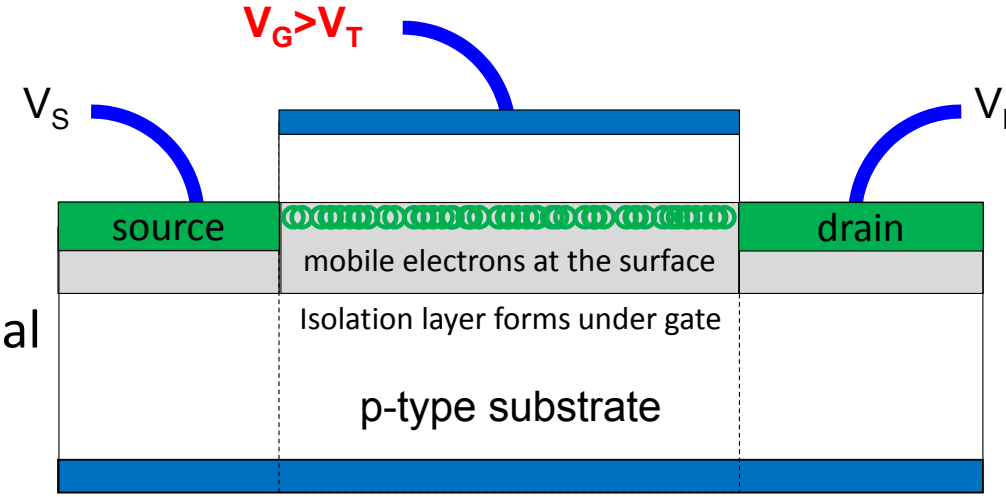
MOSFET switch model




MOSFET switch is ON

The threshold voltage $V_T$ is the gate voltage needed to form the isolation layer

MOSFET cross sectional view

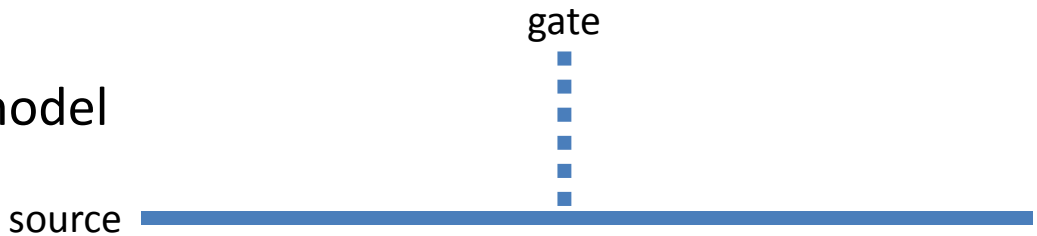



The n-channel MOSFET

For $V_G > V_T$ a channel of mobile electrons is formed between the source and drain

# MOSFET theory – applying a gate voltage

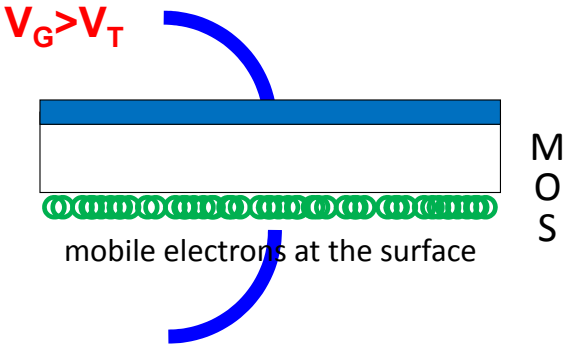
MOSFET switch model




MOSFET switch is ON

The threshold voltage $V_T$ is the gate voltage needed to form the isolation layer

A parallel-plate capacitor between gate and channel
MOS means Metal-oxide-semiconductor
Hence, a MOS capacitor
Capacitor formula Q=C*V




For $V_G > V_T$ a channel of mobile electrons is formed between the source and drain

$$Q_{channel} = WC_{ox}\left(V_{GS} - V_T\right)$$

W is MOSFET channel width
Cox is gate capacitance per unit area

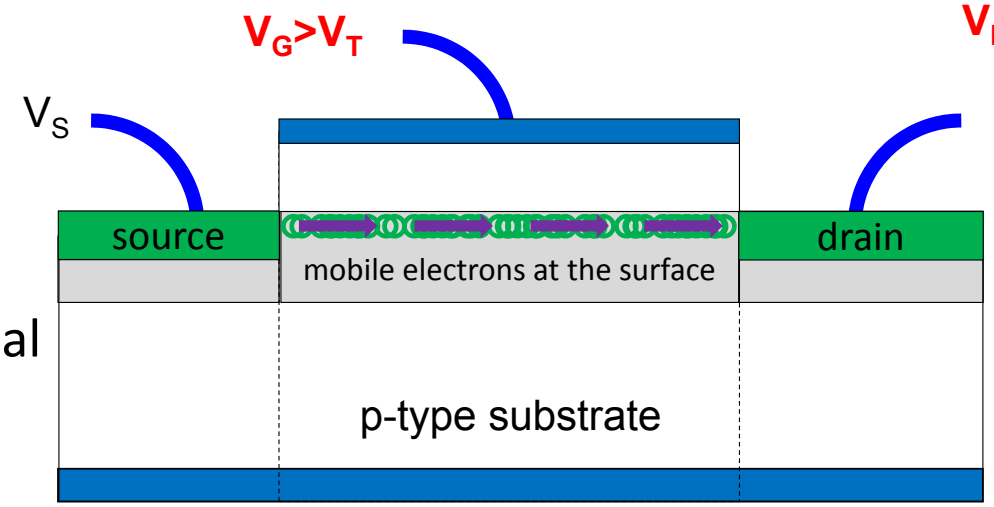
# MOSFET theory – applying a drain voltage

- The drain to source voltage creates an electric field that gives the mobile electrons in the channel at the silicon surface a drift velocity

$$v_{channel} = \mu \frac{V_{DS}}{L}$$

$\mu$ is electron mobility
$E=V_{DS}/L$ is electric field

MOSFET cross sectional view




The n-channel MOSFET

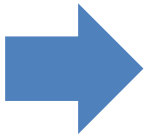
**$V_D \neq 0$ but still considered small**

For $V_G > V_T$ a channel of mobile electrons is formed between the source and drain

$$Q_{channel} = WC_{ox}\left(V_{GS} - V_T\right)$$

W is MOSFET channel width
Cox is gate capacitance per unit area

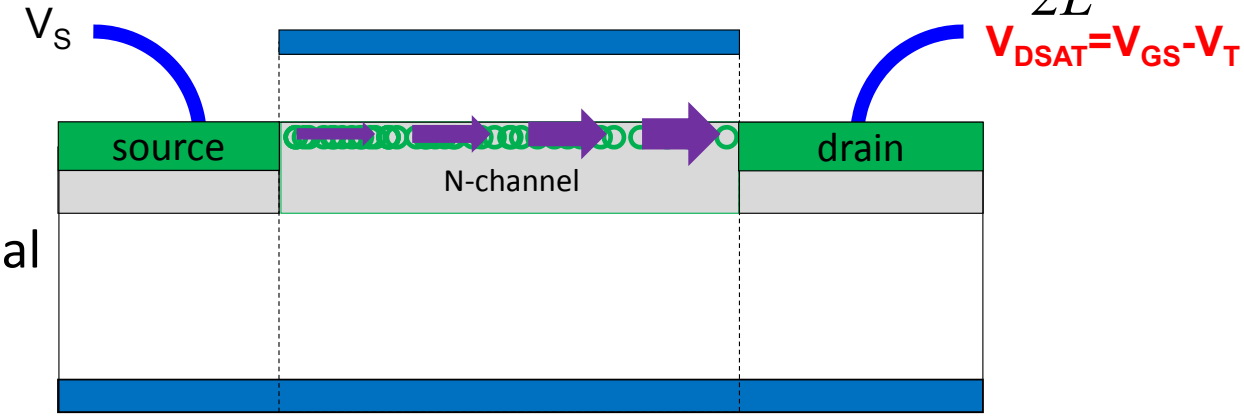
# Determining the ON-conductance $G_{ON}$

- Current is number of charges that pass per unit time
- i.e. Current = charge per unit lenght x velocity
- Therefore, $I_{DS} = WC_{ox}\left(V_{GS} - V_T\right) \times \mu \frac{V_{DS}}{L}$
- Rewrite $I_{DS} = \frac{W}{L}\mu C_{ox}\left(V_{GS} - V_T\right)V_{DS} = G_{ON}V_{DS}$  $G_{ON} = \frac{W}{L}\mu C_{ox}\left(V_{GS} - V_T\right)$
- *L* is the channel length, i.e. distance between source and drain

# MOSFET theory – forcing MOSFET into saturation

- When the drain voltage increases the MOSFET approaches saturation and enters saturation when $V_{DS}=V_{GS}-V_T$
- Charge injected at source $Q_{source} = WC_{ox}\left(V_{GS} - V_T\right)$
- Maximum charge velocity at source: $v_{source} = \mu \frac{V_{GS} - V_T}{2L}$

MOSFET cross sectional view

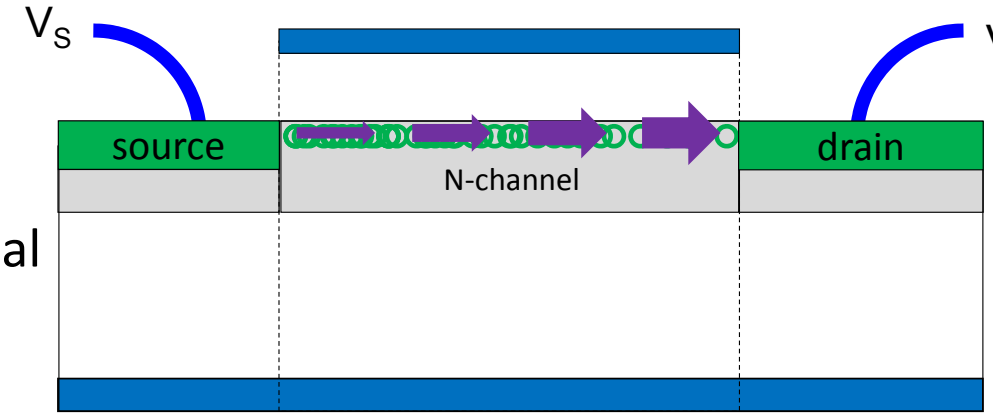



The n-channel MOSFET

# MOSFET theory – forcing MOSFET into saturation

- When the drain voltage increases the MOSFET approaches saturation and enters saturation when $V_{DS}=V_{GS}-V_T$
- Saturation current: $$I_{DS} = \frac{1}{2}\frac{W}{L}\mu C_{ox}\left(V_{GS} - V_T\right)^2$$

MOSFET cross sectional view

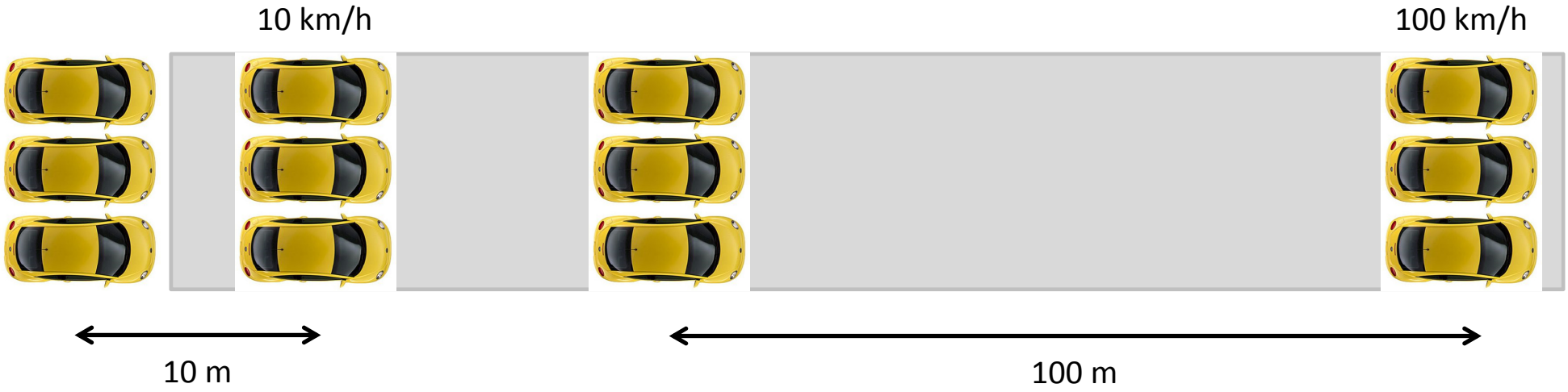



The n-channel MOSFET

The MOSFET is a square-law device

# It is like cars on a motorway

- Cars entering motorway at 10 km/h and exits at 100 km/h.
- Flow rate of cars is constant: one exit for each entry



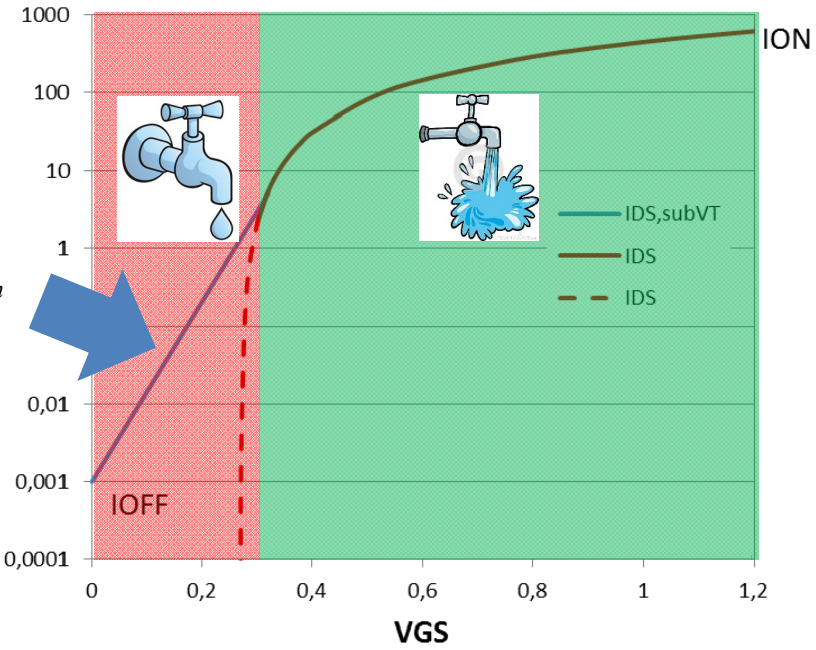
# How abrupt is the turn-off at $V_T$?

- Is there no current at all below the threshold?

# How abrupt is the turn-off at $V_T$?

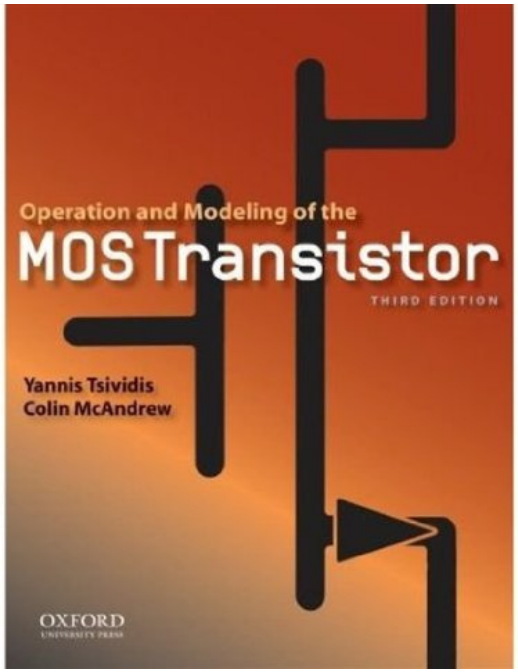
- Is there no current at all below the threshold?
- Finding a sub-$V_T$ model

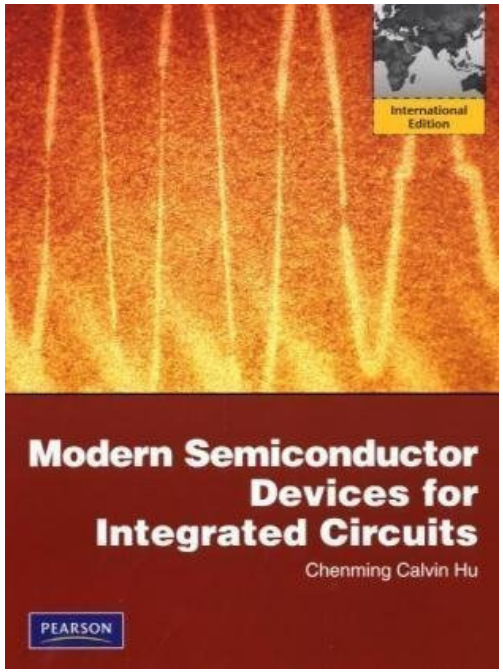
$$I_{DS,sub\text{-}VT} = I_{OFF} e^{V_{GS}/nV_{th}}$$

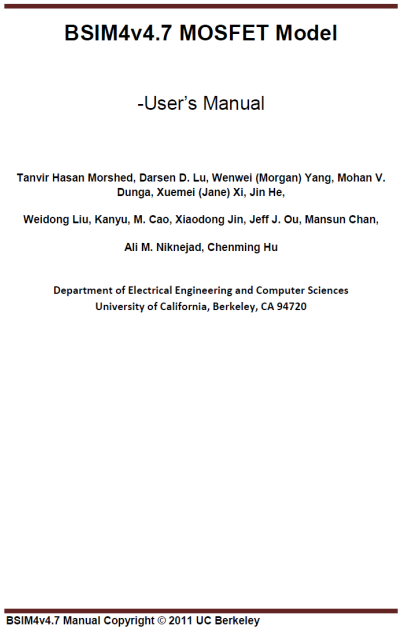


# The MOSFET in detail

- A number of textbooks treat MOSFET models in great detail, including their physical background and short-comings due to short-channel effects in nanoscale devices





BSIM4v4.7 MOSFET Model

-User's Manual

Tanvir Hasan Morshed, Darsen D. Lu, Wenwei (Morgan) Yang, Mohan V. Dunga, Xuemei (Jane) Xi, Jin He,

Weidong Liu, Kanyu, M. Cao, Xiaodong Jin, Jeff J. Ou, Mansun Chan,

Ali M. Niknejad, Chenming Hu

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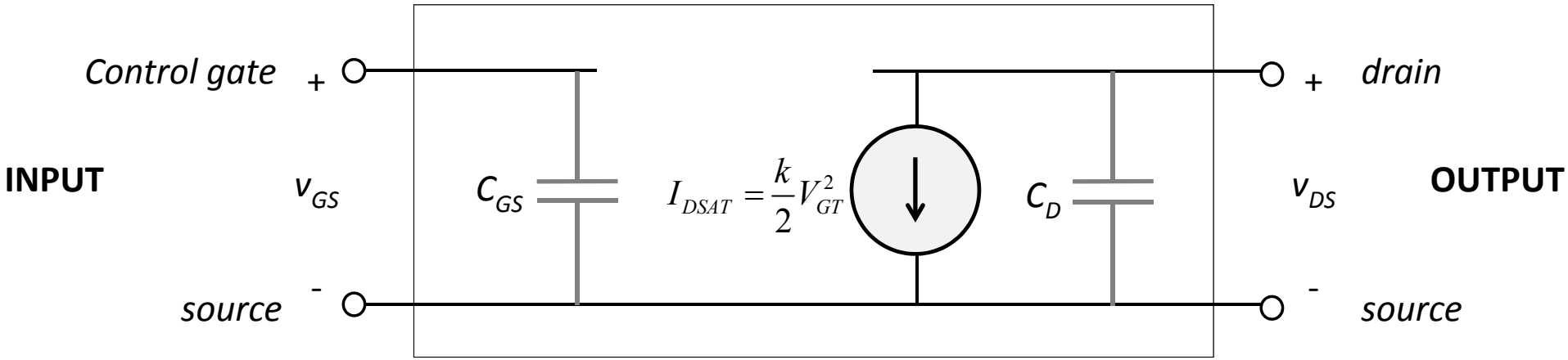
# Summary

- The MOSFET is treated as an electrically controlled ON/OFF switch.
- The input gate voltage is referred to the source, hence $V_{GS}$.
- The output drain voltage is also referred to the source, hence $V_{DS}$.
- The MOSFET current is a function of both voltages, $V_{GS}$ and $V_{DS}$.
- The ON MOSFET behaves like a resistor $R_{ON}$ in the linear region, and like a constant-current source $I_{DSAT}$ in the saturation region.
- First-order model of the saturation current is a square-law model.
- In an OFF MOSFET there is a subthreshold leakage current, $I_{SUB}$.
- Use color-coding in red, blue, and green to separate the three regions of MOSFET operation
  - Useful when deriving the static properties of the CMOS inverter.
- Focus on MOSFET as a saturated device

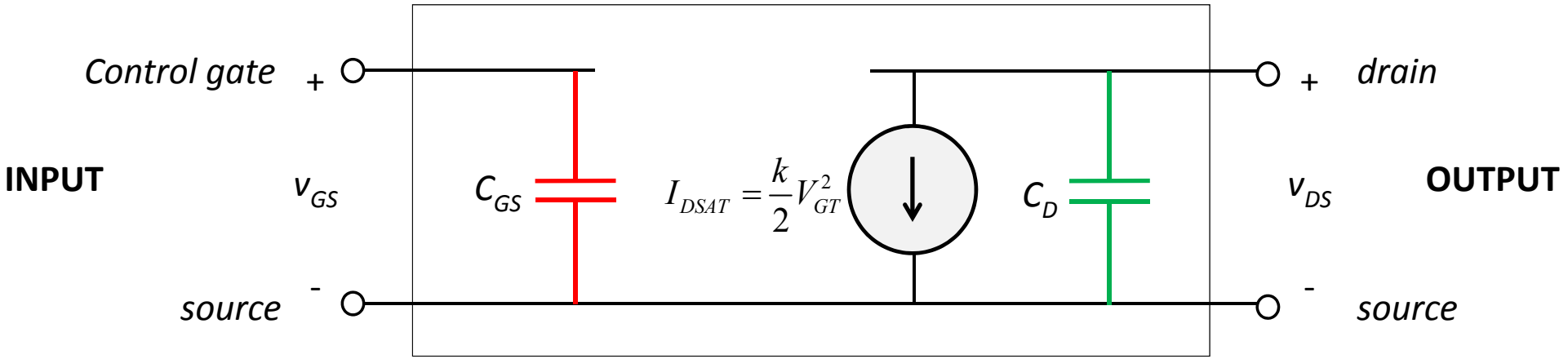
# Lecture 2b

## The MOSFET
## Dynamic properties
## (Capacitances)

# Saturated MOSFET model



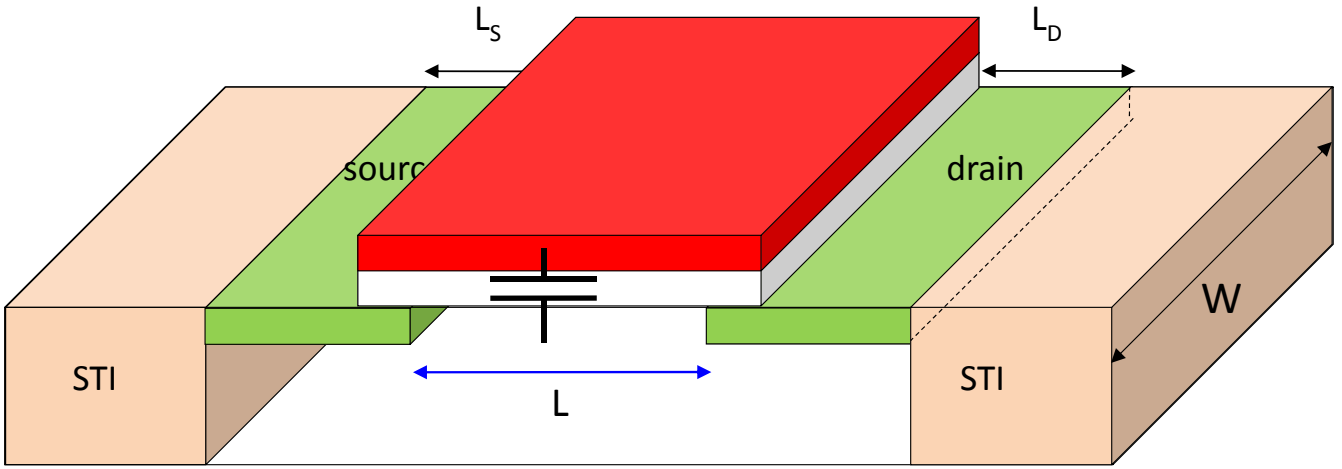
# Saturated MOSFET model




*Intrinsic input capacitance*

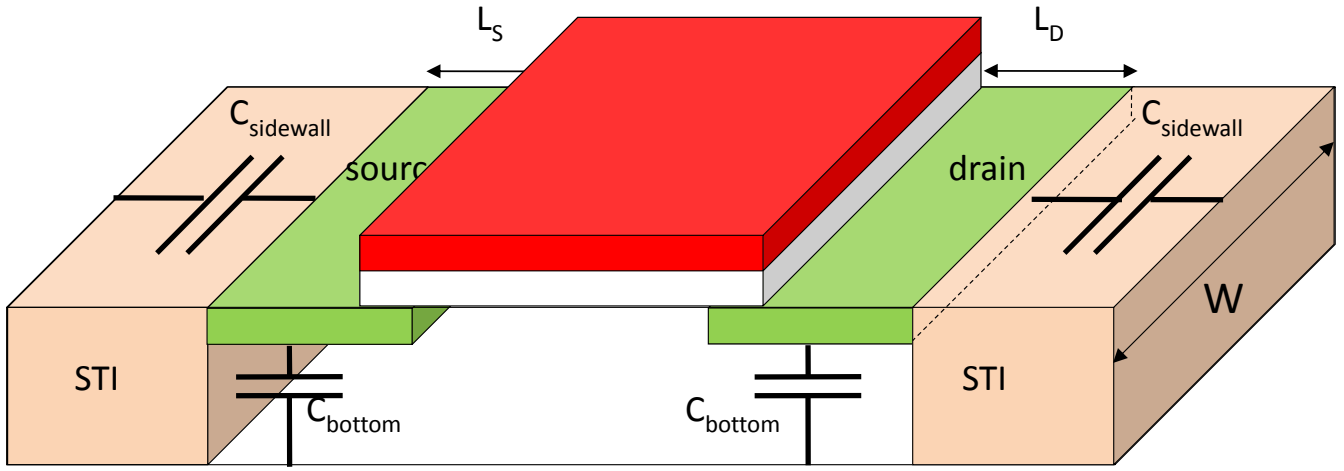
*Extrinsic output capacitance regarded as "parasitic"*

# MOSFET gate capacitance



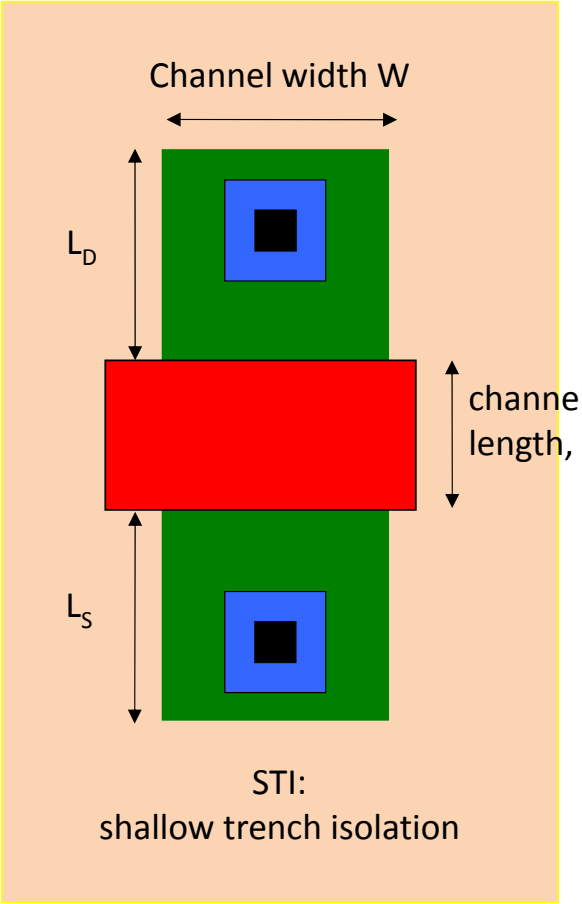

The gate capacitance $C_G$, causing the field effect is considered a parallel-plate capacitor: $C_G=WLC_{ox}$
i.e. (the red gate area) x (the oxide capacitance $C_{ox}$ per unit area)
In a 65 nm CMOS process, typically $C_{ox}$=20 fF/μm$^2$

# Source/drain parasitic capacitances




The parasitic source and drain capacitances, $C_S$ and $C_D$ respectively, can be calculated as a sum of the bottom plate capacitance $C_{bottom}$ and the sidewall capacitances $C_{sidewall}$ where the sidewall to the channel and the sidewalls to the shallow trench isolations (STIs) are to be treated differently.

# 65 nm CMOS capacitances




Gate oxide capacitance per unit area $C_{ox}$≈20 fF/um$^2$
(corresponds to 1.2 nm effective oxide thickness, EOT)

Gate capacitance $C_G$=$C_{ox}$*60 nm per micron channel width
(For different reasons the channel length in this 65 nm CMOS process is only 60 nm, so we have used L=60 nm)

For our calculations: $C_G$=1.2 fF/um

The parasitic drain/source capacitances are of the same order of magnitude as the gate capacitance, $C_S$=$C_D$=$p_{inv}C_G$

Generic approach: use $p_{inv}$ =1 to avoid detailed calculations
(We leave the detailed calculations to the circuit simulator)

# Conclusion

In this lecture, we started considering MOSFET static properties

- Three regions of operation
  - Two ON regions: linear or saturated
  - One OFF region: subthreshold

In second half of lecture we also considered dynamic properties

- The intrinsic gate capacitance
- The extrinsic, or parasitic drain capacitance

We came up with a final two-port model including both static circuit elements (current-source), and dynamic elements, i.e. capacitances!