Lecture 11 b
Metastability

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Why care?

- Digital abstraction:
  - All signals in a system must have a valid digital representation
- Consequence: Must reliably synchronize external events

Real world problem!

- Inputs from real world are usually not synchronous with system clock.
- Inputs from other synchronous systems are based on another system clock usually not synchronous with your system clock.

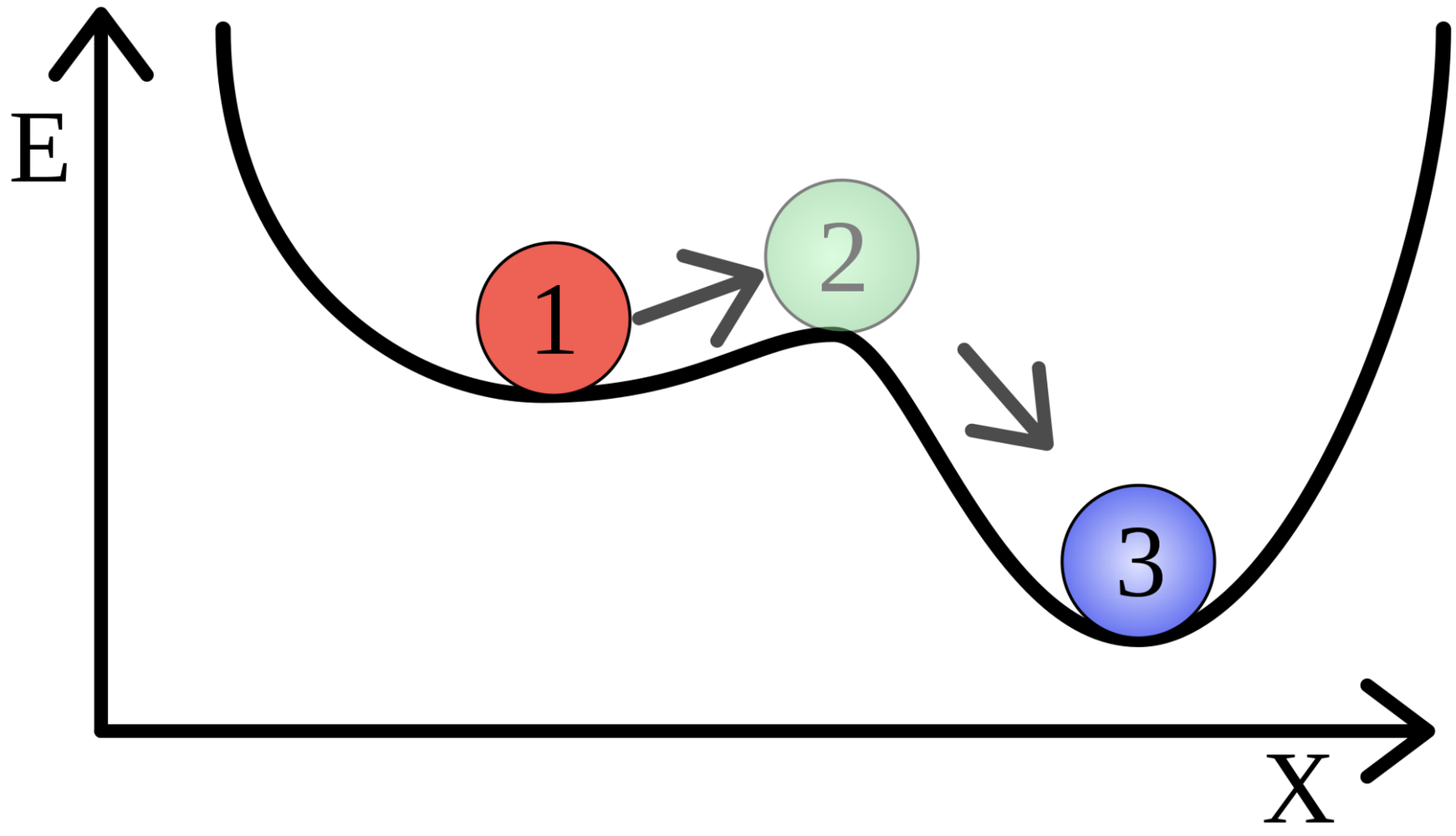
The metastability equation

$$MTBF = \frac{e^{\frac{S}{\tau}}}{T_W f_c f_D}$$

MTBF is the figure of merit for synchronisation
In this lecture we will derive this equation
See how problem can be alleviated

Derivation follows: "Metastability and Synchronizers: A tutorial" by R. Ginosar 2011
Paper is available in PingPong

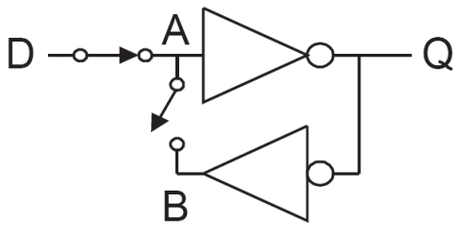
Metastability



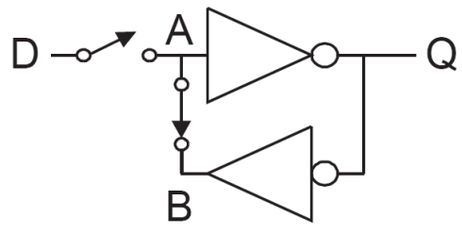
meta means “middle” or “in between”

Figure: Wiikmedia Commons. By Georg Wiora (Dr. Schorsch)

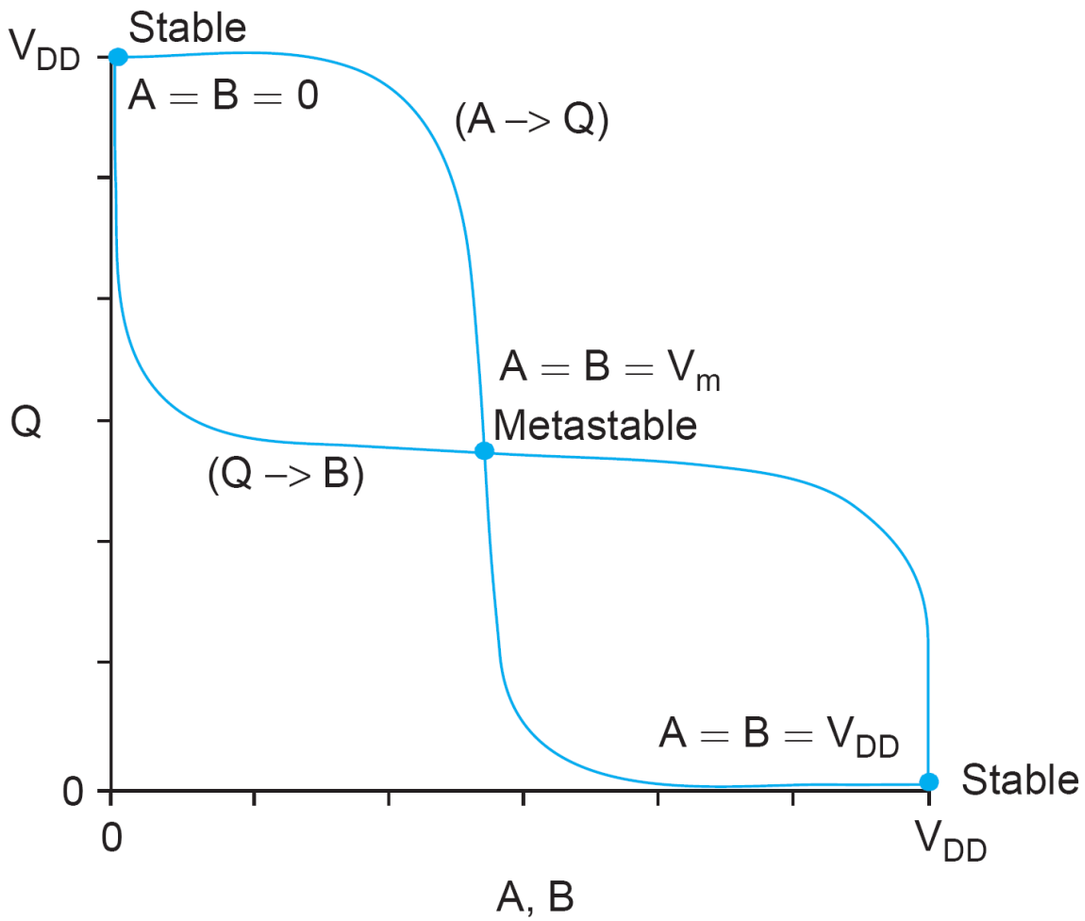
Metastability in latch



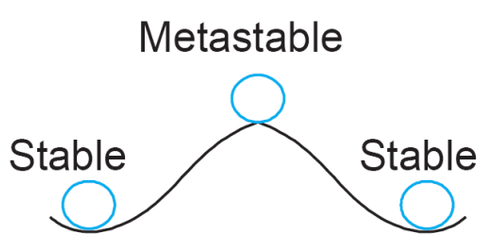
(a)



(b)



(c)



(d)

Figure:

Flip-flop = two latches

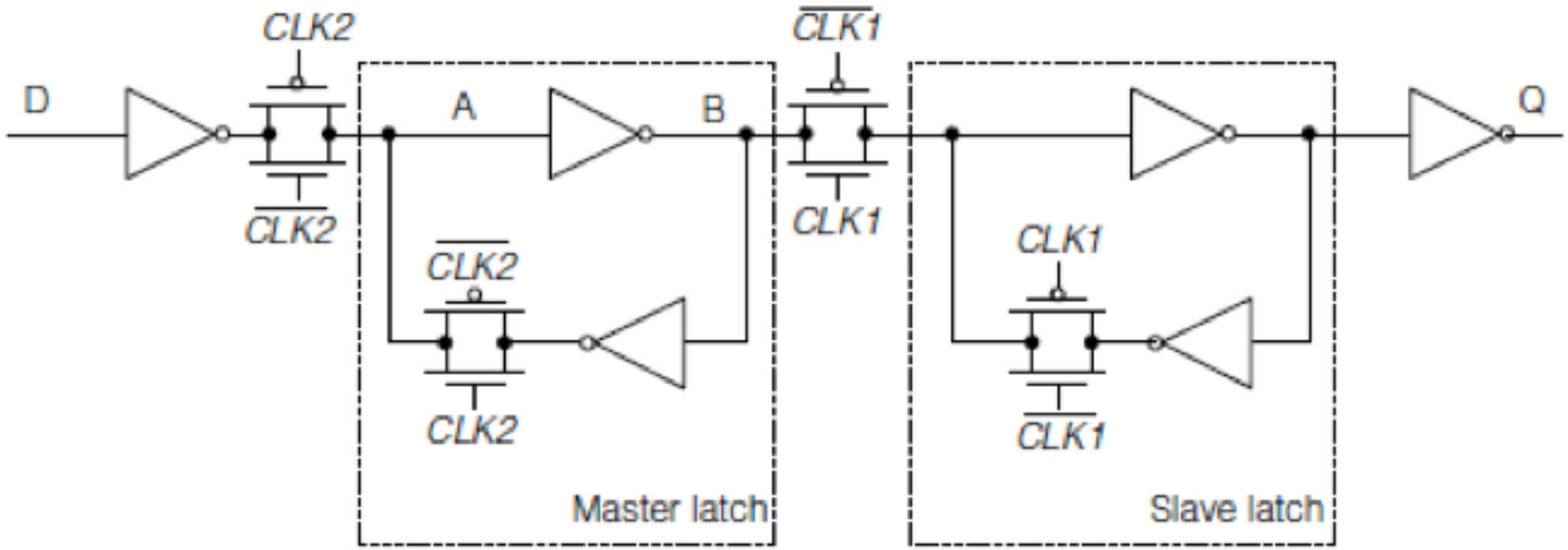
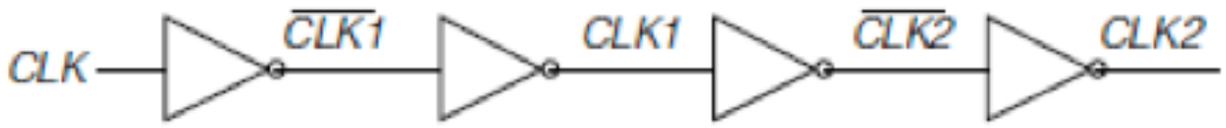


Figure 2(a)



Source: Ginosar 2011

Entering metastability

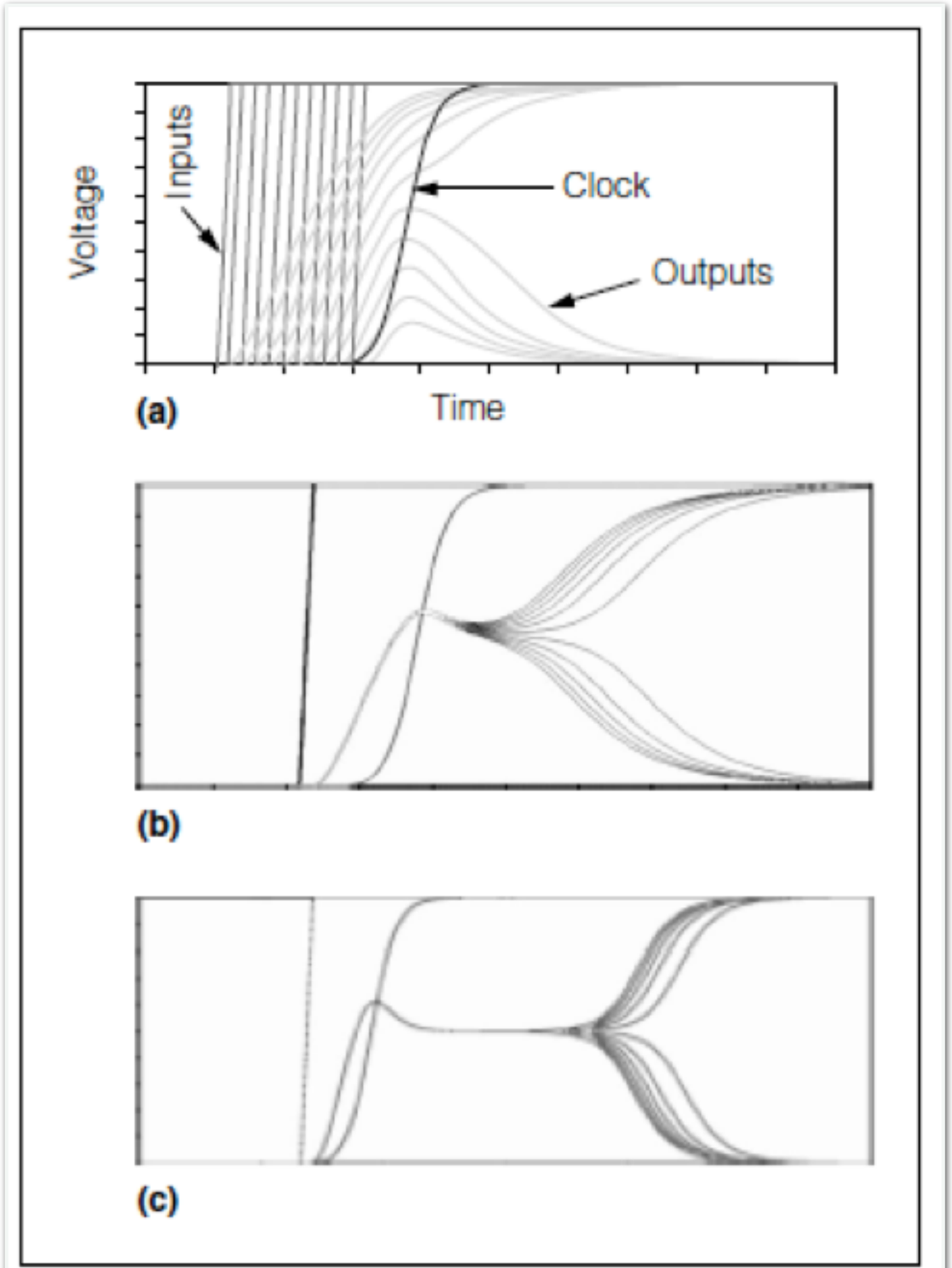


Figure 3. Empirical circuit simulations of entering metastability in the master latch of Figure 2 (a). Charts show multiple inputs D, internal clock (CLK2) and multiple corresponding outputs Q. The input edge is moved in steps of (a) 100 ps, (b) 1 ps, and (c) 0.1 fs.

Source: Ginosar 2011

Entering metastability

$$Rate = f_D T_W f_c$$

f_c = clock frequency

T_w = window of metastability

f_D = data rate at flip-flop input

Another way to express it: $Rate = f_D \frac{T_W}{T_c}$

An example

- f_c = 1 GHz
- T_W = 20 ps
- f_D = 100 MHz
- Rate for entering?

Exiting metastability

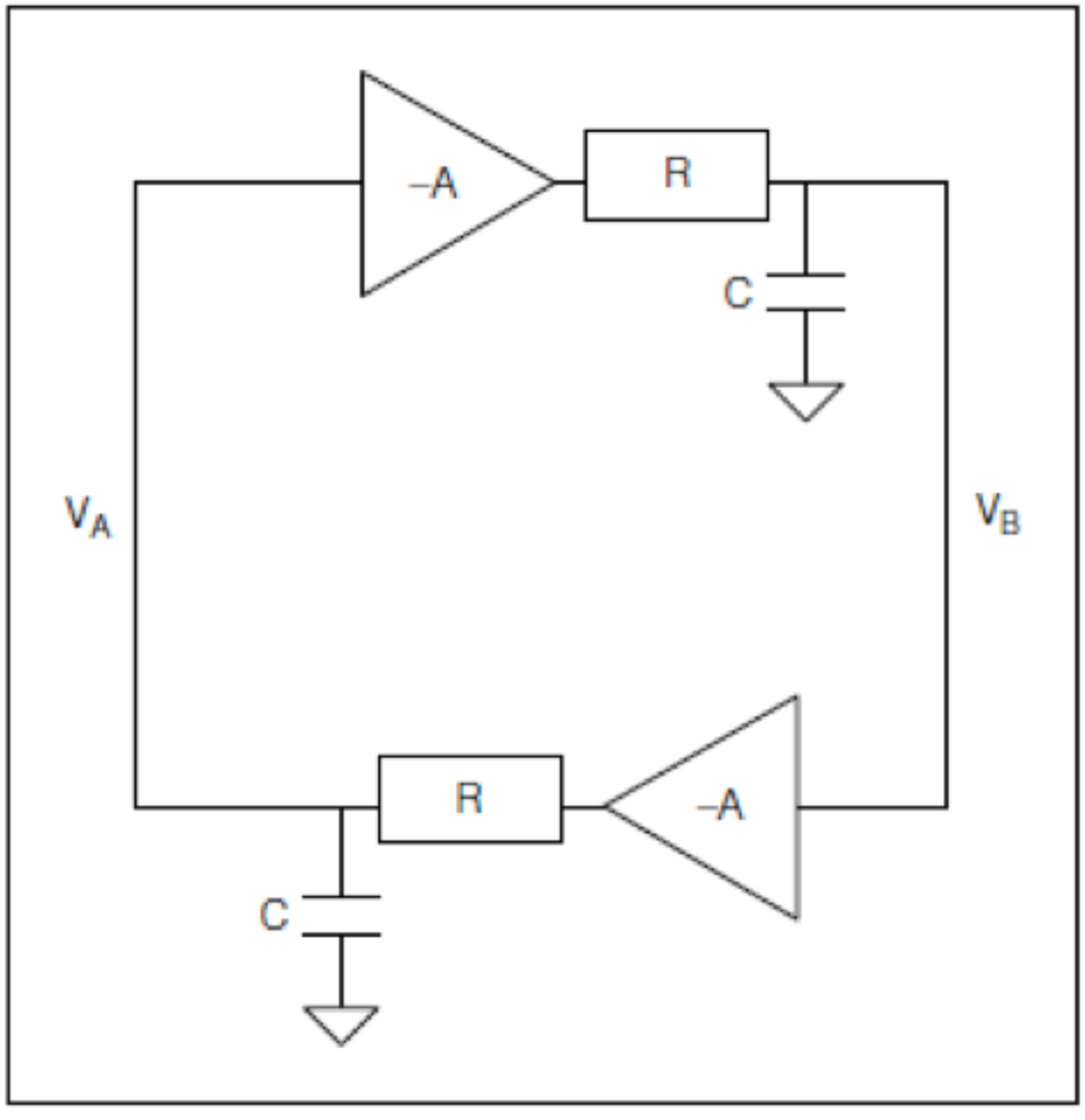


Figure 4. Analog model of a metastable latch; the inverters are modeled as negative amplifiers.
Small-signal model:,
-A is small-signal gain,
R is output resistance
and C is input capacitance of other inverter.

Source: Ginosar 2011

Virtuoso (R) Visualization & Analysis XL

File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help

cadence

Subwindows: 1 | Data Point 936470588m | family | Classic

lab1 inv-tb schematic

DC Response

Wed Sep 14 21:29:32 2016 1

Name | Vis

/net4
/net1
/gnd!
/vdd!

M6: 566.8597m 881.6961mV

M7: 626.9365m 364.8655mV

dx: 60.07674m
dy: 516.831mV
s: 8.602841V/

Recap from post lab 1

max gain is only around -8.5

Our X4 inverter has

small-signal gain, A = -8.5

V (V)

1.3 1.2 1.1 1.0 0.9 0.8 0.7 0.6 0.5 0.4 0.3 0.2 0.1 0.0 -0.1

440.0 460.0 480.0 500.0 520.0 540.0 560.0 580.0 600.0 620.0 640.0 660.0 680.0 700.0 720.0 740.0

VIN (m)

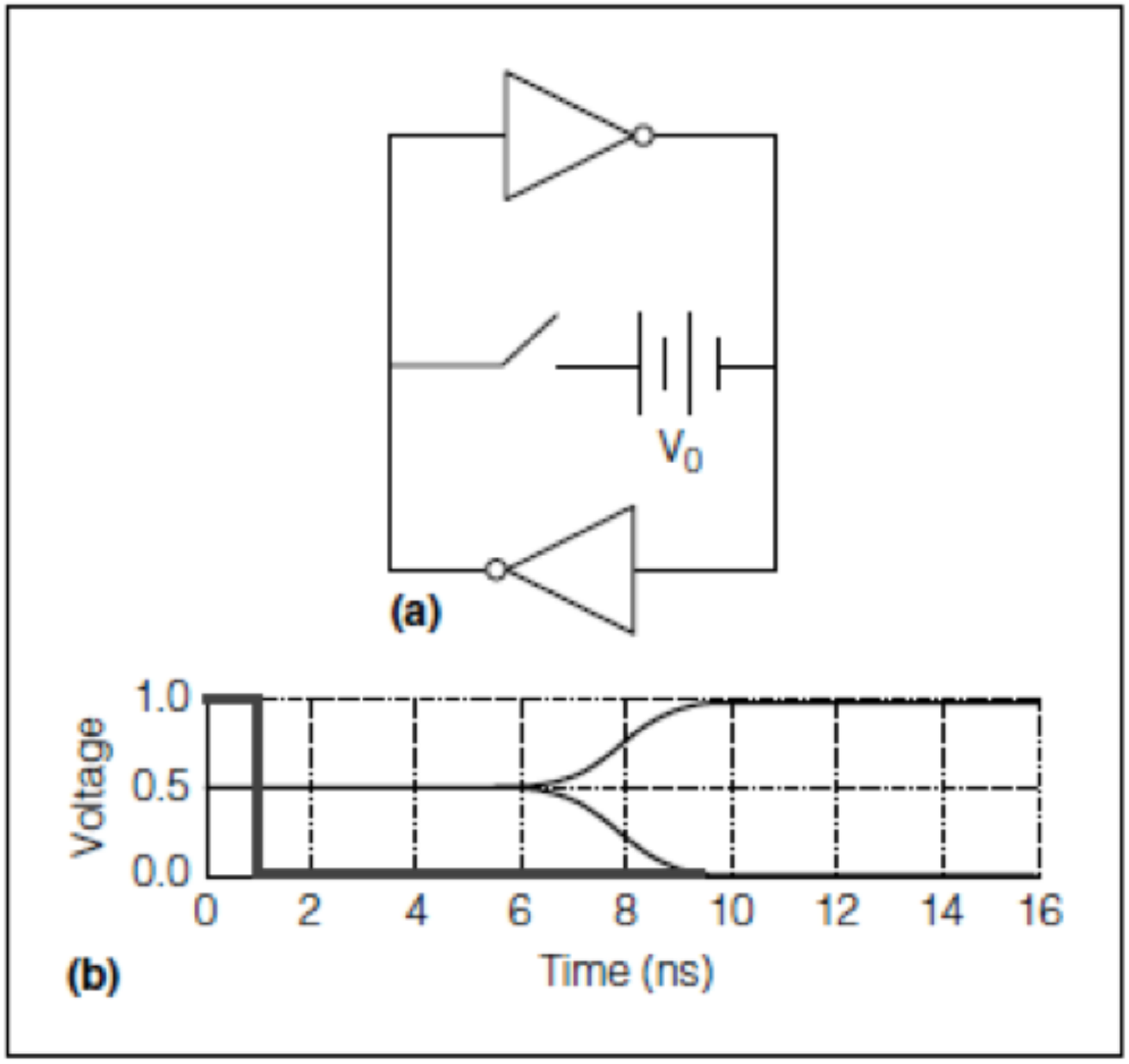
mouse L: M: R:

3(4) no error

Exiting

Figure 5. Simulation of exiting metastability: circuit (a) and voltage chart of the two latch nodes vs time (b).

The switch starts closed (applying V_0 = 1 µV) and then opens up (at t=1 ns) to allow latch to resolve.



Source: Ginosar 2011

Exiting metastbility

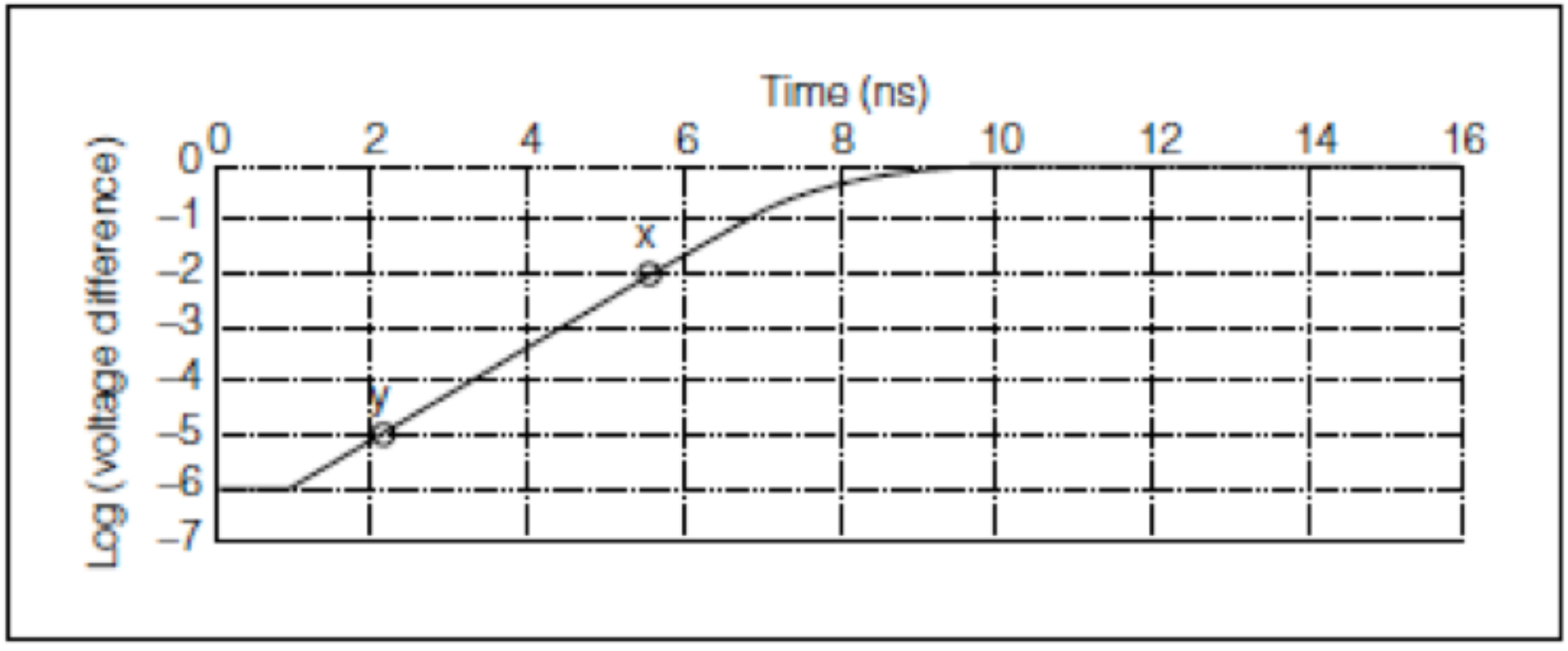


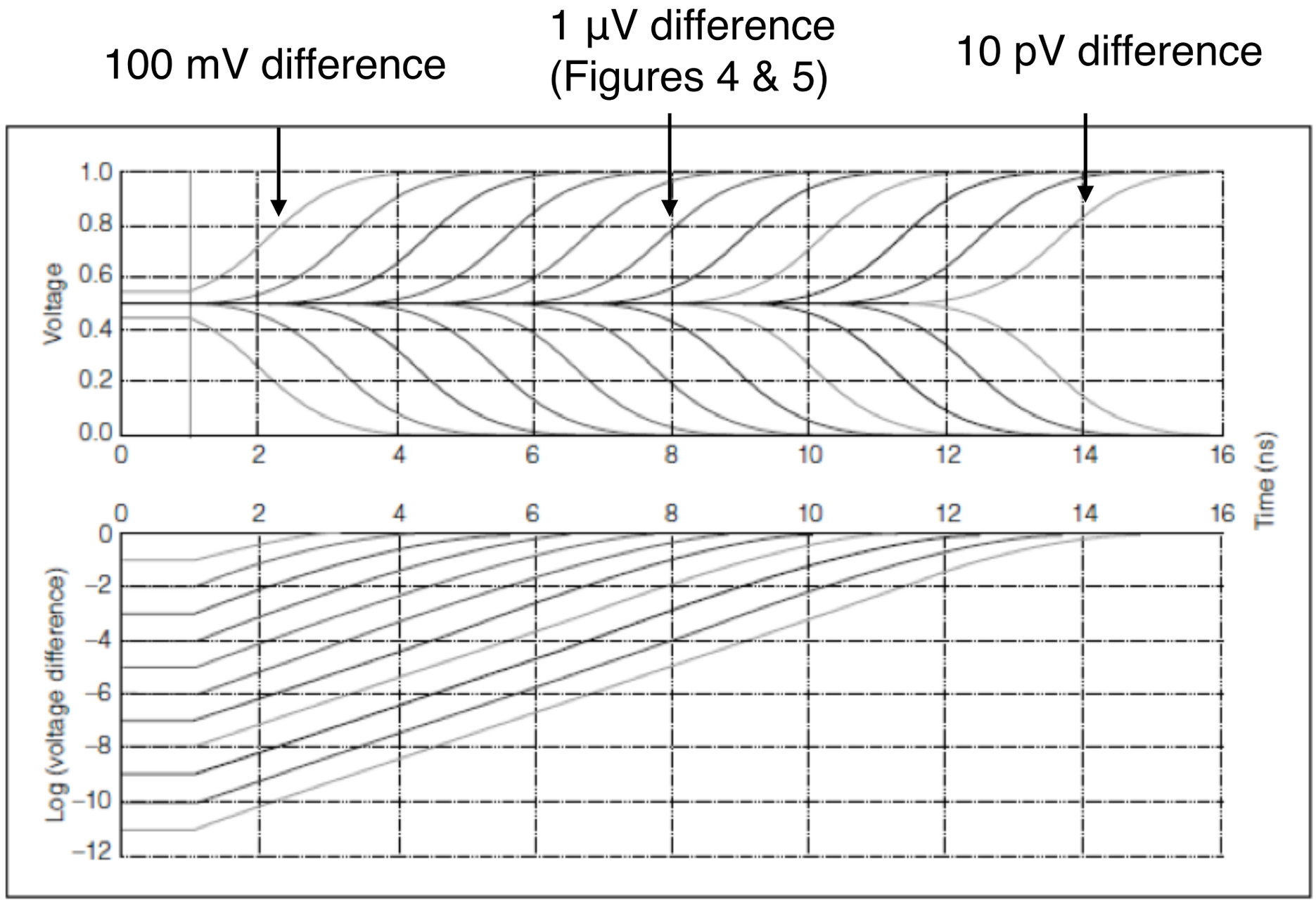
Figure 6. Log of the voltage difference of the two nodes of a resolving latch in Figure 5.

Points x and y can be used to determine time constant τ (assuming a straight line).

Source: Ginosar 2011

Exiting metastbility

Figure 7. Simulations of metastability resolution with the starting voltage difference varying from 100 mV (left) to 10 pV (right) in steps of factor 10; the lower the starting voltage difference the longer resolution takes.



Time to exit

$$V_1 = V_0 e \frac{t_m}{\tau}$$

$$t_m = \tau \ln \left(\frac{V_1}{V_0} \right)$$

V_0 starting voltage, V_1 ending voltgate,
t_m is time to exit metastability
τ depends on many things!
Often around 0.5 - 2 FO4 delays

Failure of synchronization

S is the allotted synchronization period
Probability of failure:

p(failure) = p(entering) x p(time to exit > S)

$$Rate(failures) = T_W f_D f_c e^{-\frac{S}{\tau}}$$

$$MTBF = \frac{e^{\frac{S}{\tau}}}{T_W f_c f_D}$$

Avoiding synchronization failure

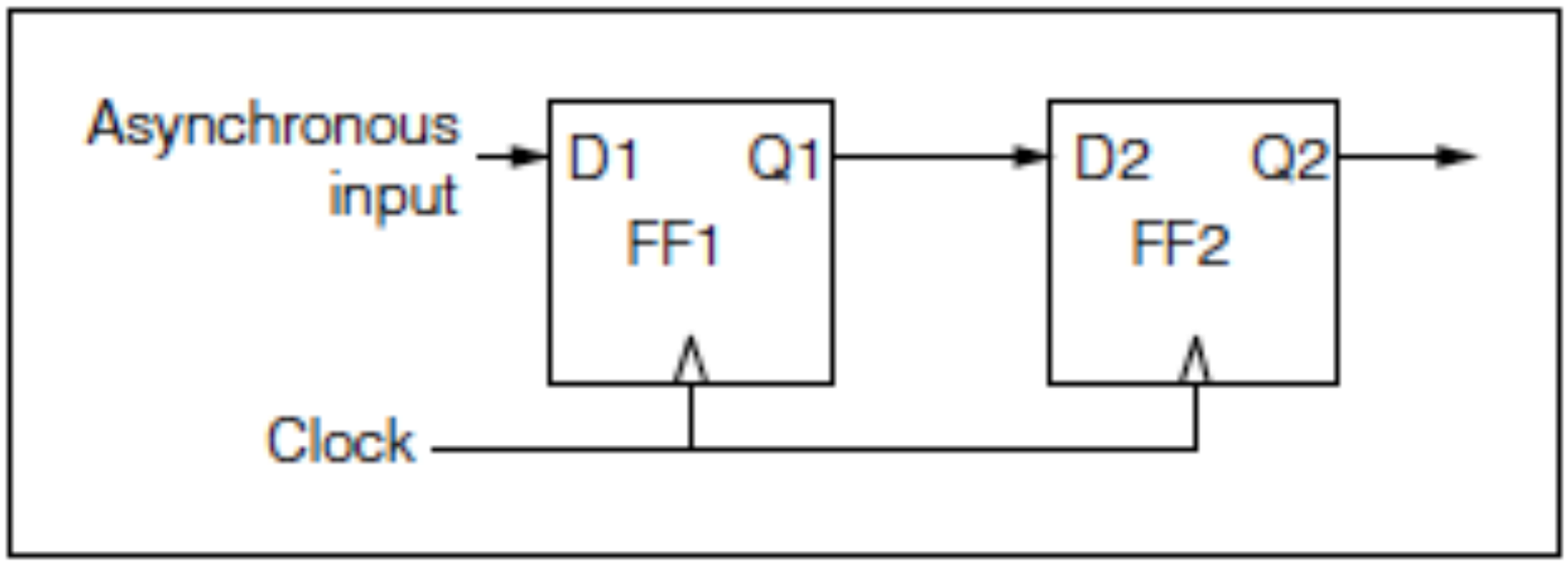


Figure 8. Two-flip-flop synchronization circuit.

6 cases

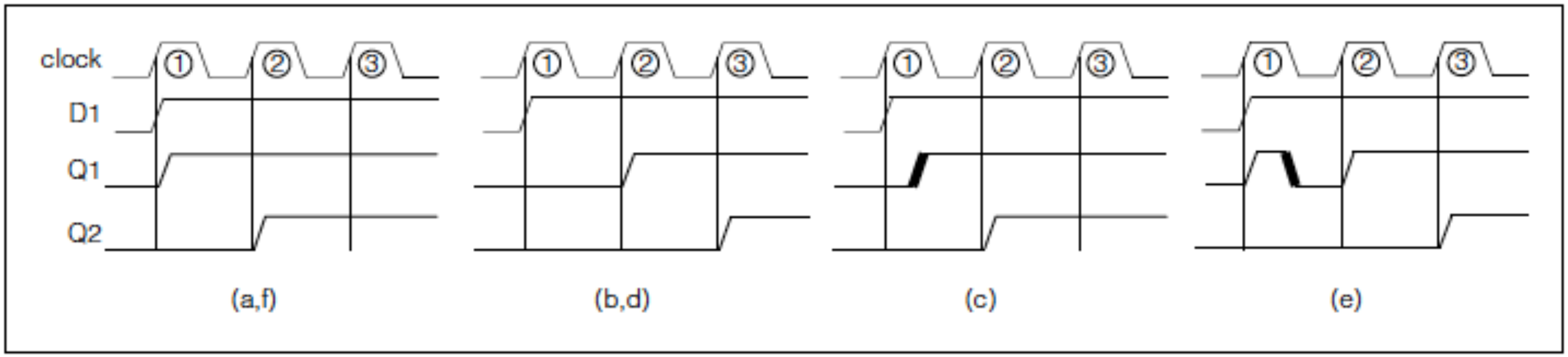


Figure 9. Alternative two-flip-flop synchronization waveforms.

Which are the 6 cases that can happen?

Many pitfalls

- Synchronizing the same signal more than once.
- Synchronizing buses
- Automated synchronizing solutions that do not work.
  - For example with dynamic latches

Metastability and synchronisation

- MTBF is figure of merit:
  - Probability to enter
    - Probability to exit
- Two FF synchronisers lower the MTBF
- Many pitfalls - be paranoid!