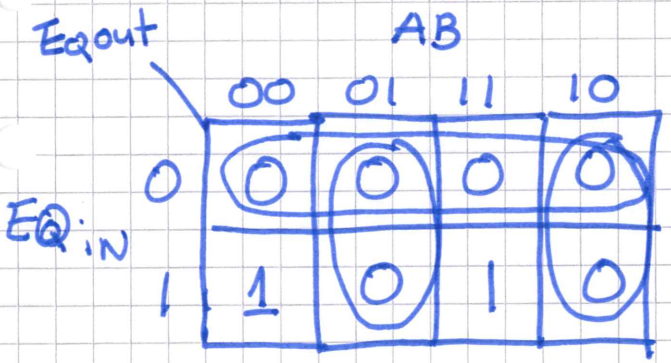
2017-09-11 Example of ILA design before prelab 2

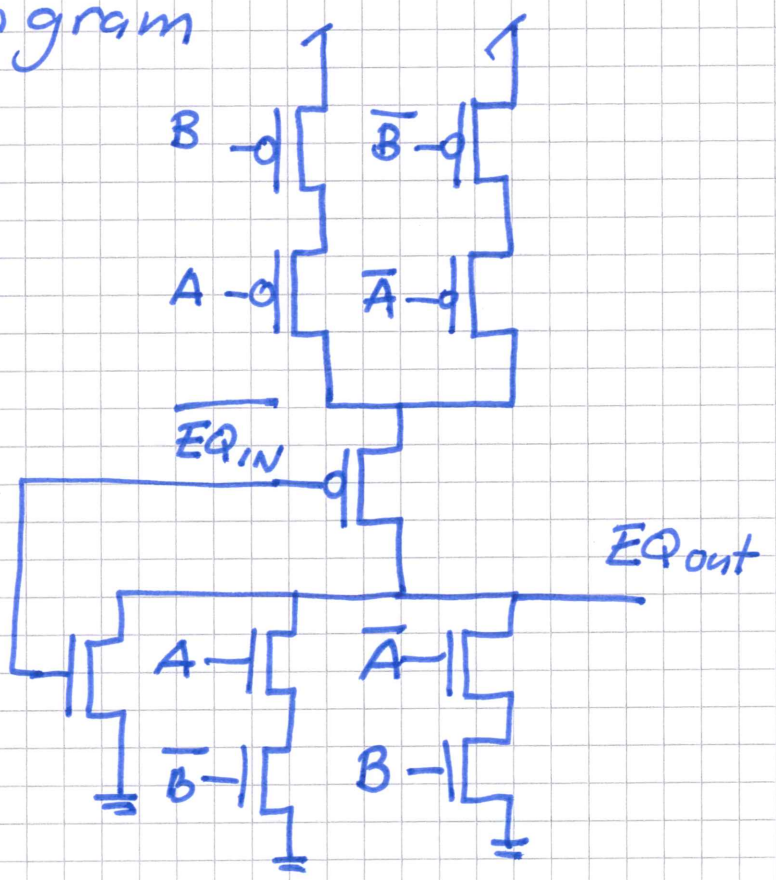
An equal circuit implemented as an iterative logic array (ILA)

A	B	EQin	EQout
0	0	0	0
0	1	0	0
1	0	0	0
1	1	0	0
0	0	1	1
0	1	1	0
1	0	1	0
1	1	1	1

Karnaugh diagram



We need an inverter to generate $\overline{EQ_{in}}$

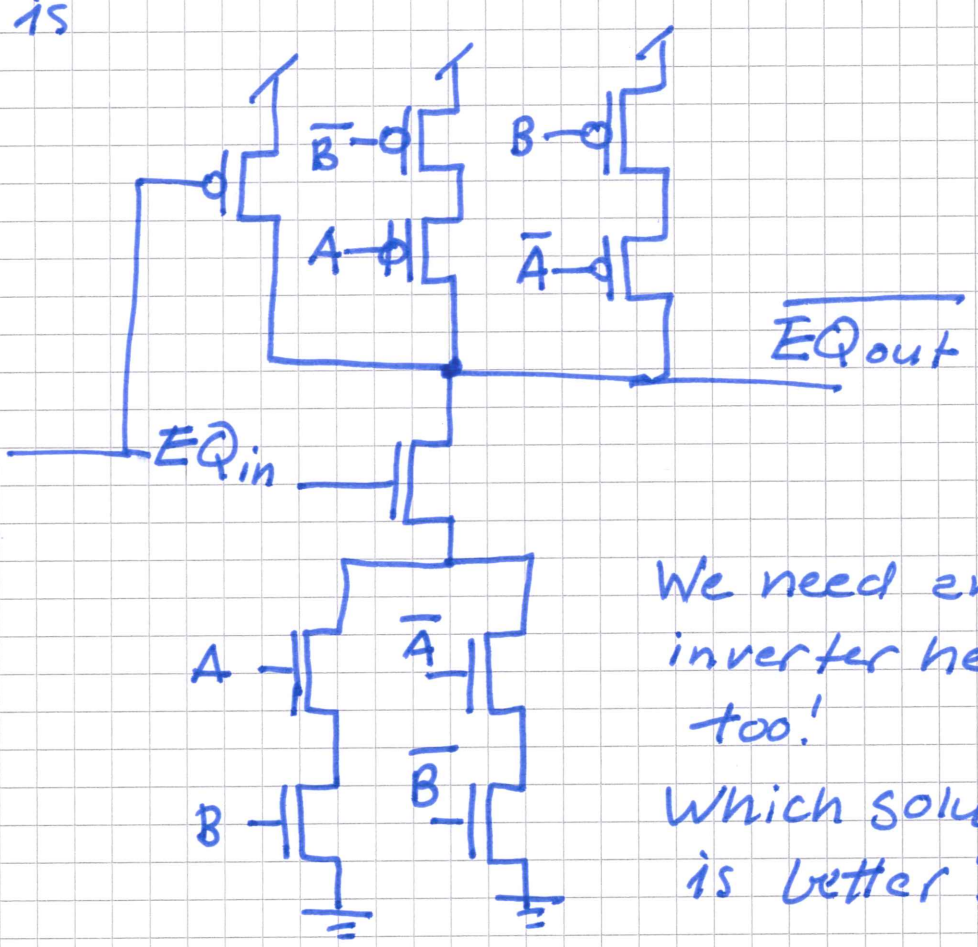


Note that we can also implement

$\overline{EQ_{out}}$

$\overline{EQ_{out}}$ / EQ_{IN}	AB = 00	AB = 01	AB = 11	AB = 10
0	1	1	1	1
1	0	1	0	1

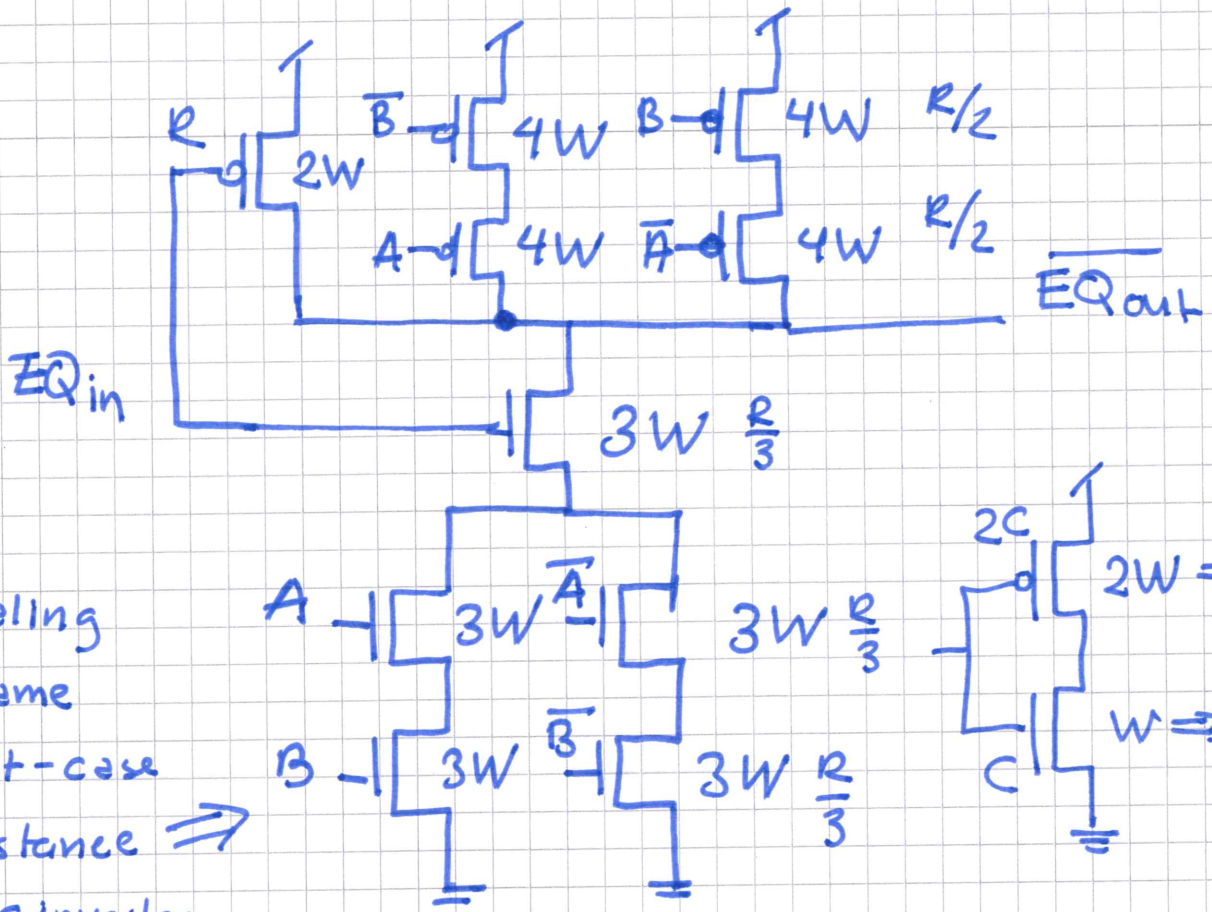
the corresponding circuit diagram is



We need an inverter here too!

Which solution is better?

The second solution is better due to fewer pMOS transistors in series



scaling for same worst-case resistance ⇒ as for inverter

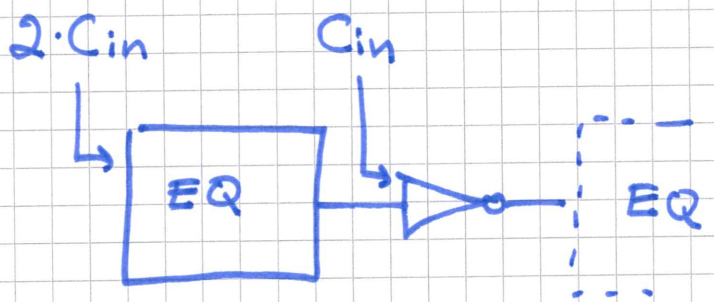
$$g_{EQ_{IN}} = \frac{2C+3C}{3C} = \frac{5}{3}$$

$$P_{EQ} = \frac{2C+4C+4C+3C}{3C} \cdot p_{INV} = \frac{13}{3}\, p_{inv}$$

for completeness

$$g_{A,B,\bar{A},\bar{B}} = \frac{4C+3C}{3C} = \frac{7}{3}$$

calculate delay with given scaling



$g = \frac{5}{3}$ $\quad$ $g = 1$

$p = \frac{13}{3} p_{inv}$ $\quad$ $p = p_{inv}$

$h = ? \frac{C_{in}}{2C_{in}} = \frac{1}{2}$ $\quad$ $h = ? \frac{2C_{in}}{C_{in}} = 2$

normalized delay $d = g \cdot h + p$

$$\frac{5}{3} \cdot \frac{1}{2} + \frac{13}{3} p_{inv} + 1 \cdot 2 + p_{inv} =$$

$$\frac{5}{6} + \frac{13}{3} p_{inv} + 2 + p_{inv}$$

$$= \boxed{2\frac{5}{6} + 5\frac{2}{3} p_{inv}}$$