## Task #1: The tools

**a)** A transient simulation is a simulation in the time-domain.
**b)** The transistor parameters use the SPICE naming conventions and are as follows[1]:

- vt0 : zero-bias threshold voltage [V]

- kp : transconductance [$\frac{A}{V^2}$]

- gamma : Bulk threshold parameter [$V^{\frac{1}{2}}$]

- lambda : Channel-length modulation [$V^{-1}$]

- phi : Surface inversion potential [V]

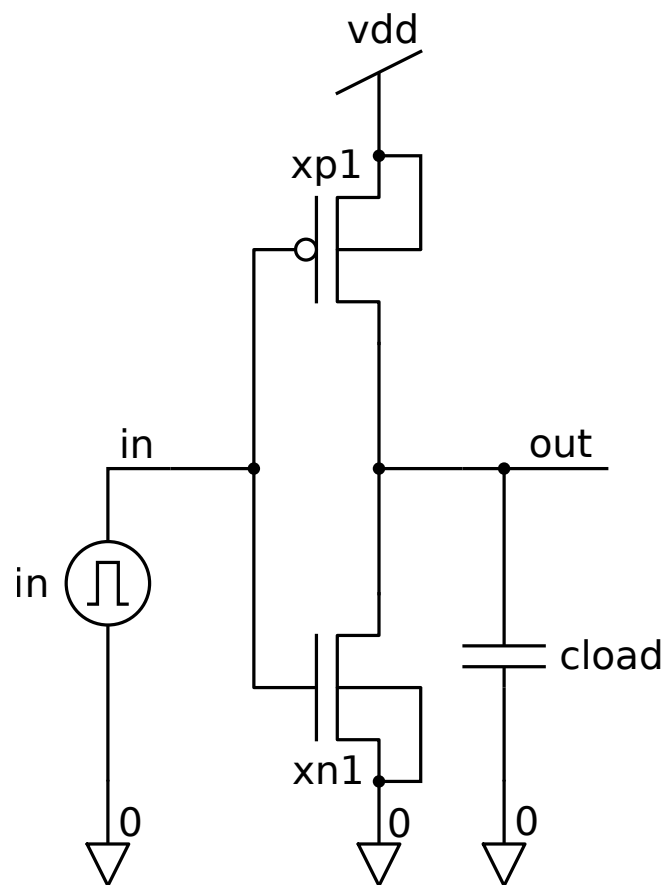**c)** Node 0 is GND (or 0V).
**d)**



Figure 1: Inverter schematic specified by Spectre netlist file. Instantiated components and nets labeled.

## Task #2: The lab

## Task #3: The Spectre netlist file

## Task #4: The capacitances of the H-tree

Ignoring (shorting) the resistances of the H-tree directly connects all the capacitances to the output node of the tapered buffer. The total capacitance is then simply the sum of the indivudual wire and leaf-inverter input capacitances.

Since none of the wire widths exceed $2\,\mu m$, the wire capacitance can be assumed to be $0.2\,fF/\mu m$.

$$C_{W1} = 10\,mm \cdot 0.2\,fF/\mu m = 2\,pF$$
$$C_{W2} = 7.07\,mm \cdot 0.2\,fF/\mu m = 1.414\,pF$$
$$C_{W2} = 5\,mm \cdot 0.2\,fF/\mu m = 1\,pF$$

The input capacitance of an X1 inverter was found in *lab 1* to be $0.36\,fF$, therefore the input capacitance of the scaled up inverter on the leaves is $1000 \cdot 0.36\,fF = 0.36\,pF$.

The total capacitance of the (zero-resistance) H-tree is

$$C_{\text{H-tree}} = 2C_{W1} + 4C_{W2} + 8C_{W3} + 8000 \cdot C_{\text{in,X1}} = 20.536\,pF$$

## Task #5: Design of the tapered buffer

If we let $C = C_{\text{in,X1}} = 0.36\,pF$ (ie. the input capacitance of an X1 inverter), and use it as a reference value, then the capacitive load of the H-tree can be *normalized* as $\frac{20.536\,pF}{0.36\,pF} = 57044C$.

Next, the various *path efforts* can be determined

- G = 1

- B = 1

- H $= \frac{57044C}{4C} = 14261$

This gives a *path effort* of $F = GBH = 14261$.

It can be shown that the *path delay* is at a minimum when all the *stage efforts* are equal and approximately 4. Thus the optimum number of stages is chosen to achieve this result as closely as possible.

$$\hat{N} = \log_4(F) = 6.9$$

At this point a value of either 6 or 7 could be chosen. Both will be evaluated here to determine which is more appropriate.

For $\hat{N} = 7$ the minimum *path delay* $D = \hat{N} \cdot \sqrt[\hat{N}]{F} + P = 7 \cdot \sqrt[7]{14261} + 7 = 34.5$ and the *stage effort* $\hat{f} = \sqrt[7]{14261} = 3.92$.

For $\hat{N} = 6$, however, the minimum *path delay* $D = 35.5$ and the *stage effort* $\hat{f} = 4.92$. The fact that the delay is insensitive to the number of stages means that accepting a marginal increases in delay (1ps, or 2.8%) allows an area reduction of 14% along with the associated power consumption!

Since this is arguably the superior implementation, it will be used going forward. Finally the absolute *path delay* is $t_{\text{pd}} = 35.5\tau = 177ps$, where $\tau = 5ps$. As a consequence of all the individual *path efforts* being equal, the delays between each stage are also equal ie. $d_i = g_i h_i + p_i = 5.92$ or 29.6ps in absolute terms.

## Task #6: The Resistances (and capacitances) of the H-tree

The resistance of a wire segment can be calculated from its *sheet resistance* and its physical dimensions

$$R_W = R_{\text{sh}} \frac{L}{W}$$

, note height (or thickness) is disregarded in this model.

The dimensions of the wires are known and $R_{\text{sh}}$ is assumed to be $0.01 \frac{\Omega}{\square}$. Thus, the resistance of the wires at each level can be calculated as

- $R_{W1} = 50\,\Omega$

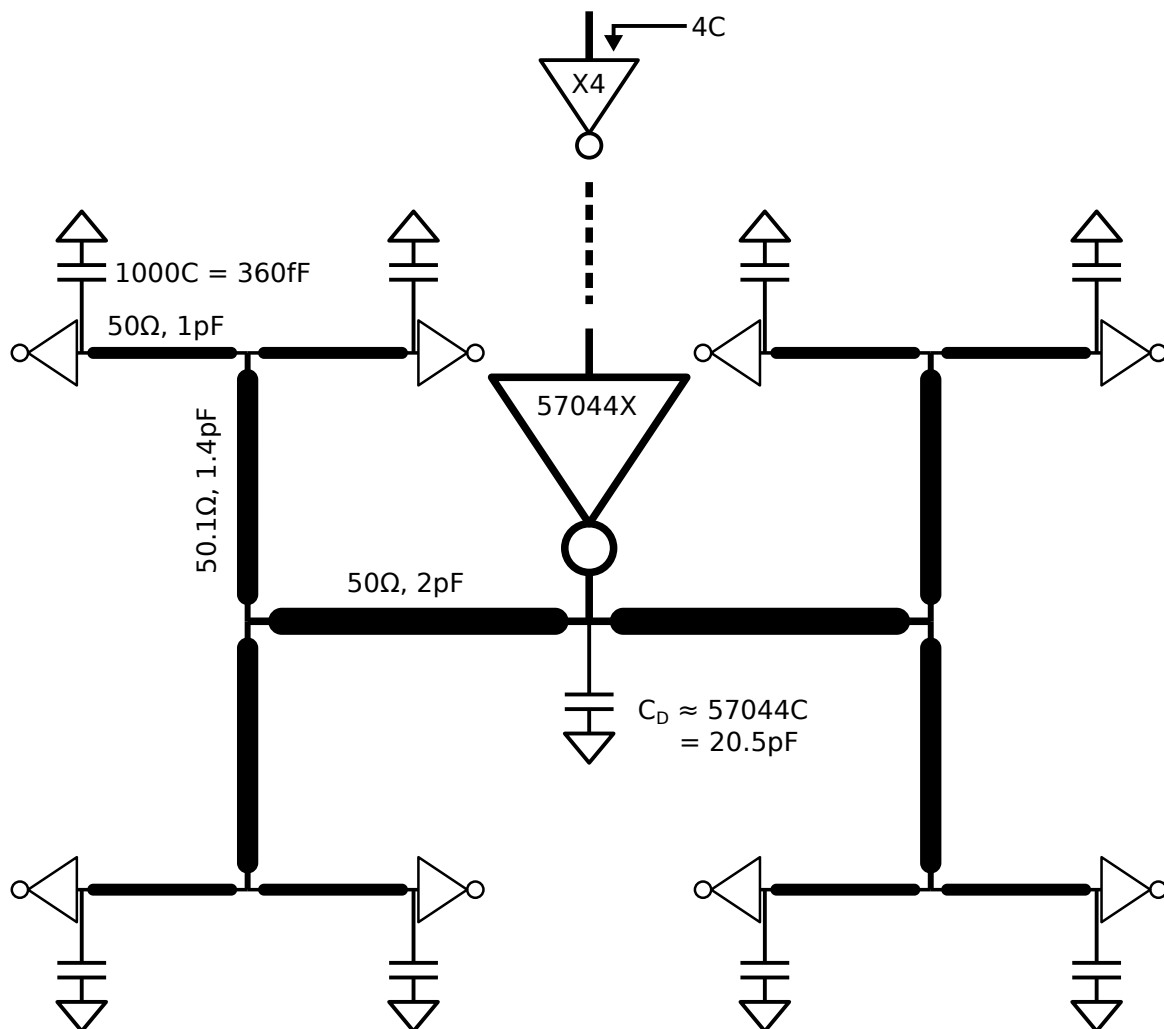- $R_{W2} = 50.1\,\Omega$

- $R_{W3} = 50\,\Omega$



Figure 2: H-tree with calculated resistances and capacitances.

# Task #7: Delay of the H-tree with capacitance and resistance when driven by the tapered buffer

The H-tree is fully symmetrical and when modeled as lumped components, parallellism becomes evident, allowing the tree to be "collapsed" into a single path with no branches. This results in the following schematic
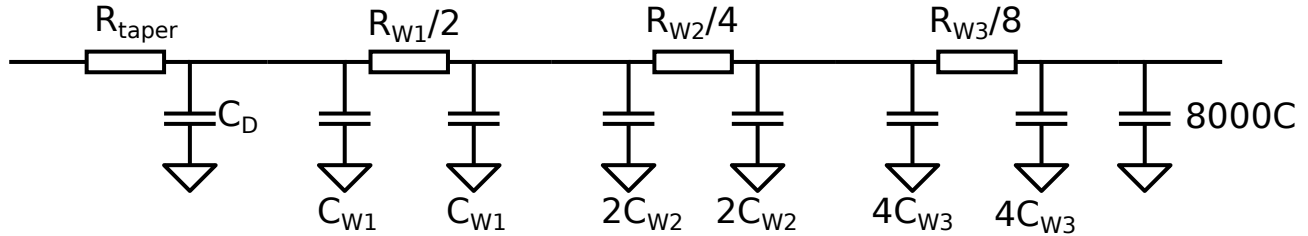


Figure 3: The "collapsed" H-tree, as a non-branching RC-chain.

The Elmore delay of this reduced H-tree is calculated in the following formula

$$
\begin{aligned}
T_E =& R_{\mathrm{rep}}(C_D + 8000C + 2C_{\mathrm{w1}} + 4C_{\mathrm{w2}} + 8C_{\mathrm{w3}}) + \\
& R_{\mathrm{w1}}/2(C_{\mathrm{w1}} + 4C_{\mathrm{w2}} + 8C_{\mathrm{w3}} + 8000C) + \\
& R_{\mathrm{w2}}/4(2C_{\mathrm{w2}} + 8C_{\mathrm{w3}} + 8000C) + \\
& R_{\mathrm{w3}}/8(4C_{\mathrm{w3}} + 8000C \\
=& 692.6ps
\end{aligned}
$$

After compensating for the behaviour of ramped signal inputs (scaling the delay by 0.7) the Elmore delay is 484.8ps.

## Task #8: Delay with inverters in the H tree driven by tapered buffer

The buffers inserted into the H-tree can be modeled as an effective resistance with an input and output capacitance. The output (diffusion) capacitance $C_D$ is assumed to be equal to the input capacitance $C_{in}$. The effective resistance of an X1 inverter was determined in *lab 1* to be $20\,\mathrm{k\Omega}$. Since the tree is still symmetrical it can again be collapsed into a single path. Since the inverters do not provide a direct electrical path between the input and the output, the path must be divided into segments with the Elmore delay calculated for each segment individually.
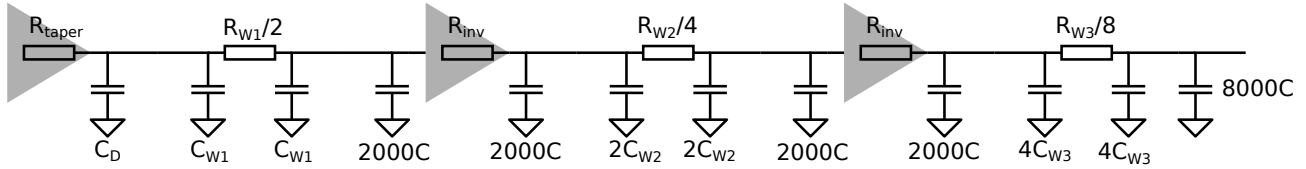


Figure 4: Collapsed H-tree with inserted buffers.

The uncompensated Elmore delay for each segment is thus (segments numbered left to right in fig 4)

$$T_{E_1} = R_{taper}(C_D + C_{w1} + C_{w1} + 2000C) + \frac{R_{w1}}{2}(C_{w1} + 2000C) = 76,8ps$$

$$T_{E_2} = R_{inv}(2000C + 2C_{w2} + 2C_{w2} + 2000C) + \frac{R_{w2}}{4}(2C_{w2} + 2000C) = 115,4ps$$

$$T_{E_3} = R_{inv}(2000C + 4C_{w3} + 4C_{w3} + 8000C) + \frac{R_{w3}}{8}(4C_{w3} + 8000C) = 159,0ps$$

, resulting in a total delay of 351.3ps. Once the results are compensated to take into account ramped input signals, the results are as follows

$$T_{E_1} = 53,8ps$$
$$T_{E_2} = 80,8ps$$
$$T_{E_3} = 111,3ps$$

, with a total of delay of 245,9ps.

# References

[1]   *M. MOSFET*. URL: http://ltwiki.org/LTspiceHelp/LTspiceHelp/M_MOSFET.htm.