Task #1: Getting to know Cadence

Task #2: CMOS inverter cell schematics

A CMOS inverter uses a pMOS pullup transistor and an nMOS pulldown transistor. The substrates of the pMOS and nMOS must be tied to V_{DD} and V_{SS} respectively in order to reverse-bias the internal p-n junctions.

The following schematic has been drawn in LTSpice using 4-terminal MOSFET components that allow the substrate (or *bulk*) to be connected freely. The substrate is represented by the middle port with an arrow indicating the internal p-n junctions.

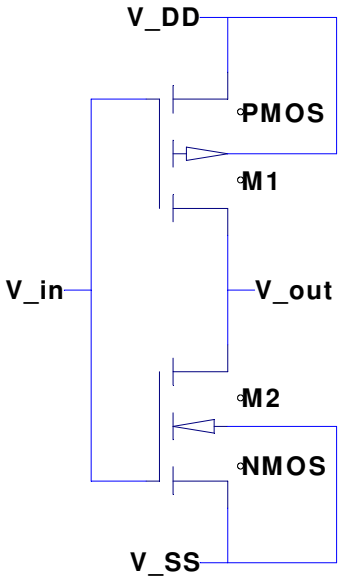

Figure 1: *CMOS Inverter drawn in LTSpice. V_{SS} is to be regarded as GND in this case.*

Task #3: FO4 inverter delay for the standard-cell X4 drive-strength inverter

Task parameters:

- 65nm process
- $I_{DS,N_{\text{sat}}}/\mu m = 600\,\mu\text{A}/\mu\text{m}$
- $I_{DS,P_{\text{sat}}}/\mu m = 300\,\mu\text{A}/\mu\text{m}$
- $C_{ox} = 20\,\text{fF}/\mu\text{m}^2$
- $V_{\text{DD}} = 1.2\,\text{V}$
- $L = 0.06\,\mu\text{m}$
- $W_{N_{\text{min}}} = 0.2\,\mu\text{m}$
- $W_{P_{\text{min}}} = 0.4\,\mu\text{m} = 2 \cdot W_{N_{\text{min}}}$
- X2 drive strength

Since the inverter is to have a drive strength of X4, the widths of both the nMOS and the pMOS should be doubled, giving $W_N = 0.4\,\mu\text{m}$ and $W_P = 0.8\,\mu\text{m}$.

The gate capacitance C_G can now be calculated

$$C_G = C_{GN} + C_{GP} = (W_N + W_P)LC_{ox} = 3W_N LC_{ox} = 1.44\,\text{fF}$$

, where $W_P = 2 \cdot W_N$.

Assuming that the drain capacitance C_D for each transistor type is $0.8C_G$

$$C_D = 0.8 \cdot 1.44\,\text{fF} = 1.15\,\text{fF}$$

In order to begin calculating the delay, we must now determine the saturation current for the transistors of drive-strength X4, set by their respective channel widths.

$$\begin{aligned} I_{DS,N_{\text{sat}}} &= I_{DS,N_{\text{sat}}}/\mu m \cdot W_N = 240\,\mu\text{A} \\ I_{DS,P_{\text{sat}}} &= I_{DS,P_{\text{sat}}}/\mu m \cdot W_P = 240\,\mu\text{A} \end{aligned}$$

We can now see that the scaling of the pMOS wrt. the nMOS has given them equivalent current driving capabilities.

The RC products can now be calculated for the rising and falling edge

$$\begin{aligned} t_{\text{pdr}} &= 0.7\frac{C_G \cdot V_{\text{DD}}}{I_{DS,P_{\text{sat}}}} = 5.04\,\text{ps} \\ t_{\text{pdf}} &= 0.7\frac{C_G \cdot V_{\text{DD}}}{I_{DS,N_{\text{sat}}}} = 5.04\,\text{ps} \\ t_{\text{pdr}} &= t_{\text{pdf}} = \tau \end{aligned}$$

, where the constant 0.7 is an empirically determined value that closely approximates the behaviour of a ramped signal edge (rather than an ideal step). Even here, the scaling of the pMOS has yielded identical values that can be consolidated as a single *time constant* τ.

The actual FO4 delay is thus

$$t_{\text{pdrFO4}} = t_{\text{pdfFO4}} = t_{\text{pd}} \cdot (p + h) = 5 \cdot 5.04\,\text{ps} = 25.2\,\text{ps}$$

, where p is a parasitic factor that can be assumed to be 1 if unknown and h is the *electrical effort*, a value that quantifies load in terms of driver strength. In this case h is equivalent to the fanout ie. 4.

Task #4: Static characterization of the CMOS inverter - expected values

Task parameters:

- 65nm process
- $V_{\mathrm{TN}} = 0.29\,\mathrm{V}$
- $V_{\mathrm{TP}} = -0.27\,\mathrm{V}$
- $V_{\mathrm{DD}} = 1.2\,\mathrm{V}$
- Assume $k_n = k_p$

Let $x = k_n/k_p = 1$ and $\Delta V = V_{\mathrm{DD}} + V_{\mathrm{TP}} - V_{\mathrm{TN}}$. The switching voltage can then be calculated with the following equation:

$$V_{\mathrm{sw}} = V_{\mathrm{TN}} + \frac{\Delta V}{1+\sqrt{x}} = 0.61\,\mathrm{V}$$

To calculate the noise margins we first have to compute the points on the VTC (and its inverse) at which $A_v = -1$ using the expressions provided in the assignment that are valid for $k_n = k_p$. These points lie on the boundaries between *valid* and *indeterminate* symbols.

$$\begin{aligned} V_{OH,\mathrm{min}} &= V_{\mathrm{DD}} - \frac{\Delta V}{8} = 1.12\,\mathrm{V} \\ V_{IL,\mathrm{max}} &= V_{\mathrm{sw}} - \frac{\Delta V}{8} = 0.53\,\mathrm{V} \\ V_{OL,\mathrm{max}} &= \frac{\Delta V}{8} = 0.08\,\mathrm{V} \\ V_{IH,\mathrm{min}} &= V_{\mathrm{sw}} + \frac{\Delta V}{8} = 0.69\,\mathrm{V} \end{aligned}$$

We can now compute the noise margins (in terms of V_{out}) using the following expressions

$$\begin{aligned} NM_H &= V_{OH,\mathrm{min}} - V_{IH,\mathrm{min}} = 0.43\,\mathrm{V} \\ NM_L &= V_{IL,\mathrm{max}} - V_{OL,\mathrm{max}} = 0.45\,\mathrm{V} \end{aligned}$$

Task #5: Static characterization of the CMOS inverter - finding the values from the VTC

The value for S_{sw} is clearly the input value with the greatest negative slope (seen highlighted in red in fig. 2). If the currents I_{DS} through each transistor are measured, V_{sw} can also be identified by the point at which they are equivalent. Likewise, the values for $V_{OH,\text{min}}$ and $V_{OL,\text{max}}$ can be directly obtained by taking the derivative of the VTC and finding the output values at which the derivative is -1. The corresponding input values at the same points give $V_{IL,\text{max}}$ and $V_{IH,\text{min}}$.

$V_{IL,\text{max}}$ and $V_{IH,\text{min}}$ can also be found by first taking the inverse of the VTC curve, plotting the derivative and finding the output values at which it is -1, the same method used to plot a "butterfly" diagram.

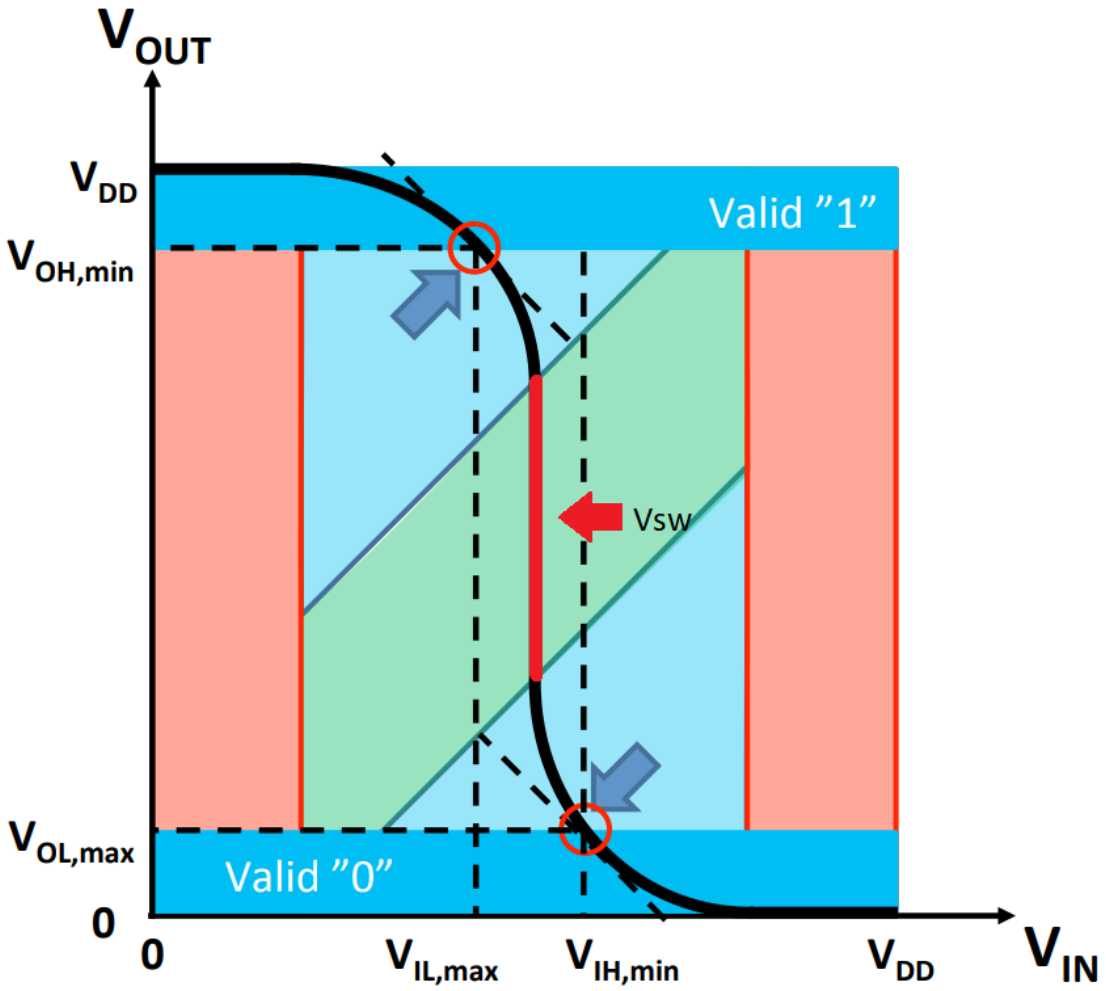

Figure 2: *CMOS inverter VTC. Switching voltage S_{sw} marked in red, V_{OH}, V_{IL}, V_{OL} and V_{IH} regions labeled.*