Prelab assignment
Lab 3

MCC092
Introduction to Integrated Circuit Design

Chalmers University of Technology

2018-07-06

2018

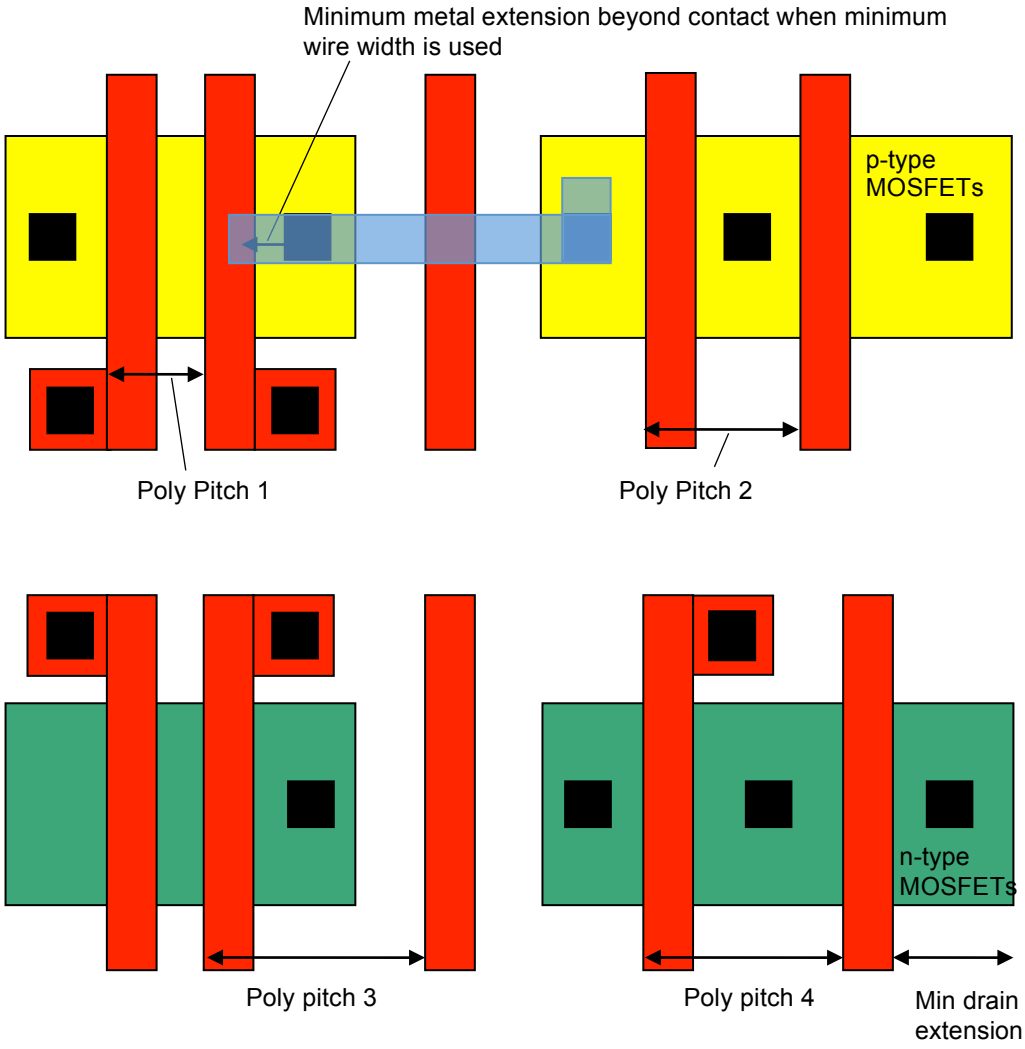
Pre-lab assignment #3 Due by Friday September 28 2018 at 1PM

Pre-lab assignment for the third lab exercise: layout of your ripple-carry cell: Design rule checking (DRC) and layout-vs-schematic (LVS) verification

In this pre-lab assignment you are expected to layout your ripple carry cell using the simplified standard-cell template provided below in Task #3. Through this exercise, you will also get acquainted with the basic geometric design rules for the 65-nm CMOS process as summarized in the appendix of this document.

Task #1 The tools Read through section 8 of the crib sheet on Layout and the information on the course web page under `Contents -> Labs -> On running DRC in Calibre` and `Contents -> Labs -> On running LVS in Calibre`. (This part of the instruction is likely moved for 2018).

Task #2 Pitches and distances Use the attached design rule sheet to determine the six minimum distances indicated with arrows in the figure below.



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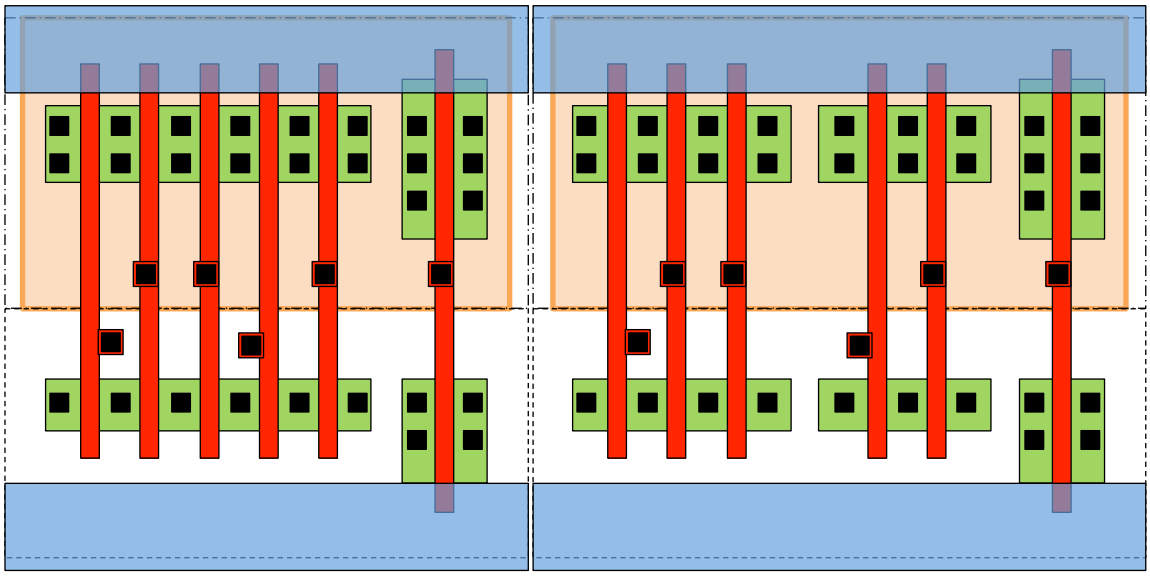
Task #3 Layout of ripple-carry cell

In this task you shall make a layout of your ripple-carry cell from lab 2. Two different layout templates are available with main measures according to the standard-cell layout constraints. That means that the cell height and the metal supply lines are fixed, and so are the n-well and n+/p+ select masks.

Since you are not training to become layout specialists, the layout task is simplified. The purpose of the exercise is to get some basic insight into physical CMOS design, and to run the appropriate EDA tools for design rule checking (DRC) and layout-versus-schematic (LVS). What is left to you is to complete the layout by drawing the metal-1 interconnect wires, and to connect the appropriate MOSFET sources to the VDD and VSS lines, respectively. This connection can be accomplished using either metal straps or diffused connectors.

Preliminary contact positions are indicated for every MOSFET source/drain and poly inputs. Source/drain contacts to active can be removed if not needed and if you need the space for metal wires. Poly contacts can be moved up or down. A and B input connections should be made with vias to the metal-2 layer. Note that only one A input and one B input is allowed to the cell. The output from the X4 inverter is to be connected to the next carry-in input by using metal 2, preferably organized to contact by abutment when cells are placed next to each other.

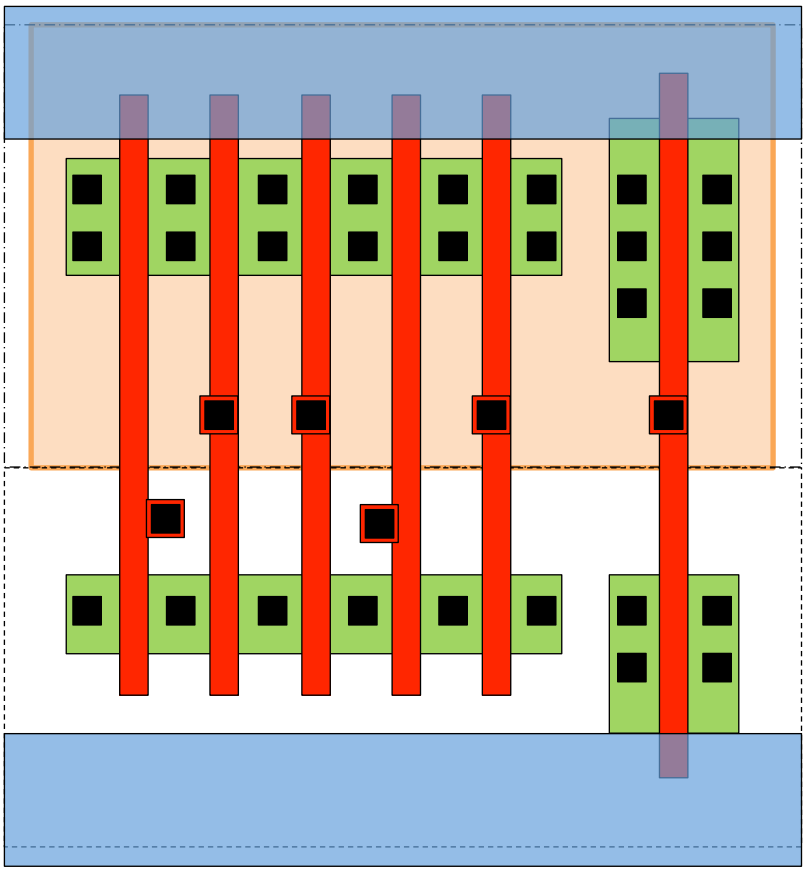


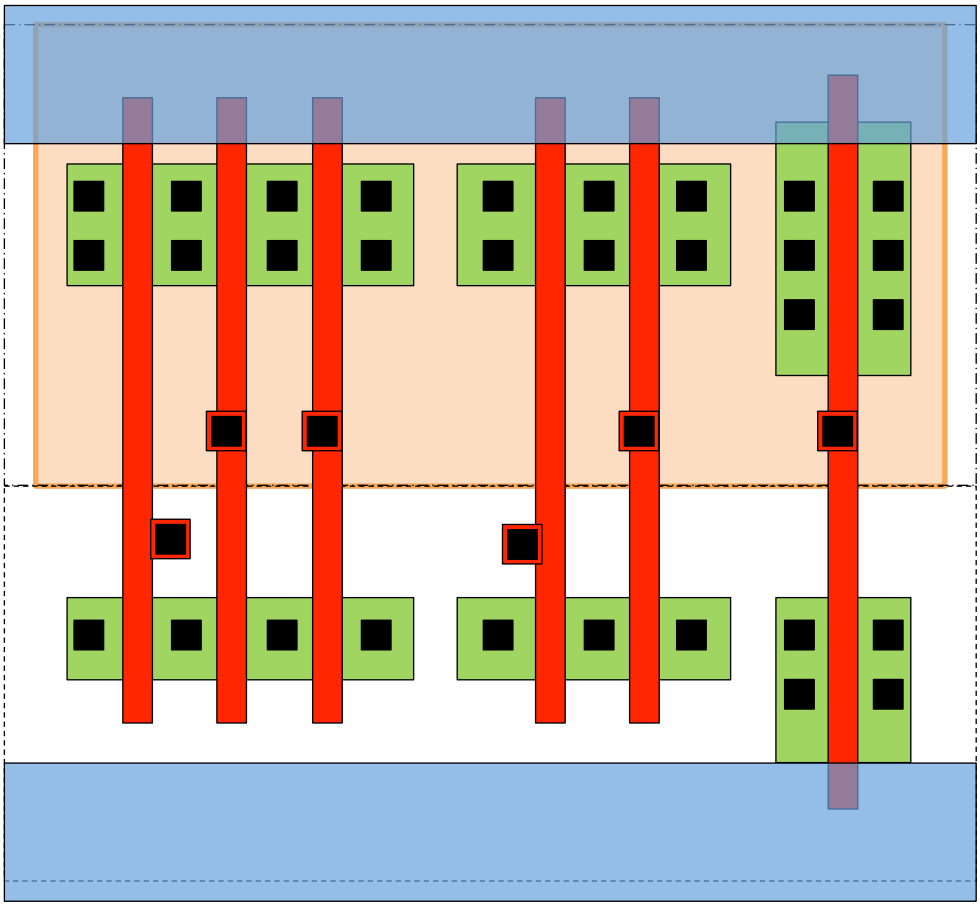
Reading suggestions: Weste and Harris: Integrated Circuit Design: section 3.3 Layout design rules, 3.5.1 Design Rule Checking (DRC), 3.5.2 Circuit Extraction, 3.8 Historical Perspective, layout examples on front and back inside color plates.

Task #4 Parasitic delay calculation The parasitic delay of a gate is due to the drain capacitance of the transistors connected to the gate output node. When we calculate the parasitic delay p from a gate schematic, as we did in prelab 2, we assume that each transistor contributes drain capacitance in proportion to its width. However, with smart layout the active areas can be shared between two transistors; then the total capacitance at the output node will be reduced. In this task, for simplicity, assume that the capacitance per µm width of the active area is the same regardless of whether the area is between two transistors or not. We can express the normalized parasitic delay in the form $p_{\text{ripple}} \times p_{\text{inv}}$. Find p_{ripple} for the ripple-carry gate in your layout from task 3.

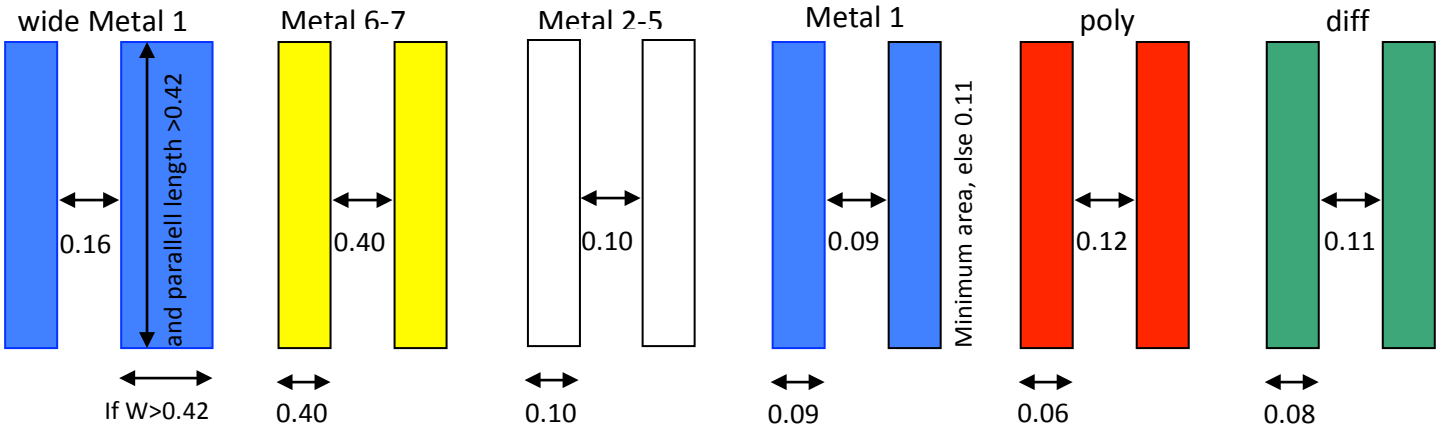
Prelab 3: Larger template that you can use for you convenience

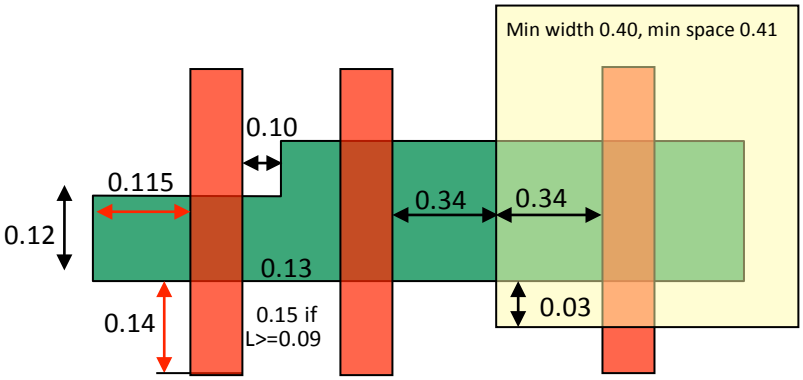
The layout templates are also available in other formats in PingPong.

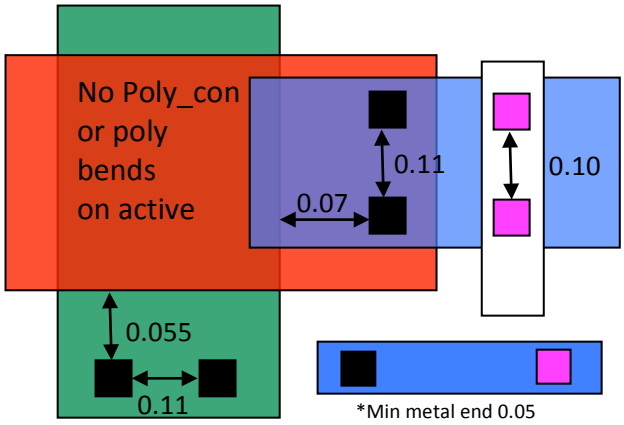




Geometric design rules for 65 nm CMOS

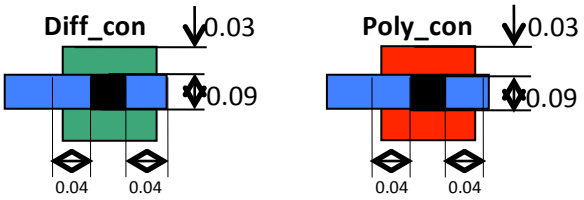




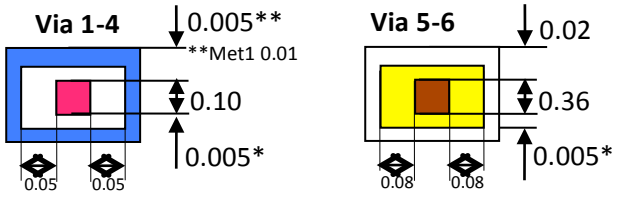


Contact & via rules

All contact and via sizes are exact measures

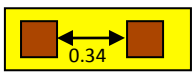


For minimum width metal lines at least 0.04 enclosure is required on two opposite sides (bottom measures).

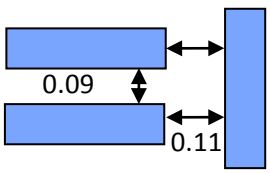


At least two 0.05 metal ends on metal pad

At least two 0.08 metal ends on metal pad



(min 0.54 in array)



Standard cell template

with rails, well, pplus and nplus design rules