Prelab assignment
Lab 2

MCC092
Introduction to Integrated Circuit Design

Chalmers University of Technology

2018-07-06

2018

Pre-lab assignment #2: To be handed in Friday September 21 2018 at 1PM

Preparations for Lab 2 Schematic entry and circuit simulation

Pre-lab assignment to the second lab exercise: designing a ripple-carry cell: schematic entry and circuit simulation

In this pre-lab assignment your task is to design a ripple-carry cell at the transistor level, which will fit in the standard-cell library of the 65 nm process. Your hand-in solution shall contain the structural description of one compound CMOS logic gate designed at the transistor level for this purpose. To fit in the cell library your gate should use the transistor widths that are used in an X2 inverter in the process[1]; if necessary you can use the X4 inverter you designed in lab 1 at the output of the compound gate, to generate the correct sign of the output signal.

During the lab session you will use the Cadence schematic entry tool and the Spectre circuit simulator to verify the logical function of the cell and to determine its worst-case propagation delay and the worst-case propagation delay of an 8-bit ripple-carry circuit.

The ripple-carry cell that we are asking for shall contain the necessary logic for computing the carry-out signal from two bits (one bit from word A and one bit from word B) and the carry-in signal, which is the carry-out signal from the previous ripple-carry cell. You may assume that both the bit signals, a_n and b_n, and their inverses, a_n' and b_n', are available as inputs to your cell. The carry output of your cell should be such that it can be used as the input signal for the next one.

Note that in this lab you will *not* include the logic to generate the sum of a_n and b_n. The reason for this choice is that it would make the layout that you will do in lab 3 too complex.

Reading suggestions:

Weste & Harris, Integrated Circuit Design, chapter 1, especially section 1.4.5. For delay estimations see Weste and Harris chapter 4 Delay sections 4.3 and 4.4 and lecture slides.

You solution to this task should contain:

- Short introduction stating problem to be solved.
- Boolean truth table for the one-bit ripple-carry cell.
- Transistor schematic for the one-bit ripple-carry cell.
- Logical effort for the c_{in} input of the compound gate (see Weste & Harris section 4.4 and lecture notes).
- Worst-case propagation delay through an 8-bit ripple-carry circuit made up of eight ripple-carry cells.
- Summary with transistor count.

[1] You can refer back to prelab 1 for more information about the inverter sizing in the 65 nm process .