Home assignment 3

MCC092
Introduction to
Integrated Circuit Design

Chalmers University of Technology

2017-10-09
Revised 2017-10-12 & 16
Power, adders &
what-if problems

Home assignment #3 Due Monday October 16 2017 @ 23.59 (midnight)

Section A Power and scaling

Task # 1 Power & scaling

This task concerns the famous (or infamous) DEC Alpha 21064 chip from 1992. It was designed in a 0.75 µm process and had a V_{DD} of 3.3 V. It is impossible to find any data for the CMOS process the Alpha processor was designed in, but you have some data for a 0.35 µm process, which also used a supply voltage of 3.3 V. In the 0.35 µm process you know that KPn = 110 µA/V^2 for 1 µm wide nMOS transistors and that they had a threshold voltage, V_{Tn}, of 0.5 V and that the gate capacitance, C_{ox} was 4.60 fF/µm^2.

In this problem assume that the square-law current equation holds for the MOS transistors in all CMOS processes and that a pMOS transistors of the same width has half the current of an NMOS transistor and that all transistors have a parasitic capacitance equal to its input capacitances.

a) How much power was dissipated in the Alpha chip if its effective switching capacitive load was 12.5 nF and the clock was running at 200 MHz? How much (in per cent) of this power was dissipated just to run the clock grid if the clock grid capacitance was 3.25 nF? For simplicity assume that the activity factor α is equal to 1.
b) Estimate the FO4 delay in the 0.35 µm process.
c) From your result in a) estimate the FO4 delay in the 0.75 µm process. How many FO4 delays in the logic, does the clock period of the 200 MHz clock signal correspond to?
d) If we assume that all the power dissipation in the Alpha processor was due to dynamic power dissipation, what would its power dissipation have been in the 0.35 µm process?
e) If you apply the Dennard scaling theory to the 0.35 µm FO4 delay you computed in b) what value for the FO4 delay do you compute for a 65 nm process such as the one we use in class? Does you result match the FO4 delay we have seen in this course class, in lab 1 for example? If not, why may that be?

Task # 2 Activity factor

The probability P_Y that the output of some basic 2- and 3-input logic gates is "1" is shown in Table 5.1 in Weste and Harris (repeated below). What if we needed also the probabilities that the outputs of the AOI21 and OAI21 gates are "ones", how could we calculate them? What would the resulting values be if we assume $P_A = P_B = P_C = 0.5$?

TABLE 5.1 Switching probabilities

Gate	P_Y
AND2	$P_A P_B$
AND3	$P_A P_B P_C$
OR2	$1 - \overline{P}_A \overline{P}_B$
NAND2	$1 - P_A P_B$
NOR2	$\overline{P}_A \overline{P}_B$
XOR2	$P_A \overline{P}_B + \overline{P}_A P_B$

Task # 3 Power gating

In Figure 5.24 in Weste & Harris (repeated below in Figure 1) a pMOS header switch for power gating is seen. Such a switch is used to turn off the static power consumption when a block is not in use. The header switch should be designed such that it does not cause too large an increase in the delay when the gated block is operating. Suppose the pMOS transistor has an ON resistance of 2.5 kΩ·µm and the block being gated has an equivalent ON current of 100 mA. V_{DD} is 1.2 V for our process as ususal.

a) How wide must the header transistor be to cause less than a 2% increase in the delay of the block when it is ON?
b) Assuming the pMOS gate capacitance is the same as in our 65 nm process what is the gate capacitance for the header switch?
c) How much energy is required to use the header switch once (that is, turn it on and off once)?

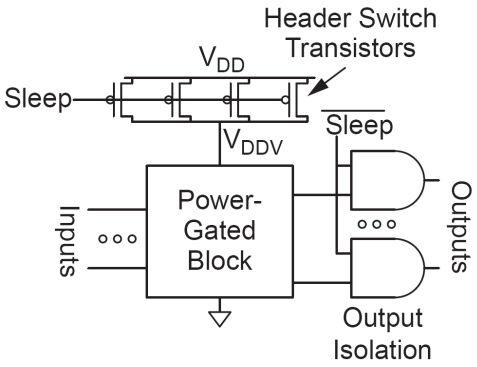

Figure 1. A power-gating arrangement with a pMOS header switch.

Section B Prefix adders

Task #4

The fundamental insight behind the prefix adders is that the logical functions for block generate and block propagate can be performed for smaller blocks and then combined to form all the necessary block generate and propagate signals. In this task you are to investigate this feature further. See Figure 2 of a prefix adder, which is not one of the usual ones.

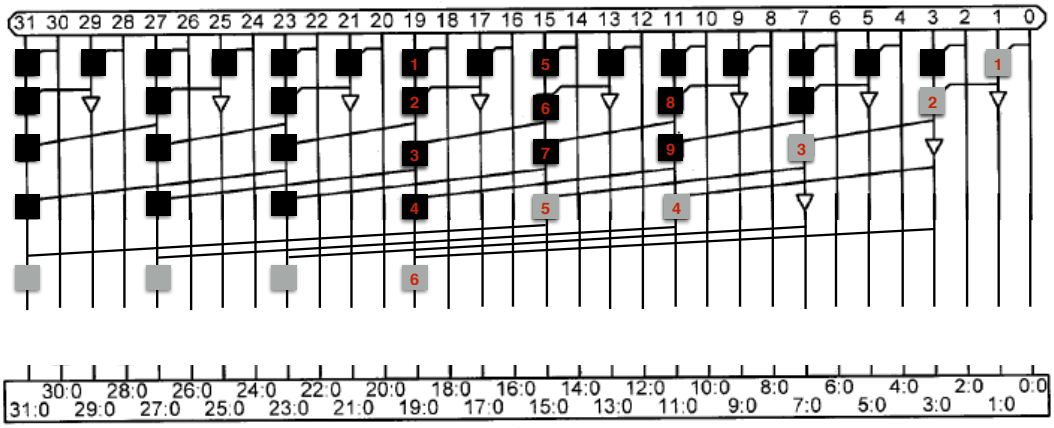

Figure 2. The PG-tree part of an unknown prefix adder. Part of the tree is missing. This drawing has been updated 2017-10-16 due to an error in Harris' approved patent.

a) Write down the spans for the nine black and six grey PG cells that are numbered in Figure 1. As an example for the black cell, which is above grey cell number 2, the span is 3:2. See also Figure 11.29 in Weste & Harris (this chapter can be downloaded from the CMOS VLSI web site).

b) What is the function to form one of the sums (study section 11.2.2.2 in the Weste & Harris if you are not sure).

c) If we assume just straight lines in the white space at the bottom of the tree in Figure 1, which of the 32 sums cannot be formed from the tree as shown in Figure 1?

d) Complete the adder schematics below with grey cells so that all sums can be formed. Any schematic that creates all the necessary signals is considered correct. Draw your solution in the attached bigger schematic.

e) If we (incorrectly) assume that all black and grey PG cell have the same propagation delay (which we call 1 unit delay), which sum(s) will be done last with your solution from task d)? List ALL sums that have this propagation delay. How many PG cells do these longest (critical) paths contain? Ignore the buffers (triangles) shown Figure 1 when you find these paths. It may be helpful to draw the paths in attached schematic and submit it with your solution.

Section C What-if problems for earlier topics

Task #5 CMOS voltage transfer curves

What if we connect the two inputs of an NAND2 gate, which has its n-net and p-net properly scaled for the same resistance, to use it as an inverter. If we sweep the input voltage to obtain the VTC, what switching voltage, V_{sw}, would we find?

Task #6 Tapered buffer

What if we were to optimize the tapering factors of a four-stage buffer driving a large capacitive load, see Figure 3. How can we **prove** that all tapering factors should be chosen equal, and more specifically equal to $\sqrt[4]{X}$?

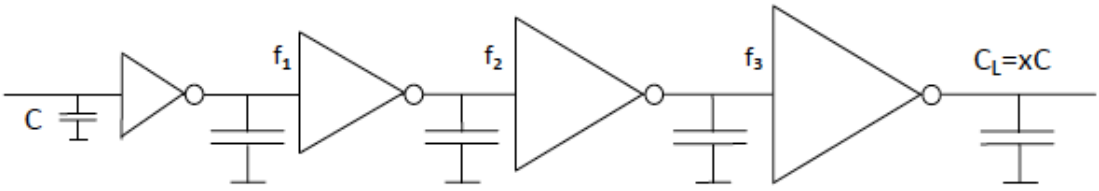

Figure 3. A tapered buffer with four inverters.

Task #7 Layout of standard cells

What if we wanted to layout our own AO22 standard cell, what would the layout look like if we are only allowed to use metal-1 in the cell? Which of the two templates in Figure 4 is preferable? (Unnecessary contacts can be removed of course). With your layout, should you modify the value for

the parasitic delay, *p*, that you have previously computed from the **schematic** of the AOI22 gate, or not? If so, what is the new value for *p*?

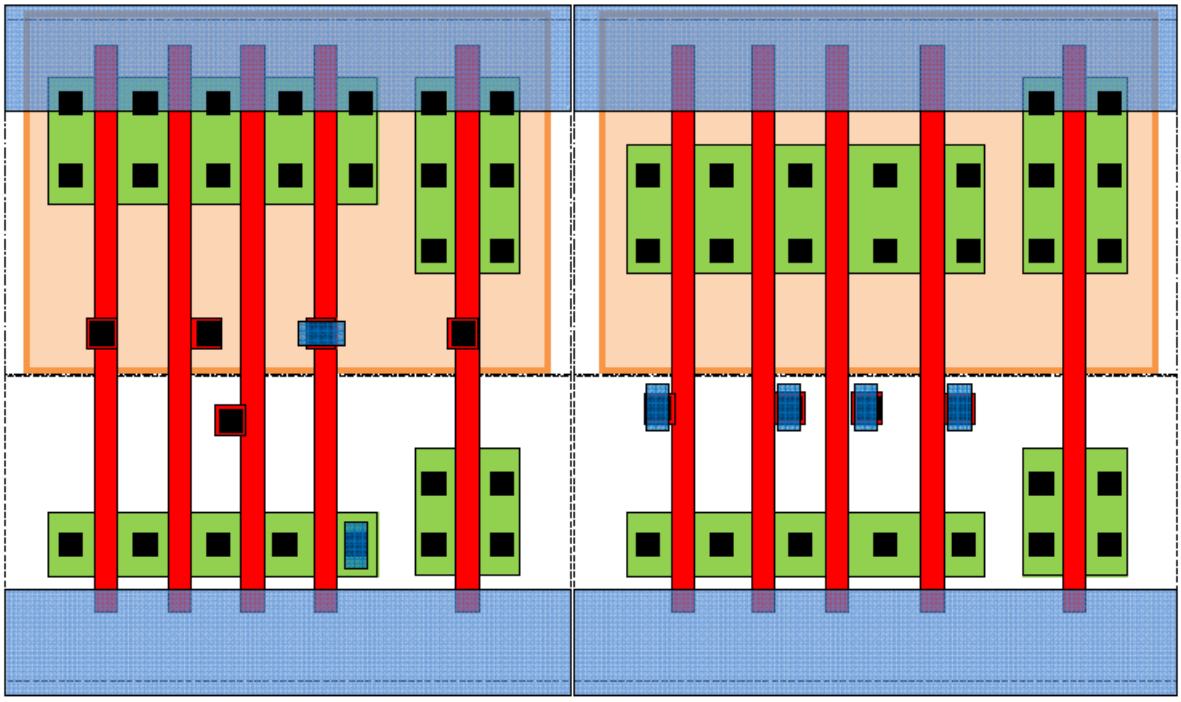

Figure 4: Two templates, a) to the left and b) to the right, for the AO22 standard cell.

Task #8 Elmore delay

What if we added a short metal wire branch on the middle of a long wire, how much would the delay to the first received increase if both receivers are identical? The setup is shown as Case 2 in Figure 5.

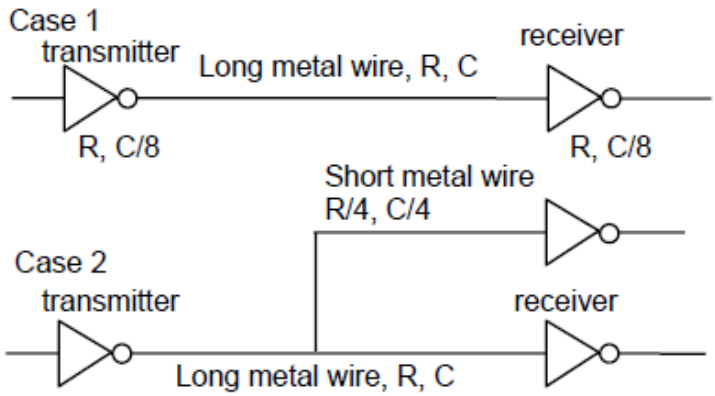

Figure 5: A short wire being added to a long wire from a transmitter to a receiver.

A larger version of Figure 2 for you convenience.

Revised figure for task 4 in HA 3