Home assignment 2

MCC092
Introduction to
Integrated Circuit Design

Chalmers University of Technology

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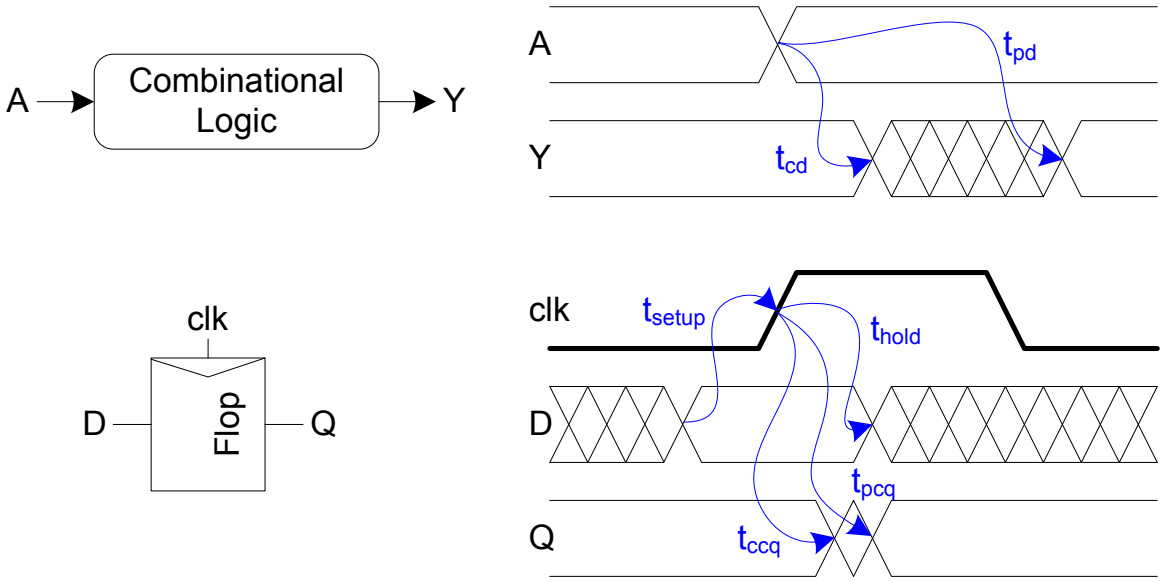
Task #1 Sequencing

You have the following data for one type of flip-flops from a cell library:

Setup time, t_{setup}	60 ps
clk-to-Q propagation delay, t_{pcq}	55 ps
clk-to-Q contamination delay, t_{ccq}	40 ps
Hold time, t_{hold}	30 ps

For you convenience we have included part of Figure 10.4 from Weste & Harris which shows these delays:



You are to use this type of flip-flops for sequencing in a system. Your task is to design the combinational logic, CL, which is to be placed between the flip-flops; therefore you need to determine the timing constraints for this logic.

a) Determine the sequencing overhead for these flip-flops.
b) Determine the maximum logic propagation delay, $t_{pd,}$ if the system is clocked with a clock frequency, f_c, of 2 GHz.
c) Determine the minimum logic contamination delay, $t_{cd,}$ with the same clock frequency as in b).
d) What if there is a clock skew of a maximum 50 ps between any two flip-flops in the system? What is the sequencing overhead then? With the same clock frequency as before, what is then the maximum logic propagation delay, t_{pd}, and the minimum logic contamination delay, t_{cd}?
e) Assume that is it possible to design the combinational logic such that $t_{pd=}$ $t_{cd.}$ With the same clock frequency as before, f_c= 2 GHz, determine the maximum clock skew the system could tolerate with the optimal design of the combinational logic. What does t_{pd} (and t_{cd}) for the CL have to be then?

Task #2 Metastability

In this task you are to use data from the article "Metastability challenges for 65nm and beyond" by Beer and co-authors for a 65 nm process. This article is available from the PingPong page for assignment HA2. The background on metastability can be found in the article "Metastability and Synchronizers: A tutorial" by Ran Ginosar, which is also available from the assignment page. Read pages 23-28 up to "two-flip-flop synchronizer".

You are working as a hardware designer for a satellite-payload system for future telecom systems. Through a project for the European space agency, ESA, a company is to develop an ASIC in a 65-nm process for this purpose. The hardware is to act as huge software-reconfigurable switch for lots of telecom data coming from the earth. The company has previously demonstrated the ASIC concept in a 0.35 um process and a 180 nm process. However, now they are moving to the 65 nm process while they are increasing the clock frequency and data frequency to increase the throughput.

Your task is to investigate the reliability of the new chips due to metastability.

a) Investigate **one** flip-flop in the data-path of the processor. Use data from the paper for T_W and τ[1]. Assume that the processor runs with full V_{DD}, 1.25 V, but that the temperature can vary (as it does in space). Assume that the clock frequency, f_c is 5 GHz and the data rate, f_D, is 200 MHz. If we set the resolution time, S, to one clock cycle, what is the resulting MTBF?

b) There are 4000 flip-flops as the one in task a) in each chip and a full system can comprise 20 chips. What is the resulting MTBF for the entire system if we assume that all the flip-flops are properly designed?

c) Some flip-flops in the control structure must fail much more seldom. Investigate **one** such flip-flop in the processor. Again, use the same data from the paper for T_W and τ. These flip-flops, fortunately, do not switch as often, Assume that f_c = 100 MHz and f_D = 10 MHz. How long resolution time for metastability, S, is required to have a failure rate of 1 per 10 years; that is an MTBF of not less than 10 years**? Express the resolution time, S, in the number of clock periods, T_c, that are required**.

d) The control logic should work correctly even if the operating conditions are less than ideal. In space the power supply and temperature may vary. Assume that the control logic should work correctly over the entire temperature range (space can be cold!) and also when V_{DD} is as low as 1 V. Use other data for τ and T_W from the paper that capture this worse operating conditions. What is the required resolution time then to achieve an MTBF of 10 years? **Express this time in the number of clock periods, T_c, that are required**.

[1] Note that in this context τ denotes the time constant for metastability resolution – note the time constant for gate delay.