Wire delay optimization with wire effort (extra section until chapter 5 is updated)

The Elmore delay model is a useful tool not only for estimating wire delays, but also for optimizing the driving capability of the driver and for optimizing the wire length with respect to the technology at hand. If we return to the situation in Fig. 6.3 where an inverter with an effective resistance R_{eff} and an input capacitance C_G is driving another identical inverter across a wire with resistance R_W and capacitance C_W, and apply the Elmore delay model, we obtain the following dominant time constant

$$T_E = R_{eff}\left(C_D + C_W/2\right) + \left(R_{eff} + R_W\right)\left(C_G + C_W/2\right). \tag{6.10}$$

This dominating Elmore time constant T_E can be rewritten on the following form

$$T_E = \underbrace{R_{eff}C_G\left(p_{inv}+1\right)}_{\text{technology constant}} + R_{eff}C_W + R_W C_G + \underbrace{\frac{R_W C_W}{2}}_{\text{wire constant}}, \tag{6.11}$$

where the first and last terms can be identified as the RC constants of the technology and the wire, respectively. The wire delay can now be written

$$t_{pd} = 0.7R_{eff}C_G\left(p_{inv} + 1 + \frac{R_{eff}}{R_W}\frac{R_W C_W}{R_{eff}C_G} + \frac{R_W}{R_{eff}} + \frac{1}{2}\frac{R_W C_W}{R_{eff}C_G}\right), \tag{6.12}$$

where the relative delay, after introduction of the wire effort

$$w_E = \frac{R_W C_W}{R_{eff}C_G}, \tag{6.13}$$

a concept similar to that of the logical effort, can be rewritten on the following simple form

$$d = p_{inv} + 1 + \frac{R_{eff}}{R_W}w_E + \frac{R_W}{R_{eff}} + \frac{w_E}{2}. \tag{6.14}$$

Having found this expression for the relative wire delay, we next use it to determine the optimal inverter driving capability that yields the smallest delay. By taking the derivative with respect to R_{eff}, we find that the optimal driving capability minimizing the wire delay is obtained when the two terms involving the effective resistance of the inverter, i.e. when

$$\frac{R_{eff}}{R_W}w_E = \frac{R_W}{R_{eff}}, \text{ and consequently } R_{eff,opt} = \frac{R_W}{\sqrt{w_E}}. \tag{6.15}$$

The relative wire delay using an optimized driver inverter now becomes

$$d = p_{inv} + 1 + 2\sqrt{w_E} + \frac{w_E}{2}. \tag{6.16}$$

Repeater insertion

Having learnt how to match the effective resistance of the driver to the resistance of the wire for minimum wire delay, the time has come to discuss what would be the optimal length L_{opt} of a wire. Since both the wire resistance and the wire capacitance are proportional to the wire length L,

$$R_W = rL, \text{ and } C_W = cL, \tag{6.17}$$

where r and c are the wire resistance and capacitance per unit length, respectively, the RC product of a wire is proportional to the wire length L squared,

$$R_W C_W = rcL^2. \tag{6.18}$$

Thus, a 4 mm wire has an RC product sixteen times that of a 1 mm wire. Therefore, the wire $R_W C_W$ product would be negligible for short wires ($L<<L_{opt}$), but dominating the delay for long wires ($L>>L_{opt}$). Wires should therefore be kept short. One way to keep wires short, if the blocks to be connected cannot be placed close to each other on the chip, is to split long wires into wire segments driven by repeaters identical to the driver inverter, shown in Fig. 6.3.

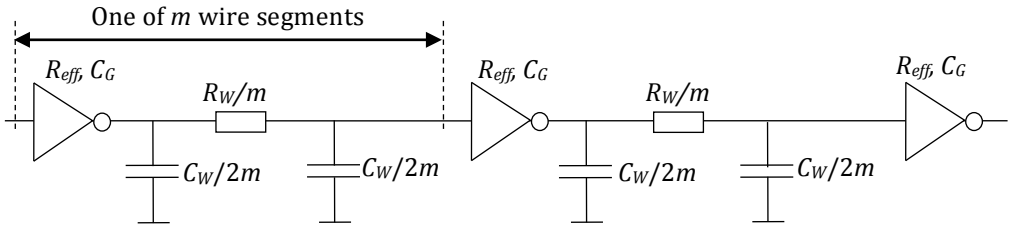

Fig. 6.4. Splitting wires into segments and inserting repeaters.

For finding the optimal number of segments m, the normalized wire delay is rewritten to account for the delay of the m wire segments

$$d = m\left(2 + \frac{R_{eff}}{mR_W} w_E + \frac{R_W}{mR_{eff}} + \frac{w_E}{2m^2}\right), \tag{6.19}$$

where we, for simplicity, we have assumed p_{inv}=1. In this equation, the two middle terms that we used to determine the optimal driving capability of the driver inverter have no dependence on the number of segments. By taking the derivatives with respect to m, we find that minimum delay is again obtained when the two terms depending on m are equal. This function has a minimum for

$$2m_{opt} = \frac{w_E}{2m_{opt}}, \rightarrow m_{opt} = \frac{\sqrt{w_E}}{2}. \tag{6.20}$$

Again, we find that the optimal number of segments depends on the square root of the wire effort. Hence, minimum delay is obtained when the wire is divided into the optimal number of segments driven by optimized repeaters. The minimum relative delay is given by

$$d = 4\sqrt{w_E}. \tag{6.21}$$

The optimal wire length that we set out to find is then given by the wire length L divided by the optimal number of wire segments, m_{opt},

$$L_{opt} = \frac{L}{m_{opt}} = 2\sqrt{\frac{RC}{rc}}. \tag{6.22}$$