Chapter 6: Layout and technology

This chapter has its focus on technology and layout. The main purpose is to give a basic understanding of the relationship between the electrical representation of a CMOS logical gate, its physical layout, and the main processing steps. On the course web page, a short animation illustrates these concepts. The first part of the animation focuses on the front-end technology for processing active devices in the silicon, while the second part focuses on the back-end processing of interconnects. Related to the technology issues, the chapter contains a short section on layout, illustrating the most basic CMOS logic cell design and layout concepts. To avoid the many detailed geometrical design rules, a simplified layout template will be used for this exercise. The purpose of the chapter is not to produce layout specialists, but rather to give an introductory insight into the importance of cell layout for performance.

A. Technology

In Fig. 6.1.a, the layout of an inverter is shown, together with the corresponding cross section of the layout. The layers shown are the p-type substrate, n-well, active areas, n-select, poly, contacts to active, and first metal. These layers are usually referred to as the front-end layers. These layers are used to design the cells in the cell library. Cells are connected to the interconnect back-end layers through vias between metal1 and metal2.

The next figure shows the first two layers of the back-end interconnect. In total, there are between six and 10+ metal layers in a modern CMOS process. Fig. 6.1.b shows how the metal2 layer has been formed using single damascene technology. This means that the upper copper layer is connected to a lower metal layer through tungsten via plugs (black). The metal3 layer is formed through the more advanced dual damascene technology, where also the via itself is made of copper. Copper has replaced aluminum today because of its higher conductivity (almost a factor of two better), but has required a completely new technology called CMP, chemical and mechanical polishing, for its implementation.

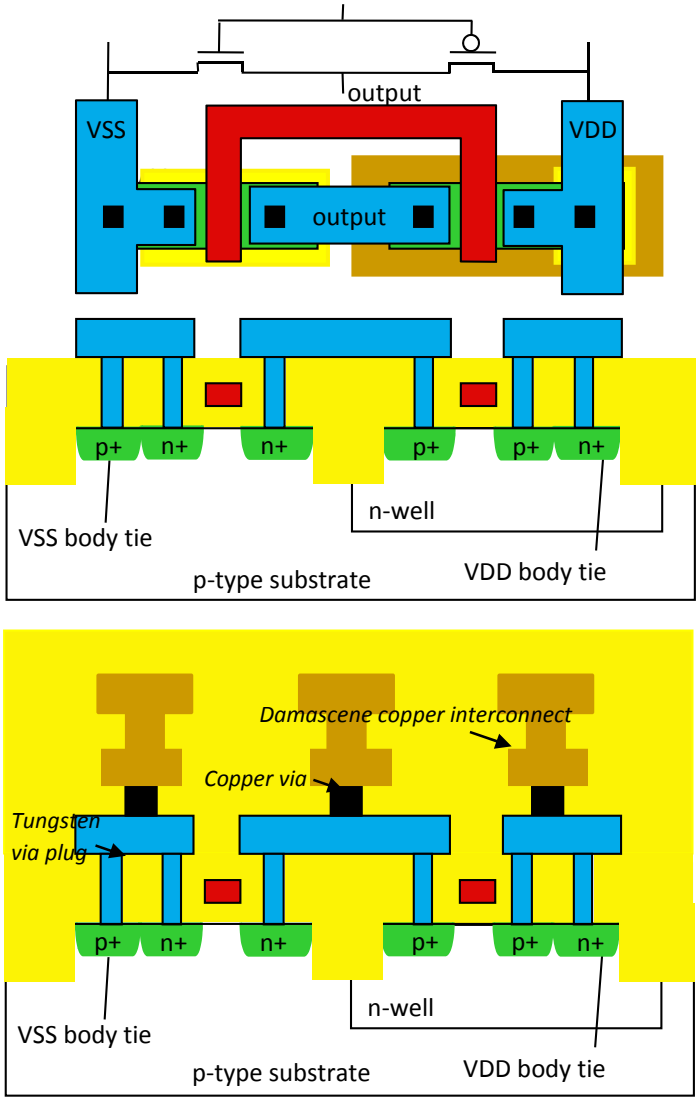


Fig. 6.1. a) Relationship between schematic, layout and cross-section. b) Back-end processing including single and dual damascene copper interconnects.

B. Layout

Although we are not aiming at becoming layout specialists, it is valuable to have some insight into the layout procedure, and to have some basic knowledge of the geometric design rules. Working as an ASIC design engineer, the cell library manufacturer usually never allows any insight into the layout of the cells in their cell library. At most, the metal1 layer is visible together with the position of the input and output terminals. Hence, it will be a good practice to have done some basic design exercises. Not to burden you with all the detailed geometric design rules, we have supplied a layout template with rails, n-well, n-select and p-select areas already defined according to the design rules. Some basic intra- and interlayer design rules are shown in Fig. 6.2. Note that MOSFETs are formed whenever polysilicon (red) crosses active (green). Also observe that the minimum poly width sets the minimum channel length. In this example, the minimum channel width is 120 nm, twice the minimum channel length.

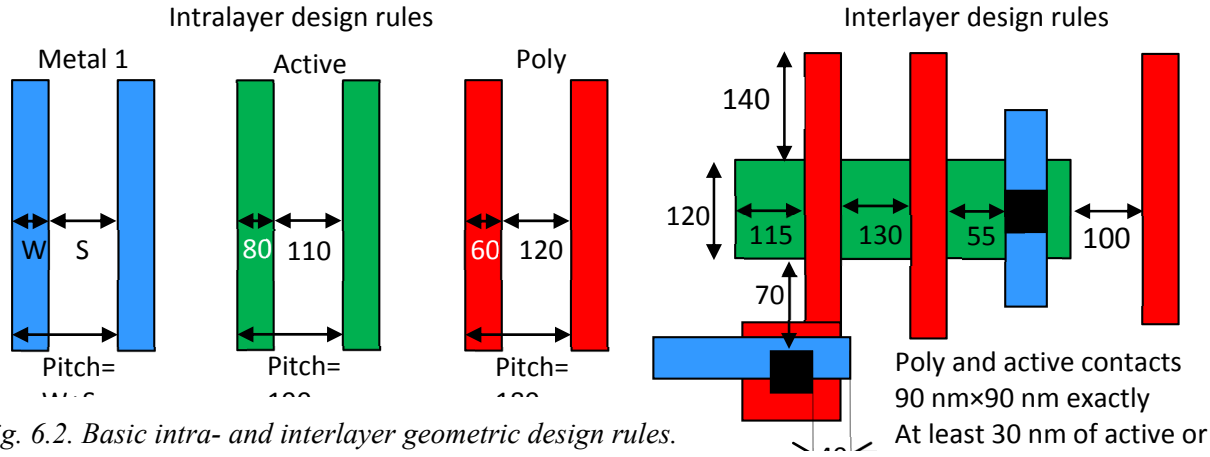


Fig. 6.2. Basic intra- and interlayer geometric design rules.

In Fig. 6.3 to the right, a typical cell library layout architecture is shown. Standard cell libraries contain the primitive cells required for digital design. All cells in a standard cell library have the same height, in this case 2.6 µm. The V_{DD} rail runs at the top, and the V_{SS} or ground rail runs at the bottom. During cell placement, cells are mirrored along the dashed lines running through rails in order to share rails and save area. Within the 2.6 µm frame-work, there is room for inverters with three different driving capabilities, X2, X4, and X8 (X9). For these three cell sizes, the n-channel device widths are 200, 390, and 780 µm, respectively, and the corresponding p-channel device widths are √2 times those sizes, i.e. 280, 550, and 1100 µm.

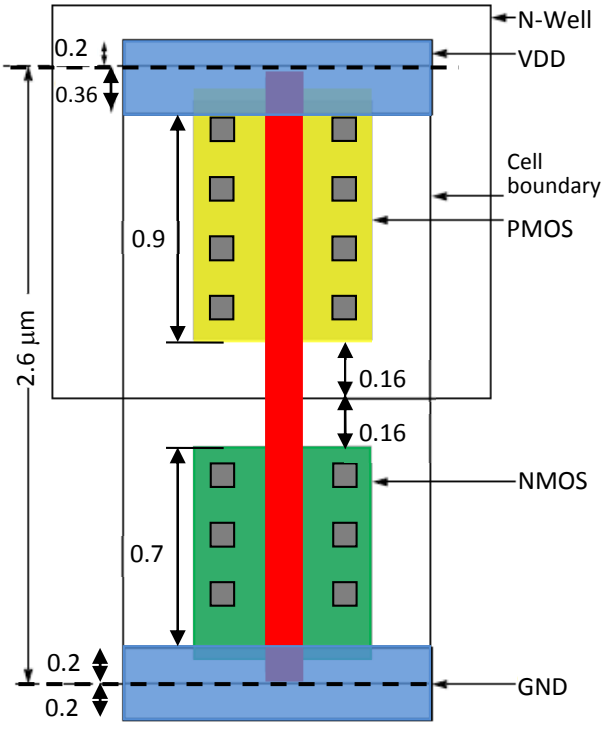
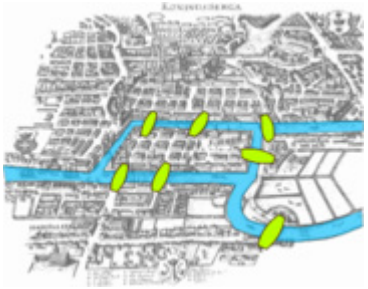


Fig. 6.3. Cell library architecture [from ST]

Layout and Euler paths. The overall goal of any layout exercise is to make a layout as compact as possible to reduce cell footprint and to reduce parasitic capacitances. The main layout strategy is that of a "single line of diffusion", i.e. one line of n-type diffusion for the n-channel MOSFETs, and one line of p-type diffusion for the p-channel MOSFETs. To save area, or silicon real-estate, it is important not to divide these lines of diffusions into segments, unless absolutely necessary. This leads us to the mathematician Leonhard Euler and the problem of "The Seven Bridges of Königsberg", a historically notable problem in mathematics.



The city of Königsberg (now Kaliningrad) was set on both sides of the Pregel River, and included two large islands which were connected to each other and the mainland by seven bridges. The problem was to find a walk through the city that would cross each bridge once and only once. Euler proved that the problem had no solution. The difficulty was the development of a technique of analysis and of subsequent tests that established this assertion with mathematical rigor. Euler pointed out that the only important feature of a route is the sequence of bridges crossed. This allowed him to reformulate the problem in abstract terms (laying the foundations of graph theory). In modern terms, one replaces each land mass with an abstract "vertex" or node, and each bridge with an abstract connection, or "edge", which serves to record which pair of vertices (land masses) is connected by that bridge. The resulting mathematical structure is called a graph. [From Wikipedia]

This graph-based technique can be used when laying out a CMOS logic gate. If all MOSFET gates can be passed, and passed only once[5], and in the same order for both the p-channel and the n-channel devices, a compact layout can be made where both lines of diffusion are unbroken. This principle is illustrated below for the 2+1 AND-OR gate.

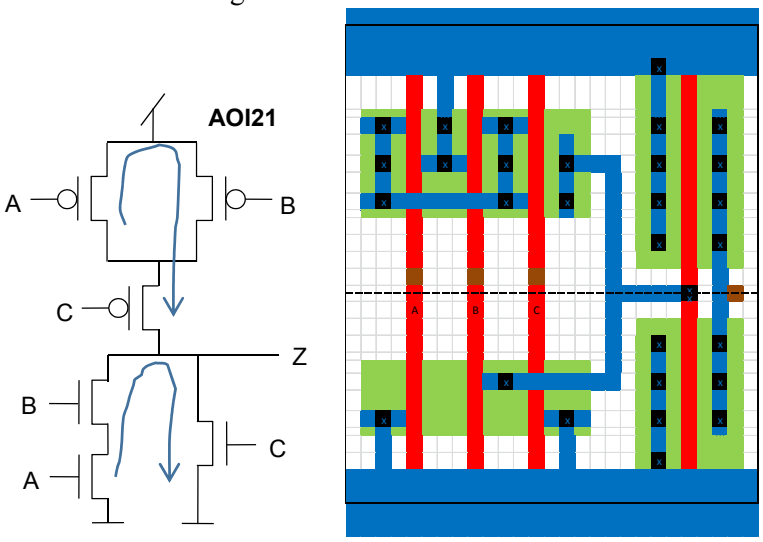


Fig. 6.4. Illustration of Euler paths and the corresponding AOI21 layout.

[5] Euler's argument shows that a necessary condition for the walk of the desired form is that the graph be connected and have exactly zero or two nodes of odd degree. (The degree of a node is the number of edges touching it). This condition turns out also to be sufficient - a result stated by Euler and later proven by Carl Hierholzer. Such a path is now called an *Euler path* in his honor. Further, if there are nodes of odd degree, then any Eulerian path will start at one of them and end at the other. [From Wikipedia]

Exercise 6.1: Use the layout templates below to lay out a 3-input AND, and a 3-input OR gate!
Exercise 6.2: Use the two layout templates below to lay out the following carry and sum logic cells of a ripple-carry adder:

$$C_{out} = (A+B)C_{in} + AB;\ SUM = ABC_{in} + (A+B+C_{in})\overline{C_{out}}\ .$$

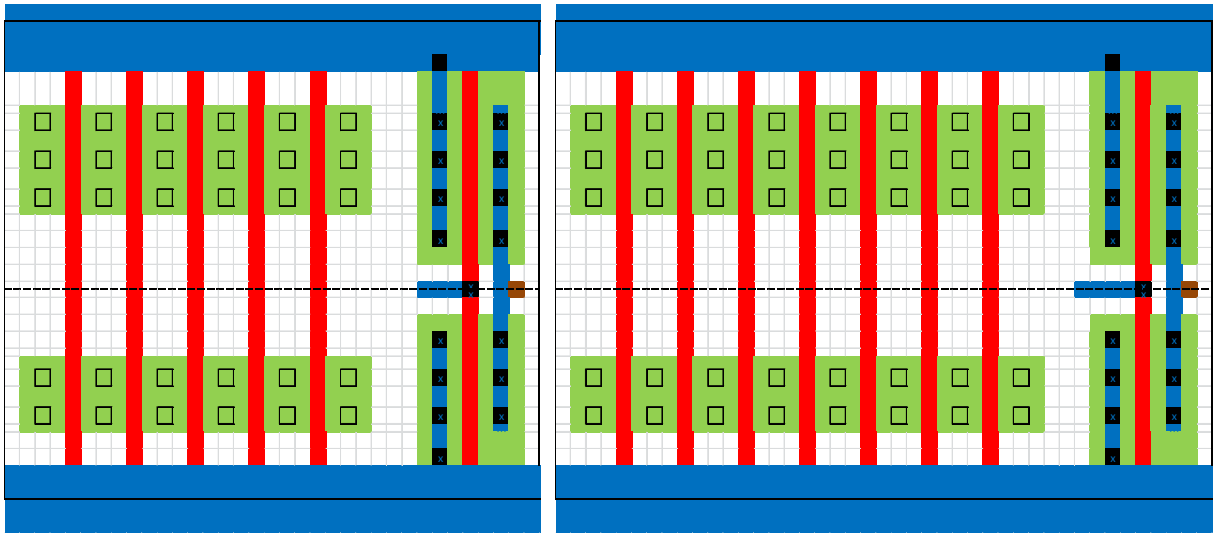


Fig. 6.5. Layout templates for ripple-carry adder layout.

Suggested hands-on laboratory exercise: Use the Cadence Virtuoso layout tool to lay out your ripple-carry cell from the exercise above. Run the geometric design rule checker to check that the layout is in accordance with the geometric design rules given in the beginning of this chapter. Finally, run the layout-versus-schematic (LVS) tool to check that the functionality of the layout is the same as that from your previous schematic entry laboratory exercise! Shown below in Fig. 6.6 are the layout templates available during the hands-on layout laboratory session.

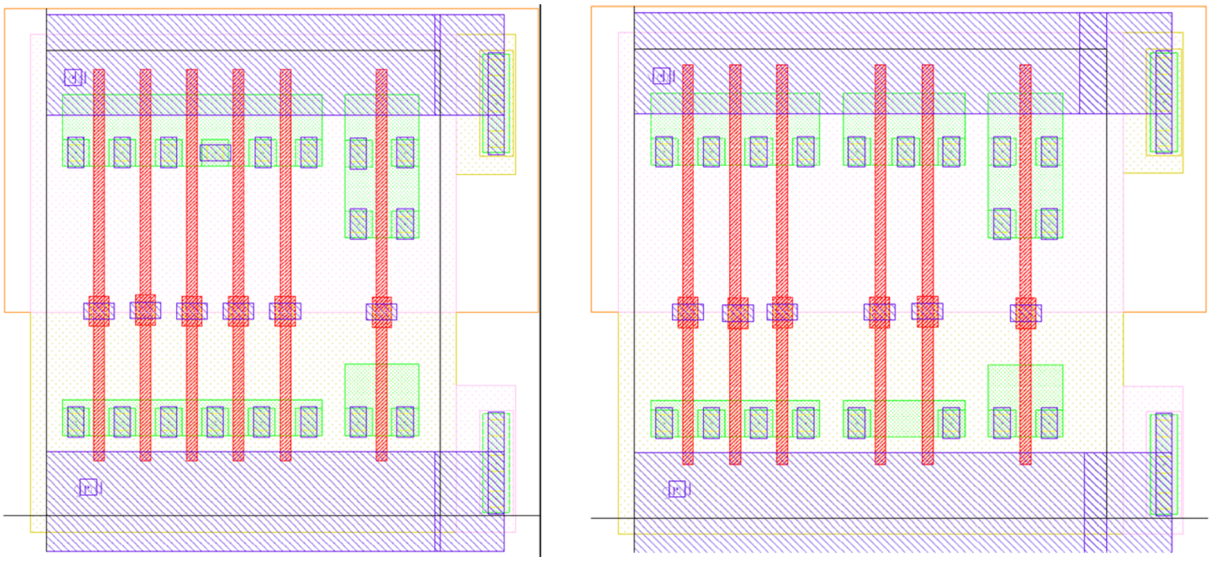


Fig. 6.6. Cadence Virtuoso layout templates for the hands-on laboratory exercise.