Chapter 5:   Wire delay

The overall aim of this chapter is to emphasize the importance of interconnect as the main cause of propagation delay in modern CMOS circuits, and to develop a simple RC-based wire delay model. The so called Elmore delay model is based on the assumption of a dominating time constant of a multi-stage RC network representing the distributed wire. We will also learn that wire delay increases as L^2, where L is the wire length, and that wires therefore should be kept short, for instance by splitting long wires into segments driven by repeaters.

Introducing the wire π-model. Previous chapters neglected the influence of wire delay on the propagation delay, and only considered capacitive loads caused by the input capacitance of the next stage logic gates. However, as already mentioned, interconnect delay becomes more and more dominant for each new technology node, since wires are becoming longer and at the same time thinner and narrower. Let us therefore look at the problem of an inverter driving a signal to another inverter across a long bus wire, as shown in the figure below. To solve this problem of estimating the propagation delay, we need a wire model. Since wires are long, and their capacitances are distributed along the wire, we need a distributed wire model. A simple distributed wire model, the π-model, is shown below. In the π-model, the wire capacitance has been split 50-50 to either sides of the wire resistance. This model is most often good enough for back-of-the-envelope estimations, but for circuit simulations wires usually need to be replaced by at least three π-segments to obtain accuracy within a few per cent.
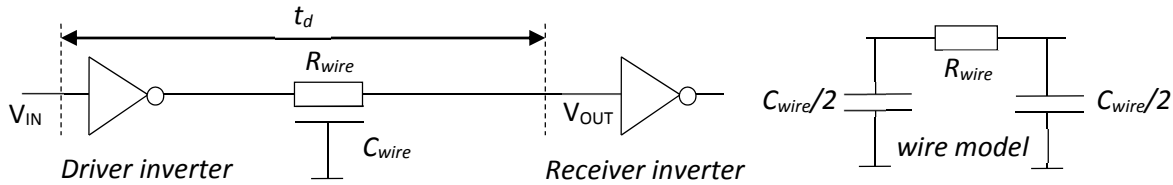

Fig. 5.1. Illustration of wire delay and of the distributed RC wire π-model.

Combining the driver inverter model, the wire model and the receiver inverter model, we obtain the following RC circuit.
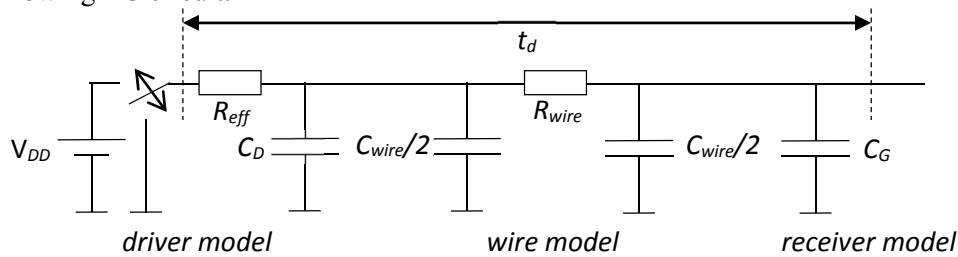

Fig. 5.2. Electrical RC model for calculation of the wire delay.

This two-pole problem can be solved analytically, since the corresponding differential equation is a linear, second-order, differential equation. Usually, the two poles are far apart, and then the dominating time constant can be approximated by

$$\tau = R_{eff}\left(C_D + C_{wire} + C_G\right) + R_{wire}\left(C_{wire}/2 + C_G\right). \tag{5.1}$$

In this approximation, each resistance is multiplied by the sum of its downstream capacitances, so model is quite easy to remember.

The wire RC flight time is given by

$$\tau = \frac{R_{wire}C_{wire}}{2} = \frac{rcL^2}{2},$$ (5.2)

where r and c are the resistance and capacitance per unit length, respectively.

Repeater insertion. As can be seen from this expression, the wire RC flight time increases as the wire length squared, L^2. Therefore, it is important to keep wire lengths short. One way of decreasing wire lengths is to split wires into segments, and to insert repeater inverters to drive the wire segments. This concept is shown in the next figure, where a wire has been split into N segments and an inverter been inserted to drive each segment. In the figure, the repeater is characterized by its effective resistance, R_{rep}, and its input capacitance C_{rep}, and parasitic output capacitance, $C_{par} = pC_{rep}$.
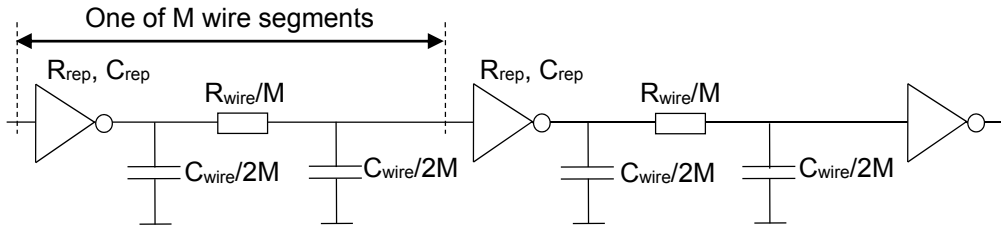

Fig. 5.3. Splitting wires into segments and inserting repeaters.

Assuming inverter $p=1$, the Elmore delay across the M wire segments can now be written

$$\tau = M\left[R_{rep}\left(\frac{C_{wire}}{M} + 2C_{rep}\right) + \frac{R_{wire}}{M}\left(\frac{C_{wire}}{2M} + C_{rep}\right)\right].$$ (5.3)

By differentiating with respect to M, minimum delay is obtained when

$$2MR_{rep}C_{rep} + \frac{R_{wire}C_{wire}}{2M} = 0,$$ (5.4)

i.e. for an optimal number of segments

$$M_{opt} = \frac{1}{2}\sqrt{\frac{R_{wire}C_{wire}}{R_{rep}C_{rep}}}.$$ (5.5)

From this expression a critical wire length for repeater insertion can be found

$$L_{crit} = L/M_{opt} = 2\sqrt{R_{rep}C_{rep}/r_{wire}c_{wire}}.$$ (5.6)

Now, we have found the optimal number of wire segments, and the critical wire length for repeater insertion. In the next step, we would like to find out how to size the repeaters with respect to the wire resistance. By differentiating with respect to R_{rep}, assuming $R_{rep}C_{rep}$ is constant, minimum delay is obtained when the repeater is sized for a driving capability given by

$$C_{wire} - R_{wire}\frac{C_{rep}}{R_{rep}} = 0, \text{ i.e. when } R_{rep}C_{wire} = R_{wire}C_{rep}, \text{ or more conveniently}$$

$$R_{rep} = \frac{R_{wire}}{2M_{opt}}.$$ (5.7)

This repeater size will minimize the delay independently of the number of wire segments. However, if the wire is split into the optimal number of segments, M_{opt}, all four terms in the delay model (5.3) turn out to be equal yielding a minimum delay of

$$\tau = 4\sqrt{R_{rep}C_{rep}R_{wire}C_{wire}} \ . \tag{5.8}$$

The approximate wire delay model just derived for a two-stage RC ladder, was generalized by Elmore[2] for RC ladders of any number of stages, N, assuming the following dominant time constant:

$$\tau = R_1\sum_{i=1}^{N}C_i + R_2\sum_{i=2}^{N}C_i + ... + R_N C_N , \tag{5.9}$$

where

$$C_{kN} = \sum_{i=k}^{N}C_i , \tag{5.10}$$

represents the downstream capacitance of node k (to the final wire node N). Elmore´s delay model can also be written on the following equivalent form:

$$\tau = C_1 R_1 + C_2\left(R_1 + R_2\right) + ... + C_N\sum_{i=1}^{N}R_i , \tag{5.11}$$

where

$$R_{1k} = \sum_{i=1}^{k}R_i , \tag{5.12}$$

represents the upstream resistance of node k (to the input wire node1). It can be shown that the propagation delay given by the Elmore delay model is to be found within the following bounds: $\tau/2 < t_{pd} < 2\tau$. Even tighter bounds have been developed by Rubinstein, Penfield and Horowitz[3].

Handling branches. Based on a mathematical manipulation of the nodal equations of an RC ladder, certain rules have been derived for handling the influence on the propagation delay of wire branches. In a first-order approximation only branch capacitances are considered, while branch resistances are neglected. Based on this discussion, Elmore´s delay model can be summarized on a form where the time constant of any wire end point, i, is given by the sum over all wire nodes, k,

$$\tau_i = \sum_{k=1}^{N}C_k R_{ki} , \tag{5.13}$$

where R_{ki} the resistance of the path from node i to the input node that is common to the path from node k to the same input node.

[2] W. C. Elmore, "The transient analysis of damped linear networks with particular regard to wideband amplifiers", Journal of Applied Physics, vol. 19, 55-63, 1948.

[3] Rubinstein, J. , Penfield, P. , Horowitz, M.A., "Signal Delay in RC Tree Networks", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 2 , No. 3, 1983
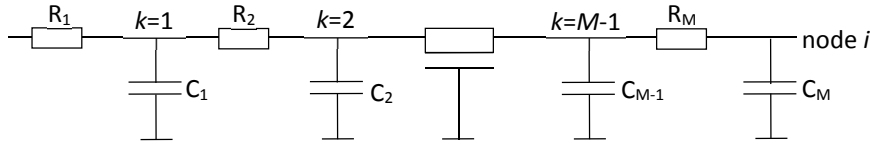
Fig. 5.4. Illustration of the Elmore delay calculation.

Example 5.1: Calculate the wire propagation delay along the highlighted main path!

Solution: After having identified the main path, neglecting the branches, we can draw an equivalent RC-circuit of the main path as shown in Fig. 5.6. From the equivalent circuit we can easily identify the downstream capacitances for each resistor and use this to estimate the wire delay using Elmore´s delay model. By summing up the wire and gate input capacitances, we find that the downstream capacitance from the X40 inverter output (node N1) is 12C (including 4C, the parasitic output capacitance of the X40 driver itself), the downstream capacitance from node N2 is 6C, the downstream capacitance from node N3 is 3C, and finally, the downstream capacitance from node N4 is 3C/2. The following Elmore main path propagation delay can now be derived:

$$t = RC\left[12 + 6 + 2 \times 3 + 4 \times \frac{3}{2}\right] = 30RC \ .$$
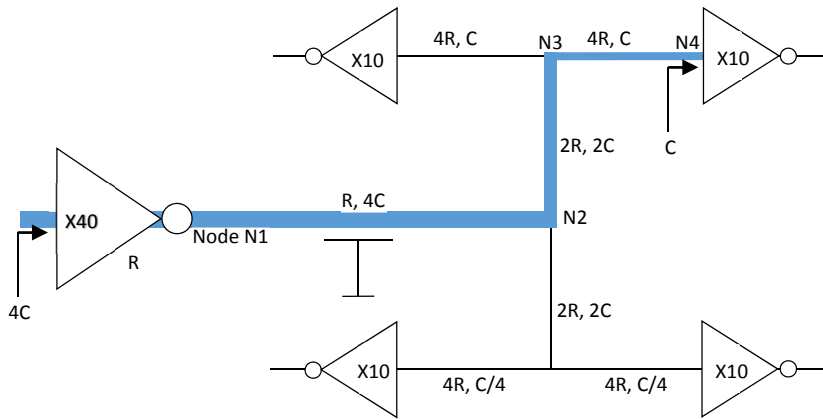

Fig. 5.5. Illustration of the H-type wire interconnect.

Now, we must add the influence of the branches on the delay. The branch capacitance of node N2 is 4.5C, while the branch capacitance of node N3 is 2C. The influence of the branches on the delay is then given by

$$t = RC\left[2 \times 4.5 + 4 \times 2\right] = 17RC \ .$$

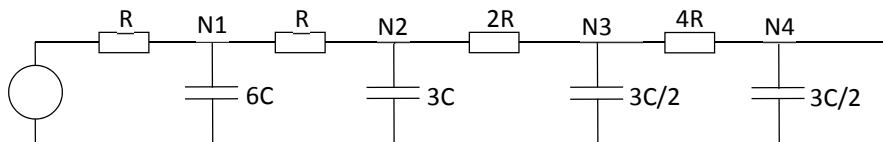Hence, the total wire delay is estimated to 47RC. ∎

Fig. 5.6. Electrical RC-model of the H-type wire interconnect.

Example 5.2: a). In the example below, a wire is divided into two segments using an X5 repeater. The X1 reference inverter has input and output capacitances C, and an effective resistance R. The wire

resistance is also R, while the wire capacitance is $100C$. Calculate the total propagation delay!

b). Where along the wire should the X5 inverter be placed for minimum delay?

c). On the other hand, if the repeater is placed in the middle of the wire, what would be its most effective driving capability in order to minimize the delay?

Solution: a) Applying Elmore's delay model, not neglecting the parasitic inverter output capacitances, the delay for the three stages can be written

$$t = \left(R \times 56C + \frac{R}{2} \times 30C \right) + \left(\frac{R}{5} \times 70C + \frac{R}{2} \times 40C \right) + \frac{R}{15} \times 90C = 111RC .$$
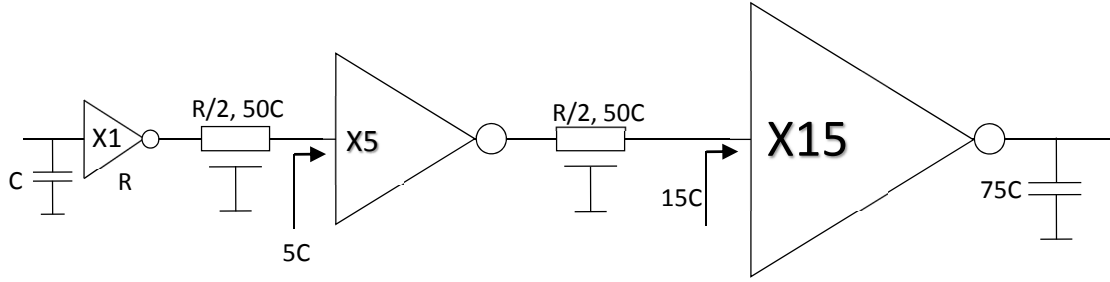

Fig. 5.7. Illustration of wire delay problem.

b). As the problem is formulated, the X5 repeater is placed in the middle of the wire, thereby dividing the wire into two segments of equal length. Assume instead that the X5 inverter is placed with x of the wire length in front of the X5 inverter (and $1-x$ after). In this case, the delay is given by

$$t = \left[\{ (6 + 100x) + x(5 + 50x) \} + \{ 1/5 \times (20 + 100(1-x)) + (1-x) \times (15 + 50(1-x)) \} + 6 \right] RC =$$
$$= 100x^2 - 30x + 101$$

Minimum delay is for $x=0.15$, i.e. with 15% of the wire to the left of the X5 repeater and 85% of the wire to the right of the X5 repeater.

c). In this case we assume that the driving capability of the repeater is y instead of 5. The delay equation given in a) is then modified as follows:

$$t/RC = \left((51+y) + \frac{1}{2} \times (25+y) \right) + \left(\frac{1}{y} \times (65+y) + \frac{1}{2} \times 40 \right) + \frac{90}{15} = 90.5 + \frac{3x}{2} + \frac{65}{x} .$$

This equation shows that the X5 inverter yields almost the same propagation delay as the X9 inverter. However, the most effective repeater size, when it comes to minimize the delay, is the X7 inverter (if available in the cell library). A minimum delay of $110RC$ is obtained for $y=6.58$, however, the decrease is less than 1%. Therefore an X5 repeater occupying less silicon area will do. ∎

Example 5.3: A metal wire is 2 mm long and 0.2 μm wide. The metal sheet resistance, R_S, is 0.1 Ω/□, and its capacitance per unit length, c, is 0.2 fF/μm wire length including the edge effects. a) Calculate the wire resistance and the wire capacitance. b) What is the critical wire length for repeater insertion, and what would be the source resistance of the driving inverter to minimize the delay?

Solution: a) The wire resistance and the wire capacitance are given by

$$R = \frac{L}{W} R_S = \frac{2000}{0.2} \times 0.1 = 1 \text{ k}\Omega, \text{ and } C = Lc = 2000 \times 0.2 = 400 \text{ fF, respectively} .$$

b) The resistance per unit length is r=0.5 Ω/μm, and hence rc=0.1 fs/μm^2. Assuming that the inverter RC constant is 5 ps for the CMOS technology of choice, the critical wire length is found, from the expression previously derived, to be

$$L_{crit} = 2\sqrt{R_{rep}C_{rep}/r_{wire}c_{wire}} = 2\sqrt{5000/0.1} = 440 \ \mu m \ .$$

The 2 mm wire should then be split into four segments, each 0.5 mm long (with R=250 Ω and C=100 fF). Previously, we found the optimal driver resistance for minimum delay to be

$$R_{rep} = \sqrt{\frac{R_{wire}}{C_{wire}}R_{rep}C_{rep}} = \sqrt{\frac{0.250}{100}\times 5} = 110 \ \Omega \ .$$

Theoretically, if the X10 reference inverter has a 1.4 k Ω source resistance, an X127 inverter with a 110 Ω source resistance would be needed here[4].
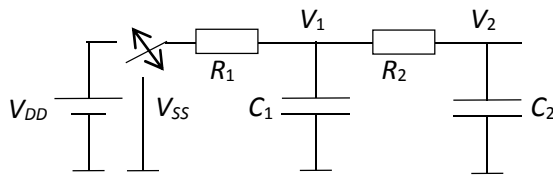
To validate the solution and to remove any doubts of having done any mistakes during calculations, let us check the relative size of the four terms of the Elmore delay after optimization. For minimum delay the four terms should be about equal. Inserting values, we obtain

$$\tau = N\left[R_{rep}\left(\frac{C_{wire}}{N}+2C_{rep}\right)+\frac{R_{wire}}{N}\left(\frac{C_{wire}}{2N}+C_{rep}\right)\right] = 4\left[0.11(100+90)+0.250(45+45)\right] =$$
$$= 4[11+9.9+11+11]=172 \ ps.$$

Since the four RC terms are equal (almost), our solution seems to be correct. ∎

Exercises
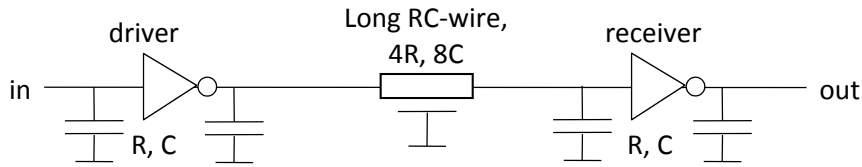
1. Shown below is a simplified version of the two-pole RC network from Fig. 1.
    a. Write down the two nodal equations for V_1 and V_2!
    b. Find a method to convert these two nodal equations into a second-order linear differential equation for $V_1(t)$ and $V_2(t)$!
    c. Use the characteristic equation found above, and the identity $(s+a)(s+b)=s^2+(a+b)s+ab=0$ to find a simple way of determining the dominating time constant $1/a$, if $1/a\gg 1/b$!
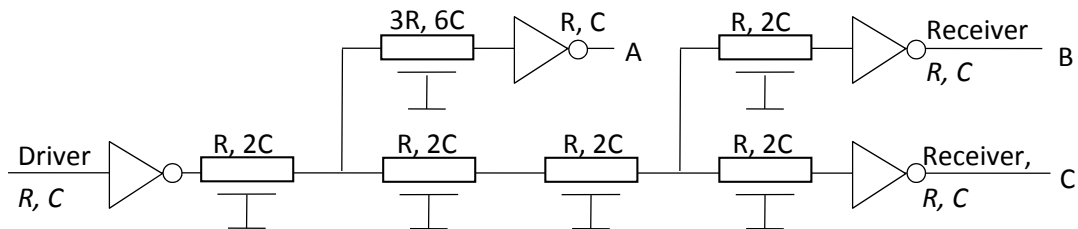

2. An inverter is driving another similar inverter across a rather long RC wire. The inverter input and output capacitances are C, and its internal source resistance is R. The wire resistance is $4R$ and the wire capacitance is $8C$. (Written exam 2008)
    a. Calculate the wire RC-delay from the driver input to the receiver input!
    b. What is the minimum wire delay if the two repeaters are properly scaled?
    c. How much does the delay increase if the receiver inverter is replaced by a 2-input NAND gate with twice the input capacitance compared to the original inverter?

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[4] In the ST 65 nm cell library, the X106 inverter is the closest with an average pull-up/pull-down resistance of 120 Ω, and a 27 fF input capacitance.

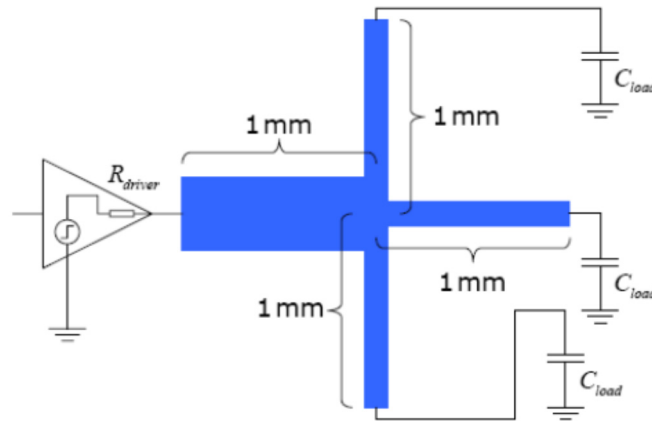d. How much does the delay increase if a branch wire R, $2C$ is added at the wire midpoint?

3. In a certain CMOS process, the wire sheet resistance is 0.10 /square, and the wire capacitance is 0.4 fF/um^2. Calculate the critical wire length for 100 nm wide wires! The inverter time constant is t_{rep}=5.6 ps.

4. In another CMOS process, the wire fringing field capacitance along the wire sidewalls cannot be neglected. Being 35 aF/μm (including both sidewalls) it must be added to the wire bottom plate capacitance of 30 aF/μm^2. The wire sheet resistance is 0.10 /square as in the previous example.
   a. Calculate the wire resistance and wire capacitance for a wire 10 mm long and 1 μm wide!
      (Answer: 1 kΩ, 650 fF; r=100 Ω/mm, c=65 fF/mm)!
   b. Calculate the delay between the input signals of a driver inverter and a receiver inverter at the other end of the 10 mm wire, if the inverter can deliver 600 μA at V_{DD}=1.2 V, and if its input capacitance is 3.25 fF (assume p=1)!
      (Answer: 2*(3.25+650+3.25)+1*(325+3.25)=1.64 ns.
   c. For this process, what would be the critical wire length?
      (Answer: $R_{rep}C_{rep}$=6.5 ps, rc=6.5 ps/mm^2. $L/N = 2\sqrt{R_{rep}C_{rep}/rc} = 2\sqrt{6.5/6.5} = 2$ mm

5. In this problem a $4R$, $8C$ wire like the one in exercise 2 has two branches. The wire lengths to each of the three receivers are the same, and each wire path has the same resistance, $4R$, and the same capacitance, 8C. However, due to the branches there will be some clock skew between the clock signals at nodes A, B, and C.
   a. Calculate the clock skew between nodes A, B, and C, assuming that the three receivers drive the same capacitive load, 16C.
   b. Recalculate the clock skew for the case where the inverter repeaters are replaced by 2-input NAND gates serving as clock gaters! By means of clock gaters, the clock signal can be turned off at any node A, B, or C, thereby considerably reducing power dissipation. The NAND gates are sized for the same driving capability as the inverters.

11. The figure below shows an on-chip metal wire network which is driven by a buffer inverter with a source resistance, R_{driver}, of 80 Ω. Both the input capacitance and the parasitic output capacitance of the buffer is equal to C_{load} = 50 fF. (Written exam 2009).

The wire metal has a sheet resistance at 0.15 Ω/square, a bottom plate capacitance of 40 aF/μm^2, and a total fringing capacitance per unit wire length of 100 aF/μm (50 aF/μm on each side).

  a. Calculate the resistance and the capacitance for the 15 μm wide feed wire if it is 1 mm long!
  b. Calculate the resistance and the capacitance for the three narrow 5 μm wide wire branches if they are also 1 mm long!
  c. Calculate the wire delay to any of the three output nodes!

Suggested hands-on lab exercise

Model a wire by four π-segments and simulate the delay from the driver input to the receiver output. Compare the signal after the driver with the signal after each of the wire segments. What happens to the signal along the wire? How is the signal affected by passing from receiver input to receiver output? How would you describe the development of the signal along the wire compared to the signal after each of four ripple-carry cells in the adder that you simulated in a previous hands-on lab exercise? What if we insert repeaters between each wire segment, what happens to the total propagation delay, and to the shape of the signal?