Technology parameters 0.13-μm process 2011

Note: The design rules and electrical aparameters presented in this document are representative for a 0.13-μm CMOS process, and are intended for teaching purposes only. $V_{DD} = 1.2V$ normally.

LL Transistors					
	Transistor type				
	nMOS		pMOS		Unit
Gain factor low V_{GS} & L < 10 μm	$k'_n(\mu_n C_{ox})$	275	$k'_p(\mu_p C_{ox})$	75	$\mu A/V^2$
Threshold voltage (W/L=10/10)	V_{t0n}	0.29	V_{p0n}	-0.37	V
Threshold voltage (W/L=10/0.13)	V_{t0n}	0.44	V_{p0n}	-0.39	V
Body-effect factor	γ_n	0.4	$2\gamma_p$	0.4	$\sqrt{V}$
Surface potential ($\phi_B \approx 2 \cdot \phi_f$)	$2\phi_{fn}$	0.9	$2\phi_{fp}$	0.9	V
Early-voltage factor (W/L = 1/1)	$V'_{An} = r'_{dsn} = 1/\lambda'$	10	V'_{Ap}	20	$V/\mu m$
Early-voltage factor (W/L = 10/10)	V'_{An}	3	V'_{Ap}	20	$V/\mu m$
Drain-source breakdown voltage		1.32		1.32	V
Saturation current (L = 0.13, W > 0.8 μm)	I_{DSATn}	0.53	I_{DSATp}	0.24	$mA/\mu m$

Sheet resistance		
Layer		$\Omega/\square$
poly	R_{sp}	10
metal1-4	R_{sm1-4}	0.075
metal5	R_{sm5}	0.06
metal6	R_{sm6}	0.02
n+ diff	R_{sdn}	10
p+ diff	R_{sdp}	10
n-well	R_{snw}	750

Capacitances (layer to substrate)				
	Area $fF/\mu m^2$		Perimeter $fF/\mu m$	
gate oxide capacitance	C_{ox}	12		
gate-diff (S/D) overlap			C_{gso}	0.18
n+ diff (0 V)	C_{j0n}	0.87	C_{jswn}	0.04
n+ diff (0 V) - gatewall			C_{jgwn}	0.4
p+ diff (0 V)	C_{j0p}	0.89	C_{jswp}	0.03
p+ diff (0 V) - gatewall			C_{jgwp}	0.3

Max current density with W > 1μm		
Layer		$mA/\mu m$
poly	J_p	?
metal1	J_{m1}	5.4
metal1-4	J_{m2-5}	7.8
metal6	J_{m6}	21

Contact resistance		
Layer-layer		Ω / cnt
metal1-n+ diff	R_{cdn}	15
metal1-p+ diff	R_{cdp}	15
metal1-poly	R_{cp}	15
metaln-metaln+1, via1-4	R_{via1-4}	1
metal5-metal6, via5	R_{via5}	0.5

Max contact current		
Layer-layer		mA/cnt
metal1-poly,diff	I_{cp}	0.6
via1-4	I_{via1-4}	0.9
via5	I_{via5}	3.1

Diffusion cap voltage-dep. parameters				
		nMOS	pMOS	
Bottom junction pot.	V_{jb}	0.47	0.65	V
Bottom grading coeff.	m_{jb}	0.26	0.3	
Sidewall junction pot.	V_{jsw}	0.55	3.1	V
Sidewall grading coeff.	m_{jsw}	0.22	0.06	
Gate sidew. junction pot.	V_{jg}	0.97	0.6	V
Gate sidew. grading coeff.	m_{jg}	0.7	0.9	

Latch-up prevention

1. All wells must have at least one contact to VDD.
2. Place well and substrate contacts whereever possible.
3. Max distance between and well/substrate contact is 30 μm.