Electrical Parameters

Transistor parameters					
	N-type		P-type		Unit
Gain factor (datasheets)	KP_n	175	KP_p	60	$\mu A/V^2$
Gain factor (simulations)	KP_n	110	KP_p	35	$\mu A/V^2$
Threshold voltage (W/L = 10/10)	V_{tn0}	0.50	V_{tp0}	- 0.65	V
Threshold voltage (W/L = 10/0.3)	V_{tn0}	0.52	V_{tp0}	- 0.65	V
Effective channel length (0.3μm)	$L_{eff,03,n}$	0.40	$L_{eff,03,p}$	0.55	μm
Effective channel width (0.6μm)	$W_{eff,06,n}$	0.55	$W_{eff,06,p}$	0.55	μm
Saturation velocity	$v_{sat,n}$	0.118	$v_{sat,p}$	0.200	Mm/s
Body effect factor (W/L = 10/10)	γ_n	0.58	γ_p	0.42	$\sqrt{V}$
Bulk potential	ϕ_{bn}	0.8	ϕ_{bp}	-0.5	V
Resistance, active region (sim.)	r_{ds_n}	$30 \cdot 10^6$	r_{ds_p}	$30 \cdot 10^6$	$\Omega\mu$A/μm
Saturation current (0.3μm)	I_{sat_n}	520	I_{sat_p}	240	μA/μm
D-S breakdown volt. (0.3μm)	V_{bkn}	> 9	V_{bkp}	< -9	V

Capacitances (layer to substrate)				
	Area $fF/\mu m^2$		Perimeter $fF/\mu m$	
gate capacitance	C_{ox}	4.60		
gate-diff overlap			C_{gdo}	0.21
gate-bulk overlap			C_{gbo}	0.11
n^+ diffusion (0V)	C_{jn}	0.93	C_{jnp}	0.28
p^+ diffusion (0V)	C_{jp}	1.42	C_{jpp}	0.38
N_{well}-bulk (0V)	C_{jw}	0.11	C_{jwp}	0.53
poly1	C_{p1}	0.119	C_{pp}	0.049
metal1	C_{m1}	0.034	C_{m1p}	0.046
metal2	C_{m2}	0.013	C_{m2p}	0.017
metal3	C_{m3}	0.008	C_{m3p}	0.011
poly1-poly2	C_{poly_s}	0.86	C_{poly_p}	0.092

Sheet resistance		
Layer		$\Omega/\square$
metal3	R_{sm3}	0.04
metal2	R_{sm2}	0.07
metal1	R_{sm1}	0.07
poly1	R_{sp}	9
n^+ diff.	R_{sdn}	80
p^+ diff.	R_{sdp}	160
n-well	R_{nw}	1000

Max. current density		
Layer		mA/μm
metal3	J_{m3}	1.5
metal2	J_{m2}	1.0
metal1	J_{m1}	1.0
poly1	J_{poly1}	tbd

Max. contact current		
0.4μm$\times$0.4μm contact 0.5μm$\times$0.5μm via, via2		
Layer–layer		mA
metal3–metal2	I_{via2}	0.9
metal2–metal1	I_{via}	0.6
metal1–poly1/diff	I_{cp}	0.9

Contact resistance		
Layer–layer		Ω/cnt
metal3–metal2	R_{via2}	1.5
metal2–metal1	R_{via}	1.5
metal1–poly1	R_{cp}	3.0
metal1–n^+ diff.	R_{cdn}	25
metal1–p^+ diff.	R_{cdp}	60

Diode data		N	P
Area junc. pot.	V_j	0.69V	1.02V
Sidewall junc. pot.	V_{sw}	0.69V	1.02V
Area grading coeff.	m_j	0.31	0.55
Sidewall grading coeff.	m_{sw}	0.19	0.39

Structural and geometrical parameters		
Gate oxide thickness	t_{ox}	7.5 nm
Poly1–poly2 oxide thickness	t_{pox}	40 nm
Field oxide thickness	t_{fox}	0.290 μm
Poly1–metal1 oxide thickness	t_{pox}	0.545 μm
Metal1–metal2 oxide thickness	t_{mox}	1.00 μm
Metal2–metal3 oxide thickness	t_{mox2}	1.00 μm
Passivation thickness	t_{prot}	0.90 μm
Poly1 thickness	t_p	0.275 μm
Metal1 thickness	t_{m1}	0.67 μm
Metal2 thickness	t_{m2}	0.64 μm
Metal3 thickness	t_{m3}	0.925 μm
n^+ and p^+ junction depth	x_j	0.2 μm
n-well junction depth	x_w	2.0 μm

Latch-up prevention

(1) All wells must have at least one well contact connected to V_{DD}.
(2) Place well and substrate contacts wherever possible.
(3) Max. spacing between well/substrate contacts: 50 μm.

Note: The design rules and electrical parameters presented in this document are representative for a typical 0.3μm CMOS process, and they are intended for teaching purposes only.