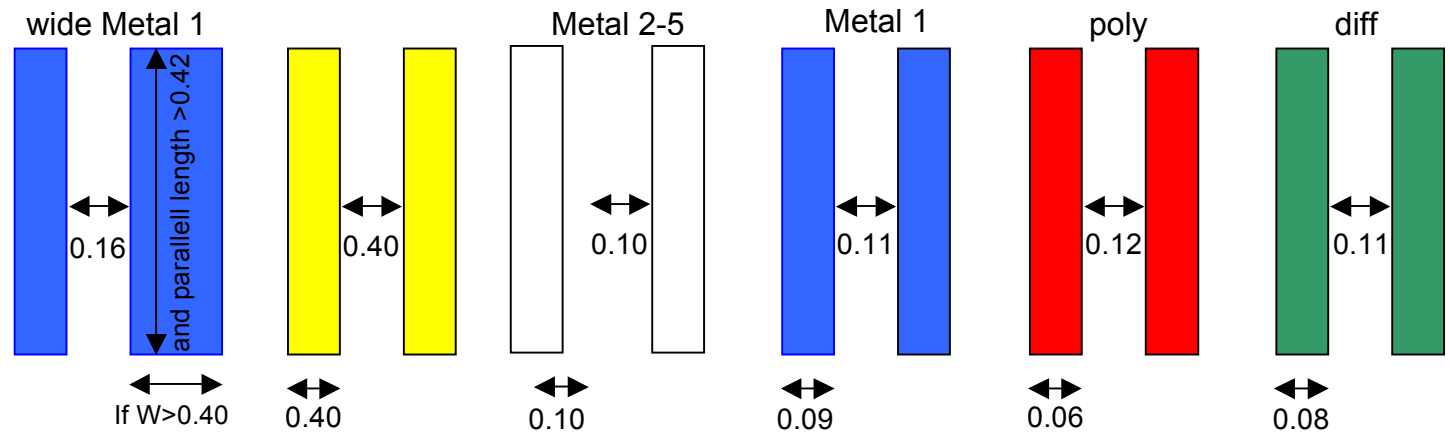
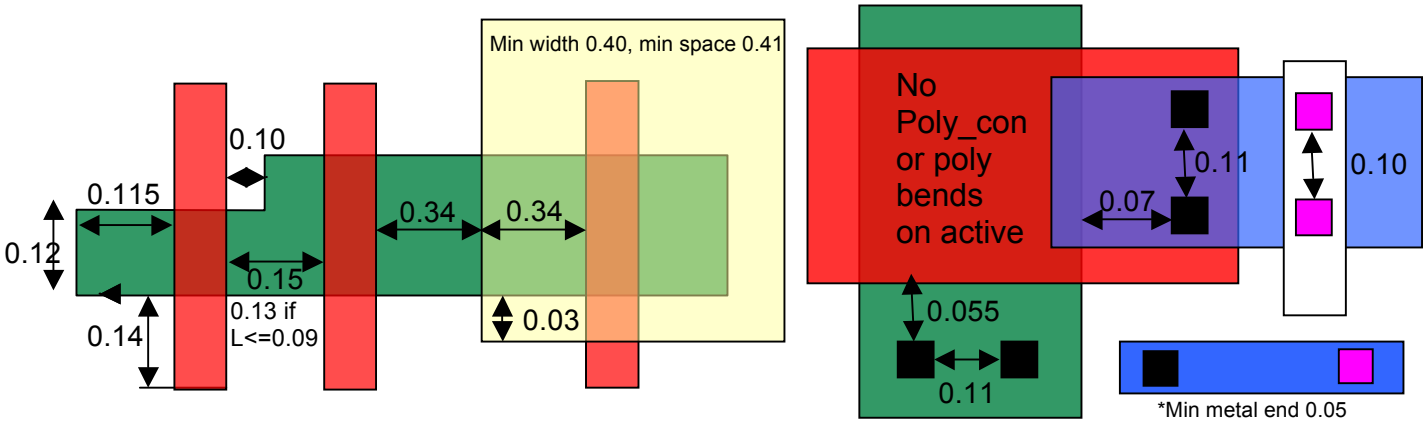
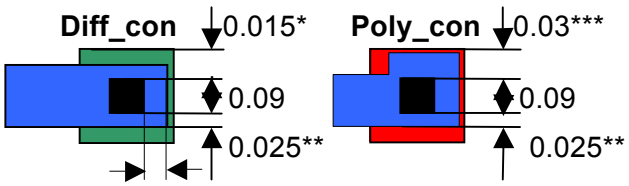
Geometric design rules for 65 nm CMOS





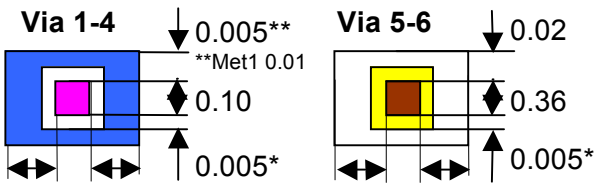
Contact & via rules

All contact and via sizes are exact measures



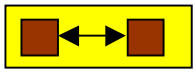
*Two opposite sides at least 0.03 enclosure
**If two opposite metal ends enclose 0.04 then 0.0 OK on remaining

***If two opposite poly ends enclose 0.04 then 0.01 OK on remaining



At least two 0.05 metal ends on metal pad

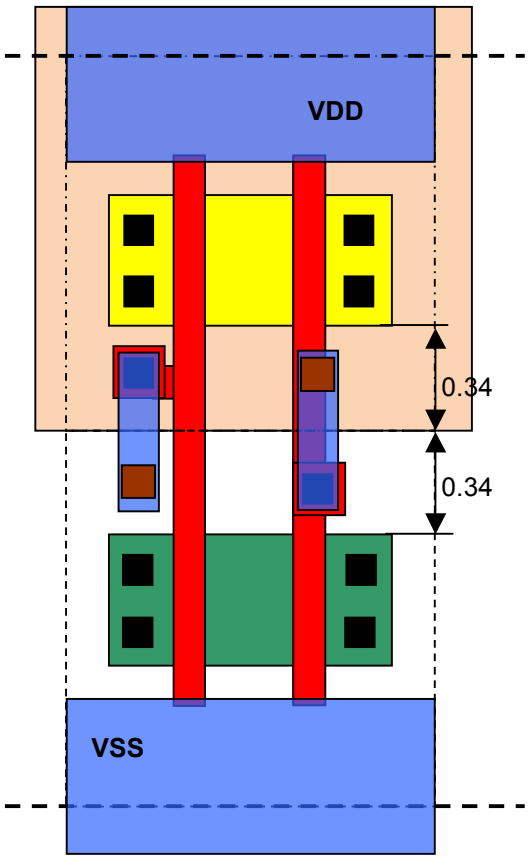
At least two 0.08 metal ends on metal pad



0.34 (min 0.54 in array)

Standard cell template

with rails, well, pplus and nplus design rules



1. Well		
1.1	Width	0.47
1.2	Space (same potential)	0.47
	Space (different potentials)	1.00
2. Active (Diffusion)		
2.1	Width	0.08
2.2	Space	0.11
2.3	Source/drain spacing to well	0.16
2.4	Source/drain margin to well	0.16
2.4	p-active spacing to well	0.16
2.4	n-active margin to well	0.16
3. Poly		
3.1	Width	0.06
3.2	Space	0.13
3.3	Gate overlap of active	0.14
3.4	Active overlap of gate	0.115
3.5	Field poly to active	0.10
4. Select (pplus and nplus)		
4.1	Select space (overlap) to (of) channel	0.16
4.2	Select space (overlap) to (of) active	0.13
4.3	Select space (overlap) to (of) substrate contact	0.02
4.4	Min width and space	0.18
5. Contact to poly: NO CONTACTS ON GATES!		
5.1	Contact size exactly	0.09x0.09
5.2	Spacing to other contacts (shorted)	0.11
	Spacing in array	0.14
5.3a	Poly overlap, all sides	0.03
	or Poly overlap, two opposite sides/other sides	0.04/0.01
5.4	Metal1 overlap all sides	0.025
	or Metal 1 overlap to sides/other sides	0.04/0.0
5.5	Spacing to active	0.14

6. Contact to active		
6.1	Contact size exactly	0.09x0.09
6.2	Spacing to other contacts (shorted)	0.11
	Spacing in array	0.14
6.3	Active overlap two opposite sides/other sides	0.03/0.015
6.4	Metal1 overlap, all sides	0.025
	or Metal1 overlap, two sides/other sides	0.04/0.0
6.5	Spacing to gate	0.055
6.6	Spacing to select	0.06
6.7	Margin to select	0.06
7. Metal1		
7.1	Width	0.09
7.2	Space short run (< 0.38) and narrow (<0.2)	0.09
7.3	Space longer run (<0.42) and wider (<0.42)	0.11
	or dense configuration	
7.4	Space longer run (<1.5) and wider (<1.5)	0.16
8. Via1. Via2. Via3 and Via4: NO VIAS ON GATES!		
8.1	Via size exactly	0.10x0.10
8.2	Space to other vias in same layer	0.10
	Space in array	0.13
8.3	Overlap by bottom metal	0.005
8.4	Overlap by top metal	0.005
9. Metal 2 to Metal 5		
9.1	Width	0.10
9.2	Space	0.10
9.3	Space to short metal	
10. Metal 6 to Metal 7		
9.1	Width	0.40
9.2	Space	0.40

65 nm CMOS Design Rules