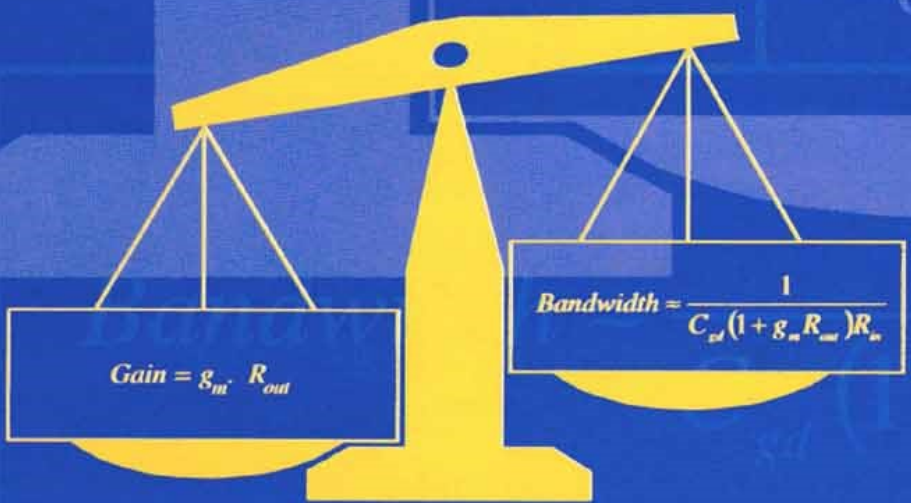
Trade-Offs in Analog Circuit Design

The Designer's Companion

Edited by
Chris Toumazou, George Moschytz
and Barrie Gilbert



Editing Assistance
Ganesh Kathiresan

Kluwer Academic Publishers

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Foreword

With so many excellent texts about analog integrated circuit design now available, the need for yet another compilation of contributions may be questioned. Nevertheless, this book fills a notable void, in addressing a topic that, while a common aspect of a product designer's life, is only occasionally addressed in engineering texts. It is about Trade-Offs: What they are; the circumstances in which they arise; why they are needed; how they are managed, and the many ingenious ways in which their conflicting demands can be resolved. We call it a Designer's Companion, since it is more in the nature of a reference work, to dip into when and where some new perspectives on the topic are needed, rather than a text to be read in isolation and absorbed as a whole. However, it is an aspect of a trade-off that it is peculiar to each situation and there are no recipes for their instant resolution. That being true, their treatment here is frequently by example, suggestive rather than definitive. The personal insights, intuitions and inventiveness of the designer remain vital to the pursuit of a well-balanced solution, but which is even then only one of many, so its selection requires a relative-value judgment.

Understanding how to cope with trade-offs is an indispensable and inextricable part of all engineering. In electronics, and particularly in analog design, the dilemmas arise in the choice of basic cell topology, its biasing, the specific element values and in making performance compromises. For example, wireless communication systems are becoming increasingly sophisticated: they must operate at ever higher carrier frequencies, while using increasingly complex modulation modes, and posing extremely stringent performance demands. Meeting these requirements is only made more difficult as the dimensions of transistors and passive elements in modern IC processes continue to shrink, and as time-to-market and cost pressures mount. Similar trends are found throughout the field of electronics: in power management, fiber-optics, clock generation for CPUs, high-precision instrumentation for signal generation and metrology, and in analytical equipment of numerous kinds in science, industry, medicine and more recently in forensics and security.

Simply stated, the need for a trade-off is generated by the dilemma of being faced with a multiplicity of paths forward in the design process, each providing a different set of benefits or posing different risks, and which can only be resolved by giving up certain benefits in exchange for others of comparable value. The trade-off invariably generates a constellation of considerations which are specific to each situation, within a particular design context and set of circumstances that will often have never occurred before, and whose resolution will have little general applicability.

It is these latter features that make writing about trade-offs so difficult: they are not easy to anticipate in a systematic treatment, and they don't teach lessons of universal applicability. Furthermore, a trade-off calls for creativity: it requires us to provide what isn't there, in the data. Trade-offs cannot be made by tossing a coin; they are rarely of an either-or character to begin with. The longer one mulls over the unique particulars, the more likely it is that a panoply of solutions will present themselves, to be added to

one's bulging list of options. At some point, of course, ingenuity has to be curbed, and a decision has to be made.

Edward de Bono has noted that "In the end, all [human] decisions are emotional". In resolving a trade-off, our intervention as laterally thinking, resourceful individuals is not required if the facts unequivocally speak for themselves, that is, if the resolution of a transient dilemma can be achieved algorithmically. It involves selecting one from several similarly attractive choices. We invariably try to apply all sorts of wisdom and logic to our choice of which car or house to buy; but when logic fails to force the answer, as it so often does, we fall back on emotion. The essential role of emotion as an intrinsic part of rational intelligence and an ally to creative thought has recently been illuminated by a few pioneering psychologists. Intriguingly, in the index to Antonio Damasio's 1994 book *Descartes' Error,* one finds the entry "Decision making: see *Emotion*". Coping with trade-offs also requires the inquisitive anticipation of the circumstances in which they may arise, and a good deal of practice in playing out *What If?* scenarios. Joel Arthur Barker[1] makes this observation, in which we may want to substitute "the next IC development" in place of "the new worlds coming":

> Some anticipation can be scientific, but the most important aspect of anticipation is *artistic.* And, just like the artist, *practice and persistence* will dramatically improve your abilities. Your improved ability will, in turn, increase your ability in dealing with the new worlds coming. [Emphases added]

Although often referred to as "an art" in casual conversation, circuit design is more correctly viewed as a craft. The central emphasis in formal treatments of integrated circuit design is generally on acquiring a thorough knowledge of the underlying electronic principles, and of semiconductor processes and devices, aided by a fluency in mathematics, familiarity with the particular domain of specialization under consideration, and a basic ability for applying various pre-packaged concepts, techniques and algorithms. But this hides the importance of developing the knack of making all the right judgments in practicing this craft, and the value of cultivating a personal flair in coping with the realities beyond the covers of the textbook.

Contrarily, from the layman's perspective, design is perceived as a linear intellectual process, which proceeds something like this: One is faced with a set of objectives, and then calls on experience to assemble all the pieces in a methodical, step-by-step fashion, making fact-driven decisions along the way. As each part of the product is considered, logic prevails at every juncture, and the whole gradually takes on a shape that is as optimal as it is inevitable, to become another testament to the power of the underlying rules and theories.

As a seasoned product designer, you will know that from the outset this will be far from the reality. Inspired guesses (more charitably labeled "engineering judgments")

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[1] Joel Arthur Barker, *Paradigms: The Business of Discovering the Future,* 1994. This highly recommended work was previously published in 1992 under the title *Future Edge.* By that time anything with the word "Future" in its title was already becoming passé, so perhaps it enjoyed only lackluster sales. By contrast, "Paradigms" was a very marketable word in 1994.

are scattered all along the path, from start to finish. To begin with, those Objectives, that are supposed to inform every step of the proceedings and give the development a sure sense of direction, are either insufferably detailed and give one a feeling of being imprisoned in a straightjacket, or they are so comically sketchy and perhaps mutually inconsistent, that anything approaching a focused, optimal solution is out of the question. Regrettably, as your own experience may testify, both of these extremes are all-too common, as well as every flavour in between. Each in its own way is mischievously setting the stage for the first trade-off to be needed.

In the over-constrained scenario, one designer may be inclined to take a stab at satisfying the provider of the objectives with the desired results, no less, but no more, either: a just-right solution. This could be unwise, however, since the writer of these specifications might be viewing the development in a way that is strongly influenced by a prior discrete-element solution, and could be unaware of the special advantages that can be provided by a monolithic implementation. On the other, this tactic might be the right one if the product needs to meet only this one customer's need, and development time is severely limited, and die cost must be minimized. Another designer might adopt the opposite rationale: Sure, the product will meet all those fussy requirements, but it could be capable of doing a lot more, too. By skillful design, many additional applications and features can be anticipated, and the versatility extended to embrace these, for little extra design effort or manufacturing cost. Thus, each of these two designers is making a trade-off, right at the start, about how to interpret and react to the challenge implicit in the specifications.

Similarly, when faced with scant information about what is needed of this new product, one designer's approach might be to opt for caution, and painstakingly solicit more detailed information from the provider of the objectives. This only generates another trade-off, since the provider/user may in fact be no more informed than the designer; but, perhaps to hide his ignorance, he will nonetheless generate more numbers based on estimates and prior practice, in other words, more guesses. If these are received and acted on with unmerited respect, the outcome could be a disaster. Alternatively, if they are treated with disdain, and another set of guesses is substituted, the outcome could be equally undesirable.

Meanwhile, a second designer may lean on her specialized experience with similar products, and assume that the missing information can be adequately interpolated, without the need for any further consultation. That tactic could work out well, or it could be just the beginning of a monstrous headache for both the potential user and the designer. In all these scenarios, it is painfully evident that the tools needed for resolution of this particular dilemma will be found in no text book (including this one!) and they each in their own way call for a trade-off to be made. And this before the design has even begun.

These sketches also make us aware of the arbitrariness of the trade-off. It's an idiosyncratic response to a dilemma. The more practiced the engineer, the more likely it is that the majority of the hundreds of trade-offs that eventually will have to be made, during the course of developing even a relatively straightforward analog circuit, will be based on good judgment, and a balanced consideration of all the alternatives that came

to mind. But we cannot say that these decisions will be entirely rational, or optimal. There are no algorithms for success.

This book covers ten subject areas: Design Methodology; Technology; General Performance; Filters; Switched Circuits; Oscillators; Data Converters; Transceivers; Neural Processing; and Analog CAD. It addresses a diversity of trade-offs ranging from such well-known couplets as frequency versus dynamic range, or gain-bandwidth vs power consumption, or settling-time vs phase-noise in PLLs, to some of the more subtle trade-offs that arise in design for robustness in manufacture and in the "polygon world" of IC layout. During its several years in development, it has transcended its original scope, becoming a designer's desktop companion while also having value as a graduate textbook, inasmuch as numerous fundamental relationships leading to design conflicts are explained, in many cases with practical examples.

Its thirty-three chapters come from a variety of sources, including some of the world's most eminent analog circuits and systems designers, to provide, for the first time, a timely and comprehensive text devoted to this important aspect of analog circuit design. Those authors who are professional designers are faced every day with difficult decisions on which the success of their products depend, and not always with all the analytic horsepower that may be demanded by some of the situations. Taken in aggregate, the trade-offs that they choose eventually shape the competitive stature and reputation of the companies for whom they work. Other authors allow themselves to take a more academic view of the nature of a trade-off, and as a group are more inclined to have greater optimism about the amenability of challenging circumstances to yield to formal approaches, and even a degree automation.

The first section on Design Methodology opens with a discussion by Toumazou about the nature and value of qualitative reasoning, in contrast to the usual emphasis in engineering on the towering importance of quantitative analysis. The underlying need for intuition, playful inventiveness and emotion in the pursuit of an engineering life is picked up by Gilbert, in Chapters 2 and 33, although the more serious focus here is nonetheless on making decisions within the context of commercial product development. In all these chapters, the sheer breadth of the field allows only an introduction to the subject matter.

The next three chapters, in the Technology section, range from the "Big Picture" of VLSI, and in particular, some of the trade-offs in CMOS circuit development, as explored by Mezhiba and Friedman, to the specific and detailed topic of bandgap voltage references, as perceived by Staveren, Kouwenhoven, Serdijn and Verhoeven (Chapter 5). Perched between these two chapters is a presentation of the less-familiar floating-gate devices and circuits that have a unique, although limited, scope of applications and might also comfortably fit into the later (and short) section on Neural Processing, in Chapter 30 of which Hanggi, Dogaru and Chua discuss specialized trade-offs in integrated neural networks.

In some cases, the emphasis is on the tension between two dominant aspects of performance. This approach is particularly evident in the five chapters about General Performance issues. A very basic trade-off is that which arises between amplifier bandwidth and gain; this is discussed by Toumazou and Payne in Chapter 7, and from a different perspective by Meyer in Chapter 8. Aspects of frequency compensation

in integrated amplifiers is explored in Chapter 9, by Staveren, Kouwenhoven, Serdijn and Verhoeven. In amplifier design, one cannot increase bandwidth without regard for noise, and this in turn is strongly influenced by the power consumption that one can afford to assign to the amplifier. Noise and bandwidth are likewise linked by device geometry. Attempts to push bandwidth may impact DC offsets or gain accuracy in certain cases, or distortion and intermodulation in others. Thus, trade-offs are usually multi-faceted, and in a very real way, nearly all the key specifications that will appear in a product data sheet will be linked to a considerable extent. Vittoz and Tsividis face up to these harsh realities in Chapter 10.

In the section on Filters, the many conflicts and compromises that surround continuous-time active-filter design are addressed by Moschytz in Chapter 11, and by Fox in Chapter 12. The particular way in which trade-offs arise in Log-Domain (Translinear) Filters is discussed by Drakakis and Burdett in Chapter 13. The next section is about Switched Circuits in general, and includes four differing perspectives. The optimization of comparators is the focus of Chapter 14, by Rodríguez-Vázquez, Delgado-Restituto, Domínguez-Castro and de la Rosa, while a general overview of switched-capacitor circuits is presented by Baschirotto in Chapter 15, followed by a review of the compatibility of such circuits with advanced digital technologies, provided by Leelavattananon. This section closes with Chapter 17, which offers some thoughts by Hughes and Worapishet about the differences and trade-offs that arise between the standard switched-capacitor circuits that are now well established and the less well-known switched-current forms that are sometimes viewed as equally useful, in certain situations.

Communications circuits are a minefield of trade-offs, and the very stringent performance required of Oscillators are examined in the Chapters 18 and 19 of this section. In the first, by Ham, some of the special problems of maintaining low phase-noise using the relatively poor on-chip components (principally low-Q inductors and lossy varactors of limited range) are put under scrutiny. A different perspective on the same subject is provided by Hajimiri. The next three chapters, in the section on Data Converters, provide insights from the foremost exponents of these extremely important gateways between the analog and digital domains. The first, which sets forth principles for the systematic design of high-performance data converters, is authored by an impressive team composed of Gielen, Vandenbussche, Van de Plas, Daems, den Bosch, Steyaert and Sansen. The following Chapter 21 is more specialized in its approach: Gielen and Lauwers discuss particular issues of power modeling for data converters and filters. Chapter 22, authored by Schreier, Steensgaard and Temes, provides a definitive account of the fundamental trade-off between speed and dynamic range in over-sampled converters.

The focus next shifts to Transceivers, in several very different arenas. In Chapter 23, Abidi shares his considerable experience in the design of wireless circuits, and the systems of which they are an integral part, where power conservation is a dominant concern. This is followed by a review by Forbes of the design trade-offs that arise in optical receivers. Finally, Chapter 25 closes this section with some considerations for analog front-ends in digital subscriber-line systems. In all these cases, the overarching challenge is the attainment of a very high dynamic range, entailing the simultaneous

provision of low distortion, of various disparate types, with a near-fundamental noise floor. The endless search for low noise is also featured in Chapter 26, as illuminated by Kouwenhoven, Staveren, Serdijn and Verhoeven, and again, noise and intermodulation are the central challenges in mixer design, the topic of the next chapter by Kathiresan and Toumazou. Phase detectors once bore a passing resemblance to mixers, and their close cousin, the analog multiplier; but in today's phase-locked loops, there is a more pressing need to capture both phase and frequency information. Some special techniques are presented by Li and Ismail. The closing chapter of this section, authored by Chan, Tu and Toumazou, looks at the trade-offs that arise in the design of various sorts of power amplifiers.

The final section is concerned with CAD for analog design. Chandra and Roberts present an overview of a design methodology for analog circuits using Matlab and Simulink, while in Chapter 32, Gielen adds a concluding word about the possibilities for using symbolic analysis tools for analog circuits.

Clearly, no book on the topic of trade-offs can ever be truly representative of the entire field of analog design, nor exhaustive in its treatment of those subjects which do get included. The primary function of any engineering text is to inform, and provide accurate and authoritative guidance of both a general and specific sort. However, as earlier suggested in this Foreword, and as these chapters testify, it is unlikely that very many general recommendations can be made regarding trade-offs, and the specialized case histories have a strictly limited scope of application. But another function of any good text is to enthuse, to inspire, to illuminate the less-explored corners of the domain, and to point the way to new perspectives on each topic. It is hoped that the material assembled here serves that objective.

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Chapter 1

INTUITIVE ANALOG CIRCUIT DESIGN

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1.1. Introduction

This chapter is concerned with ideas and methods for a teaching approach that has been developed to provide insight into, and aid creativity in, the process of analog circuit design. This approach is modeled on the way the authors see circuit designers acting as cognitive agents, namely qualitatively, intuitively, abstractly and in knowledge-rich and formalism-poor fashion. This can be contrasted with the formal mathematical approach, the tool employed by designers once an understanding has been reached of the design problem at hand.

Analog design is a knowledge intensive, multiphase and iterative task, which usually stretches over a significant period of time and is performed by designers with a large portfolio of skills. It is considered by many to be a form of art rather than a science. There is a lack of an analog circuit design formalism: there is neither circuit-independent design procedure for analog circuits, nor is there a formal representation (the equivalent of a Boolean algebra) that allows a formal mapping of function to structure (i.e. that produces, from a specification of required circuit behavior, a circuit that realises this behavior). The main obstacle to such developments is the nature of the analog signals that the circuits deal with, namely the continuous-time dependency. The techniques needed to generate successful analog circuits cannot be normally found in textbooks, but exist mainly in the form of experience and expertise gained by relatively few designers. The reason this is so is that they have essentially compiled knowledge of function-to-structure mappings from years of experience. Thus, candidate solutions can be applied easily to help provide an initial approximate mapping to which formal tools (e.g. simulators) can be applied to produce an accurate solution. This can be seen as the approach a designer takes to a non-discrete problem domain: dealing with the domain of natural numbers is formalizable into a logical system, dealing with the continuous domain requires the application of calculus and is inherently explosive in terms of complexity. However, if partial solutions are available, approximate solutions can be reached that can be automatically fine tuned in the domain of real numbers.

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1.2. The Analog Dilemma

Growing requirements for single-chip mixed VLSI designs, together with pervasive trends toward smaller feature sizes and higher scales of integration, have brought about new dimensions in circuit design complexity. Whereas the design of digital circuits is well supported by sophisticated computer-aided design (CAD) tools, the same cannot be said of analog CAD tools in several important respects. In particular, the precision to which analog circuits are to be designed, coupled with the growing need for more analog system simulation, has generally meant that the design time for analog circuits is significantly greater than the design time for digital circuits. Although 90% of an integrated circuit may be digital and only 10% analog, most of the design time and effort is devoted to the analog part.

However, there is much research and development currently taking place and powerful simulators and semi-automated CAD tools are now beginning to reduce this analog bottleneck. There is still one very important aspect of analog circuit design that these tools do not address. Although simulators may present numerical data to the designer, they do not interpret the meaning of the data nor do they reduce the number of simulations required in order to gain an understanding of or (intuitively speaking) "feel" for the behavior of a circuit. Circuit designers will, therefore, generally have to modify and simulate a circuit several times before they finally achieve satisfactory circuit behavior. It should be noted that the designer at this stage is not necessarily concerned with the exact value of a parameter, but rather the search for the set of orthogonal design parameter changes and/or circuit topology modifications that would eliminate the difference between the desired performance and that simulated. An expert will know these trade-offs for a given circuit. As presently conceived, simulators do not automate this process of assigning meaning to a structure.

The above problem raises the issue of the trade-off between design time and design accuracy. The requirement for circuit correction, together with the requirement to provide useful insight into the operation of the circuit, precludes the use of numerical optimizers or fully automated CAD systems (at least as they are presently conceived). This is where the design experience of the analog designer is important and obviously has a major effect on the proportion of analog to digital circuitry in the resulting chip.

Possibly the future will bring an automated CAD tool to every designer's desk (though such a tool may well require significant advances in computer science) but human intervention for observation, control and the provision of circuit insight and understanding may well be unavoidable for the foreseeable future. These issues have in general been recognized in computer science, partly because researchers have begun to appreciate the enormous difficulties that arise when they attempt to automate a cognitive task and partly because

Table 1.1. Designer's "thumbs table."

Increase	Geometry		Electrical biasing	
	W	L	I_D	$V_{gs} - V_T$
A	$\surd\uparrow$	$\surd\downarrow$	$\surd\downarrow$	$\downarrow$
g_m	$\surd\uparrow$	$\surd\downarrow$	$\surd\uparrow$	$\uparrow$
g_o	—	—	$\uparrow$	$(\uparrow)^2$

any tool that fully automates the cognitive parts of design will cease to be a tool and become a challenge to the designers themselves: the aspects of analog design that have been formalized are essentially those mundane and difficult tasks that any designer is happy to have (and, given the complexity of today's circuit, needs to have) taken away from him or her.

The approach that some of the editors have adopted while teaching analog circuits is the "less maths, more thumbs approach" or, to be more formal, less quantitative and more qualitative analysis. The term "thumbs" personifies the sense of a "feel for" a "rule of thumb" (or heuristic), or "thumbs up" (meaning success). Table 1.1 is an example of a "thumbs table".

The example relates the effect of a reduction or increase of a certain design parameter upon particular aspects of circuit performance. For example, to increase gain A, one can increase the transistor gate width, reduce the transistor gate length or reduce transistor bias current. The proportionality in each case is a square root, but it is not always necessary to show this.

The thumbs table is based on first-order design equations. In Table 1.1, the relationships refer to the small signal parameters of a single MOSFET. For example, A, which equals g_m/g_o is the intrinsic open-circuit voltage gain of the FET, g_m being its transconductance gain and g_o its output conductance. An arrow pointing up indicates an increase whereas an arrow pointing down indicates a decrease of a particular performance parameter. This is determined by the signum of a partial derivative of the performance parameter with respect to a design parameter; for example, the sign of $\partial A/\partial W$ is positive, which is indicated by an arrow pointing up in the thumbs table. It should be noted that it is not the complete sensitivity of the performance measure to parameter that is required here. The thumbs table can be extended to all types of circuits and systems. More detailed sensitivity is discussed in Chapter 12.

Figure 1.1 (b) shows a slightly different representation of a thumbs model for various performance measure figures of the two-stage CMOS operational amplifier (op amp) shown in Figure 1.1 (a).

The performance figures in this case, from left to right, are slew rate (SR), voltage gain (V gain), phase margin (phase M) and gain–bandwidth (GB)

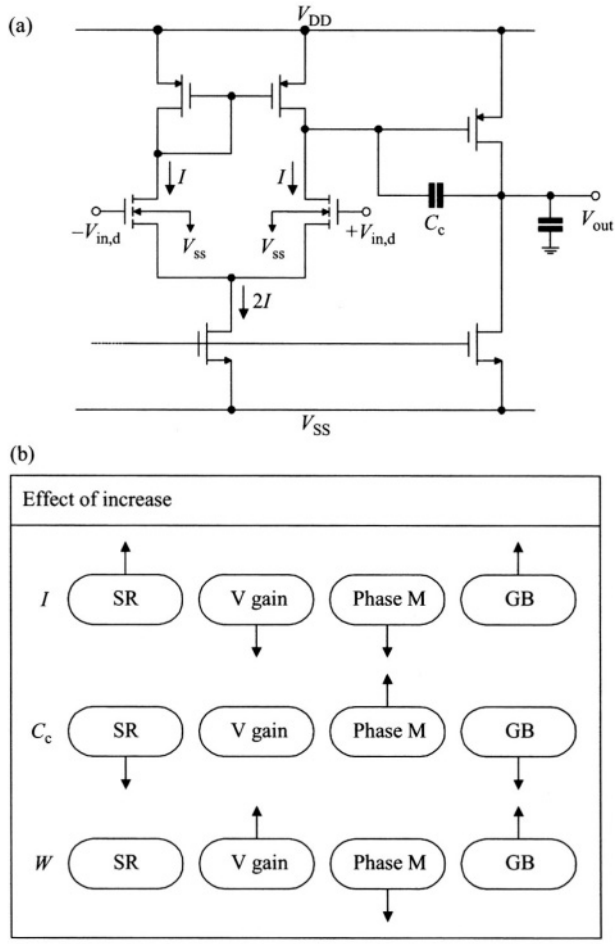


Figure 1.1. (a) Two-stage operational amplifier and (b) its "Thumbs model".

product. The design parameters from top to bottom are the differential-pair bias current (I), the compensation capacitance (C_c) and the width (W) of the input differential-pair transistors.

The following design scenario illustrates the power of such a model. Assume that, when simulated, the voltage gain and phase margin have not met their specifications. However, the designer has observed that the slew rate and GB product are well within specification, so although he or she is satisfied with their values as a first priority, he or she is willing, if necessary, to sacrifice some of the margin by which they exceed the specification, as a second priority, in order to meet all the specifications.

Below is a typical chain of thought of a circuit designer attempting to correct this design:

> *Comment.* The voltage gain can be improved by increasing the width (W) of the input transistors. This will reduce the phase margin because of the consequential increase in the amplifier's GB product. To increase the phase margin, we can now increase the compensation capacitor C_c: this will not affect the voltage gain but will reduce both the slew rate and the GB product. I do not mind trading off the slew rate and the GB product, therefore this is a scenario that is moving in the right direction towards meeting all the specifications with two parameter changes. If, on the other hand, the differential-pair current is reduced, both the voltage gain and the phase margin of the amplifier will increase, but still at the expense of the slew rate and the GB product. The simplest solution (i.e. the solution with the minimum number of modifications and side-effects) is, therefore, to reduce the bias current of the first stage.

It should be noted that the designer is not dealing with real numbers at this stage. In fact, in the above example, it may well be that the performance requirement is not numerically satisfied and so at that stage the designer may have to go through another qualitative correction. The designer is always in search of the most orthogonal procedure. Several other important and useful deductions can be made from the circuit designer's reasoning. First of all, the model of Figure 1.1 (b) uses knowledge specific to the failed performance measures. For instance, in the model the designer can see that, in order to improve the slew rate of the amplifier, he or she has either to increase the long-tail-pair current or to decrease the compensation capacitance. Such knowledge, which is derived from first-order design equations, provides an enormous advantage over blind numerical techniques as it reduces the solution space for exploration. Moreover, the assessment of the various alternative solutions to the correction problem is shown to be based upon the effects the design parameter adjustments have on other aspects of circuit performance. The preferred solution is the one that with a minimum number of design parameter adjustments improves all the performance figures that have failed to reach specification without deteriorating any others.

The fundamental formulation of the analog integrated circuit design process using qualitative reasoning is very timely in view of the much increased complexity of the analog design process, and the consequential need for systematic and well reasoned assistance, simplification, insight and creativity.

Much research has aimed to automate the qualitative design, or "thumbs", approach and this has led to novel concepts in automated circuit design and circuit correction [1,2].

In this book, we have captured the thumbs of some of the worlds best analog designers. Trade-offs in the design of band-gap references through to DSL architectures are some of the examples covered in this book.

References

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Chapter 2

DESIGN FOR MANUFACTURE

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2.1. Mass-Production of Microdevices

We generally think of mass production as a uniquely twentieth-century phenomenon. However, its evolution can be traced back much further. The explosion in printed books, following Johannes Gutenberg's fifteenth-century development of the Korean invention of movable type, had an impact on human society of heroic proportions. Precursors of modern mass-production, based on the *specialization of labour* and the *use of specialized machinery* to ensure a *high degree of uniformity,* can be traced to the eighteenth century. Writing in *The Wealth of Nations* in 1776, Adam Smith used the manufacture of pins to exemplify the improvement in productivity resulting from the utilization of uniform production techniques. Today, every conceivable sort of commodity is mass-produced. Pills, paints, pipes, plastics, packages, pamphlets and programs are mixed, extruded, poured, forged, rolled, stamped, molded, glued, printed, duplicated and dispatched worldwide on an immense daily scale. The most successful modern products are an amalgamation of many disciplines, years of experience, careful execution, rigorous production control and never-ending refinement.

In no other industry is the cross-disciplinary matrix so tightly woven, and the number of interacting elements so incredibly high, as in the semiconductor business. Reaching back to Gutenberg, and drawing on the principles of photography pioneered by Daguerre in the 1830s (embracing optics, lens-making, photosensitive films and chemistry), transistors are defined by a process of lithography, which is essentially *printing.* But what eloquent printing this is! A 200-mm silicon wafer has a useful area of about 200-cm^2, a little less than a page of this book containing some 400 words of text, equivalent to perhaps 16,000 bits. However, when divided into 1-cm^2 chips - the size of a modest microprocessor, today containing about 50 million transistors, through perhaps 20 successive layers of printing and processing - each wafer generates some 10 billion devices in a single mass-produced entity. In a production lot containing 40 such wafers, some 400 billion tiny objects are manufactured in a single batch. Multiply this by the daily manufacture of integrated circuits worldwide, and it will be apparent that the number of transistors that have been produced

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since the planar process was invented[1] runs to astronomical proportions far exceeding the expectations of its most optimistic and visionary progenitors.

Indeed, it is hard to identify any other mass-produced object that is fabricated in such prodigious quantities as the transistor. Even pills are not turned out in such numbers, and even when molecularly sophisticated, a pill remains a primitive amorphous lump of material. A transistor has a *complex fine-scale structure,* having a distinctive personality of its own (and a devious one: try modeling an MOS transistor!). Its near-perfect crystalline structure at the atomic level, and its precise dimensions and detailed organization at the sub-micron level, are fundamental to its basic function. No less important is the way these cantankerous virus-scale devices are tamed, teamed up and harnessed, in the *design of micro-electronic circuits.*

As their designers, we are faced with exciting opportunities and challenges. It is our privilege to turn essentially identical slabs of silvery-grey silicon – the stuff of mountains and the earth's most plentiful solid element – into clever, highly specialized components of crucial importance to modern life, handling everything from deceptively simple signals (voltages and currents, time intervals and frequencies) in analog ICs, all the way up to sophisticated packets of mega-information in computers and communication systems. Each of our creations will elicit uniquely different behaviour from the same starting material, and possess a distinctive personality of its own. How we shape this little piece of silicon, and the assurance with which it goes forth into the world and achieves its diverse functions, is entirely in our hands.

Integrated circuit designers who experience the rigour of dispatching their products to manufacturing, and watch them flourish in the marketplace and subsequently generate significant revenues for their company, soon discover that their craft entails a balanced blend of technique and judgment, science and economics. The path from concept to customer is strewn with numerous pitfalls, and it is all too easy to take a misstep. The practicing designer quickly becomes aware that silicon transistors, and other semiconductor devices, have a mind of their own, demanding full mastery of the medium if one is to avoid falling into these traps. One also learns that a circuit solution, no matter how original, elegant or intriguing, is of little value in abstraction. Cells, which will here be defined as small, essentially analog circuits of up to a dozen or so transistors, are merely *a resource* to be created (or discovered and understood), then tamed, refined and cataloged. Artful cell development is of fundamental importance to robustness in manufacture, but cells are certainly not the proper starting point for a *product* development, whose genesis arises within the context of broad commercial objectives, and which will exploit cell properties selectively

[1] By Jean Hoerni of Fairchild, U.S. Patent 3,025,589, filed May 1, 1959 and issued March 20, 1962.

and judiciously as the need arises. These basic fragments cannot be given any freedom to misbehave, if the products within which they are later utilized are to be manufacturable with high yields and at low cost.

This book is about how to design these basic cells so as to elicit some optimum level of performance, and particularly by considering the many trade-offs that invariably arise in adapting them to a specific use in a product. Such trade-offs are inevitable. Performance is always a compromise reached by giving up certain less desirable aspects of behavior in favor of those other objectives that are identified as essential. When such optimization is pursued with a set of public standards in mind (such as a cellular phone system like GSM), it is exceedingly important to find and utilize the "right" trade-offs, to provide an efficient and competitive design. Where the product is in the nature of a proprietary standard part, the choice of trade-offs may be harder, and involve more judgment and risk, since one often has considerable freedom to improve certain aspects of performance at the expense of others, in pursuing a particular competitive edge, which may be more sensed than certain.

For example, to halve the input-referred *voltage* noise spectral density in a bibolar junction transistor (BJT) low noise amplifier (LNA) one must at least quadruple the bias current.[2] However, this would be of little benefit in a cell phone, where battery power is severely limited, and provided that a certain acceptable noise figure is achieved, further reduction would be surplus to the system requirements. On the other hand, the same benefit would be very attractive in a state-of-the-art *standard product:* it could be the one thing that distinguishes it from all other competing parts. But then, with this increase of bias, the current-noise at the input port will double and that would no longer represent an optimal solution when the source impedance is high. While this is a rudimentary example of the pervasive "noise-versus-power" trade-off, decisions of this kind in the real world are invariably *multi-dimensional:* many different benefits and compromises must be balanced concurrently for the overall performance to be optimized for a certain purpose. It follows that trade-offs cannot be made in abstraction, in absolute terms; they only have relevance within the scope of a specific application.

2.1.1. Present Objectives

This chapter strives to illuminate the path to production a little more clearly, by providing a framework for successful commercial design. While it includes

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2 Specifically, the base–emitter voltage noise spectral density for a BJT due to shot noise mechanisms evaluates to $0.46\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at a collector current I_C of 1 mA, and varies as $1/\sqrt{I_C}$. The current noise at this port, on the other hand, varies as $\sqrt{I_C}$. To these noise components must be added the Johnson noise due to the junction resistances, which does not depend to any appreciable extent on the bias current.

a few illustrative trade-offs, its emphasis on sounding down some more general tenets of robustness in cell design, with high-volume production in mind. The examples are drawn mostly from BJT practice. It outlines some basic cautions we need to observe in our design discipline, including our awareness of the limitations of device models and simulation, and examines the notion of worst-case design. Later, it delineates a dozen work habits of the manufacturing-oriented designer. A brief discussion of some of the ways we can minimize risk and optimize performance through the use of careful layout practices can be found in Chapter 33.

To reach the point of being ready to mass-produce a robust, cost-effective, highly competitive product, we will use many tools along the way. The best tool we will ever have, of course, is the magnificent three-pound parallel processor we carry on our shoulders. Nevertheless, for the modern designer, a circuit simulator, such as SPICE, when used creatively and with due care, can provide deep insights. Many brave attempts, including those of the author in his younger years, have been made to capture design expertise, in the form of programs that automate the design process. These range from such simple matters as calculating component values for a fixed circuit structure, to choosing or growing topologies and providing various kinds of optimization capabilities. Advanced design automation works well in coping with procedures based on clearly-defined algorithms, of the sort that are routine in digital design. However, they have been less successful in aiding analog design, and are of little help in making trade-offs. This is largely because each new analog IC development poses distinctly different design challenges, often calling for on-the-spot invention, since cell reutilization is fraught with problems and of limited value. In this field, as elsewhere, there are no algorithms for success: we must continue to rely on our creativity, our experience, our ability to draw on resources, and our judgment in facing the matter of design trade-offs.

Numerous pitfalls and obstacles will be encountered on the path between the bright promise of the product concept and that moment the IC designer most looks forward to: the arrival of first silicon. But the seasoned engineer knows that these first samples are just the tokens we handle at the beginning of a longer and more arduous journey. Still ahead lie many months of further documentation and extensive testing, during which the glow of early success may fade, as one after another of the specifications is found to be only partially met, as ESD ratings are discovered to be lower than needed on some of the pins, or as shadowy, anomalous modes of operation make unwelcome cameo appearances. There follows the challenge of finding ways to make only minor mask changes to overcome major performance shortfalls; the interminable delays in life test; and the placating of impatient customers, not to mention the marketing folks, who see the window of opportunity at risk of closing.

2.2. Unique Challenges of Analog Design

Such obstacles stand in the way of all professional IC designers, but there are radical differences in individual design style, and between one sub-discipline and another. In the digital domain, the design focuses on assembling many large, pre-characterized blocks, comprising thousands of gates, amounting in all to a huge number of transistors (often known only approximately[3]) each one of which must reliably change state when a certain threshold is reached. Advances in this domain stem largely from improvements in micro-architecture, a relentless reduction in feature size and delay times, and advances in multi-layer metalization techniques, which are also necessary to pack more and more functional blocks into the overall structure, while keeping the chip size and power to manageable levels.

As clock rates climb inexorably into the gigahertz range, the dynamics of these gates at the local level, and the communication of information across the chip, are generating problems that, not surprisingly, are reminiscent of those encountered in classical RF and microwave design. Further, the very high packing densities that are enabled by scaling give rise to new problems in removing the heat load, which, milliwatt by milliwatt, adds up to levels that demand special packaging and sophisticated cooling techniques. Such issues, and the sheer complexity of modern microprocessors and DSP elements, will continue to challenge digital designers well into the century. Their trade-offs will not be addressed here.

The challenges that arise in the domain of analog functions are of a distinctly different kind, and stem principally from two unique aspects of analog circuits. First, there is *much greater variety,* both in chip function, which can take on hundreds of forms, and in the particular set of performance objectives, and even the specification methodology (such as "op-amp" versus "RF" terminology), from one product to another. Second, the actual performance, in all its many overlapping and conflicting facets, *depends on the detailed electrical parameters of every one of the many devices* comprising the complete product, and in a crucial way for a significant fraction of this total. Obviously, it is quite insufficient to simply ensure that a transistor is switched on or off, or even that this transition occurs very quickly and at just the right time; such are only the bare bones requirement of the analog transistor. So much more is now involved in "meeting the specs", and *this parametric sensitivity* touches at the very heart of what makes analog circuits so different from their distant digital cousins.

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[3] Patrick Gelsinger of Intel told me the exact number of transistors in the 486 micropocessor is 1,182,486 (the last three digits were "a coincidence") noting that how one counts devices is somewhat imprecise in the first place.

Much of what we do as designers will require constant vigilance in minimizing these fundamental sensitivities.

Many detailed challenges in signal management face the analog designer. In even a simple cell such as an amplifier, one is confronted with first, the choice of a topology that is both appropriate and robust; then the minimization of noise, distortion, and power consumption; maintenance of accurate gain; elimination of offsets; suppression of spurious responses; decoupling from signals in other sections performing quite different functions; coping with substrate effects; unrelenting attention to production spreads, temperature stability; the minimization of supply sensitivity, and much more.

In the domain of nonlinear analog circuits, special effort is needed to achieve accurate conformance to one or more algebraic functions, such as square-law, product and quotient, logarithmic and exponential responses, and the like. With all nonlinear functions there is also a special need for vigilance in the matter of scaling, that is, control of the coefficients of the contributing terms. Voltage references are often needed, which may need to be exact without recourse to trimming. In filter design, another set of imperatives arises, having to do with ensuring accurate placement of the poles and zeroes of the transfer function even in the presence of large production tolerances. Many modern products combine several of these various functions, and others, in a single chip.

Hard-won analog design victories are known only to a small group of insiders, who are proudly aware of the continual, quiet improvements that so often are behind many of the more visible successes that shape modern communications devices, and which are likely to be bundled with the DSP and microprocessor parts of the system and presented to the public in the guise of yet another advance arising solely from the wondrous properties of digital technologies. One can understand the indifference to analog techniques invariably displayed by the public, but it is worrisome to see this now appearing in the attitudes and skill-sets of new graduates in electronics. Behind all of the glamor that digital systems generate in the popular eye, there is a massive infrastructure of essential analog electronics, and a growing need for skilled analog designers. In the twenty-first century, design challenges with a pure-analog emphasis will not diminish; rather, they will be plentiful. Unfortunately, the number of new engineers available to address these challenges may not keep up with the demand. University students are often led to believe – incorrectly, just like the public at large – the now familiar mantra that "analog is obsolete." This is manifestly false.

These challenges will continue to be related to achieving *small but exceedingly difficult improvements* in certain key parameters, rather than increasing the raw number of transistors that can be crammed into the latest CPU. For example, while a 1-dB improvement in the signal-to-noise ratio of a receiver does not seem very impressive, it typically results in a ten-fold improvement in

the bit-error-rate of a digital channel. It requires considerable inside knowledge to separate the confusing claims made for the latest digital gadget, so persistently and persuasively made by their promoters, from the fact that analog techniques remain important even in the most sophisticated of these products.

The common view is that, by virtue of the certainty of binary data, digital systems avoid the many ambiguities of analog circuits, which have a reputation for being unrepeatable, temperamental, unstable, prone to drift and loss of calibration, or bursting into oscillation without warning. Many of these weaknesses are real, and can be traced to poor design, particularly through inattention to the all-important matter of *robustness* and the *minimization of parametric sensitivities,* which is why there is a need for a book of this sort. Nevertheless, a crucial dependence on the precise values of certain dimensional parameters – for example, those determining the bandwidth of an amplifier – is frequently unavoidable, and unrelenting vigilance is needed during design to ensure robustness in production. Close attention to component tolerances and design margins is essential, and trade-offs must be made carefully.

For example, it is soon discovered that there are inherent trade-offs to be made between achieving uncompromising state-of-art performance on the one hand, while minimizing cost and ensuring a high degree of robustness and chip yield on the other. Since this is true, modern system designers are only being prudent in seeking ways to reduce the "analog front end" to the barest minimum, or even eliminate it; invariably, they are not being unfair in asserting that "This is where our worst problems are to be found." Analog circuits will always be prone to these criticisms, because they are fundamentally closer to the physical reality than are digital circuits. And this is where another key difference is to be found.

2.2.1. Analog is Newtonian

In an important sense, *analog circuits are closer to nature than are digital circuits.* This viewpoint can help us to understand why these two domains of endeavor are fundamentally so different.[4] Certainly, many of the challenges in digital electronics today also have a strongly physical aspect, mostly, although not entirely, at the cell level. But these stand apart from the more important development thrusts relating to the transformation of logical data, rippling through gates which reshape and retime this data, within which the strictures of sequential discrete algorithms replace the unfettered autonomy of the analog

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4 There are actually *three* fields of electronics today: the two major groupings, analog and digital, and a third, smaller but well-defined and rapidly-growing group of techniques which we can call *quasi-analog* or *binary-analog,* exemplified by "sigma–delta" techniques. The three basic disciplines overlap strongly and are co-dependent: they are at once symbiotic and synergistic.

circuit. Once a library of digital cells has been generated, with careful attention to time delays and threshold margins, their inherently analog nature is no longer of interest in digital design.

Analog circuits are more deeply allied to the physical world because they are concerned with the manipulation *of continuous-time, continuous-amplitude* signals, often *of high accuracy,* having *dimensional* attributes, traceable *to fundamental physical constants.* (Logic signals are, of course, dimensionless.) The primary physical units are length [L] in meters, mass [M] in kilograms, and time [T] in seconds, and we here use charge [Q] in coulombs as the fourth basic unit.[5] The *physical algebra* of analog-circuit analysis differs from ordinary algebra in requiring attention to *dimensional homogeneity.* Thus, *voltage* signals embed the dimensions of $[ML^2T^{-2}Q^{-1}]$. Sometimes, greater importance is attached to the signal *currents,* which are of dimension $[QT^{-1}]$. Voltages are just another way of representing *energy* $[ML^2T^{-2}]$ normalized through division by the electron *charge* while current may be envisaged as counting multiples of charge quanta over a specified *time* interval. It follows that *current-mode* signal representation is more prone to absolute-magnitude errors than voltage-mode representation, since in the latter case, scaling can be quite directly traced to such things as the bandgap energy of silicon, the Boltzmann constant *k,* temperature and electronic charge, *q.* Nevertheless, current signals can maintain high *ratio accuracy* and have certain benefits.

Dimensional quantities are inextricably woven into the fabric of the universe, from sub-atomic forces up to the largest cosmic objects. They are also embedded in energy fields. RF signal levels in a transceiver can be equated to an electromagnetic *field strength* at the antenna, and expressed as a *power,* $[ML^2T^{-3}]$, at *some frequency* $[T^{-1}]$. Similarly, the electrical circuit elements within which these signals flourish and propagate have their own set of physical dimensions: *resistance* $[ML^2T^{-1}Q^{-2}]$; *capacitance* $[M^{-1}L^{-2}T^2Q^2]$; and *inductance* $[ML^2Q^{-2}]$. The attribute of *spin,* $[MLT^{-1}]$, is an essential aspect of semiconductor device behavior, as are the *mass* [M] and *velocity* $[LT^{-1}]$ of holes and electrons, and the pure *length, width and thickness* [L] of device structures. In view of this strongly-physical nature of analog circuits, it is not inappropriate to use the term *Newtonian* to describe them.

2.3. Designing with Manufacture in Mind

Designing integrated circuits in a commercial context, one is daily confronted with the need for compromise, expediency and pragmatism – which

[5] The International System of Units (SI) uses the Ampére, rather than charge. Charge is used in the present context because it is an intimate aspect of semiconductor physics.

continually orbit our concerns about development time and product cost – while preserving performance and robustness. These imperatives are rarely addressed in technical university courses. It is common to pursue only those aspects of design which one most enjoys, such as exploiting an exotic new technology, conceptualizing intriguing and bold new approaches, constructing grand system architectures, devising new circuit functions, discovering novel topologies, laying down a fine theory, acquiring a patent or two, or writing a paper for a major conference or professional journal. At times one may lean toward a highly favorable, idealized viewpoint of the task, deferring criticism and "second order effects" for another time. If not careful, one may completely lose sight of the fact that the variables which are so confidently manipulated in spread-sheets and simulations (gain, noise, intermodulation, power, matching and stability criteria, bandwidth, phase margin, frequency, and the like) are but a simplification of harsher realities.

Assailed by all the slings and arrows of outrageous wafer processing, products conceived in the refined conceptual world face a traumatic trial, which only the fittest survive. While intellectually aware that this is so, we may pursue our design work with optimism, in the tacit belief that our devices are basically uniform and predictable, and element variability is only a secondary consideration. Because of the tight controls on the many steps used in a modern IC process, this is not an entirely vain hope. We have come to expect extraordinarily high manufacturing standards and prodigious production yields, often to exacting specifications. Nevertheless, many disappointments can creep into the performance of production components. Some of these are certain but unavoidable; others, while equally predictable, can be averted by the use of thoughtful design practices. Often, we have to sacrifice certain desirable aspects of performance to ensure some others will be met, the essence of a trade-off, which is the central theme of this book.

2.3.1. Conflicts and Compromises

In the world of commercial product design, *performance trade-offs are rarely two-fold in nature.* Certain design conflicts arise in pairs when utilizing a given technology, such as between bandwidth and power consumption, between intermodulation and noise, in balancing the contributions of voltage and current noise, and so on. But these can just as easily be coupled in other ways: noise is in a constant contest with bandwidth; intermodulation distortion can often be lowered only by using higher power consumption; and many aspects of static accuracy are in conflict with achieving high bandwidths. Each design involves complex, multi-variable interactions, and compromises are inevitable.

Good practice demands that adequate consideration is given to every one, perhaps hundreds of such conflicts that can arise during several weeks of design

time, sometimes within the compass of a dozen transistors. Indeed, as we shall see later in this chapter, even a one-transistor LNA can consume a great deal of effort in order to optimize its performance and to be able to guarantee that it will fully meet all of its specifications in every one of millions of future instantiations of the product in which it is embedded.

A thorough understanding of these interactions is the essential starting point in the long road to design mastery in the analog domain. A very basic consideration is that of suppressing, as far as possible, the effects of temperature on circuit behavior. The second most obvious objective is to minimize the impact of changes in supply voltage. And even when suitable countermeasures have been found, and all the fundamental circuit relationships have been aligned in the most optimal manner for a particular set of objectives, there remains the significant hurdle of desensitizing performance to *production variances.*

These three top-level obstacles to achieving robust and reliable performance are sometimes referred to as the PTV (Process, Temperature, Voltage) aspect of the design challenge. Beyond these barest of necessities lie the broad plains of optimization, the central design phase in which performance conflicts will met by making trade-offs. However, before we can proceed with a detailed discussion of some examples, and start to think seriously about optimization, we must give further consideration to the various types of process sensitivities that can arise in analog design. Further, it must be understood that these are in no sense sequential parts of a design flow, during which each potential sensitivity, or an aspect of optimization, is addressed and then set aside. Undesirable circuit interactions can appear at any time. The most dangerous are those which arise due to "trivial" changes made late in the design process, changes that are in the nature of an afterthought, and which thus do not receive the benefit of the thousands of hours of simulation studies that probably went into shaping the rest of the product, and rigorously verifying its behavior.

2.3.2. Coping with Sensitivities: DAPs, TAPs and STMs

In a typical IC manufacturing process, there are numerous production parameters that vary, including: implant dose rate and time, and other factors affecting total doping concentrations; furnace temperature and time; gas flow rates; etch and deposition times; resist composition, and other factors related to chemical quality; oxide growth rates, fine structure and uniformity; resist thickness and uniformity; micro-assay composition of sputtering targets; and so on. These "low-level" physical variations will manifest themselves through an even wider variety of effects in the "high-level" electronic parameters at the device level.

Beyond this, the use of numerous different circuit topologies in the design phase, and the broad and essentially unconstrained choice of operating

conditions for each device, create even greater *parametric complexity.* It is inevitable that these variances will influence the "top-level" performance of our circuit, to a greater or lesser degree. We have to allow these variances full reign, while ensuring that nearly every instantiation of the product across the wafer meets its operational specifications (which is the first aspect of the *robustness* challenge) and that every sample passing muster during production testing will remain within its performance limits over its lifetime, when large temperature and supply voltage variations can occur (the second aspect of the robustness challenge).

Success in this context requires attention to the most minute detail, and may easily fall out of our grasp, if even a seemingly minor detail is neglected. The simplest of components, such as monolithic resistors and capacitors, embody numerous low-level process parameters which influence their absolute value. Suppose that we are relying on a resistor–capacitor product to determine a time-constant, and thus set the frequency of an oscillation. We must design our product so that the error in the unadjusted frequency can be accommodated; that is, either we can formulate a method for manually trimming to the needed accuracy, or the worst-case[6] uncertainty is within the capture range of some automatic tuning means. Errors in the resistor and capacitor contribute equally to the error in frequency, which is of the form k/CR.

Most basically, the sheet resistance of the layer used for fabricating the resistor is subject to considerable variation. In a diffused or polysilicon resistor this will arise from variations in doping concentration and the depth of the diffusion or film, and can easily be as high as ±15%, a 30% spread. Conductance in any resistive layer is also a function of temperature, sometimes a strong function. For example, the sheet resistance of a diffused resistor may typically vary by 1,500 ppm/K at $T = 300$ K, which extrapolates to variation of about 20% over the 130 K range from 230 to 360 K (–43°C to 87°C). This raises the tolerance band to about 50%. Hopes of containing the frequency within a narrow range are already fading.

Variations in the width and length of the resistor must also be accommodated. When the absolute value needs to be well controlled, one would normally choose to use a physically large resistor, but this may be contraindicated when operation at high frequencies is also required, and the parasitic capacitances of the resistive layer become prohibitive. Assuming a moderate width of about $10\ \mu m$ for such a situation, and allowing for a maximum variation of $0.25\ \mu m$ at each edge, we are faced with a further 5% uncertainty. There may also be some voltage modulation of resistance. Thus, the resistance alone may vary over a

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6 The question of whether the term *worst-case* always has a definite meaning is discussed later in the chapter.

60% range, in a high-volume, robust design context. Adding to this estimate all the similar variations in the capacitor value, particularly those due to variations in the dielectric layer, and for junction and MOS capacitors their varactor behavior, it is easy to understand why the frequency of our basic oscillator can be predicted in only approximate terms: it already has process, temperature and possibly supply sensitivities even before considering the effect of the active elements. Specifications based on the assumption of tighter controls are worthless.

This is a very common situation in analog design, and stems directly from the physical nature of analog signals and components. Aspects of performance that exhibit this particular kind of sensitivity can be classified as *Dependent on Absolute Parameters;* we will refer to such aspects of performance as "DAPs". It is impossible to eliminate sensitivity to this class of parameters by design tricks, though we may in special cases be able to reduce the sensitivity.

For example, the gain–bandwidth of an IC operational amplifier invariably can be traced to the product of a resistance (ultimately setting the value of a g_m) and a capacitance (which may be defined by an oxide layer, as would usually be true for a low-frequency op-amp, or an incidental junction capacitance, as might be the case for a wideband amplifier). Since even carefully designed resistors may have a tolerance of up to ±25%, and capacitors can vary by ±15%, the control of gain–bandwidth in an op-amp[7] may be no better than ±40%. However, it is later shown that when using this amplifier cell in a closed-loop mode, one can introduce a lag network into the feedback path such as to implement an overall two-pole response just above the high-frequency roll-off in which the gain at some (known) signal frequency can be made much less dependent on the position of the dominant pole. The method invokes the reliable *matching* of similarly-formed components, the cornerstone of all monolithic design, to lower the sensitivity to their actual values, in a rather non-obvious way.

In the fastest amplifiers we can make, using BJT processes, and in which the transistors are operating near their peak f_T, it is more likely that the variations in effective base-width and current density cause the production spreads in bandwidth. In turn, the current density depends on the actual emitter area (thus, on lithography) and is invariably dependent on some on-chip voltage source and at least one resistor. Since the f_T is a diminishing function of temperature,

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7 Few op-amp data sheets are forthcoming about this spread, often stating only a typical value. Similar vagueness is often found in the specifications for RF products. Some of this imprecision can be traced to the cost of testing ICs to allow these aspects of performance to be fully guaranteed; some of it has arisen as a kind of tradition, with concerns that the explicit revelation of the magnitude of such spreads would put a more completely-specified part in a "bad light".

spreads from this source must also be addressed. In those cases where devices are operated at very low currents, however, the device's g_m, its (uncertain and voltage-dependent) junction capacitances, and interconnect capacitances set a limit to attainable bandwidth. Whatever the precise mechanisms, the bandwidth of virtually all monolithic amplifiers is strongly "DAP", and in system design we must find ways to accurately define the channel bandwidth (which is only a fraction of the amplifier bandwidth) by the use of off-chip components, such as LC resonators, SAW or ceramic filters, or high-precision CR networks. Certainly, it would be very unwise to depend to any critical extent on the unity-gain frequency of common feedback amplifiers.[8]

As a rule, most (though not all) specifications which have a dimension[9] other than zero will be DAPs. These include time $[T]^1$ and frequency $[T]^{-1}$; current $[A]^1$ in a cell (setting g_m and total consumption); all internally-generated voltages $[V]^1$, (such as noise, V_{BE}, bandgap references, etc.); inductance $[L]^1$; capacitance $[C]^1$; resistance and impedance $[\Omega]^1$ or $[L]^{0.5}[C]^{-0.5}$; conductance and admittance $[\Omega]^{-1}$ or $[L]^{-0.5}[C]^{0.5}$; etc. These sensitivities are addressed in various ways, some well known. Where absolute accuracy is essential, we can bring the dimension of "time" to an IC by utilizing a reference frequency defined by a crystal; or we can introduce the International Volt by laser-trimming against a primary standard during manufacture; we can use external resistors to establish accurate currents; and so on.

Next we turn to the second of these sensitivities. Absolute errors in the element values of *all components made of the same materials* (of all resistors, all capacitors, all current-gains, all V_{BE}s, etc.) need not affect certain crucial aspects of performance. By relying on the use *of pure ratios,* we can assure the accuracy of any specification having dimension zero. Examples are gain at relatively low frequencies (and gain matching); attenuation (even up to high frequencies); relative phase between two signals (and precision in quadrature); filter Qs and overall filter shapes; conformance to functional laws (such as logarithmic, hyperbolic tangent, square-law); waveform, duty-cycle, weighting coefficients; DAC/ADC linearity, and the like.[10]

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8 In the 1970s a great deal of nonsense was being published about using "the operational amplifier pole" as a basis for the frequency calibration of what were misleadingly called "Active-R Filters".

9 Again, the dimensions used here are those familiar to electrical engineers. In a formal treatment, they would of course be expressed in fundamental MKS or CGS units. Logical signals have dimension zero.

10 Of course, the use of digital ratios brings an even higher level of accuracy, for example, in frequency division. But not all logical circuits are above reproach. Phase jitter and non-quadrature are just two examples of error in supposedly pure-binary circuits where analog effects lead to degraded performance.

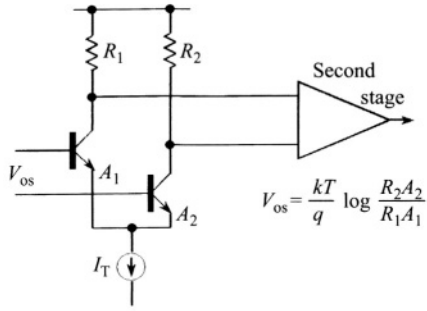


Figure 2.1. Some ratiometic circuits produce dimensional quantities.

We may call such specifications *Tolerant to Absolute Parameters,* and will refer to them as "TAPs". Because of this tolerance, or low sensitivity to tracking element values, we can in principle achieve highly accurate low-frequency gain, even in the presence of large absolute variations. In special cases, even some dimensional variables are in this class of TAPs. For example, the input-offset voltage of an op-amp using a BJT differential-pair as its g_m stage (Figure 2.1) is a precise function of the circuit parameters:

$$V_{os} = \frac{kT}{q} \log \frac{I_1 A_2}{I_2 A_1} = \frac{kT}{q} \log \frac{R_2 A_2}{R_1 A_1} \tag{2.1}$$

Provided that the emitter areas and the load resistors can each be made closely equal,[11] the offset voltage will be small, typically sub-millivolt. Its actual magnitude will be dependent on neither the absolute size of the emitters nor the absolute value of the resistors, and it is scaled only by the fundamental dimensional quantity kT/q (25.85mV at T = 300 K). In monolithic analog design, we are constantly on the lookout for phenomena of this sort. The TAP perspective relies on a strong reliance on *ratios* to eliminate the effect of large absolute variations in parameters, and on an appeal to fundamental scaling phenomena rather than a reliance on external stimuli.

A related use of the above equation is the generation of a bias voltage based on the "delta-V_{BE}" idea, in which the emitter-area ratio A_2/A_1 (sometimes in combination with the resistor ratio R_2/R_1) is deliberately made much greater than unity. For example, when the net ratio is set to 48, V_{os} has a theoretical value of 100.07 mV at 300 K. This voltage will be proportional to absolute temperature (PTAT), which is often the most suitable biasing choice in BJT design. Since its basic value can be precisely determined by a pure ratio, and subsequently

[11] This is a simplification; other factors, including base-width modulation (early voltage) and various on-chip gradients are involved.

multiplied up to a higher value, better suited for IC purposes (say from 300 mV to 1 V) by another pure ratio, we can fundamentally eliminate the sensitivity to absolutes. Incidentally, it will be apparent that the delta-V_{BE} concept can be used as the basis of a silicon thermometer, and when implemented using more careful techniques than briefly described here, the voltage can be accurate to within 0.15%, corresponding to a temperature error of < 0.5 K at 300 K.

Finally, in this set of process sensitivities, we must address aspects of circuit performance that are *Sensitive To Mismatches,* which we call "STMs". Clearly, this includes a great many effects, since the immunity conferred on a circuit function through the use of pure ratios is immediately lost if these ratios are degraded by mismatches. (As used in this frame of reference, the term refers not only to components that should be *equal,* but to the deviation from some *nominal ratio.*) Here again, the strongly Newtonian nature of analog circuits is apparent, since matching accuracy is directly related to device size. It is clear that the greater the number of atoms used to define some parameter, the lower the sensitivity to absolute variations in this number. We are here faced with a very basic trade-off, since the use of large devices, whether passive or active, is at odds with the minimization of inertia,[12] and also with the minimization of die size. In fine-line processes, one is inclined to use small geometries rather uniformly, to achieve the highest speed and packing density; but high accuracy analog design requires careful attention to the *optimal scaling* of devices. Bigger is not necessarily better, however. Even when die size and device parasitics are not critical considerations, the use of excessively large devices can actually cause a *reduction* in matching accuracy as various gradients (doping, stress, temperature, etc.) begin to assert an influence.

This interdependence of circuit design and layout design is found in all integrated circuit development, and serious lapses will occur if they are ever treated as separate and distinct activities, but especially so in analog design. There are many times when one can achieve a very distinct advantage, whether in speed, accuracy, packing density, or robustness, by altering the circuit design to accommodate a more promising layout scheme. Further, the generous use of similar device orientations, sets of physically parallel resistors, and dummy components at boundaries pay significant dividends in preserving analog accuracy.

With some thought, it may be possible to actually avoid the need for transistor matching at all, through the use of dynamic element matching, based either on the better matching that can be achieved between capacitors, or through the use of clever switching of the topology, either to alternate error sources in a

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[12] A general term favored by the author to describe the net effect of all mechanisms leading to the storage of charge in a device, which causes sluggishness in the response.

canceling fashion, or by an appeal to averaging. Thus, the most accurate silicon thermometers do not depend on the (still somewhat risky) matching between two separate transistors, which can also be degraded by mechanical strain across the die. (Transistors are always willing to operate as strain gauges.) Instead, a single junction can be used, and biased sequentially at two or more current levels. The integer ratios between these excitation phases can be generated to very high accuracy. The resulting small PTAT voltages are amplified, and subsequently demodulated, by switched-capacitor techniques.

One can implement dynamic band-gap references using similar methods, although in this case there remains an unavoidable dependence on the actual saturation current of the junction, $I_S(T)$, which is always a matter of total doping level and the delineation of the junction area. While this DAP remains, there are still further tricks up the analog designer's sleeve to reduce these sensitivities in the design of advanced band-gap references, from "direct" to "diluted", but they cannot be fully eliminated. One can see why this is so, by remembering that the transistor is used essentially as a *transducer,* from the domain of temperature to the domain of voltage. Also, since this $V_{BE}(I, T)$ is dependent on the *absolute current density* in the device, which in turn depends on some on-chip resistor, it can be stated with certainty that there is no way to design a reference to be inherently traceable to a fundamental physical constant such as the bandgap energy of silicon.

In making trade-offs in device structure, scaling and placement for analog design, one can appeal to *principles* and *guidelines,* but it is unwise to rely on *rules.* Some of the principles of matching are obvious and unequivocal; others tend to be wrapped in folklore, a reflection of the common fact that insufficient statistical data is available to state much with certainty, in many practical cases. This is often because one is designing on a new IC process for which statistically-reliable data has not yet accumulated. Guidelines for matching, which is not a matter of basic circuit design but rather, the design of the layout, are provided in Chapter 33. However, absolute attention to device sizing must be made during the design phase, and very definite parameters assigned to all components prior the Design Review, since one cannot assume the layout designer is a mind-reader. These should not only be embedded in electronic form, in the captured schematics, but should also be immediately visible on these schematic, in the pursuit of total clarity and the elimination of ambiguity, as well as in the spirit of full disclosure of all design issues for peer review, and possible correction.

2.4. Robustness, Optimization and Trade-Offs

The expression *robust design* is widely used. We have an intuitive sense of what this means and entails. A robust product is one whose design ensures that

it is not critically dependent on the precise materials used in its construction, and is able to fully perform its intended function under all anticipated operating conditions and endure vigorous environmental forces without significantly affecting its long-term utility. In civil engineering, such as the construction of a major bridge, these would include a consideration of material stress limits in the presence of worst-case traffic loading or unusually severe cross-winds, recognizing the criticality of choosing the construction materials and the actual process of fabrication.

The trade-offs related to robustness that go into the design of a modern ICs are at least as numerous as for large engineering projects, such as bridges and buildings. They may also involve similar concerns for product liability, for example, in components used in medical equipment, or where electromagnetic emanations may pose a threat to a human user.

A robust circuit design is one in which the sensitivities of critical performance specifications to variances in the manufacturing process and the circuit's operating environment are first fully anticipated and identified and then systematically nulled, or at least minimized, through optimal choices of macro-structure, cell topology, individual device design, component values, bias conditions and layout.

Can we define a "Robustness Coefficient"? Almost certainly not. Even some sort of "Figure of Merit" is unlikely. Can we delegate the maximization of robustness and its inverse, the minimization of sensitivity, to a computer? Only in a few special and limited situations. This is where one's mastery of design will play its most indispensable role. Time and again, we find that the search for the most robust solution requires that we know how to shift attention, as circumstances require, from the *whole* to *the parts* and back again to the *whole* – numerous times in the course of the product development. There is a fractal-like quality to analog IC design, in the sense that whether we are viewing it at a high level, wearing the customer's shoes, or stepping down through many layers of circuit structure and operation, the biasing of its components, device optimization, the physics at the next layer below that, there is at every level a huge amount of information to consider and a great deal of complexity to cope with.[13]

It is important to understand the distinctions between robustness, optimization and trade-offs. While these topics overlap very considerably, they stem

[13] Again, we may note that, once one gets down to the gate level, there is little to be gained, in the pursuit of digital system design, by probing deeper into structure.

from quite different impulses. As we have seen, robustness is a *state*; it is the outcome of pursuing analytical methods, simulation studies, and the selection of technologies, architecture and scaling and judgments in the course of a product design. The threads leading to this result will lead back to many sources, but most notably from the pursuit of optimization and the making of trade-offs.

Optimization is a *process.* It is the analytical consideration of a system and its parameters with a view to discovering local minima and maxima in *n*-space (where in practice *n* is often much greater than 2) which can be identified in some particular way as the best choice(s), where the performance aspects of special interest are closest to what can ever be achieved within the constraints of a given architecture, technology or specific component limitations. This is a methodical, systematic process very amenable to mathematical representations or, more commonly, numerical methods. Thus, optimization is an *algorithmic process.* Since the representational equations "know" nothing about the world beyond their *n* dimensions, there is no expectation of discovering new worlds of possibility; maxima and minima never turn into wormholes.

Consequently, one can never be sure that the solution offered by an optimization process is truly the *best of all possible choices*: it is only the best of a severely limited sub-set of choices. In this sense, it is as much the product of the framer of the algorithm as of the data. Further, numerical optimization provides little if any insight into extending performance beyond these boundaries, and because an analysis does not include all the variables, it may not even be finding the actual best case in practice. This will frequently be true even for rudimentary circuits, such as a cell-phone power amplifier. Finally, there is a strong likelihood that the under-skilled user of optimization procedures ("design programs") will believe that the "answer" is genuine and reliable, while learning nothing in the process.

In contrast, the act of making a trade-off is *no sense* algorithmic. Trade-offs require a human *decision,* namely, the difficult and vexing choice between two or more *equally attractive alternatives,* and the sacrifice of one good for another. It is a zero-sum game. It involves risk and calls for judgment. In this common situation, there are no rules to lean on; if there were, the next step in a design would not be a trade-off, but the mechanical, unthinking application of some such rule. In the end, all decisions are emotional.[14] Many engineers are inclined to reject this tenet, proclaiming that this may be so in the social world, but not in technology, where each step in a development proceeds logically. However, it does not take many years practicing design to see the truth of this statement. When all the evidence, facts and analyses point clearly and unequivocally to a single, definite course of action. no decision is needed: that

[14] Due to Edward de Bono, a professor of psychology at Oxford University.

is optimization. But in the many cases where the data are flat, equally favouring many possible ways forward, a decision is called for. *That is* a trade-off.

It may even be a coin toss. In developing a standard linear product, having a wide applications domain, but lacking all the required market data, the designer is often forced to make guesses, based on personal "market savvy" and experience as to the most useful combination of performance parameters. One frequently needs to decide whether to pitch the product toward leading edge performance and stop worrying about its 50 mA supply current, or toward portable applications, by halving the current and accepting that performance will suffer. Similar trade-offs will arise between using bare-bones, ultra-cheap design practices with a view to achieving the smallest possible die area, in order to be competitive in pricing the product, or err on the side of extending the feature set and improving the performance, to extend the applications space, and considering such factors as ease of use and customer satisfaction. There are no algorithms for success.

2.4.1. Choice of Architecture

We will now look at several case histories, to illustrate the meaning of robustness in more concrete terms. In doing so, we will appreciate how elusive a quality it can be. To achieve the most satisfactory overall solution requires that numerous parallel and competing factors need to come into focus into a unified vision of the whole. Many trade-offs, which are open-ended decisions, are needed.

Clearly, we need to start with a robust architecture. Of the numerous ways we can satisfy a system requirement, some will be more sensitive to slight changes in parameter values than others. A simple example is provided by a cellular phone system involving a limiting IF with an received signal strength indication (RSSI) output (Figure 2.2). In this example, the RSSI output voltage – which reports to the cell supervisory system the strength of the received signal, in order to minimize the transmit power in the handset and at the base station – is scaled by a band-gap reference voltage, generated in the receiver sub-system. This voltage is then measured, and converted to digital form, by another IC, a codec, in which a second bandgap generator is embedded. Either or both of these circuits may be built in CMOS, a technology which is not noteworthy for high reference-voltage accuracy.[15] A guaranteed absolute accuracy of ±5% in

[15] See B. Gilbert, "Monolithic voltage and current references: theme and variations," in: J. H. Huijsing, R. J. van de Plassche, and W. M. C. Sansen (eds), *Analog Circuit Design,* pp. 269, which includes further examples of good and bad planning in the use of voltage references.

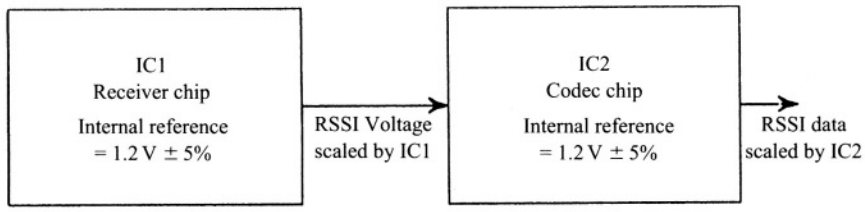


Figure 2.2. A vulnerable approach to scaling of nonlinear circuits.

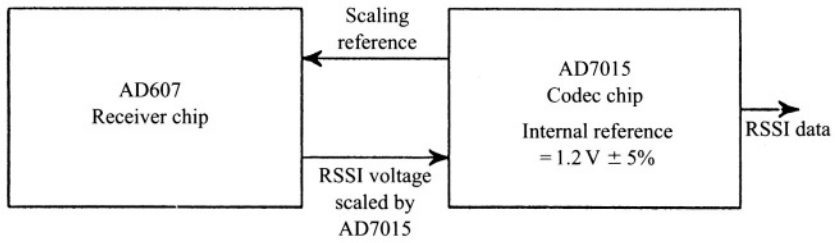


Figure 2.3. Use of a common reference voltage removes uncertainties in scaling.

each reference is a reasonable objective if high yields are to be achieved and the cost objectives do not allow trimming.

There could have been historical reasons for the use of this approach. For example, one circuit may have been designed ahead of the other, as part of a separate venture. Clearly, in this scenario, there is a worst-case error in the RSSI calibration of ±10%. If this occurs at the top end of a receiver's 70 dB dynamic range, the measurement error could amount to ±7 dB. In this scheme, there is also some yield loss due to the use of at least one redundant reference generator. Finally, it is possible that the uncorrelated noise of the two independent references could lead to LSB instabilities in the measurement; this may be especially troublesome where there is a high level of flicker noise, as in a pair of CMOS bandgap references.

Figure 2.3 shows a first alternative, in which only a single reference is used. This method is used in the Analog Devices AD607 single-chip superhet receiver. The mixer and linear IF strip are provided with a linear-in-dB gain control (AGC) function, the scaling reference for which is derived from the companion codec (AD7015). The error in that reference is now inconsequential, since it alters both the scaling of the RSSI output (so many mV/dB) and that of the ADC in the codec (so many LSBs per mV). Here, we have a classic example of the minimization of sensitivities through a dependence on ratios at the *system level.* The revised approach can allow much looser tolerances on

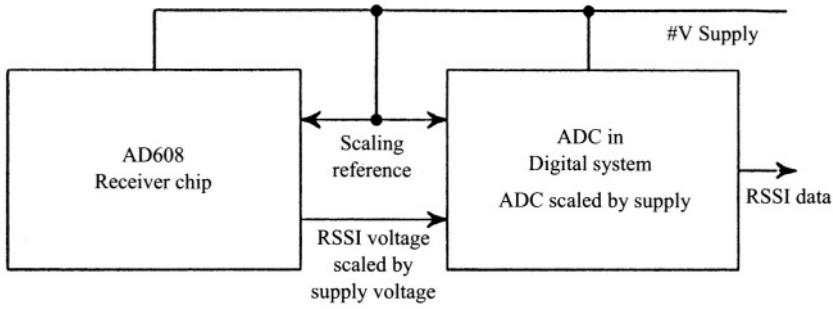


Figure 2.4. Absolutely calibrated voltage references are often quite unnecessary.

the remaining reference, if accuracy is not needed for any other purpose. Close matching of resistor ratios (utilizing unit resistors throughout) results in a high overall RSSI measurement accuracy, from antenna to bits. There sometimes is a case to be made for using more than one voltage reference circuit within the confines of a single IC. These cells are invariably quite small, and the isolation resulting from using separate cells is valuable. But these situations generally arise in less-critical systems. For example, in extensive tracts of current-mode logic, local cells are used for biasing.

In some cases, an even simpler solution is possible. This is the use of the raw supply voltage to scale both the RSSI function and the ADC (Figure 2.4). This approach is used in both the AD606 (a Log-Limiting IF Strip) and the AD608 (a Single-chip Superhet Receiver with Log-Limiting IF Strip). The RSSI output is scaled directly by the raw supply voltage, but this is also used by the ADC as its scaling reference. Thus, both bandgaps have been completely eliminated, with no loss of accuracy, as well as their supply current, die area, bonding pads, package pins and attendant ESD concerns, and guaranteed robustness. The only trade-off in this case is only that the components must be used in partnership. This slight loss of flexibility is never of great concern in high-volume system-oriented products.

2.4.2. Choice of Technology and Topology

Early in the design planning, we will select an appropriate technology for an IC product, based on issues of target cost, performance objectives, production capacity, time to market (and the possibility of cell re-utilization) and other issues of a strategic nature. In some cases, we will have little choice but to use a foundry process. We then start looking for robust circuit topologies – structures which have demonstrated low sensitivities to the absolute value of the individual passive components (minimizing the DAPs), and low sensitivities to mismatches, supply voltage and temperature (TAPs and STMs). The design

principles are invariably the same: lean heavily on the use of ratios wherever possible, in the pursuit of TAPs; adopt sensitivity analyses and chose low-sensitivity cells in the case of DAPs; use careful layout techniques to address the STMs.

A couple of examples of techniques that address robustness will be presented. In the second of these, we will consider a rudimentary voltage-mode amplifier based on a pair of bipolar transistors with resistive loads. Open-loop amplifier cells of this sort are often deprecated, partly because of concerns about gain accuracy. Rather, the common tendency is to appeal to the use of op-amp techniques, in the belief that they automatically circumvent such problems, and conveniently transfer the attainment of high gain accuracy to the ratio of just two resistors. Occasionally, this may be effective, if the op-amp has sufficient open-loop gain at the frequency of operation. But this is often not the case in practice.

Indeed, one of the worst analog-circuit myths is the notion that the chief value of an op-amp is its "very high open-loop gain". Suppose we have an op-amp cell that has been proven to have a reliable DC gain of 10^6 and a *nominal* unity-gain frequency of 200 MHz, and we are planning to use this cell to realize an amplifier having the (seemingly low) numerical gain of ×12 at 10 MHz. We choose the feedback ratio accordingly. For an inverting configuration, the input resistor R_1 might be $1\,k\Omega$ and the feedback resistor to the summing node R_2 would be chosen as $12\,k\Omega$. With robustness in mind, we might decide to make R_1 as 3 units of $3\,k\Omega$ in parallel and R_2 as 4 units of $3\,k\Omega$ in series (Figure 2.5), use a generous width, and make sure the layout designer puts these resistors side by side, even interdigitates them and adds dummy resistors at each end to further ensure the ratio accuracy.

Then, in simulation (or perhaps in a bench experiment) we find that the actual gain is much lower; instead of ×12 it is found to be only ×9.6. Why? Because the open-loop A_{OL} gain *at frequency* is only 200 MHz/10 MHz, or merely ×20,

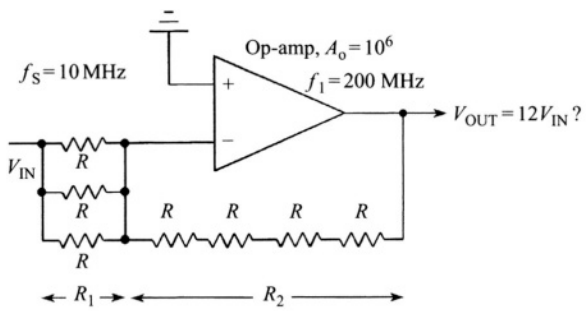


Figure 2.5. A fixed-gain amplifier designed to be robust: but is it?

assuming the usual case of dominant-pole compensation. At this juncture, one might decide to just make a correction to R_2, of slightly more than the wanted-to-actual gain ratio 12/9.6, to compensate for the lower A_{OL} at 10 MHz. Either through the use of vector arithmetic or simulation, we find that R_2 needs to be raised to 16.44 kΩ. This is no longer a low-integer ratio, but we choose to now use a total of *five* units for R_2, extending the length of each element by 9.6%, from 3 to 3.288 kΩ. A small change in the length (keeping the width constant) will not seriously jeopardize the ratio, because this dimension will invariably be relatively large. For example, using a sheet resistance of 1 kΩ/square and a width of 10 μm, the length increases from 30 to 32.9 μm, (the nearest 0.1-μm increment, resulting in an error of +0.06%).

We may think we are pursuing a sound "TAP" approach in using these "ratio-based" tactics, but this would overlook the important fact that the unity-gain frequency f_1 of the op-amp is itself a "DAP", being subject to variations in the on-chip resistor that determines the bias current and thus the g_m of the input stage, and variations in the on-chip capacitor; together these set the unity-gain frequency, f_1, which can easily vary by up to ±40% in production. Therefore, a *one-time adjustment* to the resistor ratio cannot guarantee accurate closed-loop gain at 10 MHz over all production units. In fact, the gain will vary from ×10.3 to ×13.2 over the lesser f_1 range of 150–250 MHz, a variation of only ±25% (Figure 2.6).

There are several ways in which this particular problem might be solved in practice. The preferred solution, whenever one has control over the complete ensemble, is to lower the op-amp's internal compensation capacitor and substantially raise the f_1 to a value better suited to the specific application of the amplifier cell, which no longer requires it to provide HF stability at all gains down to unity. Another solution, chosen to illustrate how robustness can often be achieved by the use of like effects, is shown in Figure 2.7. A second on-chip

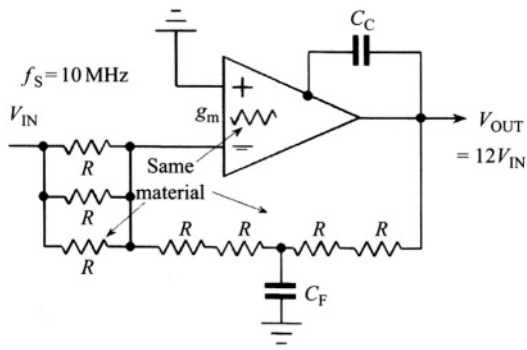


Figure 2.6. Improved amplifier using carefully-scaled bandwidth compensation.

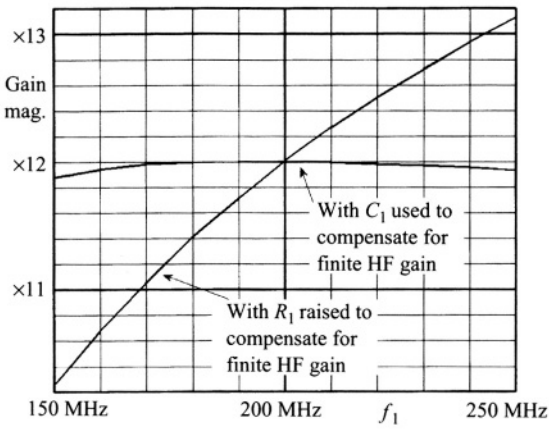


Figure 2.7. Simulation results for original and improved amplifiers.

capacitor C_F has been added at the junction of the two halves of R_2. If we make this component out of the same units as the internal HF compensation capacitor and also make the resistor that sets the bias, and thus g_m, of the input stage out of the same material and similar-sized units as R_1 and R_2, we can achieve a useful desensitization of the closed-loop gain at the presumed signal frequency of 10 MHz. Now we are *matching time-constants,* and on the path toward a true TAP situation.

It is useful to show how this improvement in robustness is obtained. We begin by modeling the op-amp's forward gain as that of an inverting-mode integrator $-1/sT_1$, and define the feedback time-constant as $T_F = R_2C_F/2$, and the magnitude of the closed-loop DC gain as $G_0 = R_2/R_1$. The transfer response of this circuit is

$$G(s) = \frac{-G_0\,(1 + sT_F)}{1 + (1 + G_0)\,sT_1 + (1 + G_0)\,s^2T_1T_F} \tag{2.2}$$

This is a two-pole response with a Q of T_F/T_1. Thus, we can rewrite (2.2) as

$$G(s) = \frac{-G_0\,(1 + sQT_1)}{1 + (1 + G_0)\,sT_1 + (1 + G_0)\,s^2QT_1^2} \tag{2.3}$$

It is easy to hold the ratio Q to within fairly narrow limits, since both T_1 and T_F are generated by CR combinations having exactly the same process sensitivities. For operation at a specific frequency, such as 10 MHz in this example, our only remaining concern is the *absolute value* of both time-constants, represented in (2.3) by the single integrator time-constant T_1. If we were concerned with the broadband response, we would choose to use a low Q; but since the

main objective in this illustrative example is presumed to be the desensitization of $G(s)$ to the actual value of T_1 over a narrow frequency range, we may find it beneficial to use a somewhat higher Q.

Suppose we decide to make the magnitude of the gain $G(s)$ at the operating frequency equal to the target (DC) gain G_0. Solving (2.3) for Q we obtain

$$Q = \frac{1 + G_0}{1 - (1 + G_0)\, sT_1} \tag{2.4}$$

Thus, for $sT_1 = 10\,\text{MHz}/200\,\text{MHz} = 0.05$ and $G_0 = 12$, the optimal value of Q is 32.5. From (2.4) it also follows that this compensation scheme cannot be used above

$$sT_1 = \frac{1}{(1 + G_0)} \tag{2.5}$$

For the target gain of ×12, this technique can provide accurate compensation only up to 200MHz/(1 + 12) = 15.4MHz, at which frequency the Q would be dangerously high.

We might also determine the sensitivity to the value of T_1, and set that to zero. One could spend a few hours in this sort of analytical wonderland, but it would not be very helpful in providing practical insights. It is often the case that the actual operating conditions differ from those assumed at the start of a project, and all the effort poured into a specific analytical solution needs to be repeated. A more efficient way to explore the general behavior of such compensation techniques is invariably through *creative simulation.* The results that were shown in Figure 2.6 required about a minute of experimentation and optimization in real time (the maths shown above took considerably longer to go through). They demonstrate that, with the optimum choice of C_F and a small adjustment to R_2, good stability in the magnitude of the gain at 10 MHz (+0/–1%) is possible over a ±25% range of f_1, which represents the bulk of the yield distribution of a production op-amp.

In this brief exercise, we were able to convert troublesome DAP behavior into a benign TAP form; that is, we ensured an accurate gain at a significant fraction of the op-amp's unity-gain frequency, with a near-zero sensitivity of gain to that parameter at the chosen frequency. Even when a higher f_1 is employed, which, as noted, would be the preferable solution to minimizing this sensitivity, the addition of C_F would still be useful in further improving robustness in production, and at very little cost in die area, and at no cost in power consumption. By contrast, solutions based on further increasing the op-amp's f_1 *will* incur power penalties, within a given technology.

An excessive reliance on small-signal modeling with linear equations, and the use of small-signal simulation, is always a *very* risky business. Unfortunately, these methods are widely used in many theoretical treatments of circuits

found in the academic literature to the neglect of the consequences of variations in circuit dynamics caused by perturbations in the working point, a result using signals of practical magnitude. Small-signal analyses and simulations totally hide numerous such effects.

It is common for device nonlinearities to introduce gain variations of a significant fraction of a decibel over the voltage (or current) swing corresponding to the full output of the circuit. This is the domain of nonlinear dynamics, which is invariably intractable using standard mathematical tools, while posing no problems to a simulator. Thus, one should spend relatively little time using simplistic frequency sweeps ("Bode plots") examining the gain magnitude and phase at some nominal bias point, and *far more time* in various kinds of dynamic sweeps. These include full transient simulations, pushing the circuit to confess its secret weaknesses, not only for comfortable operating conditions, but also at the extreme limits of the process, voltage and temperature (PVT) range, with comprehensive package models,[16] for worst-case source and load impedance, and the like. This issue is revisited in Section 2.5.7.

2.4.3. Remedies for Non-Robust Practices

One of the most intensively studied design topics is that of active filters, of both continuous- and discrete-time types, reflecting their importance in all fields of electronics. The better texts on the subject emphasize the need to choose topologies and/or component values *that formally* minimize the sensitivity of the dimensionless specifications, such as gain and the geometric disposition of poles and zeroes. Unfortunately, these same authors often show a poor appreciation of the need to convert a beautiful "minimum-sensitivity" design (in the strictly mathematical sense) into a practical, *manufacturable* entity.

For example, there is little point in concluding that the optimal (least-sensitive) solution is one in which, say, resistors of 5.3476, 1.0086, 1.7159 and $8.1030\,\mathrm{k}\Omega$ are needed, along with capacitors of similarly exotic values. Such component precision can rarely be met even in a board-level design. The chief appeal of text-book filter functions, such as the well-known Bessel, Butterworth and Chebyshev formulations, is simply that they are *mathematically tractable* and enjoy a certain sort of canonic rigor. But in these days of very fast computers and simulators, there is no compelling reason to stick to classical forms.

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16 It is essential to keep well in mind that circuits do not know what they're *supposed* to do, and design mastery entails making sure that transistors dance to *your* tune, not theirs. Thus, if you are using a common 25 GHz IC process to realize, say, an audio amplifier at the tail end of a receiver, the circuit will surely promote itself to a microwave oscillator, unless you pay attention to easily-forgotten parasitic effects having no essential relevance to your intended application.

The art of designing *manufacturable* filters begins with the sure expectation that some slight departure from the "ideal" (often over-constrained) response will be forced by the difficulty of actually realizing non-integer element ratios to high accuracy in a production context, and that it will be necessary to juggle the partitioning and topologies so as to force a solution using *simple integer ratios of Rs and Cs.* In modern filters, this paradigm is less often practiced in the design of continuous time filters than in switched capacitor filters. The most likely explanation is that the former were developed in the age of electrical theory, while the latter arose in an intensively pragmatic context, where it was known from the outset that unit replications would be essential to robustness.

The approach to monolithic filter design thus *starts with a trade-off,* namely, the need to set aside the text-books, and cut loose from the canonic rigor presented in the filter design literature. The ensuing design exercises may involve a considerable amount of "inspired empiricism" using the simulation of cells containing only element ratios that one knows can be reliably reproduced in high-volume production. Such an approach is straightforward for low-order filters, but can quickly become very difficult when advanced filter functions must be provided. However, in such cases, it is usually possible to create some adjunct routines to perform algorithmic optimization in a few minutes of unattended computer operation. Because filters are invariably required to be linear, the computational burden can be greatly simplified by the temporary use of idealized active elements in SPICE, or the use of a platform such as MathCad.

It should be realized that this is just a starting point. and it is important to note that an appeal to empiricism should not be confused with guessing, or even worse, lazy-mindedness. It simply recognizes that situations often arise in which systematic and analytic methods are either inadequate to the task at hand, or become too cumbersome to provide the needed rate of progress in a product development, or fail to generate insights that can be translated into practice. After empirical methods have pointed the way forward, it remains the responsibility of the designer to ensure a controlled and predictable outcome in the face of production tolerances. Empirical searches for manufacturable solutions are in no way a *substitute* for robust design based on fundamental considerations, but they are needed to explore the use of (and the invention of) more robust cell structures. Diligence will always be needed thereafter to preserve low sensitivities and reproducibility.

Some analog cells are inherently robust while others, that may quite appear similar, are not. Figure 2.8 shows two translinear multiplier cells.[17] The (a) form

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[17] See B. Gilbert, "Current-mode circuits from a translinear viewpoint: a tutorial," in: C. Toumazou, F. J. Lidgey, and D. G. Haigh (eds), *Analogue IC Design: The Current-Mode Approach,* Chapter 2 IEE Circuits and Systems Series, vol. 2, Peter Perigrinus, 1990.

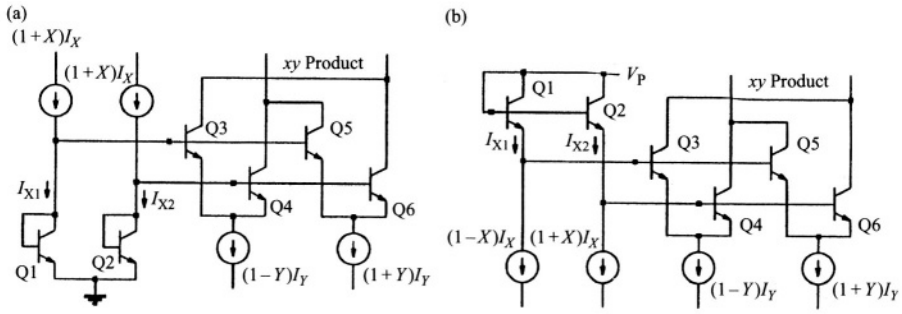


Figure 2.8. Two fundamental multiplier cells; (a) beta-immune, (b) beta-prone.

is called "beta-immune", because its scaling is very little affected by BJT current-gain, β, and can remain accurate even when I_Y is almost as high as βI_X. The (b) form is called "beta-prone", because its scaling is sensitive to beta, even for much less demanding bias conditions, for example, when $I_Y = I_X$.

The explanation is straightforward: in (a) all the base currents in Q3–Q6 are in phase with the corresponding currents in Q1 and Q2, and the ratios of I_{E3}/I_{E4} and I_{E5}/I_{E6} remain strictly equal to I_{E1}/I_{E2}. Assuming the betas are essentially equal and independent of current, the input-linearizing transistors are not affected by the reduction in the *absolute* bias levels due the current robbed by the bases of Q3–Q6, because these are in exactly the same ratio as I_{X1}/I_{X2}. On the other hand, in the (b) cell, the base currents are out of phase with the inputs, and the ratio I_{E1}/I_{E2} is therefore not equal to the input-current ratio. The overall consequence is that the scaling of the (a) cell includes the factor $1/(1 + 1/\beta)$, while for the (b) cell this factor is approximately $1/(1 + 3/\beta)$. Here we have a good example of a *trade-off in topology*. In practice, the (b) form is easier to drive (from voltage-to-current converters using the same device polarities for both the *X* and *Y* signals) than the (a) form, and the literature shows that the (b) cell has almost universally been chosen in monolithic analog multipliers because of this topological advantage, at the expense of static accuracy, temperature stability, intermodulation and slightly higher noise (due to the base currents of the core transistors). However, the beta-dependent scaling can be easily compensated in the synergistic design of the associated voltage reference.

2.4.4. Turning the Tables on a Non-Robust Circuit: A Case Study

This lesson underscores the general point. Good topologies and biasing practice are fundamental requirements in the pursuit of sensitivity minimization, in

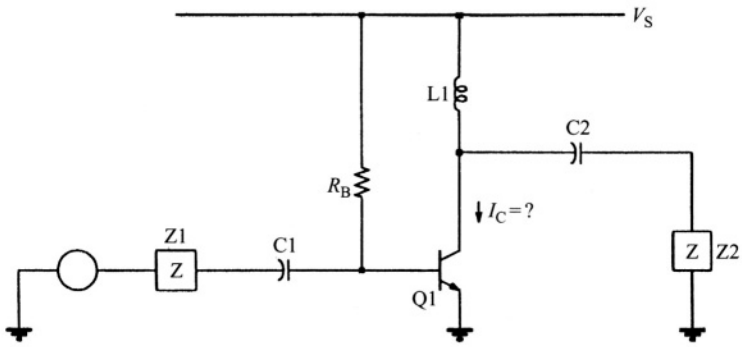


Figure 2.9. An LNA having inadequate attention to biasing.

the face of every sort of environmental factor, notably "P" (lot-to-lot production spreads leading to absolute parameter uncertainties), "V" (supply voltage) and "T" (temperature). In numerous cases, we would have to add "M" (matching) as one of these factors, though not in the following case study. Figure 2.9 shows the circuit, a low-noise RF amplifier (LNA). The topology used here is open to criticism, although the form was once widely used. The behavior of this *one transistor* circuit can be surprisingly complex, and abounds with trade-offs and compromises. It is often nonchalantly presented in articles with almost total emphasis on its high-frequency aspects and hardly any on the crucial matter of choosing and regulating the bias point. It amply illustrates the peculiarities of analog design.

We will focus here on the biasing methods. The general method shown, and regrettably still all-too-often employed in discrete-transistor RF design, uses a high-value resistor R_B taken directly to the supply voltage, V_S, in order to establish the collector current I_C. This immediately introduces serious and quite unacceptable sensitivities, of at least four kinds.

First, we need to understand that the precise value of I_C, and its temperature shaping, affects all aspects of BJT performance, and thus that of the LNA. The g_m is essentially proportional to this current,[18] and the noise, power gain and input impedance are all dependent on it. This would be true even at moderate frequencies. At high frequencies these parameters are far more seriously impacted, since I_C also affects the f_T of the transistor; for this class of operation (and as a general rule) this will be much lower than the peak f_T, which occurs

[18] Neglecting for the moment the effect of impedances in the emitter branch. For example, inductance may be incidentally introduced by the bond-wires and package, or deliberately used to desensitize the g_m to I_C.

only over a very limited range, and at current-densities above those usually permissible.

This crude rationale was based on assumptions of this sort: (1) I_C must be 2 mA; (2) the nominal DC beta is 100; (3) the nominal V_S is 3 V. A base current of $20\,\mu A$ is, therefore, needed, and using reference data, is was found that the V_{BE} for the particular transistor type is 800 mV at this current. The nominal voltage across R_B is thus 2.2 V, and this resistor must be $2.2\,V/20\,\mu A = 110\,k\Omega$. Choosing an IC resistor layer which has a sheet resistance of $440\,\Omega/square$, it is found that 250 squares are needed. Not wishing this ("trivial") biasing component to be physically too large, one might decide to make it $2\,\mu m$ wide by $500\,\mu m$ long. Now, if we examine the numerous ways in which sensitivities have been carelessly introduced into this cell, we find:

1 I_C varies with the supply voltage, V_S, in a more-than-proportional way. Noting that $I_B = (V_S - V_{BE})/R_B$, the sensitivity is increased by the factor $V_S/(V_S - V_{BE})$, or about 1.36. Thus, over the range $2.7\,V \leq V_S \leq 3.3\,V$ the g_m will alter by about ±14%.

2 I_C is essentially proportional to the DC beta. Over an assumed worst-case range of $35 \leq \beta_{DC} \leq 200$, the collector current (and thus the g_m) would vary from one third to twice its nominal value.

3 I_C is extremely sensitive to the delineation of resistor width, chosen as $2\,\mu m$. If we suppose that the worst-case variance on this parameter totals $\pm 0.25\,\mu m$, the g_m will vary by ±12.5%. (We can fairly safely ignore the length variation in this case.)

4 Using this biasing scheme, the g_m will vary with temperature for several reasons. The DC beta will vary by typically +1%/°C; over the range $-55°C < T < +125°C$, this is a large effect. Also, the V_{BE} varies by roughly –1.5 mV/°C, causing I_C to increase by another 0.07%/°C. However, a resistor TC of 1,000ppm/°C would fortuitously lower the last two effects. Some polysilicon resistors, however, have a negative TCR, which will aggravate the sensitivity.

Now let's redesign this rudimentary, but important, basic cell with robustness uppermost in mind. We must begin by squarely facing these facts:

1 In BJT practice, the control of g_m is invariably of paramount importance. In this LNA it is a major factor in the determination of gain, noise figure and the accuracy of the input/output matching. Without inductive degeneration in the emitter, the sensitivity to g_m is maximal; even when such is added, some sensitivity remains.

2 The basic g_m is qI_C/kT – it is directly proportional to collector current. This is a very reliable relationship, the fundamental basis of translinear design, and remains true even when the signal frequency f_S is a substantial fraction of the f_T. It will be diluted somewhat by the presence of significant base resistance $r_{bb'}$, and, in all modern transistors using polysilicon regions for emitter contacting (which includes SiGe structures), by the emitter resistance $r_{ee'}$.

3 It follows that I_C must be proportional to absolute temperature (PTAT) if the g_m is to be stable; furthermore, this condition must be maintained in the presence of *unknown* values for $r_{bb'}$ and $r_{ee'}$.

4 Therefore, if the design is to be robust, I_C must have a low sensitivity to V_{BE} and β_{DC}; it must have a low sensitivity to V_S; and it must be desensitized with respect to the delineation of on-chip resistances. This last objective stems from the need to achieve accurate impedance matching at both the input and output ports of an LNA, but the need for resistor control is in conflict with production variances in sheet resistance as well as lithography. It must be noted that numerous extant designs give little attention to matters of this sort and the design process may use S-parameters throughout with no regard for the fact that these are but snapshots of the full reality, *relevant only to one particular bias point.*

5 In designing the associated biasing circuit, we will need to remember that I_C will be a function of V_S also through the effects of Early voltage, V_{AF}, since (in the non-robust design being considered here) its collector is taken directly to V_S, while its base–emitter port is close to ground. Furthermore, variations in f_T, C_{JC} and (except in silicon-on-insulator processes) C_{JS} will impact the HF performance. Therefore, any improvements must seek ways to minimize all these sensitivities.

Whatever design choices we make, we should instinctively strive to find *the simplest possible solution.* On the other hand, in a monolithic context, this does not mandate the sparse use of transistors. Since this chapter is not concerned with LNA design in general, we cannot afford to pursue this example as fully as it deserves, but we can address the above challenges to robustness with the following observations.

Item (1) touches on a broader issue of LNA design, namely, the use of reactive (noise-free) emitter degeneration to lower the sensitivity of the effective g_m (now defined by the vector sum of $r_e = 1/g_m = kT/qI_C$, and the inductive reactance $Z_E = \omega L_E$). This also serves in the interest of robustness, because inductors can readily be fabricated on-chip, and have narrow

production tolerances[19] being largely dependent on the number of turns. For present purposes, the Q of the inductor does not need to be high, and it may be made in spiral form using the aluminum interconnect. It will often have a few ohms of resistance; using a typical metal thickness this amounts to roughly one ohm per nanohenry, which means that the Q will be constant at 2π, or about 6.3.

This resistance will vary, due to variations in the thickness (hence, sheet resistance) of the metal, and the width of the spiral trace, which is subject to photolithographic and etching variances. However, its resistive component will form only a small part of the overall emitter impedance, and is of relatively little consequence to the determination of gain and linearity. We can expect that there will be further impedances in completing the emitter branch and connecting to the system (board-level) ground, a path that includes the bond-wire(s) and the rest of the IC package. The inductive components will be predictable, but, keeping robustness in mind, we will want to ensure that the method used for *biasing* is not sensitive to the addition of *unknown resistances* in the emitter branch.

Item (3) demands that the I_C be PTAT. Numerous cells are available to generate a PTAT voltage, based on ΔV_{BE} techniques. Through the use of an appropriate topology, this voltage can have a low sensitivity to V_S; we can even embed it in full compensation for the effects of V_{AF} on I_C in the LNA transistor. This voltage can be converted to a current through the use of a resistor. However, when this resistor is on-chip, we will not fully satisfy the last criterion in Item (4), but we can greatly reduce the sensitivity to photolithographic and etching variations by using a physically large resistor, leaving the unavoidable uncertainty in the sheet resistance of the resistor layer and its temperature coefficient.

In many theoretical treatments of circuit design, properties such as g_m are presumed to be inherent to the device, although dependent on the bias current, which is treated as a "merely practical" consideration. However, this viewpoint is ill-advised. The generation of reliable currents in an IC using bipolar transistors, and in some RF CMOS circuits, is based on the use of resistors, and the currents will therefore be poorly controlled when these are on-chip. One may be able to still achieve robust operation when this is the case, but generally speaking many of the properties of an analog IC, such as the terminal impedances of a broadband amplifier, are directly traceable to a real resistor somewhere on the chip, and the voltage that is imposed across this resistor.

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[19] There is another very important reason why we will choose to use inductance in the emitter, which is in connection with intermodulation. The constant inductive reactance can be made much larger than the nonlinear r_e, thus greatly improving the linearity of the overall transconductance.

Not only are the port impedances a reflection of a physical resistor, but other parameters such as gain and bandwidth may be.

For example, if a wideband amplifier is constructed using a BJT differential pair as a transconductance stage, with resistive collector loads, the gain $g_m R_L$ can be stated in the form R_L/R_0, where R_0 is the transformed value of a bias resistor embedded in the chip. Thus, just as for a feedback amplifier, the gain magnitude is a simple, dimensionless ratio, which can be quite accurate when the relevant precautions are observed. For an op-amp, whose open-loop gain at a practical signal frequency f_S can be stated solely in terms of its unity-gain frequency, f_1 (its magnitude is f_1/f_S), the situation is more complex, since f_1 is determined by a CR product, and cannot be accurate without trimming. Only at very low frequencies does an op-amp's gain become a simple ratio, and then a rather uncertain one.

Holistic optimization of the LNA. It is apparent that we have been pursuing a "whole↔part↔whole" approach to this LNA, which is essential in the relentless pursuit of robustness. We started with the *whole* circuit (usually not so simple!) and then moved in closer to think about just *apart*: the biasing details. In doing so, our attention was eventually directed back to the *whole* again: the search for a new topology. It was not essential to respond to this undercurrent of concern about biasing. We could have stuck doggedly with the whole – the original circuit. But in considering how to improve the biasing part, we came to realize that this was actually a crucial and multi-faceted question, and that the flaws in the original topology were deep, necessitating a search for ways to improve the whole design, not just "choose the bias point". (Although we cannot pursue the topic here, there is a formal optimization of the bias related to the minimization of noise figure, but that does not overshadow the above considerations.)

While we fully expect to use simulation to fine-tune this design, particularly with regard to its two-port characteristics at, say, 1.9 GHz, and with the full package model included,[20] it is difficult to see how we could hand over the challenge of producing a robust design to some kind of optimization procedure. Such a program can be no better than its writer in foreseeing all the myriad ways in which a handful of components can be connected to make an improved cell. This is clearly not a matter of simply instigating an automatic search of all possible solutions and then evaluating them all to find the "best" one, in basically the same way that Deep Blue wins at chess. In the first place, we would have to decide on some very simple constraints, such as the maximum

[20] Which, in addition to the simple series inductance of bond-wires is also rife with other parasitics, including mutual inductance between these wires, the effect of which is difficult to quantify without simulation studies.

number of components that allowably could be used, and their mix (so many transistors, so many resistors, etc.). But more importantly, the critical value of certain spontaneous, unforeseen and creative topological alterations will necessarily be overlooked in a finite procedure. Even a skilled designer-programmer could not anticipate every combination and every consequence needed to drive a branching heuristic. An appeal to random topological variations would generally lead to nonsense. Equally problematical, one needs to formulate elaborate and all-embracing evaluation functions, "goodness" criteria that tell us when we are getting closer to a "better" solution, however, that may be defined.

Given a very limited set of performance criteria and only a few permissible topologies, some useful optimization may be possible in this way. However, the benefits to be gained from such a program would need to be weighed against the time taken to write it, and the number of times it would be used.[21] Such projects invariably fail, because they do not provide enduring practical value. A more serious criticism of the "Optimizer" approach to product development is that it may be seriously misunderstood by young designers, who are inclined to use "clever programs" of this sort rather than confront what seems to be the formidable challenge of learning the individual details attendant to each class of circuit. The allure of quickly having results in hand, no matter what is inside the program, may be hard to resist.

To return to our LNA, we can already see changes are going to be needed in the biasing, and perhaps in the topology, too. There is also the challenge of choosing a close-to-optimal size for the transistor, where we will be confronted with more trade-offs. Since the effective g_m is influenced by $r_{bb'}$, we will choose a device geometry that minimizes this parameter as far as practicable before the f_T of the transistor begins to suffer appreciably due to the reduction in current-density and the increase in junction capacitances. We also need to minimize $r_{bb'}$ in order to achieve an acceptable noise figure. However, large devices will have a high C_{JC}, which, in the prototype topology, will have a low capacitive reactance at high frequencies. This is a very common trade-off in RF design. Knowing that the C_{JC} of a large, low-noise transistor may be high, we might

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21 The writer speaks from painful experience. In 1960, using an Elliott 803 vacuum-tube computer, he wrote a program for *The Automatic Design of Circuits.* It really did what it claimed, for a small set of circuits. It selected the best devices for a given application out a library of 36 germanium transistors, and given simple boundary objectives, such as gain, input noise, bandwidth and the like, it calculated all component values, later selecting the nearest available standard values and recalculating the bias point and the subsequent effect on the terminal performance. It then carried out a specified number (the default was 1,000) of Monte-Carlo analyses and predicted board (not chip) yield for typical production variances and their correlation factors. This labour of love was used once or twice, in a serious capacity, and some examples published in the professional literature. Then, it fell into oblivion.

start thinking about the use of a cascode transistor to minimize the impact of this capacitance on the feedback impedance Z_F, which we will use to more reliably control the LNA parameters. A cascode is also consistent with the need to reduce the effect of the supply voltage.

But this entails another trade-off, namely a reduction in the available voltage swing at the collector and/or a tightening of the constraints on supply voltage. It must also be remembered that the emitter impedance of the cascode transistor at high frequencies is not the simple resistive $r_e = kT/qI_C$; rather, it is markedly inductive. A yet further trade-off then arises: a small transistor is needed here, to reduce its capacitances C_{JC} and C_{JS}. Large values would not only complicate the output matching but also introduce even-order distortion due to their varactor behavior; and there is a further subtle source of noise, often overlooked, arising from the resistance associated with C_{JS} and its Johnson noise. A large C_{JE} in this device will cause further parametric distortion.

So, we decide to use a small transistor. But this will have a high R_C, and at the currents often used in LNAs, this will reduce its collector junction voltage, perhaps almost to the point of saturation at the most negative signal swings at its collector. This region of operation will lead to further distortion and intermodulation. (Here, we are once again in nonlinear territory.) Furthermore, its high $r_{bb'}$ is transformed in its emitter branch – the collector load of the large transistor – into an inductive component, leading to further effects in the overall behavior of the LNA. Thus, the scaling of the cascode involves several other trade-offs.

The next step will be a pencil-and-paper session of sketching out a few other topologies, to consider different ways the trade-offs may be resolved. This sort of exercise comes easily to the experienced designer, who is unlikely to be in awe of the well-established approaches, and who realizes that the aggressive exploration of numerous alternatives is an essential part of the design process, often leading to valuable new insights, even breakthroughs which later become classics in their own right. Designing involves traveling down many dead-ends. It is as much about discovering or devising new cell forms as it is about simply "choosing the bias point", calculating a few component values, and performing perfunctory simulations to offer at the Design Review as a smoke screen to distract from the absence of real invention.

After a brain-storming session of this sort, we may find that a circuit like Figure 2.10 offers a pretty good fit to the circumstances. The supply-insensitivity is achieved through the use of an adjunct bias cell, which for the time being we can describe as a band-gap reference, generating $E_G = 1.22\,V$ independent of the supply. This provides the bias for the base of the g_m device, Q1, now delivered through a moderate-sized, and therefore more controllable, resistor, needed only to block the RF input from the bias cell. The emitter current is then defined by the resistor R_E, which we can choose to put either

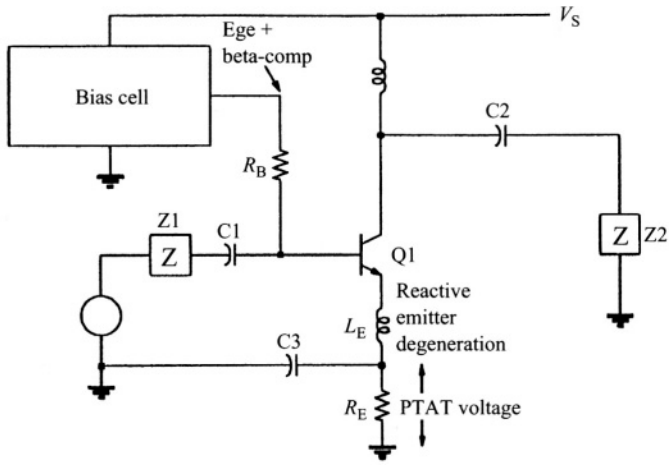


Figure 2.10. Revised LNA, having precise bias control and greater robustness.

off-chip or on-chip. An extra pin is not required, since this path to ground must already be separated from generic power-ground pins, so that choice will mainly depend on the required accuracy of gain and impedance matching. Since the bulk of the emitter impedance is now determined by the inductance L_E, using a sufficiently high value of I_C so that $r_e \ll Z_E$, we have largely desensitized the gain and matching to variations in the bias current. A fairly high current is needed anyway to achieve a low input-referred voltage-noise spectral density due to shot noise mechanisms; the input-referred voltage is proportional to $1/\sqrt{I_C}$ and evaluates to $0.27\,\text{nV}/\sqrt{\text{Hz}}$ at 3 mA.

The sum of a suitably-scaled PTAT voltage and a V_{BE} can be made equal to E_G, the so-called band-gap voltage. Here, the reverse principle is being applied: since we are applying E_G to the base, the voltage across R_E, that is $E_G - V_{BE}$, will be PTAT, and thus so will I_E when R_E is a zero-TC resistor, as would be basically the case when this resistor is placed off-chip.[22] Another benefit that accrues from the use of resistive biasing in the emitter is that the sensitivity to the collector–emitter voltage is also lowered, over that of the first LNA. Taken alone, this consideration eliminates the need for a cascode transistor (whose base would be taken to a regulated voltage of about one V_{BE} above E_G or roughly 2 V above ground), to the extent that it serves to decouple supply variations from the collector of Q1. We can afford to omit the cascode

[22] A full discussion of biasing techniques is out of place here. However, we may mention that special methods can be used to generate PTAT currents using resistors of non-zero temperature coefficient.

on these grounds, but may still decide to include it when the high-frequency response is considered. When we do, we will have to revisit all those trade-offs.

The bias cell used to generate E_G could just be some previously-designed band-gap reference. But there is no need to set the bias voltage V_B to E_G, since this voltage does not need to be stable with temperature. It is only necessary to make it the sum of a V_{BE} (tracking the V_{BE} of isothermal Q1) and set up a PTAT voltage V_{PT} across R_E. We could choose to make V_{PT} as high as possible, in order to minimize the effect of errors due to mismatches in the V_{BE}s or arising across base resistors. Again, we are faced with a trade-off, since the higher bias voltage will erode the available voltage swing at the output, lowering the 1 dB gain-compression point. In such cells, it is an easy matter to include a 'beta-fix' in the bias voltage, to compensate for the finite DC beta of Q1, ensuring that at least its bias is accurate, although there remains an unavoidable sensitivity to the AC beta, which is approximately f_T/f_S; for an operating f_T of 12 GHz and a signal frequency f_S of 2 GHz, this is only 6. This is only one of several key parameters that are in the nature of "DAPs", and which unavoidably determine into the overall performance; in fact, there are very few "TAPs" in an LNA.

Integrated with the LNA, the optimized biasing scheme might look like Figure 2.11, in an all-NPN design. LNA designs of this sort can nevertheless provide acceptably accurate gain (± 1 dB) and matching (return loss > 15 dB) at high frequencies, with low sensitivities to supply voltage, temperature, current-gain and Early voltage. That is, they can be rendered *more* robust by careful attention to biasing issues, and the use of *synergism* in the biasing cell. Clearly, there is much more to robust LNA design than can be presented here and these comments are offered only to illustrate the sort of considerations that must be applied. It is noteworthy that *"trade-off"* occurs over ten times in this section

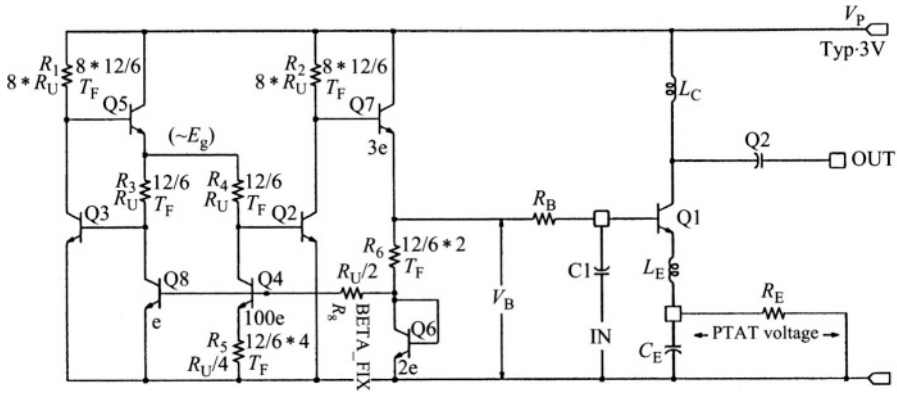


Figure 2.11. A more carefully crafted bias generator integrated into an LNA.

alone, concerned with a *one-transistor circuit* and in almost all cases, the context is not that of a pair-wise selection. This hints at the complexity of the trade-offs that must surely be expected of more typical analog circuits.

A further example of biasing synergy. Techniques of this sort – in which robust performance is ensured through the *progressive and systematic* elimination of sensitivities – are of central importance in analog design. In the next example, we will use a different approach to desensitize the gain of an open-loop amplifier in the presence of large variations in *junction resistances.*

Figure 2.12 shows a rudimentary gain cell based on a differential bipolar pair. The "simple-theory" unloaded small-signal voltage gain is

$$G_O = \frac{I_E R_C}{2V_T} \tag{2.6}$$

The first point of note is that this is another example where one would not choose to use a temperature-stable bias current. Rather, just as for the LNA, the collector currents must be basically PTAT to ensure temperature-stable gain. This is the general rule and is sometimes thought to be the only correct choice. PTAT biases are readily generated using a ΔV_{BE} cell, which generates some multiple of $V_T = kT/q$, let's say σV_T. In some way, this voltage is converted to a current by a resistor R_G. Thus we can rewrite (2.6) as

$$G_O = \frac{\sigma V_T}{R_G}\frac{R_C}{2V_T} = \frac{\sigma R_C}{2R_G} \tag{2.7}$$

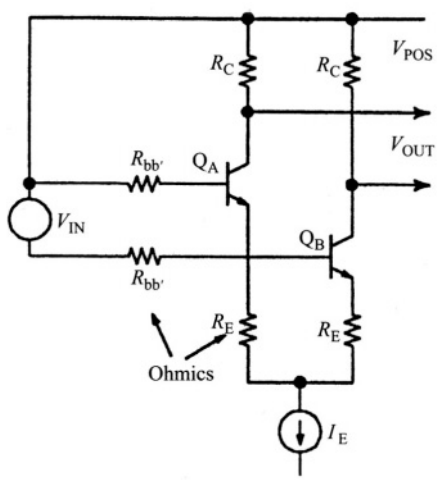


Figure 2.12. A rudimentary gain cell.

Now we appear to have a pure ratio. For small bias currents, the gain will be quite close to the theoretical value, up to fairly high frequencies, except for a small error due to the finite current-gain, β_{DC}, which can easily be corrected. But at higher values of bias (lower values of R_C and R_G), we will find the gain to be lower than expected. That is, we apparently have a DAP situation, *even though we thought we were invoking strict ratios.* Why?

It doesn't take long to realize that the finite junction resistances are responsible. Both the base resistance $r_{bb'}$ and the emitter resistance $r_{ee'}$ are involved. It is convenient to refer all such effects to the emitter, modeled in this figure by the resistors $R_E = r_{ee'} + r_{bb'}/\beta_{DC}$. Figure 2.13 shows the resulting gain error versus $V_E = I_E R_E$, in units of V_T. For example, when $R_E = 5\,\Omega$ (due, say, to $r_{bb'} = 200\,\Omega$, $\beta_{DC} = 100$ and $r_{ee'} = 3\,\Omega$) the gain error is — 8.8%, or

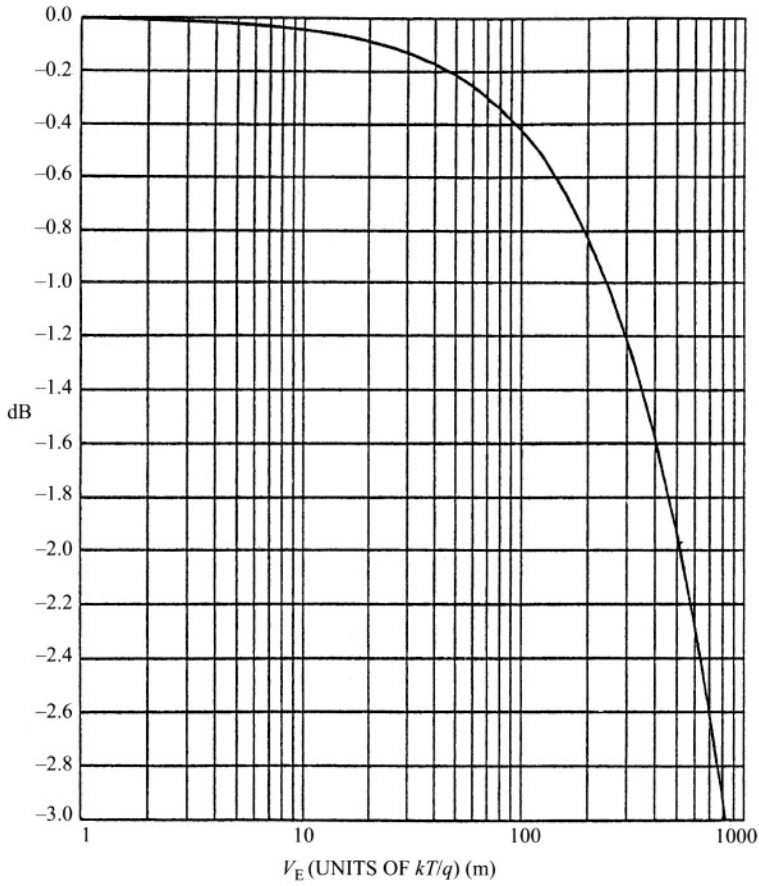


Figure 2.13. Gain error in the basic cell due to ohmic resistance.

–0.8 dB, at $I_E = 1$ mA. Clearly, this error will vary from one production lot to the next, and appears to be a basic flaw, involving an unavoidable dependence on absolute parameters: the transistor junction resistances. The obvious, "brute-force" solution is to increase the size of the transistors so as to lower these resistances, but this route represents an unacceptable trade-off when the maintenance of a high bandwidth is another goal of the design. Similarly, the use of a lower I_E and higher R_C will likewise lead to a loss of bandwidth.

In a family of ICs now in high-volume production, it was essential to push the bandwidth out to about 4 GHz, and neither of the above solutions could be used. However, there is a very simple way to virtually eliminate this error, entailing only the correct design of the bias cell, *with no added components and no trade-offs* in either gain accuracy or bandwidth. This being the case, it might as well be employed as a matter of routine to improve the robustness of the design. In fact, this proprietary technique[23] is valuable even where much lower bandwidths are required, as in IF amplifiers. We will not discuss here the techniques by which the linearity can also be improved to well beyond that of the simple BJT differential pair, as these touch only indirectly on the robustness theme.[24]

Such corrections are possible because we can view this cell as an *analog multiplier,* whose gain is essentially proportional to I_E. Through the careful crafting of this current, a variety of subtle effects can be introduced, including the desensitization to both resistance and to beta. Putting aside the second of these errors for the moment, we can write the *actual* gain as

$$G_A = \frac{I_E R_C}{2V_T (1 + I_E R_E / 2V_T)} \tag{2.8}$$

which is significantly in error when $I_E R_E$ is comparable to $2V_T$. The junction resistance R_E depends on the size of the transistors used in the gain cell. Let R_Ω be the effective emitter-referred junction resistance of a "unit" device, and assume that the gain cell transistors use N unit emitter–base regions. Then, $R_E = R_\Omega / N$. Using (2.8), we can readily calculate the actual value of I_E required to correct for the gain error:

$$I_{EA} = \frac{I_{EO}}{1 - I_{EO} R_\Omega / 2NV_T} \tag{2.9}$$

This at first appears to be an awkward function to implement, but in fact, it readily can be achieved when the associated bias cell is considered as an *integral*

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23 B. Gilbert, US Patent 4,929,909, *Differential Amplifier with Gain-Compensation,* issued May 29,1990.

24 However, the interested reader is referred to "The multi-tanh principle: a tutorial overview", *IEEE Journal of Solid-State Circuits,* vol. 33, no. 1, pp. 2–17.

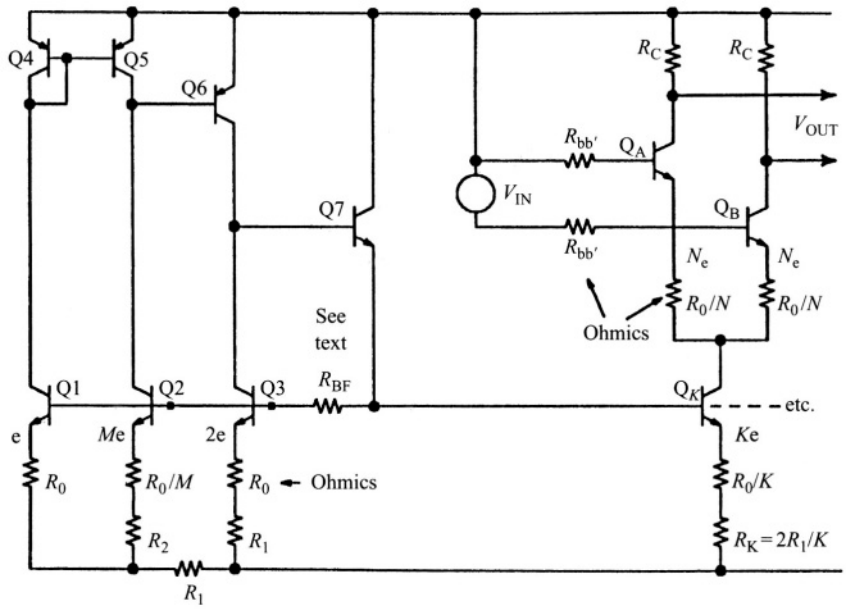


Figure 2.14. Multi-stage amplifier with a synergistic bias cell.

part of the design. Once again, we are seeking a *holistic solution* in the interest of minimizing sensitivity. Figure 2.14 shows a representative scheme.

For the moment, ignore the resistor R_{BF}. This figure also shows the junction resistances associated with Q1 and Q2 in the ΔV_{BE} cell. The *baseline* value for the currents $I_1 = I_2 = I_{CO}$ is just $(V_T/R_2)\log M$, but the *actual value* is

$$I_{CA} = \frac{I_{CO}}{1 - (R_\Omega/R_2)(1 - 1/M)} \tag{2.10}$$

Note the similarity in the form of (2.9) and (2.10); it beckons us to equate the denominators, and thus eliminate the dependence on R_Ω. The required condition is

$$\frac{I_{EO} R\Omega}{2NV_T} = \frac{(R_\Omega/R_2)}{1 - 1/M}$$

Noting that $R_2 = (V_T \log M)/I_{CO}$ and that, in general, I_{EO} is K times I_{CO}, we arrive at the condition

$$\frac{K}{2N} = \frac{(1 - 1/M)}{\log M} \tag{2.11}$$

This condition ensures that systemic variations in R_Ω will not affect the gain. But we have yet to find the value of R_2 required to set this gain to the required

value. Assuming that (2.11) is satisfied, we can use the baseline ($R_\Omega = 0$) equations to do this. The result is

$$R_2 = R_C \frac{K \log M}{2G_O} \tag{2.12}$$

In a robust, manufacturable design, *N, K* and M should all be integer. It is also desirable to find an integer relationship between R_2 and R_C, allowing the use of unit resistor sections. Such convenient solutions may not always be possible, but a little manual iteration will often reveal a solution which is "almost-integer", needing only small adjustments to the length of resistors and thus maintaining a low sensitivity to absolute dimensions.

For example, beginning with a nominal gain objective of ×4 (12.04 dB) and choosing $R_C = 1\,k\Omega$, the required I_{EO} is 206.8 μAP and a target value for I_{CO} of ~ 100 μAP puts the required integer value of K at 2. Choosing $N = 4$ and solving (2.12) shows that a value of $M = 50.5$ is close to ideal. Then, in solving for R_2 using (2.12), one finds that it would need to be 980 Ω, which is not quite integer to R_C. However, using the adjusted fully-integer solution $M = 55$, $R_2 = 1\,k\Omega$, the gain is only 0.02 dB high for $R_\Omega = 0$.

Figure 2.15 shows that the gain error remains negligible for values of R_Ω as high as 100 Ω, when the maximum resistance in the emitters of Q_A and Q_B is 25 Ω, that is, 10% of the r_e. The lower panel shows the corresponding increase in I_E needed to effect this compensation. In the ongoing pursuit of robustness, we would complete the compensation of gain errors by turning our attention to the effects of the finite DC beta, β_{DC}, in both the amplifier and bias cells. The ΔV_{BE} cell generates accurate currents in its *emitter* branches, so while the current in R_K accurately replicates that in R_1, the collector current of Q_K, and thus the gain, is low by the factor $\alpha = 1 - 1/\beta_{DC}$. Further, the g_m of the Q_A, Q_B pair is determined by their *collector* currents, which are low by a similar factor. (This is not "counting twice".) By including the resistor R_{BF}, the bias voltage is raised by an increment that increases as beta falls.

Note as a matter of detail (that's analog design) that the beta of Q_K will increase with the supply voltage, while that of Q_A and Q_B, operating at a V_{CB} roughly equal to zero, is slightly lower and *not* supply-dependent. By placing R_{BF} in the position shown, the current in it, and thus the compensation voltage, reflects the beta of Q1 and Q2, whose V_{CB} increases with the supply in the same way as that of Q_K, while that of Q3, whose V_{CB} is fixed, tracks that of Q_A and Q_B. A simple calculation suggests that it should, in this case, be roughly equal to R_1, but a slightly higher value (here 1.33 kΩ) provides more accurate compensation at very low betas.

The gain error (Figure 2.16) is under 0.05 dB over an extreme range of the SPICE parameter BF (roughly β_{DC} for moderate injection levels and low V_{CB}); the sensitivity to supply voltage is under 0.005 dB/V for VAF = 100 V. In a

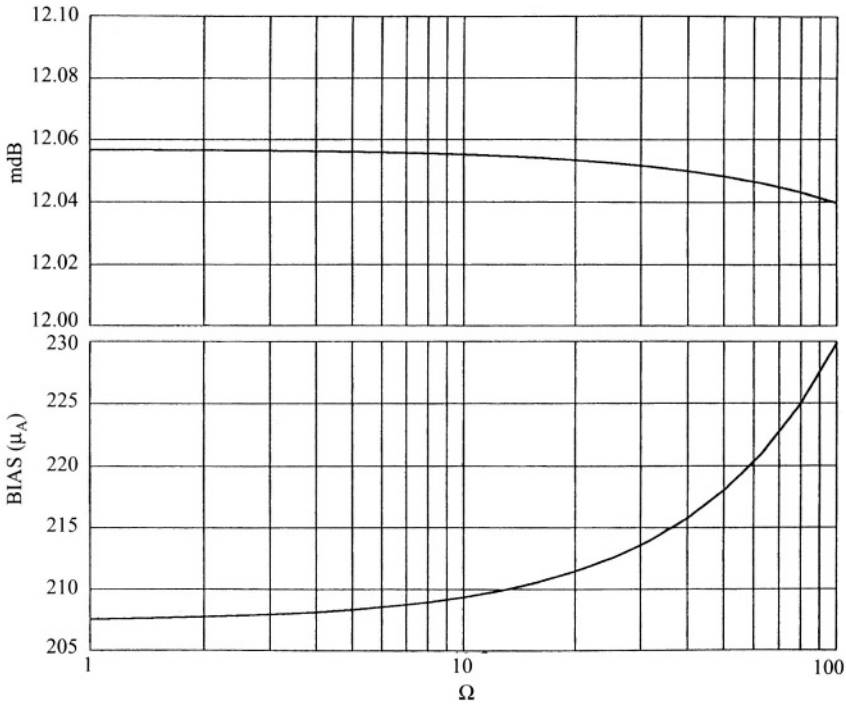


Figure 2.15. Cell gain error using synergistic bias technique.

multi-stage direct-coupled amplifier without the buffering advantage of emitter-followers between each cell, further gain errors arise due to the loading of the subsequent cell. This has a similar form, and can be closely compensated using a modified value for R_{BF}. The cell gain variation over the temperature range –55°C to 125°C is under 0.01 dB for this synergistic duo, further evidence that all the significant device variations affecting the mid-band gain have been addressed. The gain roll-off at high frequencies, while fundamentally of the nature of a DAP related to device inertia, can also be addressed in a synergistic and self-compensating fashion.

Biasing techniques of this sort can be applied to a wide variety of other errors in order to enhance manufacturability. With thoughtful use of optimal biasing methods, and sensible use of integer ratios of unit devices, very significant improvements in robustness can be assured, with little topological complication or the expenditure of more power. While the present examples are limited to bipolar studies, similar compensation methods based on assumptions of bias tracking can be applied to CMOS circuits. Indeed, even greater care is needed in this medium, where process variations are frustratingly high.

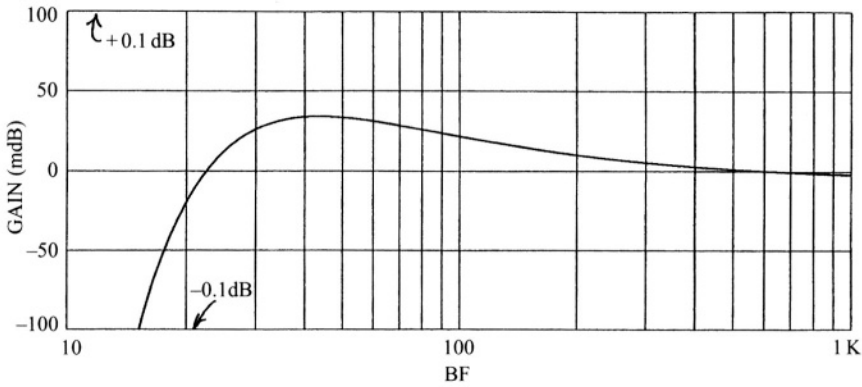


Figure 2.16. Cell gain error using beta compensation.

2.4.5. Robustness in Voltage References

There seems to a good deal of misunderstanding about the use of voltage references. Nowadays, the term "band-gap reference" is used very loosely. It is often applied to any cell in which a difference of junction voltages, that is, a ΔV_{BE} is used for general bias purposes. In this capacity, the output voltage is also made sensibly independent of the supply voltage. However, true voltage references – cells which generate a voltage to within very close tolerances relative to the *Standard Volt* – are rarely needed in complete systems. Their use in many cases is redundant, since there is no *measurement* of voltages, the only process that inescapably demands a reference standard. Exceptions include ADCs and DACs (although these often support the use of a common system reference voltage) and in volt-scaled components, such as the denominator of an analog multiplier, the gain-scaling of a VGA, and the slope and intercept calibration of logarithmic amplifiers used in power measurement. (In the latter case, the amp actually measures voltages, *not power* directly.) Notice that these are all nonlinear circuits. But even in systems where such components are used, it is often possible, and certainly preferable, to arrange for the use of a single voltage to scale them, either in pairs (as was shown in Section 2.4.1) or more broadly. This design philosophy, based on the dependence on *ratios,* not absolutes, can be viewed as an extension of the principles of analog design within an monolithic context, which are founded on the assured expectation of matching like against like and essentially isothermal operation.

The generation of a reference voltage to high absolute accuracy within the confines of a monolithic design, and without using trimming of any kind, involves different considerations to those previously discussed. It is no longer amenable to clever use of ratios, since *voltage is dimensional.* Circuits operating

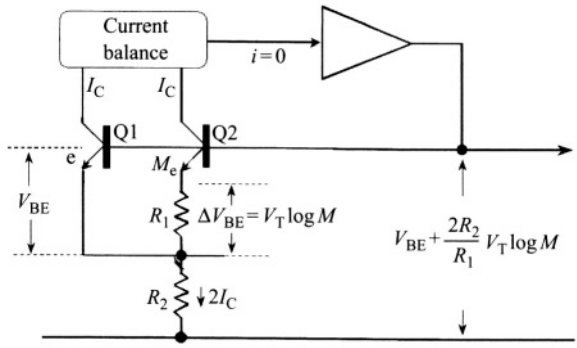


Figure 2.17. The basic Brokaw cell.

on supplies of 5 V and below will use some embodiment of the band-gap principle, such as the Brokaw cell shown in Figure 2.17. Several ways exist to get *quite close* to the intrinsic band-gap voltage of silicon, but all techniques used to realize a band-gap voltage reference are prone to fundamental sources of error of the DAP variety.

The output voltage of a band-gap reference is the sum of two voltages,[25] in proportion roughly 65% V_{BE} (sometimes called CTAT– that is, complementary to absolute temperature) and 35% ΔV_{BE} (PTAT) when using typical current densities. The latter can be generated to very high accuracy, being scaled predominantly by kT/q (a fundamental voltage) and the dimensionless logarithm of a current-density ratio $M = J_1/J_2$. This *pure ratio* can be generated in a monolithic IC to arbitrary accuracy, using unit-replicated devices and careful layout techniques, including flanking dummy elements and common-centroid placement.

It is easy to show that the sensitivity of the PTAT voltage to the value of M is lowered by the factor log M. This immediately suggests that the largest possible value of M should be used. There are other reasons for this choice. The wide-band noise associated with the ΔV_{BE}, due both to shot-noise mechanisms and junction resistances (notably $r_{bb'}$) is fairly large. Here comes another trade-off: the minimization of voltage noise in these cells dictates the use of high collector currents and correspondingly low resistances. This fact is non-negotiable; references operating at low currents will be inherently noisy, often dictating the use of an off-chip capacitor to reduce the noise bandwidth. Thus, when each transistor in a typical ΔV_{BE} pair is operating at $100\,\mu A$, the total voltage noise spectral density due to shot noise in the basic ΔV_{BE} is $2.07\,nV/\sqrt{Hz}$ at

25 Sometimes the summation is performed in current mode, but the underlying principles are the same.

T = 300 K. Assuming the $r_{bb'}$ of the small transistor is 400 Ω, this contributes a further 2.58 nV/√Hz (the ohmic noise of the larger transistor is invariably negligible). The total noise is thus 3.3 nV/√Hz. For the commonly-used ratio of M = 8, the ΔV_{BE} is theoretically 53.75 mV at 300 K; this needs to be multiplied by about 9 to generate the required PTAT component (say, 480 mV) of the output, resulting in an amplified noise contribution of about 30 nV/√Hz. However, using M = 100, the ΔV_{BE} is theoretically 119 mV, and needs to be multiplied by only 4, resulting in less than half that noise, 13.2 nV/√Hz.

Notwithstanding these clear advantages, many contemporary band-gap designs continue to use M = 8, first popularized by Widlar and later used by Brokaw.[26] For this case, a 10% uncertainty in the emitter area ratio (which is not unlikely in a modern process using sub-micron emitter widths) is reduced by the factor log (8) to a 4.8% uncertainty in the PTAT voltage, nearly 2% of the total voltage. In modern practice, a value as high as 100 can often be used without excessive consumption of chip area. The same 10% ratio error is then reduced by log (100) to 2.17%, or 0.87% of the sum. But this is still not the total possible error in the PTAT component. The ohmic junction resistances will introduce additional components of voltage, raising the ΔV_{BE} to

$$\Delta V_{BE} = \left\{1 + \frac{R_\Omega}{R_2}\frac{M-1}{M}\right\}\frac{kT}{q}\log M \qquad (2.13)$$

where R_Ω is the effective ohmic resistance $r_{ee'} + r_{bb'}/\beta_{DC}$ referred to the emitter branches. (Compare equation (2.10).) For example, using $r_{ee'} = 10\,\Omega$, $r_{bb'} = 400\,\Omega$, $\beta_{DC} = 100$, R_Ω evaluates to 14 Ω; when operating each transistor at 100 μA and using M = 8, the ΔV_{BE} is increased by about 2.3%. Using the higher ratio of M = 100, and thus a higher value of R_2 for the same current, the ΔV_{BE} error is reduced to +1.17%; when multiplied up to represent some 40% of the final reference voltage, this amounts to an elevation in output of roughly + 0.47%.

On the other hand, the control of the V_{BE} component of the "E_G" sum is much harder, since it is fundamentally "DAP", involving several production-variable parameters, including doping concentrations in the emitter-base region (determining the Gummel number), the absolute area of the emitter window, and the absolute collector current, which depends on the absolute value of the on-chip resistors. Since these are uncorrelated variables, control of the *in situ*

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26 This choice was justified when transistor geometries were much larger, and a voltage reference cell might consume a large fraction of the total die area. For this reason, it used to be common to make this one cell serve as a master biasing generator for a multi-section signal-processing circuit. Nowadays, one can often use local bias cells, to minimize coupling via biasing lines, since they can be tiny. However, this is not advised when these bias voltages are also utilized as accurate references; see Section 4.1.

V_{BE} (i.e. the operational value in the full circuit context) may be poor. For example, if we assume a ±25% variance in Gummel number (a reflection of the doping control), and a similar variation in an emitter of width $0.6\,\mu m$ (the length will generally be well controlled), and further assume that the resistors (which set all the transistor current densities) also have an absolute tolerance of ±25%, the *in situ* V_{BE} might vary by as much as ±15mV, amounting to a contribution of ±1.25% in the typical output of about 1.2V. Combined with the ±0.87% random uncertainty in the (uncorrelated) PTAT voltage, and the additional systematic elevation due to R_Ω, the worst-case error can easily amount to –2/+2.5%.

With these various trade-offs in mind, a strategy for lowering this error will now be briefly described. The chief objective has to be the improvement in the accuracy of the main V_{BE} with further reduction in ohmic errors. This clearly calls for the use of a very large Q1, in the basic cell, which could be realized by using a much wider and longer emitter, say, $3\,\mu m \times 40\,\mu m$ rather than $0.6\,\mu m \times 5\,\mu m$, perhaps having several emitter fingers to further reduce R_Ω. But imagine the area that would then be consumed by Q2: it would be at least eight times larger in a standard realization, and would preferably be as much as a hundred times larger! This is an inefficient trade-off, though technically satisfactory, except perhaps with the added concern that the cell may need a larger HF stabilization capacitor (not shown in Figure 2.17).

A better approach is to separate out the cell fragment that generates the PTAT voltage and add an *independent section optimized strictly for providing a very accurate* V_{BE}, as shown in Figure 2.18. This topology is only an example of the numerous ways in which this idea can be realized, and is used here simply to make a point. An experienced designer of reference cells will be able to find several shortcomings in this sketch, and we could easily spend the rest of this chapter discussing trade-offs to improve the supply rejection, the inclusion of holistic compensation for a variety of special applications, enable-disable functions, etc.

The main principle here is that by separating the PTAT generator from the V_{BE}-determining device and focusing on optimizing the latter for minimum sensitivity to production variances, a more robust overall solution is reached. In this case, the trade-off is one of accuracy versus complexity (and thus chip area), a trade-off frequently invoked in monolithic design. Having taken that step, we might seek to extract further performance improvements out of these extra components. As previously noted, absolute voltage references are needed less often than might be thought in well-designed systems. The sharing of less accurate references across system boundaries is one of the best ways to avoid the need for traceability to an external standard. In BJT-based design based, the more common requirement is for bias currents that are PTAT, rather than "ZTAT"; these can be generated with excellent accuracy, since they

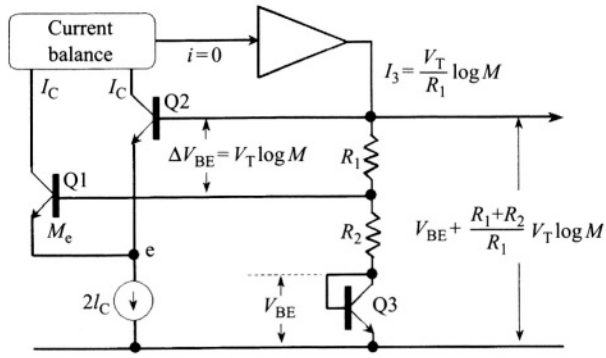


Figure 2.18. Band-gap reference using a separate transistor for the V_{BE}.

do not depend on V_{BE}, but solely on the logarithm of a simple ratio, scaled by kT/q.

2.4.6. The Cost of Robustness

Since robust design has so many benefits in high-volume production, with the expectation of net productivity gains through its use, it may seem odd to speak of a *cost* of robustness. What is that cost? It often takes the form of *reduced performance*. This happens because there is a kind of exclusion principle at work. One can push performance specifications aggressively, to the limits of the norms for some IC process. Assume an ultra-low input offset voltage is one of the target specifications for a competitive op-amp. Being "TAP", such improvements have been happening for decades. Eventually a point is reached when the sheer force of process statistics stands in the way of further progress and one must pay the price. In this simple example, it may be a trade-off between tightening the test specifications and thus discarding a higher fraction of the product; alternatively, the limit values can be relaxed with the risk of being less competitive in sheer performance, but with better yields. Here, the trade-off is more the nature of a business decision, but these issues cannot be divorced from technical considerations in a commercial context.

In another scenario, suppose we aggressively extend the bandwidth of our new op-amp, to provide a more competitive product. This is more hazardous, because dimensional attributes (such as the characteristic time-constants of the higher-order poles in the open-loop gain function) vary greatly. We are betting on DAPs, which are never a sure thing. This raises the risk of the amplifier going unstable with reactive loads, risking one's reputation for providing reliable solutions and putting a new burden on applications support engineers. The prudent trade-off in such cases is to recognize that, in volume production,

one cannot afford to indulge in brinkmanship, or pursue optimistic objectives and delineate specifications which *seem* reproducible but for which no certain foundation can be provided.

One might argue here that we are confusing robustness, which is about the reduction of circuit sensitivities to process variations, with the choice of test limits that define the specifications, which is about statistics. Certainly, there is a good deal of overlap in this area. We may apply extensive testing to the design during the later stages of product development, for example, through the use of Monte-Carlo simulations, or wait until measured data from several production lots have been accumulated, to determine specification limits consistent with certain yield requirements. The former approach is limited inasmuch as fully realistic process statistics are often unavailable, particularly for a new and aggressively-scaled technology, perhaps one developed primary for digital applications and not yet characterized well for analog use. The latter approach is very costly, and delays product introduction.

This sort of trade-off underscores the great importance in choosing one's technology, system architecture, circuit topologies, signal levels and bias points with great care, and emphasizing those approaches that are inherently robust while studiously avoiding those that may be relying too much on "everything being right". As designers, it is our job to *create solutions* in which the yield/specification trade-off is tractable and definitive, rather than in need of statistical studies or the fabrication of many production lots to demonstrate.

It is in this arena that one's contribution to robustness can be most effective. Using the *same* technology, and the *same* production standards, some designers consistently achieve better yields than others. Might it be that their high-yielding parts are specified less aggressively? Probably not. A review of many designs over a period of decades shows that robustness is not a matter of slackening down to more conservative specifications. That is, "fake robustness" and would not be competitive. Rather, it is because good designers use their medium, the *tabula rasa* of the raw silicon wafer, very thoughtfully, and extract *genuine* performance advantages that have eluded competitors, while still maintaining excellent yields.

2.5. Toward Design Mastery

Each of us has a unique and idiosyncratic approach to the task of designing IC products. We acquire this personal style over a long period of time, spent in learning-by-doing, invariably by going down many dead-ends before finding the way forward, and always learning as much through our mistakes as from our successes.

At the technical level, the design of integrated circuits for manufacture is not in any fundamental way different from design in a student context. The

emphasis on commercial success does not require that skills learned in an academic course of study, or in early industrial experience, be totally supplanted. But it does demand *a change of outlook,* from one in which intriguing technical challenges are the focal point to one in which these are seen as *only one aspect* of a much broader range of issues that will consume a large fraction of the available time. *Circuits are not products.*

Design for manufacture means that the professional needs to constantly keep in mind the singular, long-term objective of either *satisfying an existing customer demand* or *anticipating an unarticulated need* and providing a ready solution. In the best outworking of the latter scenario, one can literally *create a market* for innovative products, when these address a problem that was not obvious until the solution was offered. Product design requires a compelling, consistent and unrelenting vision of the end-game. It demands a candid and auto-critical view of all of the numerous ways in which the project can fail. The technical aspects of this challenge are very significant, perhaps even dominant, but in a commercial context the circuit design phase must be regarded as but one contribution to the success of the overall product development.

2.5.1. First, the Finale

Maxim: Product development starts with the objectives, not the availables.

This simply means that the starting point for any well-run IC project is a total comprehension of the proposed product, addressing a real need as component part of a business-development strategy. It must entail a clear understanding of what *will* be achieved in the course of the development; the competitive (and often novel) attributes which it *will* possess when delivered to the customer, at a certain time and at a certain cost that *are already* determined; the performance specifications that *will* be met at that time; the package that *will* be used; the testing methods that *will* be used to ensure performance; and similar aspects of the outcome. This is very unlikely to happen unless all of the objectives and the schedule have been agreed to by the team and the needed resources have been identified and assigned in advance.[27] A common precursor of the development is the preparation of the product definition document.

The alternative stratagem, *starting with the availables,* means that someone has a "promising new idea for a circuit", and an unscheduled project begins right away to embellish this idea in a product. The strategic value of the product has not been ascertained, nor are the objectives clear. The project very

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[27] Since at any given time a corporation is bounded by finite resources, the addition of a new project unavoidably means that fewer resources will be available to handle a large portfolio of existing projects. In a well-run organization, the impact of new projects on existing ones can be automatically accounted for by sophisticated project management and scheduling software.

probably arises in isolation and may proceed without an awareness that similar (possibly more successful) work is being pursued elsewhere in the company. Interestingly, maverick projects that have this sort of genesis are *not necessarily destined to failure.* They may actually turn out to be tremendously valuable, when eventually converted into an *outcome-oriented* project, perhaps needing significant changes in the design.

2.5.2. Consider All Deliverables

Maxim: All of the project deliverables should be identified right from the start.

These may be divided into *external* and *internal* deliverables, and are all the things that must be generated for delivery either to the customer (externals) or to development/manufacturing (internals), at various times between project start and the Product Release date.

Examples of external deliverables[28] include:

- The *Data-Sheet* – essentially a contract between the supplier and the customer.
- *Product samples,* packaged (or known-good die), tested to Data-Sheet specifications in the quantities needed to satisfy anticipated evaluation demands.
- *Application Notes* for standard catalog components, which elucidate the many ways in which the product can be used, through very specific, fully-worked examples.
- *Evaluation Boards* for high-speed and special components.
- *Reference Designs* for such things as a communications chip-set.
- *Software, Firmware and Development Systems* (for digital ICs).

Examples of internal deliverables include:

- *Detailed Product Specifications,* for use throughout the development, and defining many internal sub-objectives; usually a super-set of the Data-Sheet.
- *Project Schedule and Plan,* delineating the major milestones (Concept Review, Design Review, Layout Review, Wafer Starts, First Silicon, Evaluation Completion, First Customer Samples, Product Release, etc.) and identifying needed resources.

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28 These will generally be needed for internal development purposes, also.

- The *Product Description Document,* which should be generated as an accumulative body of material, and will include such things as marketing and cost data, overall system and circuit theory, block diagrams, cell schematics and detailed descriptions of circuit operation, results from simulation studies, test methods, usage schematics, application ideas, etc. The responsibility for generating this important internal document will usually be shared amongst several people, all of whom need to be advised as to what is expected of them in this regard.
- *Wafer-fab Documentation,* including process type, manufacturing site, lot sizes, etc.
- *Assembly Documentation,* including package type, die attach method, bonding diagrams, use of over-coats, etc.
- *Test Documentation,* including the complete delineation of the tests needed at wafer probe, full descriptions of the support hardware, details of trimming algorithms (where used), and similar details for final test, including all limit parameters.
- *Reliability Documentation,* including life-test and ESD results, production quality monitoring, failure analysis, outgoing inspection, etc.

It is unrealistic to expect that all elements of this large body of information will be available at the start of a development. However, the basic philosophy here advocated is that a very comprehensive plan must be on record before significant design resources are invested, with the certain expectation that the documentation will expand as the project proceeds. This perspective is clearly quite different from the notion of starting with a brilliant circuit concept and immediately proceeding to develop it, in the hope of it becoming a product.

2.5.3. Design Compression

Maxim: Complete the basic design within the first few weeks of the project.

One of the easiest traps to fall into when undertaking a product development is to assume that the available time, delineated in a master schedule, will be spent in a fairly homogenous fashion, being a sequence of design studies and associated simulation experiments or verifications, occurring in a steady, constant density throughout the project. However, experience teaches that *very considerable time* must be allowed for all manner of work related to validation and presentation of the design, in preparation for a Design Review and transfer to mask layout, even when the "design" is well advanced.

For example, suppose one has assessed the need for a 12-week design period, and formally agreed to this schedule. Bearing in mind the maxim "First, the Finale", it can safely be assumed that the material needed for presentation at the

Design Review should be delivered for peer consideration at least one business week prior to the date set for that review. This material minimally consists of the following: A complete set of well-annotated schematics (clearly showing all device sizes and special layout notes, bias currents at the top and bottom of each branch, internal voltages, high-current branches, etc.); a comprehensive collection of simulation results (the good, the bad and the ugly: i.e. worst-case performance, for process, supply voltage and temperature corners, and with mismatch effects, rather than just the nominal results); and a text that puts the product into perspective, outlines any necessary theory and provides a component-by-component description of circuit operation, illustrated with more basic figures than the detailed schematics. Such a document is likely to take *at least* a week to prepare, and probably longer.

This suggests that one can expect to lose between one and four weeks at the end of the nominal design period. Prior to such "wrap-up" work, time must be allowed for numerous simulation studies to be performed on the *complete product,* even if the need for this has been minimized by careful attention to cell boundaries and through rigorous verification of these smaller entities. Analog cell interactions are common, whether through bias or supply lines, or subtle substrate coupling effects; some may be serious enough to warrant a significant change in overall structure. For a complex product, these top level simulations will be quite slow and time-consuming. In this connection, it is prudent to include all the ESD devices from the very start (one sometimes needs to devise special, pin-specific ESD protection schemes), and be sure to use a complete model of the package impedances and the mutual coupling between bond-wires. Keep in mind *that fast transistors are not aware of your expectations.* Given the slightest excuse to burst into song, they will.

When such time-sinks are anticipated and identified, a basic rule becomes apparent: the nominal design should be completed with a very short span of time, a matter of a few weeks, right at the start of the project, rather than allowed to gradually evolve over *the full length of time* scheduled for it. This overarching objective can be facilitated by adopting a sort of "imagineering" approach, in which the first item to be entered into the schematic capture domain is the *top level schematic,* which should be drawn as a pseudo-layout (e.g. see Figure 2.19). At this stage, it is acceptable to simply draw cosmetic boundaries for the main sections, whose sizes are estimated only approximately, knowing their general contents.

This layout-style schematic will show all the bond-pads to scale, the ESD protection devices and their power-busses, and allows one to connect up the blocks using actual "wires", provided that the cells are assigned pin symbols. Inside these temporary blocks can be ideal elements, such as independent and dependent sources, chosen to crudely represent the block's function, or perhaps some previously-developed cells. When this is completed, the top-level

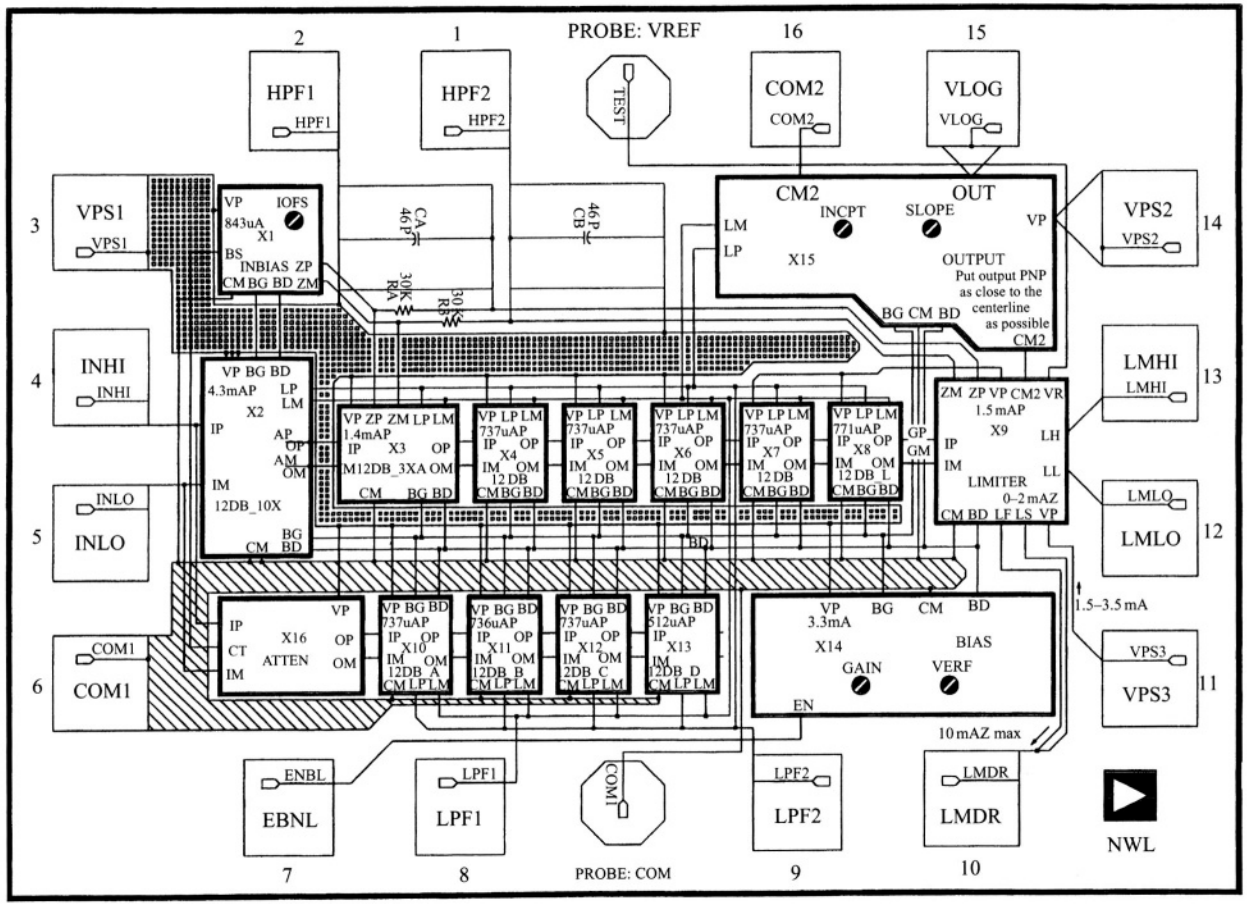


Figure 2.19. A schematic that is also an IC layout.

schematic should be error-free when generating a net list. One can thus have a *complete product schema by the end of the first day or two.* During the next few weeks, these blocks will be progressively fleshed out as real circuits, though still permissibly using some ideal elements, starting with the blocks most likely to prove challenging and needing the most invention. Although crucially important, the design of bias generators can usually be deferred until later in the project, although there may be exceptions as to any rule.

To readers unfamiliar with this approach to IC design, it may sound hopelessly idealistic and not the sort of thing one can really implement. However, the author has been using exactly this method for many years, and it is not merely workable, but very effective and time-efficient. It forces one to pay attention to the objectives – the finale – from the very start. It requires a full consideration of the pad sequence and the optimal location around the chip boundary. This in turn leads to a well-planned "street plan", showing the most important routes (such as those for the primary signals and the power supplies) and every one of the less critical, but nonetheless necessary, auxiliary connections, for biasing and control purposes. It invites one to use whatever means available to clearly indicate which of these routes must have a high current capacity or an especially low resistance (for example, by widening a "wire" into a narrow rectangle, and using cross-hatching to make these major routes very clear); or which must be extremely short or narrow, to minimize parasitic capacitances; or which paths must be kept apart to minimize coupling, or made equal in length for delay balancing, etc.

Special treatments of this sort are going to need articulation sooner or later, and to the extent that many such details can be foreseen and dealt with very early in the project, they are best got out of the way before the more troublesome mannerisms of the juvenile product begin to appear. The method is also a fine way to feel a strong sense of progress toward one's goals and to add a palpable reality to the development, on which stable platform the design can proceed with greater confidence. The alternative is to nibble at matters of cell design for weeks on end, a little here and a little there, with the hope that everything will fit together in the end; this is the antithesis of design mastery.

2.5.4. Fundamentals before Finesse

Maxim: Emphasize the use of strong basic forms; use clever tricks sparsely.

A study of a large cross-section of IC designs would almost certainly show that the ones that gave the least trouble in manufacturing were those which used strong, elegant techniques, often involving a minimal number of components, and appealing to holistic principles, in which one cell enters into a close and comfortable synergy with its surroundings. Conversely, products which are difficult to manufacture are invariably found to appeal to a lot of

"super-structure" to fix up one source of error after another, or address performance short-fall. In an actual limited study, looking for root-cause-of-failure in about two dozen products, and conducted about 17 years ago, the Pareto analysis revealed that "Design Methodology" was responsible for nearly 30% of all failures in first silicon. Adding in those failures due to "Difficulties in Simulation" and "ESD Protection" brought this up to 72%. The remainder of the failures could be traced to inadequate modeling accuracy, layout errors, omission of interconnect parasitics, and various errors in the schematics. In this particular study, none of the failures were due to manufacturing mistakes.

Although a limited and dated result, it does point to the importance of attending to *the fundamentals of design.* Some questions to ask at frequent intervals are: Is this component (in a cell) essential? When the Design Document is written, how will I justify its inclusion? What would be the impact on performance if it should be removed? Not all components should be excluded just because they play a minor role. Their combined contribution to robustness may be valuable. But in thinking at every turn about the *purpose* of adding one or more components to an otherwise satisfactory design, one can reduce the risk of unwittingly introducing future and possibly time-consuming problems.

2.5.5. Re-Utilization of Proven Cells

Maxim: Do not re-invent the wheel; adapt the trusted form.

This is actually a surprisingly hard lesson to learn. Those of us who enjoy cell innovation spend a lot of time thinking about alternative ways to achieve certain aspects of performance that have already been met numerous times before. Such activity is not to be discouraged; it is the well-spring of important new ideas, and may be considered an appropriate response to the previous maxim, reworded as: *Always be on the look-out for new fundamental forms.* Nevertheless, time-to-market pressures require that we re-utilize existing cells whenever possible. The savings in time, and *a potential* reduction of risk, come from several sources:

- The needed cell design (or something close) is already in hand.
- It will often be proven and de-bugged; a body of performance and test data for actual material will be available.
- The cell layout also already exists; while this may undergo some alterations in the new context, the general form of this layout and its subtleties can be preserved.
- Re-use eliminates time-wastage in chasing newly-invented bugs.

On the other hand, there are several reasons why cell re-use is not quite so easy:

- The needed performance will invariably differ (from slightly to radically) to that provided by the available cells, requiring varying degrees of redesign.
- The descriptive support of the cell may be minimal or even non-existent.
- The adoption of someone else's cell design without fully understanding it, and the *context* within which it was developed, can be hazardous. For example, taken in abstraction, an available voltage reference cell may appear to perform well, and the schematic annotation to the effect that "$Z_{OUT} < 1\,\Omega$" seems reassuring. However, the original usage of the cell did not require a low output impedance at 100 MHz, as does your application, and Z_{OUT} was actually measured at 10 kHz, although this was never noted. Without a meticulous assessment of its *suitability* to the present environment, this cell could contain the seeds of problems further down-stream.
- The available design may be on a different process technology to the one needed for the current project.

Closer consideration shows that there are really *two types of re-utilization.* The one that is generally discussed involves the adoption of someone else's work from a library of cells, found in an internal memorandum or company web page, presented at a design review, or by familiarity with the work of a team member. But an equally important class of re-utilization is that based on the proven concepts and cells that a designer carries around in his or her head. Skillful re-use of ideas, the essence of experience, is usually a far better basis for robust design than the opportunistic adaptation of somebody else's work.

2.5.6. Try to Break Your Circuits

Maxim: Don't pamper your circuits; make them confess their darkest secrets.

Designers enter into a kind of love affair with their circuits. Sometimes, this takes on a parental aspect, and due attention is paid to making sure that discipline is administered when needed. We are usually quite thorough in putting our progeny through a series of challenging experiences in readiness for the harsh realities of the world beyond the workstation screen. But there is also a curious inclination to be kind and considerate: we may avoid subjecting the design to more than it can bear. Such compassion for a circuit cell is unwise. The world of real applications will certainly not give your product an easy ride: neither should you.

An important function of the designer is to routinely and relentlessly push a cell design to the brink of disaster and then bring it back again to the placid

waters of normal operation. "Routinely" in this connection means at least several times a day, from the earliest moments all the way through to pre-layout final checks. "Relentlessly" means with no concern for the possibility that the design will break under stress. Such attempts to break the cell, or reveal its secrets or some hidden pathology, will include the use of numerous *parametric sweeps.* Most modern simulators allow a wide range of interactive sweep modes, in which any desired parameter can be identified and swept over massive ranges. Some of the more obvious:

- *Supply voltage*: if the nominal supply is 2.7–3.3 V, sweep it from 0 to 10V. You do not expect the circuit to work at zero, nor do you expect it to collapse in a heap at 10 V (though there may circumstances when this would be an unreasonable stress). Do this using both DC and time-domain sweeps. Use sweep-from-zero *and* sweep-to-zero exercises: these will tell you a lot about start-up and minimum supply limits. Perform these exaggerated supply sweeps at very high and very low temperatures, and using process corner models.
- *Temperature:* if the normal operating range is –35°C to +85°C, that should not prevent you *wondering* about what happens at –75°C or +175°C (the workstation will not melt) perhaps while using supply voltages at least 20% bigger or smaller than the nominal range. Frequently, one will observe several anomalies at temperature extremes. For example, the gain of an amplifier that is supposed to be 20 dB may show a sudden drop above 115°C. Since this is well above the required operating temperature, it could be ignored. Nonetheless, good design practice requires that one *immediately* picks up this trail and finds the root cause, even though a remedy may not be implemented. The discovery of all such pathologies revealed by swept-parameter experiments should be treated in this way. In many, many cases, these digressions lead to valuable new insights, and reveal incipient weaknesses that could threaten yields or result in field failures, when combined with some unhappy combination of supply voltage, temperature, process corners and device mismatches.
- *Do not stop there:* sweep *everything!* For example, sweep all sheet resistances from one half to twice their nominal value; BJT betas from a one-third to at least five times their nominal value; and so on. If it is found that the performance aspects that ought to be TAPs are not, one must ask why.

2.5.7. Use Corner Modeling Judiciously

Maxim: While "Corner Models" are often more myth and guesswork than definitive, put your prejudices aside and use them anyway: they can be most revealing.

The use of so-called Corner Models is somewhat unfocused. These models are generated by the team producing device characterization data for simulation purposes, and they invariably involve a certain amount of guesswork. For example, in a pure-bipolar process, the transistor models for one extreme may simultaneously (1) maximize all the junction resistances, including R_E, R_B, R_{BM} and R_C; (2) maximize all the junction capacitances, including C_{JE}, C_{JC} and C_{JS}; (3) minimize the saturation current I_S; (4) minimize the DC beta parameters, including BF; (5) maximize the transit time T_F, and so on. (The total number of parameters is more than 40 in the full set for a BJT, and most are treated in a similar fashion.) These extreme values give rise to what may be called the "SLOW" model, as a little consideration of the effects of these changes on circuit performance will show.

In addition, the "SLOW" library will set all resistors of every type to their maximum value, by using the maximum sheet resistance, the most extreme reduction in resistor width and the most extreme extension of resistor length. It will likewise set all the passive capacitors at their maximum value, by assuming the minimum oxide thickness and the largest expansion of the area. In some cases, this rigour will include the wiring parasitics, using a similar set of considerations. Similarly, other components, such as ESD and Schottky diodes and inductors available in the process are pushed to their "SLOW" corner. Of course, the "FAST" models reverse this process. The treatment of corners in a CMOS process is essentially the same, with similar objectives, although greater effort is expended to include the correlations between electrical parameters, based on a smaller set of physical parameters.

Note that, in using corner models, the designer is left determine the extreme temperatures and supply-voltage conditions which result in the most severe degradation in performance. A full matrix of results, for just one aspect of performance, requires no less than twenty-seven simulation runs: One uses the "SLOW", "NOMINAL" and "FAST" models, and in each case the minimum, nominal and maximum temperatures (say, – 60°C, +30°C, +130°C, even though actual operation may be limited to a smaller range – in the spirit of trying to "Break The Circuit", or at least exploring where it begins to sweat); these are repeated for the minimum, nominal and maximum supply voltage (say, 2.6, 3 and 6V). A convenient way to view these results is by using a set of three pages, one for each supply voltage, each comprising three panels, one panel for each model parameter set, and each of these having the swept parameter along the horizontal axis, and the three temperatures in each panel. If this is to be repeated for each of the critical parameters (which ought to correspond closely to the line items in the data sheet, where possible), hundreds of pages of results may be needed to fully capture the full (PVT) corner performance, and all these experiments will invariably (but unwisely) presume that matching remains perfect.

In practice, the use of these corner models is quite problematical, for several reasons. To begin with, they quite clearly represent a very extreme state of affairs, unlikely to occur *simultaneously* in practice, or even as individual extrema. Since "worst-case" values are assigned, these are presumably the limit values for which a production wafer would actually be *rejected.*[29] So, the first problem is whether to believe they are at all *realistic.* The second problem with corner testing is that it really does not show the worst case that might arise, when mismatches are included. Indeed, an otherwise flawlessly robust circuit might continue to work very well at the corners, *when all the devices match,* then collapse seriously into a mere shadow of its former self when realistic mismatches are included. Third, it may happen that local performance minima actually arise *somewhere inside* one of the ranges of worst-case extrema, which are not captured in corner studies. Or, it can arise from *a combination* of some unfortunately set of parameter values *and* certain mismatches. Fourth, these studies do not provide much insight, if any at all; they simple demonstrate a lack of robustness, without clearly pointing the way forward. Finally, it will be apparent that a huge amount of time will be needed to provide a comprehensive set of corner results. Regrettably, even a small change to the design may necessitate repeating these tedious procedures.

What we have here is a *most fundamental kind of trade-off*: that between time-to-market and risk. The use of comprehensive corner testing is inefficient. The objective of any product development is to first, exercise dominance over the material, and *dictate what the circuit shall be permitted to do,* rather than treating the challenge as something like science, which is the exploration of a domain not of one's own making, to try to understand its inner mysteries. The true purpose of one's studies throughout the design phase should be *the minimization of enigma and the maximization of insight.* As already stated, these objectives are best tackled by the routine use of *sensitivity* studies at every point in the design. If one minimizes all the major sensitivities independently, there is a high probability that the overall system will be inherently robust. Then, when small changes are made, one can be fairly sure about the consequences, and the need for time-consuming re-runs of the corners is minimized.

While these cautions are based on reasonable enough concerns, there is at least one reason why the use of corners may nonetheless be of benefit, and it is a little subtle. It was noted above that the algorithms built into the corner modeling include variations in resistor width (and other similar narrow dimensions). It has also been noted that component mismatches can destroy circuit integrity,

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29 These are based on measurements made on production-specific test sites, which are often placed at just five locations on the wafer, but sometimes embedded in the scribe lane between the chip boundaries.

and that to mitigate against these, one should routinely use equally-sized unit elements when building up large ratios or striving to maintain an exact equality of component value. Now, depending on one's schematic capture software, and the way in which these structures are defined, it is possible for errors to arise in the way the software interprets device scaling data. In turn, this may either reflect badly on the performance, or it can hide sensitivities.

For example, in that amplifier we developed (Figure 2.5), three $3\,k\Omega$ resistors were used in parallel to generate a $1\,k\Omega$ component, and four of these same units were connected in series to generate a $12\,k\Omega$ component. Suppose one first decided to make each resistor $5\,\mu m$ wide and $15\,\mu m$ long, when the sheet resistance is $1\,k\Omega/square$. Then, in the schematic capture environment, the $3\,k\Omega$ element might be denoted as a single resistor with a length of 15 ("microns" being assumed by the program) and a width of $3*5$, the multiplier being necessary to satisfy the subsequent verification of the layout against the schematic. Likewise, we might denote the $12\,k\Omega$ element as a single resistor with a length of $4*15$ and a width of 5. These will automatically be calculated in the net-lister and the simulation results will be correct.

However, the width of $3*5$ may be treated as 15 and the length of $4*15$ may be treated as 60; information about *structure* is thereby lost. The layout verification software will be happy, because it is told to measure the *total width* (for the $3\,k\Omega$ resistor) and the *total length* (for the $12\,k\Omega$ resistor). But now we apply the corner models, let's say, the SLOW models. With this representation, the $1\,k\Omega$ resistor width is reduced by only one delta-width unit on each side (just by way of example, say, $-0.2\,\mu m$), and the $15\,\mu m$ becomes $14.6\,\mu m$, while its length is increased by only one delta-length unit at each end (say, by $+0.35\,\mu m$), to $15.7\,\mu m$. Its apparent "worst-case" value (neglecting the sheet resistance, which affect all units equally) is thus $1.0753\,k\Omega = 15.7\,\mu m/14.6\,\mu m$. Working through similar arithmetic for the $12\,k\Omega$ resistor, it has an apparent value of $13.196\,k\Omega = 60.7\,\mu m/4.6\,\mu m$. So the ratio is no longer 12, but 12.27. This is likely to be a "false positive": the use of strict unit elements will *guarantee* this ratio in the presence of any width and length variations.

Counterexamples arise in which less than careful attention to this sort of possibility will *obscure* real sensitivities. It should be added that not all schematic-capture software will suffer from this particular source of error. When in doubt, the safest approach is to explicitly include all of the units in such an ensemble, even if the page gets a little cluttered, or relegate them to a sub-circuit. An secondary advantage of the explicit approach is that it forces one to remain *fully aware of the physical reality* of one's circuit, and to remain focused on the constraints of layout. For example, resistor dimensions may snap to $0.1\,\mu m$ increments, so avoid the use of ohmic values in very precise applications, and state this value in terms of length and width. allowing the netlister's knowledge of sheet resistance calculate the ohms.

Always keep in mind that there is never a worst case in the on-going production statistics for a product. There are good cases and there are bad cases. The art of design is to ensure that there are far more of the former than the latter.

2.5.8. Use Large-Signal Time-Domain Methods

Maxim: Do not trust small-signal simulations; always check responses to fast edges.

Elaborate use of, and an excessive reliance on, Bode plots and other small-signal methods is extremely risky. One might use these initially, and briefly, to generally position the AC behavior of a circuit, and occasionally as the design progresses, and again in generating the supporting documentation for a Design Review. But as a general rule, the circuit should be subjected to strenuous time-domain exercises during the product development. These will sometimes use small test signals (say, millivolts), during which the correspondence between the AC gain/phase results and the time-domain should be very good.

On the other hand, it is not at all uncommon for these little "tickler" signals to persuade the circuit to launch into a swell of oscillations, if it is prone to do so. This can happen even when the AC results appear to be satisfactory, but perhaps one has paid to much attention to the gain magnitude, which appears to roll off gently and benignly, with insufficient concern for the phase. Even when these really do predict a satisfactory stability margin, only slight deviations from a quiescent bias point can quickly change all that, in many classes of circuits.

When pursuing such experiments, one may also be inclined to choose a rise/fall time for the excitation that is consistent with the system requirements, say, in the 10ns range for a 10 MHz amplifier, having an intrinsic rise-time of about 35 ns. However, the circuit may exhibit some unexpected pathology when driven from very fast edges, perhaps as rapid as 10 ps. Though the circuit will never encounter such signals in practice, the lessons one can learn from ultra-wideband excitation are often unexpectedly valuable, revealing nuances in the response that call for immediate remedial action. Such investigations should be conducted over the full (even an extreme) range of temperature, and at process corners, even when the behavior under nominal conditions appears trouble-free. In this connection, it is also important to use fast excitation sources when the circuit is driven with much larger signals. Overdrive conditions may reveal yet other conditional oscillations, as devices approach saturation or their bias conditions cause a large change in device inertia.

2.5.9. Use Back-Annotation of Parasitics

Maxim: In simulations, a "wire" is just a node of zero extent. But an integrated circuit has many long wires which have capacitance to substrate and to each other. Don't neglect these.

Many of the differences that arise between the measurements made on silicon circuits and the predictions of simulation can be traced to these parasitic capacitances. One is inclined to neglect the extra rigor needed to extract these from the layout and verify performance with their reactances included, particularly when the circuit is only required to meet some modest low-frequency objectives. Clearly, when high frequencies are involved, such back annotation is mandatory. Many problems can arise from the loading of cells by the shunt capacitances to the substrate (particularly when using low-g_m CMOS, that may look fine until one adds a few femtofarads on its output); or from the coupling between these interconnects; or from mismatches in these capacitances that can affect certain aspects of circuit balance.

In speaking of capacitive coupling to "the substrate", one is bound to ask: What node is that? It is certainly not "ground", that is, the external reference plane that is customarily regarded as a node of "zero potential", identified in SPICE by the node name "0". The choice will vary from one technology to another. It may be satisfactory to use the paddle on which the circuit is mounted as that node; be aware that this will differ in potential from the external ground when the full package model is included, which should be standard practice whenever a modern high-speed technology is used – for whatever purpose. It may be necessary to divide the chip area into different zones for the purpose of defining these various "local grounds".

In a similar way, be very careful in selecting the appropriate node for the substrate connection to all devices (not only transistors, but also for the supermodels of resistors and capacitors). This should *never* be "0" in a monolithic product, and it may not always be correct to assign it the node name for the paddle. Frequently, different areas of an integrated system will need to use independent node names to identify the appropriate substrate potential for the various devices or blocks. The most accurate identification and partitioning of these important nodes can usually be determined only after reviewing a preliminary layout.

2.5.10. Make Your Intentions Clear

Maxim: Understanding every subtle detail and fine point of your masterful design is great. Now, take steps to ensure that everyone else on the team does.

We are inclined to assume that what is "obvious" and "only common sense" will be apparent with equal force to our co-workers. However, it often will not be. This is not a commentary on their intelligence, but invariably due to a lack of clarity in stating your precise intentions. One of the more critical team interfaces is between the schematics and the layout designer. If you are lucky enough to work with very experienced colleagues, you may be able to take the risk of presuming that they will do certain things just the way you would

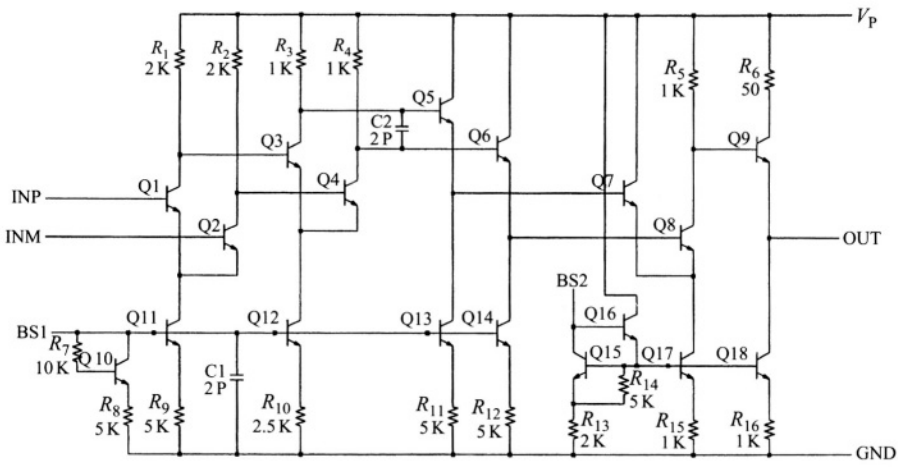


Figure 2.20. A lazily-constructed schematic having numerous ambiguities.

(i.e. the way which is absolutely critical to ensuring performance, but you did not say so).

Consider a simple example in the annotation of a schematic. Figure 2.20 shows a lazy-minded drawing of the circuit. Try writing a list of at least ten mistakes that could be made by the layout designer, acting solely on this schematic. Now examine Figure 2.21, which avoids these traps by explicitly noting certain critical requirements. Of special importance are those related to metal connections and the identification of locally merged nodes. The simulator will be quite indifferent to how the schematic is drawn in these areas: a node is just a node, having zero physical extent. But the silicon realization will be significantly impacted by a lack of attention to the use such local merging, because of the resistance of the metal traces, which will in some cases have non-local currents flowing through them. These resistances may need to be extracted from an interim layout. However, when properly indicated on the schematic and connected accordingly, and balanced in length if necessary, these small intra-connect resistances will often not matter. If nodes are allowed to be incorrectly connected one should be aware of the potential for malfunction.

2.5.11. Dubious Value of Check Lists

Maxim: Antibiotics are valuable. But it's much better to stay healthy.

Relying on check lists to achieve a robust design is hazardous. When used prior to a Design- or Layout Review, they may be of value in catching a few straggling indiscretions. Consulted religiously on a daily basis throughout the design and layout phase, they might be useful in trapping mistakes in the

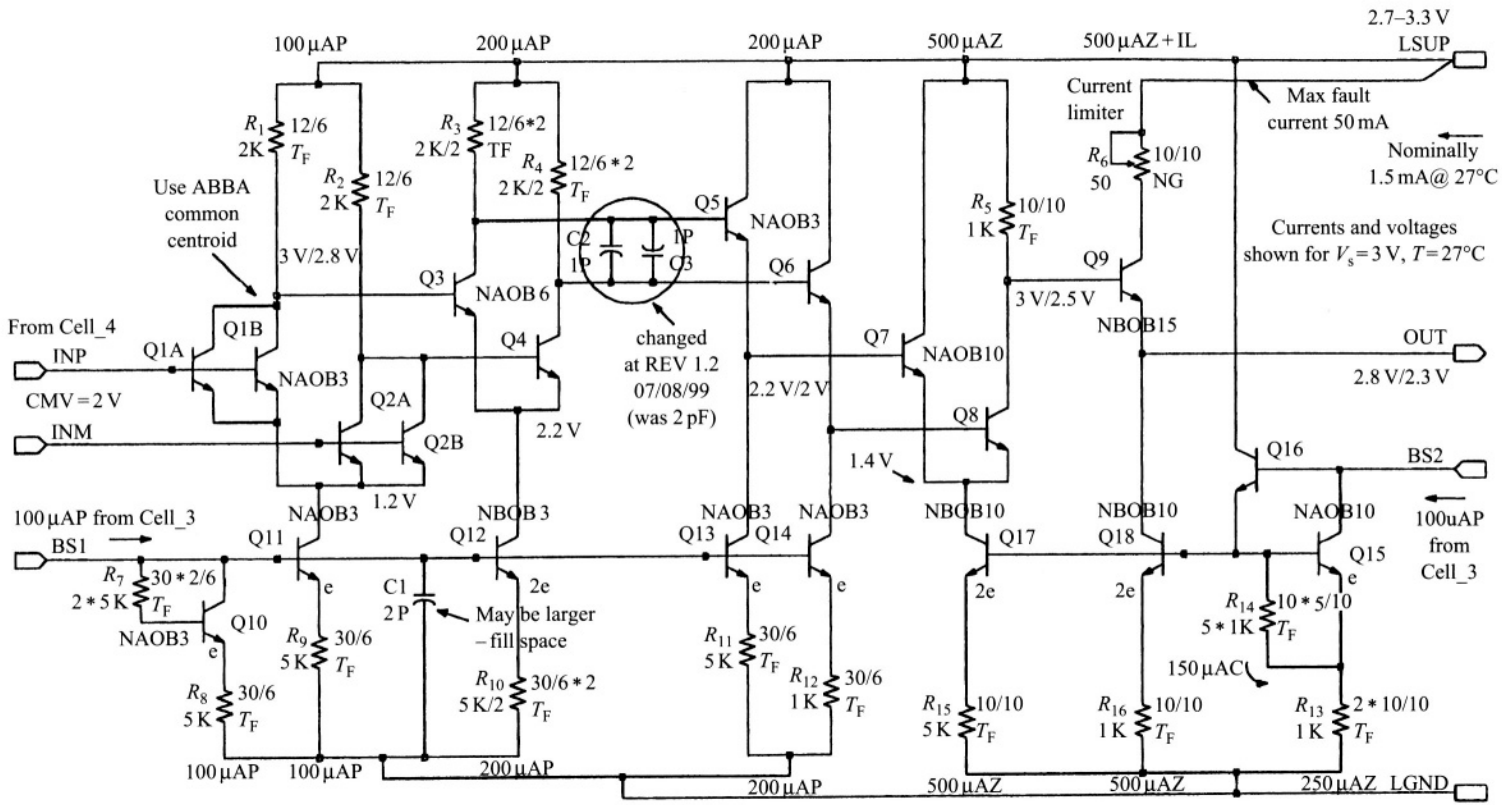


Figure 2.21. Self-documenting schematic identifying special construction needed at layout.

making. But there is a danger in either case that one may gravitate toward a mode of design that is reminiscent of painting by numbers, or responding to a multiple-choice questionnaire; that is, by reacting to a prompt for some *pre-specified* action, rather than by independently deciding what the right action should be at each juncture.

Check lists tend to be superficial, stating broad and often comically commonsensical truths. They touch on a limited set of issues, and may overlook major areas of concern. Some of the questions (such as "Did you simulate your circuit over a full range of operating conditions?") will appear downright stupid and naïve. These may prompt the person sincerely wishing to extract some value from the checking process to wonder whether to spend any further time with the rest of such rules. At the other extreme, specific operational problems that have arisen in connection with previous developments may seem too arcane to include in a general list.

However, check-lists have their place. In the pursuit of robust design, and the minimization of time-to-market, it probably does no harm to review the issues they raise, if time is available in the rush to get your product into wafer-processing. You might seek ways to add your experiences to these lists, particularly those relating to unexpected anomalies. (A well-structured system for the capture and retrieval of information is needed.) In the spirit of Total Quality Management (TQM), the check lists should continue to grow in value, particularly to new recruits, as additional non-obvious pitfalls and sources of failure become apparent.

2.5.12. Use the "Ten Things That Will Fail" Test

Maxim: After finishing the design and layout, subject your product to an end-of-term exam.

We have struggled with many challenges in getting our product this far, to the layout stage, and may understandably be disinclined to try yet more ways to break this prize design. But it is far better to discover these, if they exist, before the costs begin to escalate, and delays accumulate in wafer fabrication. So the idea here is to project one's mind forward to the time when first silicon will be available, and vigorously play a few more. What if? scenarios, in an attempt to find the skeletons in the closet. Ask such questions as "When the supplies are applied to first silicon and the currents are found to be excessive, how might that occur?". One possibility: an additional ESD diode somehow got added at the last minute, and a full re-check of the layout against the schematic was not conducted, since "this is such a trivial change". But it was wired in *reverse polarity.* Another scenario: You did a pretty good job of indicating which interconnections must be wide, or short. But have you included the resistance of the

longer, unspecified traces back into the circuit? There has been much gnashing of the teeth over such "minor" details!

Attempt to draw up a list of ten such errant possibilities; then, implement stern remedies.

2.6. Conclusion

The path from concept to customer is unquestionably a tortuous one. Choices of architecture, cell structure and technology must be made. Many vexing trade-offs will have to be faced; these are in every respect human decisions based on experience and judgment, sometimes arbitrary but never algorithmic. Many errors of both omission and commission can occur in the development of an integrated-circuit product. Making the best choices about *all aspects of performance* is just the beginning of a long journey, but nonetheless the essential starting point. It is given greater substance by generating the data sheet in as complete a form and possible, leaving placeholders for all the characterization graphs that will eventually be included, and describing all the features, applications and circuit theory, as if the part really existed. This will be your anchor through the entire journey to the customer's door.

The bulk of the design should be *compressed* into the first few weeks of the development, leaving plenty of time for validation and verification of robustness. Begin by preparing a top schematic that is a *pseudo-layout,* with all sections clearly identified, of about the correct size and positioned correctly on the floor-plan. As the inner details gradually fill in, make sure that all of the relevant details are captured in this one document, in the same spirit as in preparing a set of architectural drawings. While supporting documentation will be essential for a Design Review, for Product Engineering purposes, and as part of a permanent record, the schematics themselves should be a complete, detailed recipe for the construction of the layout, as well as a means of communication to all who need to understand the product.

The extreme sensitivity of an analog circuit to production parameters poses especially daunting challenges, in finding a suitable overall form, in realizing optimal cell topologies and in rationalizing and regulating their operation. Conflicts will need to be resolved by making compromises, deciding between many possible directions and trade-offs, minimizing every conceivable sensitivity, and much else of a circuit design nature. Furthermore, one must enter deeply into a consideration of worst-case behavior, using corner models, extreme temperatures and the limit values for supply voltage. After the basic electrical design, the most minute details of the chip layout will need your full consideration, as well as the numerous ways in which the package will impact performance, such as chip stresses, bond-wire reactances, substrate coupling

over a noisy header, and much else of an highly practical nature. Thermal management is often an essential aspect of the packaging phase.

This chapter has presented a cross-section of representative trade-offs, and proposed a few methods to ensure robustness. It will be apparent that this is not by any means the whole story. The matter of substrate coupling is becoming very important, not only in mixed-signal systems on a chip, but also in pure analog and strictly digital products. The topic of designing for testability similarly needs close attention and planning.

Circuits are not products. Circuit design is but the starting point for the numerous corrections, adjustments and adaptations that will inevitably follow, accumulating increasing delays as the project rolls along, unless the author's experience is an unfortunate aberration.

Chapter 3

TRADE-OFFS IN CMOS VLSI CIRCUITS

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3.1. Introduction

The pace of integrated circuit (IC) technology over the past three decades is well characterized by Moore's law. It was noted in 1965 by Gordon Moore [1] that the integration density of the first commercial ICs doubled approximately every year. A prediction was made that the economically effective integration density, that is, the number of transistors on an IC leading to the minimum cost per integrated component, will continue to double every year for another decade. This prediction has held true through the early 1970s. In 1975, the prediction was revised [2] to suggest a new, slower rate of growth – the transistor count doubling every two years. This new trend of exponential growth of IC complexity has become widely known as "Moore's Law". As a result, since the start of commercial production of ICs in the early 1960s, circuit complexity has risen from a few transistors to hundreds of millions of transistors operating concurrently on a single monolithic substrate. Furthermore, Moore's law is expected to continue at a comparable pace for at least another decade [3].

The evolution of integration density of microprocessor and memory ICs is shown in Figure 3.1 along with the original prediction of [1]. As seen from the data illustrated in Figure 3.1, DRAM IC complexity has been growing at an even higher rate, quadrupling roughly every three years. The progress of microprocessor clock frequencies is shown in Figure 3.2. Associated with increasing IC complexity and clock speed is an exponential increase in overall microprocessor performance (doubling every 18–24 months). This performance trend has also been referred to as Moore's law.

Such spectacular progress could not have been sustained for three decades without multiple trade-off decisions to manage the increasing complexity of ICs at the system, circuit and physical levels. The entire field of engineering can be described as the art and science of understanding and implementing trade-offs. The topic of IC design is no exception; rather, this field is an ideal example of how trade-offs drive the design process. In fact, the progress of VLSI technology makes the topic of trade-offs in the IC design process particularly instructive.

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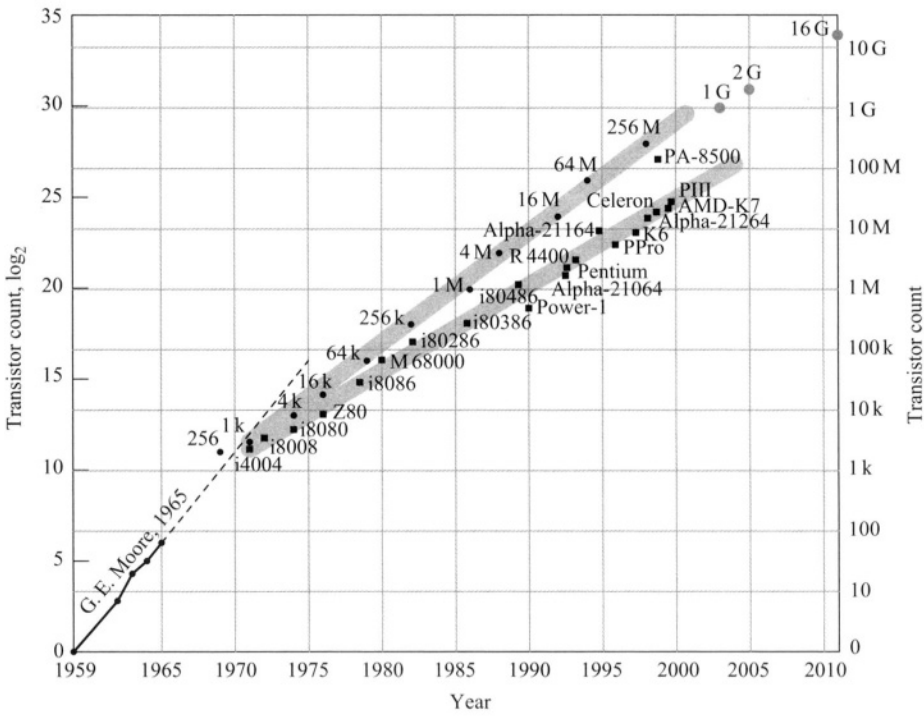


Figure 3.1. Evolution of transistor count of CPU/microprocessor and memory ICs. In the lower left corner, the original Moore's data [1] is displayed followed by the extrapolated prediction (dashed line).

The evolution of design criteria in CMOS ICs is illustrated in Figure 3.3. Design paradigm shifts shown in the figure are due to advances in the fabrication technology and the emergence of new applications. In the 1970s, yield concerns served as the primary limit to IC integration density and, as a consequence, die area was the primary issue in the IC design process. With advances in fabrication technology, yield limitations became less restricting, permitting the rise of circuit speed in the 1980s as the criterion with the highest level of priority. At the same time, new applications such as satellite electronics, digital wrist watches, portable calculators and pacemakers established a new design concept – design for ultra-low power. As device scaling progressed and a greater number of components were integrated onto a single die, on-chip power dissipation began to produce significant economic and technical difficulties. While the market for high-performance circuits could support the added cost, the design process in the 1990s has focused on optimizing speed and power, borrowing certain approaches from the ultra-low power design

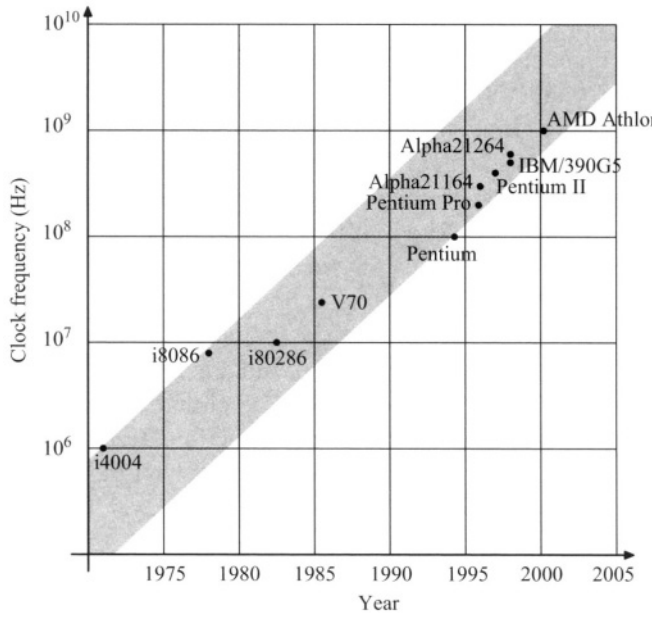


Figure 3.2. Evolution of microprocessor clock frequencies.

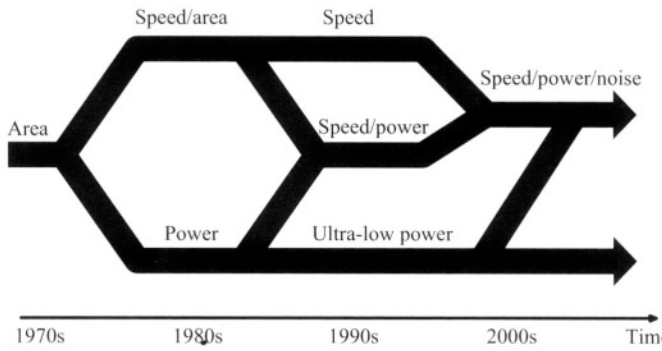


Figure 3.3. Evolution of design goals in CMOS ICs.

methodologies. Concurrently, a variety of portable electronic devices further increased the demand for power efficient and ultra-low power ICs. A continuing increase in circuit power dissipation exacerbated system price and performance, making power a primary design metric across an entire range of applications. Furthermore, aggressive device scaling and increasing circuit complexity are causing severe noise (or signal integrity) issues in VLSI circuits. Ignoring the effect of noise is no longer possible in the design of high-speed digital ICs.

These changes are reflected in the convergence of "speed" and "speed/power" trends to "speed/power/noise," as depicted in Figure 3.3.

Current semiconductor fabrication technology is able to place an entire system on a single die. Implementation of such systems-on-a-chip (SoC) has created new constraints and placed different requirements on the design process. The challenge of the VLSI design process has become the difficult problem of determining the proper set of trade-offs across high levels of complexity from system specification to the lowest physical circuit and layout details.

The material presented in this chapter on trade-offs in VLSI-based CMOS circuits is not intended to be comprehensive; rather, effort is made to summarize the primary trends and provide the reader with a general understanding of the topic of trade-offs in digital VLSI-based CMOS circuits. All types of trade-offs are available at different levels of system abstraction. Trade-offs at the higher levels of abstraction such as at the system and behavioral levels are highly application specific and difficult to systematize. These levels are not specifically treated in this chapter.

The chapter is organized as follows. Different VLSI design criteria are summarized in Section 3.2. Design trade-offs at various levels of design abstraction are considered in further sections. Architectural (register transfer) level trade-offs are treated in Section 3.3. Circuit trade-offs are considered in Section 3.4. Physical and process level trade-offs are discussed in Sections 3.5 and 3.6, respectively. The chapter closes in Section 3.7 with some conclusions and comments on future trends in trade-offs in CMOS-based VLSI systems. The terms and notations used throughout the chapter are defined in the following Glossary.

3.2. Design Criteria

Traditionally, there have been three primary figures of merit in the digital circuit design process: area, delay and power. Increasing speed, physical size, complexity and scaling of ICs have produced additional metrics to be considered as major design criteria, such as reliability, testability, noise tolerance, packaging performance and design productivity. A brief survey of these design criteria is provided in the following subsections.

3.2.1. Area

Die area is synonymous with "cost" in the VLSI field as die area has the greatest impact on die fabrication costs. Larger area reduces the number of dies that can fit onto a wafer, leading to a linear increase in processing and material costs. Much more significant, however, is the impact of die area on die yield. The yield, or the fraction of the fabricated ICs that are fully functional [4], falls sharply with die area, as shown in Figure 3.4. As a result, die manufacturing

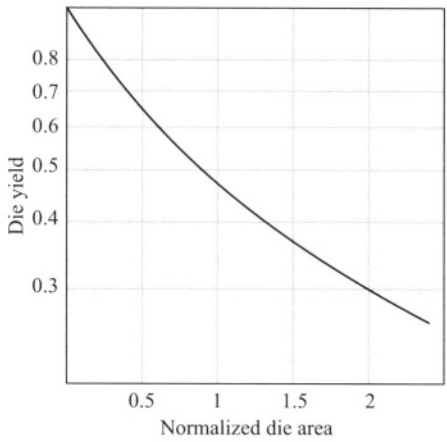


Figure 3.4. Dependence of yield on die area [6]. The area is scaled by the average defect density. The numbers on the abscissa provide the average number of defects per die.

costs quickly become prohibitive beyond some size determined by the process technology and the defect density characteristics of the manufacturing facility.

3.2.2. Speed

Although circuit performance is highly application specific, lower circuit propagation delay almost always leads to higher performance in digital systems. For this reason, VLSI performance is primarily discussed in terms of circuit speed (i.e. circuit propagation delay or the maximum clock frequency of a synchronous circuit) [4]. Therefore, the area-delay characteristics of a circuit are quite similar to the greater price-performance characteristics of that same circuit.

3.2.3. Power

Power dissipation in VLSI circuits also has a profound impact on both price and performance. High power dissipation penalizes the overall system since more advanced packaging and heat removal technology are necessary. Limits on power dissipation in advanced packaging can place an upper bound on economically viable integration densities before die yield limits the maximum die size. Higher power dissipation not only limits a circuit through packaging issues but also requires wider on-chip and off-chip power buses (reducing the wiring capacity available for the signal interconnect), larger on-board bypass capacitors, and often more complicated power supplies. These factors increase the system size and cost. Furthermore, portable electronic devices are limited by battery life (i.e. the time of autonomous operation); therefore, power is also a

system performance metric. In fact, the primary reason for CMOS dominating the VLSI era has been the low power dissipation characteristics of static CMOS circuits.

3.2.4. Design Productivity

Technology scaling has brought new design challenges. These challenges are caused by two primary issues. The first issue is the increasing complexity of the systems being designed. During most of the history of the semiconductor industry, die fabrication has been the primary constraining factor in circuit complexity. The design task had been to make the most effective use of the limited silicon real estate. This situation has changed radically. The capabilities of the semiconductor manufacturing industry have far outpaced those of the IC design industry. This "design gap" is well demonstrated by the graph shown in Figure 3.5. Current multimillion transistor systems require huge amounts of highly skilled non-recurring engineering (NRE) effort. As the design productivity gap widens and NRE design cycles become longer, design teams have become larger and NRE design costs have become a larger fraction of the total cost. This trend has limited the development of high complexity SoCs to those applications where the large NRE can be amortized over a high volume of products, such as RAMs and microprocessors. The large demand on NRE is further exacerbated when the circuits operate at high levels of performance, requiring significantly more design effort.

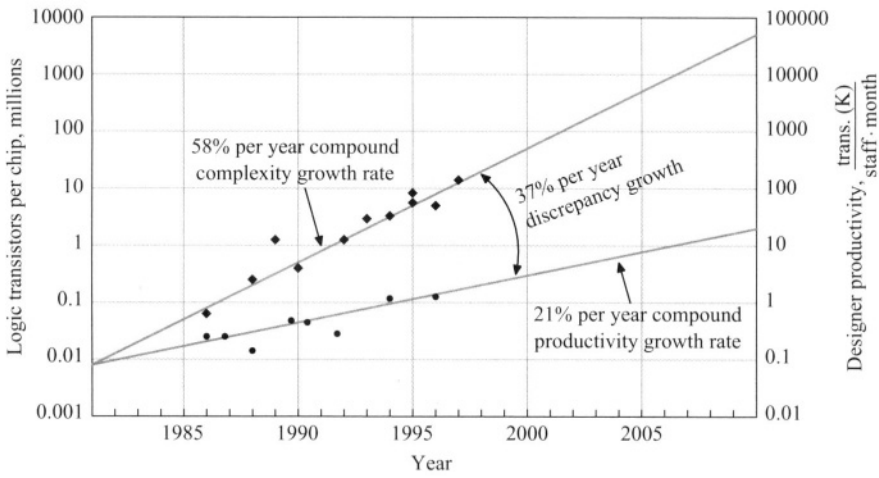


Figure 3.5. The design productivity gap [3].

In addition to the issue of cost, insufficient design productivity has made the time-to-market longer and less predictable. This NRE to recurring engineering (RE) issue has become critical within the semiconductor industry. The current pace of technology is shrinking the product life cycle, creating windows of opportunity for many products that are measured in months. Therefore, timely market introduction is paramount. Missing a product delivery deadline is extremely costly and can jeopardize the commercial success of a product. Large design teams may shorten the average development time but often do not prevent design deadline slips. Trading off product capabilities and features for less development effort to meet time-to-market constraints is often unavoidable.

3.2.5. Testability

Another challenge related to increasing system complexity lies in the area of testing, specifically debug testing (as compared to production testing). The number of distinct stable signal patterns a digital system can assume increases exponentially with the number of inputs and the number of registers storing the internal states. A state (i.e. a logic value) of a circuit node is typically not directly accessible and must be shifted to the output pins of an IC. This process makes the cost of exhaustive testing prohibitive for even relatively simple circuits. Limited testing of a complex system has become exorbitant unless special provisions are made during the design process to ensure that the testing process is more effective. Thus, a moderate sacrifice in area and speed is justified since the increased die manufacturing cost and decreased performance are compensated by a vast increase in system testability. Even with such added measures, the cost of testing per transistor has not changed significantly over the years, whereas manufacturing costs have plummeted exponentially. As a result, the portion of the test costs in terms of the total cost has grown. If current trends continue, this share will surpass all other cost components within a few years [7]. Forecasts of the number of transistors per I/O signal pin and the cost of testers for high-performance ICs are shown in Figure 3.6. The number of I/O pins increases moderately with time resulting in a large increase in the number of transistors per I/O pin. The time required to test multimillion transistor logic through dozens to hundreds of pins is not realistic, necessitating the extensive use of built-in self-test (BIST) structures. Thus, due to the high cost and limited throughput of test equipment and support personnel, a moderate reduction in test time can produce a considerable reduction in total project cost.

3.2.6. Reliability

Another source of circuit and physical problems is the smaller dimensions of the circuit elements. Changing physical dimensions and increasing

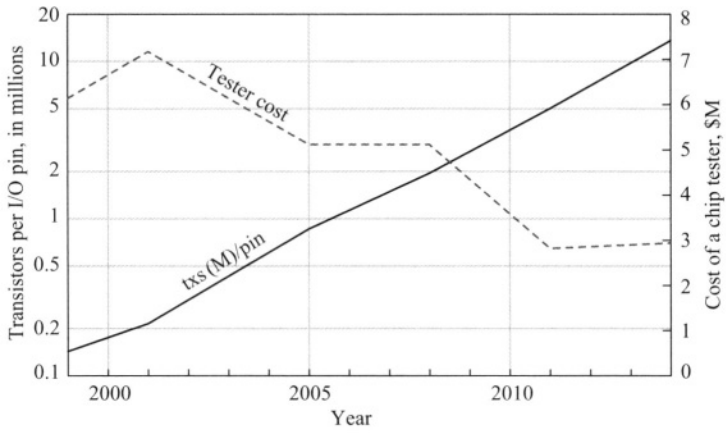


Figure 3.6. The forecast of transistor per signal I/O pin ratio and the forecast of high-performance tester cost (based on data from [3]).

speed has made reliability, packaging, and noise constraints more difficult to satisfy.

Scaling of device feature sizes without a proportional reduction in the supply voltage leads to higher electric fields, exacerbating many reliability concerns. Breakdown caused by high electric fields is one of the primary failure mechanisms. An example of a problem caused by high electric fields is that these fields give rise to hot electrons which tunnel from the channel into the gate oxide causing long-term reliability problems such as threshold voltage variations and transconductance degradation. High electric fields also produce carrier multiplication and substrate leakage current [5]. Excessive current densities in the metal lines cause electromigration problems: the metal ions are moved from the crystal lattice by colliding with the electrons propagating through the conductor [8]. The resulting voids and hillocks create open and short circuits, leading to permanent circuit failure. Electromigration can become a limitation at greater integration densities and finer feature sizes [9].

3.2.7. Noise Tolerance

Noise rejection and signal regeneration properties are two of the principal advantages of digital circuits. Nevertheless, many types of noise sources are present in VLSI systems. Inter- and intra-layer capacitive and inductive coupling of interconnect, as illustrated in Figure 3.7, results in increased delay, waveform degradation, and most importantly, the possibility of an erroneous interpretation of the digital signals [10,12,17,18]. Substrate currents result in substrate coupling which is particularly critical in dynamic

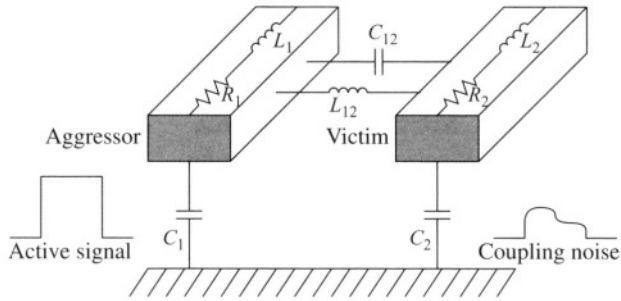


Figure 3.7. Cross-coupled interconnect noise in ICs. An active transition on an aggressor line induces a coupling noise voltage on a victim line.

circuits where a high impedance node can be easily affected [11]. As IC power consumption increases, the supply current has risen rapidly, currently reaching tens of amperes in high-performance ICs. The distribution of such high currents over increasingly larger die areas has produced challenging noise problems [5,13,14]. Due to the resistance of the power supply lines, significant *IR* voltage drops are created across the power buses, increasing the signal delay and delay uncertainty [15]. Another problem related to power distribution is simultaneous switching noise: as many amperes of current are switched on and off in subnanosecond time periods, the inductive voltage drops across the on-chip power lines and off-chip package bonding wires induce unacceptable voltage variations across the power rails [16]. Faster clock rates create higher slew rates of the signal waveforms, increasing the on-chip noise. Issues of signal integrity necessitate considering the analog nature of digital signals. These noise sources can potentially cause a circuit to both slow down and malfunction. Mitigating these noise problems has become a major VLSI challenge.

3.2.8. Packaging

Packaging is another important criterion requiring serious consideration in the design process. Packaging imposes many limits on an IC: heat dissipation, packaging price overhead, number of pins, circuit bandwidth, input cross-coupling noise, simultaneous switching noise, etc. The performance, price and power dissipation of a product are all affected (and often constrained) by the target package.

3.2.9. General Considerations

A few comments on power dissipation, technology scaling and VLSI design methodologies are offered in this section so as to better understand the trade-offs

discussed later in this chapter. These few paragraphs provide a synopsis of highly complicated topics important to the CMOS VLSI circuit design process.

Power dissipation in CMOS VLSI circuits. There are three primary components of power dissipation in CMOS circuits:

$$\begin{aligned} P_{\text{total}} &= P_{\text{dynamic}} + P_{\text{sc}} + P_{\text{leakage}} \\ &= C V_{\text{DD}}^2 f_{\text{switch}} + \tfrac{1}{2} I_{\text{peak}} t_{\text{base}} V_{\text{DD}} f_{\text{switch}} + I_{\text{leakage}} V_{\text{DD}} \end{aligned} \tag{3.1}$$

The dynamic power P_{dynamic} accounts for the energy dissipated in charging and discharging the nodal capacitances. When a capacitor C is charged, $C V_{\text{DD}}^2/2$ joules of energy is stored on the capacitor. An equivalent amount of energy is dissipated on the interconnect and transistors that are being charged. In the discharge phase, $C V_{\text{DD}}^2/2$ joules of energy that are stored on the capacitor is dissipated on the transistors and interconnect through the discharge path as shown in Figure 3.8. Thus, the total energy expended in the charge/discharge cycle is $C V_{\text{DD}}^2$. The average dynamic power is the $C V_{\text{DD}}^2$ amount of energy times the average frequency of the charge/discharge cycle f_{switch}, producing the well-known expression for dynamic power in CMOS circuits, $C V_{\text{DD}}^2 f_{\text{switch}}$.

A short-circuit current flows in a static CMOS gate when a conductive path exists from the power rail to the ground rail. It is possible for such a path to exist when a signal at one of the gate inputs transitions, passing through intermediate voltage levels [19–23]. For a static CMOS gate, this voltage range is from the n-type transistor threshold V_{Tn}, the voltage at which the n-type transistors turn on, to $V_{\text{DD}} + V_{\text{Tp}}$, the voltage at which the p-type transistors cut off. Within this voltage range, both of the pull-up and pull-down networks conduct current, producing short-circuit current, as exemplified in Figure 3.9. The period of time when this conductive path exists is denoted as t_{base} in (3.1). An analytical expression [24] that characterizes the short-circuit power P_{sc} that exhibits 15% accuracy for a wide variety of RC loads based on the Sakurai alpha-power law

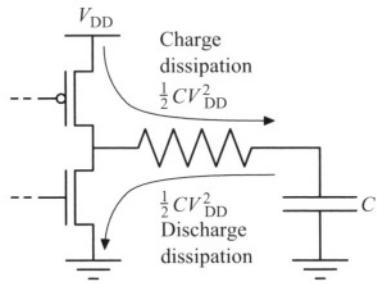


Figure 3.8. Energy dissipation during the charge/discharge cycle.

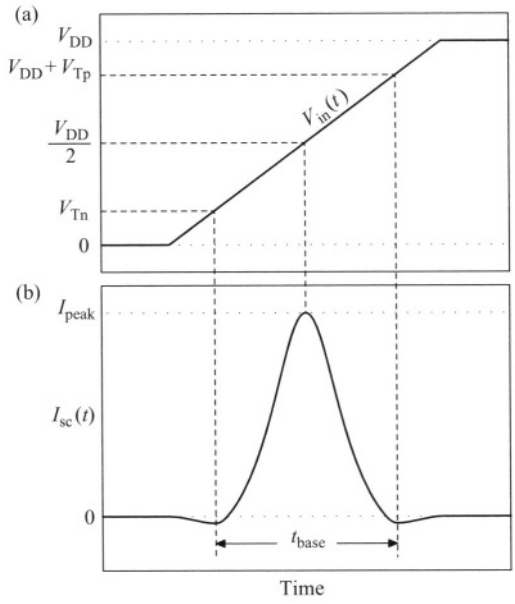


Figure 3.9. Short-circuit current waveform of a CMOS gate. (a) Ramp-shaped input waveform, (b) short-circuit current waveform.

model [25] is:

$$P_{sc} = \left| \ln \left(\frac{V_{Tn}}{V_{DD} + V_{Tp}} \right) \right| (R_{tr}C + RC)\, I_{peak}\, V_{DD}\, f_{switch} \qquad (3.2)$$

where $R_{tr} = V_{d0}/I_{d0}$ is alpha-power model effective transistor resistance in the linear region of operation.

The leakage current $I_{leakage}$ in a transistor is the current that flows between the power terminals in the absence of switching, giving rise to a leakage power component $P_{leakage}$. Typically, the dynamic power is the dominant power component, contributing 70–90% or more of the total power dissipation. Therefore, the most effective strategy for reducing the total power dissipation is to reduce the dynamic dissipation. For example, the quadratic dependence of the dynamic power on V_{DD} implies that lowering V_{DD} is an effective way to reduce both the dynamic and total power dissipation.

Technology scaling. The exponential growth of IC complexity has been largely driven by improvements in semiconductor fabrication technologies due to both technology scaling and defect density reduction. Shrinking the size of the circuit elements addresses all three of the "classical" VLSI design criteria. Capacitive loads within CMOS circuits are reduced as circuit elements become

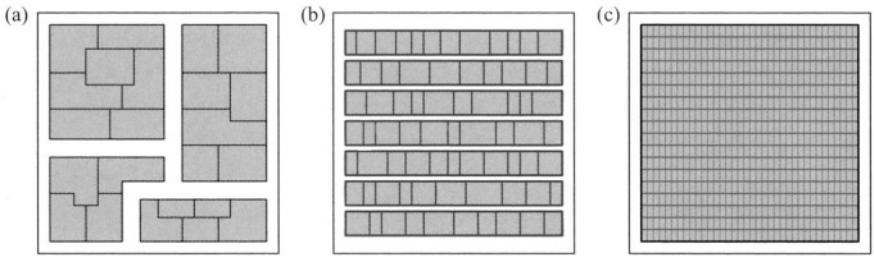


Figure 3.10. Different design approaches. (a) full custom – most laborious but most flexible, the size, shape and placement of the circuit components are freely tailored; (b) standard cell – the circuit is composed of logic gates aligned in rows of fixed height with routing channels between the rows, a library of standard logic cells is compiled prior to the design implementation and connected by metalization layers; (c) channelless gate array – wafers containing arrays of transistor cells are prefabricated and the transistors are interconnected to form a target circuit function during the metalization steps.

smaller, enhancing the delay characteristics. Circuits require less area, thereby lowering manufacturing costs, permitting the on-chip integration of larger and more complex circuits. To maintain a constant electric field, the supply voltage is often reduced. As a result, less energy is required to charge (and discharge) a capacitive load, reducing the power consumed. (For a more thorough discussion of technology scaling, see e.g. [5].)

VLSI design methodologies. The high cost and long design time of full custom circuits have prompted the creation of automated design approaches. These approaches rely on a variety of different methodologies in which circuits are automatically mapped into silicon such as automated placement and routing of standardized cells [26]. Significant geometrical constraints are imposed on the layout to make the circuit more amenable to automated place and route techniques. Circuit structures amenable to such approaches are illustrated in Figure 3.10. Automated design methods yield suboptimal designs as compared to full custom methodologies. The greater number of constraints on the design methodology makes the resulting circuit less optimal, albeit with a faster time-to-market.

3.3. Structural Level

Once a system is specified at the behavioral level, the next step in the design process is to determine which computational algorithms should be employed and the type and number of system building blocks, interfaces and connections. While the process is application specific, two types of basic trade-offs are available: parallel processing and pipelining. A simple data path, shown

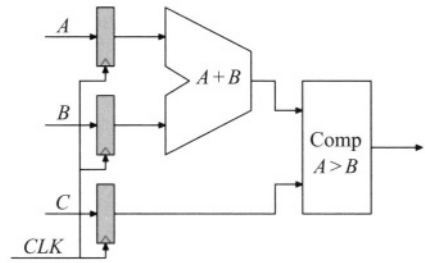


Figure 3.11. A simple data path [27].

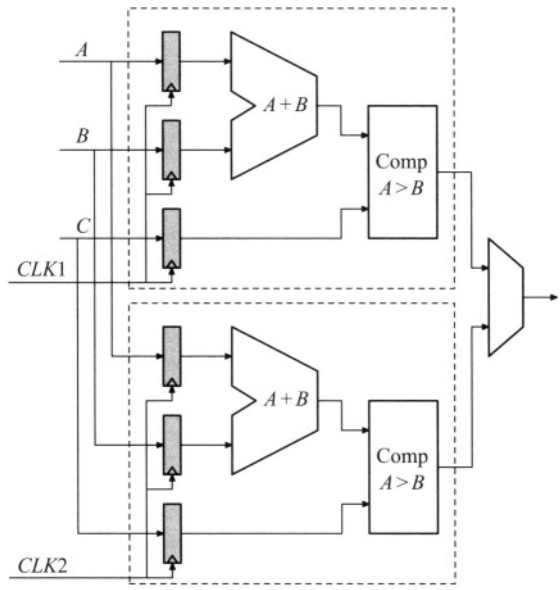


Figure 3.12. Parallel implementation of the data path [27].

in Figure 3.11, is used here to demonstrate these concepts. The speed, area and dynamic power of this circuit are compared and contrasted to a parallel implementation in Section 3.3.1 and to a pipelined implementation in Section 3.3.2.

3.3.1. Parallel Architecture

Parallel processing consists of duplicating a portion of a data path a number of times, and connecting the duplicate circuits in parallel with each other. This approach is illustrated by the circuit shown in Figure 3.12, where the parallel implementation of the data path shown in Figure 3.11 is depicted. Additional

circuitry is needed to maintain the correct data flow, such as the multiplexer and related control circuitry. Extra circuitry is also used to generate the different clocking signals for the two parallel blocks (not shown). Other conditions being equal, the computational throughput of the parallel implementation of the circuit is doubled as compared to the original serial implementation (assuming the multiplexer delay to be negligible). The circuit area is more than doubled due to the added circuitry and interconnect. As described by Chandrakasan et al. [27], the area of the parallel implementation shown in Figure 3.12 is 3.4 times larger than that of the reference circuit (a circuit implementation based on a $2\,\mu m$ technology is assumed in [27]). The circuit capacitance is increased 2.15 times, leading to a proportional increase in power dissipation. For parallel processing to be effective, the algorithms should be suitable for parallelization such that high utilization of the added processing units is achieved and the overhead of the complex control circuitry is minimized.

3.3.2. Pipelining

The process of pipelining inserts new registers into a data path, breaking the path into shorter paths. This process shortens the minimum clock period from the delay of the original path to the delay of the longest of the new shorter paths [28]. Therefore, the resulting circuit can be clocked faster to achieve a higher synchronous performance. A pipelined version of the data path shown in Figure 3.11 is illustrated in Figure 3.13. If the delays of the adder and comparator are equal, the path can be clocked at almost double the original frequency, with the delay of the inserted registers preventing the system from operating at precisely double the original performance. The area penalty of pipelining is less than that of the parallel architecture approach since the processing elements are not duplicated and only the inserted registers are introduced. The area of the pipelined circuit shown in Figure 3.13 is 1.3 times larger than the area of the reference circuit shown in Figure 3.11 [27]. The capacitance (and therefore the dynamic power) is 1.15 times greater than that

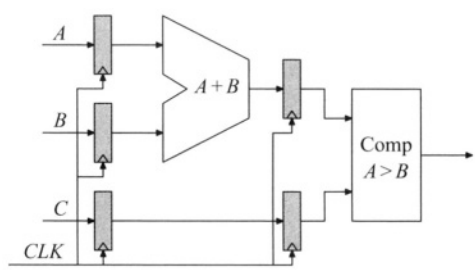


Figure 3.13. Pipelined implementation of the data path [27].

used in the serial approach. As in the parallel processing approach, pipelining is most effective in those circuits with a feed-forward nonrecursive data flow path. Pipelining also increases the latency of the system because of the added set-up and clock-to-output delays of the extra registers and any imbalance in the delays of the pipeline stages which may be detrimental to the overall system performance. As more registers are inserted into a data path, the delay of these registers becomes a larger fraction of the total path delay. Introducing more registers, therefore, has a diminishing return on performance. For a more detailed treatment of these issues, see [29,30].

The performance benefits of the parallel and pipelined approaches can improve the power characteristics, trading off area and power for speed. Instead of maintaining a fixed voltage and gaining computational throughput, another possible trade-off is to decrease the supply voltage to a level sufficient to maintain the original throughput. For the circuit shown in Figure 3.12, this strategy means decreasing the power supply until the delay doubles. The same voltage maintains the performance of the pipelined version at the original level assuming the added register delays are negligible and the delay of the new data paths are well balanced. Assuming an initial voltage of 5 V, the scaled voltage level to maintain the same effective performance is 2.9V [27]. The power of the parallel implementation $P_{\|}$ normalized to the power of the reference path P_{ref} is:

$$P_{\|} = C_{\|} V_{\|}^2 f_{\|} = (2.15C_{\text{ref}})\,(0.58V_{\text{ref}})^2 \left(\frac{f_{\text{ref}}}{2}\right) \approx 0.36P_{\text{ref}}$$

Similarly, the normalized power of the pipelined implementation P_{pipe} is:

$$P_{\text{pipe}} = C_{\text{pipe}} V_{\text{pipe}}^2 f_{\text{pipe}} = (1.15C_{\text{ref}})\,(0.58V_{\text{ref}})^2\, f_{\text{ref}} \approx 0.39P_{\text{ref}}$$

These substantial reductions in power consumption are the result of the quadratic dependence of dynamic power on the supply voltage.

Pipelining and parallelism can also be combined to further improve performance and power. To maintain a critical delay of the original data path, the supply voltage can be lowered to 2 V, reducing the power by a factor of five,

$$P_{\|\text{pipe}} = C_{\|\text{pipe}} V_{\|\text{pipe}}^2 f_{\|\text{pipe}} = 2.5C_{\text{ref}} \cdot (0.4V_{\text{ref}})^2 \cdot \left(\frac{f_{\text{ref}}}{2}\right) \approx 0.2P_{\text{ref}}$$

The data and the implicit trade-offs are summarized in Table 3.1.

3.4. Circuit Level

Most CMOS-specific trade-offs are made at the circuit abstraction level. Trade-offs involved in selecting dynamic or static implementations are discussed in Section 3.4.1. Transistor sizing, a central issue in CMOS circuit

Table 3.1. Summary of trade-off data (from [27]).

Data path implementation	*Voltage (V)*	*Area*	*Power*
Original data path	5.0	1	1
Parallel data path	2.9	3.4	0.36
Pipelined data path	2.9	1.3	0.39
Parallel and pipelined	2.0	3.7	0.2

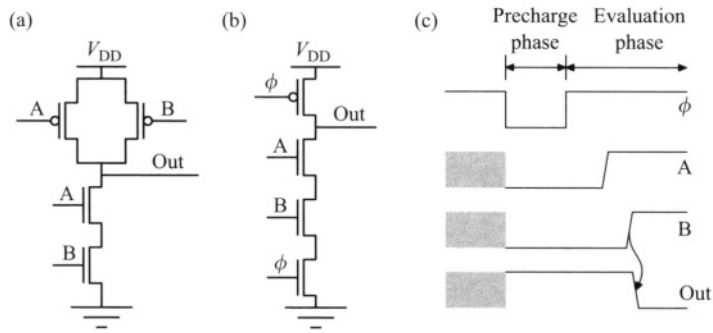


Figure 3.14. CMOS implementations of a two-input NAND gate. (a) Static implementation of the NAND gate, (b) dynamic implementation of the NAND gate, (c) timing diagram of the dynamic implementation.

design, is considered in Section 3.4.2. Trade-offs in tapered buffers are reviewed in Section 3.4.3.

3.4.1. Static versus Dynamic

The use of dynamic or static CMOS structures to implement a circuit function is an important decision that is made at the circuit level. The concepts of static and dynamic styles are illustrated in Figure 3.14. Both choices have virtues. Static CMOS is relatively simple to design, and is both robust and noise tolerant. Alternatively, dynamic CMOS uses fewer transistors to implement a given logic function, requires less area, has smaller parasitic capacitances, and is able to operate at higher speeds. Dynamic circuits also do not dissipate power due to spurious transitions (or glitches). However, dynamic circuits have higher switching activities. All of the nodes are charged during a precharge phase; many of these nodes are charged and immediately discharged during the evaluation phase. In contrast, in static circuits, except for spurious transitions, the output nodes are charged or discharged only when the logic values change. Static circuits can also be easily powered down by gating the clock signal; dynamic circuits, alternatively, require a small amount of additional circuitry

to preserve a state in the absence of the clock signal, increasing the parasitic capacitance and decreasing the circuit speed. The choice of circuit type is, however, not mutually exclusive. Static and dynamic circuits can both be used within the same IC. More complex design and verification of dynamic circuits is required in order to avoid potential hazards. It is, therefore, common to implement performance critical parts of a circuit design in dynamic CMOS in order to meet stringent performance goals and to implement the remaining circuitry in static CMOS in order to save design time while improving overall circuit robustness.

3.4.2. Transistor Sizing

Transistor sizing is another fundamental trade-off at the circuit level in CMOS logic families [31–45]. As transistors become wider, the current drive increases (the output resistance decreases) linearly with the transistor width, decreasing the propagation delay. The physical area and gate capacitance also increase linearly with width, increasing the circuit area and power. Thus, the optimal transistor size is strongly dependent on the trade-off of area and power for speed. Furthermore, the same type of optimization process may produce different approaches satisfying different design goals. Consider, for example, a static CMOS inverter in which the NMOS to PMOS transistor width ratio is chosen to minimize the propagation delay. The ratio

$$\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p} \tag{3.3}$$

balances the output rise and fall transition times. An alternative option is the ratio

$$\frac{W_p}{W_n} = \sqrt{\frac{\mu_n}{\mu_p}} \tag{3.4}$$

which minimizes the average of the rise and fall delays [48]. Note, however, that either of these choices can produce the worst case signal delay depending upon the input rise and fall transition times. Transistor sizing depends, therefore, on both the optimization criteria and the circuit context. The primary transistor sizing trade-offs are considered below.

A common objective of transistor sizing is delay minimization. Consider a CMOS circuit with the output loads dominated by the input capacitances of the following stages. The typical dependence of the capacitor charging delay on the transistor width is shown in Figure 3.15. The charge time monotonically decreases with increasing transistor width. However, a caveat is that the input load of the transistor increases linearly with the transistor width, delaying the preceding gate. The net result is that the total delay of a data path with more stages can be smaller; an example circuit is illustrated in Figure 3.16. Similarly,

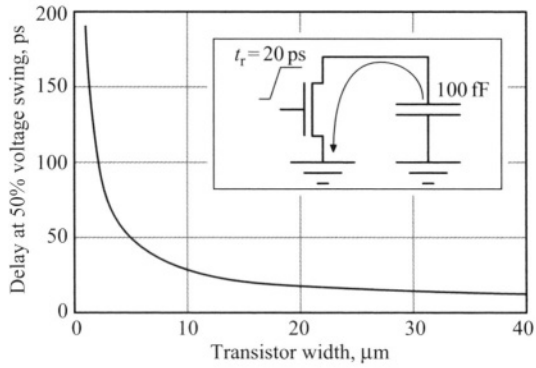


Figure 3.15. SPICE simulation of a capacitor discharge time as a function of the transistor width. TSMC 0.25 μm CMOS technology (MOSIS), 100 fF external load and $V_{DD} = 2.5$ V.

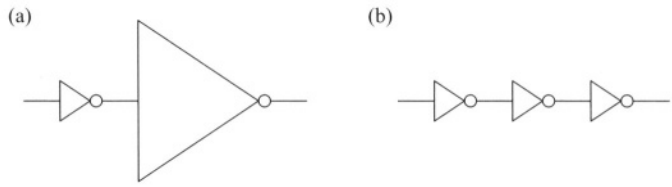


Figure 3.16. The effect of the gate input load on the propagation delay of a data path. Due to the large input capacitance it is possible for the path shown in (a) to have a longer delay than the path shown in (b) although there are less gates in the path shown in (a).

a uniform increase of all of the transistor sizes does not substantially change the propagation delay of a circuit in which the output loads are dominated by the input capacitances of the fanout while a linear increase in power and area will occur. The current drive of the gates I_{out} will increase which is offset by an increase in the output capacitive loads C_L. The I_{out}/C_L ratio remains essentially constant. A careful balance of the current drive and input load is therefore necessary to enhance circuit performance.

Two iterative algorithms, one algorithm for minimum delay and the other for minimum active area under a delay constraint, are described by Lee and Soukup in [31] for combinational circuits driving large capacitive loads. An important conclusion of these algorithms is the rapid rise of silicon area as the minimum area is approached. For example, the area of a tristate output buffer designed in a 2.5 μm CMOS technology to drive a 25 pF load more than triples when the delay is reduced from 28 ns to the minimum of 22 ns. This behavior is further aggravated in deep submicrometer (DSM) technologies as the interconnect impedances increase the area penalty while degrading any

device delay advantages. Design for minimum delay is therefore seldom a practical solution.

The area and speed trade-offs achieved by transistor sizing are also dependent on the design style. Full-custom design is the most flexible; semi-custom design strategies impose certain geometrical constraints such as a fixed cell height in standard cell methodologies (see Figure 3.10). The size of the transistors within the cells can be either fixed (a typical cell library contains several cells implementing the same function with different output current capabilities) or adjusted at the time of cell invocation to satisfy a target current drive; gate array circuits are the most restrictive, with transistor sizes being multiples of the width of the prefabricated transistors, producing inefficient area utilization. A comparison of area-delay trade-offs in these design styles is presented in [32]. A full custom style offers the most efficient and flexible area-delay trade-off. Area-delay trade-offs among different implementations of a combinational path driving a large capacitive load are compared in [32]. One implementation uses a unit-sized cell with a tapered output driver between the last logic stage and the capacitive load. The second implementation uses tapered logic gates [32], where the final stage is sufficient to effectively drive the capacitive load. A circuit consisting of a chain of three inverters and a capacitive load one hundred times larger than the input load of a unit size inverter is considered for comparison. The first approach yields a circuit area and delay of 29 minimum inverter delays and 22 minimum inverter areas, while the second approach produces a delay and area of 16.8 minimum inverter delays and 32 minimum inverter areas, respectively.

The transistor size also affects the circuit power dissipation characteristics. A simple approximation is to consider the circuit power as linearly proportional to the total active area of a circuit A, that is, $P = CV^2 f$, where $C = C_{ox}A$, and the gate oxide capacitance per unit area C_{ox} is constant for a given technology. Under this assumption (i.e. no interconnect capacitance), power optimization and circuit area optimization are the same since the circuit area is assumed to be proportional to the active area. Therefore, a power optimal design should use only minimum size transistors as long as correct circuit operation is not affected.

Yuan and Svensson [33] discuss transistor sizing with respect to power-delay optimization. For a one-stage pass transistor circuit or inverter with a symmetric voltage transfer characteristic (VTC), the power-delay reaches a minimum when the gate output parasitic capacitance equals the load capacitance. Power optimal loading ratios are also calculated for more complex structures. Transistor size optimization for an energy-delay performance metric is considered in [34]. However, [33,34] neglect the short-circuit current contribution to the power dissipation, a significant power component in circuits with large fanout and, therefore, long transition times. An analytical power dissipation model

characterizing short-circuit power is described in [35], In this case, the power optimal size of the transistors is dependent on the input slew rate, which in turn is a function of the input driver size and output load. The power optimal size for inputs with high slew rates are smaller than for inputs with low slew rates, as the short-circuit power is inversely proportional to the slew rate s [20]. If driving large capacitive loads, the power savings is substantial for optimally sized gates as compared to minimally sized gates. For an inverter driving ten minimal inverters, the power savings is 35%. If the load is 20 inverters, the power savings is 58%. However, the fraction of such high fanout gates in practical circuits is typically small.

The power optimal transistor size is smaller than the power-delay optimal transistor size. An efficient trade-off of power for delay occurs at intermediate sizes. Trade-offs beyond the power-delay optimum can be pursued in aggressive circuit designs. Two algorithms based on a power model are also developed in [35]. The first algorithm searches for the power optimal transistor size. Benchmark circuits optimized with this algorithm have average power savings of approximately 5%, average area increases of approximately 5%, and, typically, a lower delay as compared to those circuits with minimum active area. The second algorithm performs power optimization under a delay constraint. In benchmark circuits, this algorithm achieves a power savings of about 1–5% over a similar algorithm with minimum active area as the only design criterion.

The power supply has been assumed fixed in the discussion of transistor sizing. Releasing this restriction provides an added degree of freedom for power-area trade-offs. As described in [36], power savings through transistor sizing in order to lower the supply voltage is not effective for long channel devices; only a marginal savings can be achieved under a limited set of load conditions. However, for short channel devices, when the device current is linearly proportional to $V_{GS} - V_T$, a wide opportunity for such optimization exists. Beyond this power optimal size, any power saving through lower voltages is lost due to the larger amount of capacitance being switched. The increase in interconnect capacitance due to an increase in circuit area is neglected in the analytical model presented in [36].

A prescaler, consisting of four identical toggle flip flops, is investigated through SPICE simulations. An optimal size of four times the minimum width for uniformly scaled transistors is determined. At 300 MHz, the optimally scaled circuit consumes 50% less power (in a $1\ \mu m$ CMOS technology). Two versions of the prescaler have also been manufactured in a $1\ \mu m$ CMOS technology, one version based on minimum sized transistors and another version based on large, individually optimized transistors. To operate at 300 MHz, the first circuit requires a 5 V supply and consumes 1.740 mW, whereas the optimized circuit requires only a 1.5 V power supply and dissipates only 0.575 mW.

A variety of tools for automated transistor sizing has also been reported [37–39]. In [38], an average 50% reduction in power is reported for optimized circuits as compared to standard cell implementations operating at the same clock frequency. Alternatively, an average 25% gain in clock frequency is achieved dissipating the same amount of power. Techniques can also be applied to perform transistor size optimization under noise margin and charge sharing constraints [37]. Research on transistor size and input reordering optimization with respect to hot carrier reliability has been described in [43]. It is shown that optimization for hot carrier reliability and for power dissipation are quite different.

3.4.3. Tapered Buffers

An important special case of transistor sizing is tapered buffers. Consider the problem of driving a large capacitive load. Driving board traces and on-chip buses, where capacitances are typically two to four orders of magnitude larger than on-chip logic levels, is an example of such a task. To drive such large capacitive loads at an acceptable speed, an intermediate buffer is often used. Using an inverter appropriately scaled for the capacitive load (as shown in Figure 3.17(a)) reduces the delay; however, the large input capacitance of the inverter loads the previous logic with too large a capacitive load. A similar argument can be made when inserting another inverter, large enough to drive the inverter driving the load, and so on until the initial input inverter of the buffer is sufficiently small to be driven by the previous logic gate at an acceptable speed. Thus, a tapered buffer consists of a chain of inverters of gradually increasing size as illustrated in Figure 3.17(b). The ratio of an inverter size to the size of the preceding inverter is called the tapering factor β.

The idea of tapering was first introduced by Lin and Linholm [46]; these authors investigated trade-offs based on a weighted product of a *per-stage* delay and used the total buffer area as a figure of merit. Following Lin and Linholm, Jaeger [47] considered minimization of the *total* buffer delay as the primary optimization objective. Jaeger showed that, under the assumption that a stage

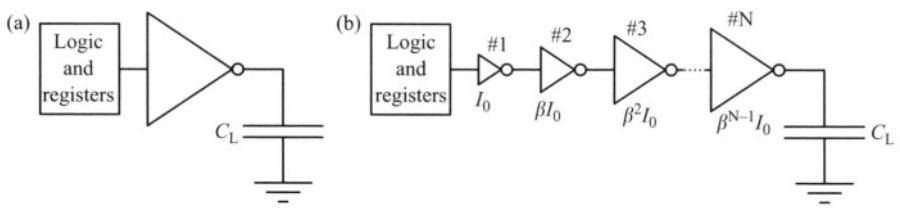


Figure 3.17. Circuit approaches to driving a large capacitive load. (a) A large inverter, (b) a tapered buffer. The delay of the tapered buffer is less than the delay of a single large inverter.

load is proportional to the next stage size (i.e. neglecting the intrinsic load of the gate), the delay of a tapered buffer reaches a minimum at a constant tapering factor $\beta_{opt} = e$ (the base of the natural logarithm) with a corresponding number of stages $N_{opt} = \ln M$, where $M = C_L/C_0$ is the ratio of the load capacitance C_L to the input capacitance C_0 of the initial inverter in the chain (usually considered to be minimum size). Note that because the number of buffer stages N is an integer, the aforementioned condition cannot in general be satisfied precisely. Therefore, one of the two integers closest to $\ln M$ is chosen, and β is calculated to satisfy $\beta^N = M$.

The approach of Lin and Linholm followed by Jaeger has been improved in several directions. More accurate delay models [48]–[50,54] and capacitance models [48,50,51,53] have been employed to allow for the intrinsic load capacitance, a ramp input signal, and short-circuit current. Initially, the effect of the intrinsic load capacitance was investigated by Kanuma [48] and Nemes [49]. These authors determined that the delay optimal tapering factor increases with the ratio of the intrinsic output capacitance (diffusion and gate overlap) to the input gate capacitance. Further improvements to account for the effects of the finite input slew rate and resulting short-circuit current were developed in [50,51,53]. In [51], the intrinsic output capacitance is increased by an analytically calculated value to account for the slower charging of the nodal capacitance. In [53], empirical data from circuit simulations are used to calculate the increased equivalent capacitance. A model considering both a finite slew rate and intrinsic loading is described in [50], Further discussion of this topic can be found in [55,56]. To summarize these results, the delay optimal tapering factor varies from three to five, depending upon the target technology (i.e. the ratio of the input capacitance to the intrinsic output capacitance). The delay optimal transistor ratio of the inverter stages is $\sqrt{\mu_n/\mu_p}$, which minimizes the average output delay [50], although less than a 10% gain in delay is achieved as compared to equally sized transistors. A possible exception from this rule is the final stage where equal rise and fall times are often preferred over average delay minimization.

Area-power-delay trade-offs have also been considered [20,50,52,57,58]. It has been observed that for a given load the buffer delay versus tapering factor dependence is relatively flat around β_{opt}, as illustrated in Figure 3.18. Also, the total area of the buffer is a relatively strong function of β, falling with β. Thus, an effective trade-off of delay for area and power is possible. For example, if a buffer with an optimum number of stages is implemented with both four stages and three stages, the buffer delay rises by 3% and 22% but the area shrinks by 35% and 54%, respectively. Similar results are obtained by Vemuru in the investigation of tapered buffers with a geometrically increasing tapering factor [52]. While producing higher minimum delays (less than 15% greater than the smallest delays in a fixed-taper (FT) buffer), such buffers have

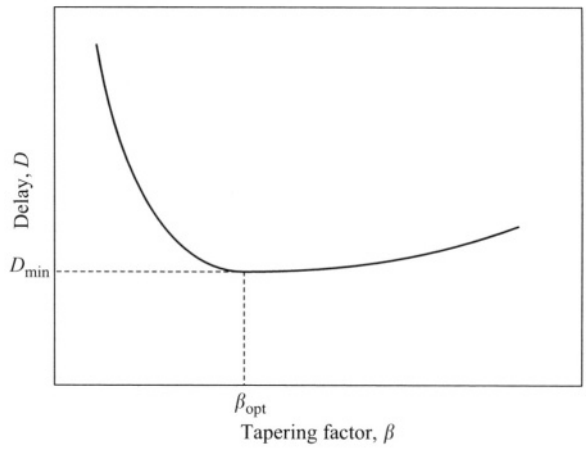


Figure 3.18. Dependence of the tapered buffer propagation delay on the tapering factor.

lower area and power at comparable suboptimal delays. The minimum delay of variable-taper buffers can be reduced and brought to within a few percent of the delay of a FT buffer by implementing the first few stages with a FT factor. Therefore, the optimal area-delay trade-offs are achieved in a FT buffer with the final one to two stages utilizing a larger tapering factor. This strategy is consistent with the observation in [50] that the buffer delay is reduced when the tapering factor of the final stage is increased. Power-delay product optimization of the tapered buffers is considered in [57]. Power-delay optimized buffers require fewer stages (and, consequently, a higher β) where the power-delay product improves by 15–35% as compared to delay optimal buffers.

Cherkauer and Friedman integrated these disparate approaches to CMOS tapered buffers into a unified design methodology, considering speed, area, power and reliability together [58]. Enhanced short channel expressions are presented for tapered buffer delay and power dissipation based on the alpha-power law short channel transistor model [25]. Analytic expressions of similar form are produced for the four performance metrics, permitting the combination of these metrics into different weighted optimization criteria. An important result is that short channel effects do not change the form of the propagation delay through a tapered buffer chain. The *I–V* model affects the absolute value of the delay, but does not change the process of delay optimization. Consequently, delay optimization schemes developed under long channel assumptions are also applicable to short channel devices.

A design methodology is presented in [59] for the optimal tapering of cascaded buffers in the presence of interconnect capacitance. Though interconnect capacitance is typically small in a full custom circuit, in those circuits based on

channel routing, physical proximity of the stages is not necessary and the capacitive interconnect load can often be substantial. Also, as shown in the paper, neglecting interconnect capacitance may result in suboptimal circuits even in those cases where the interconnect capacitance is small. A method, called constant capacitance-to-current ratio tapering (C^3RT), is based on maintaining the capacitive load to current drive ratio constant, such that the delay of each buffer stage also remains constant. Hence, in the presence of high interconnect loads, it is possible for the C^3RT methodology to produce a buffer in which a particular stage is smaller than the preceding stage, that is, with a tapering factor of less than unity between the stages. The importance of interconnect capacitance can vary from small to significant, depending upon the ratio of the interconnect capacitance to the total load capacitance at a node. The larger the interconnect load and the closer the load to the input of the buffer, the greater the impact on the circuit, as the input and output capacitances of the stages close to the load are larger and, therefore, the interconnect load is typically a proportionally smaller fraction of the total load. To demonstrate this methodology, a case study is conducted on a five-stage buffer driving a 5 pF load at 5 MHz. Implementation in a $2\,\mu m$ technology is assumed; the interconnect capacitance is varied from 10fF (the best case scenario in practice where the stages are physically abutted) to 500 fF (a severe case, possibly a gate array or standard cell circuit). C^3RT optimized buffers exhibit delay, area, and power advantages over FT buffers, as listed in Table 3.2. Note the steady *absolute* decrease in power of the C^3RT buffer as the interconnect capacitance increases. Although it may appear counterintuitive, this absolute decrease is accounted for by the reduction in the active area capacitance which offsets the increase in the interconnect capacitance such that the *total* capacitance is decreased. In general, the omission of interconnect capacitance leads to suboptimal designs in DSM CMOS circuits.

Table 3.2. C^3RT buffers as compared to FT buffers in the presence of interconnect capacitance [59].

C_{int} (fF)	*Propagation delay*			*Power dissipation*			*Active area*		
	FT (ns)	C^3RT (ns)	*Improvement* (%)	*FT* (mW)	C^3RT (mW)	*Improvement* (%)	*FT* (μm^2)	C^3RT (μm^2)	*Improvement* (%)
10	2.29	2.28	0.6	1.42	1.38	2.8	1900	1795	5.5
100	2.56	2.54	0.9	1.44	1.32	8.3	1900	1591	16.3
250	2.87	2.85	0.7	1.48	1.25	15.6	1900	1313	30.9
500	3.38	3.32	2.0	1.56	1.21	22.4	1900	1024	46.1

3.5. Physical Level

Coping with interconnect is a major problem in VLSI circuits. Interconnect affects system performance, power consumption and circuit area. The increasing importance of interconnect [5,67,68] is due to the classical scaling trend that while device feature size is *decreasing,* interconnect feature sizes are shrinking, and the die size is *increasing,* doubling every eight to ten years [3]. Thus, the wiring tends to become longer and the interconnect cross-section area smaller.

A problem resulting from this trend is increased *RC* interconnect impedances, degrading the delay of the gates. Consider a CMOS inverter driving an *RC* interconnect line as illustrated in Figure 3.19 (the driver output capacitance is omitted for the sake of simplicity). A first-order model of the delay of the circuit is [5]

$$T_{50\%} = 0.4R_{\text{int}}C_{\text{int}} + 0.7(R_{\text{tr}}C_{\text{int}} + R_{\text{tr}}C_{\text{L}} + R_{\text{int}}C_{\text{L}}) \tag{3.5}$$

If the driver load is effectively capacitive, that is, the interconnect resistance R_{int} is much less than the effective driver resistance R_{tr}, the interconnect capacitance can be combined with the input capacitance of the gate to form a lumped load capacitance, permitting the circuit delay to be characterized by a lumped *RC* circuit delay, $0.7R_{\text{tr}}(C_{\text{int}} + C_{\text{L}})$. The signal propagation delay is due to the capacitive load being charged by the driver. Increasing the driver transistor width and consequently reducing R_{tr} decrease the circuit delay, trading off circuit power and area for higher speed. However, this behavior changes when R_{int} becomes comparable to R_{tr}. The delay cannot be reduced below $R_{\text{int}}(0.4C_{\text{int}} + 0.7C_{\text{L}})$. Note that the purely interconnect-related delay component, $0.7R_{\text{int}}C_{\text{int}}$, increases quadratically with interconnect length as both R_{int} and C_{int} are proportional to the length of the interconnect. This component of the total delay quickly becomes dominant in long interconnect. This interconnect delay component cannot be reduced significantly by making the interconnect wider as a decrease in wire resistance is offset by an increase in the

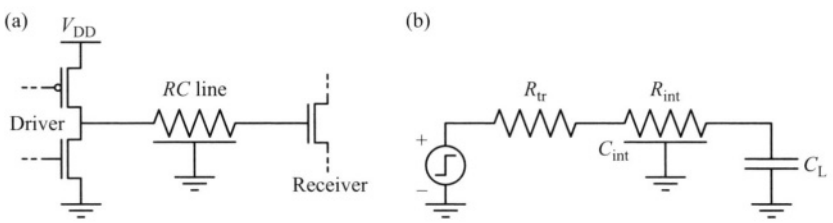


Figure 3.19. A model of a CMOS circuit driving an *RC* interconnect. (a) A circuit driving an *RC* line, (b) a corresponding simple model [5].

Table 3.3. Typical interconnect physical characteristics of a 0.18 μm CMOS process.

Layer characteristic	*Impedance*
Sheet resistance	$0.08\frac{\Omega}{\square}$
Metal pitch	0.5 μm
Metal thickness	0.5 μm
Interlayer spacing	0.5 μm
Metal width	0.25 μm
Line spacing	0.25 μm
Minimum width wire capacitance	0.2 fF/μm

wire capacitance. The increasing importance of interconnect delay is demonstrated by a 0.18 μm CMOS technology with aluminum interconnect. The physical characteristics of the first level metal interconnect typical for this technology are listed in Table 3.3. As an example, consider a local interconnect spanning several gates which is minimum width and 100 wire widths long, that is, 25 μm. The total resistance and capacitance are

$$R_{\text{int}} = 100\square \cdot 0.08\frac{\Omega}{\square} = 8\,\Omega \quad \text{and} \quad C_{\text{int}} = 0.2\frac{\text{fF}}{\mu\text{m}} \cdot 25\,\mu\text{m} = 5\,\text{fF}$$

respectively, yielding an interconnect delay of $t_{\text{int}} = 0.4 \cdot 8\,\Omega \bullet 5\text{fF} = 16\text{fs}$. Thus, interconnect delay is not important for local interconnect. As the dimensions scale with feature size, the local interconnect delay is expected to remain relatively insignificant with technology scaling [3]. The interconnect becomes significant, however, at the level of intermediate interconnect, where the length is approximately a half perimeter of a functional block, typically 3–4 mm. At such a length,

$$R_{\text{int}} = \frac{4\,\text{mm}}{0.25\,\mu\text{m}} \cdot 0.08\frac{\Omega}{\square} = 1280\,\Omega \quad \text{and} \quad C_{\text{int}} = 0.2\frac{\text{fF}}{\mu\text{m}} \cdot 4000\,\mu\text{m} = 0.8\,\text{pF}$$

and the interconnect delay is $t_{\text{int}} = 0.4 \cdot 1280\,\Omega \cdot 0.8\,\text{pF} = 0.4\,\text{ns}$. This delay exceeds typical gate delays in a 0.18 μm CMOS technology and is a significant fraction of the minimum clock period of a high-performance circuit (1–3 ns). Global interconnections can be as long as half a perimeter of the die (and longer for bus structures). Assuming a die with $1 \times 1\,\text{cm}^2$ dimensions, a moderate size for current fabrication capabilities, a half perimeter line would have the following parameters,

$$R_{\text{int}} = \frac{20\,\text{mm}}{0.25\,\mu\text{m}} \cdot 0.08\frac{\Omega}{\square} = 6400\,\Omega \quad \text{and} \quad C_{\text{int}} = 0.2\frac{\text{fF}}{\mu\text{m}} \cdot 20,000\,\mu\text{m} = 4\,\text{pF}$$

and the interconnect delay would equal $t_{int} = 0.4 \cdot 6400\,\Omega \bullet 4\,\text{pF} \simeq 10\,\text{ns}$. A 10 ns path delay (equal to a 100 MHz clock frequency) exceeds the clock period of many circuits, dwarfing the delay of the logic elements. The delay of global interconnect is, therefore, a central topic of concern in high-performance VLSI circuits.

Widening a uniform line has a marginal impact on the overall wire delay. These delay estimations are based on the thin first layer metal. The thickness of the upper metal layers is typically increased to provide less resistive interconnections. The pitch and interlayer spacing of the top layers are also wider, therefore, the line capacitance does not significantly change as compared to the first metal layer. The impedance characteristics of the metal lines in the upper layers are about an order of magnitude lower than the impedance characteristics of the lower metal levels. While mitigating the problem, the thick upper metal layers do not solve the overall problem as global line impedances severely limit circuit performance.

An effective strategy for reducing long interconnect delay is inserting intermediate buffers, typically called repeaters [5]. Repeaters circumvent the quadratic increase in interconnect delay by partitioning the interconnect line into smaller and approximately equal sections, as shown in Figure 3.20. The sum of the section delays is smaller than the delay of the original path since the delay of each section is quadratically reduced. The decreased interconnect delay is partially offset by the added delays of the inserted repeaters.

A number of repeater insertion methods has been proposed [69–74]. Bakoglu presents a method based on characterizing the repeaters by the input capacitance and the effective output resistance deduced from the repeater size [5,67]. The minimum delay of the resulting *RC* circuit is achieved when the repeater section delay equals the wire segment delay. Another method has been described by Wu and Shiau [69]; in this method a linearized form of the Shichman–Hodges

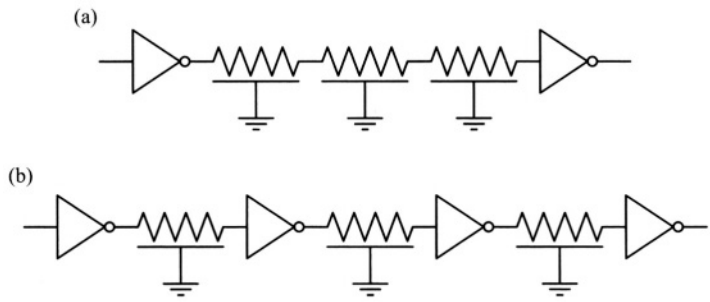


Figure 3.20. Repeater insertion. (a) The original interconnect line, (b) the interconnect line with inserted repeaters.

equations is used to determine the points of repeater insertion. Nekili and Savaria have introduced the concept of parallel regeneration in which precharge circuitry is added to the repeaters to decrease the evaluation time [70,71]. This technique reduces the number of repeaters, but requires extra area and a precharge signal to maintain correct operation. A mathematical treatment of repeater optimization with and without area constraints is described by Dhar and Franklin [72]. Elegant solutions are obtained; however, a simple resistor-capacitor model is used to characterize the repeaters and no closed form solutions are described.

A repeater design methodology is presented by Adler and Friedman [74]. A timing model of a CMOS inverter driving an *RC* load based on the alpha-power law transistor model is used to account for short channel velocity saturation effects. The closed form expression for the overall signal delay of a uniform repeater chain driving a large distributed *RC* load is described. The analytical delay estimates are within 16% of SPICE simulations of representative long interconnect loads. A comparison of uniform and tapered-buffer repeaters is also described. Uniform repeater are found to outperform tapered-buffer repeaters when driving even relatively low resistive *RC* loads. Power issues in the repeater design process are also considered. An analytic expression for the short-circuit power in a repeater chain is described which exhibits a maximum error of 15% as compared to SPICE simulations within the primary regions of interest. It is shown that short-circuit power can represent up to 20% of the total dynamic power dissipation. It also shown that a 4% increase in delay over the minimum delay of a repeater chain can be traded off for a 40% savings in area and 15% savings in power.

3.6. Process Level

Changing technology is typically not a design or trade-off option, however, it is sometimes feasible to choose different semiconductor manufacturers or specialized technologies. Two technologies, both described as "0.25 μm CMOS technologies," can be substantially different. The notion of "0.25 μm" refers to the smallest resolvable feature size in a process, typically the transistor channel length *L*. While *L* is the primary parameter controlling the transistor current drive, the channel length is just one of the many dozens of design rules that characterize a process. As the interconnect system (with related contacts and vias) occupy an increasing portion of the total die area, these design rules are of great significance in the overall circuit performance and area characteristics. The effects of technology scaling are discussed in Section 3.6.1. The trade-offs involved in the choice of threshold voltage and power supply voltage are discussed in Sections 3.6.2 and 3.6.3, respectively. The impact of improved materials on design trade-offs is considered in Section 3.6.4.

3.6.1. Scaling

Shrinking dimensions (i.e. length, height and width) directly improve circuit area and power. The circuit area decreases rapidly (quadratically, assuming linear scaling). The parasitic capacitance of the transistors and interconnect is reduced; therefore, the power consumed by the circuit is also reduced. These gains in area and power can be traded for increased speed. The effects of changes in the vertical dimensions differ depending upon the circuit component. Thinner gate oxides translate to increased transistor transconductance and therefore higher speed, which can be effectively traded for lower power by lowering the power supply voltage. Thicker intermetal oxide reduces the parasitic wiring capacitance, leading to shorter *RC* delays (i.e. higher speed) and lower cross-coupling noise. Increased metal thickness lowers the sheet resistance of the metal layers. The wiring is denser and the total die area is reduced; however, there is also an increase in interwire capacitive coupling and noise.

3.6.2. Threshold Voltage

The control of the threshold voltage V_T is one of the primary issues at the process level. A higher V_T means higher noise margins and lower leakage currents when the transistors are cut off. However, the leakage current contribution to the total power dissipated in most low power systems is typically small and the coupling noise can be proportionally lowered as the supply voltage is decreased. The relative magnitude of the capacitive cross-coupling noise to the signal level is determined by the circuit geometries. The magnitude of the switched current is decreased as V_{DD} is lowered; therefore, the *IR,* inductive and simultaneous switching components of noise also scale. A lower V_T, however, enhances the transistor current drive, permitting the circuit to operate faster or, alternatively, providing a substantial power saving by lowering the supply voltage without a significant increase in the logic delay. Threshold voltage process variations set a limit on the maximum V_T reduction. If a statistical deviation of V_T in just one transistor is above some critical value, an entire multimillion transistor IC can be lost. As more and more transistors are integrated onto one die, tens of millions transistor ICs have become commonplace, making tight control of the threshold voltage ever more challenging.

3.6.3. Power Supply

Power supply voltage V_{DD}, strictly speaking, is not a process parameter; however, the power supply voltage is effectively defined by the process technology. The delay rises dramatically as V_T approaches V_{DD}, see Figure 3.21. Increasing V_{DD} above several V_T is often not practical due to a small increase in speed at the expense of a quadratic increase in the power consumption [61–63]. Due to carrier velocity saturation effects, the transistor current increases

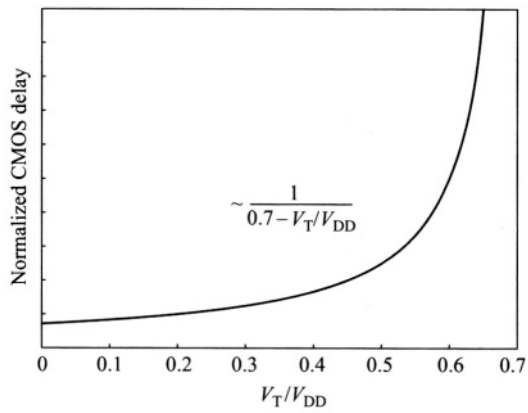


Figure 3.21. Dependence of transistor switching delay on threshold voltage V_T [75].

almost linearly with voltage and no significant speed benefits are attained with further voltage increases. Furthermore, reliability issues such as gate oxide breakdown, hot electron injection, carrier multiplication and electromigration place an upper limit on the magnitude of the power supply and current density.

3.6.4. Improved Interconnect and Dielectric Materials

The introduction of copper as a low resistance interconnect material and low dielectric constant materials as interlayer isolators is a relatively recent phenomenon. The immediate effect on existing circuits is higher operating speeds due to reduced interconnect impedances. Though copper-based CMOS processes cost more than conventional aluminum-based CMOS processes at the present time, once matured, the cost should drop below the cost of aluminum interconnect. By some estimates, a layer of copper interconnect costs 20% less than a comparable layer of aluminum [76]. Much greater speed improvements are expected for those ICs originally designed for copper interconnect processes. The higher wiring capacity of a copper metal layer as compared to an aluminum layer will also result in a substantial decrease in die area and/or the use of less interconnect layers, further decreasing overall fabrication costs.

3.7. Future Trends

Semiconductor fabrication technology has reached the point where integrating an entire large system on a single chip is possible. The increased level of integration will, however, exacerbate design productivity issues, greatly affecting design time and cost. Designing an SoC at the transistor level is considered impractical from both a cost and a design time point of view. A large fraction

of an SoC consists of functional cores either reused from previous circuits or automatically synthesized from a high level description (such as RTL). Another reason for design reuse is that the design of certain functional units of a system may not be within a particular company's areas of expertise. The circuit design information, therefore, must be purchased from other IC design houses, raising complicated intellectual property (IP) issues. The necessary business and legal framework is required to support the use of expertise accumulated from extensive IP outsourcing. The current CMOS circuit design approach of choosing a design style for a specific circuit is likely to continue: noncritical regular circuit structures are likely to be automatically synthesized from high level descriptions while performance critical parts of the circuits are likely to be customized or reused from previous high-performance circuits. Extensive reuse of high-speed functional blocks will likely become a common practice even among the more aggressive IC design companies.

Furthermore, a move to system-scale integration has produced qualitatively new issues. SoCs are heterogeneous in nature. These systems integrate a combination of circuit functionality: digital logic, signal processing and conditioning, memory, communications, analog signal processing. Such diverse functionality necessitates a number of heterogeneous circuits being designed into an integral system and fabricated within a single semiconductor technological process: digital circuitry for control and computation; SRAM, FLASH or embedded DRAM memory for code and data storage; RF for communications; sensors, analog and mixed-signal for interfacing to physical signals, high-speed buses for communication among functional units. This diversity is presenting the circuit design industry with formidable challenges and design trade-offs.

Since the reused cores have not been specifically designed for a target SoC, these circuits can place different constraints on system-wide signals such as the clock and power distribution; additionally, protocols for reset, test and data exchange interfaces can be quite different. Multiple clock domains and asynchronous intercore communication may emerge as viable solutions for multiple core integration. Significant design effort will be required to properly integrate the reused cores into a cohesive SoC without drastically affecting performance. Detailed specifications of the cores are required: circuit delay versus power supply voltage dependence, power consumed versus power supply level dependence, power supply tolerance, peak current, maximum inductance of the power supply bus, clock signal load, clock duty cycle, period, and rise/fall time constraints are just a few of the many system level trade-offs which will need to be integrated into core-based design methodologies. Multiple cores share many system-wide signals; thus, system level trade-offs will have to be integrated into core-based SoC design methodologies. These compatibility and specification issues will require an entirely new set of standards for circuit reuse. Furthermore, the reuse of analog and mixed-signal circuits is far more

difficult than that of digital circuits due to the higher sensitivity to input and output load and parasitic impedances within the linear circuits. New problems affecting the proper operation of the analog circuits have developed such as core-to-core substrate coupling. Substrate coupling remains an open design problem which must be surmounted.

The technical and economic necessity of design reuse will likely lead to a new design paradigm – design for reusability. With a goal of ease of design effort, reuse being a principal design merit, design trade-offs will need to be made at every level of design to render the circuit more easily reusable to a wider range of applications, circuit environments and fabrication processes at the expense of performance, area and power. Multiple versions of the same functional core may need to be individually optimized with each version tailored to a specific application.

While system functionality has been growing at an exponential rate according to Moore's law, the cost of fabricating state-of-the-art ICs has remained relatively flat [3] and the cost of fabricating the same IC drops with time as it is implemented in the newer scaled processes with finer feature sizes. The market has proven to be highly elastic, that is, the cost reduction of semiconductor products has greatly expanded the consumption of ICs. The history of the fast growth of the semiconductor market and projections for the next few years are shown in Figure 3.22. To a great part, this growth has been primarily due to the boom in personal computers. The next major opportunities for high sustained growth in the semiconductor market is internet infrastructure

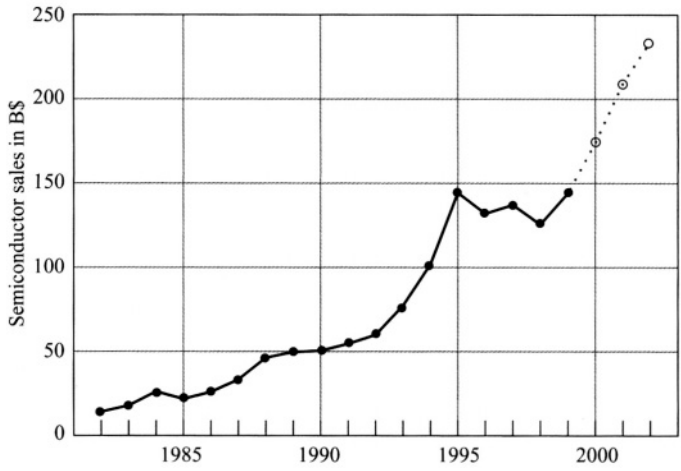


Figure 3.22. History and forecast of semiconductor market sales (with the forecast represented by the dotted line). Data from Semiconductor Industry Association [77].

products, and personal information and wireless communication appliances. While potentially lucrative, personal appliances are a consumer market with inherently tough competition, thin margins, and tight and unforgiving product windows. Low risk design strategies that consider multiple trade-offs at all levels of design abstraction will be required to produce commercial success in a market of commodities.

Summarizing, the following trends will shape the immediate future of CMOS VLSI circuits. As CMOS fabrication technologies are continually scaled at a breathtaking pace and as SoC integration emerges, the process of developing VLSI circuits will become increasingly design productivity constrained rather than technology constrained. High level design capture and design reuse will become important solutions to increase design productivity. Incremental design approaches and design standardization will also be instrumental for effectively reusing existing circuits. Design cost and time will likely dominate decision making in the development of next generation products [78]. Cost, as always, will be crucial in making design trade-offs in semiconductor products that target commodity markets.

Glossary

The following notations and abbreviations are used in this chapter.
Acronyms used in terminology pertaining to VLSI circuits:

IC	integrated circuit
CMOS	complementary metal oxide semiconductor
DSM	deep submicrometer
CPU	central processing unit
RAM	random access memory
DRAM	dynamic random access memory
SRAM	static random access memory
RF	radio frequency
IP	intellectual property
VTC	voltage transfer characteristic
RTL	register transfer level
BIST	built-in-self test
SoC	system on a chip
RE	recurring engineering
NRE	non-recurring engineering

Circuit-specific parameters:

$P_{dynamic}$	dynamic power
P_{sc}	short-circuit power
$P_{leakage}$	power dissipated due to the leakage current

$I_{leakage}$	transistor leakage current when operating in the cut-off mode
I_{out}	gate drive current
I_{peak}	peak magnitude of short-circuit current
I_{D0}	drain current at $V_{GS} = V_{DS} = V_{DD}$
V_{DD}	power supply voltage
V_{Tn}	N-channel transistor threshold voltage
V_{Tp}	P-channel transistor threshold voltage (negative for an enhancement mode device)
V_{D0}	drain saturation voltage at $V_{GS} = V_{DD}$
R_{int}	interconnect resistance
R_{tr}	effective transistor "on" resistance
C_{int}	interconnect capacitance
C_{ox}	gate oxide capacitance per unit area
C_0	input capacitance of a minimum size inverter
C_{gate}	transistor gate capacitance
C_L	load capacitance
μ_n	electron mobility in n-type transistor
μ_p	hole mobility in p-type transistor
W_n	N-channel transistor width
W_p	P-channel transistor width
f	circuit clock frequency
f_{switch}	average charge/discharge cycle frequency
t_{base}	duration of short-circuit current
s	slew rate of a ramp-shaped signal
β	multistage buffer tapering factor
β_{opt}	delay optimal tapering factor
N	number of stages in a tapered buffer
N_{opt}	delay optimal number of stages in a tapered buffer
K	transistor gain factor
A	total active area of a CMOS circuit

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Chapter 4

FLOATING-GATE CIRCUITS AND SYSTEMS

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4.1. Introduction

In this chapter, we will look into the whereabouts of floating-gate circuits and systems. Our goal is to present how floating-gate circuits may be used in a constructive way without any technological "special effects". We will only briefly touch digital circuits and focus primarily on analog properties.

The floating-gate MOS device is not new. Experiments on floating-gate devices from Fairchild Research Laboratories are reported as early as the mid-1960s [1,27]. Some of the first published scientific reports dates back to 1967 [2]. In 1971, the first commercial product was announced and became known as EPROM [3] using a floating-gate avalanche-injection MOS (FAMOS) transistor. Since then floating-gate devices have been utilized in many digital systems. The Flash-EPROM of present computers is storing vital programs (BIOS) and parameters in a non-volatile way using floating-gate structures.

With research in neural networks picking up in the 1980s, demand for analog non-volatile storage arise and floating-gate structures were obvious candidates [4,5]. Fundamentally the stored charge on a floating gate is an analog quantity, but finding ways to control this storage with sufficient precision has turned out to be difficult.

In the following, we will briefly go through the fundamentals of floating-gate physics. Then, we will proceed with simple circuit elements. Finally, we will present some real working circuits and systems.

4.2. Device Physics

The concept of leaving the gate of a MOS-transistor floating is exploring the unique close to infinite input impedance of the MOS-transistor gate. The polycrystalline silicon gate (or polysilicon for short) is electrically insulated from the transistor channel by a thin sheet of silicon dioxide and otherwise wrapped in silicon dioxide [6]. The silicon dioxide is an excellent insulator resisting transfer of electrical charges unless great efforts are made to do so.

In floating-gate circuits we are totally dependent on the insulating properties of silicon dioxide, yet again we need temporarily to break the insulating

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properties of the dioxide in order to manipulate the charge on the floating gate. Sometimes the process of manipulating charge is damaging the silicon dioxide, affecting the long-term properties of the device. In order to get a handle on these matters we will look a little closer at the physical structures involved.

4.2.1. Thin Dioxide

The gate region of a MOS-transistor is one of the most impressive engineering endeavors of modern time. The thickness of this layer is 50–100 times thinner than the transistor width and is typically 10nm in a standard process and is one of the smallest engineering structures in mass production. Still the gate oxide is a perfect insulator preventing current flowing from the gate of the MOS-transistor.

Looking closer at the gate oxide the thickness is not exactly the same all over. In production, the gate oxide is "grown" on top of the extremely planar substrate stacking atoms to form the thin gate oxide. Although this process is well controlled, the growing process will result in a little more "bulky" surface with some variation in oxide thickness.

As feature sizes are constantly reduced in advanced production processes, the gate oxide must be made thinner to ensure optimal operation of the MOS-transistor. But again gate oxide thickness is already approaching the limit were complete insulation cannot be guaranteed. In some of the most advanced processes, the highly appreciated feature of gate insulation is sacrificed for gate efficiency resulting in a small gate current (similar to the base current of bipolars). Leaky gates may be acceptable for digital stuff, but is fatal to floating-gate circuits.

Another important thin oxide is the oxide layer grown between two polysilicon plates to make floating capacitors. Although the production process is somewhat different, the fundamental problems are similar. A significant difference is that inter-poly oxide is grown on top of a polysilicon plate, which is not as planar as the substrate surface. The texture of the polysilicon surface is added to the variation of oxide thickness usually resulting in thicker oxides between polysilicon plates compared to gate oxide of the same process.

4.2.2. Capacitive Connections

All structures in microelectronics separated with thin dioxide are candidates for charge transfer to a floating gate. The standard floating capacitor made by thin dioxide between two polysilicon layers may be used, but there are other options.

The physical structure of a MOS transistor includes several capacitive structures as indicated in Figure 4.1. As we know from MOS-transistor behavior, the dynamic capacitive load is changing with biasing conditions usually leaving



Figure 4.1. MOS transistor.

most of the capacitive coupling between the gate and the source under normal operation. When there is no channel formed underneath the gate, the largest capacitive connection is between the bulk (well) and the gate. In addition, there is a small overlap between the source/drain and the gate. All these capacitive structures may be explored for charge transfer.

4.2.3. Special Process Requirements

In addition to the physical structures outlined above, special processing steps may be introduced to enhance floating-gate features. The patented ETOX process [7,8] from Intel, USA or the HIMOS process [9] from IMEC, Belgium, are both good examples of how dedicated processing steps may be used to enhance FLASH EPROM properties. Although additional processing steps could be beneficial also for analog applications of floating gate, we will restrict our efforts to features available in most standard CMOS.

In general, floating-gate structures are demanding a floating capacitive connection to the gate, making double poly a necessary requirement for usable floating-gate circuits. Although single poly-solutions are possible using other capacitive structures, the degradation in performance is too severe. Other than double-poly structures, we will not require additional processing steps for the circuits presented here.

4.3. Programming

Equipped with the understanding of available physical structures, we will turn to techniques for adding or removing charge from a floating gate. In short, we want to make an insulator slightly conductive, which in general is rather hard. Within normal operation the silicon dioxide is behaving as a perfect insulator. Unless we expose the floating gate to a rather hostile and abnormal environment, the silicon dioxide withstands all attacks. In the process of transferring charge under extreme conditions, we may accidentally damage the silicon dioxide reducing the excellent insulating properties. In the following, we will review the three most frequently used techniques.

The best way to understand all these methods of charge transfer is to grasp the notion of energy barriers and tunneling. The charge stored on the floating

gate is "fenced in" by an energy barrier provided by the insulating silicon dioxide. Free particles like electrons are trying to move through the energy barrier, but will not usually make it all the way through and will bounce back again. However, if we both make the energy barrier thin and give the free particles sufficient energy, particles are able to penetrate the energy barrier all the way through the other side. This process is a quantum mechanical effect called tunneling.

4.3.1. UV-conductance

The classical mechanism for making silicon dioxide conductive is by using short-wave ultra-violet light, known as UV-C. The nominal wavelength of the light source should be 254 nm emitting high-energy light (so please wear eye-protection!). Those of you who know about EPROM-erasers are already familiar with an adequate light source. Exposing silicon dioxide to UV-C will shake loose free electron–hole pairs with sufficient kinetic energy to surmount the silicon dioxide energy barrier fencing in the floating-gate charge.

As the sun does not burn behind a window, so do also most materials shield UV-C light. Care must be taken to make the UV-light come through all the way down to the desired silicon dioxide. Most standard CMOS production lines cover the wafer with one or several passivation layers containing nitride, effectively preventing UV-light to pass. Polysilicon itself is absorbing UV-light leaving us with a conductive edge to the layer underneath.

The efficiency of UV-light conductance is not high since the UV-activated current through silicon dioxide is really small. In the old days of EPROM, you may recall an erase time of more than half an hour. With reduced feature size, the UV-conductance is increased, but most operations are still counted in minutes.

4.3.2. Fowler–Nordheim Tunneling

Another well established technique for charge transport through silicon dioxide is called Fowler–Nordheim (FN) tunneling after the first researchers pointing out (in 1928) that electrons may tunnel through an energy barrier provided a sufficient electric field. The silicon dioxide is shielding the floating-gate charge with a 3.2 eV energy barrier. The thickness of this "wall" is proportional to the thickness of the silicon dioxide and again determines the strength of the electric field required for tunneling of particles to occur. The FN tunneling is applicable to most structures insulated by a thin layer. Thicker insulating layers may also be used, but the voltage across the dioxide must be raised accordingly. An inherent problem of FN tunneling is the texture of most insulators grown on silicon leaving a variable thickness. FN tunneling is an exponential function of both field and insulator thickness leaving most of the current

flow to the thinnest sports of the insulating silicon dioxide. These local high current sports are called "hot spots", since the current may locally be so high that the silicon diamond lattice is broken, leaving open traps for free carriers. The long-term effect is called "wear-out" of the silicon dioxide making it leaky. Wearing out the silicon dioxide is the fundamental reason for a limited number of reprogramming of FLASH EEPROMs frequently used for BIOS in most PCs.

FN tunneling may be fast, provided sufficient electric fields across the silicon dioxide. Programming is usually carried out in μs. The trade-off between speed and wear-out is evident; faster programming implies higher fields, but increased damage to the silicon dioxide.

4.3.3. Hot Carrier Injection

The most complicated method for charge transfer is called "channel hot carrier injection" or just hot carrier injection (HCI). The idea is to produce free carrier with sufficiently high energy in the channel underneath the gate. Carriers with sufficient energy (>3.2 eV) to tunnel through the thin gate oxide are called "hot carriers". Due to collisions in the channel, the free carriers will scatter in random directions and a fraction will accidentally tunnel through the gate oxide. Normally, we do not experience any effect of this process present in every MOS-transistor because the electric field in the gate oxide makes the carriers bounce back to the channel. So, we need to help this process by providing an electric field towards the gate. Looking closer at the transistor channel, we find the hot carriers located close to the drain side.

The HCI technique may be used to implement fast transfer of gate charge, but is usually requiring fairly high channel currents and the desired electric field in the gate oxide is not always easy to establish without special processing effects.

4.4. Circuit Elements

The basic floating-gate MOS transistor (FGMOS) is shown in Figure 4.2. As illustrated in the figure, the floating gate is inserted between the transistor

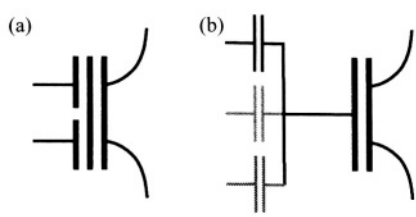


Figure 4.2. Floating-gate MOS transistor.

channel and a *control gate* giving indirect, capacitivly coupled control over the MOS-transistor operation. The symbol in Figure 4.2(a) indicates a stacking of the control gate on top of the actual transistor gate, which is done in most commercial EEPROM production. It is possible to split the control gate on top of the floating gate and also move the control gate capacitor away from the MOS-transistor as indicated in Figure 4.2(b). With the capacitors aside the MOS-transistor, it is possible to have several control gates with larger freedom in sizing, but the penalty is increased area.

4.4.1. Programming Circuits

In the following, we will use the word *programming* for the controlled manipulation of floating-gate charge. We will approach the programming process from a regular CMOS process perhaps with the addition of two layers of poly silicon. Although the fundamentals of FGMOS transistors are simple, putting FGMOS into usable circuits seem to be difficult. The combination of manipulating the charge on the floating gate and at the same time maintaining a valid output is demanding. Do not trust floating-gate circuits unless a validated programming strategy is included.

We will start with some simple programming structures using inter-poly tunneling.

Inter-poly tunneling. Most likely the simplest circuit for programming the stored charge on a floating gate is the use of two capacitors as shown in Figure 4.3. As indicated the small capacitor is used to set up a field for FN tunneling over the inter polysilicon oxide without affecting the stored gate voltage too much. The voltage on the control gate will to a large extent determine the actual voltage on the floating gate.

The programming procedure is carried out using FN tunneling both to increase charge and decrease charge on the floating gate. In order to obtain a sufficient field over the C_{tunnel} capacitor, a voltage between 10 and 30 V must be applied. Increasing the V_{tunnel} voltage removes charge and increasing the

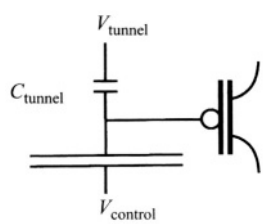


Figure 4.3. Simple inter-poly tunneling structure.

$V_{control}$ voltage is adding charge. The programming process is certainly affecting the drain–source current of the transistor and must be taken care of in actual circuits. Raising the $V_{control}$ voltage will also set up a field over the gate oxide and possibly cause some damage with a nMOS transistor since the channel is connected to the ground reference. For pMOS transistors, the channel is connected to the well potential, reducing the gate-channel potential with the power supply voltage.

Example: Floating-gate on-chip knobs. Inter-poly FN tunneling was used by Lazzaro et al. [10] to set biasing voltages and store the programmed value as a voltage on a floating gate. An elegant event-driven asynchronous digital bus structure (AER) was used both for programming and read-out of stored values. The core of the analog knobs was the FGMOS with dual control gates as shown in Figure 4.3.

The programming circuits as shown in Figure 4.4 has two "one-shots" or monostables firing a "crank up" or "crank down" pulse depending on which pin is activated. Following the one-shots a high voltage driver converts a low-voltage pulse to a suitable FN tunneling voltage. Different voltages are required for the two high-voltage drivers. Supplying high voltage requires some care, but the switching is done locally reducing cross-talk to a minimum.

These knobs were implemented in a standard MOSIS process and 30 analog parameters were controlled in this way.

Inter-poly UV-programming. Another simple method for charge transfer is to use short-wave UV-light exposing a poly1–poly2 capacitor.

As indicated in Figure 4.5, the poly2 plate is smaller than the poly1 plate. Polysilicon is opaque to UV-C light, so the only areas where the UV-activated conductance occurs is along the poly2 edge. With the poly1 plate close by, a small current will flow between the plates proportional to the voltage difference. Unfortunately, the UV-conductance is reduced in a non-linear way when the

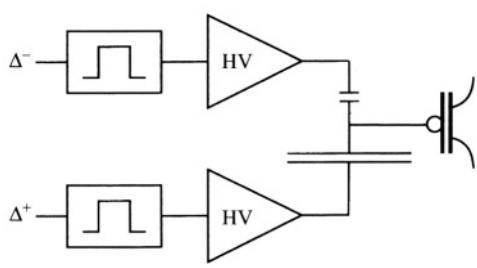


Figure 4.4. FGMOS tuning knob as presented in [10].

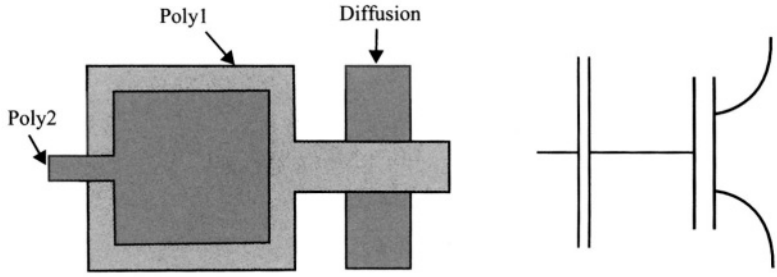


Figure 4.5. Layout of inter-poly UV-activated tunneling.

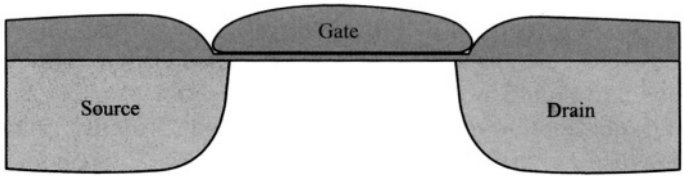


Figure 4.6. The MOS-transistor showing the source/drain overlap.

potential difference is approaching zero [11], but with some gain in the control loop, this structure may still be used. Due to the thicker inter-poly oxide, the UV-activated conductance is rather small making the programming process slow. It is also important to prevent UV-exposure to other areas of the chip shielding with metal layers and passivation.

MOS-transistor UV-conductance. Since the MOS-transistor itself has the thinnest oxide layers available it is tempting to use the thin gate oxide between the active diffusion layer (source/drain) and the floating gate.

As most experienced engineer will know there is an overlap between the source/drain active diffused substrate and the polysilicon gate as indicated in Figure 4.6. We may use this overlap capacitance constructively to program the floating gate. Simply exposing the gate with UV-C light will certainly introduce an UV-conductance between the source/drain and the gate. As for inter-poly structures, we may both add and remove charge. There is, however, a significant difference due to the work function difference between polysilicon doping and substrate doping. N-doped polysilicon is most frequently used. Stacked on top of N-doped substrate the UV-programming will converge towards a –0.6 V voltage difference. If N-doped polysilicon is stacked on top of P-doped substrate a –1.1 V work function difference must be accounted for.

Compared to inter-poly UV-programming, these structures are doing better due to thinner gate oxide. A typical programming cycle would be some minutes.

Example: MOS transistor threshold tuning. As an example of how this UV programming technique may be used, we will show a circuit-configuration where the effective threshold voltages may be tuned in a simple way. This tuning technique proposed by Yngvar Berg at Department of Informatics, University of Oslo [12]. Tuning of high precision analog circuits is typically done with laser trimming burning off resistive connections, but FGMOS structures for trimming analog circuits have also been reported [13–15].

The fundamental structure is built around a simple CMOS inverter as shown in Figure 4.7. The FGUVMOS transistor is simply a regular MOS transistor with a UV-window on the source side of both the nMOS and the pMOS transistor. The UV-window is created with an opening in the passivation layer just above the transistor. By bending the design rules for pad-openings a little, it is feasible to make smaller openings in the passivation layer. A $5\,\mu m \times 5\,\mu m$ micrometer passivation opening seem to be OK. The more detailed shielding within the UV-window is done with the metal layers leaving only the source side of the transistor exposed to UV-light.

The tuning is done using the supply rails. Under UV-light exposure, the power rails are reverse biased taking the ground terminal to some positive voltage while flipping the V_{dd} rail to some negative voltage. The reverse biasing does not result in any problems (like forward biased junction diodes) provided the substrate is disconnected from the ground-rail. Now the reverse biasing flips the source and drain terminals of the transistors setting up two source followers to the output node leaving the high impedance drain terminals to the rails. Under UV-exposure, there is a small conductance between the floating gate and the rails, which are now available to play with for setting a suitable

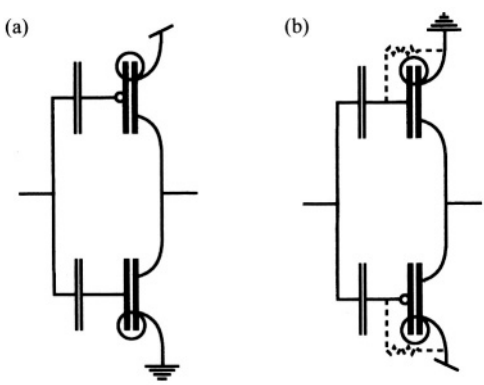


Figure 4.7. FGUVMOS inverter with power biasing (a) under normal operation and (b) during programming with UV-C light.

programming voltage accounting for work function differences. By monitoring the output voltage, the source followers should provide the input voltage on the output when both source followers are active. An even better control is possible when the current is monitored.

This tuning procedure is providing a simple way of post-fabrication tuning of threshold voltages enabling low-power/low-voltage operation in standard CMOS. The threshold programming is done at chip level programming all transistors in one programming cycle. By reducing the threshold voltages, more speed is obtained at the cost of more power consumption. A consequence of the rail tuning is that only two transistors may be stacked; one pMOS on top of one nMOS. Complete circuits using FGUVMOS transistors will be presented later.

Combined programming techniques. The combination of HCI and FN seem to be a winner. In almost every commercial available EEPROM or FLASH EPROM, FN tunneling is used for removing floating-gate charge while HCI is used for adding floating-gate charge. The EEPROM processes have special processing steps not available in a standard CMOS process.

A group at California Institute of Technology [16,17] demonstrated how a standard MOS process might be twisted to implement the same features as in a dedicated EEPROM processes.

Figure 4.8 show how the structure is implemented and at the bottom, the programming is illustrated with an energy diagram. The left part is a stacked floating-gate pMOS transistor (a regular pMOS with the control gate aside would do as well). The right part is a transistor-like structure used for tunneling.

The HCI is achieved in an elegant way with only subthreshold currents (<100nA)! The majority carriers being holes in pMOS transistors are accelerated entering the channel from the drain of the pMOS. The high-energy holes collide with the semiconductor lattice shaking loose electron–hole pairs (impact ionization). The energy barrier made up by the silicon dioxide towards the gate is approximately 3.2 eV, but since the liberation of electrons is an indirect quantum mechanical process, a little more than 6 V drain-channel potential difference is required before the electrons have enough kinetic energy to surpass the silicon dioxide energy barrier. In addition, we need an attractive field towards the floating gate. Since the source–gate voltage in subthreshold is less than the threshold voltage of the device, with the source above 6 V, the gate–drain voltage is at least 5 V ensuring a nice attractive field for hot electrons. pMOS transistors are naturally suited for HCI. Just leave the drain to ground and crank the source/well potential up to a little above 6 V. Use the control gate to let through a small current and you will see electrons added to the floating gate reducing the voltage.

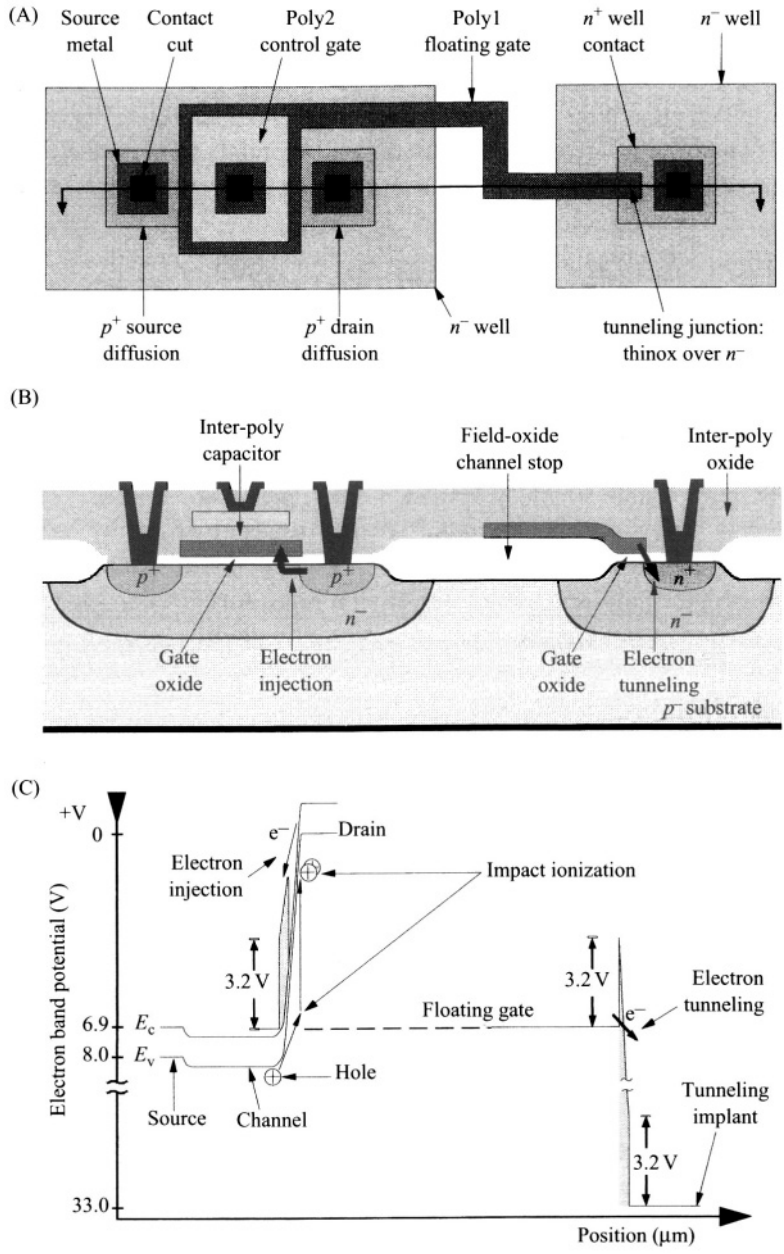


Figure 4.8. pMOS HCI and tunneling structure (kindly provided by Chris Diorio [16]) with a MOS structure to the left explaining the process of HCI. To the right a simple FN tunneling structure is shown. Side view (B) and electron band diagram (C).

The reverse process of removing electrons from the floating gate is done with FN tunneling. A nMOS transistor (without separate source/drain terminals) located in an n^- well (reducing the n^+ source/drain region to a well-contact) is used to build a tunneling structure between the well contact and the polysilicon. Since the well is following the well contact potential, some tunneling might happen between the well and the polysilicon, but the well is lightly doped and is depleted when the potential is raised, leaving the tunneling to the edges overlapping the heavy doped well contact. Depending on the gate oxide thickness a significant voltage must be supplied. In [18] approximately 33 V is reported for a 350 Å thick gate oxide. This voltage should be much lower in a modern process with typically 100 Å gate oxide.

It is hard to make HCI structures with standard nMOS transistors since establishing a sufficient field between the gate and the channel will result in a significant current flow. It is, however, possible to shift the threshold voltage using base implant available in some BiCMOS processes [16,18].

Recently, an even simpler structure is reported [19] where the tunneling is done by raising the source/drain/well voltage of a standard pMOS until tunneling occurs in the gate–source/drain overlap region. An even denser structure is achieved eliminating the need for the separate tunneling structure to the right of Figure 4.8.

Example: Single transistor synapse. As the focus on neural networks caught up in the 1980s, efforts to implement these computational systems in analog microelectronics were initiated. The basic computations required like multiplication and addition came easy and promised dense and effective systems. The killer in most of these efforts was lack of permanent weight storage [20]. Using digital weights introduced data-converters and consumed a lot of area. The only real analog weight around was FGMOS transistors.

Based on the FN-HCI structure combined weight storage and multiplication may be implemented in a single transistor as shown in Figure 4.9 [21].

In several neural network algorithms some input value represented by the voltage V_{in}, is multiplied by some weight represented by the stored charge on the floating gate. Assuming weak inversion, we may express the source–drain current sourced by the pMOS transistor as:

$$I_{\text{out}} = I_s \cdot W \cdot \exp\left(\frac{V_{\text{in}}}{nU_T}\right) \tag{4.1}$$

I_s is the specific current, n is the slope factor (process dependent constant typically around 1.5 for pMOS transistors), and U_T the thermal voltage ($\approx 25\,\text{mV}$ at room temperature). We have a multiplication between the stored weight, W, and an exponential function of the input voltage, V_{in}. Since we need to bias the gate, source and drain voltages during programming, the output will not

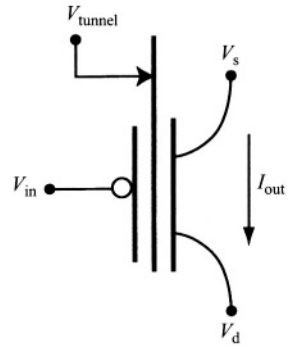


Figure 4.9. The single transistor synapse.

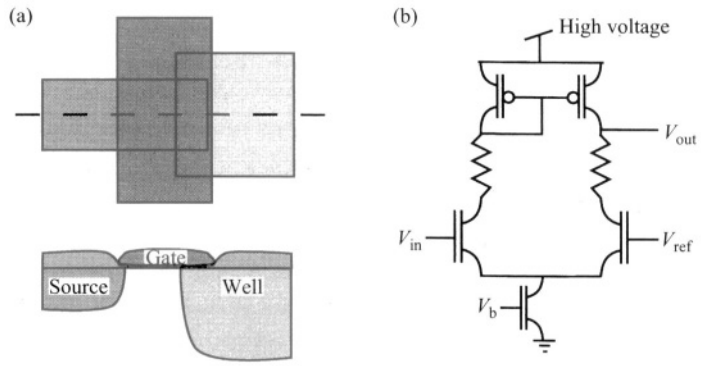


Figure 4.10. (a) The physical implementation of the DMOS transistor and (b) the DMOS used in a high-voltage driver.

continuously supply the correct value, but some sort of short-term capacitive storage may be used.

High-voltage drivers. Working with FN-tunneling relatively high voltages are needed. Even in commercial EEPROMs they really use voltages around 12V inside the chip, but these voltages are generated on-chip with charge-pumps. Handling higher voltages in standard CMOS may cause problems. However, there are a couple of ways to get along making high-voltage drivers without extra process requirements.

As suggested in Figure 4.10(a), a MOS transistor with a significant drain resistance may be realized substituting the heavily doped drain diffusion with a lightly doped well. Since the gate is not self-aligned to the well, some overlap

must be added. Designing the DMOS with some length up to 60 V may be applied as source–drain voltage without breaking anything.

The long-tailed pair using DMOS transistors will handle high voltage power supplies and the output voltage will be driven to the upper rail voltage when $V_{in} > V_{ref}$, but when $V_{in} < V_{ref}$, the output voltage will fall until punch-through will occur in the output-transistor of the current mirror. With tail current adjustments the "off" voltage may be set to some . The bias current may be limited (even to weak inversion) avoiding power waste. Lazzaro et al. [10] is using a similar structure as a low-to-high voltage buffer for controlling FN tunneling.

4.5. FGMOS Circuits and Systems

Equipped with the programming strategies outlined above we are now able to proceed to some real reported circuits. A careful selection of working circuits with measured results is briefly presented together with references for further reading.

4.5.1. Autozero Floating-Gate Amplifier

Most of us are familiar with biasing circuitry often occupying more chip area than the primary circuit itself. The "Autozeroing Floating-Gate Amplifier" (AFGA) [22,23] is one of my favorite floating-gate circuits solving the classical problem of setting up a suitable operation point in analog circuits without adding a lot of biasing circuitry.

The circuit as shown in Figure 4.11 is build around a pMOS common source configuration with an nMOS transistor as constant current load. The control gate (V_{in}) is the input. A feedback capacitor (C_2) sets up the closed loop gain to approximately $-C_1/C_2$. As a normal inverting amplifier the upper frequency range is determined by the gain of the amplifier and the load capacitance (C_{load}) on the output. For low frequencies we apply suitable voltages to both the positive power rail and the V_{tunnel} input terminal, setting up both a small tunneling current dragging out electrons from the floating gate and a small injection current adding electrons. There is an equilibrium state where the tunneling current is matching the injection current setting up the input operating voltage. Since these currents are really small, the input operating point correction is happening slowly and is setting up the lower end of the frequency range (usually in the mHz or even μHz range). As consequence of the tunneling process is a high-pass filtering function taking out the DC of the input signal, meaning autozeoring the amplifier.

In Figure 4.12 measured results from an AFGA is shown for to different gain settings. As expected we have a band-pass function with a low

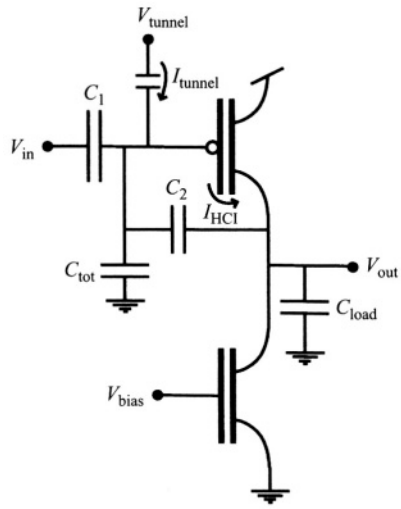


Figure 4.11. Autozeroing floating-gate amplifier from [23].

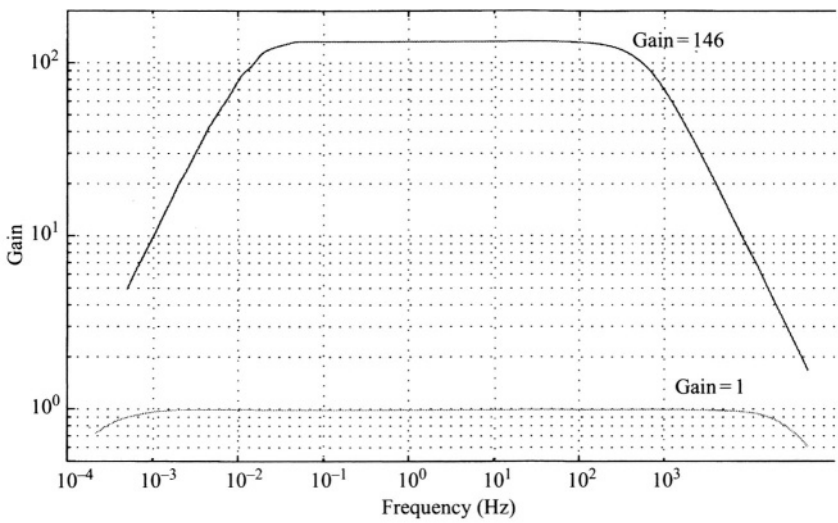


Figure 4.12. Measured frequency response for AFGA amplifier kindly provided by Hasler [23].

frequency roll-off starting below 0.1 Hz. The DC level of the input signal is filtered and the operating point is set by the FGMOS programming currents. A complete discussion of these kinds of amplifiers may be found in [23].

4.5.2. Low-power/Low-voltage Rail-to-Rail Circuits Using FGUVMOS

The FGUVMOS inverter presented above is using UV-C light to manipulate charge on the floating gate using no additional wires. Post-fabrication circuit tuning using the FGUVMOS transistor might be a nice way to use the fairly slow, but global UV process (imagine programming all transistors on a complete wafer).

There is, however, a somewhat hidden penalty since both wells and substrate biasing cannot be shared with the power rails of the circuit. Also, these kinds of circuits are using a lot of capacitors. Nevertheless, experience seems to verify that area-penalty is minor even compared to traditional analog and digital circuits. Remember the capacitors are all small (approximately twice or three times the gate area) and virtually no biasing circuitry is required.

Another property of FGUVMOS circuits is that no stacking of transistors is possible. All pMOS transistors must be source-connected to the positive power rail while the nMOS transistors must be source-connected to the negative power rail. The important question remains; how do we make usable circuits within these limitations?

Surprisingly enough both analog amplifiers and digital gates may be implemented with the following benefits:

1 Low-voltage rail-to-rail operation in standard (normal threshold) CMOS.

2 Trading speed for power by threshold voltage adjustment.

3 Reduced threshold voltage spread due to current matching under programming.

Digital FGUVMOS circuits. The FGUVMOS inverter was already presented in Figure 4.7. To show the feasibility of FGUVMOS circuits, some measured results of a single FGUVMOS inverter are shown in Figure 4.13. Operation voltages down to 0.3 V are feasible in standard high-threshold CMOS. Some gain-adjustment is also possible by playing with the threshold voltages, but will always be limited by the relative g_m of the MOS device.

In Figure 4.14, the circuit configurations for FGUVMOS implementation of NAND and NOR gates are presented [24]. The general idea is to eliminate stacked transistors with multiple control gates. This procedure, however, have practical limitations, since one control gate act as capacitive load for the other, ultimately limiting performance.

Low-voltage rail-to-rail FGUVMOS amplifier. The simplest FGUVMOS amplifier configuration is based on the FGUVMOS inverter (Figure 4.7).

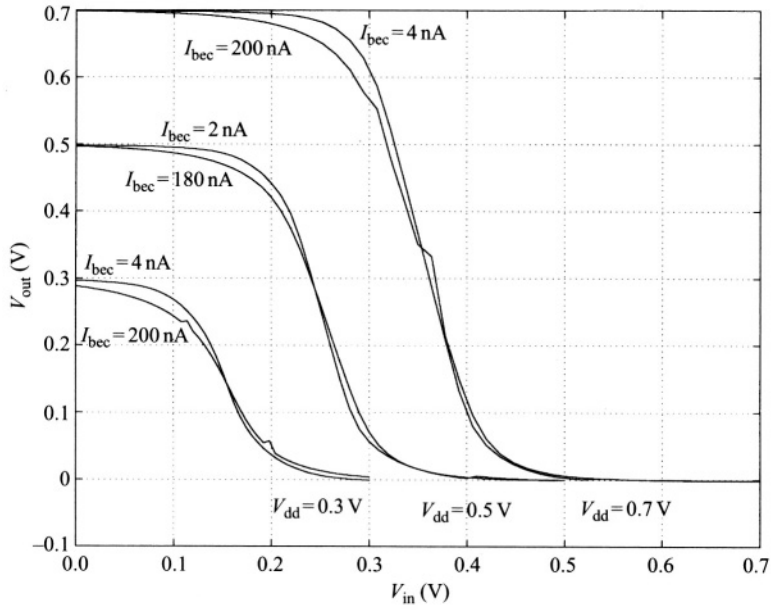


Figure 4.13. Measured inverter characteristics kindly provided by Berg [26]. A CMOS inverter is programmed to operate at 0.7, 0.5 and 0.3 V. The nominal threshold voltages of nMOS is 0.7 V and pMOS is 0.9 V.

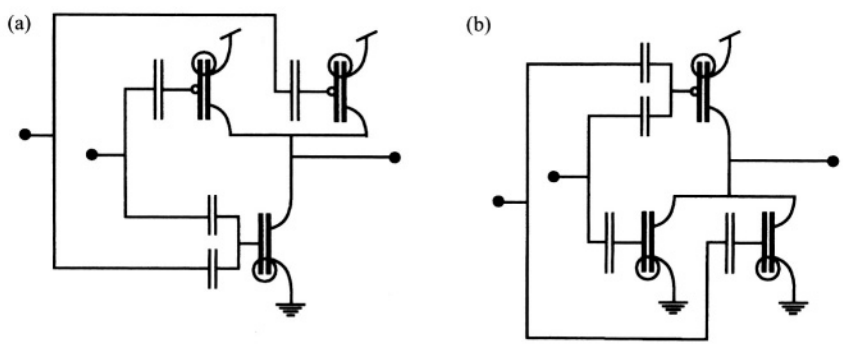


Figure 4.14. FGUVMOS digital gates [24].

In order to reduce the gain of the inverter, a feedback capacitor is added between the output and the floating gates to the left of Figure 4.15. The closed-loop gain is approximately $C_{p(n)}/C_f$. Additional tuning is available if additional capacitors are added (grayed out in Figure 4.15). To the right a dual input inverter stage is added. The V_1 voltage is inverted in the first stage and fed

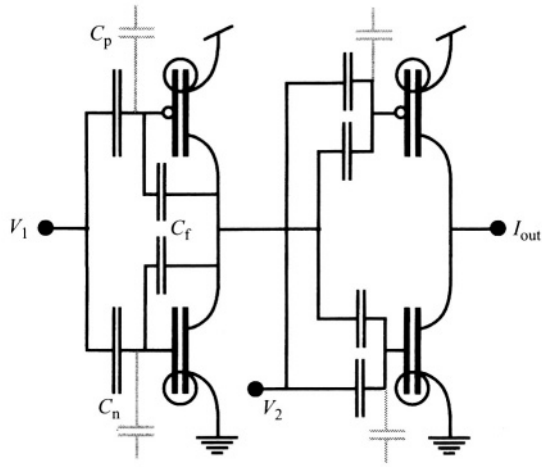


Figure 4.15. The FGUVMOS amplifier [25].

directly to one control gate of the output stage. The other differential input is simply the other control gate of the output stage. In weak inversion, the transfer function is

$$I_{out} = 2I_b \sinh\left[\frac{1}{nU_T}(V_1 - V_2)k_i\right] \tag{4.2}$$

Here, the bias current, I_b, may be set either by UV-tuning or with additional tuning capacitors indicated in gray. n (≈ 1.5) is the slope factor and U_T (= 25 mV at room temperature) is the thermal voltage. k_i is the *capacitive division factor* expressing the coupling efficiency seen from the input. Also tanh( ) transfer functions is available and a combination of sinh( ) and tanh( ) gives a close to linear transfer function [26].

The nice feature of this amplifier is rail-to-rail operation if "threshold-voltages" seen from the control gates are reduced. Furthermore the amplifier is able to operate for extremely low supply voltages (measurements?).

4.5.3. Adaptive Retina

One of the remarkable applications of FGMOS is the "Adaptive retina" chip [27] published in 1989. "Salt-and-pepper" noise is a well-known problem in imagers, where device mismatch is directly visible, as significant random variation in measured light-intensity with uniform illumination. With post-processing most of these offsets may be compensated for, but mimicking properties in the human retina as a simple, real-time, analog systems requires other solutions.

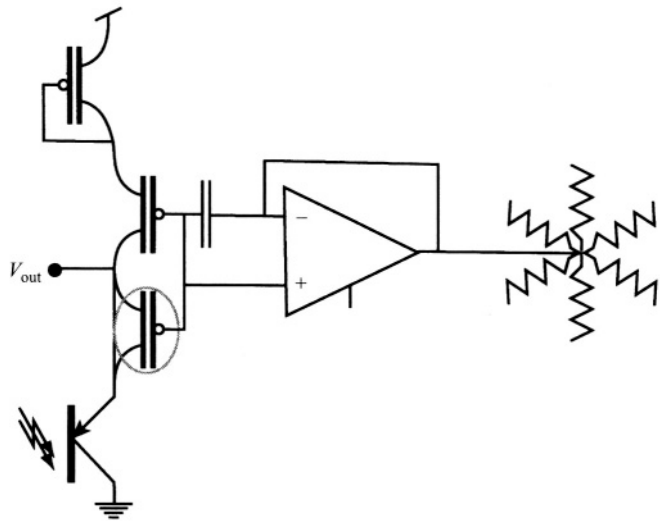


Figure 4.16. The adaptive FGMOS photo sensor.

The adaptive photo sensor used for the "Adaptive retina" chip is shown in Figure 4.16. The transducer is a well bipolar phototransistor. A suitable bias-current is provided by two diode-connected pMOS transistor, where the lower diode has a FGMOS compensation circuit inserted. The output voltage is read through a FGUVMOS transistor attached to the output node (indicated with a gray circle in Figure 4.16). The FGUVMOS transistor is not in series with the current source, but is only used to introduce an UV-activated resistive connection to the output node. A differential amplifier is used as a biased-controlled conductance, providing a current to a resistive hexagonal network (electronic spread).

When the silicon retina is exposed to UV-C light, a uniform illumination is provided together with a UV-activated conductance. The differential amplifier will amplify differences between the average value provided by the resistive network and the measured photocurrent. Depending on the strength of the electronic spread and the g_m of the amplifier, some voltage shift will appear in the local average. The local average is fed back through the control gate closing the adaptation loop.

Hundreds of these photo sensors are stacked in a two-dimensional structure and scanned out on a monitor. From experiments, the "salt-and-pepper" noise is removed providing a uniform image from the silicon retina. To my best knowledge, the adaptive retina is the first *FGMOS analog adaptive system* implemented.

4.5.4. Other Circuits

In this book, only a small selection of published FGMOS circuits are presented. There are a number of beautiful circuits published. Barrie Gilbert proposed the translinear circuit principle back in the 1970s. In [28,29], Minch is using multiple input FGMOS structure to implement translinear elements in weak inversion MOS. Both amplifiers [30,31] and non-linear winner-take-all circuits [32] are reported.

4.6. Retention

An ever-returning question is for how long does the charge stay unchanged on the floating gate. An undamaged silicon dioxide will keep the stored charge for a long time. With time-constants counted in decades it is kind of hard to handle this question. It might be tempting to say; "Long enough, based on experience", but this is too easy. For digital systems heating the silicon does a provoked aging, giving some indications of expected retention time. Typical numbers are less than 1% in 10 years, but for analog values this might be a lot. To my best knowledge there are no published results on charge retention for analog circuits. For now we have to use good engineering practice based on what we know about basic physical mechanisms and avoid conditions promoting floating-gate charge transport.

A specific problem occurs with FN tunneling and HCI (not with UV) when high-energy particles are breaking down the semiconductor lattice leaving open "wounds". These defects may temporary trap electrons helping them on their efforts to penetrate the silicon dioxide. With a sufficient number of traps, a leakage current will occur. This phenomenon is called "wear-out" of the silicon dioxide. The problem may be reduced if only small tunneling currents are used.

This retention problem is also transient due to the rapidly developing technology. In some ways reduced feature sizes is improving floating-gate capabilities through reduced dioxide thickness, leading to increased programming speed for all known methods. Unfortunately the dioxide thickness of advanced processes is approaching a limit were both HCI and FN tunneling will happen under normal operation. Dioxide thickness less than 5 nm is starting to leak. In [33] measurements of both FN tunneling and HCI is reported for dioxides less than 3 nm exhibiting significant current through the gate dioxide under normal operation. For floating-gate purposes these devices cannot be used.

4.7. Concluding Remarks

The merits of floating-gate circuits are quite impressive. All those millions of nodes left floating in PCs today should account for something reliable and well known. Surprisingly enough the skepticism to floating gates as constructive

elements in both analog and digital circuits is strong. There are some understandable reasons to avoid floating gate like special process requirements, area penalty, high voltages and retention problems, but with adequate insight these obstacles may be handled.

Floating-gate devices are available in any CMOS process and may be utilized as constructive elements in both analog and digital systems.

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Chapter 5

BANDGAP REFERENCE DESIGN

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5.1. Introduction

For many years bandgap references have been used as voltage references in various fields of application; for instance, in DA converters [1], automotive industry [2] or battery-operated DRAMs [3].

All of the bandgap references used in this diverse variety of applications are based on the idea of Hilbiber in 1964 [4]. After his publication, a vast number of articles appeared describing other topologies and components being used [5–11]. In this chapter, a structured design method is presented which structures the knowledge gained in the past decades concerning bandgap reference design and from that an extrapolation is made.

Explicit relations are derived between, for instance, the noise level and the current consumption. In this way existing trade-offs are made explicit. To get a clear insight into the bandgap reference to be synthesized, first a general description is given of a bandgap reference, see Section 5.2. The base–emitter junction is used as the core element for bandgap references. Section 5.3 describes its temperature behavior. Subsequently, Section 5.4 describes in general terms the temperature compensation of the base–emitter voltage in order to approximate a temperature independent voltage. It is shown that the general bandgap reference can be described by a linear combination of base–emitter voltages. This linear combination is used as a high-level description for temperature compensation, Section 5.5. From this description, the key parameters for bandgap reference design are derived in Section 5.6. Then, as the basic structure of the bandgap reference is found, the influence of the temperature dependency of resistors can be described at a high level of abstraction, Section 5.7. Section 5.8 describes the trade-off between the noise level and the current consumption. From the high-level description of the bandgap reference, found in Section 5.4, simplification can be made leading to some specific structures with nice properties, see Section 5.9. Section 5.10 shows in an overview two design examples. Finally, conclusion for this chapter is given in Section 5.11.

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5.2. The Basic Function

The starting point is to describe the basic function to be realized: *a reference voltage,*

V_{REF}, related to the bandgap voltage at 0 K, $V_G(0)$ or:

$$V_{REF} = x \cdot \frac{E_G(0)}{q} = x \cdot V_G(0) \tag{5.1}$$

where q is the electron charge (1.6e – 19 C), x is a constant scaling factor accounting for reference voltages not equal to the bandgap voltage and $E_G(0)$ is the bandgap energy at 0 K. For realizing a bandgap reference, at least one component must be available of which a port voltage is related to the bandgap energy. Generally, this core component of the bandgap reference is the bipolar transistor as the base–emitter voltage is related to the bandgap energy in a very simple and accurate way, see Section 5.3. Even in most MOS bandgap references at least one bipolar transistor/junction is used for the relation to the bandgap energy [9,10–16]. However, in [17] the difference of two gate–source voltages with different polysilicon-gate work functions is proposed to realize a voltage, which is related to the bandgap energy.

Since with bipolar transistors as core component more accurate bandgap references can be made than with MOS transistors, because of better matching [18] and modeling, and thus reaching the ideal reference the best, here the bipolar transistor is chosen as the core element of the bandgap reference. Still, MOS transistors can be favorably used in other parts of the bandgap reference because of their high DC gain.

5.3. Temperature Behavior of V_{BE}

The temperature behavior of the base–emitter (V_{BE}) voltage is the key item in bandgap reference design. The basic relation is:

$$I_C(T) = I_S(T)\left[\exp\left(\frac{qV_{BE}}{kT}\right) - 1\right] \tag{5.2}$$

with I_C the collector current, I_S the saturation current, T the absolute temperature and k the Boltzmann constant ($1.38 \cdot 10^{-23}$ J/K). Suppose the transistor is biased with a temperature-dependent current $I_C(T)$ that can be described by:

$$I_C(T) = I_{C0}\left(\frac{T}{T_0}\right)^{\theta} \tag{5.3}$$

with I_{C0} the current at temperature T_0 and θ the order of the temperature behavior of the current (e.g. $\theta = 0$ means a constant current and $\theta = 1$ means

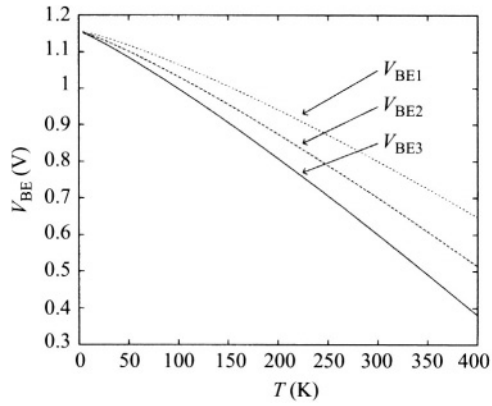


Figure 5.1. The base–emitter voltage as a function of temperature for several values of V_{BE}, $V_{BE1} > V_{BE2} > V_{BE3}$.

a PTAT[1] current). Then the base–emitter voltage is given by [19]:

$$V_{BE}(T) = V_G(T) - [V_G(T_r) - V_{BE}(T_r)]\frac{T}{T_r} + \frac{kT}{q}(\eta - \theta)\ln\left(\frac{T}{T_r}\right) \quad (5.4)$$

with T_r being the center of the temperature range for which the bandgap reference has to be designed, $V_{BE}(T_r)$ the base–emitter voltage at that temperature, $V_G(T)$ the bandgap voltage and η the order of the temperature dependency of the saturation current I_S of the transistor (corresponding to X_{TI} in SPICE). This expression is depicted in Figure 5.1 for several values of the base–emitter voltage.

Some general conclusion can be drawn from this picture. Independent of the value of the base–emitter voltage at T_r, the base–emitter voltage at 0 K always equals $V_{G(0)}$ and its temperature dependency is always negative. Further, for higher base–emitter voltages, the temperature dependency of the base–emitter voltage reduces. How these properties can be used to realize a bandgap reference is the topic of the next section.

5.4. General Temperature Compensation

The expression for the base–emitter voltage found in the previous section, is the key expression for bandgap reference design. Figure 5.2 depicts how a temperature-independent voltage can be realized. An additional voltage V_{COMP} compensates for the temperature dependency of the base–emitter voltage. Consequently, the sum of V_{BE} and V_{COMP} equals, over the total temperature range,

[1] Proportional to absolute temperature.

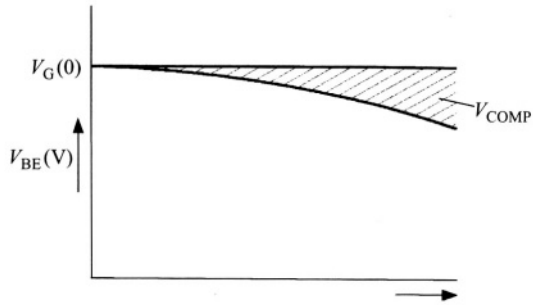


Figure 5.2. The principle realization of a bandgap reference.

$V_G(0)$. As this voltage is independent of all kinds of parameters, a true reference is obtained.

However, it should be noted that for higher doped base regions, higher than $10^{17}\ \mathrm{cm}^{-3}$, bandgap narrowing may slightly change the value of $V_G(0)$ [20].

For exact compensation, V_{COMP} is a complex function of the temperature and not easy to realize. Therefore, the temperature dependency chosen for V_{COMP} is less complex and, consequently, a remaining temperature dependency is found. V_{COMP} can be realized with several temperature-dependent voltages. For instance, in [9] V_{COMP} is partially realized by a voltage which is related to the temperature behavior of the base current. In that case, however, two different physical processes are used to compensate each other. Their sensitivity to process variations, for instance, may be different resulting in a larger spread. In this chapter, base–emitter voltages are also used for the compensation voltage.

Thus, the bandgap reference is realized by a weighted sum of base–emitter voltages, that is, a linear combination.

5.5. A Linear Combination of Base–Emitter Voltages

As the base–emitter voltage is a function of the temperature a weighted sum of a number of V_{BE}s is a function of the temperature too. It is convenient to express this sum as a Taylor polynomial:

$$V_{REF}(T) = \sum_{m=1}^{i} a_m V_{BE_m} = \gamma_0 + \gamma_1(T - T_r) + \gamma_2(T - T_r)^2 + \cdots \qquad (5.5)$$

with V_{REF} the sum of the V_{BE}s, a_m the scaling factors and γ_i the Taylor coefficients.

In order to find the values of a_m and V_{BEm} the weighted sum of equation (5.5) is evaluated with the use of equation (5.4). For this a Taylor polynomial for the

bandgap voltage is defined as:

$$V_G(T) = V_G(T_r) + \alpha_1 \frac{dV_G(T)}{dT}\bigg|_{T=T_r} + \cdots \tag{5.6}$$

with α_m the Taylor coefficients. Substitution of equation (5.4) and equation (5.6) in the weighted sum of equation (5.5) and deriving the coefficients yields:

$$\begin{aligned}
\gamma_0 &= \sum_{m=1}^{i} a_m V_{BE_m}(T_r) \\
\gamma_1 &= \sum_{m=1}^{i} \frac{a_m}{T_r}\left[V_{BE_m}(T_r) - V_G(0)'\right] \\
\gamma_n &= \sum_{m=1}^{i} \frac{a_m}{T_r^n}\left[\alpha_n T_r^n - (\eta - \theta_m)\frac{(-1)^n}{n(n-1)}\right], \quad \forall n \geq 2
\end{aligned} \tag{5.7}$$

with $V_G(0)' = V_G(T_r) - \alpha_1 T_r + (kT_r/q)(\eta - \theta_m)$, called the extrapolated bandgap reference voltage. In these expressions, γ_0 represents the reference voltage whereas γ_n for $n > 1$ should be made zero depending on the order of compensation. From these expressions, it follows that for transistors biased at equal θs, their corresponding higher order terms are equal. Therefore, these are defined as:

$$\text{Higher order terms} = \sum_{n=2}^{\infty} B_n(\theta_m) \tag{5.8}$$

5.5.1. First-Order Compensation

In the previous section, general expression were given for the linear combination of base–emitter voltages. In this section, the theory is applied to a first-order compensated bandgap reference. At least two *different* base–emitter voltages are required [21]. It is assumed that they have equal θs. The reference voltage, V_{REF}, can be written as:

$$V_{REF} = a_1 V_{BE1}(T_r) + a_2 V_{BE2}(T_r) \tag{5.9}$$

With equations (5.5) and (5.7), the two scaling factors as a function of the base–emitter voltages can be found (assuming γ_1 is made zero for first-order

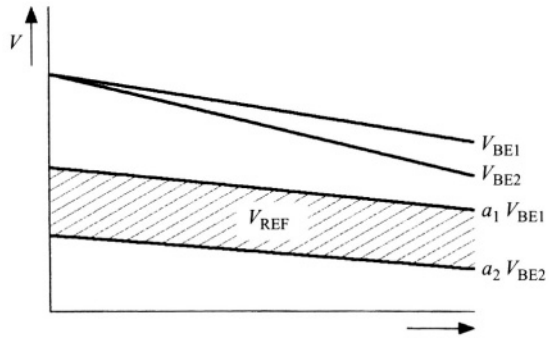


Figure 5.3. The principle of first-order compensation with two base–emitter voltages.

compensation):

$$a_1 = \frac{V_{REF}}{V_G(0)'} \cdot \frac{V_G(0)' - V_{BE2}(T_r)}{V_{BE1}(T_r) - V_{BE2}(T_r)}$$
$$a_2 = -\frac{V_{REF}}{V_G(0)'} \cdot \frac{V_G(0)' - V_{BE1}(T_r)}{V_{BE1}(T_r) - V_{BE2}(T_r)} \tag{5.10}$$

From these expressions, it follows that the two scaling factors have opposite signs. This is necessary for obtaining compensation, as the first-order temperature dependency of a base–emitter voltage is always negative. The principle is depicted in Figure 5.3. In the figure, the base–emitter voltages are approximated up to their first-order dependency.

The two scaling factors are chosen for the temperature compensation whereas the two base–emitter voltages are still free to choose. This can be used for instance for noise minimization, to be discussed later on. For more base–emitter voltages used in the linear combination, the same reasoning can be applied.

5.5.2. Second-Order Compensation

Again, two base–emitter voltages suffice for realizing a second-order compensation. However, the collector currents should have different temperature dependencies (θ) to be able to get a non-singular set of equations [21]. The reference voltage is given by:

$$V_{REF} = a_1 V_{BE1}(T_r) + a_2 V_{BE2}(T_r) \tag{5.11}$$

Solving the expressions for a second-order compensation, a ratio for the two scaling factors is found:

$$\frac{a_1}{a_2} = -\frac{B_2(\theta_2)}{B_2(\theta_1)} \tag{5.12}$$

where θ_1 and θ_2 correspond to V_{BE1} and V_{BE2}, respectively. For two given θs, the ratio of the two scaling factors is given. Thus: As *ratios depend on matching, the second-order compensation of the bandgap reference depends on the matching instead of on absolute values. A second-order compensation can be implemented relatively accurately.*

Introducing subsequently the constraint for the first-order compensation yields:

$$a_1 = \frac{V_{REF}}{V_{G2}(0)'} \cdot \frac{1}{V_{G1}(0)'/V_{G2}(0)' - B_2(\theta_1)/B_2(\theta_2)}$$
$$a_2 = -\frac{V_{REF}}{V_{G1}(0)'} \cdot \frac{1}{B_2(\theta_2)/B_2(\theta_1) - V_{G2}(0)'/V_{G1}(0)'} \tag{5.13}$$

in which $V_{G1}(0)'$ and $V_{G2}(0)'$ are the extrapolated bandgap voltages for θ_1 and θ_2, respectively. From these two expressions, it follows that a_1 and a_2 have, again, different signs and also a previous conclusion is found that two different θs have to be used otherwise the denominator of the last two expressions would become zero.

For the second-order compensated bandgap reference, the two scaling factors are completely determined by the compensation of the first and second-order temperature behavior. For other optimizations, these scaling factors can be treated as being constants. Also, for this case, the two base–emitter voltages are still free to choose.

The remaining temperature dependencies for a first and second-order compensated bandgap reference are depicted in Figure 5.4. In the figure, the

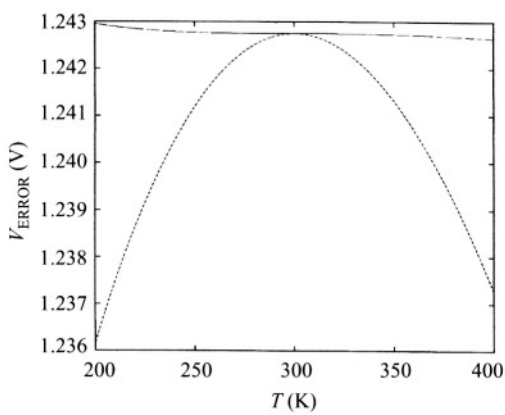


Figure 5.4. The remaining temperature dependency for a first-order (lower curve) and a second-order (upper curve) compensated bandgap reference with reference voltage equal to $V_G(0)'$.

expression of Varshni [22] is used for the bandgap voltage as a function of the temperature, which is also implemented in SPICE [23]:

$$V_G(T) = 1.1557 - \frac{7.021 \cdot 10^{-4} T^2}{T + 1108} \tag{5.14}$$

The figure clearly shows the mainly second-order temperature dependency of the output voltage of the first-order compensated bandgap reference and the third-order temperature dependency of the second-order compensated bandgap reference. Further, the error voltage of the second-order compensated bandgap reference is considerably smaller than the error voltage of the first-order compensated bandgap reference.

5.6. The Key Parameters

As may be clear from the previous sections, the design of bandgap references already concerns several parameters when only ideal physical models are used for the base–emitter voltages. For practical bandgap references, the models describing the behavior of the transistor introduce even more parameters. Therefore, it is good to know which parameters of the practical model dominate the behavior of the transistor in the case of bandgap reference design.

The Gummel and Poon model [24] as used in SPICE [23] is a well-known model and often used for circuit design. Therefore, this model is used here as the basis for the design of bandgap references. A minimum set of key parameters will be derived that describes the relation between the base–emitter voltage and the collector bias current.

The bulk resistors are not taken into account because it is possible to make their influence negligibly small, especially in the case of low-current design. The Gummel and Poon model is reduced further to the effects that are relevant for the forward-biased transistor. The leakage currents are ignored too, because in modern IC processes these leakage currents are negligibly small [25]. Further, it is assumed that the transistor is biased far from high-level injection. The relevant part of the Gummel and Poon model that remains is given by the following:

$$I_C(T) = I_S \cdot \exp\left[\left(\frac{T}{T_{nom}} - 1\right)\frac{E_G}{q V_T}\right] \cdot \left(\frac{T}{T_{nom}}\right)^{X_{TI}} \times \left[1 - \frac{V_{BC}}{V_{AF}} - \frac{V_{BE}}{V_{AR}}\right] \cdot \exp\left(\frac{V_{BE}}{N_F V_T}\right) \tag{5.15}$$

A further reduction is obtained when the transistor is biased such that $V_{BC} \approx 0\,V$. In that case the forward Early effect, modeled by V_{AF}, can be ignored. In contrast to V_{AR}, which is in the order of several volts, which cannot

be ignored. For a given temperature, V_T is known and T_{nom} is the temperature at which the parameters are extracted from measurements. Finally, N_F equals 1. Thus, for an accurate design of bandgap references, *four* parameters need to be known accurately, describing the relation between the base–emitter voltage and the collector current.

E_G (V_G)	the bandgap energy (voltage)
I_S	the saturation current
X_{TI}	order of the temperature dependency of I_S
V_{AR}	the reverse Early voltage

These parameters are the key parameters for bandgap reference design. When other models are used instead of the Gummel and Poon model, the corresponding parameters are found.

5.7. Temperature-Dependent Resistors

Besides the key parameters found in the previous section, one additional phenomenon has to be taken into account. This is the resistance by which the collector current is derived from a voltage. When this resistance is temperature dependent, it introduces an extra temperature dependency in the reference current.

Assume a collector bias current, I_C, is derived from a voltage, V, by a resistor, R, having a temperature-dependent relative error, as given by:

$$R(T) = R_0\left[1 + \alpha_1 T' + \alpha_2 T'^2\right] \tag{5.16}$$

where $T' = T - T_0$, R_0 is the resistance at the nominal temperature T_0 and α_1, α_2 are the first and second-order temperature dependencies of the resistor, respectively. Then, for the collector current, the following expression can be found:

$$I_C(T) = \frac{V(T)}{R_0}\left[1 - \alpha_1 T' + \left(\alpha_1^2 - \alpha_2\right) T'^2 + O(T'^3)\right] \tag{5.17}$$

in which V may be temperature dependent. Then, for the error in the base–emitter voltage, ΔV_{BE} the following expression can be found:

$$\begin{aligned}\Delta V_{BE} &= V_{BE}(T, \alpha_1, \alpha_2) - V_{BE}(T, \alpha_1 = 0, \alpha_2 = 0) \\ &= \frac{kT_0}{q}\left[-\alpha_1 T' + \left(\frac{1}{2}\alpha_1^2 - \alpha_2 - \frac{\alpha_1}{T_0}\right) T'^2 + O(T'^3)\right] \\ &= \frac{kT_0}{q}\left[\gamma_1 T' + \gamma_2 T'^2 + O(T'^3)\right]\end{aligned} \tag{5.18}$$

Table 5.1. The resulting *relative* error at the output of a bandgap reference due to the temperature dependency of resistors. Diffused: $\alpha_1 = 1.7\text{E}{-3}/°\text{C}, \alpha_2 = 5.4\text{E}{-6}/°\text{C}^2$. NiCr: $\alpha_1 = 5\text{E}{-5}/°\text{C}$, $\alpha_2 = 0/°\text{C}^2$ [26]; $(kT_0/q)/V_G(0)' = 0.026/1.2$.

Resistor type	$(kT_0/qV_G(0)')\gamma_1$ (/°C)	$(kT_0/qV_G(0)')\gamma_2$ (/°C^2)
Diffused	−37E−6	−0.2E−6
Thin-film NiCr	−1.1E−6	−3.6E−9

Thus, a relative error in the resistor causes an additive error in the base–emitter voltage (which is a consequent of the logarithm). The error is independent of the value or temperature dependency of the collector current. Recalling that a bandgap reference is a linear combination of base–emitter voltages, the resulting error at the output of the bandgap reference source can be found. This error voltage, V_{ERROR}, is found from:

$$V_{\text{ERROR}} = \sum_{m=1}^{i} a_m \Delta V_{\text{BE}_m} = \Delta V_{\text{BE}_m} \sum_{m=1}^{i} a_m$$
$$= \frac{V_{\text{REF}}}{V_G(0)'} \cdot \frac{kT_0}{q} \left[\gamma_1 T' + \gamma_2 T'^2 + O(T'^3)\right] \qquad (5.19)$$

for which are used the constraints for temperature compensation and the assumption that the influence of the different θs on the error can be ignored. This results in

$$\sum_{m=1}^{n} a_m = \frac{V_{\text{REF}}}{V_G(0)'}$$

The final error depends on the type of resistors being used. In Table 5.1, examples are given for a diffused resistor and a thin-film NiCr-resistor. The second-order error resulting from the temperature behavior of the diffused resistor is about a factor 4 lower than the second-order behavior of the intrinsic base–emitter voltage. Therefore, when designing second-order (or higher) compensated bandgap references, this effect has to be taken into account. Adding the corresponding term to the term describing the second-order behavior of the base–emitter voltage can do this.

5.8. Noise

As the accuracy and temperature independence of bandgap references increase, the mean errors will now become in the order of a few ppm/K over a temperature range of 100K. Consequently, the noise performance of bandgap

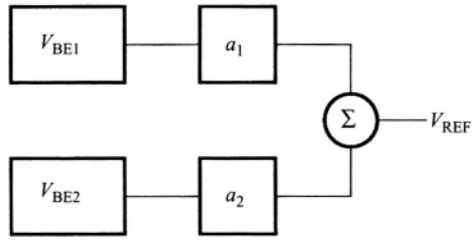


Figure 5.5. A general block diagram of a first and second-order compensated bandgap reference derived from two base–emitter voltages.

references becomes more and more important. For instance: assume a bandgap reference with an output voltage of 200 mV and a mean temperature dependency of 2 ppm/K. The mean uncertainty due to the temperature dependency then equals only $0.4\,\mu V/K$. When the equivalent noise voltage at the output is higher than this value, the noise is the dominant cause of the uncertainty. This example concerns relatively low-frequency noise. In the context of delta–sigma modulators, the relatively high-frequency noise of the bandgap reference is also important. Since the modulators sample at a relatively high rate, the noise is important over a larger bandwidth.

To be able to minimize the noise level of the bandgap reference, all the noise sources in the bandgap reference are transformed to the output. For a first and second-order compensated bandgap reference a minimum of only two base–emitter voltages are required. The general block diagram of those bandgap references can therefore be visualized as depicted in Figure 5.5.

Three types of blocks can be identified:

- base–emitter voltage generator
- sealer
- summing node.

Of these three types of blocks, the base–emitter voltage generators are the core of the bandgap reference. They realize the required relation to the bandgap voltage. Here the noise minimization is only discussed for the V_{BE} generators. For the other blocks, equivalent minimizations can be done.

In Figure 5.6, an ideal base–emitter voltage generator is depicted. The desired collector current, I_C, is forced into the collector by means of negative feedback. The nullor controls the base–emitter voltage such that the desired current flows into the collector. As the input current of the nullor is zero, the complete current flows into the collector, and an accurate relation is found between V_{BE} and I_C. Further, as the input voltage of the nullor is zero, the

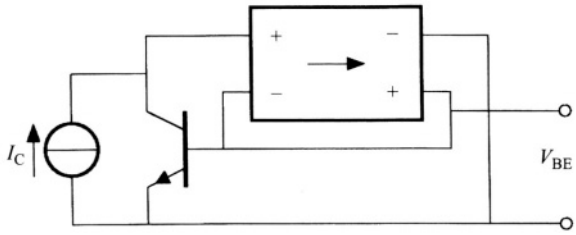


Figure 5.6. An ideal base–emitter voltage generator.

forward Early voltage can be ignored. This cell is the core of the idealized bandgap reference and is used to calculate the minimum noise level.

5.8.1. Noise of the Idealized Bandgap Reference

To find the noise performance of a single cell, the noise of the transistor has to be transformed to an equivalent source at the output of the base–emitter voltage generator. The transistor noise sources are depicted in Figure 5.7.

Three noise sources can be distinguished [27]:

- collector shot noise, $S_{I_C} = 2qI_C$
- base shot noise, $S_{I_B} = 2qI_B$
- thermal noise of the base resistance, $S_{r_b} = 4kTr_b$.

The $1/f$ noise is ignored as for modern (bipolar) processes the noise corner can be relatively low. For the noise-power density spectrum of the equivalent noise voltage, $S_{v_{eq}}$, see Figure 5.7, holds [27]:

$$S_{v_{eq}} = 4kT\left\{\frac{1}{2}r_e\left[1+\left(\frac{r_b}{r_e}\right)^2\frac{1}{\beta_f}\right]+r_b\right\} \tag{5.19}$$

where β_f is the small-signal forward current-gain factor and r_e equals kT/qI_C. The equivalent noise current does not influence the noise behavior as this source is shorted by the nullor output. Simplifications can be made for the equivalent noise voltage. When the base resistance is made considerably smaller than r_e, it can be ignored for the noise performance and the equivalent noise source can then be written as:

$$S_{v_{eq}} = 2kTr_e \tag{5.20}$$

For low-current applications, r_b is very often already much smaller than r_e. For the relatively high-current applications, for minimum noise level r_b must be made small by dedicated transistors design, that is, more and larger base-contacts.

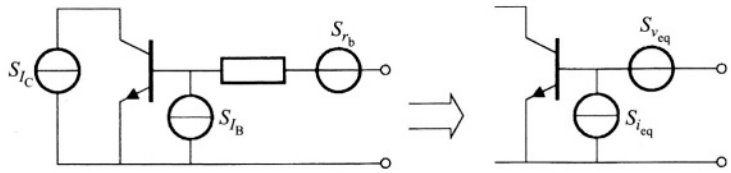


Figure 5.7. The noise sources of a bipolar transistor which are transformed to equivalent noise sources at the output of the cell.

Using this equivalent noise source for both V_{BE} generators in Figure 5.6, yields for the total noise-power density spectrum at the output of the bandgap reference, $S_{v_{out}}$:

$$S_{v_{out}} = 2kT\left(a_1^2 r_{e1} + a_2^2 r_{e2}\right) \tag{5.21}$$

where a_1, a_2 and r_{e1}, r_{e2} are the corresponding parameters for base–emitter voltages one and two, respectively. This equation describes the noise at the output of the first-order compensated bandgap reference as well as the noise at the output of the second-order compensated bandgap reference. In the following sections, this equation will be used when discussing the noise for a first and second-order compensated bandgap references.

5.8.2. Noise of a First-Order Compensated Reference

In Section 5.5.1, the scaling factors for a first-order compensated bandgap reference were derived. When these are substituted into expression (5.21) the following expression is found for the noise-power density:

$$S_{\text{out_second}} = 2qV_T^2\left(\frac{a_1^2}{I_{C1}} + \frac{a_2^2}{I_{MAX} - I_{C1}}\right)$$

in which $I_{MAX} = I_{C1} + I_{C2}$ and $x = I_{C1}/I_{MAX}$. In the numerator, I_{MAX} only appears in the log functions whereas the denominator is proportional to I_{MAX}. So the noise level is approximately inversely proportional to I_{MAX}. The minimum noise level corresponds with an optimum ratio $y = I_{C1}/I_{C2}$ that can be found from the (approximated) implicit equation:

$$\ln\left(y\frac{I_{S2}}{I_{S1}}\right) = -2\frac{1+y}{1-y} \tag{5.22}$$

Clearly, only the ratio of the two bias currents and the ratio of the two saturation currents appear in the expression. This minimum is independent of the reference voltage. As an example, Table 5.2 shows the optimum ratio for two cases.

Table 5.2. The optimum ratio of collector currents (y) for a given ratio of saturation currents and the corresponding minimum noise level.

I_{S1}/I_{S2}	y_{opt} *approximated*	y_{opt} *exact*	$\overline{v_n}$ (nV/$\sqrt{Hz}$) *approximated*	$\overline{v_n}$ (nV/$\sqrt{Hz}$) *exact*
1	*10.99*	*11.36*	*79.5*	*79.5*
10	*3.55*	*3.45*	*39.0*	*39.0*

Thus, for each ratio of saturation currents an optimum ratio y follows. The requirements for the saturation currents can be derived straightforwardly [21]. Then, for a first-order compensated bandgap reference based on two base–emitter voltages, the following rules are found for the minimum noise level: the ratio of the two collector currents; $y = I_{C1}/I_{C2}$, follows from:

$$\ln\left(y\frac{I_{S2}}{I_{S1}}\right) = -2\frac{1+y}{1-y}$$

the noise level is inversely proportional to $I_{C1} + I_{C2}$; the ratio I_{S1}/I_{S2} should be as large as possible for $I_{C1}/I_{C2} < 1$ and vice versa; $I_{S1} + I_{S2}$ should be as small as possible.

5.8.3. Noise of a Second-Order Compensated Reference

For the noise performance of second-order compensated bandgap references based on two base–emitter voltages, the corresponding expressions equation (5.13) for the scaling factors have to be used in equation (5.21). As these scaling factors are already completely determined by the first and second-order temperature compensation, they are constants for the noise minimization. The equation for the noise minimization is given by:

$$S_{out_second} = 2qV_T^2\left(\frac{a_1^2}{I_{C1}} + \frac{a_2^2}{I_{MAX} - I_{C1}}\right) \tag{5.23}$$

The noise-power density is minimal for:

$$\frac{I_{C1}}{I_{C2}} = -\frac{a_1}{a_2} = \frac{B_2(\theta_2)}{B_2(\theta_1)} \tag{5.24}$$

The two corresponding collector currents are given by:

$$\begin{aligned} I_{C1} &= \frac{a_1}{a_1 - a_2} I_{MAX} \\ I_{C2} &= \frac{-a_2}{a_1 - a_2} I_{MAX} \end{aligned} \tag{5.25}$$

Substitution of the expressions for a_1 and a_2, in expression (5.23) yields:

$$S_{\text{out_second}} = 2qV_T^2 \left(\frac{V_{\text{REF}}}{V_G(0)'}\right)^2 \cdot \left(\frac{B_2(\theta_1) + B_2(\theta_2)}{B_2(\theta_1) - B_2(\theta_2)}\right)^2$$
$$= V_{\text{REF}}^2 \cdot \frac{\text{CONSTANT}}{I_{\text{MAX}}} \tag{5.26}$$

in which it is assumed that $V_{G1}(0)' = V_{G2}(0)' = V_G(0)'$, resulting in a negligibly small error. From this expression, some remarkable conclusions can be drawn: the noise-power density of a second-order compensated bandgap reference, based on two V_{BE}s, with a given reference voltage can only be influenced by the designer by means of the current consumption; it is inversely proportional to the total current consumption; for a given current consumption, the "signal-to-noise ratio" is independent of the reference voltage; the size of the transistors used, does not influence the noise level.

Substituting the constants and choosing for the θs 0 and 1, the equivalent noise voltage is given by (assuming a white noise spectrum):

$$\overline{v_{\text{eq}}} = V_{\text{REF}} \cdot 10^{-10} \sqrt{\frac{B}{I_{\text{MAX}}}} \tag{5.27}$$

From this expression, the minimum current consumption can easily be found for a given reference voltage and a required noise level.

Example: Assume a second-order compensated bandgap reference with an output voltage equal to 1 V is required of which the noise voltage is at most $1\,\mu\text{V}/\sqrt{\text{Hz}}$. From expression (5.27), a minimum current consumption of $1\,\mu\text{A}$ is found.

It should be noted that this is the minimum noise level of the idealized bandgap reference, that is, sealer and summing node still ideal. So, the noise level found is a lower bound.

5.8.4. Power-Supply Rejection

In this section, the influence of the current sources in the base–emitter voltage generators are considered (Figure 5.6). As a result of the finite output impedance for practical current sources, additional noise will appear at the output of the bandgap reference.

Assume a bandgap reference based on n base–emitter voltages as given in Figure 5.8. The nullor realizes a zero impedance at the collector node, in order to make the bias currents completely flow into the collector lead. Therefore, for a disturbance, v_{dis}, on the supply voltage, the currents injected into the

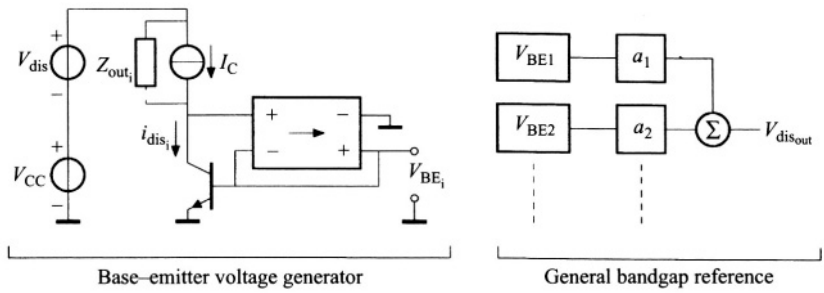


Figure 5.8. An idealized bandgap reference with non-ideal current sources.

collectors of the reference transistors, i_{dis_i} equal:

$$i_{dis_i} = \frac{v_{dis}}{Z_{out_i}} \tag{5.28}$$

where Z_{out_i} is the output impedance of the corresponding current source. The low-frequency output impedance of the current sources, r_{out_i} is given by:

$$r_{out_i} = \frac{V_{AF_i}}{I_{C_i}} \tag{5.29}$$

It may be assumed that the forward Early voltages are equal for the current sources. The resulting disturbance on the base–emitter voltage is related to i_{dis_i} via $1/g_m$. Then, the disturbances found at the output of the bandgap reference amount to:

$$v_{dis_{out}} = \sum_{i=1}^{n} a_i \frac{v_{dis}}{g_{m_i} V_{AF_i}/I_{C_i}} = v_{dis} \frac{V_T}{V_{AF}} \sum_{i=1}^{n} a_m = v_{dis} \frac{V_T}{V_{AF}} \frac{V_{REF}}{V_G(0)'} \tag{5.30}$$

where V_T is the thermal voltage. A commonly used figure of merit is the power-supply rejection ratio (PSRR); it is a measure of how good the isolation is between the power-supply voltage and the circuit output. For the bandgap reference, the PSRR is given by:

$$\text{PSRR} = 20 \log \left[\frac{V_T}{V_{AF}} \frac{V_{REF}}{V_G(0)'} \right] \tag{5.31}$$

Example: $V_T = 25\,\text{mV}$, $V_{AF} = 50\,\text{V}$, $V_{REF} = 0.2\,\text{V}$ and $V_G(0)' = 1.2\,\text{V}$. The PSRR of the bandgap reference is then −82 dB.

For this derivation of the PSRR it was assumed that the current sources are equal; in this case they did not have any series feedback. When series feedback is applied, the PSRR improves as the output impedances of the current sources

increase. When it is possible to realize the output impedances such that the injected disturbances of the current sources cancel at the output, a very high PSRR can be achieved. Of course, the ratio of the output impedances becomes very important and this may be too tough a job to reach the desired matching. The required measures, however, can be taken independently of the other design consideration as discussed in the previous section.

5.9. Simplified Structures

Special cases of bandgap references can be found. These arise, for instance, when the circuits are reduced to having only one scaling factor. In the next section, a special case a first-order and a second-order compensated bandgap reference is discussed.

5.9.1. First-Order Compensated Reference

When for a first-order compensated bandgap reference the reference voltage is chosen to be $V_G(0)'$, the sum of the two scaling factors becomes one (easily derived from equation (5.10)). Or, in other words, the two scaling factors differ by one. As a result, a simplification of the circuit can be made, see Figure 5.9.

The bandgap reference as proposed by Brokaw [28] is found. As a result of the topology, the scaling factors always differ by one. A first-order compensation is inherently realized when the output voltage is $V_G(0)'$. When, as a result of component spread, the reference needs trimming, tuning a bias current or the scaling factor at one temperature such that the output voltage becomes $V_G(0)'$, is sufficient. However, when non-idealities introduce some additional first-order temperature dependencies, the value to which the reference voltage must be tuned in order to obtain first-order compensation changes.

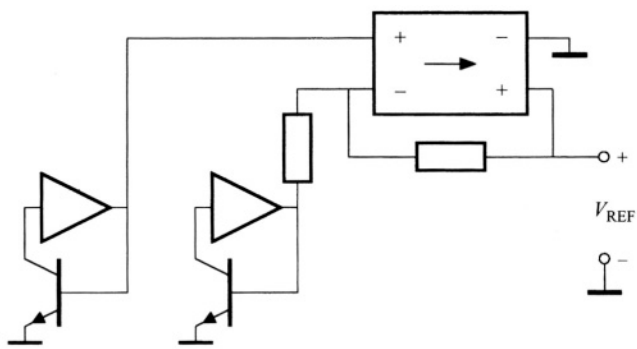


Figure 5.9. The first-order compensated bandgap reference with output voltage equal to $V_G(0)'$.

5.9.2. Second-Order Compensated Reference

For a second-order compensated bandgap reference, a special structure can be obtained in the following way. Consider the bandgap reference as depicted in Figure 5.10.

In this structure, scaling factor a_1 is shifted through the summing node (see Figure 5.10(b)). The output voltage of the reference is still the original value. As the scaling factors are assumed to be temperature independent, the input voltage of sealer a_1 in Figure 5.10(b), is also temperature independent. Therefore, assuming a_1 to be one, only one scaling factor remains and still a temperature compensated reference voltage is obtained, see Figure 5.10(c). As, however, one degree of freedom is used by assuming a_1 to be one, the reference voltage can no longer be chosen freely.

In Figure 5.10, a_1 is shifted through the summing node, as this is the positive scaling factor. Shifting a_2 through the summing node and assuming it to be one, results in a negative reference voltage; to obtain a positive reference voltage $|a_2|$ has to be shifted through the summing node.

The reference voltage that is found when a_1 is assumed to be one follows directly from equation (5.13), yielding:

$$V_{REF} = V_{G1}(0)' - V_{G2}(0)' \cdot \frac{B_2(\theta_1)}{B_2(\theta_2)} \tag{5.32}$$

This reference voltage is determined by the two θs and process parameters only. For the θs being 1 and 0, and the model of Varshni for the bandgap energy [22], the following reference voltage is found:

$$V_{REF} = 245\,\text{mV} \tag{5.33}$$

The remaining scaling factor, a_2, completely determines the second-order compensation (the output voltage of the reference with $a_2 = 1$ equals –312 mV). As a_2 can be realized by a ratio of components, a_2 can be accurately realized on a chip. Thus, second-order compensation is readily achieved. Subsequently, to obtain the first-order compensation, the output voltage only has to be made 245 mV. Thus, in the case of an unacceptable spread on the

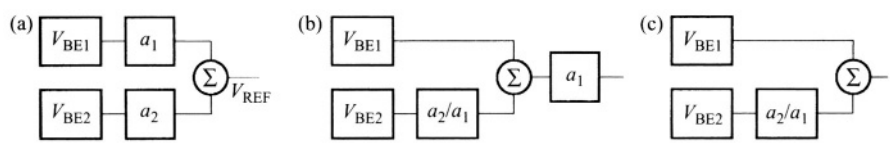


Figure 5.10. Simplification of a second-order compensated bandgap reference.

component values, trimming at only one temperature is sufficient for obtaining a second-order compensated reference voltage.

5.10. Design Example

In this section, two example designs are discussed. Section 5.10.1 describes a first-order compensated bandgap reference with the focus on noise minimization, whereas a second-order compensated bandgap reference with focus on temperature compensation is described in Section 5.10.2.

5.10.1. First-Order Compensated Bandgap Reference

In this section, an overview of the design of a first-order compensated bandgap reference is described. More details about this design can be found in [29]. The bandgap reference has an output voltage of about 200 mV and the power-supply voltage is 1 V, whereas the current consumption is about $5\,\mu A$. As a direct result of the first-order temperature compensation, the mean temperature dependency of the output voltage is about 20 ppm/K over the range of 0–100°C with mainly a quadratic behavior, see Figure 5.4.

For this design, noise minimization was the key issue. The basic structure chosen for the bandgap reference is a linear combination of two base–emitter voltages with scaling factor a_2 equal to one. This is analogous to the simplification as discussed for the second-order compensated bandgap reference; see Section 5.9.2 and Figure 5.10. As for the first-order compensated bandgap reference, one degree of freedom less is used compared with the situation for the second-order compensated bandgap reference, the reference voltage can still be chosen freely.

An implementation of the basic structure is depicted in Figure 5.11. In this figure, two base–emitter voltage generators can be distinguished and one voltage amplifier. The size of transistors Q_{ref1} and Q_{ref2} were chosen as 1:10.

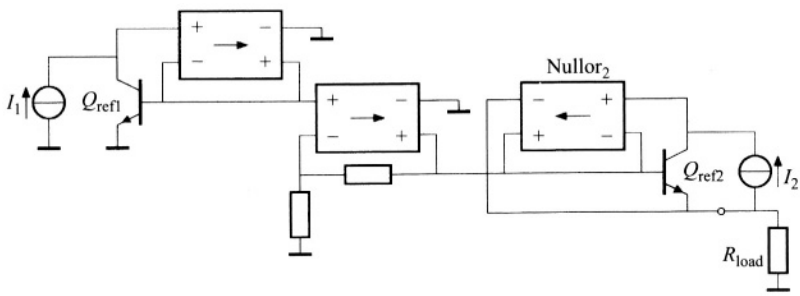


Figure 5.11. Implementation of the bandgap reference at nullor level.

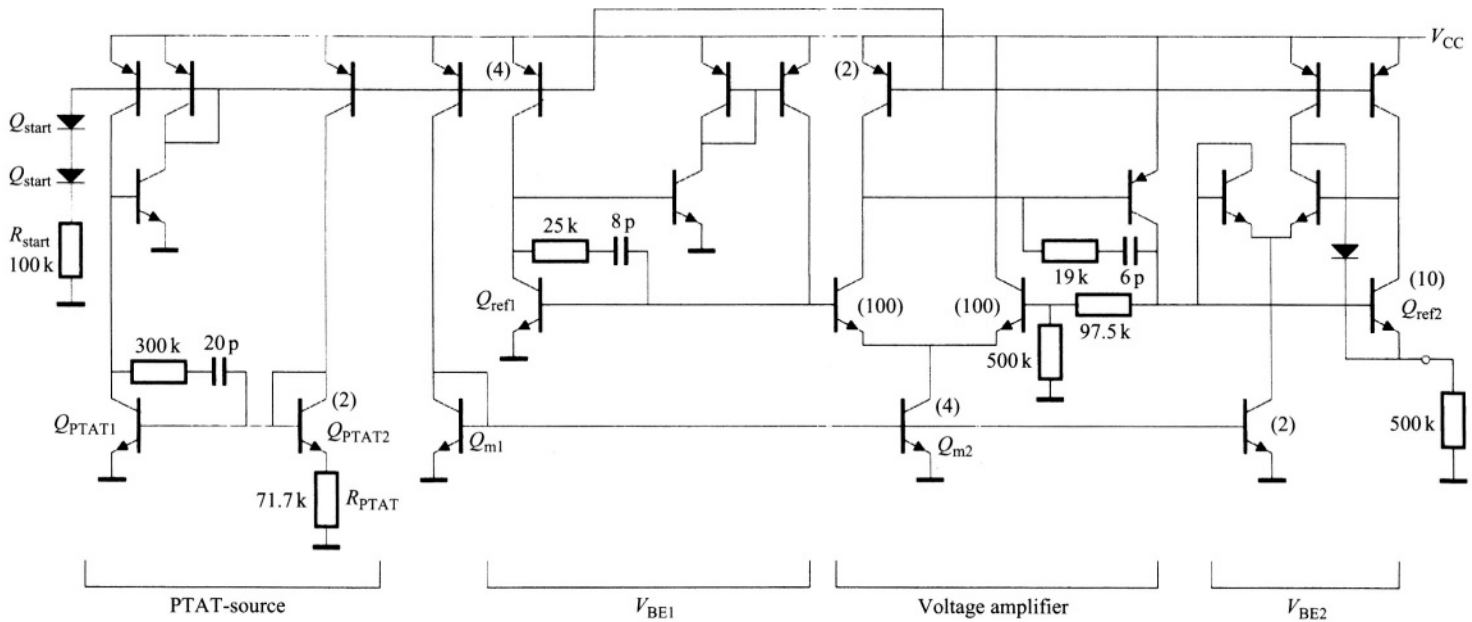


Figure 5.12. The total circuit of the bandgap reference.

This yields an optimal current ratio of 1:0.28. Currents were chosen $I_{C1} = 1\,\mu A$ and $I_{C2} = 0.25\,\mu A$. The actual ratio was chosen somewhat besides the optimum to get a convenient scaling ratio for the currents. As the noise optimum is relatively flat, the influence on the noise is negligible.

Figure 5.12 shows the circuit when the nullors and the biasing circuitry are implemented.

The bias currents for the transistors implementing the nullors were mainly chosen on noise constraints and output capabilities of the nullor implementations. The resistors setting the gain of the voltage amplifier are chosen to be relatively large, that is, $500\,k\Omega$ and about $100\,k\Omega$. Then the noise contribution and the current consumption can be kept at the same order of magnitude as they are for the base–emitter voltage generators. The bias currents were derived from a PTAT source realizing a current of $0.25\,\mu A$. A summary of the noise contributions of the sub-blocks of the bandgap reference is given in Table 5.3.

A striking fact from this table is the relative large contribution of the noise of the biasing. This is mainly a result of the number of mirror actions for deriving the bias currents. Using emitter resistors in the mirrors can reduce this noise contribution. For a voltage of about 100mV across these resistors, the noise power of the biasing can be reduced to about 5% of the original level [30]. Further, for reducing the noise of the PTAT source used, the basic PTAT voltage in the source should be enlarged.

5.10.2. Second-Order Compensated Bandgap Reference

This section summarizes the design of a second-order compensated bandgap reference. For this reference, the goal was to show the feasibility of reaching high-performance references with a linear combination of base–emitter voltages. Details of this design can be found in [31]. The bandgap reference realized showed a mean temperature dependency of only 1.5ppm/K over a temperature range of 0–100°C. The output voltage was about 200 mV. The power-supply voltage was only 1 V and the current consumption about $100\,\mu A$.

Table 5.3. The noise contribution of the sub-blocks of the first-order compensated bandgap reference.

Part	*Contribution* ($nV/\sqrt{Hz}$)
V_{BE1} *generator*	*15*
V_{BE2} *generator*	*30*
Voltage amplifier	*54*
Biasing circuit	*153*
Total	*166*

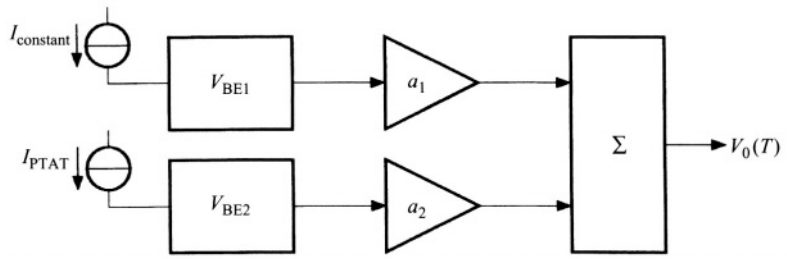


Figure 5.13. A linear combination of two base–emitter voltages with two collector currents having different temperature behavior.

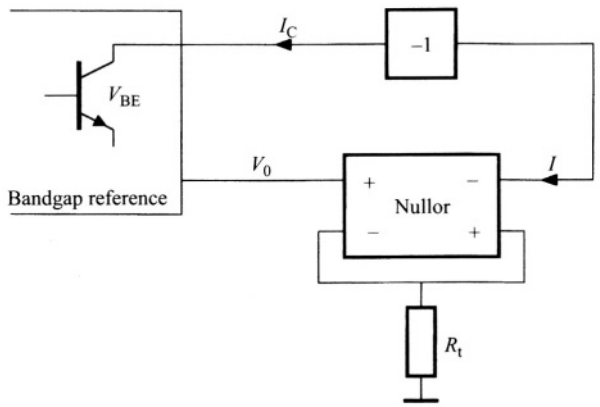


Figure 5.14. Bias loop for biasing transistor 2 with a constant current.

The basic structure for the reference is depicted in Figure 5.13. This reference requires two different temperature behaviors for the collector currents. One was chosen to FIAT. This one is easy to derive from a PTAT source. The other collector current was chosen to be constant. This current could be approximated very well from the output voltage of the reference by means of a transconductance amplifier, see Figure 5.14.

The resulting loop has one bias point, which is stable, corresponding to the desired one. In this design, resistive dividers realized the scaling factors. The ratios were mainly chosen on low-voltage considerations. This can be explained with the help of Figure 5.15 showing the basic structure implementing the summing node and scaling factors.

The input voltage of both resistive dividers is a base–emitter voltage. Consequently, the minus input of the nullor has a voltage, which is equal to a fraction of a base–emitter voltage. To be able to implement an input stage for

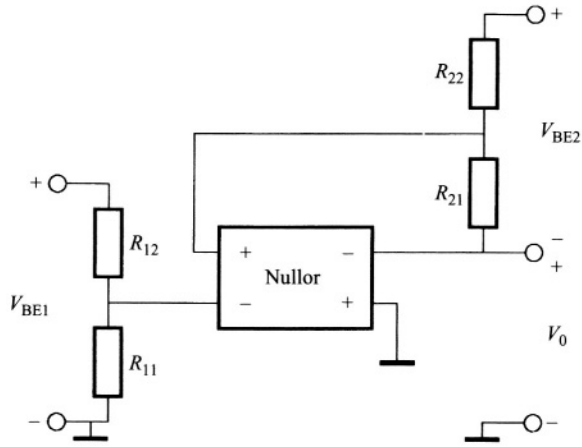


Figure 5.15. The combiner implementing the summing node and the scaling factors.

this nullor, this voltage should not be too low. The scaling factors were chosen approximately 0.8 and 0.6, respectively. When the base–emitter voltage generators are again implemented according to Figure 5.6, the circuit diagram of Figure 5.16 (on the next page) is obtained.

In this circuit diagram the two base–emitter voltage generators can be recognized, the resistive dividers implementing the scaling factors, the summing node, the transconductance amplifier for the constant current and the PTAT source for the PTAT current. The supply voltage, V_{CC}, is 1 V.

Measurement results of this bandgap reference are shown in Figure 5.17. The mean temperature dependency is about 1.5ppm/K. From calculations on the idealized bandgap reference, a minimum temperature dependency of 0.22 ppm/K can be found for this temperature range. This remaining dependency is a result of the non-compensated third and higher order temperature dependencies of the base–emitter voltage. However, to reach this, the influence of the remaining of the implementation must be negligibly small. The cause of the deviation for this design is twofold. First, for the lower temperatures the voltage available for the tail-current source of the differential pair in the combiner becomes too low. Consequently, saturation of this source occurs and an error voltage results. Second, at the higher end of the temperature range, the deviation is mainly caused by the influence of leakage currents. At about 125°C, a sharp drop in the reference voltage was found (on the order of several mV over a range of 10°C), its influence is already noticeable at 100°C, Figure 5.17.

The noise performance was not optimized for the reference. For the bias currents of the two reference transistors, a large ratio was chosen as this was

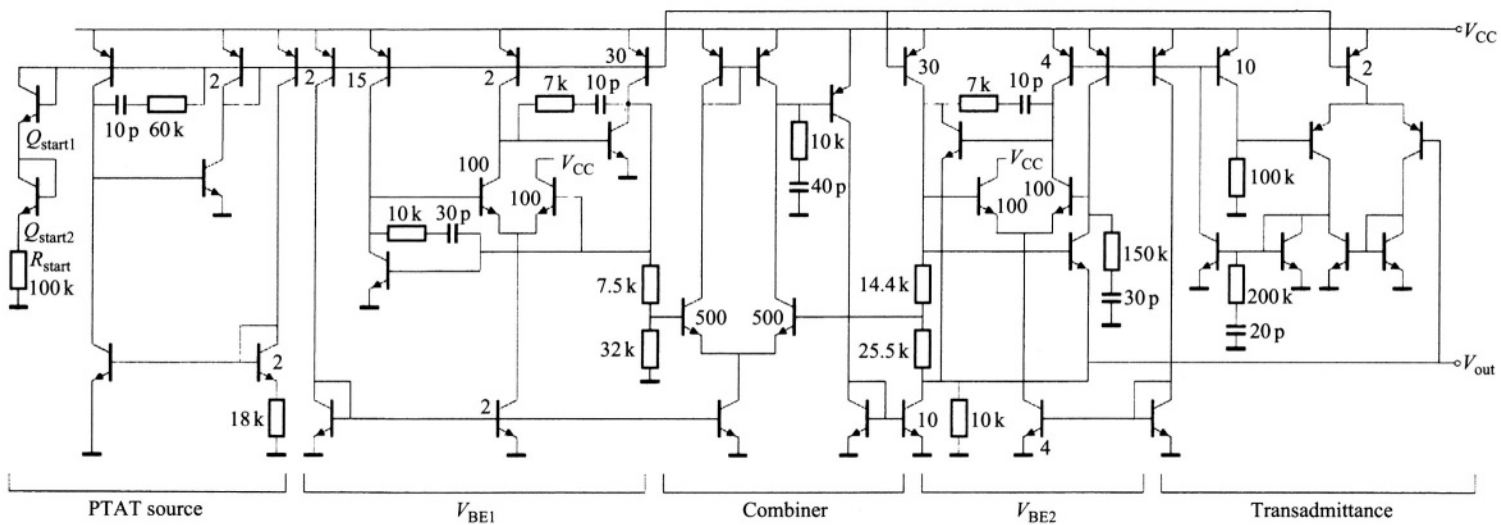


Figure 5.16. The total circuit diagram of the second-order compensated reference.

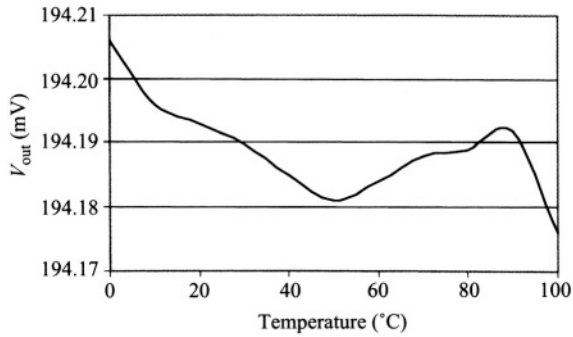


Figure 5.17. The measured output voltage as a function of temperature.

assumed to be a correct (logic) choice. The total equivalent noise production of the associated idealized bandgap reference amounts to about $20\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. One reference transistor was biased at $\approx 15\,\mu\mathrm{A}$ whereas the other was biased at $\approx 0.2\,\mu\mathrm{A}$. However, from noise minimization, see Section 5.8.3, it is found that for optimum noise performance, the current ratio of these two currents should be the same as the ratio of the two scaling factors (which equals about 0.75 and thus differs considerably from the used collector current ratio). When the optimum ratio for the collector currents is used, equation (5.27) applies and the minimum noise level for the same total current of $15.2\,\mu\mathrm{A}$ is found to be $5.1\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$; about a factor 4 better. As the noise contribution of the biasing is a relative contribution, the expected noise of the complete optimized bandgap reference, for the same power consumption is about $20\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ (from Table 5.3 a ratio of 4 is found between the noise of the idealized bandgap reference and the noise of the total bandgap reference). This is a factor 4 lower compared with the noise voltage production of the realized reference!

5.11. Conclusions

In this chapter, a structured design method for bandgap references has been presented. The bandgap reference was described in terms of a linear combination of base–emitter voltages. This linear combination was described using the Taylor series of the base–emitter voltages. Subsequently, the scaling factors for obtaining a first and second-order compensated bandgap reference were derived. For both cases, two different base–emitter voltages showed to be sufficient. On top of that, for compensating second-order temperature dependencies, the temperature behavior of the two collector currents should also be different.

From the Gummel and Poon model, it was derived that only four key parameters are dominant in the behavior of the bandgap reference: the bandgap

energy, E_G, the saturation current of the base–emitter junction, I_S, including its order of temperature dependency, XTI and the reverse Early voltage, V_{AR}.

For the design of the noise behavior of the bandgap references, in this chapter, the idealized bandgap reference was studied (i.e. assuming that only the base–emitter voltages of the reference devices introduce noise). This results in an expression giving a lower bound for the noise performance of a bandgap reference consuming a certain current.

For the first-order compensated idealized bandgap reference, realized with the minimum of two base–emitter voltages, it was found that for a minimum noise level an optimum ratio of the two collector currents exists which only depends on the ratio of the two saturation currents.

For the second-order compensated bandgap reference, also realized with the minimum number of two base–emitter voltages, the minimum noise level is found for a collector-current ratio which only depends on the second-order temperature dependencies of the base–emitter voltages. The noise level appeared to depend on a constant with only process parameters and the current consumption. Further, for a given current consumption, the "signal-to-noise ratio" of a second-order compensated idealized bandgap reference is fixed, that is, it is independent of the reference voltage.

For the PSRR, an expression was derived giving the maximum attainable PSRR in terms of transistor parameters. This expression showed that the PSRR is independent of the topology and can only be improved by increasing the output impedances of the current sources or by choosing a specific ratio for these output impedances such that cancellation takes place.

From the general description of the bandgap reference, specific structures were derived by choosing the scaling factor such that the references could be implemented with only one scaling factor. For both, first and second-order compensated references, this results in structures with inherent temperature compensation when the output voltage has its nominal value.

Finally, two design examples were discussed. One concerning a first-order compensated bandgap reference, in which noise minimization was the key item and one concerning the design of a second-order compensated bandgap reference, for which the temperature compensation by means of the linear combination of base–emitter voltages was the main topic. The second-order compensated bandgap reference described showed from measurements a temperature dependency of only 150 ppm over a temperature range of 100 K and is supplied from a power supply of only 1V.

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Chapter 6

GENERALIZED FEEDBACK CIRCUIT ANALYSIS

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6.1. Introduction

Feedback, whether intentionally incorporated or parasitically incurred, pervades all electronic circuits and systems. A circuit is a feedback network if it incorporates at least one subcircuit that allows a circuit branch current or branch voltage to modify an input signal variable in such a way as to achieve a network response that can differ dramatically from the input/output (I/O) relationship observed in the absence of the subcircuit. In general, the subcircuit that produces feedback in the network, as well as the network without the feedback subcircuit, can be nonlinear and/or time variant. Moreover, the subcircuit and the network in which it is embedded can process their input currents or voltages either digitally or in an analog manner. In the discussion that follows, however, only linear, time-invariant analog networks and feedback subcircuits are addressed.

There are two fundamental types of feedback circuits and systems. In a positive, or regenerative feedback network, the amplitude and phase of the fed back signal, which is effectively the output response of the feedback subcircuit, combine to produce an overall system response that may not be bounded even when the input excitation to the overall system is constrained. Although regenerative feedback may produce unbounded, and hence unstable, responses for bounded input currents or voltages, regeneration is not synonymous with instability. For example, regenerative amplifiers have been designed to deliver reproducible I/O voltage gains that are much larger than the gains achievable in the absence of positive feedback [1,2]. In another application of regeneration, high-frequency compensation has been incorporated to broadband the frequency response of bipolar differential amplifiers that are otherwise band limited [3]. The most useful utility of positive feedback is electronic oscillators [4], while the most troubling ramification of positive feedback derives from the parasitic capacitances and inductances indigenous to high-performance analog integrated circuits. These elements interact with on chip active elements to produce severely underdamped or outright unstable circuit responses [5].

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The companion to positive feedback is negative or degenerative feedback, which is the most common form of intentionally invoked feedback architecture in linear signal processing applications. Among the most important of these applications are amplifiers [6] for which degeneration serves at least four purposes. First, negative feedback desensitizes the gain of an open loop amplifier (an amplifier implemented without feedback) with respect to uncertainties in the model parameters of passive elements and active devices. This desensitization property is crucial in view of open loop parametric uncertainties caused by modeling approximations, temperature variations, biasing perturbations, and non-zero fabrication and manufacturing tolerances. Second, and principally because of the foregoing desensitization property, degenerative feedback reduces the dependence of circuit response on the parameters of inherently nonlinear active devices, thereby improving the linearity otherwise attainable in open loops. Third, negative feedback displaying non-zero feedback at zero signal frequencies broadbands the dominant pole of an open loop amplifier, which conduces at least the possibility of a closed loop network with improved high-frequency response. Finally, by modifying the driving point input and output impedances of the open loop circuit, negative feedback provides a convenient vehicle for implementing voltage buffers, current buffers [7] and circuits that effect impedance transformation [8]. Other applications of negative feedback include active RC filters [9,10], phase-locked loops [11], and a host of compensation circuits that offset common mode biasing difficulties [12], circumvent the deleterious effects of dense poles in open loop amplifiers [13,14], and allow for low power biasing of submicron CMOS devices used in low voltage circuit and system applications [15].

Despite Bode's pathfinding disclosures [16], which framed a mathematically elegant and rigorous strategy for investigating generalized feedback architectures, most analog circuit designers still perceive feedback circuit analysis and design as daunting tasks. Their perceptions doubtlessly derive from traditional literature which often simplifies feedback issues through such approximations as dominant pole open loops, global feedback (feedback applied only between the output and input ports of a considered structure), frequency-invariant feedback, and feedback subcircuits that presumably conduct signals only unilaterally, in a direction opposite to the flow of signals through the open loop. While these and other commonly invoked assumptions are generally acceptable in relatively low-frequency signal processors, their validity is dubious in broadband and/or low-voltage/low-power analog circuits. In such applications, second-order effects – non-dominant open loop poles and zeros, energy storage associated with on-chip interconnects and packaging, complex models necessitated by device scaling requirements, etc. – often surface as significant phenomenology whose tacit neglect precludes an insightful understanding of feedback dynamics.

The objective of this chapter is to formulate an easily understandable mathematical strategy for the meaningful analysis of electronic feedback circuits realized in any device technology. The procedure developed herewith is understandable because it exploits only such conventional tools of linear circuit analysis as the Kirchhoff laws, superposition principles, network branch substitution theory and the elementary features of two port network theories [17]. As is the case with most design-oriented analytical techniques, the intent of the procedures disclosed on the following pages is to illuminate network response characteristics whose understood attributes and limitations breed the engineering insights that necessarily underpin prudent engineering circuit design.

6.2. Fundamental Properties of Feedback Loops

The transfer function and driving point impedance characteristics of the majority of electronic feedback systems respectively subscribe to the same mathematical forms. It is, therefore, instructive to precede the circuit level disclosure of feedback principles with a generalized system level study of feedback diagrams, parameters and performance metrics. In this section of material, the parameters governing the electrical signatures of open loop gain and feedback factor are reviewed, as are the interrelationships among the parameters of the closed loop gain, open loop gain and feedback factor. Included among these parameters are the frequencies, the damping factor and the undamped natural frequency of oscillation of the open and closed loops. These parameters are exploited to delineate the closed loop sensitivity to open loop gain, the relative stability of the feedback loop, and the phase margin as a function of open loop critical frequencies. The small signal step response of a second order closed loop is then examined to forge the open loop design guidelines commensurate with acceptable settling times.

6.2.1. Open Loop System Architecture and Parameters

If the feedback undergoing study is global in the sense that the feedback subcircuit routes a portion of the output port signal to the input port, the I/O dynamics of the subject system can be modeled as the block diagram abstracted in Figure 6.1. In this diagram, $A_{ol}(s)$ is the frequency domain transfer function of the open loop amplifier, while $f(s)$, the feedback factor, represents the frequency domain transfer function of the feedback subcircuit. If signals flow only in the direction indicated by the arrows in the diagram, the closed loop transferfunction, $A_{cl}(s)$, is easily verified to be

$$A_{cl}(s) \triangleq \frac{Y(s)}{X(s)} = \frac{A_{ol}(s)}{1 + f(s)A_{ol}(s)} \tag{6.1}$$

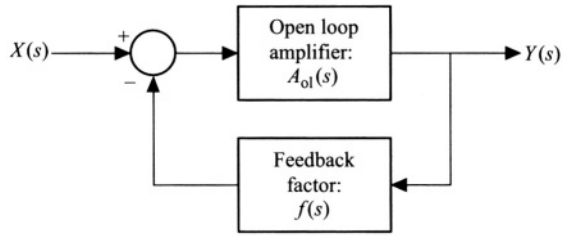


Figure 6.1. System level abstraction of a global feedback architecture. The inputs and outputs, whose frequency domain transforms are symbolized as $X(s)$ and $Y(s)$, respectively, can be voltage or current.

The foregoing expression shows that if $f(s) = 0$, which effectively opens the loop formed by the signal processing blocks whose transfer functions are $A_{ol}(s)$ and $f(s)$, the resultant closed loop gain, $A_{cl}(s)$, is the open loop gain, $A_{ol}(s)$. In lowpass electronics, the open loop invariably contains gain stages, buffers, broadband compensation networks and other topologies that render $A_{ol}(s)$ large over stipulated frequency passbands. Although elementary treatments of feedback systems commonly represent this open loop gain as a single pole transfer function, a more realistic representation is

$$A_{ol}(s) = \frac{A_{ol}(0)(1 - s/z_0)}{(1 + s/p_1)(1 + s/p_2)} \tag{6.2}$$

where p_1 is the frequency of the lower frequency or more dominant pole, p_2 is the frequency of the less dominant pole, and z_0 is the frequency of the transfer function zero. Open loop stability mandates that both p_1 and p_2 have positive real parts. Open loop physical realizability requires that the single zero be a real number and if p_1 and p_2 are complex numbers, they must be complex conjugate pairs. For $z_0 > 0$, the zero lies in the right half complex frequency plane; $z_0 < 0$ implies a left plane zero. Finally, $A_{ol}(0)$ is the zero, or low, frequency gain of the open loop.

An alternative expression for the open loop gain is

$$A_{ol}(s) = \frac{A_{ol}(0)\ (1 - s/z_0)}{1 + (2\zeta_{ol}/\omega_{nol})s + s^2/\omega_{nol}^2} \tag{6.3}$$

In this relationship, z_{ol} is the damping factor. In concert with (6.2), it is given by

$$\zeta_{ol} = \frac{1}{2}\left(\sqrt{\frac{p_2}{p_1}} + \sqrt{\frac{p_1}{p_2}}\right) \tag{6.4}$$

On the other hand,

$$\omega_{nol} = \sqrt{p_1 p_2} \tag{6.5}$$

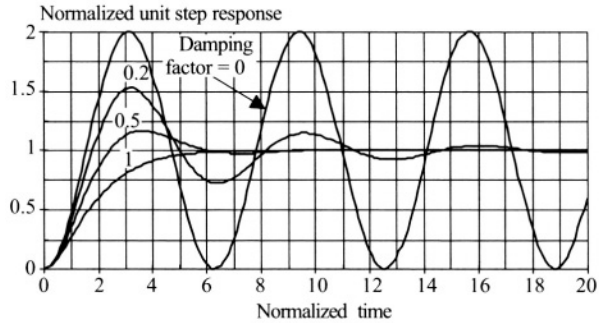


Figure 6.2. Normalized step response of a second order open loop amplifier as a function of normalized time and various damping factors. The open loop amplifier is presumed to have a right half plane zero lying at infinitely large frequency.

symbolizes the undamped natural frequency of oscillation of the open loop network.

A practical implication of the undamped frequency parameter is that υ_{nol} is a measure of the open loop 3-dB bandwidth. Indeed, if $\zeta_{ol} = 1/\sqrt{2}$ and if the frequency of the open loop zero is infinitely large, ω_{nol} is precisely the open loop 3-dB bandwidth. On the other hand, ζ_{ol} is a measure of open loop stability. This contention is supported by Figure 6.2, which depicts the open loop unit step response, normalized to its steady-state value, as a function of the normalized time, $\upsilon_{nol}t$, for the special case of a right half plane zero, z_0, lying at infinitely large frequency. Observe that for $\zeta_{ol} = 1$, which implies identical real poles, a well-behaved step response – albeit one having a relatively large rise time – is produced. In contrast, damping factors smaller than one, which correspond to complex conjugate poles, deliver responses displaying progressively more pronounced ringing. The extreme case of zero damping results in a sinusoidal oscillation. Because an open loop having a second-order transfer function is invariably a simplified approximation of a third or higher order system, inferring potential instability from unacceptably small damping factors in a second-order model comprises prudent engineering interpretation.

6.2.2. Closed Loop System Parameters

An expression for the closed loop transfer function of the feedback system depicted in Figure 6.1 derives from substituting either (6.3) or (6.2) into (6.1). To this end, consider the simplifying case of a frequency-invariant feedback factor; that is $f(s) = f_0$. Then

$$A_{cl}(s) = \frac{A_{ol}(s)}{1 + T(s)} = \frac{A_{cl}(0)(1 + s/z_0)}{1 + (2\zeta_{cl}/\omega_{ncl})s + (s^2/\omega_{ncl}^2)} \tag{6.6}$$

where

$$T(s) = f_0 A_{ol}(s) \tag{6.7}$$

is the loop gain, and the zero frequency closed loop gain is

$$A_{cl}(0) = \frac{A_{ol}(0)}{1 + T(0)} = \frac{A_{ol}(0)}{1 + f_0 A_{ol}(0)} \tag{6.8}$$

A necessary condition for degenerative, or negative, feedback is that the feedback factor, f_0, and the zero frequency open loop gain, $A_{ol}(0)$, have the same algebraic sign. For this negative feedback constraint, the closed loop undamped natural frequency is meaningfully expressed as

$$\omega_{ncl} = \omega_{nol}\sqrt{1 + T(0)} \tag{6.9}$$

Finally, the closed loop damping factor is

$$\zeta_{cl} = \frac{\zeta_{ol}}{\sqrt{1 + T(0)}} - \left[\frac{T(0)}{\sqrt{1 + T(0)}}\right]\frac{\omega_{nol}}{2z_0} \tag{6.10}$$

The foregoing five relationships highlight both advantages and disadvantages of feedback purposefully applied around an open loop circuit. Perhaps the most obvious attribute of feedback is that it desensitizes the closed loop transfer function with respect to perturbations in open loop gain. For example, if the magnitude of the loop gain, $T(j\omega)$, is large over a specified frequency passband, (6.6) and (6.7) show that the closed loop gain over this passband reduces to $(1/f_0)$; that is

$$A_{cl}(jw)\big|_{|T(jw)|\gg 1} \approx \frac{1}{f_0} \tag{6.11}$$

In most integrated circuit amplifiers, the open loop gain depends on poorly controlled or ill-defined processing and active and passive device parameters. Equation (6.11) suggests that a tightly controlled feedback ratio can render predictable and reproducible closed loop performance that is nominally unaffected by the parametric vagaries of the open loop. However, a closed loop gain magnitude of at least unity mandates a feedback factor whose magnitude is at most unity. It follows that the maximum practical value of zero frequency loop gain, T(0), is the magnitude of the open loop gain, $A_{ol}(0)$.

A second advantage of negative feedback is the potential broadbanding that it affords. Recalling that the undamped natural frequency is a measure of, but certainly not identically equal to, the 3-dB bandwidth, (6.9) alludes to bandwidth improvement by a factor of nominally the square root of one plus the zero frequency loop gain. Since this loop gain is necessarily large for acceptably

small closed loop sensitivity to open loop gain, the bandwidth enhancement afforded by negative feedback is potentially significant.

Unfortunately, the factor by which the undamped frequency is increased is roughly the same as the factor by which closed loop stability is degraded. The special case of a right half plane zero lying at infinitely large frequency confirms this contention. From (6.10), observe that the resultant closed loop damping factor is smaller than its open loop counterpart by a factor of the square root of one plus the zero frequency loop gain. As an example, consider a feedback structure at low signal frequencies which has an open loop gain of 24 or 26.6 dB, and an open loop damping factor of 2. The latter stipulation assuredly suggests a dominant pole open loop, since (6.4) yields an open loop pole ratio, p_2/p_1, of 13.9 for $\zeta_{ol}2$. But (6.10) gives a closed loop damping factor of only 0.4, which implies complex conjugate closed loop poles with corresponding significant ringing and overshoot in the closed loop step response.

The preceding numerical example casts a shadow on commonly invoked pole splitting stability compensation measures [18,19]. Pole splitting aims to achieve a large open loop pole ratio, p_2/p_1, so that the resultant closed loop damping factor, is suitably large. Assume that the desired closed loop damping factor satisfies $\zeta_{cl} = 1/\sqrt{2}$, where $\zeta_{cl} = 1/\sqrt{2}$ delivers, in the absence of a finite frequency zero, a maximally flat magnitude second-order frequency response. Then with $T(0) = 24$, (6.10) confirms that the requisite open loop damping factor must be at least 3.54 whence by (6.4), the non-dominant-to-dominant pole frequency ratio must be at least 48. Since the bandwidth of a dominant pole amplifier is essentially prescribed by the frequency of the dominant pole, a pole separation ratio of 48 may be plausible for amplifiers that need deliver only relatively restricted open loop 3-dB bandwidths. But for amplifier applications that mandate large 3-dB bandwidths, pole splitting alone is likely an inadequate or impractical stability compensation measure.

Note that worse case damping factor degradation derives from unity gain closed loop designs for which the loop gain lies at its practical maximum value. This observation explains why general purpose circuits are routinely compensated to ensure stability under unity gain closed loop operating circumstances. Although compensation to ensure unity gain stability is both prudent and desirable in general applications, it usually proves to be overly constraining in many RF amplification and other special purpose integrated circuits.

The damping factor degradation for $z_0 = \infty$ is exacerbated by a finite frequency right half plane zero since the term involving z_0 on the right hand side of (6.10) subtracts from the term proportional to the open loop damping factor. On the other hand, a left half plane zero, say $z_0 = -z_1$, is seen to improve the stability situation in the sense of increasing the closed loop damping attributed to the first term on the left hand side of (6.10). Prudent feedback

compensation scenarios, particularly in high-frequency signal processing applications, therefore, combine procedures aimed toward realizing appropriate left half plane zeros in the loop gain with traditional pole splitting methodologies [14,20].

6.2.3. Phase Margin

Although the preceding damping factor arguments convey a qualitative picture of the stability of a closed feedback loop, they fail to offer a design-oriented guideline that quantifies the degree to which a feedback circuit realization is stable. If the loop gain magnitude response is a well-behaved, monotonically decreasing function of signal frequency, either the phase margin or the gain margin proves to be an expedient stability metric. Of these two metrics, the phase margin is more easily evaluated mathematically.

For steady-state sinusoidal operating conditions, the closed loop gain in (6.6) becomes

$$A_{cl}(j\omega) = \frac{A_{ol}(j\omega)}{1 + T(j\omega)} \tag{6.12}$$

where, from (6.7) and (6.2), the loop gain is

$$T(j\omega) = f_0 A_{ol}(j\omega) = \frac{T(0)(1 - j\omega/z_0)}{(1 + j\omega/p_1)(1 + j\omega/p_2)} \tag{6.13}$$

For frequency-invariant feedback, this loop gain displays a frequency response that mirrors that of the open loop transfer function. Moreover, the loop gain equals the open loop transfer function for the special case of a closed loop designed for unity gain.

Let ω_u denote the radial frequency at which the magnitude of the loop gain is unity. Then

$$T(j\omega_u) = e^{j(\phi_m - \pi)} \tag{6.14}$$

where $(\phi_m - \pi)$ is the phase angle of the loop gain at the frequency where the loop gain magnitude is one. The phase angle, ϕ_m, is the phase margin of the closed loop. Its significance can be appreciated by noting that if $\phi_m = 0$, $T(j\omega_u) = -1$, whence (6.12) predicts sinusoidal closed loop oscillations. It follows that closed loop stability requires that the phase angle of the loop gain at the loop gain unity gain frequency be sufficiently less negative than –180°; that is, a sufficiently large and positive phase margin, ϕ_m, is required.

The phase margin can be quantified if a few simplifying approximations appropriate to pragmatic design objectives are invoked. In particular, assume that the open loop amplifier, and hence, the loop gain, possesses a dominant pole frequency response. This approximation implies $p_2 \gg p_1$ and gives rise to a greater than unity open loop damping factor, which has been noted as

conducive to an acceptably large closed loop damping factor. Assume further that the frequency, z_0, of the right half plane zero, like the frequency of the non-dominant pole, p_2, is also very large. This requirement also reflects design practicality since small z_0 results in an uncompromisingly small closed loop damping factor. As a result, the 3-dB bandwidth of the loop gain approximates p_1, and the gain bandwidth product of the loop gain is simply $T(0)p_1$. If both p_2 and z_0 are larger than the loop gain unity gain frequency, ω_u, it follows that

$$\omega_u \approx T(0)p_1 \tag{6.15}$$

It is convenient to normalize the frequencies, p_2 and z_0, to the approximate loop gain unity gain frequency defined by (6.15). In particular, let

$$k_p = \frac{p_2}{\omega_u} \tag{6.16}$$

and

$$k_0 = \frac{z_0}{\omega_u} \tag{6.17}$$

Equations (6.15)–(6.17) allow the closed loop damping factor in (6.10) and the closed loop undamped natural frequency in (6.9) to be expressed respectively as

$$\zeta_{cl} = \frac{1}{2\sqrt{k_p T(0)[1+T(0)]}}\left[k_p T(0)\left(1-\frac{1}{k_0}\right)+1\right] \approx \frac{\sqrt{k_p}}{2}\left(1-\frac{1}{k_0}\right) \tag{6.18}$$

and

$$\omega_{ncl} = \omega_u\sqrt{\frac{k_p[1+T(0)]}{T(0)}} \approx \omega\sqrt{k_p} \tag{6.19}$$

The approximations in these last two relationships are premised on the assumption of very large zero frequency loop gain, a condition observed earlier as one that encourages closed loop response desensitization to open loop parameters.

Returning to the phase margin problem, (6.13)–(6.17) deliver

$$\phi_m - \pi = -\tan^{-1}(1k_0) - \tan^{-1}T(0) - \tan^{-1}\left(\frac{1}{k_p}\right) \tag{6.20}$$

Upon introducing the constant, k, such that

$$k \triangleq \frac{k_p k_0 - 1}{k_p + k_0} \tag{6.21}$$

the application of the appropriate trigonometric identities to (6.20) provides

$$\phi_m = \tan^{-1}\left[\frac{1+kT(0)}{T(0)-k}\right] \tag{6.22}$$

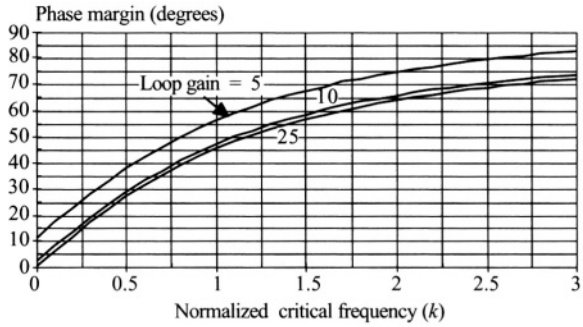


Figure 6.3. Phase margin dependence on zero frequency loop gain and on frequencies of right half plane zero and non-dominant pole.

For large zero frequency loop gain, (6.22) collapses to the simple result,

$$\phi_m \approx \tan^{-1}(k) \tag{6.23}$$

It should be remembered that because of the presumption that the unity gain frequency of the loop gain in (6.13) closely approximates the product, $T(0)p_1$, (6.22) and (6.23) provide realistic estimates of phase margin only when the frequencies of the non-dominant pole and zero are each larger than the estimated unity gain frequency. This is to say that (6.22) and (6.23) are valid insofar as

$$k_0, k_p > 1 \tag{6.24}$$

For the deleterious circumstance of a right half plane zero (z_0 and thus, k_0 positive), Figure 6.3 graphically displays the dependence of phase margin on parameter k for various values of the zero frequency loop gain, $T(0)$.

Example 6.1. A second-order negative feedback amplifier is designed to have a loop gain at zero frequency of 25 (28 dB). The loop gain displays a right half plane zero at a frequency that is four times larger than the loop gain unity gain frequency. What phase margin is required if, ignoring the right half plane zero, the closed loop amplifier is to establish a maximally flat magnitude frequency response?

Solution 6.1.

1 A maximally flat lowpass amplifier implies (ignoring the effects of any zeros) a closed loop damping factor, ζ_{cl}, of $1/\sqrt{2}$. Since the right half plane zero is four times the unity gain frequency of the loop gain, $k_0 = 4$. The approximate form of (6.18) therefore, suggests $k_p = 3.56$. This is to

say that the non-dominant pole of the open loop amplifier must be more than 3.5 times larger than the unity gain frequency of the loop gain!

2 With $k_p = 3.56$ and $k_0 = 4$, k in (6.21) is 1.75.

3 Given k = 1.75 and T(0) = 25, (6.22) implies a phase margin of $\phi_m = 62.6°$.

Comment. To protect against oscillations incurred by parasitic energy storage and related interconnect phenomena, practical analog integrated circuits designed to be stable under unity closed loop gain conditions must generally have phase margins in the range of 60–70 degrees. This constraint typically translates into the requirement that the non-dominant amplifier pole be at least 3–4 times larger than the amplifier unity gain frequency. Since such an operating prerequisite comprises a formidable design task for amplifiers that must operate at RF signal frequencies, the stability condition is often relaxed to ensure adequate phase margin for only closed loop gains in the neighborhood of the specified closed loop gain performance.

6.2.4. Settling Time

The preceding section of material demonstrates that the phase margin, which effectively is the degree to which a closed feedback loop is stable, is strongly influenced by the frequencies of both the non-dominant pole and the zero implicit to the loop gain. These critical frequencies have an equally strong effect on the closed loop damping factor, which, in turn, determines the time domain nature of the closed loop transient response. For the often encountered case of a closed loop damping factor that is smaller than one, it follows that the phase margin influences the time required by the step response to converge to within a suitably small percentage of the desired steady-state output value. This time domain performance metric is commonly referred to as the settling time.

An investigation of the settling time of a closed feedback loop commences with designating the input to the system abstracted in Figure 6.1 as a unit step, for which the Laplace transform is $X(s) = 1/s$. The resultant transformed output is, from (6.6)

$$Y(s) = A_{cl}(s)X(s) = \frac{A_{ol}(s)}{s[1 + T(s)]} = \frac{A_{cl}(0)(1 - s/z_0)}{s\left(1 + (2\zeta_{cl}/\omega_{ncl})s + s^2/\omega_{ncl}^2\right)} \tag{6.25}$$

where $A_{cl}(0)$ now represents the steady-state value of the unit step response. This step response, say $y(t)$, is obviously the inverse Laplace transform of the right hand side of (6.25). If $y(t)$ is normalized to its steady-state value,

$$\epsilon(t) = 1 - \frac{y(t)}{A_{cl}(0)} \tag{6.26}$$

signifies an error between the normalized steady-state response and the actual normalized step response. An error, $\epsilon(t)$, of zero corresponds to an instantaneously settling output; that is, zero settling time.

Introducing the constants, M and θ, such that

$$M \triangleq \frac{z_0}{\omega_{\text{ncl}}} \equiv \frac{k_0}{\sqrt{k_p}} \tag{6.27}$$

and

$$\theta \triangleq \tan^{-1}\left(\frac{M\sqrt{1-\zeta_{\text{cl}}^2}}{1+M\zeta_{\text{cl}}}\right) \tag{6.28}$$

and letting

$$x \triangleq \omega_{\text{cl}} t \tag{6.29}$$

denote a normalized time variable, it can be shown that the error function defined by (6.26) is given by

$$\epsilon(x) = \left[\frac{1+2M\zeta_{\text{cl}}+M^2}{M^2(1-\zeta_{\text{cl}}^2)}\right]^{1/2} e^{-\zeta_{\text{cl}}x} \sin\left[x\sqrt{1-\zeta_{\text{cl}}^2}+\theta\right] \tag{6.30}$$

This result presumes an underdamped closed loop and a zero lying in the right half plane.

Figure 6.4 pictures the time domain nature of the error function in (6.30). The presence of a right half plane zero causes the error to be positive in the neighborhood of the origin. Equivalently, the step response displays undershoot shortly after time $t = 0$. Thereafter, the step response error is a damped sinusoid

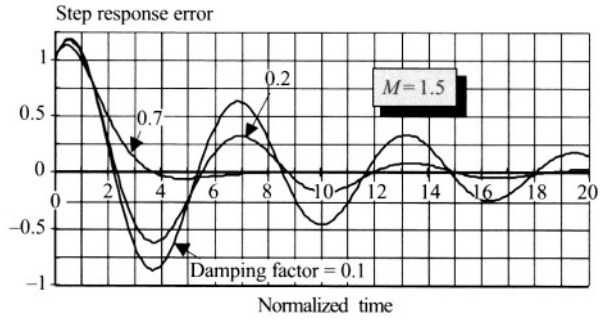


Figure 6.4. The time domain error between steady state and actual normalized step responses of an underdamped second order closed feedback loop. A right half plane zero whose frequency is 50% larger than the closed loop undamped frequency of oscillation ($M = 1.5$) is presumed.

for which maxima are manifested with a period of π. As expected, the rate at which the error converges toward its idealized value of zero increases for progressively larger damping factors, thereby suggesting that small damping factors imply long settling times.

The strategy for determining the closed loop settling time entails determining the time domain slope, $d\epsilon(x)/dx$, of the error function. From the preceding discussion, this slope is periodically zero. The smallest value of normalized time x corresponding to zero slope of error defines the maximum error associated with initial undershoot. The second value of x, say x_m, corresponding to zero slope of error defines the maximum magnitude of error, say ϵ_m. If this maximum error magnitude at most equals the specified design objective for allowable error in the steady-state response, x_m defines the normalized settling time for the closed loop.

Upon adoption of the foregoing analytical strategy, the settling time, t_m, is implicitly found as

$$x_m = \omega_{ncl} t_m = \frac{1}{\sqrt{1-\zeta_{cl}^2}} \left[\pi + \tan^{-1} \left(\frac{\sqrt{1-\zeta_{cl}^2}}{\zeta_{cl} + M} \right) \right] \tag{6.31}$$

which conforms to an error maximum of

$$\epsilon_m = e^{-\zeta_{cl} x_m} \sqrt{1 + \frac{2\zeta_{cl}}{M} + \frac{1}{M^2}} \tag{6.32}$$

Very small closed loop damping factors are obviously undesirable. Thus, for reasonable values of damping (perhaps, $z_{cl} \geq 0.6$) and/or large M (large right half plane zero frequency), (6.31) and (6.32) respectively reduce to

$$x_m = \omega_{ncl} t_m \approx \frac{\pi}{\sqrt{1-\zeta_{cl}^2}} \tag{6.33}$$

and

$$\epsilon_m \approx e^{-\zeta_{cl} x_m} \tag{6.34}$$

Given large M, (6.18), (6.21), and (6.23) allow expressing the preceding two relationships in the more useful forms,

$$x_m = \omega_{ncl} t_m \approx \frac{2\pi}{\sqrt{4-k_p}} \tag{6.35}$$

and

$$\epsilon_m \approx \exp\left(-\pi \sqrt{\frac{k_p}{4-k_p}} \right) \tag{6.36}$$

Example 6.2. A second order feedback amplifier is to be designed so that its response to a step input settles to within 2% of steady-state value within 750 pSEC. The low frequency loop gain is very large and to first order, the frequencies of any right half plane circuit zeros can also be taken as large. Determine the requisite unity gain frequency of the loop gain, the frequency of the non-dominant loop gain pole and the phase margin.

Solution 6.2.

1 From (6.36),

$$\epsilon_m \approx \exp\left(-\pi\sqrt{\frac{k_p}{4-k_p}}\right) \leq 0.02$$

implies $k_p \geq 2.43$. Thus, the non-dominant pole of the loop gain function must be more than 2.4 times larger than the unity gain frequency of said loop gain.

2 With $k_p = 2.43$, and in view of the 750 pSEC settling time specification, (6.35) delivers $\omega_{ncl} = (2\pi)(1.07\,\text{GHz})$. Recalling (6.19), this result means that the requisite unity gain frequency must be at least as large as $\omega_u = (2\pi)(682.8\text{MHz})$.

3 Since k_p symbolizes the ratio of the frequency of the non-dominant pole to the unity gain frequency, the preceding two computational steps yield $p_2 = (2\pi)(1.66\ \text{GHz})$.

4 When the frequency of the right half plane zero is very large, k in (6.21) and (6.23) is very nearly k_p. The latter of these two relationships delivers a required phase margin of $\phi_m = 67.7°$.

Comment. Since the impact of the right half plane zero is tacitly ignored in this calculation, a prudent design procedure calls for increasing the computed phase margin by a few degrees. Although the resultant phase margin and other design requirements indigenous to this example are hardly trivial, they are achievable with appropriate device technologies and creative circuit design measures. The latter are likely to entail open loop pole splitting and/or the incorporation of a compensating zero within the feedback factor.

6.3. Circuit Partitioning

From a purely computational perspective, the preceding section of material is useful for determining the steady-state performance, transient time-domain performance, sensitivity, and stability of practical feedback networks. But from the viewpoint of circuit design, the practicality of the subject material might logically be viewed as dubious, for it promulgates results that depend on unambiguous definitions of the open loop gain and feedback factor. Stated

more directly, the results of Section (6.2) are useful only insofar as the transfer function of interest for a given circuit can be framed in the block diagram architecture of Figure 6.1. Unfortunately, casting a circuit transfer function into the form of Figure 6.1 is a non-trivial task for at least three reasons. First, neither the open loop amplifier nor the feedback function conducts signals unilaterally. This is to say that amplifiers, and especially amplifiers operated at high signal frequencies, invariably have intrinsic feedback. Moreover, since the feedback subcircuit is generally a passive network, it is clearly capable of conducting signals from circuit input to circuit output ports, as well as from output to input ports. Second, the open loop amplifier function is not completely independent of the parameters of the feedback subcircuit, which invariably imposes impedance loads on the amplifier input and output ports. Third, Figure 6.1 pertains only to global feedback structures. But practical feedback circuits may exploit local feedback; that is, feedback imposed between any two amplifier ports that are not necessarily the output and input ports of the considered system. Local feedback is often invoked purposefully in broadband analog signal processing applications. On the other hand, parasitic local feedback is commonly encountered in high-frequency systems because of energy storage parasitics associated with proximate on-chip signal lines, bond wire interconnects and packaging.

Fortunately, theoretical techniques advanced originally by Kron [21,22] exist to address this engineering dilemma. As is illustrated below, these techniques, which are now embodied into modern circuit partitioning theory [23], have been shown to be especially utilitarian in feedback circuit applications [24].

6.3.1. Generalized Circuit Transfer Function

Consider the arbitrary linear circuit abstracted in Figure 6.5(a). A voltage signal having Thévenin voltage V_s and Thévenin impedance Z_s, is presumed to excite the input port of the circuit, while a load impedance, Z_l, terminates the output port. If the subject linear circuit can be characterized by a lumped equivalent model, the voltage gain, $A_{vo} = V_o/V_s$, the input impedance, Z_{in0}, seen by the applied signal source, and the output impedance, Z_{out0}, facing the load termination can be evaluated straightforwardly. Although a voltage amplifier is tacitly presumed in the senses of representing both the input and output signals as voltages, the same statement regarding gain and the driving point input and output impedances applies to transimpedance, transadmittance and current amplifiers.

Let the network under consideration be modified by applying feedback from its k-th to c-th ports, where port k can be, but is not necessarily, the output port of the circuit, and port c can be, but is not necessarily, the input port. An elementary representation of this feedback is a voltage controlled current source,

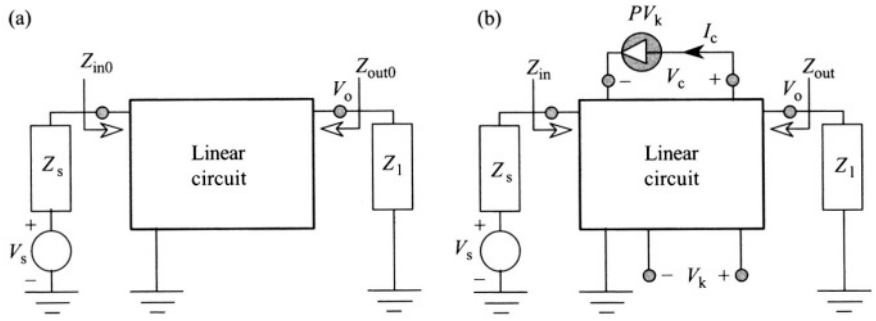


Figure 6.5. (a) arbitrary linear circuit operated as a voltage amplifier. (b) The circuit in (a) with feedback, represented by an ideal voltage controlled current source, applied from controlling port k to controlled port c.

PV_k, as diagrammed in Figure 6.5(b). The implication of this controlled source is that a feedback subcircuit is connected from the k-th to c-th ports of the original linear network, as suggested in Figure 6.6(a). In the interest of analytical simplicity, this subcircuit is presumed to behave as the ideal voltage controlled current source delineated in Figure 6.6(b). In particular, the input voltage to the feedback subcircuit is the controlling voltage, V_k, of the dependent current source, $I_c = PV_k$, which emulates a simplified Norton equivalent circuit of the output port of the feedback subcircuit.

Superposition theory applied with respect to the independent signal source, V_s, and the dependent, or controlled, current, I_c, in Figure 6.5(b) yields

$$V_o = A_{vo}V_s + Z_{oc}I_c \tag{6.37}$$

and

$$V_k = A_{ks}V_s + Z_{kc}I_c \tag{6.38}$$

In these relationships, A_{vo}, Z_{oc}, A_{ks} and Z_{kc} are frequency dependent constants of proportionality that link the variables, V_s and I_c to the observable circuit voltages, V_o and V_k. In (6.37), it should be noted that A_{vo} is the voltage gain, V_o/V_s, under the condition of $I_c = 0$. This observation corroborates with the circuit in Figure 6.5(a), for which the voltage gain in the absence of feedback, which implies P, and hence I_c, is zero, has been stipulated as A_{vo}.

Recalling that $I_c = PV_k$, (6.38) implies

$$V_k = \frac{A_{ks}V_s}{1 - PZ_{kc}} \tag{6.39}$$

whence

$$I_c = PV_k = \frac{PA_{ks}V_s}{1 - PZ_{kc}} \tag{6.40}$$

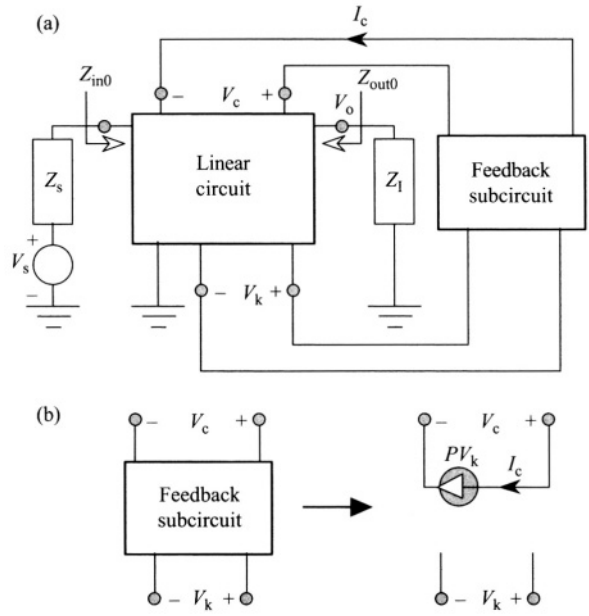


Figure 6.6. (a) The linear circuit in Figure 6.5(a) with a feedback subcircuit incident between k-th and c-th ports of the original network. (b). Voltage controlled voltage source model of the feedback subcircuit in (a).

Assuming A_{vo} is non-zero and bounded, the insertion of the last result into (6.37) establishes the desired voltage transfer function relationship,

$$A_{vc} = \frac{V_o}{V_s} = \frac{A_{vo}[1 - P(Z_{kc} - A_{ks}Z_{oc}/A_{vo})]}{1 - PZ_{kc}} \tag{6.41}$$

Equation (6.41) properly defines the closed loop gain in that through non-zero P, an analytical accounting of the effects of feedback between any two network ports has been made.

In the denominator on the right hand side of (6.41), respectively define

$$Q_s(Z_s, Z_l) \triangleq -Z_{kc} \tag{6.42}$$

and

$$T_s(P, Z_s, Z_l) \triangleq -PZ_{kc} \equiv PQ_s(Z_s, Z_l) \tag{6.43}$$

as the normalized return ratio with respect to feedback parameter P and the return ratio with respect to P. Although not explicitly delineated, both $Q_s(\cdot)$ and $T_s(\cdot)$ are functions of frequency because in general, the parameters, P and Z_{kc}, as well as the source and load impedances, Z_s and Z_l, are frequency

dependent. Analogously, introduce

$$Q_r(Z_s, Z_l) \triangleq -\left(Z_{kc} - \frac{A_{ks} Z_{oc}}{A_{vo}}\right) \tag{6.44}$$

as the normalized null return ratio with respect to P and

$$T_r(P, Z_s, Z_l) \triangleq -P\left(Z_{kc} - \frac{A_{ks} Z_{oc}}{A_{vo}}\right) \equiv P\,Q_r(Z_s, Z_l) \tag{6.45}$$

as the null return ratio with respect to P. Like $Q_s(\cdot)$ and $T_s(\cdot)$, $Q_r(\cdot)$ and $T_r(\cdot)$ are functions of frequency. Equation (6.41) is now expressible as

$$A_{vc} = A_{vo}\left[\frac{1 + T_r(P, Z_s, Z_l)}{1 + T_s(P, Z_s, Z_l)}\right] = A_{vo}\left[\frac{1 + P\,Q_r(Z_s, Z_l)}{1 + P\,Q_s(Z_s, Z_l)}\right] \tag{6.46}$$

Either form of the preceding relationship is a general expression for the voltage gain of feedback structures whose electrical characteristics subscribe to those implied by Figure 6.6. Equation (6.46) is actually a general gain expression for all feedback architectures, regardless of either the electrical nature of parameter P or the electrical model that emulates the terminal characteristics of the feedback subcircuit. Because of this generality contention, it may be illuminating to observe that (6.46) gives rise to the block diagram representation offered in Figure 6.7. This architecture portrays the null return ratio, $T_r(\cdot) = P\,Q_r(\cdot)$, as a feedforward transfer function from the source signal node to the node at which the output signal produced by the feedback subcircuit is summed. The transfer function of the feedback subcircuit is clearly dependent on the return ratio, $T_s(\cdot) = P\,Q_s(\cdot)$, so that no feedback prevails when the normalized return ratio is zero. Both the null return ratio and the return ratio are directly proportional to the parameter, P, which causes feedback to be incurred between two

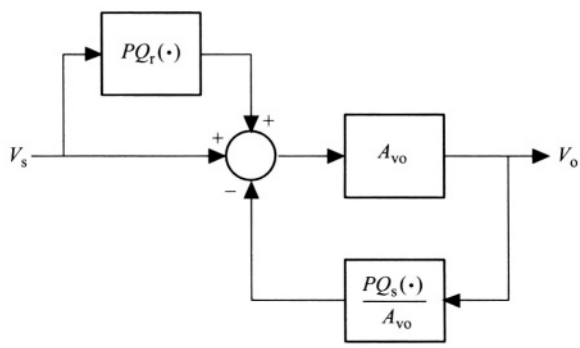


Figure 6.7. Block diagram model of the I/O transfer function for the feedback network in Figure 6.6.

network ports. It might, therefore, be stated that the return ratio is a measure of the feedback caused by the feedback subcircuit, while the null return ratio measures feedforward phenomena through the feedback subcircuit.

It is also interesting to speculate that the general feedback system of Figure 6.6 can be viewed, at least insofar as the I/O transfer function is concerned, as an equivalent global feedback network. To this end, a comparison of (6.46) with (6.6) and the abstraction in Figure 6.1 suggests defining an equivalent open loop gain as

$$A_{ol}(s) = A_{vo}[1 + P\,Q_r(Z_s, Z_l)] \tag{6.47}$$

while the equivalent loop gain, T(s), follows as

$$T(s) = P\,Q_s(Z_s, Z_l) \tag{6.48}$$

Since the feedback factor, $f(s)$, in (6.6) is the loop gain divided by the open loop gain, (6.47) and (6.48) imply

$$f(s) = \frac{P\,Q_s(Z_s, Z_l)}{A_{vo}[1 + P\,Q_r(Z_s, Z_l)]} \tag{6.49}$$

As conjectured earlier, the open loop gain and feedback factor are difficult to separate in practical feedback structures. In particular, (6.47) shows that the open loop gain is dependent on the feedback parameter, P, and (6.48) depicts a feedback factor that is not independent of the open loop gain function.

Equation (6.46) underscores the fact that the voltage gain of the architecture depicted in Figure 6.6 relies on only three metrics. These metrics are the gain, A_{vo}, for parameter $P = 0$, the return ratio, $T_s(\cdot)$, and the null return ratio $T_r(\cdot)$. Since a straightforward nodal or loop analysis of a feedback network such as that shown in Figure 6.6(a) is likely to be so mathematically involved as to obscure an insightful understanding of network volt–ampere dynamics, it may be productive to investigate the propriety of alternatively evaluating the foregoing three metrics. In other words, it may be wise to partition the single problem of gain evaluation into three, presumably simpler, analytical endeavors.

Recalling (6.42)–(6.45), the voltage gain, A_{vo}, in (6.46) is the gain for the special case of $P = 0$. Since $P = 0$ corresponds to zero feedback from k-th to c-th ports, and since the configuration in Figure 6.5(b) is the model of the feedback network in Figure 6.6(a), A_{vo} can be evaluated by analyzing the reduced network depicted symbolically in Figure 6.8(a). Observe that the calculation of A_{vo} is likely to be simpler than that of A_{vc} because the subcircuit causing voltage controlled current feedback from k-th to c-th ports in Figure 6.6(a) is effectively removed.

From (6.38),

$$\left.\frac{V_k}{I_c}\right|_{V_s=0} \equiv Z_{kc} \tag{6.50}$$

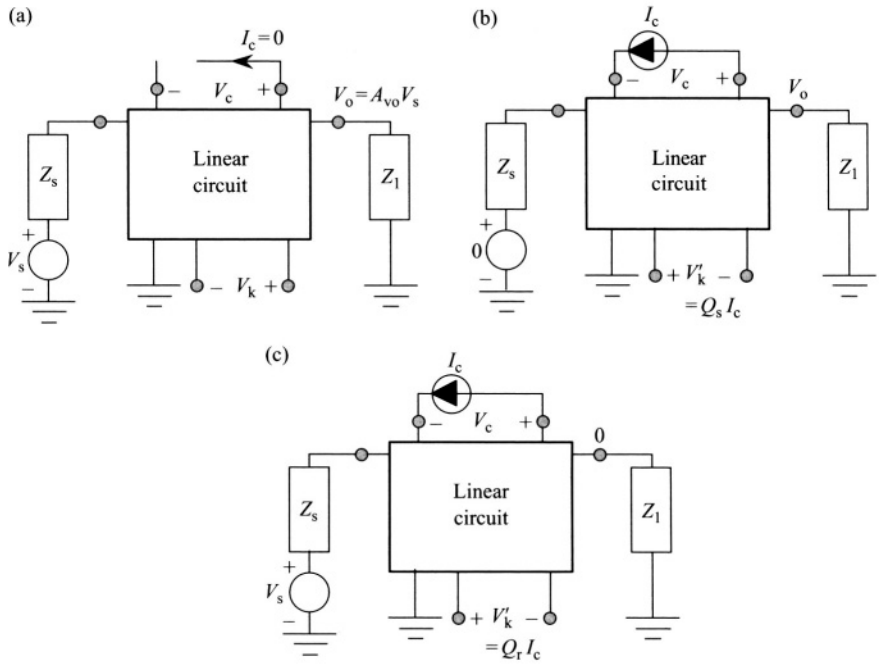


Figure 6.8. (a) Circuit used to calculate voltage gain for nulled feedback parameter. (b) Circuit used to calculate the normalized return ratio. (c) Circuit used to calculate the normalized null return ratio.

Because of (6.42),

$$Q_s(Z_s, Z_l) = \frac{-V_k}{I_c}\bigg|_{V_s=0} = \frac{V'_k}{I_c}\bigg|_{V_s=0} \tag{6.51}$$

This result suggests a return ratio evaluation that entails (1) setting the independent signal source to zero, (2) replacing the dependent current generator at the output port of the feedback subcircuit by an independent current source, I_c, and (3) calculating the negative ratio of V_k to I_c. In short, $T_s(\cdot)$ is parameter P multiplied by the negative ratio of controlling variable $(V_k = -V'_k)$ to controlled variable (I_c), under the condition of nulled input signal. The computational scenario at hand is diagrammed in Figure 6.8(b), where the original polarity of voltage V_k is reversed, and hence denoted as V'_k, while the original direction of current I_c is preserved.

Return to (6.37) and (6.38) but now, constrain the output voltage, V_o, to zero. With the PV_k generator replaced by an independent current source, I_c,

the signal source voltage, V_s, necessarily assumes the value,

$$V_s = -\frac{Z_{oc} I_c}{A_{vo}} \tag{6.52}$$

If this source voltage is inserted into (6.38), it follows that

$$\left.\frac{-V_k}{I_c}\right|_{V_o=0} = -\left(Z_{kc} - \frac{A_{ks} Z_{oc}}{A_{vo}}\right) \tag{6.53}$$

whence by (6.44)

$$Q_r(Z_s, Z_l) = \left.\frac{-V_k}{I_c}\right|_{V_o=0} = \left.\frac{V_k'}{I_c}\right|_{V_o=0} \tag{6.54}$$

As suggested in Figure 6.8(c), the null return ratio computation entails (1) nulling the output response, (2) replacing the dependent current generator at the output port of the feedback subcircuit by an independent current source, I_c, and (3) calculating the negative ratio of V_k to I_c. In short, $T_r(\cdot)$ is parameter P multiplied by the ratio of phase inverted controlling variable $(V_k - V_k')$ to controlled variable (I_c), under the condition of a nulled output response.

6.3.2. Generalized Driving Point I/O Impedances

The driving point input impedance, Z_{in}, seen by the signal source applied to the feedback network in Figure 6.5(b) derives from replacing the source circuit by an independent current source, say I_x, and computing the ratio, V_x/I_x, where V_x is the disassociated reference polarity voltage developed across the I_x source. This computational scenario is illustrated in Figure 6.9(a). Since $Z_{in} V_x/I_x$ is a transfer function, (6.46) prescribes the form of this transfer relationship as

$$Z_{in} = \frac{V_x}{I_x} = Z_{in0}\left[\frac{1 + P Q_r(Z_s, Z_l)}{1 + P Q_s(Z_s, Z_l)}\right] \tag{6.55}$$

In (6.55) Z_{in0} is the $P = 0$ value of the input impedance. This null parameter input impedance is the V_x/I_x ratio evidenced when parameter P is set to zero, as diagrammed in Figure 6.9(b). The functions, $Q_s'(\cdot)$ and $Q_r'(\cdot)$, respectively represent the normalized return ratio and the normalized null return ratio associated with the network input impedance.

Figure 6.9(c) is appropriate to the computation of $Q_s'(\cdot)$, wherein (1) the independent signal source, I_x, applied to the circuit in Figure 6.9(a) is set to zero, (2) the dependent current generator at the output port of the feedback subcircuit is supplanted by an independent current source, I_c, and (3) the negative ratio

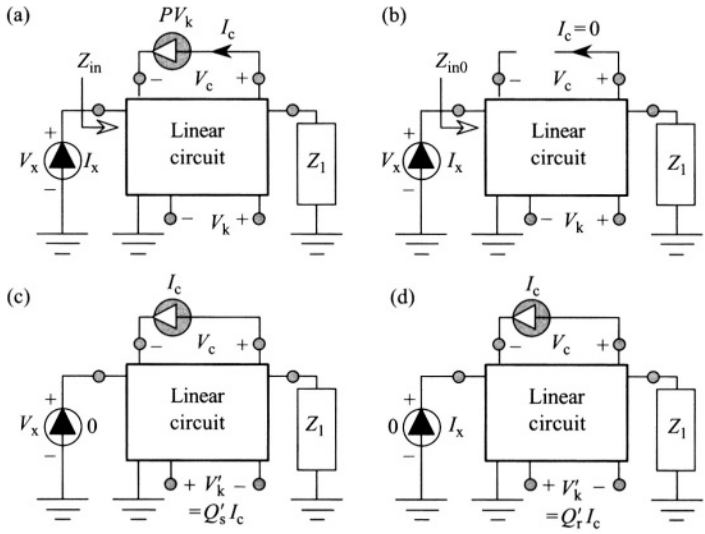


Figure 6.9. (a) Circuit configuration used to calculate the driving point input impedance. (b) Circuit used to calculate the null parameter driving point input impedance. (c) Circuit used to compute the normalized return ratio pertinent to the input impedance function. (d) Circuit used to compute the null normalized return ratio pertinent to the input impedance function.

of V_k ($V_k = -V'_k$) to I_c is evaluated. Observe, however, that Figure 6.9(c) is similar to Figure 6.8(b), which is exploited to determine the normalized return ratio pertinent to the voltage transfer function of the considered network. Indeed, if Z_s were infinitely large in Figure 6.8(b), both circuits would be identical since nulling I_x in Figure 6.9(c) is tantamount to open circuiting the source circuit. Accordingly,

$$Q'_s(Z_s, Z_l) \equiv Q_s(\infty, Z_l) \tag{6.56}$$

The normalized null return ratio, $Q'_r(\cdot)$, is evaluated from a circuit analysis conducted on the system shown in Figure 6.9(d). In this diagram, (1) the output response in the circuit of Figure 6.9(a), which is V_x, is set to zero, (2) the dependent current generator at the output port of the feedback subcircuit is replaced by the current source, I_c, and (3) the negative ratio of V_k ($V_k = -V'_k$) to I_c is evaluated. But Figure 6.9(d) is also similar to Figure 6.8(b). Both structures are topologically identical if Z_s in Figure 6.8(b) is zero since nulling V_x in Figure 6.9(d) amounts to grounding the source input port. Thus,

$$Q'_r(Z_s, Z_l) \equiv Q_s(0, Z_l) \tag{6.57}$$

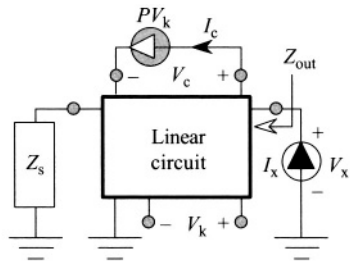


Figure 6.10. Circuit configuration used to calculate the driving point output impedance.

and it follows that the input impedance in (6.55) is expressible as

$$Z_{in} = \frac{V_x}{I_x} = Z_{in0}\left[\frac{1 + PQ_s(0, Z_l)}{1 + PQ_s(\infty, Z_l)}\right] \tag{6.58}$$

The last equation suggests that since $Q_s(\cdot)$ is already known from work leading to the determination of the circuit transfer function, the null parameter impedance, Z_{in0}, is the only function that need be determined to evaluate the driving point input impedance. It is noteworthy that the evaluation of Z_{in0} is likely to be straightforward since, like the evaluation of the null parameter gain, A_{vo}, it derives from an analysis of a circuit for which the dependent source emulating feedback from k-th to c-th ports is nulled.

Figure 6.10 is the applicable circuit for determining the driving point output impedance, Z_{out}, facing the load impedance, Z_l. Observe that the Thévenin source voltage, V_s, is nulled and that the load is replaced by an independent current generator, I_y. The analytical disclosures leading to the input impedance relationship of (6.58) can be adapted to Figure 6.10 to show that

$$Z_{out} = \frac{V_y}{I_y} = Z_{out0}\left[\frac{1 + PQ_s(Z_s, 0)}{1 + PQ_s(Z_s, \infty)}\right] \tag{6.59}$$

where Z_{out0} is the output impedance under the condition of a nulled feedback parameter; that is, $Z_{out} = Z_{out0}$ when $P = 0$.

6.3.3. Special Controlling/Controlled Port Cases

Equations (6.46), (6.55), and (6.59) are respectively general gain, input impedance, and output impedance expressions for any linear network in which feedback is evidenced between any two network ports. In addition to their validity, these relationships are quite useful in modern electronics and can be confidently applied as long as the null metrics, A_{vo}, Z_{in0}, and Z_{out0}, are non-zero and finite. Despite their engineering utility, several special cases

commonly arise to justify particularizing the subject relationships for the applications at hand.

Controlling feedback variable is the circuit output variable. In Figure 6.5(b) consider the case in which the variable, V_k, which controls the amount of current fed back to the controlled or c-th port of the network, is the output response, voltage V_o in this case. The present situation is delineated in Figure 6.11 (a). The pertinent input and output impedance expressions remain given by (6.55) and (6.59), respectively, where Z_{in0} and Z_{out0} are impedances evaluated under the condition of $P = 0$. Similarly, Z_{vo} in (6.46) is the $P = 0$ value of the input-to-output voltage gain.

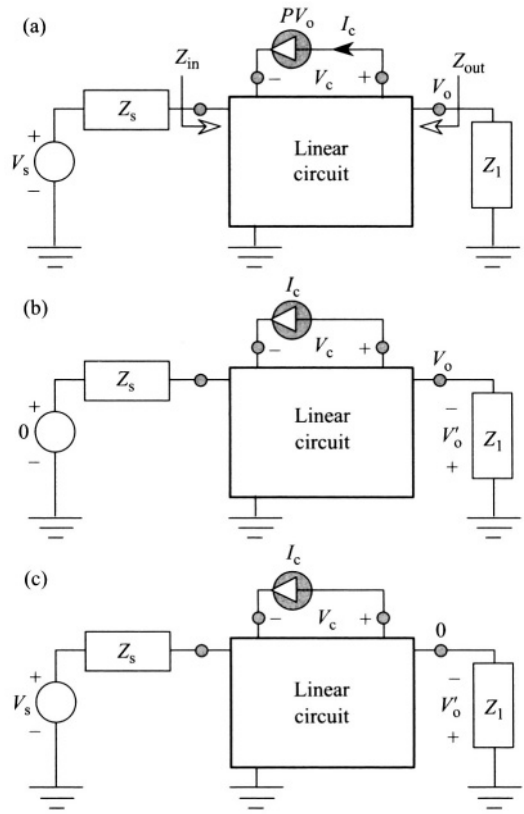


Figure 6.11. (a) Feedback circuit in which the controlling feedback variable is the output response. (b) Circuit used to calculate the normalized return ratio with respect to parameter P. (c) Circuit used to calculate the normalized null return ratio with respect to parameter P.

Figure 6.11 (b) shows the circuit pertinent to evaluating the normalized return ratio, $Q_s(\cdot)$. In accordance with the procedures set forth above, the Thévenin signal voltage, V_s, is set to zero, the $PV_k = PV_o$ dependent current generator is replaced by an independent current source, I_c, and the polarity of the controlling variable, V_o, of the dependent source is reversed and noted as V_o'. From (6.51), the normalized return ratio is

$$Q_s(Z_s, Z_l) = \left.\frac{-V_o}{I_c}\right|_{V_s=0} = \left.\frac{V_o'}{I_c}\right|_{V_s=0} \tag{6.60}$$

The normalized null return ratio, $Q_r(\cdot)$, derives from an analysis of the configuration depicted in Figure 6.11(c). In this circumstance, the Thévenin signal voltage is not nulled, but the output voltage, V_o, is. Moreover, the $PV_k = PV_o$ dependent current source is replaced by an independent current, I_c, and the polarity of the controlling variable, V_o, of the dependent source is reversed and noted as V_o'. But since $V_o' = -V_o = 0$, (6.54) delivers

$$Q_r(Z_s, Z_l) = \left.\frac{-V_o}{I_c}\right|_{V_o=0} = \left.\frac{V_0'}{I_c}\right|_{V_o=0} \equiv 0 \tag{6.61}$$

Since the normalized null return ratio is zero, the resultant gain equation in (6.46) simplifies to

$$A_{vc} = A_{vo}\left[\frac{1 + PQ_r(Z_s, Z_l)}{1 + PQ_s(Z_s, Z_l)}\right] = \frac{A_{vo}}{1 + PQ_s(Z_s, Z_l)} \tag{6.62}$$

Global feedback. In the global feedback system abstracted in Figure 6.12(a), the controlling feedback variable, V_k, is the output variable, V_o and in addition, the controlled, or c-th, port is the network input port. Since the controlling and output variables are the same, the normalized null return ratio is zero, as in the preceding special case. Although the null parameter voltage gain, A_{vo}, and the normalized return ratio, $Q_s(\cdot)$, can be computed in the usual fashion, for global feedback circumstances it is expedient to model the signal source as the same type of energy source used to emulate the fed back signal. In this case, the fed back signal happens to be a current source. Thus, as shown in Figure 6.12(b), the signal source is converted to an independent current source, I_s, where I_s is obviously V_s/Z_s. Note that the fed back current and the signal current flow in opposite directions and hence, the fed back current subtracts from the source current at the input node of the linear circuit. This situation reflects the negative feedback inferred by the block diagram in Figure 6.1. The source conversion renders the null gain a transimpedance, say Z_{vo}, where in

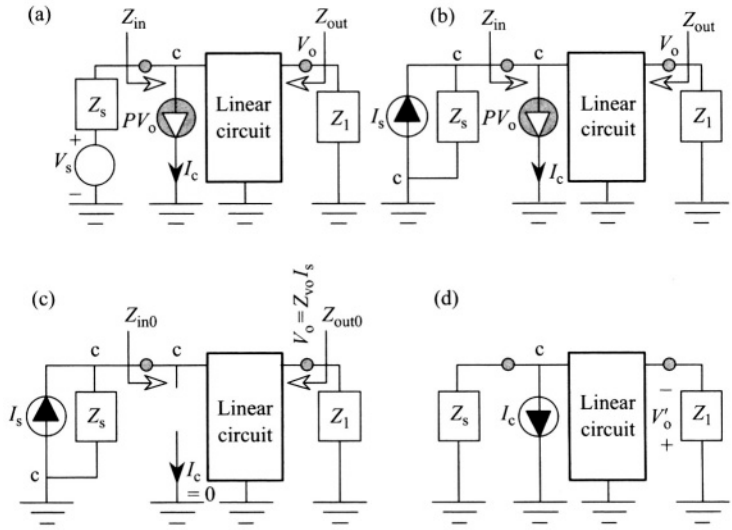


Figure 6.12. (a) Global feedback circuit. (b) Circuit of (a) with signal source replaced by its norton equivalent circuit so that signal and feedback generators are of the same energy type (currents). (c) Circuit used to calculate the null parameter transimpedance. (d) Circuit used to calculate the normalized return ratio with respect to parameter P.

concert with the definition of a null parameter gain and Figure 6.12(c),

$$Z_{vo} = \left.\frac{V_o}{I_s}\right|_{P=0} \tag{6.63}$$

As is suggested by Figure 6.12(d), the normalized return ratio derives from (1) nulling, or open circuiting, the applied independent signal current source, (2) replacing the PV_o dependent source by an independent generator, I_c, and (3) computing the ratio of the resultant phase inverted output voltage, $V'_o = -V_o$ to I_c. But since I_c is applied across the same input port to which I_s is applied, I_c reflects a polarity opposite to that of I_s, and V'_o is a phase inverted version of V_o, $Q_s(\cdot)$ is identical to the previously determined transimpedance, Z_{vo}. This is to say that

$$Q_s(Z_s, Z_l) = \left.\frac{V'_o}{I_c}\right|_{I_s=0} \equiv \left.\frac{V_o}{I_s}\right|_{P=0} = Z_{vo} \tag{6.64}$$

Resultantly, the closed loop transimpedance, Z_{vc}, is

$$Z_{vc} = \frac{V_o}{I_s} = \left[\frac{Z_{vo}}{1 + PQ_s(Z_s, Z_l)}\right] = \left[\frac{Z_{vo}}{1 + PZ_{vo}}\right] \tag{6.65}$$

whose mathematical form is precisely the same as the gain expression for the system abstraction of global feedback in Figure 6.1. Since $I_s = V_s/Z_s$, the

corresponding closed loop voltage gain is

$$A_{vc} = \frac{V_o}{V_s} = \left[\frac{Z_{vo}/Z_s}{1 + PZ_{vo}}\right] \tag{6.66}$$

Controlling feedback variable is the branch variable of the controlled port. Consider Figure 6.13(a) in which there is no obvious feedback from k-th to c-th ports but instead, a branch admittance, say Y_c, is incident with the c-th port. As illustrated in Figure 6.13(b), this branch topology is equivalent to a voltage controlled current source, $Y_c V_c$, where the controlling voltage, V_c, is the voltage established across the c-th port. By comparison with Figure 6.5(b), the latter figure shows that the feedback parameter, P, is effectively the branch admittance, Y_c, while the controlling voltage, V_k, is the voltage, V_c, developed across the controlled port.

The gain, input impedance, and output impedance of the network in Figure 6.13(a) subscribe to (6.46), (6.58), and (6.59), respectively. The zero parameter gain, A_{vo}, input impedance, Z_{in0}, and output impedance, Z_{out0}, are evaluated by open circuiting the branch admittance, Y_c, as per Figure 6.14(a). Note that open circuiting Y_c in Figure 6.13(a) is equivalent to nulling the controlled generator, $Y_c V_c$, in Figure 6.13(b).

The evaluation of the normalized return ratio, $Q_s(\cdot)$, mirrors relevant previous computational procedures. In particular, and as is delineated in Figure 6.14(b), (1) the independent signal source is set to zero, (2) the dependent current generator, $Y_c V_c$, across the c-th network port is replaced by an independent current source, I_c, and (3) the ratio of the negative of V_c, indicated as V_c', to I_c is calculated. However, this ratio is identically the Thévenin

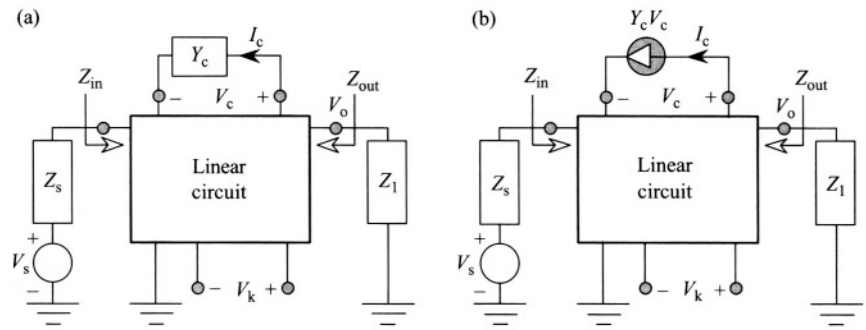


Figure 6.13. (a) Feedback circuit entailing a simple branch admittance incident with a network port. (b) The circuit of (a) with the subject branch admittance represented by a voltage controlled current source.

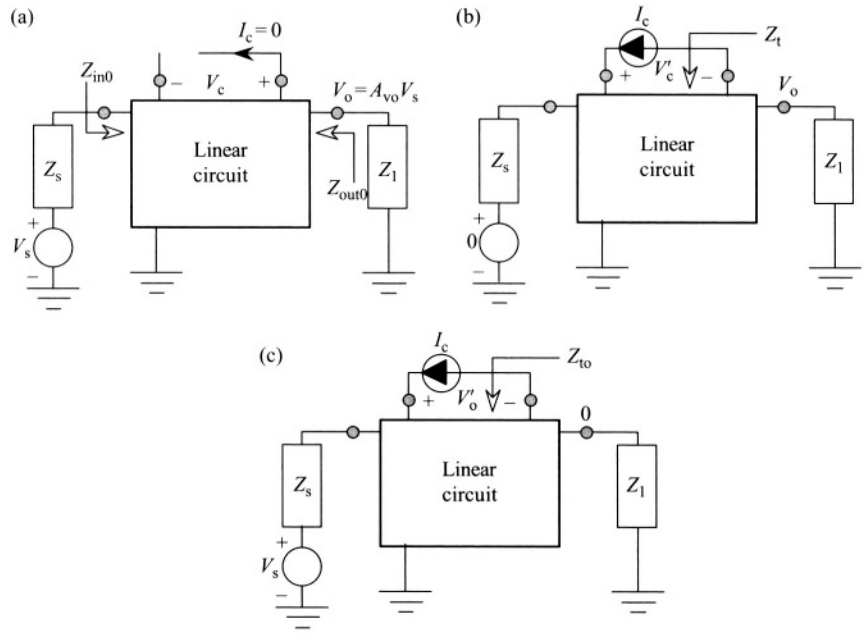


Figure 6.14. (a) The computation of the null gain for the circuit of Figure 6.13(a). (b) The computation of the normalized return ratio with respect to admittance Y_c in Figure 6.13(a). (c) The computation of the normalized null return ratio.

impedance, $Z_t(Z_s, Z_l)$, "seen" by admittance Y_c. Accordingly,

$$Q_s(Z_s, Z_l) = \left.\frac{-V_c}{I_c}\right|_{V_s=0} = \left.\frac{V'_c}{I_c}\right|_{V_s=0} \tag{6.67}$$

Similarly, and as highlighted in Figure 6.14(c), the normalized null return ratio, $Q_r(\cdot)$, is the null Thévenin impedance, $Z_{to}(Z_s, Z_l)$, seen by Y_c; that is, the normalized null return ratio is the Thévenin impedance facing Y_c under the condition of an output response constrained to zero. It follows from (6.46), (6.58) and (6.59) that the closed loop voltage gain, A_{vc}, the driving point input impedance, Z_{in}, and the driving point output impedance, Z_{out}, are given respectively by

$$A_{vc} = \frac{V_o}{V_s} = A_{vo}\left[\frac{1 + T_r(P, Z_s, Z_l)}{1 + T_s(P, Z_s, Z_l)}\right] = A_{vo}\left[\frac{1 + Y_c Z_{to}(Z_s, Z_l)}{1 + Y_c Z_t(Z_s, Z_l)}\right] \tag{6.68}$$

$$Z_{in} = Z_{in0}\left[\frac{1 + Y_c Z_{to}(0, Z_l)}{1 + Y_c Z_t(\infty, Z_l)}\right] \tag{6.69}$$

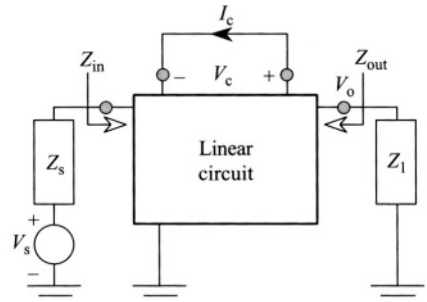


Figure 6.15. Feedback circuit in which the critical parameter is a branch short circuit.

and

$$Z_{out} = Z_{out0}\left[\frac{1 + Y_c Z_{to}(Z_s, 0)}{1 + Y_c Z_t(Z_s, \infty)}\right] \tag{6.70}$$

Two special circumstances can be extrapolated from the case just considered. The first entails a short circuit across the controlled c-th port, as is depicted in Figure 6.15. Recalling Figure 6.13(a), this situation corresponds to $Y_c = \infty$, whence (6.68)–(6.70) become

$$A_{vc} = \frac{V_o}{V_s} = A_{vo}\left[\frac{Z_{to}(Z_s, Z_l)}{Z_t(Z_s, Z_l)}\right] \tag{6.71}$$

$$Z_{in} = Z_{in0}\left[\frac{Z_{to}(0, Z_l)}{Z_t(\infty, Z_l)}\right] \tag{6.72}$$

and

$$Z_{out} = Z_{out0}\left[\frac{Z_{to}(Z_s, 0)}{Z_t(Z_s, \infty)}\right] \tag{6.73}$$

These three expressions imply that for the case of a short circuit critical parameter, the gain, input impedance and output impedance are simply scaled versions of their respective null (meaning open circuited c-th port branch) values. The scale factors are related to the ratio of the null Thévenin impedance to the Thévenin impedance facing the short circuited branch of interest.

The second of the aforementioned two special circumstances involves a capacitive branch admittance connected to the c-th port of a memoryless network driven by a source whose internal impedance is resistive and terminated in a load resistance, as abstracted in Figure 6.16. With reference to Figure 6.13(a), the condition at hand yields $Y_c = sC$, which can be substituted directly into (6.68)–(6.70). But in addition, the memoryless nature of the network to which capacitance C is,connected gives Thévenin and null Thévenin impedances that

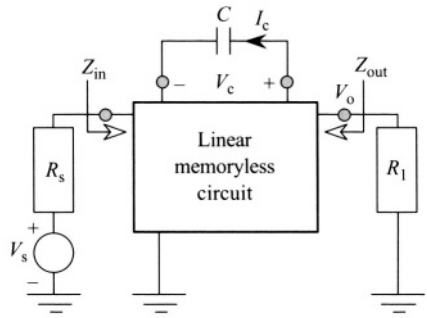


Figure 6.16. Feedback circuit in which the critical parameter is a capacitive branch admittance.

are actually Thévenin resistances, $R_t(\cdot)$ and $R_{to}(\cdot)$, "seen" by the subject branch capacitance. It follows that

$$A_{vc} = \frac{V_o}{V_s} = A_{vo}\left[\frac{1 + sCR_{to}(R_s, R_l)}{1 + sCR_t(R_s, R_l)}\right] \tag{6.74}$$

$$Z_{in} = Z_{in0}\left[\frac{1 + sCR_{to}(0, R_l)}{1 + sCR_t(\infty, R_l)}\right] \tag{6.75}$$

and

$$Z_{out} = Z_{out0}\left[\frac{1 + sCR_{to}(R_s, 0)}{1 + sCR_t(R_s, \infty)}\right] \tag{6.76}$$

The pole incurred in the voltage transfer function by the branch capacitance lies at $s = -1/CR_t(R_s, R_l)$, while the zero lies at $s = -1/CR_{to}(R_s, R_l)$. Observe that the pole and zero frequencies associated with the input and output impedances are not necessarily respectively identical, nor are they respectively identical to those of the voltage transfer relationship.

Example 6.3. The operational amplifier (op-amp) circuit shown in Figure 6.17(a) exploits the resistance, R_f, to implement shunt–shunt global feedback. The signal source is a voltage, V_s, whose Thévenin resistance is R_s, and the load termination is a resistance of value R_l. The simplified dominant pole equivalent circuit of the op-amp is given in Figure 6.17(b), where A_o symbolizes the positive and frequency-invariant open loop gain, R_i is the effective input resistance, C_i is the effective input capacitance, and R_o is the Thévenin equivalent output resistance of the op-amp. Determine expressions for the open loop voltage gain, $A_{ol}(s)$, of the circuit, the 3-dB bandwidth, B_{ol}, of the open loop circuit, the loop gain, $T(s, R_s, R_l)$, the closed loop voltage gain of the entire amplifier, $A_{cl}(s)$, and the 3-dB bandwidth, B_{cl}, of the closed loop. Also, derive approximate expressions for the low frequency closed loop driving point

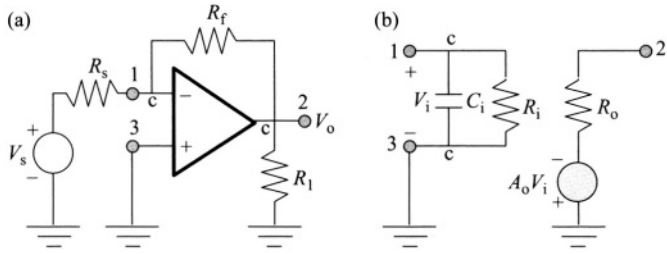


Figure 6.17. (a) Operational amplifier circuit using shunt–shunt feedback. (b) The approximate equivalent circuit of the operational amplifier.

input and output impedances, $Z_{in}(s)$ and $Z_{out}(s)$, respectively. The approximations invoked should reflect the commonly encountered op-amp situation of large open loop gain, large input resistance, and small output resistance.

Solution 6.3.

Comment. There are several ways to approach this problem. For example, the problem solution can be initiated by taking the conductance, G_f, associated with the resistance, R_f, as the feedback parameter. The gain for $G_f = 0$, which open circuits the feedback path, can be evaluated, as can the return ratio and null return ratio with respect to G_f. To this end, note that the normalized return ratio is the impedance "seen" by G_f with zero source excitation, while the normalized null return ratio is the impedance seen by G_f with the output voltage response nulled. Equations (6.46)–(6.49) can then be applied to address the issues of this problem. Alternatively, the feedback parameter can be taken as the short circuit interconnect between the feedback resistor, R_f, and either the input or the output port of the op-amp, whereupon (6.71)–(6.73) can be invoked. The strategy adopted herewith entails the replacement of resistance R_f by its two port equivalent circuit. As is to be demonstrated, this strategy unambiguously stipulates the analytical nature of the open loop gain, the loop gain, and even the feedforward factor associated with R_f.

1 Figure 6.18(a) repeats the circuit displayed in Figure 6.17(a) but additionally, it delineates the voltage (with respect to ground) and current, V_o and I_2, at the input port of the feedback resistance, as well as the voltage and current, V_i and I_1, at the feedback input port. Clearly,

$$I_1 = G_f(V_i - V_o) = -I_2$$

which suggests that the feedback resistance, R_f, can be modeled as the two port network offered in Figure 6.18(b). When coalesced with the op-amp model of Figure 6.17(b), this two port representation allows the circuit of Figure 6.18(a) to be modeled as the equivalent circuit shown in Figure 6.18(c). In the latter

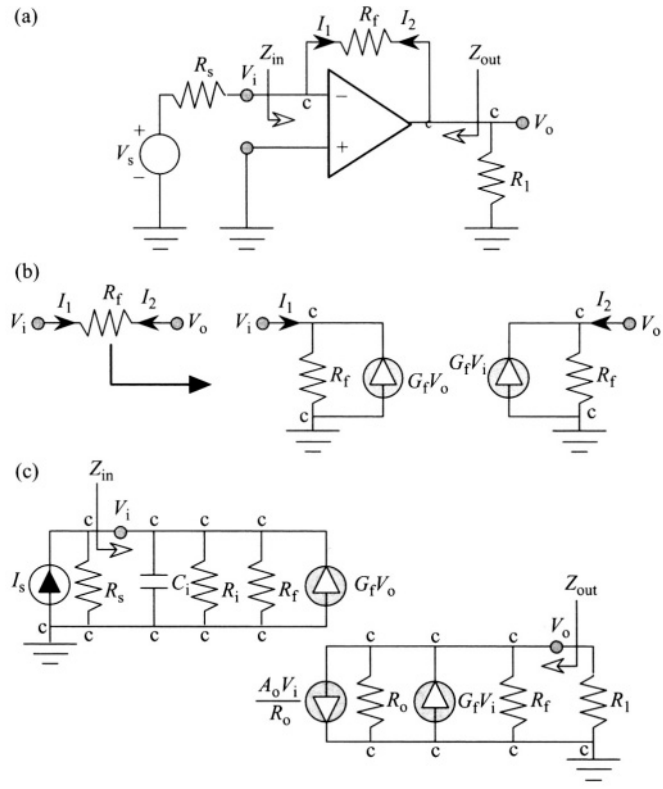


Figure 6.18. (a) Amplifier of Figure 6.17 with voltages and currents pertinent to the feedback resistance, R_f, delineated. (b) Two port model of the feedback subcircuit. (c) Equivalent circuit of the entire amplifier in (a).

structure, the output port of the op-amp has been modeled by a Norton equivalent circuit to facilitate analytical computations. The signal source circuit has also been replaced by its Norton equivalent circuit, where

$$I_s = \frac{V_s}{R_s} = G_s V_s$$

2 The model in Figure 6.18(c) illuminates the presence of global feedback in the form of the current generator, $G_f V_o$, across the network input port. It follows that the feedback parameter (symbolized as P in earlier discussions) is $P = G_f$. The model at hand also shows that feedforward through the feedback resistance is incurred by way of the current generator, $G_f V_i$, at the output port. If the feedback term is set to zero, the resultant model is the open loop equivalent circuit submitted in Figure 6.19(a). It is important to understand that although this structure is an open loop model, its parameters nonetheless include the

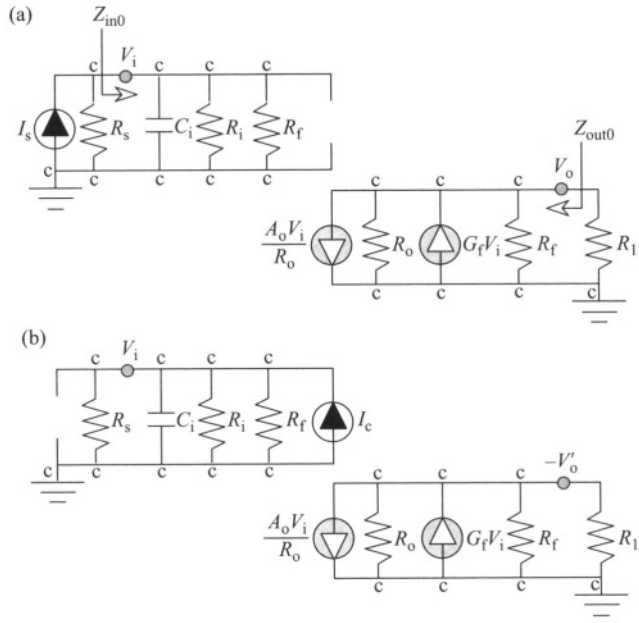


Figure 6.19. (a) Equivalent circuit used to determine the open loop values of transimpedance and driving point input and output impedances for the circuit in Figure 6.17(a). (b) Equivalent circuit used to determine the normalized return ratio with respect to conductance G_f for the amplifier in Figure 6.17(a).

resistance, R_f, which accounts for feedback subcircuit loading of the amplifier input port, resistance, R_f, which incorporates output port loading caused by the feedback network, and the generator, $G_f V_i$, which emulates feedforward phenomena associated with the feedback subcircuit. A straightforward analysis of the circuit in Figure 6.19(a) delivers

$$I_s = (G_s + G_i + G_f + sC_i)V_i$$

and

$$V_o = -\frac{(A_o/R_o - G_f)V_i}{G_o + G_f + G_l}$$

It follows that the open loop transimpedance, say $Z_m(s)$, is expressible as

$$Z_m(s) = \frac{V_o}{I_s} = -\frac{Z_m(0)}{1 + sC_i/(G_s + G_i + G_f)}$$

where the magnitude of the zero frequency value of the open loop transimpedance is

$$Z_m(0) = \left(A_o - \frac{R_o}{R_f}\right)\left(\frac{R_f \parallel R_l}{R_o + R_f \parallel R_l}\right)(R_s \parallel R_i \parallel R_f)$$

3 Because $I_s = V_s/R_s$, the open loop voltage gain is seen to be

$$A_{ol}(s) = \frac{V_o}{V_s} = \frac{Z_m(s)}{R_s} = -\frac{A_{ol}(0)}{1 + s/B_{ol}}$$

where the magnitude of the zero frequency open loop voltage gain is

$$A_{ol}(0) = \frac{Z_m(0)}{R_s} = \left(A_o - \frac{R_o}{R_f}\right)\left(\frac{R_f \parallel R_l}{R_o + R_f \parallel R_l}\right)\left(\frac{R_f \parallel R_i}{R_s + R_f \parallel R_i}\right)$$

and

$$B_{ol} = \frac{G_s + G_i + G_f}{C_i} = \frac{1}{(R_s \parallel R_i \parallel R_f)C_i}$$

is the open loop 3-dB bandwidth.

4 Since global feedback prevails, the normalized null return ratio is zero. The circuit appropriate to the determination of the normalized return ratio is offered in Figure 6.19(b), wherein with reference to Figure 6.18(c), the $G_f V_o$ feedback generator is supplanted by an independent current source, I_c, the Norton source current, I_s, is nulled, and the controlling voltage, V_o, for the feedback generator, is replaced by its phase inverted value, $-V_o'$. Since the original signal voltage source has been replaced by its Norton equivalent circuit, both the Norton signal source and the feedback generator are current sources incident with the amplifier input port. This renders simple the computation of the normalized return ratio; in particular, an inspection of the circuit in Figure 6.19(b) confirms

$$Q_s(s, R_s, R_l) = -Z_m(s)$$

whence the loop gain of the amplifier is

$$T(s, R_s, R_l) = G_f Q_s(s, R_s, R_l) = -G_f Z_m(s) = \frac{T(0, R_s, R_l)}{1 + s/B_{ol}}$$

where the zero frequency loop gain is

$$T(0, R_s, R_l) = G_f Z_m(0) = \left(A_o - \frac{R_o}{R_f}\right)\left(\frac{R_f \parallel R_l}{R_o + R_f \parallel R_l}\right)\left(\frac{R_s \parallel R_i}{R_f + R_s \parallel R_i}\right)$$

5 The preceding analytical stipulations render a closed loop transimpedance of

$$Z_{mc}(s) = \frac{V_o}{I_s} = \frac{Z_m(s)}{1 + T_s(s, R_s, R_l)}$$

which is expressible as

$$Z_{mc}(s) = -\frac{Z_{mc}(0)}{1 + s/B_{cl}}$$

where the magnitude of the zero frequency amplifier transimpedance is

$$Z_{mc}(0) = \frac{Z_m(0)}{1 + T(0, R_s, R_l)}$$

and

$$B_{cl} = [1 + T(0, R_s, R_l)]B_{ol}$$

is the closed loop 3-dB bandwidth. It follows that the closed loop voltage gain is

$$A_{cl}(s) = \frac{V_o}{V_s} = G_s Z_{mc}(s) = -\frac{Z_{mc}(0)/R_s}{1 + s/B_{cl}}$$

Comment. For most operational amplifier networks like that depicted in Figure 6.17(a), the zero frequency loop gain, $T(0, R_s, R_l) = G_f Z_m(0)$, is much larger than one. This means that the zero frequency closed loop gain collapses to the well-known relationship,

$$A_{cl}(0) = -\frac{Z_{mc}(0)}{R_s} = -\frac{Z_m(0)}{[1 + T(0, R_s, R_l)]R_s} \approx -\frac{Z_m(0)}{G_f Z_m(0) R_s} = -\frac{R_f}{R_s}$$

Moreover, the open loop op-amp gain, A_o, is invariably much larger than the resistance ratio. R_o/R_f, and the op-amp input and output resistances easily satisfy the inequalities, $R_i \gg R_s \parallel R_f$ and $R_o \ll R_f \parallel R_l$. Thus, the zero frequency loop gain closely approximates

$$T(0, R_s, R_l) \approx \frac{A_o}{1 + |A_{cl}(0)|}$$

In turn, the closed loop bandwidth of the circuit becomes

$$B_{cl} \approx T(0, R_s, R_l)B_{ol} \approx \frac{A_o}{R_f C_i}$$

6 The closed loop input impedance can be found through use of (6.58), while (6.59) applies to a determination of the closed loop output impedance. An inspection of Figure 6.19(a) provides a low-frequency open loop input resistance of

$$Z_{in0} = R_i \parallel R_f \approx R_f$$

and an open loop output resistance of

$$Z_{out0} = R_o \parallel R_f \approx R_o$$

The results of the third and fourth computational steps above confirm

$$T(0, 0, R_l) = 0$$

$$T(0, R_s, 0) = 0$$

$$T(0, \infty, R_l) = \left(A_o - \frac{R_o}{R_f}\right)\left(\frac{R_f \parallel R_l}{R_o + R_f \parallel R_l}\right)\left(\frac{R_i}{R_f + R_i}\right) \approx A_o'$$

and

$$T(0, R_s, \infty) = \left(A_o - \frac{R_o}{R_f}\right)\left(\frac{R_f}{R_o + R_f}\right)\left(\frac{R_s \parallel R_i}{R_f + R_s \parallel R_i}\right) \approx \frac{A_o}{1 + |A_{cl(0)}|}$$

Thus, the approximate low frequency closed loop I/O impedances are

$$Z_{in} \approx \frac{R_f}{A_o}$$

and

$$Z_{out} \approx [1 + |A_{cl}(0)|]\frac{R_f}{A_o}$$

Comment. Although the low frequency output resistance of the circuit in Figure 6.18(a) is somewhat larger than the low frequency input resistance, both the input and the output resistances are small owing to very large open loop op-amp gain. Although the circuit is commonly used as a voltage amplifier, the small I/O resistance levels make the amplifier more suitable for transimpedance signal processing.

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Chapter 7

ANALOG AMPLIFIERS ARCHITECTURES: GAIN BANDWIDTH TRADE-OFFS

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7.1. Introduction

Amplifiers with high open-loop gain (operational amplifiers) are frequently encountered in analog signal processing circuits, since the application of negative feedback enables numerous transfer functions to be implemented. The traditional voltage operational amplifier (op-amp) architecture is still the most widely used topology for implementing high gain analog amplifiers, but in fact this architecture is just one of a range of possible implementations. This chapter investigates the relationship between amplifier open-loop topology and the resulting closed-loop performance, in particular focusing on the resulting closed-loop bandwidth. Trade-offs in performance across different open-loop architectures are shown to depend on the particular closed-loop application, and analysis demonstrates that many ideas such as fixed gain–bandwidth product are not inherent to negative feedback amplifier circuits, but result from the choice of amplifier architecture within a particular application.

The concept of an ideal amplifier dates back many decades, and early theories demonstrated that the general definition of an ideal amplifier could be satisfied by various alternative topologies; there was no fundamental reason why one particular architecture should perform better than another. However, when integrated circuit technology was in its infancy, IC designers were very limited in terms of available components, and this made it impractical to implement certain amplifier topologies. As process technology matured new features were integrated onto silicon in response to designers' requirements; for example, the provision of integrated capacitors and polysilicon resistors with high sheet resistivity. These circuit-driven advances in technology allowed earlier designs to be refined, giving enhanced performance and efficiency.

IC processing techniques have now evolved to the point where many high-performance and "exotic" devices are being integrated. This in turn has led to a renewed interest in circuit design techniques which were previously limited by the technology available – essentially we are now seeing technology-driven advances in circuit design. An example is the development of "current-mode"

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techniques [1], many of which have only become practically feasible with the development of true complementary bipolar processes.

In this chapter, we revisit some of the original amplifier concepts in the light of recent advances in process technology, and show that many circuits recently proposed in response to particular system requirements are practical implementations of these original concepts. The chapter begins by examining early theories of ideal amplifiers, and then discusses a diverse range of practical amplifier topologies which have since been proposed. By relating these practical circuits back to the early theories, we can classify and generalize the relationships between them. In particular, the benefits associated with each amplifier topology become immediately clear, and the scope for future development is also highlighted.

7.2. Early Concepts in Amplifier Theory

7.2.1. The Ideal Amplifier

In 1954, Tellegen introduced the concept of an "ideal amplifier" [2] as a general building block for the implementation of linear and nonlinear analog systems. This ideal device was a two-port with four associated variables – V_1, I_1 at the input port and V_2, I_2 at the output port. When represented geometrically in four-dimensional space the device could be defined by the planes $V_1 = 0$, $I_1 = 0$ and V_2, I_2 arbitrary. The amplifier would, therefore, exhibit an infinite power gain between the input and output ports.

In 1964, Carlin proposed the concept of the "nullor" [3], which was a two-port comprising an input nullator and an output norator, as shown in Figure 7.1. The port voltage and current of a nullator are always zero, while the port voltage and current of a norator can independently take any value; both components, therefore, have an undefined impedance. The nullor satisfies the definition of an ideal amplifier as given by Tellegen in [2].

As an electrical circuit component, the transfer properties of the nullor only become well defined if an external network provides for feedback from the output to the input port, as shown in Figure 7.2. The output variables (V_2, I_2)

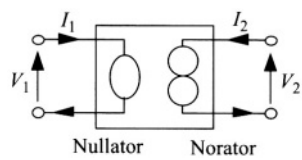


Figure 7.1. The nullor figure.

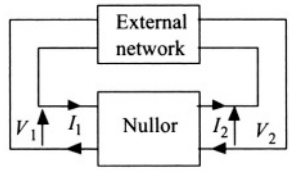


Figure 7.2. Nullor with feedback network.

will then be determined by the external network in such a way that the input conditions $(V_1 = 0, I_1 = 0)$ are satisfied.

Depending on the nature of the external feedback network, many linear and nonlinear analog transfer functions can be implemented. In addition, the external network can usually be chosen such that the resulting transfer function is independent of any source or load. The nullor is thus particularly suitable for separating two stages of an analog system which are mismatched in terms of impedance, thereby eliminating loading effects and allowing stages to be easily cascaded.

7.2.2. Reciprocity and Adjoint Networks

Tellegen's Reciprocity Theorem [4] defines a network as reciprocal if the same transfer function is obtained when the input excitation and output response are interchanged. Many useful network theorems can be derived from the principle of reciprocity, which facilitate, for example, the calculation of energy distribution and dissipation and network sensitivities [5]. A network which satisfies the definition of reciprocity is always composed of components which are themselves reciprocal (generally passive elements such as resistors, capacitors, inductors). Networks containing active components generally do not satisfy the criteria for reciprocity, so Bordewijk extended the scope of the theorem by defining the concept of inter-reciprocity [6]. Two networks are said to be inter-reciprocal if they jointly satisfy the condition of reciprocity; that is, if the two networks give the same transfer function under an interchange of excitation and response. Clearly any reciprocal network will be inter-reciprocal with itself.

An inter-reciprocal network N_2 is known as the "adjoint" of the original network N_1. Since a network and its adjoint are inter-reciprocal, they are exactly equivalent in terms of signal transfer, sensitivity, power dissipation etc. The properties of the adjoint network can, therefore, be inferred from the properties of the original, without requiring any further analysis. The adjoint network can be found by following rules given by Tellegen [7], and summarized by Director [8]; first construct a replica of the original network, then go through this replica, replacing each element with its adjoint. A resistor is left alone

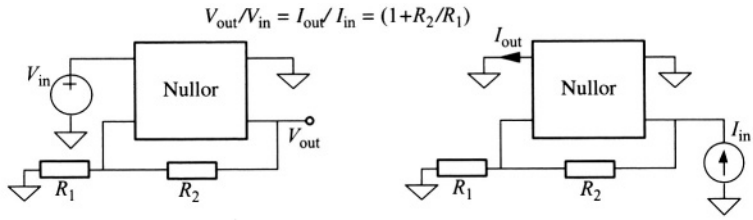


Figure 7.3. Adjoint (inter-reciprocal) networks.

(i.e. it is replaced by itself), and similarly capacitors and inductors are left alone. A voltage source becomes a short circuit (and vice versa), while a current source is replaced by an open circuit (and vice versa). Following these rules, a nullor is replaced by a nullor, but with the input and output ports interchanged (thus, the nullor is "self inter-reciprocal" or "self adjoint"). Adjoint networks are also known as "dual" networks, since they are equivalent under an interchange of voltage and current signals. Figure 7.3 illustrates the adjoint network principle.

7.2.3. The Ideal Amplifier Set

The nullor is the most general case of a universal ideal amplifier, but in practice the undefined input and output resistance levels make this device difficult to implement. Tellegen recognized this problem and proposed a set of four ideal amplifiers [2], each with a well-defined input resistance (R_{in}) and output resistance (R_{out}). These four ideal amplifiers are:

1 The Voltage Amplifier or Voltage-Controlled Voltage Source (VCVS). This device has an open circuit input port ($R_{in} = \infty$), a short circuit output port ($R_{out} = 0$), and an open-loop voltage gain ($V_2 = A_v V_1$).

2 The Current Amplifier or Current-Controlled Current Source (CCCS). This device has a short circuit input port ($R_{in} = 0$), an open circuit output port ($R_{out} = \infty$), and an open-loop current gain ($I_2 = A_i I_1$).

3 The Transresistance Amplifier or Current-Controlled Voltage Source (CCVS). This device has short circuit input and output ports ($R_{in} = R_{out} = 0$), and an open-loop transresistance gain ($V_2 = R_t I_1$).

4 The Transconductance Amplifier or Voltage-Controlled Current Source (VCCS). This device has open circuit input and output ports ($R_{in} = R_{out} = \infty$), and an open-loop transconductance gain ($I_2 = G_t V_1$).

For each amplifier, the available power gain is infinite, and the output voltage or output current is directly proportional to the input voltage or input current, independent of any loading effects. Each amplifier differs from the nullor in

the respect that they are no longer "self inter-reciprocal"; however, they can be arranged into dual or adjoint pairs. The ideal voltage and current amplifiers form one dual pair (provided that $A_v = A_i$, and the input and output ports are interchanged), and the ideal transresistance and transconductance amplifiers form another dual pair (provided that $R_t = G_t$, and the input and output ports are interchanged).

7.3. Practical Amplifier Implementations

The amplification of signals is perhaps the most fundamental operation in analog signal processing, and in the early days amplifier circuit topologies were generally optimized for specific applications. However, the desirability of a general purpose high-gain analog amplifier was recognized by system designers and IC manufacturers alike, since the application of negative feedback allows many analog circuit functions (or "operations") to be implemented accurately and simply. A general purpose device would also bring economies of scale, reducing the price and allowing ICs to be used in situations where they may have previously been avoided on the basis of cost. "Op-amps" were thus featured among the first generation of commercially available ICs, and the development of these practical devices is discussed in the following section.

7.3.1. Voltage Op-Amps

Of the four amplifier types described by Tellegen, the voltage op-amp (VCVS) has emerged as the dominant architecture almost to the exclusion of all others, and this situation has a partly historical explanation. Early high-gain amplifiers were implemented using discrete thermionic valves which were inherently voltage-controlled devices, and a controlled voltage output allowed stages to be easily cascaded. The resulting voltage op-amp architectures were translated to silicon with the development of integrated circuit technologies, and the device has since become ubiquitous to the area of analog signal processing. The architecture of the voltage op-amp has several attractive features; for example, the differential pair input stage is very good at rejecting common-mode signals. In addition a voltage op-amp only requires a single-ended output to simultaneously provide negative feedback and drive a load, and the implementation of a single-ended output stage is a much simpler task than the design of a fully differential or balanced output.

On the negative side, the architecture of the voltage op-amp produces certain inherent limitations in both performance and versatility. The performance of the voltage op-amp is typically limited by a fixed gain–bandwidth product and a slew rate whose maximum value is determined by the input stage bias current. The versatility of the voltage op-amp is constrained by the single-ended output, since the device cannot be easily configured in closed-loop to provide

a controlled output current (this feature requires the provision of a differential current output). The voltage op-amp is, therefore, primarily intended for the implementation of closed-loop voltage-processing (or "voltage-mode") circuits, and as a result most analog circuits and systems have been predominantly voltage driven. Since it is often desirable to maximize signal swings while minimizing the total power consumption, voltage-mode circuits generally contain many high impedance nodes to minimize the total current consumption.

Alongside this voltage-mode mainstream, the investigation and implementation of so-called "current-mode" circuits has progressed. Circuits are classified as current-mode if the signals being processed are represented by time-varying currents. To minimize the total power consumption, impedance levels are kept low to reduce the voltage swings throughout the circuit. Certain applications benefit from operating in the current-mode domain rather than in voltage-mode [1]; for example, in a predominantly capacitive environment, speed is maximized by driving currents rather than voltages. Amplifier architectures which allow the provision of a controlled output current are, therefore, useful for current-mode applications. Figure 7.4 summarizes some of the "novel" amplifier topologies and design techniques which have been proposed in response to the limitations in voltage op-amp performance and versatility mentioned above. These practical circuits are discussed briefly in the following sections; the reader is referred to the appropriate references if a more detailed description is required.

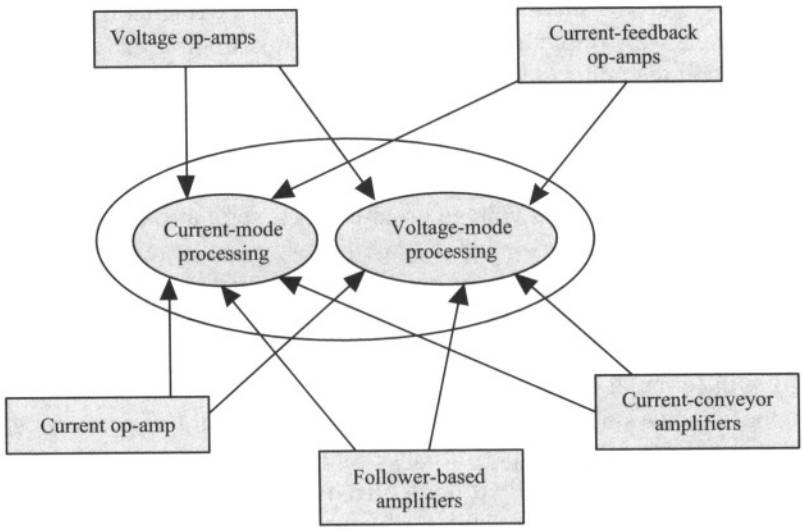


Figure 7.4. Practical amplifier architectures for analog signal processing.

7.3.2. Breaking the Gain–Bandwidth Conflict

The fixed gain–bandwidth product of the voltage op-amp limits the frequency performance of the device in situations where a high closed-loop gain is required. The development of techniques to overcome this gain–bandwidth conflict are described in the following sections.

Current-feedback op-amps. The current-feedback op-amp is a device which has emerged as a high-speed alternative to the voltage op-amp [9]. The architecture of this device comprises a transresistance op-amp (CCVS) with an additional input voltage follower (VF) as shown in Figure 7.5. An ideal VF has an infinite input resistance, an output resistance of zero, and unity voltage gain. The current-feedback op-amp thus has one high-resistance input (+), one low-resistance input (–), and a transresistance gain $V_{out}/I_{in}(-) = R_t$.

The current-feedback op-amp is intended to be configured in closed-loop in much the same way as a conventional voltage op-amp, but with voltage-sampling current-feedback applied from the output back to the low resistance input. The resulting closed-loop circuit has a bandwidth which is determined by the feedback resistor R_2, leaving R_1 free to independently set the gain, and there is no fixed gain–bandwidth product.

The internal architecture of a typical current-feedback op-amp contains both npn and pnp transistors in the signal path, and so the commercial availability of this device has resulted from the development of true complementary bipolar processes, with both vertical pnps and npns. As well as achieving closed-loop bandwidth independent of closed-loop gain, the current-feedback op-amp has a much higher slew-rate capability than a conventional voltage op-amp. The tail current of the input stage differential pair puts an upper limit on the

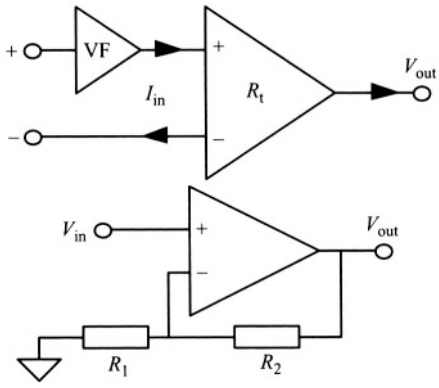


Figure 7.5. Current-feedback op-amp (open-loop and closed-loop).

slew rate of most voltage op-amps; in the current-feedback op-amp there is no such limiting factor, and slew rates of $1000\,\mathrm{V}/\mu\mathrm{s}$ are commonly quoted for commercial devices [10].

Follower-based amplifiers. The fixed gain–bandwidth product of the voltage op-amp results from the application of negative voltage-sampling voltage-feedback. An alternative approach, proposed by Bel [11] and later extended by Toumazou [12], was to use cascaded voltage followers (VFs) and current followers (CFs) to implement an open-loop amplifier architecture. An ideal VF has an infinite input resistance (thus $I_{\mathrm{in}} = 0$), zero output resistance, and unity voltage gain. Conversely an ideal CF has an input resistance of zero (thus $V_{\mathrm{in}} = 0$),an infinite output resistance, and unity current gain. Figure 7.6 shows a follower-based voltage amplifier; the bandwidth of this circuit will be determined by the frequency response of the VFs and CFs.

Current-conveyor amplifiers. The second-generation current conveyor (CCII) was proposed by Sedra and Smith in 1970 as a versatile building block for analog signal processing [13]. This device can be described as a combined VF and CF as shown in Figure 7.7, thus $V_{\mathrm{X}} = V_{\mathrm{Y}}$ and $I_{\mathrm{Z}} = I_{\mathrm{X}}$. The current conveyor can be used to achieve voltage amplification in much the same way as the follower-based amplifier circuits described above. Figure 7.8 shows a CCII-based voltage amplifier where the second current conveyor provides current drive to the load.

Wilson [14] has also demonstrated how the current conveyor can be configured with negative feedback to implement voltage amplifiers with bandwidth

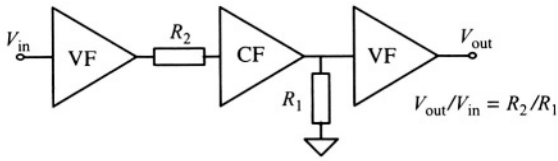


Figure 7.6. Follower-based voltage amplifier.

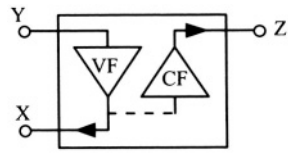


Figure 7.7. The current conveyor.

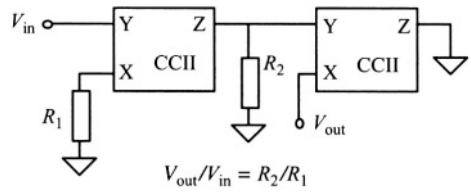


Figure 7.8. Conveyor-based voltage amplifier.

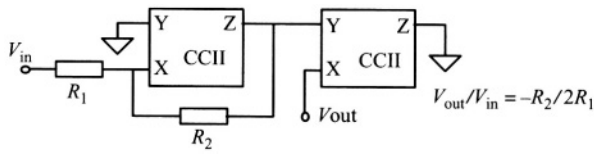


Figure 7.9. Closed-loop conveyor amplifier.

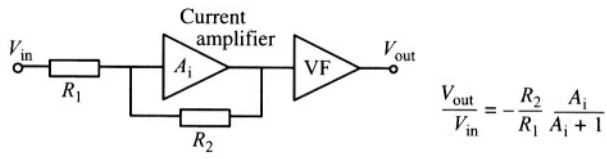


Figure 7.10. Voltage amplifier implemented using a CCCS.

independent of gain, as shown in Figure 7.9. In this case, the first current conveyor is being used as a unity gain current amplifier since the voltage input node Y is grounded. This circuit can, therefore, be recognized as an implementation of a principle proposed earlier by Allen [15], whereby a current amplifier is used to implement voltage-mode circuits with gain-independent bandwidth (see Figure 7.10). If the amplifier has a high current gain (A_i) then $V_o/V_{in} \approx -R_2/R_1$, while if $A_i = 1$ the gain reduces to $-R_2/2R_1$.

In the circuits of Figures 7.6–7.10, current-output devices have been used to implement voltage-mode circuits with gain-independent bandwidth. In each case a single-ended current output is used; no balanced amplifier output stage needs to be designed.

7.3.3. Producing a Controlled Output Current

The implementation of a closed-loop circuit with a controlled output current requires an amplifier with a differential current output, to permit the application of current-sampling negative feedback. For a systems designer to whom no current op-amp is available, an alternative is to modify the voltage op-amp to

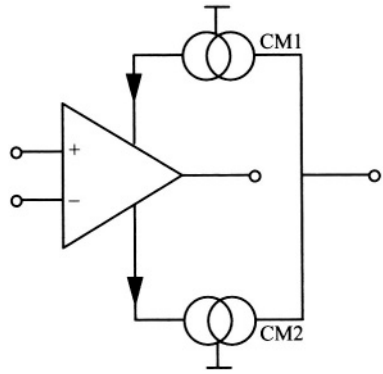


Figure 7.11. Voltage op-amp with supply-current-sensing.

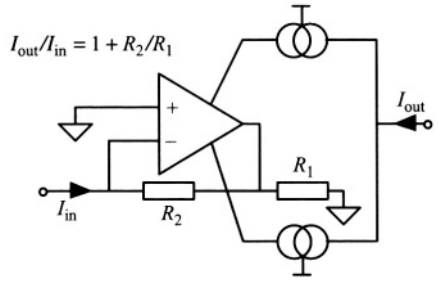


Figure 7.12. Current amplifier.

enable it to drive current loads, and several ingenious circuits which do exactly this function have been developed. The most successful have been based on the principle of supply-current-sensing [16,17]; this technique makes use of the fact that the current flowing from the output of the op-amp must be drawn through the supply leads. Current mirrors are thus used to sense the phase split output current via the op-amp's supply leads, as shown in Figure 7.11. The current mirror outputs are then recombined to provide the required single high impedance bipolar output. Huijsing has coined the term "Operational Mirrored Amplifier" to describe this circuit [18].

By applying negative feedback around the op-amp, circuits with well-defined current gain may be implemented as shown in Figure 7.12. The resulting closed-loop bandwidth of this circuit is found to be independent of the closed-loop gain, and is equal to the gain–bandwidth product of the op-amp (provided that the closed-loop current gain is greater than unity). The supply-current-sensing technique has also been applied to the current-feedback op-amp to implement the so-called "Operational Floating Conveyor" [19]. This device combines the

versatility of a differential current output with the high slew rate and bandwidth capabilities of the current-feedback op-amp architecture.

Although the supply-current-sensing technique allows the implementation of circuits with controlled current outputs, these "floating" amplifiers cannot really be described as current op-amps (CCCS). Following Tellegen's original definition, a CCCS amplifier has a fully differential current output with infinite output resistance, and this type of architecture has proved generally difficult to implement. However, technological developments, such as complementary bipolar processing, have led to the recent emergence of true "current op-amp" architectures [1,20].

7.4. Closed-Loop Amplifier Performance

7.4.1. Ideal Amplifiers

The various practical amplifier implementations described in the previous section have been developed in response to particular system requirements, or in an attempt to overcome some performance limitation associated with the more conventional voltage op-amp architecture. Many of these architectures can be recognized as approximations to Tellegen"s ideal amplifier set; for example, amplifiers for voltage-mode processing generally have a high input resistance, while amplifiers for current-mode processing generally have a high output resistance. The differing levels of input and output resistance among the various amplifier types suggests that each might perform differently when presented with the same external network. To investigate this further we return to Tellegen's ideal amplifier set (VCVS, CCCS, VCCS, CCVS), and derive the transfer functions obtained when each amplifier is configured in turn to implement the various closed-loop functions shown in Figure 7.13.

These circuits are chosen for the varying combinations of input source and output drive which they impose on the ideal amplifier. The transfer functions for these circuits are obtained by replacing the ideal amplifier by each of the specific types (VCVS, CCCS etc.) in turn, and the results are summarized in Table 7.1 (note $G = 1 + R_2/R_1$).

This table offers valuable insight into the operation of the various amplifier types, since the relationship between the closed-loop transfer function and the circuit components can be clearly seen. The similarity between certain pairs of entries illustrates the inter-reciprocal mapping between the dual amplifiers (VCVS/CCCS and VCCS/CCVS). For example, circuits 1A and 2B are voltage-mode and current-mode duals, as are circuits 1B and 2A, 3C and 4D etc.

Each single transfer function within the table has been divided into two parts. The first term is dependent only on the external feedback resistors and defines the ideal closed-loop gain (that which would be obtained if the amplifier was

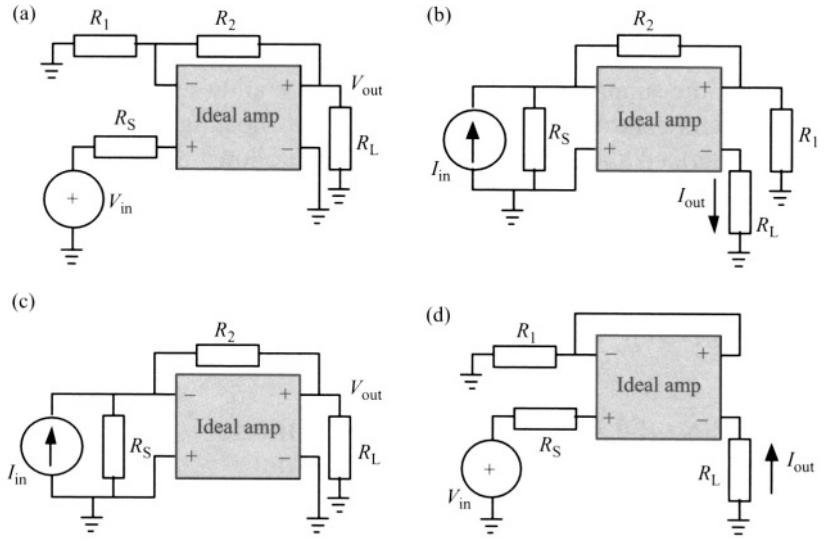


Figure 7.13. Closed-loop amplifier applications. (a) V-to-V converter; (b) I-to-I converter; (c) I-to-V converter; (d) V-to-I converter.

an ideal nullor). The second term is dependent on the open-loop gain of the amplifier and the magnitude of the source and load resistance, in addition to the gain-setting resistor values. To approximate the behavior of an ideal nullor, the closed-loop transfer functions should be entirely independent of both source and load resistance, and this can be achieved if each amplifier has an infinite open-loop gain (i.e. if $A_v = A_i = R_t = G_t = \infty$). The second terms will then become unity, and Table 7.1 will condense to Table 7.2 as shown below.

If each of the four amplifier types have infinite open-loop gain, it is irrelevant which particular type is chosen to implement a particular application, since the resulting closed-loop transfer functions reduce to the same basic form.

7.4.2. Real Amplifiers

The ideal amplifier requirement of infinite open-loop gain is not possible to achieve, and practical devices have open-loop gains which are both finite and frequency dependent. Assume for simplicity that the amplifier open-loop gain $A(s)$ has a single dominant pole which can be written as:

$$A(s) = \frac{A_o}{1 + s/\omega_a} \tag{7.1}$$

Table 7.1. **Closed-loop amplifier transfer functions.**

	(A) V-to-V converter	*(B) I-to-I converter*
(1) VCVS (A_v)	$\left(1+\frac{R_2}{R_1}\right)\cdot\left(\frac{A_v}{A_v+1+R_2/R_1}\right)$	$\left(1+\frac{R_2}{R_1}\right)\cdot\left(\frac{A_v+1/G}{A_v+1+R_2/R_S+R_L/R_1+GR_L/R_S}\right)$
(2) CCCS (A_i)	$\left(1+\frac{R_2}{R_1}\right)\cdot\left(\frac{A_i+1/G}{A_i+1+R_2/R_L+R_S/R_1+GR_S/R_L}\right)$	$\left(1+\frac{R_2}{R_1}\right)\cdot\left(\frac{A_i}{A_i+1+R_2/R_1}\right)$
(3) CCVS (R_t)	$\left(1+\frac{R_2}{R_1}\right)\cdot\left(\frac{R_t}{R_t+R_2+GR_S}\right)$	$\left(1+\frac{R_2}{R_1}\right)\cdot\left(\frac{R_t}{R_t+R_2+GR_L}\right)$
(4) VCCS (G_t)	$\left(1+\frac{R_2}{R_1}\right)\cdot\left(\frac{G_t}{G_t+1/R_1+G/R_L}\right)$	$\left(1+\frac{R_2}{R_1}\right)\cdot\left(\frac{G_t}{G_t+1/R_1+G/R_S}\right)$
	(C) I-to-V converter	*(D) V-to-I converter*
(1) VCVS (A_v)	$(R_2)\cdot\left(\frac{A_v}{A_v+1+R_2/R_S}\right)$	$\left(\frac{1}{R_1}\right)\cdot\left(\frac{A_v+1/G}{A_v+1+R_L/R_1}\right)$
(2) CCCS (A_i)	$(R_2)\cdot\left(\frac{A_i}{A_i+1+R_2/R_L}\right)$	$\left(\frac{1}{R_1}\right)\cdot\left(\frac{A_i}{A_i+1+R_S/R_1}\right)$
(3) CCVS (R_t)	$(R_2)\cdot\left(\frac{R_t}{R_t+R_2}\right)$	$\left(\frac{1}{R_1}\right)\cdot\left(\frac{R_t-R_1}{R_t+R_S+R_L+R_SR_L/R_1}\right)$
(4) VCCS (G_t)	$(R_2)\cdot\left(\frac{G_t-1/R_2}{G_t+1/R_L+1/R_S+R_2/R_SR_L}\right)$	$\left(\frac{1}{R_1}\right)\cdot\left(\frac{G_t}{G_t+1/R_1}\right)$

Table 7.2. Ideal closed-loop amplifier transfer functions.

	(A) V-to-V converter	*(B) I-to-I converter*	*(C) I-to-V converter*	*(D) V-to-I converter*
All amplifiers (1)–(4)	$1 + \frac{R_1}{R_1}$	$1 + \frac{R_2}{R_1}$	R_2	$\frac{1}{R_1}$

where A_o is the open-loop DC gain magnitude and ω_a is the open-loop 3 dB bandwidth. At frequencies greater than ω_a,

$$A(s) \approx \frac{A_o \omega_a}{s} = \frac{\text{GB}}{s} \tag{7.2}$$

where GB is known as the gain–bandwidth product of the amplifier. The "second terms" in Table 7.1 mainly[1] have the form:

$$T(s) = \frac{A(s)}{A(s) + K} \tag{7.3}$$

Substituting equation (8.2) into equation (8.3):

$$T(s) = \frac{\text{GB}/s}{\text{GB}/s + K} = \frac{1}{1 + sK/\text{GB}} \tag{7.4}$$

The closed-loop bandwidth of the circuit is thus equal to GB/K. Since GB is fixed by the open-loop characteristics of the amplifier, the closed-loop bandwidth of a particular circuit will depend on the associated value of K for that circuit. From Table 7.1, a list of K values for each of the circuit configurations in Figure 7.14 can be compiled as shown in Table 7.3 (note $G = 1 + R_2/R_1$).

The K values in Table 7.3 indicate how the bandwidth of each circuit depends on the components external to the amplifier. In the majority of cases the circuit bandwidth is dependent on the source and/or the load resistance, unlike the

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[1] Some of the table entries contain an additional term in the numerator:

$$T(s) = \frac{A(s) \pm Z}{A(s) + K}$$

This Z value indicates the presence of a zero in the closed-loop response, at a frequency s = GB/Z. If this zero frequency is much higher than that of the pole, the closed-loop bandwidth will still be determined by the pole K value. However, if the zero frequency is below that of the pole the closed-loop response will exhibit peaking, and could become unstable. In this situation additional external components would be required to bring the pole frequency down below the zero, and restore circuit stability. For the present it will be assumed that all circuits have $K \gg Z$, so the zero term can be neglected.

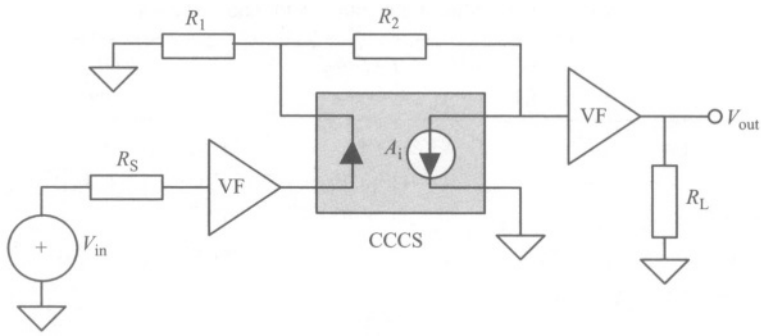


Figure 7.14. Voltage amplifier with source and load isolation.

Table 7.3. Closed loop amplifier K values.

	(A) V–V converter	*(B) I–I converter*	*(C) I–V converter*	*(D) V–I converter*
(1) VCVS (A_v)	$1+\frac{R_2}{R_1}$	$1+\frac{R_2}{R_S}+\frac{R_L}{R_1}+\frac{GR_L}{R_S}$	$1+\frac{R_2}{R_S}$	$1+\frac{R_L}{R_1}$
(2) CCCS (A_i)	$1+\frac{R_2}{R_L}+\frac{R_S}{R_1}+\frac{GR_S}{R_L}$	$1+\frac{R_1}{R_1}$	$1+\frac{R_2}{R_L}$	$1+\frac{R_S}{R_1}$
(3) CCVS (R_t)	R_2+GR_S	R_2+GR_L	R_2	$R_S+R_L+\frac{R_SR_L}{R_1}$
(4) VCCS (G_t)	$\frac{1}{R_1}+\frac{G}{R_L}$	$\frac{1}{R_1}+\frac{G}{R_S}$	$\frac{1}{R_S}+\frac{1}{R_L}+\frac{R_2}{R_SR_L}$	$\frac{1}{R_1}$

situation with an ideal (infinite gain) amplifier. The four highlighted diagonal K values, however, are independent of source and load resistance, and their actual values are identical to the closed-loop gain terms in Table 7.1. For each of these circuits, the product of the closed-loop gain and the closed-loop bandwidth remains constant, and there is a gain-bandwidth conflict.

Circuit 1A in Tables 7.1 and 7.3 represents the conventional voltage op-amp with voltage-sampling voltage-feedback, and the fixed gain–bandwidth product is a well-known limitation of this device. However, the other entries in column 1 show clearly why operational current, transresistance or transconductance amplifiers have not been popular in realizing voltage amplifier applications, since their K values are related to the source and/or load impedance. These circuits would thus exhibit an ill-defined bandwidth if the source/load conditions were not accurately known, and more seriously could become unstable if the source or load impedance was reactive. Conversely, the other entries in row 1 show that a voltage op-amp is not such a good choice for implementing circuits with closed-loop current, transconductance or transresistance gain, again because of the poorly defined K values. This reinforces the knowledge that a voltage op-amp is best suited for the implementation of closed-loop voltage-mode circuits. In effect, the dominance of the voltage

Table 7.4. K values with source and load isolation.

	(A) V-to-V converter	*(B) I-to-I converter*	*(C) I-to-V converter*	*(D) V-to-I converter*
(1) VCVS (A_v)	$1 + \frac{R_2}{R_1}$	1 (CF_I,CF_O)	1 (CF_I)	1 (CF_O)
(2) CCCS (A_i)	1 (VF_I, VF_O)	$1 + \frac{R_2}{R_1}$	1 (VF_O)	1 (VF_I)
(3) CCVS (R_t)	R_2 (VF_I)	R_2 (CF_O)	R_2	R_2* (VF_I, CF_O)
(4) VCCS (G_t)	$\frac{1}{R_1}$ (VF_O)	$\frac{1}{R_1}$ (CF_I)	$\frac{1}{R_1}$* (CF_I, VF_O)	$\frac{1}{R_1}$

*The K values in these examples become zero when the source and load resistances are neglected, that is, the closed-loop pole is at infinity. These circuits both contain a zero in the transfer function as described in fn. 1, where it was also explained that for circuit stability, the closed-loop pole must be lower in frequency than this closed-loop zero. Adding an additional external resistor (R_2 for circuit 3D, R_1 for circuit 4C) ensures that a pole is present in each closed-loop transfer function, with the K values given above. These circuits will then be stable if $K > Z$.

op-amp over any other amplifier type has restricted analog signal processing to circuit 1A.

7.5. Source and Load Isolation

Apart from the four highlighted diagonal entries, all the circuits in Table 7.3 have closed-loop bandwidths which are dependent on the source and/or load impedance. This situation arises if the open-loop input resistance of the amplifier is comparable to the output resistance of the source, or if the open-loop output resistance of the amplifier is comparable to the load resistance. The resulting interaction between the amplifier and the source/load could be eliminated by the use of VFs and CFs, whose ideal properties have already been described in a previous section. The followers would be used to isolate the source and load resistance from the amplifier circuit; Figure 7.14 shows an example of a voltage amplifier based on a current op-amp (CCCS).

In this circuit example, source and load isolation is achieved using VFs. Conversely, CFs should be used to isolate a VCVS amplifier from a current source or load. Isolation of the amplifier using CFs and VFs thus allows the source and load terms (R_S and R_L) to be eliminated from Table 7.3, and the K values simplify to those shown in Table 7.4. Entries marked CF_I or VF_I indicate the addition of an input CFs or VFs, respectively, while those marked CF_O or VF_O indicate the addition of an output CF or VF, respectively.

This table reveals some interesting facts regarding the relationship between closed-loop gain and closed-loop bandwidth. For example, the only circuits which still have bandwidth dependent on gain are the diagonal circuits which were highlighted in Table 7.3. These circuits do not seem so attractive now when it is considered that none of the other entries suffer from the gain–bandwidth conflict. Some entries (e.g. 3A, 3B, 4A, 4B) have K values which are determined by a single feedback component, leaving the other component free to independently set the gain. Moreover, several entries have K values which are equal to unity, indicating that these particular amplifiers will achieve a maximum bandwidth equal to GB, regardless of the value of closed-loop gain, source or load resistance.

In the light of Table 7.4, it might be considered surprising that the voltage op-amp is still the most popular building block of analog electronics, and is generally used to implement closed-loop voltage-mode amplifiers. Why should this be the case when you consider the other more attractive implementations in column A? One obvious answer is that 1A is the only voltage amplifier topology which does not require local input or output VFs, and the additional circuitry required to implement the followers is perhaps viewed as an unnecessarily complex arrangement for the performance benefits obtained. In practice, realizing high-performance VFs and CFs is non-trivial, since the frequency response of the followers would have to be significantly higher than the main amplifier so as not to degrade the overall performance.

On closer investigation, it can be seen that Table 7.4 can be used to classify the various practical amplifier topologies discussed in Section 7.3. For example, the application of supply-current-sensing to a voltage op-amp is equivalent to adding an output CF, as represented by circuits 1B and 1D in Table 7.4. The maximized bandwidth of current-mode circuits based on the voltage op-amp, as reported by Toumazou [21] et al., can be directly seen from Table 7.4 since circuits 1B and 1D have K values of unity.

The theoretical basis for the current-feedback op-amp can be found in Table 7.4 circuit 3A, which describes a transresistance amplifier with an input VF. Table 7.4 shows that the closed-loop bandwidth of this device when configured as a voltage amplifier is determined only by the feedback resistor R_2, and thus the closed-loop gain can be independently varied via R_1. This well-known feature of current-feedback op-amps has led to their replacement of conventional voltage op-amps in many high-speed applications.

Applying supply-current-sensing to the current-feedback op-amp is equivalent to adding an input VF and an output CF to a transresistance amplifier. Such a device covers all circuits in row 3 of Table 7.4, and in each case the closed-loop bandwidth is determined only by the feedback resistor R_2. This device can be recognized as the "Operational Floating Conveyor" [19], and

row 3 underlines the versatility of this device in implementing both voltage-mode and current-mode circuits with gain-independent bandwidths. The use of current amplifiers to implement voltage-mode circuits, as proposed by Allen, can be related back to cell 2A. The maximized bandwidth for all gain values is made clear in Table 7.4, since the K value of this circuit is unity.

This analysis has demonstrated that a bewildering array of operational amplifier architectures and novel design techniques can be neatly summarized as shown in Table 7.4. In effect, the practical devices summarized by Table 7.4 are simply modern implementations of much earlier amplifier theories, which have been made possible in many cases by advances in process technology. Although these novel ideas are practical realizations of earlier theories, this does not detract from the clear improvements in performance which many of the circuits offer over more conventional implementations. However, by showing the underlying origins of these circuits, the performance benefits and limitations can clearly be seen, enabling the circuit designer to make a more informed decision as to which device or architecture to choose in a particular situation.

7.6. Conclusions

This chapter has attempted to explore the relationship between open-loop topology and closed-loop bandwidth of analog amplifiers, and to highlight the similarities between early ideal amplifier concepts and many of today's "new" ideas relating to the comparative merits of current-mode and voltage-mode processing. The early theories of Tellegen and Carlin make no distinction between current-mode and voltage-mode, and the division that exists today is due in part to the widespread dominance of the voltage op-amp. The popularity of this device means that concepts such as the fixed gain–bandwidth product are often assumed to be a general property of all amplifier architectures, when in fact Table 7.4 shows this to be the exception rather than the rule. The implementation of voltage amplifiers using current-mode techniques has resulted in circuits with bandwidth independent of gain, and this is often given as evidence of the superiority of current-mode processing. Table 7.4, however, shows that the bandwidth of a circuit is determined by the chosen implementation, and that certain current-mode circuits exhibit fixed gain–bandwidth products while other circuits based on voltage op-amps achieve a maximum bandwidth for all values of gain.

The development and analysis of Table 7.4 is particularly relevant today because advances in processing techniques have made possible the implementation of high-performance VFs and CFs. This has led to the commercial availability of devices such as the current-feedback op-amp and

current-conveyor. Furthermore, there are other entries in Table 7.4 which have yet to be realized, indicating possible technology-driven areas of development for high-performance amplifier architectures.

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Chapter 8

NOISE, GAIN AND BANDWIDTH IN ANALOG DESIGN

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Trade-offs between noise, gain and bandwidth are important issues in analog circuit design. Noise performance is a primary concern when low-level signals must be amplified. Optimization of noise performance is a complex task involving many parameters. The circuit designer must decide the basic form of amplification required – whether current input, voltage input or an impedance-matched input. Various parameters which can then be manipulated to optimize the noise performance include device sizes and bias currents, device types (FET or bipolar), circuit topologies (Darlington, cascode, etc.) and circuit impedance levels. The complexity of this situation is then further compounded when the issue of gain–bandwidth is included. A fundamental distinction to be made here is between noise issues in wideband amplifier design versus narrowband amplifier design. Wideband amplifiers generally have bandwidths of several octaves or more and may have to operate down to dc. This generally means that inductive elements cannot be used to enhance performance. By contrast, narrowband amplifiers may have bandwidths of as little as 10% or less of their center frequency, and inductors can be used to great advantage in trading gain for bandwidth and also in improving the circuit noise performance. In order to explore these issues and trade-offs, we begin first with a description of gain–bandwidth concepts as applied to both wideband and narrowband amplifiers, followed by a treatment of electronic circuit noise modeling. These concepts are then used in combination to define the trade-offs in circuit design between noise, gain and bandwidth.

8.1. Gain–Bandwidth Concepts

All commonly used active devices in modern electronics are shown in Figure 8.1(a) and may be represented by the simple equivalent circuit shown in Figure 8.1(b). Thus the bipolar junction transistor (BJT), metal-oxide-semiconductor field-effect transistor (MOSFET), junction field-effect transistor (JFET) and the gallium arsenide field-effect transistor (GaAsFET) can all be generalized to a voltage-controlled device whose small-signal output current is related to the input control voltage by the transconductance g_m. In this

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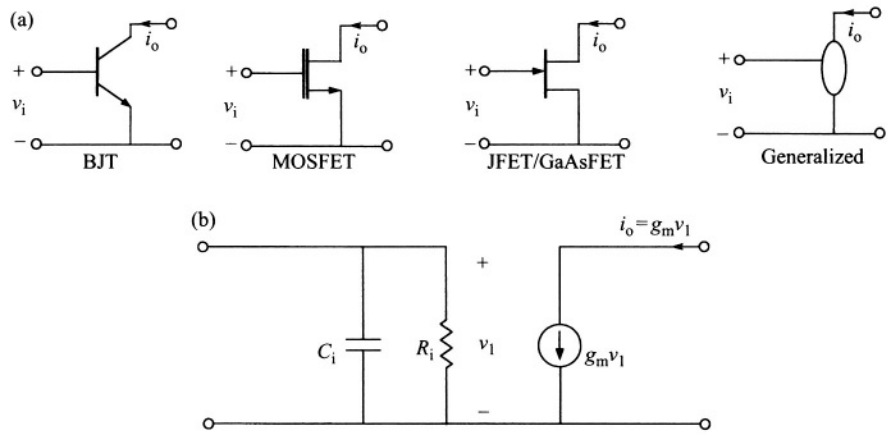


Figure 8.1. (a) Active devices, (b) simplified general equivalent circuit.

simplified representation, the output signal is assumed to be a perfect current source and any series input resistance or shunt feedback capacitance is initially neglected. This enables us to focus first on the dominant gain- bandwidth limitations as they relate to noise performance. (Note that $R_i = \infty$ for the FETs.) The effective transit time of charge carriers traversing the active region of the device is [1]

$$\tau_1 = \frac{C_i}{g_m} \tag{8.1}$$

and the effective low-frequency current gain is

$$\beta = g_m R_i \tag{8.2}$$

Again note that $\beta = \infty$ for the FETs. In this simple model neglecting parasitic capacitance, we find that the frequency of unity small-signal current gain is [1]

$$f_T = \frac{1}{2\pi\tau_1} \tag{8.3}$$

In order to obtain broadband amplification of signals we commonly connect amplifying devices in a cascade with load resistance R_L on each stage. Consider a typical multistage amplifier as shown in Figure 8.2.

The portion of Figure 8.2 enclosed in dotted lines can be considered a repetitive element that comprises the cascade. The gain of this element or stage is

$$\frac{v_1}{v_i} = -\frac{g_m R_L'}{1 + sC_i R_L'} \tag{8.4}$$

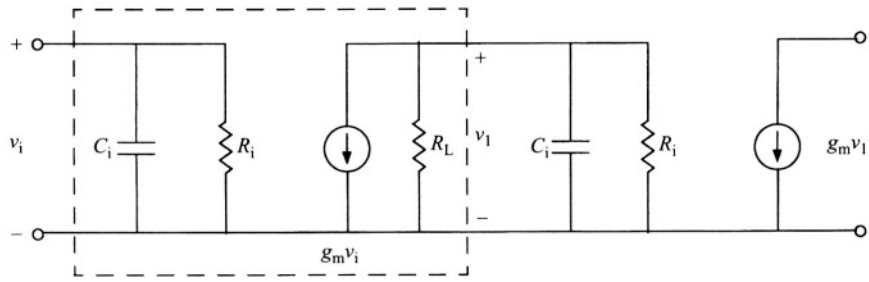


Figure 8.2. Cascade amplifier equivalent circuit.

from which we see that the mid-band gain magnitude is

$$G = g_m R'_L \tag{8.5}$$

and the – 3 dB bandwidth (rad/sec) is

$$B = \frac{1}{C_i R'_L} \tag{8.6}$$

Thus the gain–bandwidth product of this stage is

$$GB = \frac{g_m}{C_i} = \frac{1}{\tau_1} = 2\pi f_T \tag{8.7}$$

The importance of the device (or process for integrated circuits) f_T is thus apparent. From (8.7) we can conclude that in a cascade we cannot achieve gain over a wider bandwidth than the device f_T (excluding inductors) and that we can trade-off gain against bandwidth by choosing R_L. This process is called *resistive broadbanding*. Wider bandwidth is achieved at the expense of lower gain by using low values of R_L. These conclusions also apply if the signal input to the amplifier approximates a current source and the stage considered is not part of a multi-stage amplifier but is an isolated single gain stage. This is the case, for example, in fiber-optic preamplifiers. However, if the signal source to the amplifier approximates a voltage source, then the single-stage bandwidth (and thus the gain–bandwidth) is ideally infinite. This case is rarely encountered in practice at high frequencies (gigahertz range), but may be found in sub-gigahertz applications. More commonly at frequencies in the gigahertz range, we find the first stage of an amplifier driven by a voltage source (e.g. coming from an antenna) in series with a resistive source impedance R_S (often 50 or 75 Ω). In that case the signal input can be represented by a Norton equivalent current source in parallel with R_S and the previous analysis is valid, as R_S can be lumped in with R_i.

8.1.1. Gain–Bandwidth Shrinkage

If we construct a multi-stage amplifier consisting of N identical stages with resistive interstage loads as shown in Figure 8.2, we can describe the gain–bandwidth behavior of the amplifier as follows. If the gain per stage is G and the bandwidth per stage is B then the overall amplifier transfer function for N stage is

$$\frac{v_o}{v_i} = \left(\frac{G}{1 + j(\omega/B)}\right)^N \tag{8.8}$$

The overall – 3 dB frequency of the amplifier is the frequency where $|v_o/v_i| = G^N/\sqrt{2}$. From (8.8) this is

$$\omega_{-3\,dB} = B\sqrt{2^{1/N} - 1} = B_N \tag{8.9}$$

Thus, we see that the bandwidth shrinks as we add stages. For example, $\omega_{-3\,dB} = 0.64B$ for $N = 2$ and $\omega_{-3\,dB} = 0.51B$ for $N = 3$. In an N-stage amplifier, the overall mid-band gain is $G_N = G^N$ and we can define a per-stage gain–bandwidth figure-of-merit as

$$(GB)_N = (G_N)^{1/N} B_N \tag{8.10}$$

$$= GB\sqrt{2^{1/N} - 1} \tag{8.11}$$

We conclude that the cascading of stages each with a negative-real-pole transfer function results in significant loss of gain–bandwidth product.

Gain–bandwidth shrinkage is also caused by parasitic elements. The inclusion of parasitic capacitance in shunt with C_i causes a reduction of the device f_T and consequent loss of gain–bandwidth. Thus, in wideband integrated circuit (IC) design, the layout must be carefully chosen to minimize parasitic capacitance. Any resistance in series with the input lead (such as the base resistance r_b of a BJT) also causes loss of gain–bandwidth. Consider the cascade of Figure 8.2 with parasitic resistance r_b added to each device as shown in Figure 8.3 where R_i is now neglected. Taking one section as shown in the dotted line, we find

$$\frac{v_o}{v_i} = -\frac{g_m R_L}{1 + (R_L + r_b)j\omega C_i} \tag{8.12}$$

from which the mid-band gain is

$$G = g_m R_L \tag{8.13}$$

and the –3 dB bandwidth is

$$B = \frac{1}{(R_L + r_b)C_i} \tag{8.14}$$

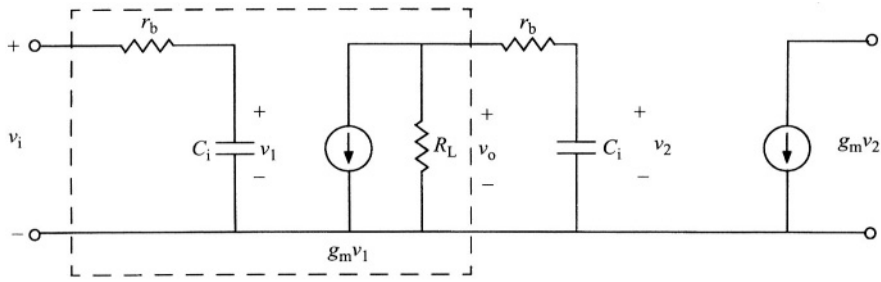


Figure 8.3. Cascade amplifier equivalent circuit including parasitic resistance.

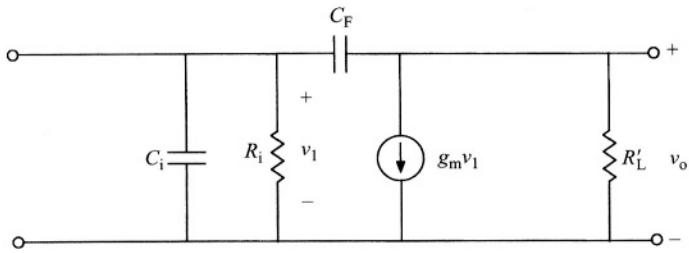


Figure 8.4. Device equivalent circuit including parasitic feedback capacitance.

Thus the gain–bandwidth product of the stage is

$$GB = \frac{R_L}{R_L + r_b}\frac{g_m}{C_i} \tag{8.15}$$

$$= 2\pi f_T \frac{R_L}{R_L + r_b} \tag{8.16}$$

We see that the gain–bandwidth is reduced by the ratio $R_L/(R_L + r_b)$. This leads to trade-offs in wideband design since we can reduce the magnitude of r_b by increasing the device size in the IC layout. This also reduces the noise contribution from r_b (to be considered later) which is highly desirable, but has the unwanted effect of increasing the parasitic device capacitance which leads to a reduction of f_T and consequent loss of gain–bandwidth.

Loss of gain–bandwidth also occurs in simple amplifier cascades due to Miller effect, although the loss becomes less severe as R_L is reduced, which is often the case for high-frequency wideband amplifiers. Consider the single amplifier stage shown in Figure 8.4 where feedback capacitance C_F is included. (This represents the collector–base parasitic capacitance in BJTs and the drain–gate parasitic in FETs.)

The Miller capacitance seen across the input terminals is [2]

$$C_m = (1 + g_m R'_L C_F) \tag{8.17}$$

Thus, the total input capacitance is

$$\begin{aligned} C_T &= C_i + C_m \\ &= g_m \left(\frac{1}{\omega_T} + C_F R'_L \right) \\ &= g_m (\tau_1 + C_F R'_L) \end{aligned} \tag{8.18}$$

The time constant $C_F R'_L$ can be compared with $\tau_1 = 1/(2\pi f_T)$ to determine the loss of stage gain–bandwidth. The smaller R'_L, the less the effect. For example, if $R'_L = 50\,\Omega$, $C_F = 10\,\text{fF}$ and $f_T = 30\,\text{GHz}$, we find $\tau_1 = 5.3\,\text{ps}$ and $C_F R'_L = 0.5\,\text{ps}$. In this case, Miller effect reduces the stage gain–bandwidth by 10%. A trade-off occurs again if noise must be minimized by increasing the device size (to reduce r_b) in that this will increase C_F and increase the Miller effect.

8.1.2. Gain–Bandwidth Trade-Offs Using Inductors

Inductive elements have long been used to advantage in electronic amplifiers. Inductors can be used to obtain a frequency response which peaks in a narrow range and thus tends to reject unwanted out-of-band signals. However, the advantages of using inductors extend beyond this as they allow the inherent device gain–bandwidth to be arbitrarily moved across the spectrum, as will now be shown. Consider the single-stage amplifier shown in Figure 8.5 and initially neglect feedback capacitance. The input resistance R'_i represents the basic device input resistance in shunt with any external resistors such as bias resistors. The stage transfer function is

$$\frac{i_o}{i_i}(s) = \frac{g_m R'_i}{1 + R'_i C_i s} \tag{8.19}$$

The stage gain is

$$G = g_m R'_i = \beta_{\text{eff}} \tag{8.20}$$

and the – 3 dB bandwidth is

$$B = \frac{1}{R_i C_i} \tag{8.21}$$

giving the stage gain–bandwidth product as

$$GB = \frac{g_m}{C_i} = 2\pi f_T \tag{8.22}$$

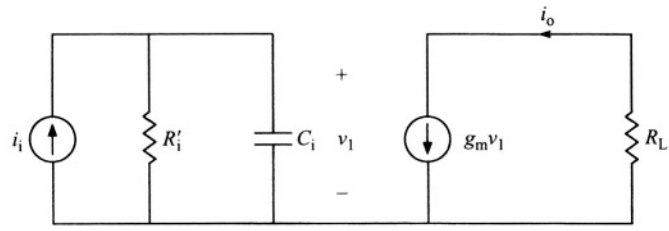


Figure 8.5. Single-stage equivalent circuit.

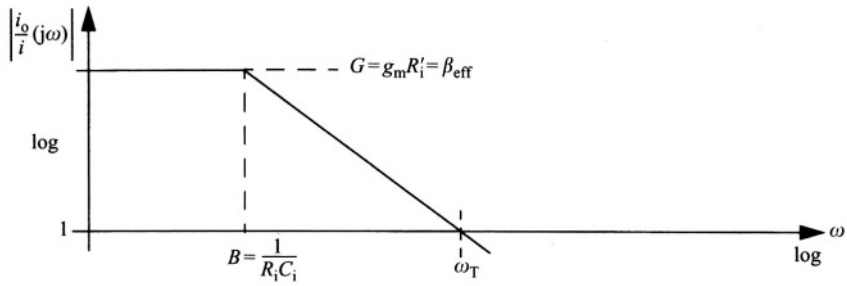


Figure 8.6. Frequency response of the circuit in Figure 8.5.

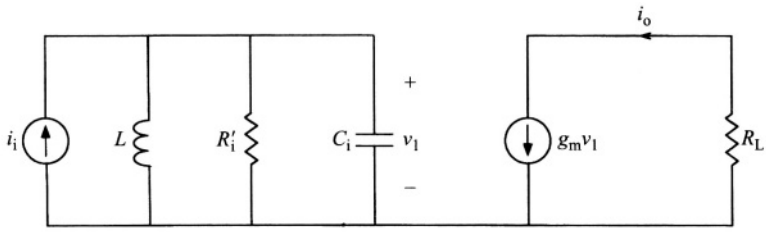


Figure 8.7. Single stage with input shunt inductor.

as before. The frequency response given by (8.19) is plotted in Figure 8.6.

Now consider adding a shunt inductor as shown in Figure 8.7. The transfer function of the circuit of Figure 8.7 is

$$\frac{i_o}{i_i}(s) = g_m \frac{Ls}{1 + (L/R_i')s + LCs^2} \tag{8.23}$$

At resonance

$$\omega_0 = \frac{1}{\sqrt{LC_i}} \tag{8.24}$$

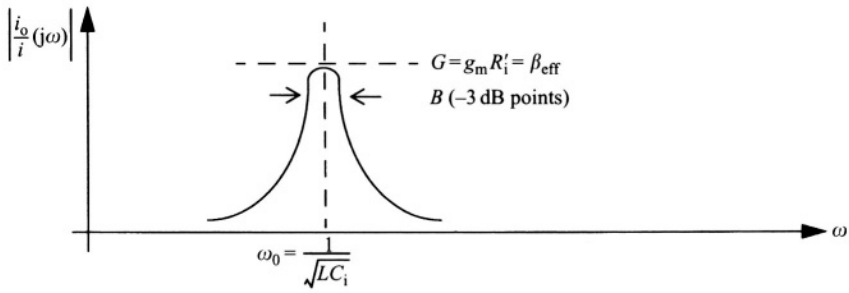


Figure 8.8. Frequency response of the circuit of Figure 8.7.

where

$$G = \left|\frac{i_o}{i_i}(j\omega_0)\right| = g_m R_i' \tag{8.25}$$

The – 3 dB bandwidth of the transfer function is

$$B = \frac{\omega_0}{Q_0} = \frac{1}{R_i C_i} \tag{8.26}$$

where

$$Q_0 = \frac{R_i'}{\omega_0 L} = \omega_0 C_i R_i' \tag{8.27}$$

From (8.25) and (8.26), we find the gain–bandwidth product of the circuit is now

$$GB = 2\pi f_T \tag{8.28}$$

as before. However, the gain is now realized in a narrow band centered on the frequency ω_0 as shown in Figure 8.8.

We can thus shift the high-gain region of the device transfer function to high frequencies using the inductor. In practice, the existence of lossy parasitics such as r_b reduces the gain at very high frequencies, but nonetheless we are still able to trade-off gain for bandwidth quite effectively in this way. Typical performance is shown in Figure 8.9 where ideal lossless behavior is compared with typical practical results. High-frequency gain larger than the lowpass asymptote is readily achieved.

8.2. Device Noise Representation

In order to examine trade-offs between noise performance and gain–bandwidth, we need a convenient means to compare the noise performance of different devices and different configurations. This is best done by representing the active-device noise behavior by equivalent input noise voltage and

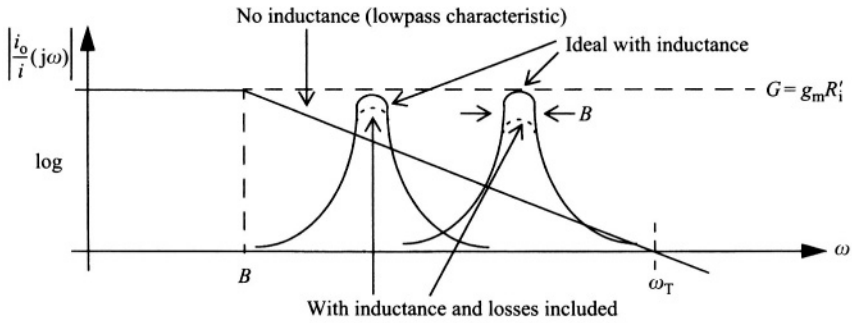


Figure 8.9. Frequency response of the circuits of Figures 8.5 and 8.7.

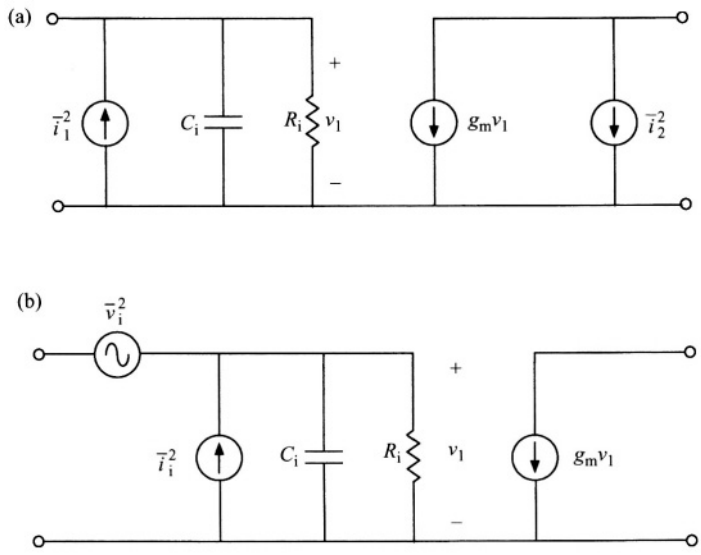


Figure 8.10. Noise representation of active devices with equivalent input generators.

current generators [3]. Although these generators are correlated in general, we find in many applications that one or other generator is dominant and thus the other generator and the correlation can be neglected. Once again we begin with the simple general representation of Figure 8.1 and add noise generators as shown in Figure 8.10(a) (white noise only is considered).

We then calculate equivalent input generators which model the device noise behavior as shown in Figure 8.10(b). In Figure 8.10(a), the output noise source $\overline{i}_2^2$ is caused by thermal noise in FETs and shot noise in BJTs. Thus,

$$\overline{i}_2^2 = 2qI_c\Delta f \tag{8.29}$$

for BJTs and

$$\bar{i}_2^2 = 4kT\tfrac{2}{3}g_m\Delta f \tag{8.30}$$

for FETs.

The input noise generator can be assumed zero for FETs and for BJTs it is caused by shot noise in the base current given by

$$\bar{i}_1^2 = 2qI_B\Delta f \tag{8.31}$$

Note that if a physical shunt resistor R is connected in shunt with the device input (e.g. due to bias circuits), then this can be folded into the noise representation by including it in R_i (which becomes R_i') and adding a thermal noise generator to $\bar{i}_1^2$ of value

$$\bar{i}_R^2 = 4kT\frac{1}{R}\Delta f \tag{8.32}$$

The equivalent input generators of Figure 8.10(b) now become

$$\bar{v}_i^2 = \frac{\bar{i}_2^2}{g_m^2} \tag{8.33}$$

and

$$\bar{i}_i^2 = \bar{i}_1^2 + \frac{\bar{i}_2^2}{|\beta(j\omega)|^2} \tag{8.34}$$

where the ac current gain $\beta(j\omega)$ of the device is given by

$$\beta(j\omega) = \frac{g_m R_i}{1 + j\omega R_i C} \tag{8.35}$$

$$= \frac{\beta}{1 + j\omega\beta(C_i/g_m)} \tag{8.36}$$

$$= \frac{\beta}{1 + j(\omega/\omega_T)\beta} \tag{8.37}$$

The expression for $\bar{v}_i^2$ in (8.33) can be related to the device transconductance in general for any active device by using $g_m = qI_c/kT$ for BJTs and deriving:

$$\bar{v}_i^2 = 4kT\frac{2}{3}\frac{1}{g_m}\Delta f \tag{8.38}$$

for FETs and

$$\bar{v}_i^2 = 4kT\frac{1}{2}\frac{1}{g_m}\Delta f \tag{8.39}$$

for BJTs. Finally, the representation of Figure 8.10(b) can be enhanced by adding to $\bar{v}_i^2$ a thermal noise generator due to any physical series input resistance such as base resistance r_b for BJTs, given by $4kTr_b\Delta f$.

The equivalent input noise representation of Figure 8.10(b) can now be used to generate some general conclusions regarding low-noise design before we examine the specifics of the gain–bandwidth noise trade-off. For amplifiers in which the input noise current is important (such as fiber-optic amplifiers driven by a high-impedance source), the noise is dominated by $\bar{i}_i^2$. Thus FETs have an advantage in that there is no input shot noise contribution as in BJTs. However, both FETs and BJTs tend to be dominated in high-frequency wideband applications by the frequency-dependent second term in (8.34). At high frequencies, this asymptotes to

$$\frac{\bar{i}_2^2}{|\beta(j\omega)|^2} = \bar{i}_2^2 \left(\frac{\omega}{\omega_T}\right)^2 \tag{8.40}$$

for all devices. Thus a high device f_T becomes important as does minimization of $\bar{i}_2^2$. This then involves trade-offs involving device bias point and dc power dissipation. The use of low collector current I_C in BJTs can help the noise performance but may degrade the device f_T. In the case of FETs the designer has more degrees of freedom in that the FET transconductance depends on both drain bias current I_D and device geometry via *W/L*.

For applications where the input noise voltage generator $\bar{v}_i^2$ is dominant (where the driving source impedance is low) all active devices are operated with the maximum possible transconductance g_m. This in general calls for high bias currents and large area devices with high *W/L* when using FETs. If BJTs are used, then high bias currents are also required to give a large value of g_m, and in addition, the base resistance must be minimized which also requires large device area. The trade-offs here involve dc power dissipation and the deleterious effects of increasing device parasitic capacitance as the active device area is increased.

The issue of the impact of negative feedback on the noise-gain–bandwidth trade-off will be discussed in a later section. However, at this point it is worth considering the impact of noise performance of the most common form of feedback-series resistive degeneration (local series feedback) in the common

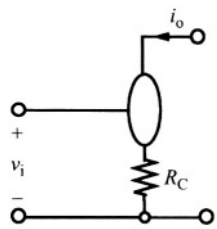


Figure 8.11. Generalized series resistive negative feedback.

lead as shown in Figure 8.11, This connection can be used with all active devices.

It leads to improved linearity, facilitates the trade-off of gain for bandwidth and allows the manipulation of the device input and output impedances. However, there is a noise penalty in that the equivalent input noise voltage generator $\bar{v}_i^2$ of the circuit is increased by the amount of thermal noise in R_C, which is $4kTR_C\Delta f$. The equivalent input noise current is unchanged. The gain of the circuit as expressed by the transconductance is reduced by the negative feedback due to R_C and is given by

$$\frac{i_o}{v_i} = \frac{g_m}{1 + g_m R_C} \tag{8.41}$$

Note that the feedback loop gain in this circuit is $T = g_m R_C$.

8.2.1. Effect of Inductors on Noise Performance

The use of inductors to trade-off bandwidth versus gain was described above. Inductors also offer the opportunity to realize significantly improved noise performance in high-frequency amplifiers. This can be appreciated by adding a shunt inductor L as shown in Figure 8.7 across the input of the equivalent circuits of Figure 8.10. Then at the parallel resonant frequency, $\omega_0 = 1/\sqrt{LC_i}$, the inductive and capacitive impedances cancel at the input of the device and the frequency dependent term in $\bar{i}_i^2$ in (8.34) disappears. This gives significantly improved noise performance in many high-frequency applications, although the technique is obviously restricted to narrowband circuits. Inductive optimization of noise performance based on these principles is commonly implemented in gigahertz range narrowband low-noise amplifiers (LNAs) used in wireless communication systems.

Another common and important use of the inductors in high-frequency low-noise circuits is in inductive common-lead degeneration as shown in Figure 8.12(a). The small-signal equivalent of this connection is shown in Figure 8.12(b), where a simplified active device equivalent has been used. In order to examine the effect of L_C on noise performance, the output noise generator $\bar{i}_2^2$ is also included.

First, we omit $\bar{i}_2^2$ and examine the effect of L_C on the gain and input impedance of the stage. The major benefit of L_C is in boosting the resistive part of the input impedance of the stage without degrading the noise performance, as happens with resistive degeneration. The use of common-lead inductance is widespread in LNA design using both FETs and BJTs, although once again the technique is limited to narrowband applications. The physical inductor is often realized using the package bond wires [4], or on-chip spiral inductors can also be used [5–7]. By calculating the current i_i flowing into the equivalent circuit

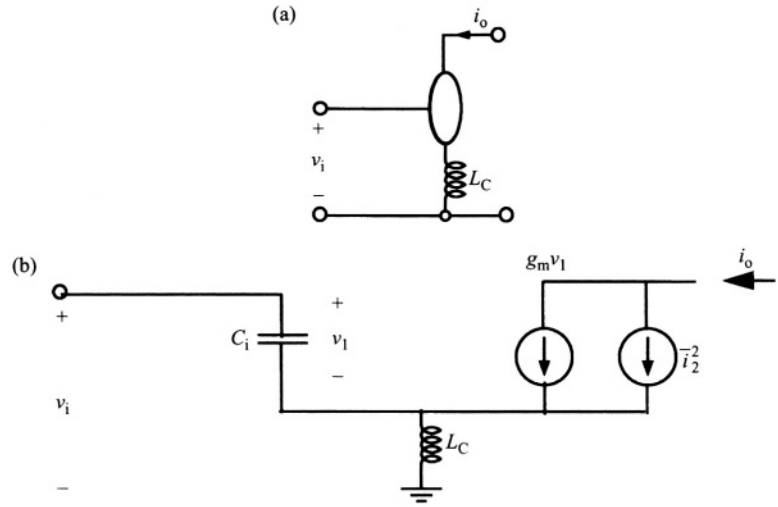


Figure 8.12. (a) Common-lead inductive degeneration using L_C, (b) small-signal equivalent circuit.

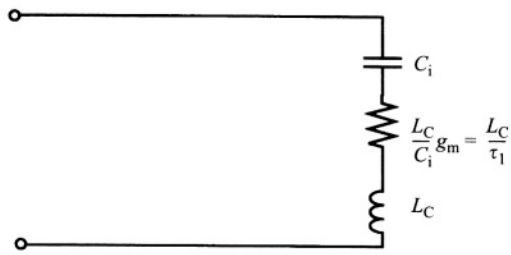


Figure 8.13. Input impedance representation of Figure 8.12(b).

of Figure 8.12(b), we find the input impedance is

$$Z_i = \frac{v_i}{i_i} = \frac{1}{j\omega C_i} + \frac{L_C}{C_i} g_m + j\omega L_C \tag{8.42}$$

This expression can be represented by the equivalent circuit of Figure 8.13. We see that a resistive portion $(L_C/C_i)g_m$ appears which can be chosen to have an appropriate value to allow matching to typical RF source resistances of 50 or 75 Ω. This same result could be achieved by simply adding a physical series input resistor, but this would add a large amount of noise to the circuit and is generally an unacceptable option. Additional input inductive and capacitive elements are usually added to produce a purely resistive external input impedance. Typical values in (8.42) might be $L_C = 0.5\,\text{nH}$,

$C_i = 1\,\text{pF}$ and $g_m = 100\,\text{mA/V}$ giving the resistive portion of Z_i a value $0.5 \times 10^{-9} \times 10^{12} \times 10^{-1} = 50\,\Omega$. This would correspond to $\tau_1 = C_i/g_m = 10\,\text{ps}$ and $f_T = 16\,\text{GHz}$.

The introduction of L_C typically causes a reduction in gain and this can be estimated from

$$\frac{i_o}{v_i} = \frac{g_m}{1 - \omega^2 L_C C_i + j\omega L_C g_m} \tag{8.43}$$

The effect of L_C on noise performance is somewhat complicated, but a rough idea can be obtained by referring the noise generator $\bar{i}_2^2$ in Figure 8.12(b) back to the input, giving an equivalent input noise voltage generator

$$\bar{v}_i^2 = \frac{\bar{i}_2^2}{g_m^2}(1 - \omega^2 L_C C_i)^2 \tag{8.44}$$

We see that the effect of L_C is to reduce the magnitude of $\bar{v}_i^2$ compared to the case where L_C is absent. In practice, we find small but useful improvements in the noise performance of high-frequency LNAs when this technique is used to help match the input. For $L_C = 0.5\,\text{nH}$ and $C_i = 1\,\text{pF}$, we find the factor $(1 - \omega^2 L_C C_i)^2$ to have values 0.96 (–0.2 dB) at 1 GHz and 0.67 (–1.7 dB) at 3 GHz.

8.3. Trade-Offs in Noise and Gain–Bandwidth

The considerations described above focused on noise and gain–bandwidth representation of electronic circuits. We now use these tools to examine issues and methods of trade-off between these quantities.

8.3.1. Methods of Trading Gain for Bandwidth and the Associated Noise Performance Implications [8]

The trade-off of gain for bandwidth can be achieved in a number of ways, with noise performance, terminal impedances and the form of the circuit transfer function being important constraints. The use of inductors to transfer the device gain to a higher frequency in narrowband applications has been treated in Subsection 8.1.2 and will not be considered further. For broadband amplifiers, the simplest method of trading gain for bandwidth is the use of resistive broadbanding as described in Section 8.1. This method has the advantage of simplicity, but has the drawbacks of gain–bandwidth shrinkage over multiple stages and limitations on control of the circuit terminal impedances. For example, if a resistive input impedance of $50\,\Omega$ is required to match a source resistance of $R_S = 50\,\Omega$, the only option available is connection of a shunt resistor R_X to ground as shown in Figure 8.14. Assume the device input resistance R_i is large and let $R_S = R_X$.

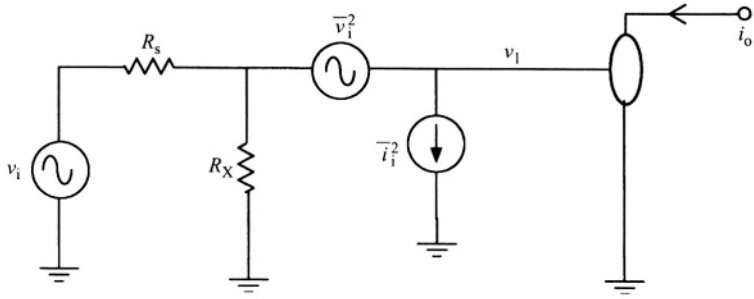


Figure 8.14. Simple input shunt resistive matching.

We can calculate the circuit noise figure by comparing the total noise at v_i with that due to the source resistance. The input impedance of the active device does not affect the following noise figure calculation and is neglected. Using $R_S = R_X$, we find for the total noise at v_1

$$v_{IT}^2 = 4kT\frac{R_S}{2} + v_i^2 + i_i^2\frac{R_S^2}{4} \tag{8.45}$$

where correlation has been neglected. The noise at v_1 due to the source resistance is

$$\bar{v}_{IS}^2 = 4kT\frac{R_S}{4} \tag{8.46}$$

From the definition of noise figure, we have

$$NF = \frac{\bar{v}_{IT}^2}{v_{IS}^2}, \tag{8.47}$$

and using (8.45) and (8.46) in (8.47), we find

$$NF = 2 + 4\frac{\bar{v}_i^2}{4kT R_S} + \frac{\bar{i}_i^2 R_S}{4kT R_S} \tag{8.48}$$

If R_X is omitted from the calculation, the circuit noise figure is

$$NF = 1 + \frac{\bar{v}_i^2}{4kT R_S} + \frac{\bar{i}_i^2 R_S^2}{4kT R_S} \tag{8.49}$$

From (8.48) and (8.49), we see that for low-noise circuits, the degradation in circuit noise figure caused by the addition of $R_X = R_S$ is about 3 dB and can be higher. This is unacceptable in many applications.

These limitations on simple resistive broadbanding lead us to examine other options. One of the most widely used is negative feedback [9]. The basic

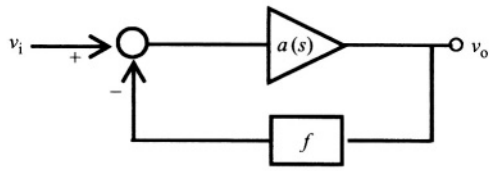


Figure 8.15. Negative feedback amplifier.

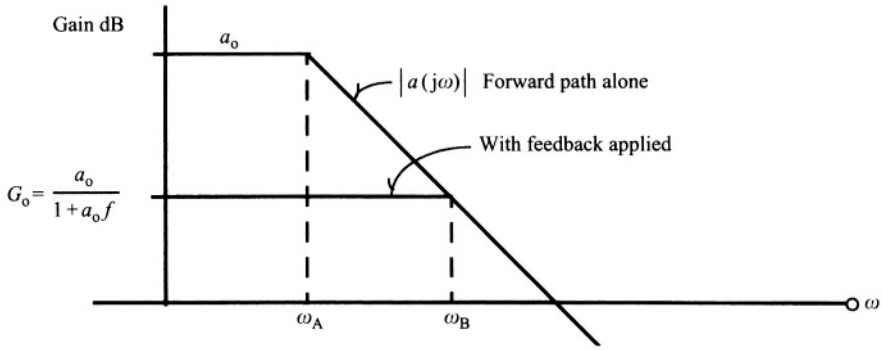


Figure 8.16. Gain versus log frequency for the circuit of Figure 8.15.

trade-off of gain and bandwidth allowed by the use of negative feedback can be illustrated by the following simple example. Consider an idealized negative feedback amplifier with a one-pole forward gain function as shown in Figure 8.15.

The forward gain path has a transfer function

$$a(s) = \frac{a_o}{1 + s\tau_A} \tag{8.50}$$

where

$$\omega_{-3\,dB} = \omega_A = \frac{1}{\tau_A} \tag{8.51}$$

The gain versus frequency of the open and closed loop amplifier is shown in Figure 8.16 where f is assumed frequency independent.

The gain of the feedback amplifier is

$$\begin{aligned} \frac{v_o}{v_i}(s) &= \frac{a(s)}{1 + a(s)f} \\ &= \frac{a_o}{1 + a_o f} \frac{1}{1 + s\tau_A/(1 + a_o f)} \end{aligned} \tag{8.52}$$

where the loop gain is

$$T = a_o f \tag{8.53}$$

the mid-band gain is

$$G_o = \frac{a_o}{1+T} \tag{8.54}$$

and the – 3 dB frequency is

$$\omega_B = (1+T)\omega_A \tag{8.55}$$

From (8.52) and Figure 8.16, we see that the use of negative feedback allows a direct trade-off of gain for bandwidth while maintaining a fixed gain–bandwidth product.

In addition to the gain–bandwidth trade-off, the use of feedback allows modification of the terminal impedance of the amplifier. If the forward gain block has an input resistance R_i, then shunt feedback at the input gives a modified (lowered) input resistance

$$R_i' = \frac{R_i}{1+T} \tag{8.56}$$

Series feedback at the input raises the input resistance to

$$R_i' = R_i(1+T) \tag{8.57}$$

The use of combined shunt and series feedback can give intermediate values of terminal impedances and this technique will be described below. The use of combined feedback allows realization of matched terminal impedances with much less noise-figure degradation than is caused by simple shunt or series resistive matching.

8.3.2. The Use of Single-Stage Feedback for the Noise-Gain–Bandwidth Trade-Off

Consider a cascade of local series feedback stages as shown in Figure 8.17. The active device with feedback resistor R_C can be represented by the simplified high-frequency equivalent circuit of Figure 8.18. If the loop gain $T = g_m R_C$ is large, this equivalent circuit reduces to that shown in Figure 8.19, where the effective transconductance is given by

$$g_m' = \frac{g_m}{1+g_m R_C}\frac{1}{1+s\tau_1} \tag{8.58}$$

The transconductance g_m' has a pole with magnitude f_T that can usually be neglected. We see that the input capacitance and transconductance are both

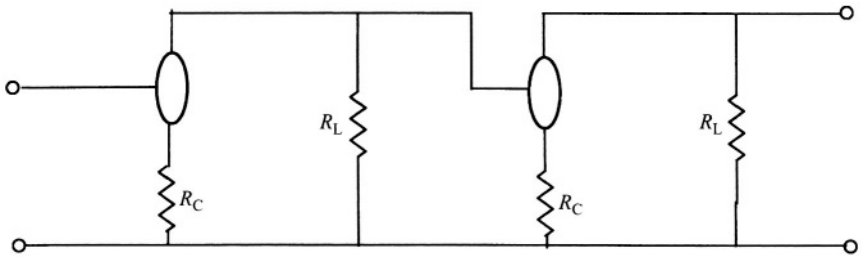


Figure 8.17. Cascade of local series feedback stages.

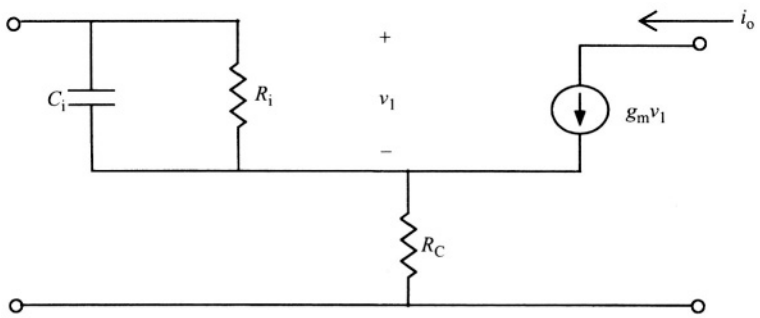


Figure 8.18. Simplified, high-frequency equivalent circuit of an active device with series feedback.

reduced by the factor $(1 + T)$. Thus using the analysis of Section 8.1, we conclude that gain and bandwidth can be traded off via the feedback resistor R_C. A significant advantage of this technique over simple resistive broadbanding is the linearization produced by R_C. The noise introduced by R_C is described in Section 8.2. The device dc power dissipation is also part of this trade-off since $T = g_m R_C$ and g_m increases as the bias current increases. This trade-off allows smaller R_C to be used for a given value of T with improved noise performance. Note that the input resistance of this stage is now quite large and will generally not meet $50\,\Omega$ matching requirements.

Single-stage feedback can also be implemented in the form of shunt feedback as shown in Figure 8.20. The shunt feedback stage has low input and output impedances and is not suitable for cascading. It can be used as a stand-alone single stage and if parasitic capacitances are neglected, we find the transimpedance gain is

$$\frac{v_o}{i_i} \cong -R_F \frac{1}{1 + s\tau_1 R_F / R_L} \tag{8.59}$$

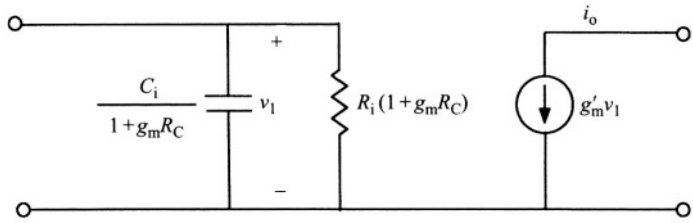


Figure 8.19. Circuit equivalent to Figure 8.18 for large loop gain.

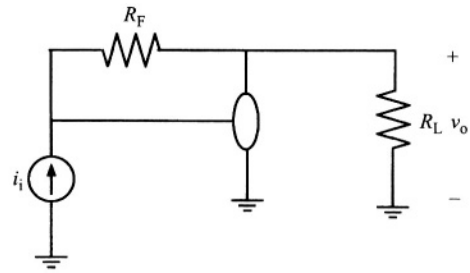


Figure 8.20. Single-stage shunt feedback.

From (8.59), we see that the gain–bandwidth product is

$$\left|\frac{v_o}{i_i}\right| B = R_F \frac{R_L}{R_F}\frac{1}{\tau_1} = 2\pi f_T R_L \tag{8.60}$$

Thus, gain and bandwidth can be traded using the value of R_F. The input impedance is given by

$$Z_i = \frac{1}{C_i s} \| R_i \| (R_F + R_L) \| \frac{1}{g_m}\left(1 + \frac{R_F}{R_L}\right) \tag{8.61}$$

The input impedance is usually dominated by the last term in (8.61) and is low. Thus, this stage is well suited to current amplification and is often used in that role.

The noise performance of the shunt feedback stage of Figure 8.20 is easily estimated by recognizing that a shunt feedback resistor such as R_F contributes to the equivalent input current noise generator

$$\bar{i}_F^2 = 4kT\frac{1}{R_F}\Delta f \tag{8.62}$$

Thus, as the stage is broadbanded by reducing R_F, the equivalent input noise current increases. This trade-off is well known to designers of high-speed wideband current amplifiers such as are used in fiber-optic receivers [10,11].

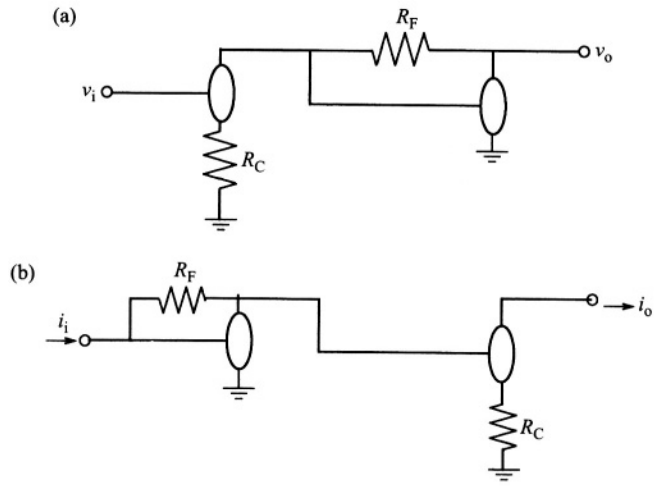


Figure 8.21. (a) Wideband voltage amplifier, (b) wideband current amplifier.

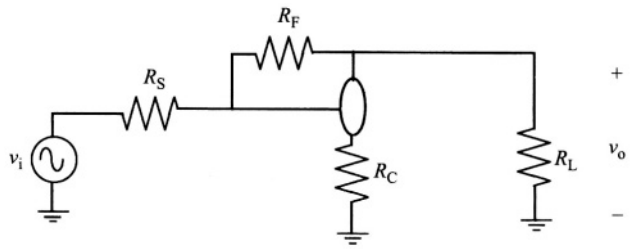


Figure 8.22. Single-stage dual-feedback amplifier.

The single-stage feedback circuits described above can be used in mismatched cascades to form wideband voltage or current amplifiers using two stages as shown in Figure 8.21 [12]. Transimpedance and transresistance amplifiers can be implemented by adding additional stages. The advantage of the configurations of Figure 8.21 is the minimal interaction between stages and the dependence of the gain solely on resistor ratios for large values of loop gain T.

The single-stage feedback amplifiers considered so far do not allow realization of low-noise wideband matched-impedance amplifiers. This function can, however, be achieved by appropriate use of multiple feedback loops. Consider a single-stage dual-feedback amplifier as shown in Figure 8.22. We assume $R_S = R_L = R$.

If $g_m R_C \gg 1$ and $R_F \gg R_L$, the input impedance can be approximated by a parallel RC combination with values

$$C_i' = \frac{C_i}{g_m R_C} = \frac{\tau_1}{R_C} \tag{8.63}$$

$$R_i = \frac{R_F R_C}{R_L} \tag{8.64}$$

The output resistance is approximately

$$R_o = \frac{R_F R_C}{R_S} \tag{8.65}$$

and we find $R_o = R_i$ if $R_S = R_L$. In a matched amplifier we set $R_i = R_o = R_S = R_L = R$. The gain is then given by

$$G = \frac{R_L}{2R_C} = \frac{R}{2R_C} = \left|\frac{v_o}{v_i}\right| \tag{8.66}$$

The – 3 dB bandwidth is set by the time constant of C_i' and $R_S/2$ (the impedance level at the input node) giving

$$B = \frac{2}{C_i' R} \tag{8.67}$$

Thus the gain–bandwidth of the stage is

$$GB = \frac{1}{\tau_1} = 2\pi f_T \tag{8.68}$$

using (8.63), (8.66) and (8.67). We can thus realize a matched impedance amplifier and trade gain for bandwidth using resistor values.

The advantages of the circuit of Figure 8.22 are further evident when we examine the noise performance. If the basic active device has equivalent input noise generators $\bar{i}_i^2$ and $\bar{v}_i^2$, then the addition of resistors R_C and R_F modify these to

$$\bar{v}_{i1}^2 = \bar{v}_i^2 + 4kTR_C\Delta f \tag{8.69}$$

$$\bar{i}_{i1}^2 = \bar{i}_i^2 + 4kT\frac{1}{R_F}\Delta f \tag{8.70}$$

The noise figure of the amplifier can now be calculated as

$$\mathrm{NF} = 1 + \frac{\bar{v}_{i1}^2}{4kTR_S\Delta f} + \frac{\bar{i}_{i1}^2 R_S^2}{4kTR_S\Delta f} \tag{8.71}$$

$$= 1 + \frac{R_C}{R_S} + \frac{R_S}{R_F} + \frac{\bar{v}_i^2}{4kTR_S\Delta f} + \frac{\bar{i}_S^2 R_S^2}{4kTR_S\Delta f} \tag{8.72}$$

We see that the noise figure is degraded by an additive factor of $R_C/R_S+R_S/R_F$, and this can be made a reasonably small contribution. For example, if $R_S = R_L = R = 50\,\Omega$, $R_C = 5\,\Omega$ and $R_F = 500\,\Omega$, then the amplifier gain is $G = 5$, bandwidth $B = f_T/5$, and $R_C/R_S + R_S/R_F = 0.2$. If the basic device noise figure is 2 dB (8.58), then the overall amplifier noise figure is 1.58+0.2 = 1.78 which is 2.5 dB. The addition of the matching resistors has only degraded the device noise figure by 0.5 dB.

8.3.3. Use of Multi-Stage Feedback to Trade-Off Gain, Bandwidth and Noise Performance

The single-stage feedback circuits described above are widely used in practice because of their ease of design and good overall performance. However, higher levels of performance can be achieved (higher gain and bandwidth and lower noise) if we allow use of feedback over multiple stages. The price paid for this improved performance is increased complexity of design and, in particular, the possibility of oscillation [13] which must be addressed by appropriate circuit compensation.

Consider the two-stage shunt–series feedback amplifier in Figure 8.23 [9–11,14,15]. This circuit has low input impedance, high output impedance and a well-stabilized current gain given by

$$\left|\frac{i_o}{i_i}\right| \cong \frac{R_F + R_C}{R_C} \tag{8.73}$$

for high loop gain. This is called a current-feedback pair.

The gain–bandwidth trade-off in this circuit can be calculated from the small-signal equivalent circuit of Figure 8.24. The feedback current is given by

$$i_{fb} = \frac{R_C}{R_C + R_F} i_o \tag{8.74}$$

The feedback loading on the input is $(R_F + R_E)$, and this is lumped in with R_{i1} to form R_1. The input resistance and capacitance of the second stage are R'_{i2}

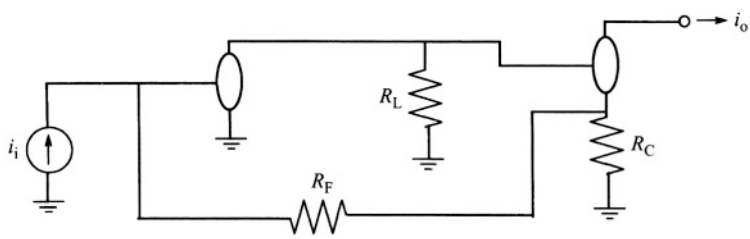


Figure 8.23. Current feedback pair.

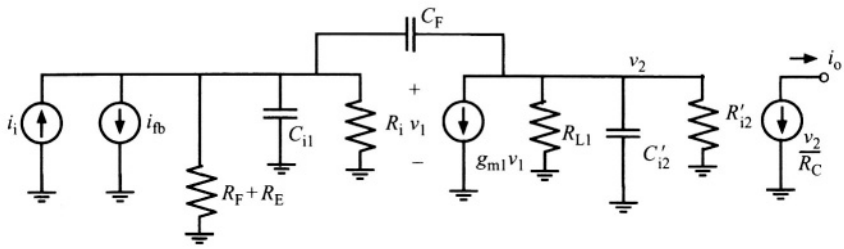


Figure 8.24. Small-signal equivalent of the circuit of Figure 8.23.

and C'_{i2}, respectively and are given by

$$R'_{i2} = (1 + g_{m2}R_C)R_{i2} \tag{8.75}$$

and

$$\begin{aligned} C'_{i2} &= \frac{C_{i2}}{1 + g_{m2}R_C} \\ &\cong \frac{C_{i2}}{g_{m2}R_C} \\ &= \frac{\tau_1}{R_C} \end{aligned} \tag{8.76}$$

for $g_{m2}R_C \gg 1$. Resistors R_{L1} and R'_{i2} are lumped to form R_2. Feedback capacitor C_F includes the inherent feedback capacitance of the input device plus any added capacitance used for frequency compensation.

The forward path gain function of the amplifier is [2]

$$a(s) = \frac{a_o}{(1 - s/p_1)(1 - s/p_2)} \tag{8.77}$$

If $g_{m1}R_1 \gg 1$ and $C_F \ll C_i$, then

$$p_1 \cong -\frac{1}{g_{m1}R_1R_2C_F} \tag{8.78}$$

$$p_2 \cong -\frac{g_{m1}C_F}{C_{i1}C'_{i2}} \tag{8.79}$$

$$p_1p_2 = \frac{1}{R_1C_{i1}R_2C'_{i2}} \tag{8.80}$$

and $|p_2| \gg |p_1|$. Note that as C_F is made larger, the dominant pole p_1 decreases in magnitude and p_2 increases while the product p_1p_2 is constant.

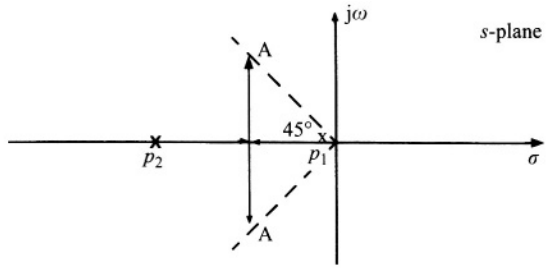


Figure 8.25. Root locus for the circuit of Figure 8.24.

The frequency response of the circuit can be estimated using the root locus [13] of Figure 8.25. As the loop gain is increased from zero, the poles of the circuit transfer function come together and then split out in the s-plane. We assume the loop gain is adjusted to give pole positions as shown at AA at angles of 45° to the real axis. This gives a maximally flat frequency response (no peaking) and a circuit – 3 dB bandwidth equal to the distance from A to the origin. If $|p_2| \gg |p_1|$, this is $|p_2|/\sqrt{2}$. Thus the bandwidth of the circuit is

$$B = \frac{|p_2|}{\sqrt{2}} \tag{8.81}$$

These pole positions give the maximum possible gain–bandwidth without peaking and are set by manipulating the loop gain and the compensation capacitor C_F. Note that a similar compensation function can be achieved by a capacitor connected across R_F. The loop gain required to set the poles in the position AA is [13]

$$T_o = \frac{1}{2}\frac{|p_2|}{|p_1|} \tag{8.82}$$

The mid-band forward gain (current gain) a_o is given by

$$a_o = \frac{g_{m1} R_1 R_2}{R_C} \tag{8.83}$$

From (8.80), we have

$$\begin{aligned} p_1 p_2 &= \frac{1}{R_1 C_{i1} R_2 C'_{i2}} \\ &= \frac{R_C}{g_{m1} R_1 R_2} \frac{g_{m1}}{C_{i1}} \frac{1}{C'_{i2} R_C} \\ &= \frac{\omega_T^2}{a_o} \end{aligned} \tag{8.84}$$

where $\tau_1 = 1/\omega_T = R_C C'_{i2} = C_{i1}/g_{m1}$ has been used. In practice, parasitic capacitance shunting C'_{i2} at the internal node will cause a degradation of device frequency capability and (8.84) becomes $\omega_{T1eff}\omega_{T2eff}/a_o$, where ω_{Teff} is the effective value of ω_T which is realized in practice with parasitic capacitance included.

The mid-band forward gain of the circuit (current gain) with feedback applied is

$$G = \frac{a_o}{1 + T_o} = \left|\frac{i_o}{i_i}\right| \tag{8.85}$$

$$\cong \frac{a_o}{T_o} \tag{8.86}$$

$$= \frac{1}{f} = \frac{R_F + R_C}{R_C} \tag{8.87}$$

Substituting (8.84) and (8.82) in (8.86), we find

$$G = \frac{\omega_T^2}{p_1 p_2}\frac{2|p_1|}{|p_2|}$$

$$= 2\frac{\omega_T^2}{p_2^2} \tag{8.88}$$

Using the multistage gain–bandwidth figure-of-merit defined in (8.10), we find

$$\sqrt{G}B = \omega_T \tag{8.89}$$

using (8.88) and (8.81). Thus, for this two-stage feedback connection, the full device gain–bandwidth per stage is preserved. This is a significant advantage when compared to the gain–bandwidth shrinkage experienced in a cascade of two single stages.

The noise performance of the two-stage amplifier is simply that of the amplifier input device with the addition of thermal noise $\bar{i}_F^2 = 4kT(1/R_F)\Delta f$ due to the feedback resistor. However, due to the extra gain–bandwidth available in the two-stage configuration compared with a single-stage cascade, we find that larger values of R_F can be used in the two-stage amplifier, giving improved noise performance. It should also be noted that the compensation capacitor C_F does not appreciably degrade the circuit noise performance as long as $C_F \ll C_i$.

A two-stage feedback voltage amplifier can be realized using the series–shunt configuration of Figure 8.26. The series feedback at the input gives the stage a high input impedance while the shunt feedback at the output produces a low output impedance. For large loop gain, the overall voltage gain is set by

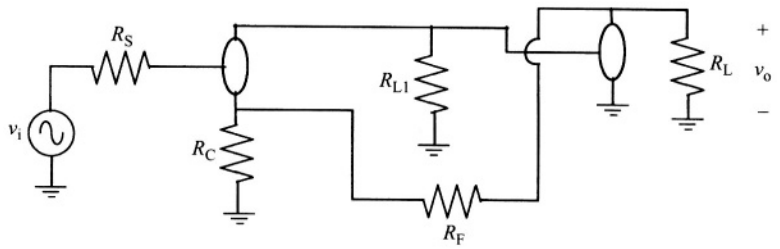


Figure 8.26. Series–shunt feedback voltage amplifier.

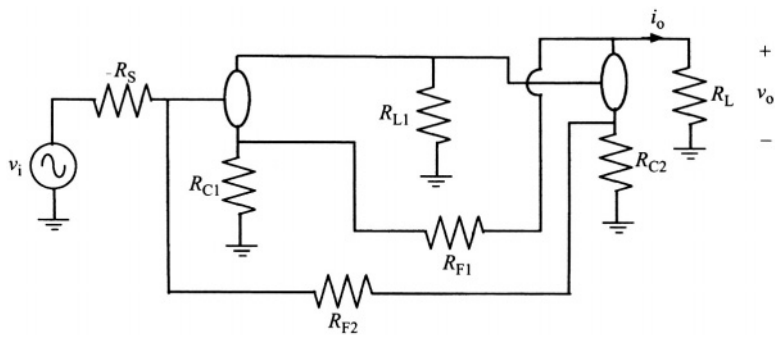


Figure 8.27. Two-stage dual-feedback amplifier.

resistor ratios and is

$$\frac{v_o}{v_i} = \frac{R_F + R_C}{R_C} = G \tag{8.90}$$

If $R_S = R_L$, the gain–bandwidth product is again given by (8.89), where G is now the amplifier voltage gain. In this case, the noise performance is that of the input device with an addition of $\bar{v}^2 = 4kTR_C\Delta f$ to the equivalent input noise voltage.

Finally, in the realm of two-stage feedback amplifiers, we examine the two-stage dual-feedback amplifier shown in Figure 8.27 [16–19]. This is derived by analogy and extension from the single-stage version in Figure 8.22 and incorporates both series–shunt and shunt–series feedback loops. Like the single-stage version of Figure 8.22, the circuit of Figure 8.27 gives excellent gain–bandwidth performance while simultaneously allowing realization of matched terminal impedances with good noise performance. A simplified small-signal equivalent circuit of the amplifier in Figure 8.27 is shown in Figure 8.28 where

$$i_{fb} = i_o \frac{R_{C2}}{R_{C2} + R_{F2}} \tag{8.91}$$

and

$$v_{fb} = v_o \frac{R_{C1}}{R_{C1} + R_{F1}} \tag{8.92}$$

The circuit of Figure 8.28 can be manipulated into the equivalent form of Figure 8.29 where

$$\begin{aligned} C'_{i1} &= \frac{C_{i1}}{1 + g_{m1} R_{C1} \| R_{F1}} \\ &\cong \frac{C_{i1}}{g_{m1} R_{C1}} \\ &= \frac{\tau_1}{R_{C1}} \end{aligned} \tag{8.93}$$

$$R'_{i1} = (1 + g_{m1} R_{C1} \| R_{F1}) R_i \tag{8.94}$$

$$\begin{aligned} g'_{m1} &= \frac{g_{m1}}{1 + g_{m1} R_{C1} \| R_{F1}} \\ &\cong \frac{1}{R_{C1}} \end{aligned} \tag{8.95}$$

$$C'_{i2} \cong \frac{\tau_1}{R_{C2}} \tag{8.96}$$

$$R'_{i2} = (1 + g_{m2} R_{C2} \| R_{F2}) R_i \tag{8.97}$$

$$g'_{m2} \cong \frac{1}{R_{C2}} \tag{8.98}$$

and it is assumed that $R_C \ll R_F$, $g'_m R_C \gg 1$ and $R_{F2} + R_{C2} \gg R_S$.

The circuit of Figure 8.29 is in the form of the ideal feedback configuration of Figure 8.15. The total feedback voltage is

$$\begin{aligned} v_{fbT} &= v_{fb} + i_{fb} R_S \\ &= v_o \left(\frac{R_{C1}}{R_{C1} + R_{F1}} + \frac{R_{C2}}{R_{C1} + R_{F2}} \right) \\ &\cong v_o \left(\frac{R_{C1}}{R_{F1}} + \frac{R_{C2}}{R_{F2}} \right) \end{aligned} \tag{8.99}$$

where $i_o = v_o / R_L$ has been used and $R_S = R_L = R$ assumed. The voltage gain from v_3 to v_o is set by the series–shunt feedback loop and is given by

$$\frac{v_o}{v_3} \cong \frac{R_{F1} + R_{C1}}{R_{C1}} \cong \frac{R_{F1}}{R_{C1}} \tag{8.100}$$

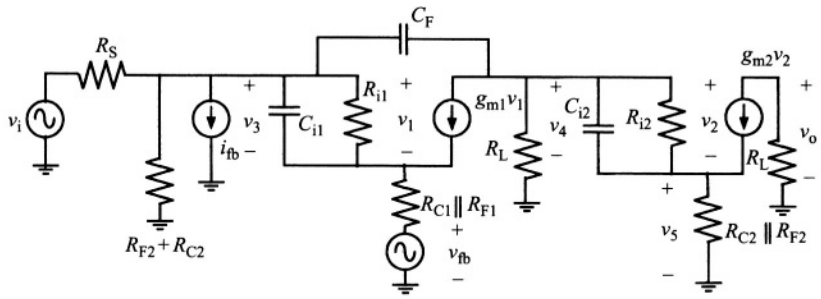


Figure 8.28. Simplified small-signal equivalent circuit for the amplifier of Figure 8.27.

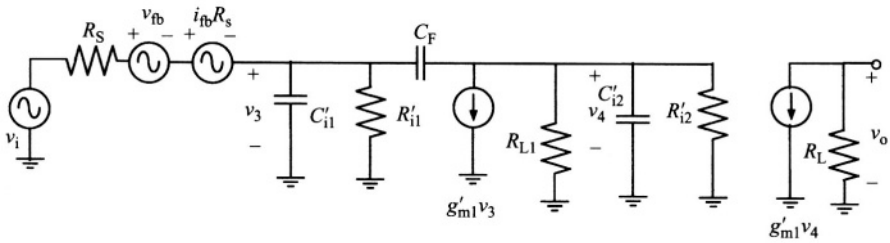


Figure 8.29. Transformation of Figure 8.28.

If the input resistance seen at v_3 is set to match $R_S = R$, then the voltage gain from v_i is

$$\frac{v_o}{v_i} \cong \frac{1}{2}\frac{R_{F1}}{R_{C1}} = G \tag{8.101}$$

The input resistance R_i seen at v_3 can be estimated by a resistive Miller approximation

$$R_i \cong \frac{R_{F2}}{1 + A_v} \tag{8.102}$$

where

$$A_v = \frac{v_5}{v_3} \cong \frac{R_{F1}R_{C2}}{R_{C1}R_L} \tag{8.103}$$

If $A_v \gg 1$, then substitution of (8.103) in (8.102) gives

$$R_i \cong \frac{R_{C1}R_L}{R_{F1}R_{C2}}R_{F2} \tag{8.104}$$

For $R_i = R_L = R$, we require

$$\frac{R_{F1}}{R_{C1}} = \frac{R_{F2}}{R_{C2}} \tag{8.105}$$

Note that in (8.99) this implies that the influence of both feedback loops is equal.

The output resistance can be estimated by driving the output node with a test voltage and calculating the current response. This gives

$$R_o \cong \frac{R_{C2}R_S}{R_{F2}R_{C1}}R_{F1} \tag{8.106}$$

Again, if (8.105) holds, then $R_o = R_S = R$ and we have both input and output ports matched. This circuit has the advantage that since $R_i \propto R_L$ and $R_o \propto R_S$, the input and output ports retain their impedance matches for a range of system impedances [19] (unlike the single-stage dual-feedback circuit where $R_i \propto 1/R_L$ and $R_o \propto 1/R_S$).

Further advantages of the two-stage dual feedback configuration are improved noise performance and gain–bandwidth. A calculation similar to that for the current feedback pair shows that the gain–bandwidth of this circuit is also $\sqrt{G}B = \omega_T$, so that $\sqrt{G}$ can be traded for bandwidth. The noise performance is functionally the same as the single-stage dual feedback configuration except that with two-stage feedback, the values of R_{C1} and R_{F2} (which contribute to the equivalent input noise) can be made smaller and larger respectively, due to the larger loop gain of the two-stage configuration. Thus, their noise contributions can be made lower.

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Chapter 9

FREQUENCY COMPENSATION

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9.1. Introduction

Many electronic designs require frequency compensation, that is, their dynamic behavior needs to be designed. It can be that stability has to be guaranteed for specified conditions or that a specified frequency dependency has to be realized. For a negative-feedback amplifier, for instance, the dynamic behavior of the loop needs to be designed carefully otherwise instability may result. On top of that, a Butterworth type of frequency behavior can be required, for instance.

The design of the frequency behavior can be a tedious job as due to (local) loops, (base–collector (C_μ)/gate–drain (C_{gd}) capacitances, etc.), non-unilateral circuits are obtained. Consequently, poles in the circuit are coupled and frequency compensation is not a local design problem. A systematic way for performing frequency compensation makes the existing trade-offs clear and helps the designer to obtain a high performance in a relatively easy way.

In this chapter, frequency compensation is discussed in the context of negative-feedback amplifiers. What specific constraints apply for the frequency compensation depends on the type of application. Roughly speaking, in this context, negative-feedback amplifiers can be split into two classes:

- general-purpose amplifiers
- dedicated amplifiers.

For general-purpose amplifiers, the dynamic behavior should be designed in such a way that stability is guaranteed for a large range of input and output conditions. This is done by realizing a first-order dynamic behavior [1,2]. For dedicated amplifiers, the source and load conditions are well known and an optimum design of the dynamic behavior can be done for that specific application. In that case, a higher bandwidth is obtained, as the design margins can be much smaller.

In this chapter, frequency compensation is treated with a main focus on dedicated negative-feedback amplifiers. Thus it is assumed that maximum

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bandwidth is required. Techniques presented can be applied to general-purpose amplifiers as well. However, techniques to design first-order behavior, starting from a higher order behavior, are not treated here [3].

In Section 9.2, a definition of frequency compensation is given based on the characteristic equation of a circuit. The model used for describing the feedback is presented in Section 9.3: the asymptotic-gain model. To reduce the change on a unsuccessful frequency compensation, which only wastes design time, it is preferable to have some rule which gives us, before the frequency compensation is performed, an upper limit of the bandwidth that can be obtained with the circuit under consideration. When this upper limit is too low, frequency compensation will not yield the required bandwidth, that is, other measures need to be taken. Such a rule is the Loop-gain-Poles (LP) product. It is described in Section 9.4. This LP product should give a maximum attainable bandwidth that is higher than the required bandwidth, before one should start with the frequency compensation. To ease the frequency compensation, it is performed with the relevant part of the small-signal diagrams only. Specific techniques are described in Section 9.5. These techniques are evaluated in the sense of their influence on the overall performance of the amplifier. When the frequency compensation is realized, the ignored second-order effects are added in order to check whether it was allowed or not to ignore them. If not, counter measures need to be taken. This is described in Section 9.6. To demonstrate the method, Section 9.7 describes the frequency compensation for an example transimpedance amplifier. The chapter ends with conclusions in Section 9.8.

9.2. Design Objective

The dynamic behavior of circuits in general is governed by the characteristic equation. The solutions of this equation are the poles of the circuit, which are called in the remainder of this chapter: the *system poles,* (p_s). For stability all the poles should be in the left half-plane. On top of that for having a specific dynamic behavior, the relative positions of the poles are important. Therefore, frequency compensation is the design of the characteristic equation in such a way that the required pole-pattern is found. Thus, for an amplifier with a transfer $H(s)$:

$$H(s) = \frac{H(0)/\alpha_0}{s^2 + \alpha_1 s + \alpha_0} \tag{9.1}$$

the frequency behavior is designed by giving the constants α_0 and α_1 the appropriate values. This frequency compensation can be a tedious job. In order to reduce the number of design iterations and design time, design rules must help

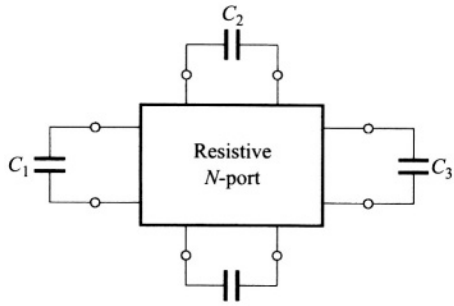


Figure 9.1. A circuit represented by an N-port with N external capacitors.

the designer at a relatively early stage, to tell him/her whether his/her design can succeed or not.

For frequency compensation in general, two approaches can be distinguished:

- using the direct relation between frequency-compensation components and the characteristic equation of the system;
- using an intermediate step between the frequency compensation and the system poles.

An example of the first method is the one described in [4] which is based on Cramer's rules as described in [5]. The method visualizes a circuit as an N-port, where N is the number of capacitors present in the circuit, and the corresponding ports are the terminals, between which the capacitors are connected, see Figure 9.1.

The characteristic polynomial of the circuit is found from relatively simple calculations of port resistances under various conditions, that is, a number of the other ports are shorted. This method is more suited for analysis purposes. It gives no insight into where compensation components have to be added. The correct compensation place has to be found by means of an exhaustive search. This is not permissible for short designing times.

The other method uses an intermediate step in the process of frequency compensation. The most commonly used is the root locus method [6], which implicitly assumes feedback. This method uses the poles found in the loop, that is, the *loop poles,* and the DC loop gain to determine, by means of the construction rules of root loci, the actual *system poles.* As the loop poles are mostly related to explicit RC combinations and the construction rules for the root loci are relatively simple, measures which have to be taken to obtain the desired *system poles* are relatively easy to find.

The frequency behavior of an amplifier can be split into two parts:

- absolute frequency behavior
- relative frequency behavior.

The absolute frequency behavior is proportional to the distance between the poles and the origin, whereas the relative frequency behavior has to do with the final relative pole positions. The absolute frequency behavior is explicitly determined by the speed capability of the constituent devices and the relative frequency behavior is determined by the frequency compensation components. Therefore, the design of the frequency behavior is split into two steps. First, the absolute frequency behavior has to be derived and made large enough and second, the loop poles have to be placed such that the system poles are at the desired relative positions in the *s*-plane.

The *bandwidth* of a system is closely related to the absolute frequency behavior when the poles *have* the desired relative position. For instance, when the relative frequency behavior is of the Butterworth type, the absolute frequency behavior equals the bandwidth of the transfer. In the remaining discussion, the term bandwidth will be used for the absolute frequency behavior, remembering that for the final transfer, the relative positions also have to be realized.

9.3. The Asymptotic-Gain Model

In this chapter, the asymptotic-gain model [7,8] is used to describe the transfer, $A_t(s)$, of negative-feedback amplifiers:

$$A_t(s) = A_{t\infty}(s)\frac{-LG(s)}{1-LG(s)} + A_{t0}(s)\frac{1}{1-LG(s)} \tag{9.2}$$

In this expression, $A_{t\infty}(s)$ is the asymptotic gain, that is, the gain of the amplifier when the active part is a nullor [9] and thus the loop gain (LG) is infinite, $A_{t0}(s)$ is the gain of the amplifier in the situation that the gain of the active part is zero, that is, LG = 0. This models the direct path between source and load. For most cases, $A_{t0}(s)$ can be ignored. This will be done in this chapter.

9.4. The Maximum Attainable Bandwidth

Designing the frequency behavior of an amplifier can be a lengthy job. When a designer has to conclude after a lot of frequency-compensation trials that the bandwidth capability of its amplifier is not high enough to reach the requirements, a lot of time and money is wasted. The LP product [7], which can be seen as a generalized GB product, is a measure for the maximum attainable bandwidth of an *n*th-order system.

9.4.1. The LP Product

Assume that the negative-feedback loop comprises n poles, $p_{li} = a_i + jb_i$ with $a_i < 0$ and j the imaginary unit, as given by:

$$\mathrm{LG}(s) = \frac{\mathrm{LG}(0)}{\prod_{i=1}^{n} (1 - s/p_{li})} \tag{9.3}$$

where LG(0) is the DC loop gain. Then (a part of) the characteristic polynomial, CP, of $A_t(s)$ is given by:

$$\mathrm{CP}(s) = s^n + \cdots + [1 - \mathrm{LG}(0)] \prod_{i=1}^{n} |p_{li}| \tag{9.4}$$

The zeroth-order term is called the LP product for short [7]. A more precise name would be the DC-return-difference-poles product, because the term [1 – LG(0)] is the return difference as defined in [10]. However, for accurate amplifiers, the magnitude of the loop gain is relatively large and the magnitude of the DC loop gain is approximately equal to the magnitude of the DC return difference. Expression (9.4) is found from the root locus point of view. However, of final interest are the system poles. The corresponding part of the characteristic polynomial in terms of the n system poles, $p_{si} = c_i + jd_i$, with $c_i < 0$, equals:

$$\mathrm{CP}(s) = s^n + \cdots + \prod_{i=1}^{n} |p_{si}| \tag{9.5}$$

Here the zeroth-order term is the product of the moduli of all the system poles. Thus this term explicitly describes the absolute frequency behavior of the system. Consequently, the zeroth-order term found in equation (9.4) is a measure of the maximum attainable bandwidth of the corresponding system. When the LP product is considered for a first-order system, it reduces to the Gain–Bandwidth product.

For amplifiers, the Butterworth characteristic is commonly used as relative frequency behavior because it results in a maximum-flat-magnitude transfer. Therefore, in the rest of this chapter, it will be assumed that a Butterworth characteristic is required unless explicitly stated otherwise.

For a Butterworth characteristic, the system poles are regularly placed on a half circle in the left half of the s-plane, see Figure 9.2. For an nth-order system, the half circle is divided into n equal parts and in the middle of each part a pole is located.

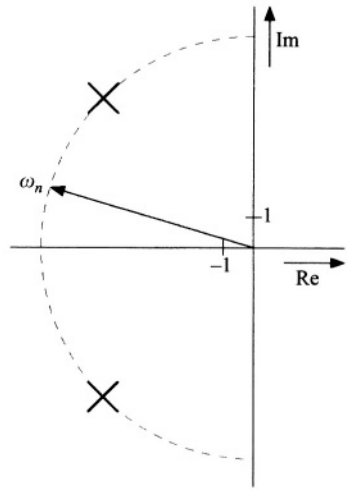


Figure 9.2. The pole positions for a second-order Butterworth system.

For a bandwidth of ω_n, the radius of the circle equals ω_n and thus the modulus of each pole equals ω_n. Applying this to equation (9.5) yields:

$$\mathrm{CP}(s) = s^n + \cdots + \omega_n^n \tag{9.6}$$

Comparing equations (9.4) and (9.6) yields the following relation that holds:

$$[1 - \mathrm{LG}(0)] \cdot \prod_{i=1}^{n} |p_{i1}| = \omega_n^n \tag{9.7}$$

The question is, which poles must be used to calculate this LP product?

Example 9.1. What maximum bandwidth can be expected when the loop comprises three poles, $p_{11} = -1\,\mathrm{kHz}$, $p_{12} = -9\,\mathrm{kHz}$ and $p_{13} = -1\,\mathrm{GHz}$, and the DC loop gain equals – 100?

When the three poles are used to calculate the LP product, the maximum bandwidth, B_{s3}, is found to be: $B_{s3} = \sqrt[3]{101 \cdot 1\,\mathrm{kHz} \cdot 10\,\mathrm{kHz} \cdot 1\,\mathrm{GHz}} \approx 1\,\mathrm{MHz}$. With a bit of experience one knows that the pole at –1 GHz does not belong to the dominant group, that is, it does not contribute to the bandwidth. The maximum bandwidth, B_{s2}, calculated on basis of p_{11} and p_{12} yields: $B_{s2} = \sqrt{101 \cdot 1\,\mathrm{kHz} \cdot 10\,\mathrm{kHz}} \approx 32\,\mathrm{kHz}$, which is about a factor 30 lower than B_{s3}.

That the 1 GHz pole does not contribute to the bandwidth is clear; however, what to do when it was at – 1 MHz? As was stated, the LP product only predicts

the upper limit or the attainable bandwidth when the poles used can be placed into the required relative positions, for this case the Butterworth positions. These poles then contribute to the bandwidth and are, therefore, called the poles belonging to the dominant group, that is, *dominant poles.* Thus, only dominant poles should be used to calculate the LP product.

9.4.2. The Group of Dominant Poles

The following derivation of the dominant poles is not limited to Butterworth behavior; it is generally applicable to other relative frequency behaviors as well. In contrast, the derivation of the dominant poles is limited to loops with only real poles, which will be explained at the end of this section.

To find the dominant poles, the frequency behavior of the system is described again from two points of view. First, the characteristic polynomial is described from the loop point of view, which yields:

$$\mathrm{CP}(s) = s^n - s^{n-1} \sum_{i=1}^{n} p_{li} + \cdots \tag{9.8}$$

with $p_{li} < 0$.

Second, CP(s) is described in terms of the system poles, which yields:

$$\mathrm{CP}(s) = s^n - s^{n-1} \sum_{i=1}^{n} p_{si} + \cdots \tag{9.9}$$

Now the coefficient of the term of order $(n - 1)$ is of interest. Comparing the term of equation (9.8) with the corresponding term of equation (9.9) yields:

$$\sum_{i=1}^{n} p_{li} = \sum_{i=1}^{n} p_{si} \tag{9.10}$$

which states that the sum of the loop poles is equal to the sum of the system poles. From this property, a criterion can be derived for the dominant poles.

The LP product gives a measure of the maximum attainable bandwidth. As the required relative frequency behavior is known, the position of the system poles can be determined and from that their *sum* can be calculated. The *sum* of the loop poles is also known. These sums are generally not equal and frequency compensation has to be used as discussed in the next sections. All the techniques to be discussed have the property of making the sum of the system poles smaller (i.e. more negative, remind that the poles are negative). Thus, when the sum of the loop poles is smaller than the sum of the required system poles, frequency compensation will *not succeed*; the loop poles cannot be placed in the desired

position; at least one loop pole is too far away from the origin. Such a pole will be called a non-dominant pole, that is, not belonging to the group of dominant poles. The most negative pole from the loop has to be ignored and the LP product and the sum of the remaining poles has to be calculated again, etc., until the number of dominant poles is found.

Thus when p_{li} are the poles of the loop and p_{si} are the poles of the system, the dominant poles are the largest set of poles for which holds:

$$\sum_{i=1}^{n} p_{li} \geq \sum_{i=1}^{n} p_{si} \tag{9.11}$$

The sum of the loop poles has to be less negative than the sum of the system poles.

Fulfilling this criterion is necessary but not sufficient. The characteristic polynomial mostly includes more coefficients that must be given the appropriate values. It is not always possible to implement the required frequency-compensation elements in the circuit. In contrast, when the criterion is not fulfilled, it is certain that frequency compensation will not succeed with the given set of poles and loop gain, and the LP product of the set of dominant poles has to be increased. In [8] methods are described for systematically increasing the LP product of an amplifier (increasing bias currents, adding additional amplifying stages).

Example 9.2. For the previous example, the LP product for the third-order system gave a maximum attainable bandwidth of 1 MHz. For a 1 MHz third-order Butterworth system, the sum of the poles equals –2 MHz. The sum of the loop poles is approximately – 1 GHz which is much smaller than – 1 MHz and therefore at least p_{l3} is non-dominant. The maximum attainable bandwidth of the second-order system is 32 kHz. The sum of the loop poles equals – 11 kHz which is greater than the sum obtained from the system poles, –45 kHz. Thus the system has two dominant poles.

At the beginning of this section, the constraint was proposed that all the loop poles have to be real. This is required because for complex poles the contribution to the LP product can be relatively large, whereas the contribution to the sum of the poles is relatively small as only the real parts count; the imaginary parts cancel. These complex poles can cause too optimistic a value for the maximum bandwidth.

Complex poles arise due to:

- LC-resonators
- local feedback loops.

When these complex poles are non-dominant for the overall loop, they still can be dominant for the specific local loop and can even end up in the right-half plane. Intervening in the corresponding local loop should properly damp these poles. Taking measures in the overall loop is likely to have only a slight effect since, at the frequencies for which the overall loop gain is reduced to one, the local loop gain may still be considerable and thus the overall loop can no longer control the local loop.

When the complex poles are dominant, these poles have to be taken into account in the frequency compensation. Either the local loop should be broken in order to end up with real poles to be able to use the LP product and the dominant-pole criterion again, or the Rosenstark method [4] has to be used in which the system poles are directly manipulated; it does not use the notion of feedback and, therefore, it can be used for very complex networks.

A totally different strategy is to accept the number of loops and use techniques for designing the frequency behavior of multi-loop amplifiers. As these techniques are not well established yet and they are beyond the scope of this chapter, they are not discussed here.

Further, the dominant-pole criterion is derived from the assumption that only compensation techniques are available which reduce the sum of the system poles. However, techniques also exist for increasing the sum of the system poles. These techniques use either negative feed forward, resulting in zeros in the right-half plane, or positive feedback. These techniques have the property of reducing stability and are, therefore, less favorable and not used here.

9.5. Pole Placement

In the previous sections the maximum attainable bandwidth of an amplifier was found. Nothing was said about either *how* to reach this bandwidth or the *possibility* of reaching it. The only thing that can be said is that when the LP product is too low, it is not possible to reach the required bandwidth at all.

This section discusses the *placement* of the poles, that is, obtaining the required relative frequency behavior. The frequency compensation techniques should preferably not reduce the LP product as then bandwidth capabilities are reduced. To ease the frequency compensation any further, the small-signal diagram for the active devices is limited to the relevant part only [8], see Figure 9.3.

After the frequency compensation using these simple models, the models can be gradually extended with second-order effects. When a second-order effect has a non-negligible influence, measures should be taken. This is discussed in Section 9.6.

In this chapter, frequency compensation is assumed to be the addition of *passive networks* to a circuit in order to alter the position of system poles. The

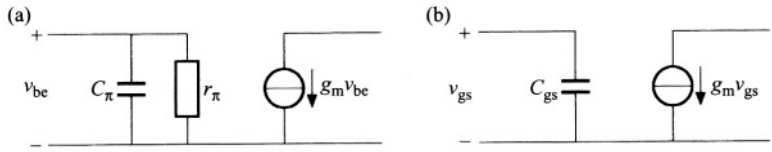


Figure 9.3. The relevant small-signal model for active devices, (a) The bipolar transistor and (b) the field-effect transistor.

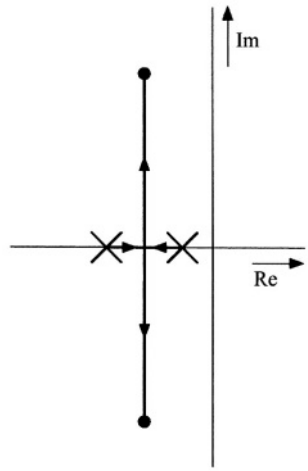


Figure 9.4. A typical root locus of a non-compensated second-order amplifier.

simplest situation occurs in the case of two poles.[1] Figure 9.4 depicts a typical root locus of a second-order non-compensated amplifier.

Clearly, the sum of the loop poles is too high for obtaining system poles that are in the Butterworth position. Consequently, the system poles become relatively complex. To obtain Butterworth behavior, the sum of the poles has to be reduced. Four different techniques can be applied for this, see Figure 9.5.

Figure 9.5(a) depicts the situation in which the real part of *one* pole is reduced. As the compensation networks are passive and thus cannot increase the LP product, this action inherently reduces the DC loop gain. An example of this method is resistive broadbanding.

Figure 9.5(b) depicts the situation in which *two* poles are split. One pole is shifted to the origin, which is done by an additional element in the circuit. For frequencies beyond the second original pole, the influence of this extra element

[1] Frequency compensation of a first-order system is not necessary as it reaches the bandwidth given by the LP product without compensation techniques.

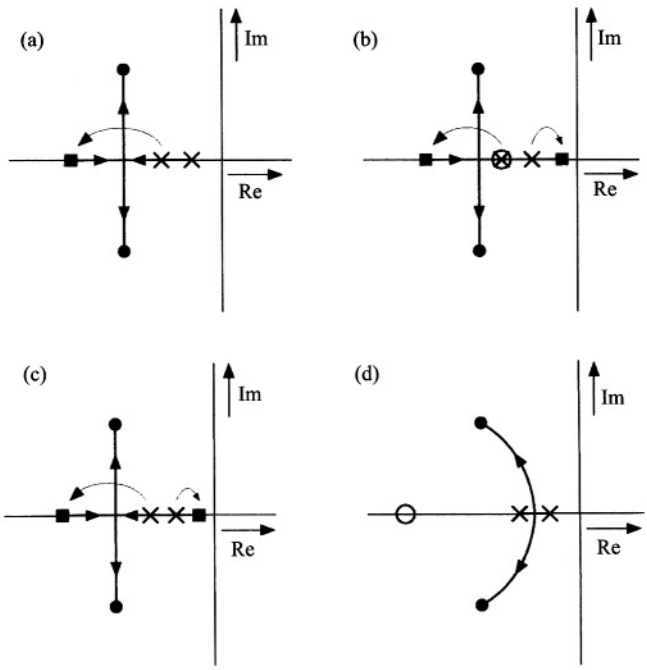


Figure 9.5. Four techniques to alter the pole pattern of an amplifier.

is gradually reduced, resulting in a zero canceling this second pole and finally, when the influence is completely canceled, a new pole is found. This pole is a factor δ away from the original second pole, which equals the factor by which the original first pole was shifted to the origin. Thus, the sum of the poles is reduced and the LP product is not degraded. An example of this method is pole–zero cancelation.

Figure 9.5(c) depicts pole splitting which introduces interaction between the *two* poles such that they split. No intermediate zero is used. An example is the technique called pole splitting.

Figure 9.5(d) shows the use of a zero to bend the root locus. In contrast to the earlier techniques, this method alters the position of the system poles by influencing the root locus without altering the position of the loop poles. In order to obtain an all-pole system transfer, this zero has to be a phantom zero [6]. Further, the techniques depicted in Figure 9.5(a)–(c) only influence at most two poles, whereas the phantom zero technique of Figure 9.5(d) can exert an influence on all the poles.

For higher order systems, a combination of these techniques can be applied. Generally, for an nth order system, $n-1$ frequency compensations are required.

In the following sections, the four techniques are discussed and the influence on the LP product is derived.

9.5.1. Resistive Broadbanding

Resistive broadbanding acts on one pole only. The basic idea of resistive broadbanding is depicted in Figure 9.6. With a compensation network, a single pole is shifted further from the origin. The factor by which the DC loop gain reduces is equal to the factor by which the pole has shifted downwards.

Resistive broadbanding can be realized in two ways, passive and active. Figure 9.7 shows a passive implementation. The original pole shifts a factor $1 + r_\pi/R_{BR}$ downwards, the DC loop gain is reduced by the same factor and thus the LP product remains the same. Adding base resistances to the model reduces the LP product by a factor:

$$\frac{LP_{before}}{LP_{after}} = 1 + \frac{r_b}{R_{BR}} \tag{9.12}$$

where r_b is the base resistance. In the original case, that is, without R_{BR}, for relatively high frequencies, the complete input current, i_i, flows through r_π and C_π. In the case of a finite R_{BR}, for relatively high frequencies, input current i_i divides over R_{BR} and r_b giving a reduction of the gain the stage contributes to the overall amplifier loop gain. This current division can be removed by adding an inductor in series with R_{BR} [7], resulting in the original LP product.

This method of implementing resistive broadbanding has two drawbacks. First, the gain by which the overall loop gain is reduced is totally wasted; the

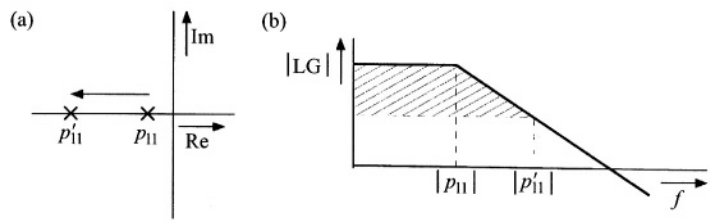


Figure 9.6. The basic idea of resistive broad banding. The influence on (a) the pole–zero plot and (b) the loop gain.

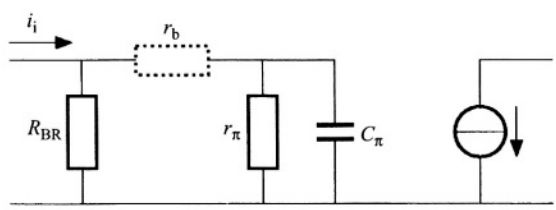


Figure 9.7. A passive implementation of resistive broadbanding.

dashed area in Figure 9.6 indicates this. Nothing is done with it, resulting in an increased distortion level. Second, for relatively low values of R_{BR}, the LP product reduces considerably.

Resistive broadbanding by means of local feedback does not have these drawbacks. An example is given in Figure 9.8. By means of the current-feedback network, the asymptotic gain of the differential pair is reduced to:

$$\frac{i_o}{i_i} = 1 + \frac{R_1}{R_2} \tag{9.13}$$

and a result of the local feedback, the bandwidth of this stage increases. The method is elucidated by the Bode plot of Figure 9.9.

The thick line indicates the original transfer and the thin line is the asymptotic gain for the local loop. At the intersection point of these two lines, the loop gain is 1 and the new pole is found, p'_{11}. Now the loop gain reduction is not wasted but is used in a local feedback, this local stage is linearized. However, as the total loop gain is reduced, the nonlinearities of other stages are less suppressed, resulting in a slight increase of their distortion.

The new pole position is found at approximately:

$$p'_{11} \approx p_{11} \cdot \frac{R_2}{R_1 + R_2} \tag{9.14}$$

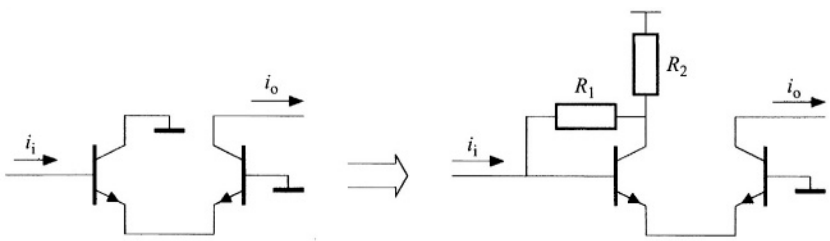


Figure 9.8. Resistive broadbanding by means of local feedback.

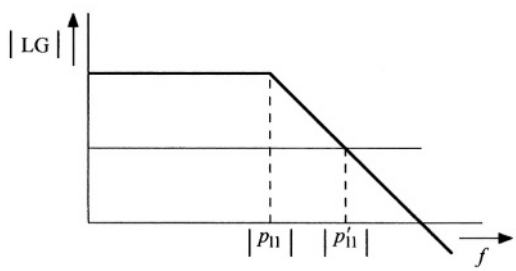


Figure 9.9. The Bode plot for resistive broadbanding by means of a local loop.

The main difference with the previous type of implementation is that the impedance level of the feedback network can freely be chosen, up to a certain extent, of course. From exact calculations, the following reduction factor of the LP product is found:

$$\frac{\mathrm{LP_{before}}}{\mathrm{LP_{after}}} \approx 1 + \frac{2r_b}{R_1 + R_2} \tag{9.15}$$

where r_b is the base resistance of one transistor and assuming that $R_2 \pi 1/g_m, r_b$ $(R_1 + R_2)$ and the DC loop gain of the local loop is much larger than one. The LP product reduction is now caused by the remaining high frequency current division between the input impedance of the differential pair, $2r_b$, and the series connection of the two feedback resistors, $R_1 + R_2$.

9.5.2. Pole–Zero Cancelation

Pole–zero cancelation is a method for splitting two poles, that is, the sum of the poles reduces. The principle is depicted in Figure 9.10. One pole is shifted to the origin; as a result a zero can be created to cancel another pole and inherently, a new pole is found because the LP product cannot increase. Figure 9.11 shows a straightforward implementation of pole–zero cancelation.

With a capacitor, a pole is shifted closer to the origin, p'_{11}. When at higher frequencies, the influence of this capacitor is nullified again by a resistor, a zero is obtained, n_1. With this zero, another pole p_{12} can be canceled. For even

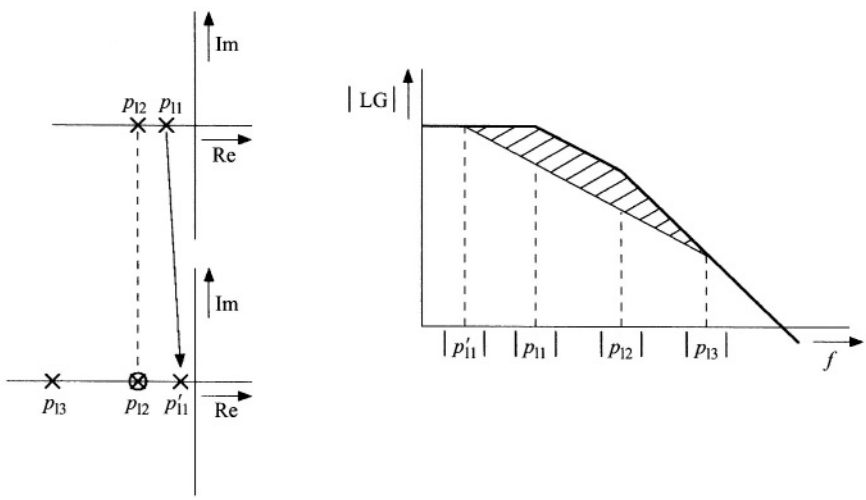


Figure 9.10. The principle of pole–zero cancelation.

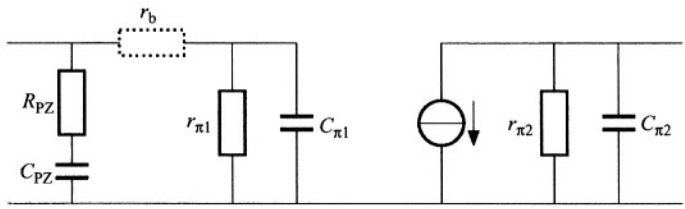


Figure 9.11. A straightforward implementation of pole–zero cancelation.

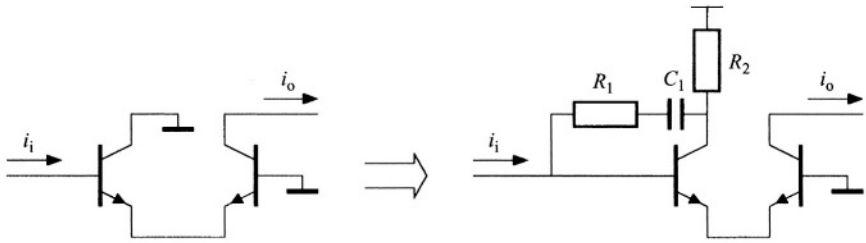


Figure 9.12. Pole–zero cancelation by means of local feedback.

higher frequencies, R_{PZ} and C_π result in a new pole, p_{13}. When calculating the two new poles, assuming that the zero cancels pole p_{12}, it is easily found that the LP product does not change.

Again introducing the base resistances, the loop gain reduces by a factor:

$$\frac{LP_{before}}{LP_{after}} = 1 + \frac{r_b}{R_{PZ}} \tag{9.16}$$

By using the pole–zero cancelation in a local feedback configuration, the influence of the base resistance and the effect of reduced loop gain (cf. resistive broadbanding) are diminished. This principle is depicted in Figure 9.12.

This figure depicts a single-side driven and loaded differential pair. The pole–zero cancelation is implemented by means of R_1, R_2 and C_1, which realize a frequency-dependent current feedback. The influence on the Bode plot is depicted in Figure 9.13.

Originally, the current transfer of the differential pair equals the current-gain factor β_f, with a pole at f_T/β_f; the thick line in Figure 9.13. The thin line indicates the asymptotic gain of this stage including the local feedback. At the intersection points of the thin and thick line, the loop gain is again 1 and the actual poles of the new transfer are found. The zero in the asymptotic gain is at a frequency for which the loop gain is relatively high and thus this zero is

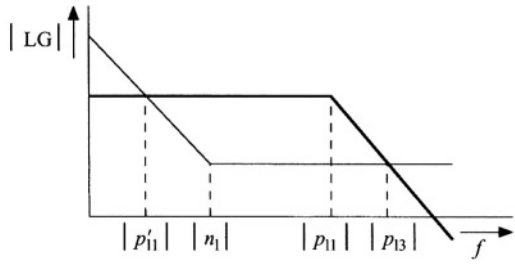


Figure 9.13. The effect of local feedback on the transfer of a differential pair.

also found in the new transfer. It is given by:

$$n_1 = \frac{-1}{2\pi C_1(R_1 + R_2)} \tag{9.17}$$

With this zero, a pole of another stage can be canceled. The influence of the base resistance for this type of pole–zero cancelation is also significantly reduced; the decrease in LP product is only:

$$\frac{\text{LP}_{\text{before}}}{\text{LP}_{\text{after}}} = 1 + \frac{2r_b}{R_1 + R_2} \tag{9.18}$$

which is the same result as was found for resistive broadbanding implemented by means of local feedback. This is easily understood when it is noticed that for relatively high frequencies, the two stages tend to the same equivalent circuit.

9.5.3. Pole Splitting

Pole splitting is a technique that splits two poles by introducing an interaction between them by means of a local loop. The principle is depicted in Figure 9.14. The poles are split apart while their product, ideally, remains constant such that the LP product is not changed. In Figure 9.15, an example is given of pole splitting.

Capacitor C_{SP} acts as a Miller capacitance, the poles at the input and output are split by means of local feedback. The reduction of the LP product can readily be found to be equal to (ignoring r_b for the moment):

$$\frac{\text{LP}_{\text{before}}}{\text{LP}_{\text{after}}} = 1 + C_{SP}\left(\frac{1}{C_1} + \frac{1}{C_2}\right) \tag{9.19}$$

The more the poles are split, the lower the LP product becomes. The level of splitting is determined by C_{SP} and by the voltage gain between the two nodes over which C_{SP} is connected. For higher voltage gains, C_{SP} can be smaller in

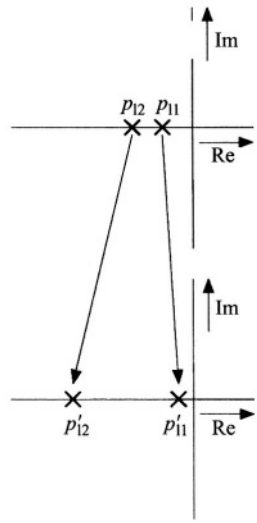


Figure 9.14. The principle of pole splitting.

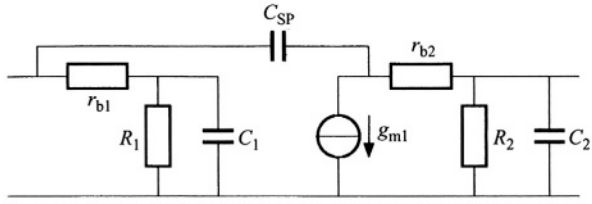


Figure 9.15. Pole splitting in a circuit.

order to end up with the same amount of splitting, and thus less LP product is lost. Therefore, stages with a high voltage gain are the best stages to introduce this type of pole splitting.

Introducing the base resistances in the circuit results in the following approximated expression for the LP-product reduction:

$$\frac{\mathrm{LP}_{\mathrm{before}}}{\mathrm{LP}_{\mathrm{after}}} = 1 + C_{\mathrm{SP}}\left(\frac{1}{C_1} + \frac{1}{C_2}\right) + g_{\mathrm{m1}} r_{\mathrm{b2}} \frac{C_{\mathrm{SP}}}{C_1} \tag{9.20}$$

in which it is assumed that the driving impedance for the input is negligibly large, and the base resistances are relatively small compared to R_1 and R_2. Clearly, the reduction due to the base resistances can be ignored for a relatively low g_{m}.

Compared to pole–zero cancelation, this method requires less capacitance to achieve the same splitting as the voltage gain of a stage is used. However, pole

splitting by means of realizing an interaction costs more LP product. Further, due to C_{SP}, a right-half plane zero is introduced. The stage is no longer unilateral which can be a severe problem for the stability.

There are several methods for reducing the effect of this right-half plane zero. In [11], the use of a voltage follower is described in order to obtain a unilateral stage; the zero is *removed.* In [3], a series resistor is used to *compensate* for the zero. This resistor has to be equal to $1/g_m$. However, as the collector current of the transistor is not constant as a result of an applied signal, g_m varies and perfect compensation of the zero is not achieved. The resulting pole–zero doublet is disadvantageous for the settling time of the amplifier. In [12], the different active buffering techniques are summarized. In [13], a different method is introduced. Here multipath techniques are used to *remove* the right-half plane zero.

The active buffer techniques and the multipath techniques completely remove the zero while the technique using the resistor compensation does not. The effect of the compensation technique is studied here in more detail. With the additional resistor, R_{SP}, see Figure 9.16, the zero is found at:

$$n_1 = \frac{+1}{2\pi C_{SP}\,(1/g_{m1} - R_{SP})} \tag{9.21}$$

For the zero there are three possibilities:

- $R_{SP} < 1/g_{m1}$: zero in RHP
- $R_{SP} = 1/g_{m1}$: zero at infinity
- $R_{SP} > 1/g_{m1}$: zero in LHP.

This third case seems to be the most advantageous, pole splitting and a LHP zero. However, when calculating the characteristic polynomial, a third pole is found at:

$$p_{13} = \frac{-1}{2\pi R_{SP} C_{SP}} \cdot \left[1 + C_{SP}\left(\frac{1}{C_1} + \frac{1}{C_2}\right)\right] \tag{9.22}$$

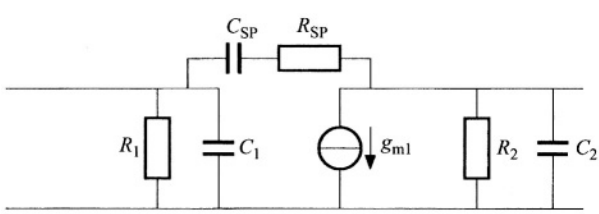


Figure 9.16. The compensation of the right-half plane zero by a resistor.

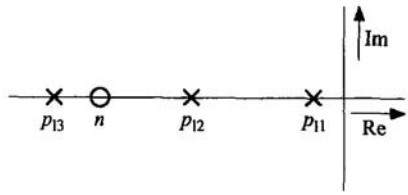


Figure 9.17. The pole–zero plot for pole splitting with $R_{SP} > 1/g_{m1}$.

with the last factor equal to the factor of equation (9.19). For relatively small split capacitors, the pole is found at:

$$p_{13} = \frac{-1}{2\pi R_{SP} C_{SP}} \tag{9.23}$$

With exact compensation, $g_{m1} = R_{SP}$, the zero in the RHP vanishes, but an additional pole is found at the same position in the LHP. The additional loop gain due to the RHP zero is changed in a loop-gain reduction whereas the additional phase shift remains.

For the third situation, the pole–zero pattern of Figure 9.17 applies. The zero is now found in the LHP closer to the origin than the third pole. The fraction between this pole and zero equals the factor by which the LP product is reduced, equation (9.19). For relatively small split capacitors, the pole and zero cancel each other. For a relatively large capacitor, that is, the case that a considerable part of the LP-product is lost, the pole and zero are a reasonable factor apart.

9.5.4. Phantom Zeros

Phantom zeros [6] are zeros that are realized in the feedback factor β, [7]. This means that they can be realized in the feedback network, at the input of the amplifier or at the output of the amplifier. Note that they are realized *outside* the active part of the amplifier. In the case of a zero, n, in β, the relevant part of the asymptotic-gain model is given by:

$$A_t(s) = \frac{1}{\beta(0)(1 - s/n)} \cdot \frac{-LG(s)(1 - s/n)}{1 - LG(s)(1 - s/n)} \tag{9.24}$$

As can be seen, the pole in the denominator of the asymptotic-gain part cancels with the zero in the numerator of the second factor. Note that β is a part of the loop. The effect of the zero is not found in the asymptotic gain, which is why it is called a *phantom* zero. In contrast, it is found in the denominator of the second factor and can, therefore, be used for the frequency compensation. The characteristic polynomial of a second-order system when one phantom zero is

introduced is given by:

$$\mathrm{CP}(s) = s^2 - s\left[p_{11} + p_{12} - \frac{\mathrm{LG}(0)\,p_{11}\,p_{12}}{n_1}\right] + p_{11}\,p_{12}\,[1 - \mathrm{LG}(0)] \quad (9.25)$$

As can be seen, the LP product does not change as a result of the phantom zero. Of course, when a phantom zero is practically realized, influences via base resistances, and so on, may also occur. However, the phantom zero is generally near the band edge of a system and, therefore, the resulting second-order effects will be far beyond the band edge. For an nth-order system, $(n - 1)$ phantom zeros are required to alter the sum of the system poles.

A phantom zero is realized when attenuation in the feedback network is nullified beyond a certain frequency. The level of the attenuation that is nullified determines the effectiveness of the phantom zero. The higher this attenuation is, the more effective this phantom zero is. This can be seen when the unavoidable accompanying pole is examined. Assume that in β a reduction of a factor δ is canceled beyond a frequency corresponding to the zero n. Then the accompanying pole is given by:

$$p = n \cdot \delta \quad (9.26)$$

This is in the case of a single phantom zero; the reduction is removed by means of a first-order behavior. An example is given in Figure 9.18. Originally, the current from the feedback resistor, R_{fb}, was divided between C_{s} and C_{i}. This resulted in a reduction of $(1 + C_{\mathrm{s}}/C_{\mathrm{i}}) = \delta$. With resistor R_{ph}, the current path via C_{s} is made less favorable with respect to the current path via C_{i} beyond the frequency f_{ph}:

$$f_{\mathrm{ph}} = \frac{1}{2\pi R_{\mathrm{ph}} C_{\mathrm{s}}} \quad (9.27)$$

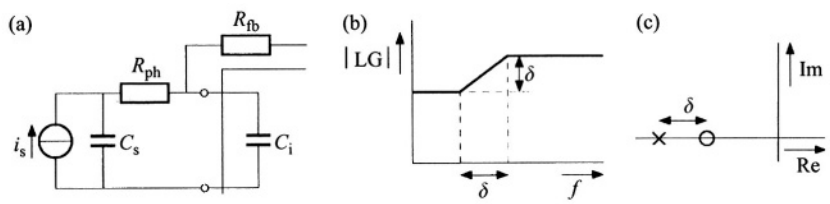


Figure 9.18. An example of the effectiveness of a phantom zero, (a) The realization of a phantom zero by R_{ph}, (b) the influence on the magnitude of the loop gain and (c) the pole–zero plot.

The accompanying pole is found at:

$$p = \frac{-1}{2\pi R_{ph} C_s C_i/(C_s + C_i)} \tag{9.28}$$

This pole is a factor δ away from the phantom zero.

9.5.5. Order of Preference

From the previous it may become clear that the following order of preference for the different compensation is the most likely:

1 phantom zero

2 pole splitting

3 pole–zero cancelation

4 resistive broadbanding.

Phantom zeros do not change the LP product. This way of frequency compensation often only influences the circuit behavior at the band edge and beyond. The other techniques influence the loop gain in the amplifier band (cf. the difference of changing the loop poles and bending the root locus, see Figure 9.5). Further, these methods have a negative influence on the LP product.

As pole splitting uses local feedback, the overall reduction of the loop gain in the corresponding part of the band is used to linearize the corresponding stage. For a passive implementation of pole–zero cancelation and resistive broadbanding the fraction by which the loop gain reduces in the corresponding band is not used. This difference is distinctive for active and passive techniques. When for the pole–zero cancelation and resistive broadbanding active implementations are used, this drawback is not apparent any longer. On top of that, for active implementations, the influence of base resistances is less.

9.6. Adding Second-Order Effects

When the frequency compensation based on the simple models is done, this simplification needs to be checked by adding one by one the C_μs, the output resistances (r_o) and the base resistances (r_b), and the equivalent model components for FETs. When a C_μ or a r_o introduces an unacceptable change in the pole positions, the load impedance of the corresponding transistor needs to be made relatively low. This can be done by a current follower, see Figure 9.19.

As a result of this current follower, r_o is shorted and C_μ is in parallel with C_π. The zero due to C_μ is still at $+g_m/C_\mu$. Thus when the current follower does not make the influence of C_μ negligible, either it cannot be neglected with respect to C_π or the zero cannot be ignored. For the first effect C_μ can be reduced by

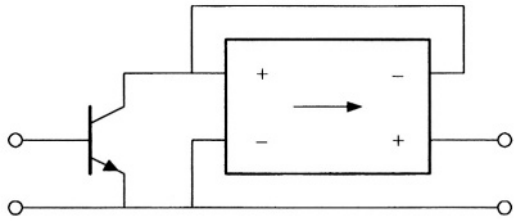


Figure 9.19. A transistor cascaded by an ideal current follower.

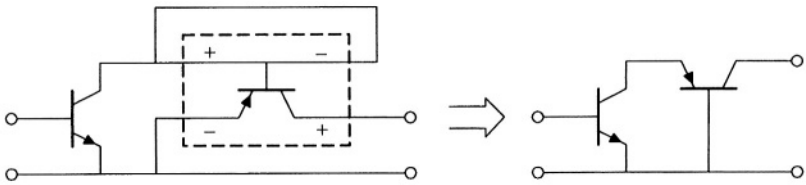


Figure 9.20. A single-stage implementation for the nullor.

increasing the reverse base–collector bias (C_μ is a junction capacitor) or instead of C_π, $C_\pi + C_\mu$ should be used in the frequency compensation. Reducing the effect of the zero can be done by: reducing C_μ as before, increasing g_m, canceling the zero (see Section 9.5.3). If none of these methods is possible, the zero must be taken into account in the frequency compensation.

Increasing the impedance of the driving stage can reduce the effect of base resistances. A current follower preceding this stage can realize this. Of course, no passive frequency compensation network should be connected to this base terminal; otherwise, the effect of the high driving impedance is nullified.

When the required current followers are found, they can be implemented, Figure 9.20. In this figure, the nullor is implemented by a single bipolar transistor resulting in a CB stage. Of course, other implementations are also possible (FETs, multi-stage). When the g_m of the CB stage is equal to the g_m of the CE stage, the result is $+2C_\mu$ adds to C_π and the output resistance is βr_o, with β the current-gain factor of the CB stage. Further, the CB stage adds a pole at f_T to the loop.

9.7. Example Design

Suppose the transimpedance amplifier of Figure 9.21 is to be implemented. After implementation of the input and output stage on noise and output capability constraints [8], the signal diagram of Figure 9.22 can be obtained. For this amplifier, 2N3904 devices are used.

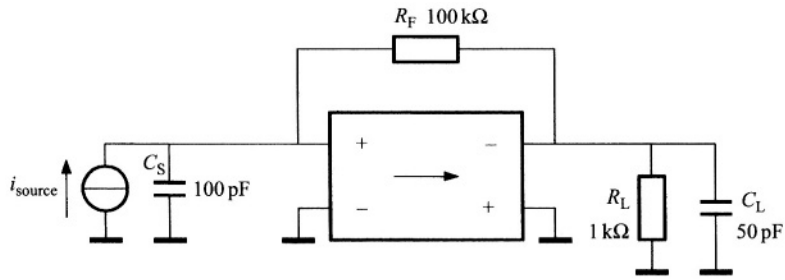


Figure 9.21. A transimpedance amplifier with source capacitance (C_S), load impedance (R_L, C_L) and feedback resistor (R_F).

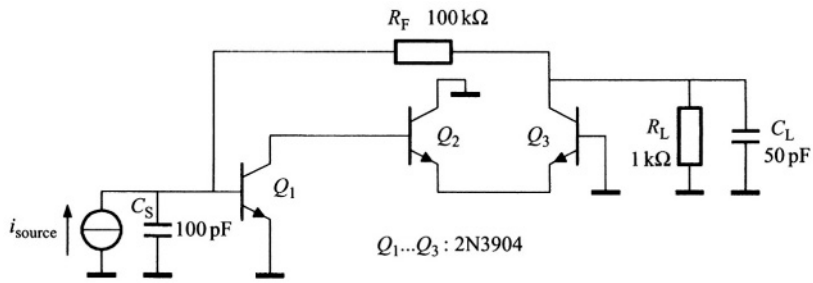


Figure 9.22. Signal diagram of the transimpedance amplifier with an implementation for the input and output stage.

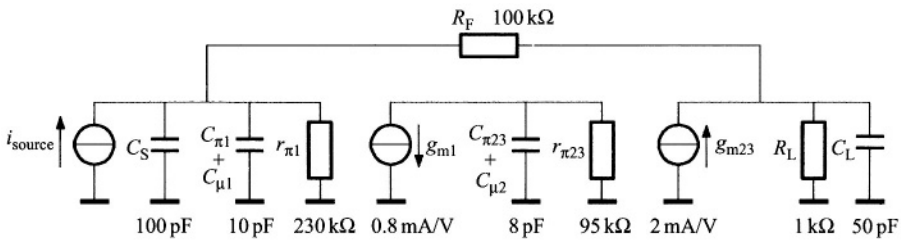


Figure 9.23. Small-signal diagram of the transimpedance amplifier of Figure 9.22.

The transistors are assumed to be biased at 20, 100 and 100 μA for transistor Q_1, Q_2 and Q_3, respectively. For frequency compensation purposes, the small-signal diagram of Figure 9.23 is used. In this diagram, the minimum effect of $C_{\mu 1}$ and $C_{\mu 2}$ are accounted for in $C_{\pi 1}$ and $C_{\pi 23}$, respectively.

For this network, the DC loop gain and the loop poles are found from calculating the transfer from current source g_{m1} via the loop, to the voltage across $r_{\pi 1}$.

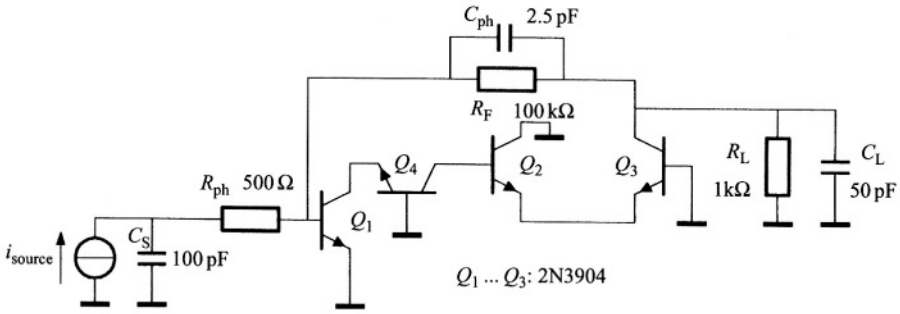


Figure 9.24. The amplifier with frequency compensation.

Multiplying this by g_{m1} yields the loop gain.[2] The DC loop gain [LG(0)] and loop poles (p_l) are given by:

- LG(0) = –104
- $p_{l1} = -21\,\text{kHz}$
- $p_{l2} = -220\,\text{kHz}$
- $p_{l3} = -2.9\,\text{MHz}$.

From the third-order LP product, a maximum bandwidth of 1.1 MHz is found. For a third-order Butterworth system with this bandwidth, the sum of the poles is –2.2 MHz. The sum of the loop poles is lower so it is not a third-order system. The second-order LP product gives a maximum bandwidth of 700 kHz. The sum of the corresponding Butterworth poles is – 1 MHz. Thus this system is a second-order system. In order to prevent the third pole from influencing the root locus, it is taken away from the loop by means of a phantom zero. In this way, the pole is placed now in the asymptotic gain. This phantom zero is realized at the input by means of a resistor $R_{ph} = 500\,\Omega$, see Figure 9.24. Subsequently, to place the two remaining poles in Butterworth position, a phantom zero is required at –650 kHz (equation (9.25)). This is realized by $C_{ph} = 2.5\,\text{pF}$. At this point, the system poles are found at: $p_{s1,2} = -500(1 \pm \text{j})\,\text{kHz}$. After adding the second-order effects one by one, it appears that only $C_{\mu 1}$ has a considerable influence. The system poles move to: $p_{s1,2} = -470 \pm \text{j}275\,\text{kHz}$. After adding a current follower and implementing it by a CB stage (Q_4), the system poles are: $p_{s1,2} = -490 \pm \text{j}510\,\text{kHz}$. Thus the bandwidth indicated by the LP product is

[2] In this calculation, the current source g_{m1} is assumed to be independent. For calculating the loop gain, the loop has to be broken. When chancing the controlled source to an independent source this is realized without chancing the topology.

closely reached. The effect of $C_{\mu 4}$ of transistor Q_4 has already been taken into account in this result. It is assumed that $C_{\mu 2}$ and $C_{\mu 4}$ are halved by applying the required reverse bias. The amplifier with the frequency compensation is shown in Figure 9.24.

It should be noted that R_{ph} introduces noise at the input of the amplifier. An alternative is to cancel the third pole by means of a phantom zero realized in the feedback network and to do the frequency compensation of the second-order system by means of pole splitting. In this case, the poles need to be split by a factor 4. As the voltage gain for transistor Q_1 is about 75 $(g_{m1}r_{\pi 23})$, this requires a capacitor of (split–factor – 1) times $(C_S + C_\pi)$/voltage gain = 4 pF. From equation (9.19) follows a LP reduction of about a factor 1.5. So, this is with respect to bandwidth less optimal.

9.8. Conclusion

In this chapter, the structured design of the frequency performance of a negative-feedback amplifier is discussed. It consists of two steps: first the LP product, which is a measure of the maximum attainable bandwidth, must be made high enough. This requires the identification of the group of dominant poles. Second, after realizing a sufficient LP product, the poles have to be placed to end up with the required relative frequency behavior, for instance Butterworth behavior.

The frequency compensation is done using the relevant part of the small-signal models only. Four types of frequency compensation techniques have been discussed and their influence on the LP product was investigated. The order of preference is:

- phantom zeros
- pole splitting
- pole–zero cancelation
- resistive broadbanding.

Finally, it was shown how current followers could validate the use of simple models in the process of frequency compensation.

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Chapter 10

FREQUENCY-DYNAMIC RANGE-POWER

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10.1. Introduction

A certain level of noise affects every electronic system. The lower limit of noise is due to the thermal agitation energy kT of electrons or due to shot noise, which both display a constant spectral density (white noise) up to very high frequencies. The corresponding noise power N is thus proportional to the noise bandwidth Δf_N, which is always equal to or larger than the usable signal bandwidth Δf of the system.

The power S of the output signal must be large enough to achieve the required signal-to-noise ratio S/N. Although S/N and the dynamic range DR of a circuit should be distinguished from each other, as will be explained in Section 10.4, these two values are often closely related. Indeed, if N has a constant value independent of S, then DR is proportional to $(S/N)_{\max}$. Except for purely passive systems, the signal power is extracted from the power P delivered by the source of energy. Therefore, the factor

$$K = \frac{P}{kT \cdot \Delta f \cdot S/N} \tag{10.1}$$

has a lower limit $K_{\min}$. Thus, $1/K$ can be used as a factor of merit to compare various circuit solutions with respect to their power efficiency. This equation makes explicit the fundamental trade-off that exists between power consumption, signal-to-noise ratio and available signal bandwidth.

The knowledge of $K_{\min}$ is useful for *a priori* discarding impossible specifications, for assessing the merit $K/K_{\min}$ of a particular solution, and for evaluating its potential for improvement. However, knowing this lower limit does not necessarily provide the solution to reach it.

The value of $K_{\min}$ does not depend on the process used, but may depend on the function to be implemented, and on the approach used for its implementation, as will be shown in Section 10.2. The value of K that is achieved

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in a particular realization is affected by various process-dependent limitations, which will be discussed in Section 10.3.

In this chapter, we will evaluate K_{min} for a variety of standard building blocks. Of the many possible variants of a circuit function, we have attempted to choose ones that our intuition tells us will provide the lowest K_{min} among known techniques. This is no rigorous proof that the derived K_{min} is, indeed, the minimum possible, although intuition and experience suggest that it might well be. As a rule, we evaluate circuits that are as simple as possible or that provides results as simple as possible and we aim at simple, intuitively appealing results. Due to space limitations, several steps have to be skipped.

10.2. Fundamental Limits of Trade-Off

10.2.1. Absolute Lower Boundary

Since all physical systems are frequency limited, the most elementary electronic function is a single-pole low-pass filter.

As illustrated in Figure 10.1, the single-state variable of such a filter is the voltage across a capacitor *C*. This capacitor is charged and discharged at the frequency *f* of the signal by means of a transconductance amplifier G_m in unity gain configuration. It is assumed to have a current efficiency of 100% (class B operation): the current *i* supplied by the voltage source V_B (between rails *V*+ and *V*– of the power supply) is entirely used to recharge the capacitor. If V_{pp} is the peak-to-peak amplitude of voltage *v* across *C*, the average value of *i* is fCV_{pp} and the average power *P* delivered by the source of energy is

$$P = V_B f V_{pp} C = \frac{V_B}{V_{pp}} f V_{pp}^2 C \tag{10.2}$$

The noise current power spectral density at the output of the transconductor can be expressed as

$$S_{Ni} = 4kT\gamma G_m \,^{1} \tag{10.3}$$

where γ is the "excess noise factor". Thus the circuit is equivalent to a resistance $1/G_m$ across capacitor *C*, but with noise, which would correspond to a resistor of value $1/(\gamma G_m)$; the total mean square noise voltage is thus $\gamma kT/C$ [1]. Assuming a minimum value of $\gamma = 1$ (the absolute minimum possible is 0.5 for a non-degenerated bipolar transistor, but the related transconductance amplifier is strongly nonlinear), the signal-to-noise ratio is:

$$S/N = \frac{V_{pp}^2/8}{kT/C} \tag{10.4}$$

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1 *S* with a subscript is power spectral density, and without a subscript is signal power.

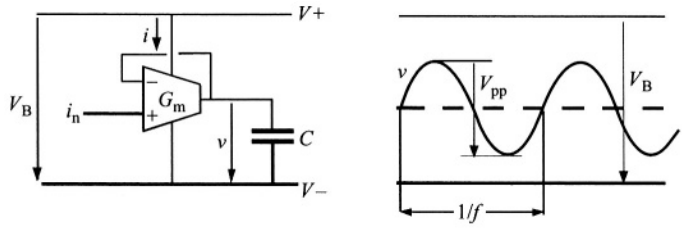


Figure 10.1. Single-pole low-pass filter.

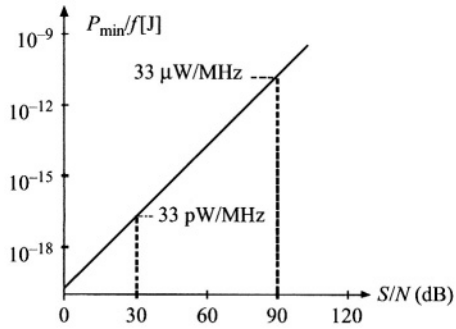


Figure 10.2. Limit of trade-off for power P, frequency f and signal-to-noise S/N.

Combining (10.2) and (10.4) yields:

$$P = 8\frac{V_B}{V_{pp}}kT \cdot f \cdot S/N \tag{10.5}$$

which shows that the peak-to-peak value of the signal should be increased to its maximum possible value V_B to reach the absolute minimum power:

$$P_{min} = 8kT \cdot f \cdot S/N \tag{10.6}$$

This minimum is proportional to the operating frequency f, which is the bandwidth Δf effectively used by this low-pass filter. Thus, the assessement of the value of K for circuit operated in class B must be done at the high-frequency end of the bandwidth, that is, $f = \Delta f$ in a low-pass filter. In class A circuits, power is independent of the signal frequency. The result of equation (10.6) corresponds to $K = K_{min} = 8$ in equation (10.1). It is the absolute minimum possible for any analog circuit, since band-limiting cannot be carried out in a more efficient manner. This minimum was first reported in [2] and later addressed by various authors [3–5]. It is represented in Figure 10.2.

As a result of this linear relation, increasing the requirement on S/N by 10 dB results in a ten-fold increase of minimum necessary power consumption. It is worth to point out that such a "steep" relation does not exist for digitally implemented filters. Indeed, the quantization noise is reduced exponentially by increasing the number of bits N_b, whereas power consumption only increases as a limited power function of N_b. The increase of P with S/N is therefore logarithmic instead of linear [2,4]. However, digital processing must usually be associated with analog-to-digital (A/D) and digital-to-analog (D/A) converters, which themselves require at least the minimum power above.

10.2.2. Filters

It is reasonable to assume that increasing the number M of poles of a filter increases the minimum necessary power. A pessimistic evaluation would assume that the minimum power is required for each pole, while the noise created at each pole is added. P_{min} would thus increase with M^2. But the noise created by the section implementing a pole may be filtered out by a subsequent section, and some signal energy might be transferred from section to section. A particular problem arises with the realization of a high-Q pair of poles when no physical inductor is available [6,7]. The required resonator must be implemented by emulating the inductor by a capacitor combined with a gyrator. The gyrator itself must be implemented by two transconductance amplifiers, as illustrated in Figure 10.3(a). The resulting expressions for inductance L, resonant angular frequency ω_0 and quality factor Q are:

$$L = C/G_m^2 \quad \omega_0 = G_m/C \quad Q = G_m R \tag{10.7}$$

The output noise current i_n of each transconductance amplifier can be characterized by its spectral density (10.3) where practical values of γ are usually significantly larger than 1.

The circuit can then be reduced to the equivalent circuit of Figure 10.3(b), where the combined noise current density S_{Ni} including the thermal noise of

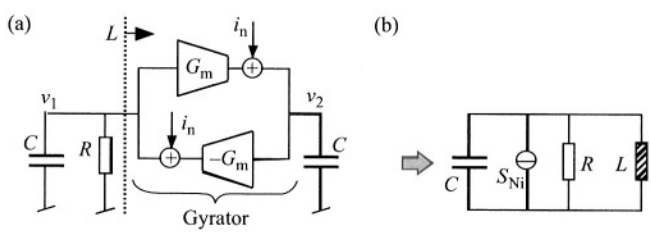


Figure 10.3. Active resonator.

resistor R is:

$$S_{Ni} = \frac{4kT}{R} + 4\gamma kTG_m\left[1 + \left(\frac{G_m}{\omega C}\right)^2\right] \cong \frac{4kT}{R}(1 + 2\gamma Q) \quad \text{for } \omega \cong \omega_0 \tag{10.8}$$

This noise density is $(1 + 2\gamma Q)$ times that of the resistance R, which would be the only source of noise in a passive resonator, for which the total noise voltage square is known to be kT/C [8]. The signal-to-noise ratio of this active resonator is thus,

$$S/N = \frac{V_{pp}^2/8}{(1 + 2\gamma Q)kT/C} \tag{10.9}$$

where V_{pp} is the peak-to-peak value of voltages v_1 and v_2 across the two capacitors (these values are equal at $\omega = \omega_0$). Assuming again 100% current-efficient amplifiers, the power used by each of them is given by (10.2). Hence, neglecting the power needed to drive R (since the corresponding current is Q times smaller than that for either of the two capacitors), we have:

$$\begin{aligned} P &\geq 16(1 + 2\gamma Q)kT \cdot f_0 \cdot S/N \\ &\cong 32\gamma Q \cdot kT \cdot f_0 \cdot S/N \quad \text{for } Q \gg 1 \end{aligned} \tag{10.10}$$

In comparison to (10.6), the factor 32 comes from the fact that we have two transconductors, with twice the power and two noise contributions, and the factor Q can be traced to effective noise amplification by this factor.

As for any active continuous-time filter, high-frequency capability can be traded for low power by reducing the value of transconductance G_m while keeping C constant to maintain S/N. In switched-capacitor implementations, it can be shown that the corresponding trade-off is obtained by changing the clock frequency. The value of transconductance must be sufficient to achieve adequate settling time, but has no effect on the total noise [9, p. 83]. For both kinds of implementations, high S/N can be traded for low power by decreasing the value of C, while decreasing that of G_m to keep the same frequency scale.

According to equation (10.10), the minimum power increases linearly with the value of Q. High-Q poles should thus be avoided in the implementation of low-power filters. If only one resonator is used to implement a narrow bandpass filter, then $\Delta f = f_0/Q$ and the minimum power necessary at resonance is given by:

$$P \geq 32\gamma Q^2 \cdot kT \cdot \Delta f \cdot S/N \quad \text{for } Q \gg 1 \tag{10.11}$$

corresponding to $K_{min} = 32\gamma Q^2$.

The situation is totally different if a physical inductor is available to implement the resonator. The noise spectral density S_{Ni} of Figure 10.3(b) can be

limited to that of the resistor, and the total noise is kT/C. Defining V as the RMS value of the sinusoidal voltage across the resonator then yields:

$$S/N = \frac{V^2}{kT/C} \quad \text{and} \quad P = \frac{V^2}{\eta R} = \frac{\omega_0 C V^2}{\eta Q} \tag{10.12}$$

where η is the power efficiency, which can reach a maximum value of $\pi/4$ in class B (η could approach 1 in class C, D or E, but the circuit is then no longer linear). Combining the two parts of (10.12) yields

$$P \geq \frac{8}{Q} kT \cdot f_0 \cdot S/N \tag{10.13}$$

The improvement proportional to $4Q^2$ compared with the active resonator is due to a $2Q$-time reduction of both noise and power for a given level of capacitor C. Introducing again $\Delta f = f_0/Q$, shows that

$$P \geq 8kT \cdot \Delta f \cdot S/N \tag{10.14}$$

corresponding to the lowest possible limit of $K_{\min} = 8$.

A case in-between the ones discussed above is that of an active LC resonator, in which an on-chip inductor is used, and active elements are used only to cancel the latter's losses. It can be shown that, in this case, the required power, compared to (10.10), is decreased by a factor proportional to Q_L^2, where Q_L is the quality factor of the lossy inductor [10].

For more general, high-order filters, lower bounds for P can also be derived; the reader is referred to [11–13].

10.2.3. Oscillators

Oscillators transform the DC power provided by a source into AC power at some fundamental frequency f_0 or period $T_0 = 1/f_0$. They must include some form of nonlinearity, in order to fix the amplitude of the signal produced. In harmonic oscillators, this nonlinearity is very weak or the amplitude stabilization mechanism involves a very long time constant, which produces an almost sinusoidal oscillatory signal. In the opposite case of relaxation oscillators, the nonlinear effects are very strong, and the harmonic content of the signal produced is high.

Figure 10.4 shows the principle of the most simple relaxation oscillator. A capacitor C is charged by a DC current I_0. When the voltage v across it reaches a threshold value V_0, it is discharged by a current $I \gg I_0$ produced by current-stable nonlinear circuit, NL, following the discharge cycle illustrated in Figure 10.4(b). The discharge current i is interrupted when v reaches zero, and a new oscillation cycle is initiated. In absence of any noise source, and assuming that

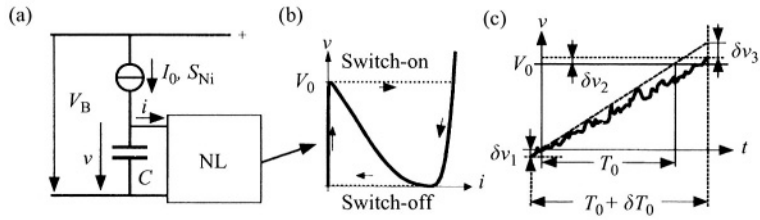


Figure 10.4. Most simple relaxation oscillator.

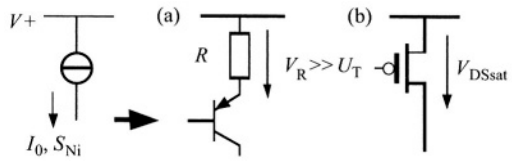


Figure 10.5. Implementation of current source I_0.

$i \ll I_0$ in the off state of NL and $i \gg I_0$ in the on state, the period of oscillation would be given by

$$T_0 = 1/f_0 = CV_0/I_0 \tag{10.15}$$

Capacitor C is always connected across the incremental resistance r of NL, so the minimum total noise voltage squared is always kT/C, but is distributed in a frequency range inversely proportional to r. Therefore, the switch-on and switch-off levels are affected by random errors δv_1 and δv_2 with mean square values given by:

$$\delta v_1^2 = \delta v_2^2 = kT/C \tag{10.16}$$

Furthermore, some noise current of spectral density S_{Ni} corrupts the current source I_0. This noise current is integrated in C during time T_0 together with I_0, resulting in a random departure δv_3 from the noiseless voltage ramp, given by [14]

$$\delta v_3^2 = \frac{T_0 S_{Ni}}{2C^2} \tag{10.17}$$

Some minimum voltage $V_B - V_0$ is needed across the sub-circuit producing current I_0, as illustrated by Figure 10.5.

The minimum possible value of S_{Ni}/I_0 is achieved by a bipolar transistor strongly degenerated by a resistor R, as shown in Figure 10.5(a). If the voltage V_R across R is much larger than the thermodynamic voltage $U_T = kT/q$, the

noise of the transistor can be neglected, and the minimum noise current spectral density is the thermal noise of resistor R, given by:

$$S_{Ni} = \frac{4kT}{R} = \frac{4kTI_0}{V_R} \tag{10.18}$$

Neglecting the minimum voltage across the transistor, the maximum value of V_R is $V_B - V_0$. Combining (10.15), (10.17) and (10.18) thus yields, in the best case:

$$\delta v_3^2 = \frac{2kT}{C} \frac{V_0}{(V_B - V_0)} \tag{10.19}$$

Since the period T_0 is proportional to the voltage swing V_0, their relative noise contents are equal, and the noise-to-signal ratio (variance of the relative period jitters) can be expressed as:

$$N/S = \frac{\delta T_0^2}{T_0^2} = \frac{\sum \delta v_i^2}{V_0^2} = \frac{kT}{CV_0^2}\left(2 + \frac{2V_0}{V_B - V_0}\right) \tag{10.20}$$

The power consumption can then be calculated by using successively equations (10.15) and (10.20):

$$P = I_0 V_B = f_0 C V_0 V_B = 2kT f_0 \cdot S/N \left(\frac{V_B/V_0}{1 - V_0/V_B}\right) \tag{10.21}$$

The power is increased if V_0/V_B is too small, reducing the voltage swing; it is also increased if V_0 approaches V_B, thereby reducing the voltage across the current source and thus increasing its noise content, according to (10.19). The optimum is reached for $V_0/V_B = 0.5$, resulting in the minimum possible power

$$P_{min} = 8kT f_0 \cdot S/N \tag{10.22}$$

which corresponds to the minimum value $K_{min} = 8$ if the frequency of oscillation f_0 is assimilated to the bandwidth. If a MOS transistor operated in saturation implements the current source, then the minimum noise current is the channel noise [9,15]

$$S_{Ni} = \frac{16kTI_0}{3V_{DSsat}} \tag{10.23}$$

where the saturation voltage V_{DSsat} must be smaller than $V_B - V_0$. By comparing with (10.18), noise and minimum power are increased by a factor 4/3, assuming $V_{DSsat} = V_R$.

Within the assumptions made, this minimum power is independent of the supply voltage. For a given frequency f_0, low power can be traded for high S/N (low jitter) by increasing I_0 and C.

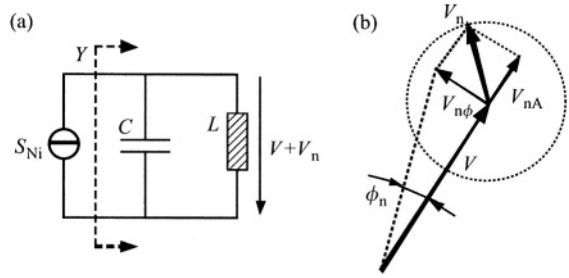


Figure 10.6. Noise calculation of harmonic oscillator.

Practical implementations of the nonlinear circuit NL usually result in some additional voltage loss and consume some bias current.

Harmonic oscillation is obtained by compensating the losses in a resonator. Thus, the active resonator of Figure 10.3 becomes a harmonic oscillator if $R = \infty$. According to equations (10.7) and (10.8), the minimum noise current spectral density around $f = f_0$ is then

$$S_{Ni} = 8\gamma kT\omega_0 C \tag{10.24}$$

and is loaded by the admittance Y of the equivalent LC circuit as shown in Figure 10.6(a).

Around the frequency of oscillation f_0, this admittance can be expressed as:

$$Y \cong 2j\omega_0 Cx$$

where

$$x = \frac{f - f_0}{f_0} \ll 1 \tag{10.25}$$

The spectral density of noise voltage V_N across the resonator is then given by [16]:

$$S_{Nv} = \frac{S_{Ni}}{|Y|^2} = \frac{2\gamma kT}{\omega_0 Cx^2} \tag{10.26}$$

As suggested by the phasor representation of Figure 10.6(b), this noise is added to the oscillation voltage of RMS value V with a random phase, so half of the noise power appears as amplitude V_{nA} and half as phase noise ϕ_n [16]. The phase noise spectral density is thus given by

$$S_{N\phi} = \frac{1}{2}\frac{S_{Nv}}{V^2} \quad \text{where} \quad V^2 = \frac{V_{pp}^2}{8} \tag{10.27}$$

For each of the transconductors driving the two capacitors in the active circuit, the minimum power consumption is given by (10.2); thus, combining (10.2), (10.26) and (10.27) results in

$$S_{N\phi} = \frac{8}{\pi}\frac{\gamma kT}{x^2 P}\frac{V_B}{V_{pp}} \geq \frac{8}{\pi}\frac{\gamma kT}{x^2 P} \tag{10.28}$$

For frequencies very close to the center frequency, nonlinear effects limit the noise spectral density, which therefore does not tend to infinity as suggested by this relation.

This minimum level of phase noise spectral density that can be achieved with power P is a very important limitation to low-power voltage-controlled oscillators used in the frequency synthesizers for RF applications [17]. Large signal swings are needed to minimize power according to (10.28), resulting in nonlinear effects and non-stationary noise sources. As a consequence, the phase noise may be increased beyond the limit expressed by (10.28) [18].

10.2.4. Voltage-to-Current and Current-to-Voltage Conversion

In analog circuits, signals are frequently converted from voltage to current and vice versa, in order to best exploit the respective features of theses two modes of representation. Such conversions are carried out by transconductors of transconductance G_m, as illustrated in Figure 10.7, where voltage V and current I are RMS values, whereas I_B is the average current delivered by DC voltage source V_B.

The signal power S and noise power N at the output of the transconductor are:

$$S = I^2 = (G_m V)^2$$

and

$$N = 4\gamma \cdot kT \cdot G_m \Delta f_N$$

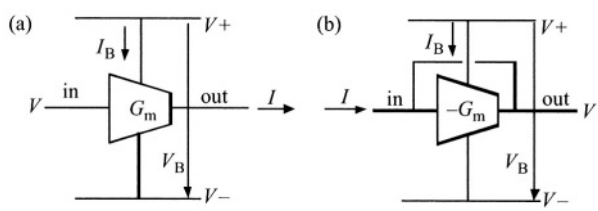


Figure 10.7. Transconductors for (a) V-to-I and (b) I-to-V conversion.

thus

$$S/N = \frac{G_m V^2}{4kT\gamma \Delta f_N} \tag{10.29}$$

where $\Delta f_N \geq \Delta f$ is the noise bandwidth; the power consumption is then:

$$P = V_B I_B \geq 4\gamma \frac{V_B I_B}{V^2 G_m} kT \cdot \Delta f \cdot S/N \tag{10.30}$$

The corresponding factor K is

$$K \geq 4\gamma \frac{V_B I_B}{V^2 G_m} \tag{10.31}$$

valid for both voltage-to-current conversion (Figure 10.7(a)) and current-to-voltage conversion (Figure 10.7(b)). Maximizing both V and G_m/I_B can minimize it. However, with the physical devices needed to implement the transconductor, increasing G_m/I_B reduces by the same factor the maximum value of V acceptable for a given distortion rate, thereby *increasing* the value of K. As a consequence, G_m/I_B should be maximized, and the most efficient known circuit implementation of a transconductor is the push–pull *of fully degenerated* complementary active devices represented in Figure 10.8 [19].

For this circuit, $I_B/G_m = V_R/2$ (which can be adjusted by means of the level shifters represented by circles) and $\gamma \cong 1$, thus

$$K \geq 2\frac{V_B V_R}{V^2} \tag{10.32}$$

Now $V_R \geq \sqrt{2} \cdot V$ to avoid cutting off the transistors. Furthermore, to avoid inverting the voltage across the transistors:

$$V_B \geq 2\sqrt{2} \cdot V + V_{SH} \tag{10.33}$$

where V_{SH} is the required DC shift between voltages v_n and v_p at the two emitters, as illustrated in the figure. If the output voltage v_O is maintained

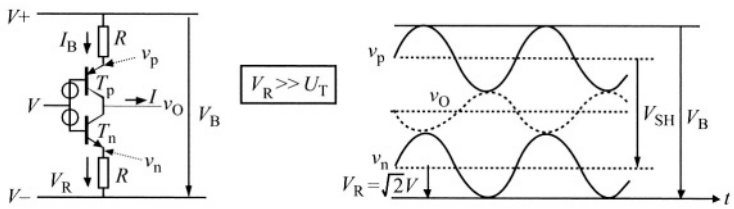


Figure 10.8. Most efficient transconductor circuit.

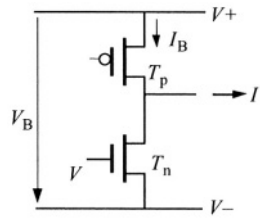


Figure 10.9. Simple MOS transconductor.

constant at $V_B/2$, then $V_{SH} = 2\sqrt{2} \cdot V$ and $K_{min} \geq 16$. If it is not constant, with a phase opposite to that of the input, then V_{SH} is increased, increasing the minimum. If the output follows the input, as in the current-to-voltage converter of Figure 10.7(b), then V_{SH} can be reduced to zero and $K_{min} \geq 8$; in this case, the transistors are not needed anymore.

Operating the circuit in class B ($V_R = 0$, each transistor blocked during half the period) would reduce K by a factor $\pi/2$. If it were not a push–pull, T_P being deactivated by connecting its base to a fixed potential, K for v_O constant would be increased by a factor 3, since I_B/G_m and γ would both be doubled, but V_{SH} would be reduced to $\sqrt{2} \cdot V$.

This circuit requires a large supply voltage V_B, not compatible with modern technologies, to keep a linear transconductance in spite of the nonlinear transfer characteristics of the active devices.

In a more realistic case, the active devices are not fully degenerated and the minimum power consumption depends on the acceptable level of distortion D, as in the elementary non-push–pull MOS transconductor illustrated in Figure 10.9.

The linearity of the transconductance can be improved at will by increasing the degree of inversion of the channel of transistor T_n, which also increases its saturation voltage V_{DSsatn}. Saturated transistor T_p delivers a constant current, the noise content of which can be adjusted by adjusting V_{DSsatp}.

The RMS input voltage V is assumed to be small enough to limit distortion. Therefore, the current through T_n remains equal to I_B. The transconductance and channel noise current spectral density of transistors in strong inversion are [9,20]:

$$g_m = \frac{2I_B}{nV_{DSsat}} \quad \text{and} \quad S_{Ni} = \frac{8n}{3}kT \cdot g_m \tag{10.34}$$

Thus, for the whole circuit, assuming the same value of n for the two transistors:

$$G_m = g_{mn} \quad \text{and} \quad \gamma = \frac{8nkT}{3}\frac{g_{mn} + g_{mp}}{4kT \cdot G_m} = \frac{2n}{3}\left(1 + \frac{V_{DSsatn}}{V_{DSsatp}}\right) \tag{10.35}$$

Now, to maintain both transistors saturated, assuming that the output voltage remains constant:

$$V_B > V_{DSsatn} + V_{DSsatp} \tag{10.36}$$

Introducing (10.34), (10.35) and (10.36) in (10.31) yields:

$$K > \frac{4n^2}{3}\left(1+\frac{V_{DSsatn}}{V_{DSsatp}}\right)\left(1+\frac{V_{DSsatp}}{V_{DSsatn}}\right)\left(\frac{V_{DSsatn}}{V}\right)^2 \tag{10.37}$$

which is minimum for $V_{DSsatn} = V_{DSsatp}$ giving

$$K > \frac{16n^2}{3}\left(\frac{V_{DSsatn}}{V}\right)^2 \tag{10.38}$$

Thus, K can be reduced by reducing $V_{DSsatn} = V_{DSsatp}$ and hence the supply voltage V_B. However, decreasing V_{DSsatn} increases the rate of distortion D due to the square-law characteristics, according to [21] (with model of [9,15])

$$D = \frac{\sqrt{2}V_i}{4nV_{DSsatn}} \tag{10.39}$$

The acceptable rate of distortion therefore participates in the trade-off, with

$$K > \frac{2}{3D^2} \tag{10.40}$$

For $D = 1\%$, $K > 6700$, which is considerably larger than the minimum $K_{min} = 16$!

High S/N can be traded for low power by decreasing the current I_B (increasing R in Figure 10.8, decreasing the width-to-length ratio of the transistors of Figure 10.9).

10.2.5. Current Amplifiers

Current amplifiers are built by combining current-to-voltage and voltage-to-current converters as shown in Figure 10.10.

The current gain A_i is given by:

$$A_i = \frac{I_o}{I_i} = \frac{I_o}{V}\frac{V}{I_i} = \frac{G_{m2}}{G_{m1}} \tag{10.41}$$

For noiseless input current, the total noise current at the output is

$$\begin{aligned} N &= 4kT\left(A_i^2\gamma_1 G_{m1} + \gamma_2 G_{m2}\right)\Delta f_N \\ &= 4kT G_{m2}\left(A_i\gamma_1 + \gamma_2\right)\Delta f_N \end{aligned} \tag{10.42}$$

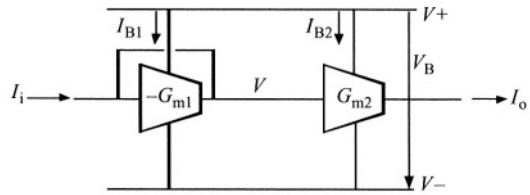


Figure 10.10. Current amplifier.

Now since the output signal power $S = I_o^2 = (G_{m2}V)^2$, the signal-to-noise ratio is

$$S/N = \frac{G_{m2}V^2}{4kT(A_i\gamma_1 + \gamma_2)\Delta f_N} \tag{10.43}$$

The total power consumption can be expressed as

$$P = V_B(I_{B1} + I_{B2}) = V_B\left(\frac{1}{A_i}\frac{I_{B1}}{G_{m1}} + \frac{I_{B2}}{G_{m2}}\right)G_{m2} \tag{10.44}$$

thus, by extracting G_{m2} from (10.43):

$$K \geq \frac{P}{kT \cdot \Delta f \cdot S/N} = 4(A_i\gamma_1 + \gamma_2)\left(\frac{1}{A_i}\frac{I_{B1}}{G_{m1}} + \frac{I_{B2}}{G_{m2}}\right)\frac{V_B}{V^2} \tag{10.45}$$

If the two transconductors have the same γ and same I_B/G_m, (10.45) becomes

$$K \geq 4\gamma\frac{(1 + A_i)^2}{A_i}\frac{V_B I_B}{V^2 G_m} \tag{10.46}$$

which is minimum for $A_i = 1$. Comparison of (10.46) with (10.31) shows that the power is $(1 + A_i)^2/A_i$ time larger than that of a single transconductor. With the most efficient known transconductor of Figure 10.8 and $A_i = 1$, (10.46) gives $K_{min} \geq 64$.

Linear current amplification is possible with nonlinear transconductors, like the one of Figure 10.9, provided they are identical with just a different current scale, as illustrated in Figure 10.11. It is a current mirror biased by current sources T_{p1} and T_{p2} to accommodate for AC currents I_i and I_o. To minimize power (see equation (10.32)), the modulation depth $m = \sqrt{2} \cdot I_i/I_{B1}$ of the drain current i_{D1} of T_{n1} should be large, resulting in a variable value of I_{B1}/G_{m1} if the transistor is operated in strong inversion.

If m remains sufficiently small (<0.5), the average value of i_{D1} stays approximately equal to I_{B1} and the variation of V_{DSsat} can be neglected in a first

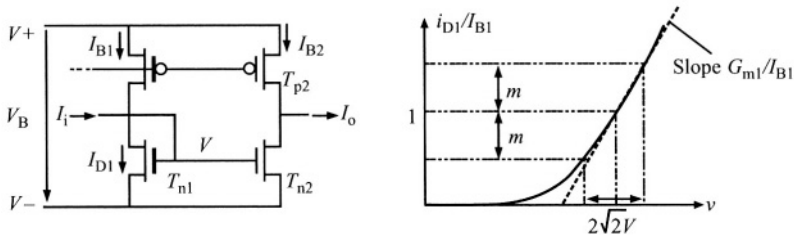


Figure 10.11. Current mirror.

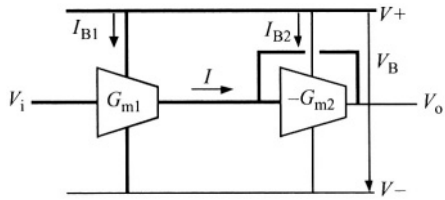


Figure 10.12. Voltage amplifier.

approximation; then equation (10.38) remains valid with, according to (10.34)

$$\frac{V_{DSsat1}}{V} \cong \frac{2I_{B1}}{nG_{m1}V} \cong \frac{2I_{B1}}{nI_i} \cong \frac{2\sqrt{2}}{n \cdot m} \tag{10.47}$$

The lower limit of K for the input transconductor alone can then be obtained by (10.38) and must be multiplied by $(1 + A_i)^2 / A_i$ to obtain its value for the whole mirror (see comment following (10.46)), which yields:

$$K > \frac{128\,(1 + A_i)^2}{3m^2 A_i} \quad \text{approximately valid for } m < 0.5 \tag{10.48}$$

If $A_i = 1$ and $m = 0.5$, then $K > 683$, which is much better than if the distortion of $V(I_1)$ would have been limited, but much larger than the value of 64 which is possible using the optimum transconductor of Figure 10.8.

10.2.6. Voltage Amplifiers

Voltage amplifiers may be built by combining voltage-to-current and current-to-voltage converters as shown in Figure 10.12.

The voltage gain A_v is given by:

$$A_v = \frac{V_o}{V_i} = \frac{I}{V_i}\frac{V_o}{I} = \frac{G_{m1}}{G_{m2}} \tag{10.49}$$

For noiseless input voltage, the total noise voltage at the output is

$$N = 4kT\left(\frac{\gamma_1 G_{m1}}{G_{m2}^2} + \frac{\gamma_2}{G_{m2}}\right)\Delta f_N = \frac{4kT}{G_{m2}}(A_v\gamma_1 + \gamma_2)\,\Delta f_N \qquad (10.50)$$

Now since the output signal power $S = V_o^2$, the signal-to-noise ratio is

$$S/N = \frac{G_{m2}V_o^2}{4kT(A_v\gamma_1 + \gamma_2)\Delta f_N} \qquad (10.51)$$

The total power consumption can be expressed as

$$P = V_B(I_{B1} + I_{B2}) = V_B\left(A_v\frac{I_{B1}}{G_{m1}} + \frac{I_{B2}}{G_{m2}}\right)G_{m2} \qquad (10.52)$$

thus, by extracting G_{m2} from (10.51):

$$K = \frac{P}{kT\cdot\Delta f\cdot S/N} \geq 4(A_v\gamma_1 + \gamma_2)\left(A_v\frac{I_{B1}}{G_{m1}} + \frac{I_{B2}}{G_{m2}}\right)\frac{V_B}{V_o^2} \qquad (10.53)$$

If the two transconductors have the same γ and same I_B/G_m, (10.53) becomes

$$K \geq 4\gamma\,(1 + A_v)^2\,\frac{V_B I_B}{V_o^2 G_m} \qquad (10.54)$$

The power required increases with $(1 + A_v)^2$ and the minimum value of I_B/G_m is limited by the nonlinear effects in G_{m2}.

For $A_v \gg 1$, the minimum power can be reduced if $I_{B1}/G_{m1} \ll I_{B2}/G_{m2}$, which is possible since $V_1 = V_2/A_v$. For example, if $I_{B2}/G_{m2} = A_v I_{B1}/G_{m1}$ and $I_{B1} = I_{B2}$, then (10.53) becomes:

$$K \geq 8A_v\gamma_1\frac{V_B}{V_o^2}\frac{I_{B2}}{G_{m2}} \qquad (10.55)$$

Using two optimum transconductors of Figure 10.8 as shown in Figure 10.13(a) (the transistors of the second transconductor are short-circuited and may thus be omitted), $I_{B2}/G_{m2} = V_B/4$ and $\gamma_1 = \gamma_2 = 1$. If $A_v = R_2/R_1 \gg 1$, then (10.55) results in $K > 16A_v$. The power only increases linearly with the voltage gain. A factor 2 can be gained if G_{m2} is implemented by means of a single grounded resistor of value $R_2/2 = A_v R_1/2$, which requires a double supply voltage $\pm V_B/2$.

This optimum circuit would require a very large supply voltage V_B, to fulfil the respective input and output conditions for linearity $V_R \gg U_T$ and $V_B/2 > A_v V_R$. Since $I_{B1} = I_{B2}$, a factor 2 can also be gained if the same current I_B

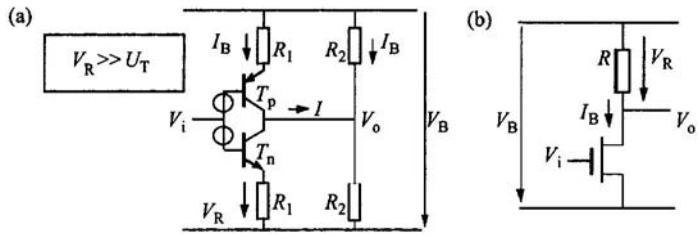


Figure 10.13. Voltage amplifiers: (a) most efficient, (b) simple stage.

flows through the two transconductors, as for the more realistic simple amplifier stage of Figure 10.13(b), where G_{m1} is the transconductance of the transistor and $G_{m2} = G_{m1}/A_v = 1/R$. If the transistor operates in strong inversion, then [9,20]:

$$\gamma_1 = \frac{2n}{3} \quad \frac{I_{B1}}{G_{m1}} = \frac{nV_{DSsat}}{2} \quad \frac{I_{B2}}{G_{m2}} = \frac{I_{B1}}{G_{m1}} A_v \tag{10.56}$$

and

$$V_B \geq V_{DSsat} + 2\sqrt{2} \cdot V_o \tag{10.57}$$

Thus, with equation (10.39) for the distortion D, the expression (10.55) of K reduced by the factor of 2 (due to the fact that only one bias current flows) results in:

$$K \geq \frac{1}{6D}\left[\frac{1}{D} + 8nA_v\right] \tag{10.58}$$

High voltage gain and low distortion compound their effects to increase the power. For example, for $D = 1\%$, $A_v = 10$ and $n = 1.5$, then $K > 3700$. High voltage gain cannot be obtained if V_B is limited to a few volts, since V_{DSsat} cannot be reduced below a few hundred millivolts. The maximum value of A_v is limited to $V_B/(2nU_T)$, when I_{B1}/G_{m1} reaches its minimum possible value nU_T in weak inversion [9,15]. To obtain more gain, a current source must be provided in parallel with R, which further increases the value of K.

10.3. Process-Dependent Limitations

10.3.1. Parasitic Capacitors

As seen in Section 10.2, capacitors are needed to limit the noise by limiting the bandwidth. Indeed, several of them are usually needed in filters, in order to shape their transfer function by means of several poles. Parasitic capacitors are capacitors that are imposed by the technology, but which play no intentional role in limiting the noise or shaping the transfer function. However, their very presence may result in an increase of power consumption through

various possible mechanisms. The most obvious example is the limitation to the maximum achievable speed, which may require an increase of current to increase the transconductance g_m of active devices. This problem is especially severe with MOS transistors for which, at a given size (and thus given parasitic drain capacitor), $I \sim g_m^2$ and $V_{DSsat} \sim g_m$, resulting in $P \sim f^3$. Another well-known example is found in operational amplifiers: because of the phase shift produced by parasitic capacitors, a compensation capacitor is needed to reach the necessary phase margin, and thus more current is necessary to reach the gain–bandwidth product.

These effects are independent of the required signal-to-noise ratio. Hence, parasitic capacitors only play an *indirect* role in the trade-off discussed in this chapter, as will be shown below.

10.3.2. Additional Sources of Noise

The only noise sources considered in Section 10.2 are the thermal noise of resistors and the thermal or shot noise of transistor channels. Those are fundamental sources of noise, which do not depend on the process. If other sources of noise are present, the signal power S has to be increased to maintain the signal-to-noise ratio, with the result of an increased power consumption P.

Flicker noise is a process-dependent additional source of noise, which is especially important for MOS transistors. It shows a spectral density approximately proportional to $1/f$, and corresponds, therefore, to an increase of the γ factor of a transistor by

$$\Delta\gamma \approx \frac{1}{\Delta f}\int_{f_{min}}^{f_{min}+\Delta f}\frac{df}{f} = \frac{1}{\Delta f}\ln\left(1+\frac{\Delta f}{f_{min}}\right) \tag{10.59}$$

It may thus drastically increase the value of K if the lower end frequency f_{min} of the bandwidth is small. Since flicker noise tends to be inversely proportional to the gate area, $\Delta\gamma$ can be reduced by increasing this area. Parasitic capacitors will then be increased, possibly requiring more power to maintain the speed. A more efficient manner of combating $1/f$ noise is to resort to auto-zeroing (or double correlated sampling) techniques. The price to pay is also some increase of power, due to clocking.

Any unwanted signal falling inside the circuit bandwidth can be assimilated to a noise. A particularly severe case is that of intermodulation [17,21]. It occurs when two strong signals of frequencies f_1 and f_2 lying outside the output bandwidth of the system are superimposed and distorted by a third-order nonlinearity, creating components of frequency $2f_1 - f_2$ or $2f_2 - f_1$ that fall inside the bandwidth. As explained in Section 10.2, extending the linear range of a transconductor implies a reduction of G_m/I_B and an increase of supply voltage. Thus, at high frequencies, more power is needed to drive the

parasitic capacitors. Log domain filters may offer a very attractive alternative, since they implement linear filtering *without* linearizing the transconductors [22–25].

Important contributions to additional noise may come from the power supply, or from other blocks on the chip by substrate coupling. High values of power supply rejection ratio (PSRR) and common-mode rejection ratio (CMRR) drastically help to reduce these sources of noise, but require more complex circuits with higher values of K.

10.3.3. Mismatch of Components

The close similarity of the electrical characteristics of several identical components fabricated on the same chip is most important for analog circuits. Such matching properties of devices are exploited to implement process-independent transfer functions, and to compensate for parasitic effects. The residual mismatch is, therefore, very often an important limitation to the performance of analog circuits in general, and to their dynamic range in particular. For example, it limits the linearity of A/D and D/A converters. It limits the CMRR of differential circuits, thereby limiting their insensitivity to power supply and substrate noise. In RF front ends, it limits the rejection of image frequencies when it is based on matched channels.

For all kinds of components, the random mismatch of their parameters tends to have a variance inversely proportional to their area. Mismatch is thus reduced by using larger devices, with the result of increased parasitic capacitors. More power is then necessary to reach the required speed, as discussed in Section 10.3.1. The additional power due to mismatch is strongly dependent on the function and on the circuit by which it is implemented [26,27]. It may exceed by a large margin the minimum due to noise.

10.3.4. Charge Injection

Elementary sample-and-hold circuits combining a sampling transistor and a storage capacitor C are found in all switched-capacitor circuits. The charge released into C when the transistor is switched-off causes an error voltage ΔV [28]. Compensation of this charge by means of appropriate techniques is limited by mismatch. It can be shown that increasing the clock frequency increases ΔV [29], which may reach tens of millivolts. This systematic error voltage is equivalent to a DC offset and may, therefore, be the main limitation to the dynamic range of circuits including DC in their passband.

By assimilating ΔV to a noise and using equation (10.2), the minimum power consumption associated with this circuit can be expressed as

$$P = fCV_{pp}V_B \geq fC\left(\frac{V_{pp}}{\Delta V}\right)^2 (\Delta V)^2 = 8fC\frac{S}{N}(\Delta V)^2 \qquad (10.60)$$

Thus, at the high-frequency edge of the passband where $f = \Delta f$:

$$K = \frac{P}{kT \cdot \Delta f \cdot S/N} \geq 8\frac{(\Delta V)^2}{kT/C} \tag{10.61}$$

For example, if $C = 1\,\text{pF}$, then switching noise $kT/C = (64\,\mu\text{V})^2$. If the error due to charge injection $\Delta V = 6.4\,\text{mV}$, then K is 10^4 larger than its minimum possible value $K_{\min} = 8$.

10.3.5. Non-Optimum Supply Voltage

The supply voltage V_B does not appear explicitly in the expressions for the minimum power derived in Section 10.2. This is because it has been assumed that the relative voltage swing V_{pp}/V_B can be close to unity. In real circuits as those discussed in Subsections 10.2.4–10.2.6, the voltage swing is limited by the nonlinear transfer characteristics of active devices. Minimum power is achieved by fully degenerating the active devices, as in circuits of Figures 10.8 and 10.13(a), but this requires a value of V_B several orders of magnitude larger than the thermodynamic voltage U_T (26 mV at ambient temperature).

For realistic values of V_B lower than 3 V, the voltage swing must be limited to a small fraction of V_B in order to maintain linearity, with the result of an increased power (see equation (10.40) for Figure 10.9 and equation (10.58) for Figure 10.13(b) [30]). Any additional reduction of possible voltage swing, for example, by a cascode transistor or by the tail current source of a differential pair, has an increasing relative importance with decreasing V_B. Thus in general, and contrary to digital circuits, analog circuits require more power when the supply voltage is reduced.

There are, however, some particular cases where reducing V_B may reduce the power. One example is that of very small-signal low-frequency voltage amplifiers. For the circuit of Figure 10.13(b) and an input signal $V_i \ll 1\,\text{mV}$, I_{B1}/G_{m1} can be reduced to its minimum possible value nU_T (transistor operated in weak inversion for which $\gamma = n/2$ [9]) without creating any relevant nonlinearity. Since $I_{B2} = I_{B1} = I_B$ and $G_{m2}/G_{m1} = V_i/V_o$, the expression (10.55) of K (reduced again by a factor of 2, due to the presence of only one bias current) then becomes

$$K \geq 2n^2 V_B U_T / V_i^2 \tag{10.62}$$

The required power is inversely proportional to V_i^2 and decreases linearly with V_B. Thus for this particular circuit, V_B could be reduced to the threshold voltage V_T of the transistor. If V_T is very low and the output voltage $V_o \ll U_T$, then V_B can be as low as the minimum value of $4U_T$ needed to ensure saturation in weak inversion, resulting in

$$K \geq 8\,(nU_T/V_i)^2 \tag{10.63}$$

Another example of circuits that may benefit from low supply voltage is that of log domain filters [22–24,31–34]. These circuits operate in a wide dynamic range with a voltage swing limited to a few hundred millivolts. To minimize power, the supply voltage V_B should thus ideally be reduced to the base–emitter voltage for bipolar transistors or to the threshold V_T for MOS transistors in weak inversion.

10.4. Companding and Dynamic Biasing

10.4.1. Syllabic Companding

As discussed earlier in this chapter, the use of certain circuits results in high noise, and thus limited dynamic range for a given, low power dissipation. In this section we show that the dynamic range of such circuits can be increased by using a process known as "companding". Filters will be used as examples to illustrate the concepts, since filters can be very noisy, especially if they employ high-Q poles (see Subsection 10.2.2). Below, all voltage and current quantities represented by capital V or I and lowercase subscripts denote RMS values.

Consider a filter with its stages biased at fixed bias points and operating in class A. For simplicity, the filter is assumed to have a passband gain equal to 1, and to be fed by an in-band input signal; see Figure 10.14(a). The output noise of this filter is constant; let V_n represent its RMS value. When the input is equal to the maximum value that can be handled, V_{max}, the output S/N is the maximum possible, $(S/N)_{max}$, as indicated in the same figure. At lower input signal levels V, S/N will be lower, as indicated in Figure 10.14(b). We note that the bias points within the filter have been set by considering the maximum possible signal level, and the resulting power dissipation is independent of the input signal.

Consider now the same filter between two blocks, with gains g and $1/g$, respectively, as shown in Figure 10.15 [35]. We neglect for now the noise of these blocks, and assume that, with the help of an envelope detector, g is made

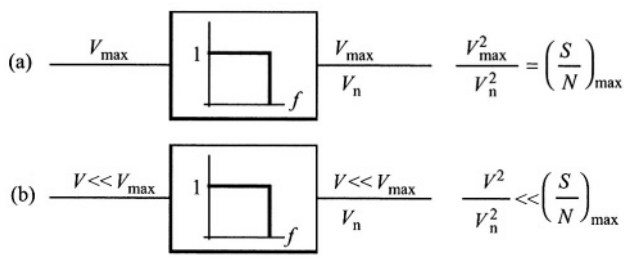


Figure 10.14. Conventional filter with (a) maximum signal, and (b) signal much smaller than that in (a).

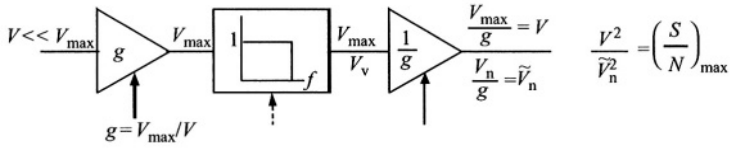


Figure 10.15. Companding filter.

proportional to the inverse of the envelope of the input signal (through feedback or feedforward, as in AGC systems). For simplicity, we assume for now that the input is a constant-amplitude sinusoid. Then g can be as indicated in the figure, where $V_{\max}$ is the maximum signal RMS value that can be handled by the filter. Then, independent of the input level, the filter is presented always with the maximum signal that it can handle, and S/N at its output is always $(S/N)_{\max}$. The last block in the figure divides the signal by g to restore its original input level; at the same time, it divides the noise by the same factor. Hence, the final S/N is always $(S/N)_{\max}$, independent of the value of V, as indicated in the figure.

In the above system, the input block compresses the dynamic range of the signal before it feeds the latter to the filter, so that the signal can remain well above the noise level; the output block expands the dynamic range to its original level. The combined effect of *compressing* and *expanding* is called *companding*. This technique has been used in communication channels for a very long time [36]. Its use in signal processing poses challenges [35], as will be explained below. The type of companding we have described so far, in which the compression and expansion are based on the envelope of the signal rather than its instantaneous value, is referred to as "syllabic companding".

If the input signal envelope is changing, the system in Figure 10.15 will distort, since the input and output gains are controlled simultaneously, not taking into account the envelope delay in the filter [35]. To eliminate this distortion, it is necessary to control the state variables of the filter [37]. For continuously varying g, it has been shown that this can be done by appropriately controlling some internal filter gain elements by using $\dot{g}/g$, where the dot indicates derivative with respect to time [38]. This control is indicated by the bottom broken arrow in Figure 10.15. Due to space limitations, we do not discuss this issue here; the reader is referred to [38]. The control can in principle be exact, but it is not trivial in practice. These considerations may not be necessary if the input envelope varies slowly. The quantity g can also be changed in discrete steps (e.g. multiplied by powers of 2) [37]. The design of the envelope detector can be done as for AGC systems.

Let us for simplicity assume that the minimum usable input signal is that for which the output S/N is 1. Then the systems of Figures 10.14 and 10.15

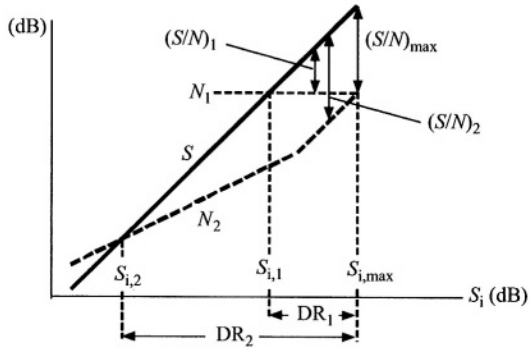


Figure 10.16. Output signal power (S), output noise power (N), signal-to-noise ratio (S/N) and dynamic range (DR), versus input signal power (S_i), for the conventional filter of Figure 10.14 (subscript 1) and the companding filter of Figure 10.15 (subscript 2).

behave as shown in Figure 10.16. S_i and S represent the input and output power, respectively. The subscript 1 represents quantities in Figure 10.14, and the subscript 2 represents the corresponding quantities in Figure 10.15. The upper part of the N_2 curve behaves as expected from the above discussion, for which it was assumed that the input and output blocks are noiseless. When the noise of these blocks is taken into account, the slope of the N_2 curve decreases for low-level signals, as shown in the figure. (The behavior shown in the figure assumes that these blocks are dynamically biased; see discussion below in reference to Figure 10.18.) In the upper part of the input range, $(S/N)_2 = (S/N)_{max} > (S/N)_1$, as expected from the above discussion. For low input levels, $(S/N)_2$ is smaller than the maximum possible, but is still much larger than $(S/N)_1$ at those levels. Thus, by using companding the input dynamic range is extended from DR_1 to DR_2, as shown in the figure, although both filters have the same $(S/N)_{max}$ (this must be interpreted carefully, see Subsection 10.4.3). Notice that, for the companding filter, the dynamic range can be much larger than $(S/N)_{max}$. The above discussion assumes that the overload levels of the filter and of the compressing and expanding blocks are the same.

If distortion is taken into account, the signal-to-noise plus distortion ratio, $S/(N + D)$ for a companding system is of the form shown in Figure 10.17. Assuming for simplicity that the spec is for a minimum acceptable value for this ratio denoted by $[S/(N + D)]_{acc}$, the resulting "usable dynamic range" is as indicated by DR in this figure.

If the input and output signals are currents, one can use a companding voltage-processing filter between an input block with transresistance $1/G_{mc}$ and an output block with transconductance G_{mc}, as shown in Figure 10.18 [39]. Thus G_{mc} cancels in the overall transfer function, which remains that of the center filter. The value of G_{mc} is made proportional to the envelope of the input

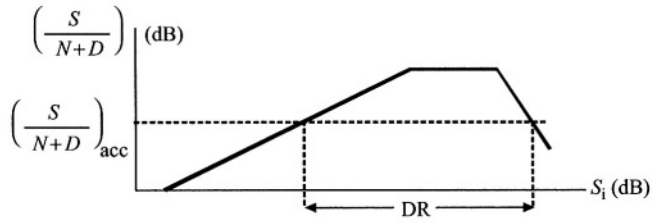


Figure 10.17. Signal-to-noise plus distortion ratio for the companding filter of Figure 10.15.

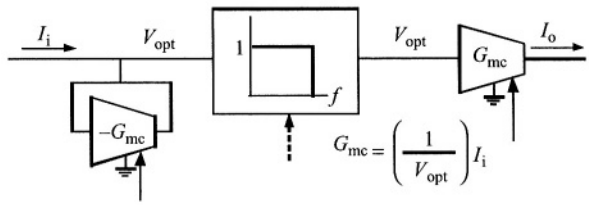


Figure 10.18. Companding filter with current input and output and a voltage-mode filter core [39].

current signal, so that, independent of the latter, the filter is always fed by an optimum voltage signal level V_{opt}, as large as possible above noise, but not as large as to cause unacceptable distortion. Thus, we have $G_{mc} = aI_i$, where the constant of proportionality a is chosen as $1/V_{opt}$:

$$G_{mc} = \frac{1}{V_{opt}} I_i \tag{10.64}$$

10.4.2. Dynamic Biasing

An obvious question is, of course, whether the dynamic range gained by using companding is worth the extra power dissipation required for the input and output blocks (as well as for the circuit required to control these blocks based on the amplitude of the input signal) in the above systems. To answer this question, we will use the system of Figure 10.18 as an example. The input block has been discussed in Subsection 10.2.4, and its S/N is given by (10.29). Using $V = V_{opt}$ and $G_{mc} = (1/V_{opt})I_i$ in the latter, we have

$$(S/N)_{G_{mc}} = \frac{V_{opt} I_i}{4kT\gamma \Delta f_N} \tag{10.65}$$

If dynamic biasing is used, the supply current can be made proportional to the signal current that can be handled; the same would apply if class B

operation were employed. The power dissipation of the input block can thus be assumed to be proportional to I_i (this, for example, would be the case with a BJT transconductor whose transconductance is controlled by its tail current).

Assume as an example that the filter is a G_m-C biquad based on the resonator discussed in Subsection 10.2.2, and that its noise and power dissipation are dominated by those of the latter (corresponding to the upper part of the N_2 curve in Figure 10.16). For a given S/N, then, the power dissipation of the filter will be bounded by (10.11). For each of the input and output blocks we assume a power dissipation as given by (10.1), with $K = 16$ (see the discussion in Subsection 10.2.4). We thus see that the power dissipation in the filter is Q^2 times larger than that needed for the input and output blocks, assuming the same S/N. Based on the above results, we obtain the behavior shown in Figure 10.19.

As seen, for input signals in a range of the order of Q^2, the power dissipation needed for the two transconductors is lower than that of the filter. Thus, for a minimum acceptable signal-to-noise ratio $(S/N)_{acc}$ shown in the figure, the filter need only be designed with a S/N slightly above this value, and the specifications will be met over an input range of about Q^2 with no more than doubling the power dissipation (and using some extra dissipation for the rest of the control circuits, such as the envelope detector). In contrast to this, to achieve such a dynamic range with a conventional filter, one would need to increase its peak S/N by Q^2, which would require a proportionate increase in power dissipation.

As seen above, the power dissipation will double when the input signal is increased over a ratio of the order of Q^2. In fact, one may be able to even process signals over an even larger range (I_{min} to I_{max} in Figure 10.19, where I_{max} is the level at which the transconductor distortion becomes unacceptable),

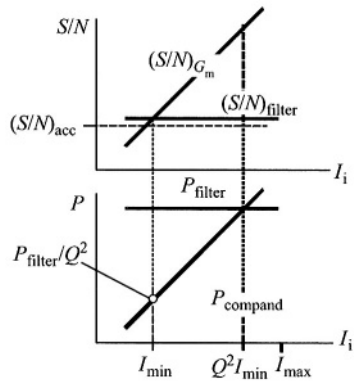


Figure 10.19. Signal-to-noise ratio and power dissipation for the blocks of the companding filter in Figure 10.18.

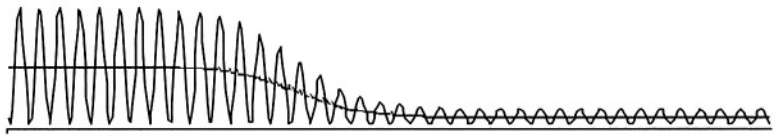


Figure 10.20. Typical bias plus signal waveform for a dynamically biased device.

with large power being consumed only when it is needed, that is, for large signals. This type of dynamic, or adaptive, biasing can mean large battery energy savings for some applications. A typical bias plus signal waveform for such systems [39] is shown in Figure 10.20.

Even when the power needed for the auxiliary circuitry including the envelope detector is included, the savings can still be significant for high-Q filters and other noisy circuits. Quantitative simulation results for a specific filter design can be found in [39]. Of course, for the above technique to be viable, the transconductor design must be able to provide low distortion over the entire usable input range.

A calculation of the total output current noise power spectral density in Figure 10.18 gives

$$\left(1 + |H(\mathrm{j}\omega)|^2\right) \cdot 4kT\gamma G_{\mathrm{mc}} S_{\mathrm{v}} + G_{\mathrm{mc}}^2 S_{\mathrm{v}}$$

where S_{v} is the PSD of the equivalent output noise voltage of the filter by itself. Thus, the noise contributed by the adaptively biased transconductors varies in the right direction: it increases or decreases, depending on whether the signal (and thus the value of G_{mc}) is large or small.

In conclusion, systems like the one in Figure 10.18, employing both companding and dynamic biasing, can provide two types of benefits when the signal envelope becomes small: (a) the power dissipation decreases, and (b) the noise decreases.

10.4.3. Performance in the Presence of blockers

The advantages of companding discussed above may be impossible to obtain if a desired signal to be processed coexists at the input with a much larger one; the latter signal is referred to as "blocker". We now discuss this issue.

Consider again a companding filter as in Figure 10.15 or 10.18, and assume first that only a single signal with power S_{i} is present at the input. Then the noise varies with S_{i} as shown by the curve marked "N_2" in Figure 10.16, in agreement with what has already been discussed. Assume, now, that a blocker is *also* present at the input, with power $S_{\mathrm{i,max}}$ (worst-case situation), indicated along

the horizontal axis in the figure. If $S_{i,max}$ is much larger than the desired signal, then for common signal waveforms the envelope of the input will practically correspond to that of the blocker. Since, in the companding filter, the input and output blocks are controlled by the envelope of the total input, it is now $S_{i,max}$ that will determine the level of *N, S / N* and *P*. In particular, it will cause a corresponding noise of value N_1 (see Figure 10.16). Now reducing the power of the desired signal will not change *N* and *P,* since it does not affect the envelope, which has been set by the blocker. In the presence of the fixed blocker, then, the system behaves as a conventional filter, with constant noise and power dissipation, and its *S / N* deteriorates linearly as the power corresponding to the desired signal is reduced. If the blocker power is smaller than $S_{i,max}$, the problem will be less serious, but still the benefits of companding will be compromised.

The above effect can be from very serious to unimportant, depending on the application. If the blocker is out-of-band, one faces the worst possible situation, since a signal that is to be rejected by the filter raises the noise of the filter even in-band, and corrupts the smaller in-band signals. In such cases, and especially if the expected out-of-band blockers can be large, companding and dynamic biasing may not be worth pursuing, unless the blocker is at frequencies far away from the passband, and can be adequately reduced by simple pre-filtering. If the blocker is in-band, then although it increases the noise level, the latter may be masked by the blocker power itself, and its effect on the smaller input signal may not be felt. This may be the case, for example, in a hearing aid; whether the sound corresponding to S_i is discernible or not will depend on the ratio $S_i/S_{blocker}$, which is much smaller than S_i/N despite the fact that *N* has been raised by the blocker. In high-quality audio, the effect of the noise level dependence on the input envelope may be audible if the noise is large, resulting in the so-called "breathing effect". Note, however, that this effect is also present in well-known noise reduction systems used in audio recording and reproduction (which also use companding), and it is not a problem as long as the noise level is kept sufficiently low. In general, companding and dynamic biasing are best suited to spectral shaping applications, rather than applications such as channel selection.

10.4.4. Instantaneous Companding

Rather than companding based on the envelope of a signal, one can compand based on the signal's instantaneous value. This is referred to as "instantaneous companding". Log domain filters [23,24] fall in this category, especially those in which positive and negative signal values are treated symmetrically [23,31]. In such circuits, advantage is taken of the exponential *i–v* characteristic of the bipolar transistor (or of the MOS transistor in weak inversion [33,34]). In these,

an input compressor produces a voltage with instantaneous value proportional to the logarithm of the instantaneous value of the input current. At the output, an exponential converter produces an output current with an expanded range of instantaneous values. While input and output current instantaneous values can vary over orders of magnitude, the internal filter voltages are logarithmically depended on the currents, and the range of their instantaneous values is thus compressed. All this can be accomplished, in principle, without distortion, even for large signals. This can be done for types of nonlinearities other than log, too. There are many other theoretical possibilities for such "Externally Linear" (ELIN) circuits [38]. So far, only log domain has received considerable attention.

True instantaneous companding in log domain circuits requires operation in class B or AB [23,31,34]. In class B circuits, the instantaneous current does not contain a bias component and can thus vary over a very large range. The resulting noise is then nonstationary. Under certain conditions, this results in constant signal-to-noise ratio [40]. In fact, the S/N and P curves for such circuits turn out to be similar to those for syllabic companding, discussed above.

Another possibility is the use of class A log domain circuits with dynamic biasing [41,42], such that the power dissipation and noise decrease when the signal is small, again as in the case of syllabic companding. Since these circuits are class A, problems associated with crossover distortion do not occur.

10.5. Conclusion

In analog circuits, a fundamental trade-off exists between power consumption, signal-to-noise ratio and available bandwidth, as expressed by equation (10.1). The absolute minimum value[2] of factor K that quantifies this trade-off is 8. However, independently of any process limitation, this minimum may be larger, depending on the function that is considered and on the approach used for its implementation: signal swing smaller than the supply voltage, several poles and/or high-Q poles in active filters, current or voltage amplification. A severe increase of K may be caused by the need to achieve linearity in spite of the nonlinear transfer characteristics of active devices. In practice, K is further increased by process-dependent limitations including parasitic capacitors, additional noise sources with respect to fundamental thermal or shot noise, mismatch of components and charge injection by switches. Lowering the supply voltage below a few volts usually causes an increase of K, but it may help to reduce it in cases where the signal swing is limited.

The dynamic range of a circuit, which is often considered similar to the maximum value of its signal-to-noise ratio, can be extended much beyond it by resorting to companding techniques.

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[2] Or, at least, the smallest known value.

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Chapter 11

TRADE-OFFS IN SENSITIVITY, COMPONENT SPREAD AND COMPONENT TOLERANCE IN ACTIVE FILTER DESIGN

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11.1. Introduction

The concept of sensitivity in analog circuit design has taken on increasing importance with the inclusion of analog and mixed-mode (i.e. analog and digital) circuits on an integrated circuit (IC) chip. Spectacular as the continued trend towards complex "systems on a chip" may be, the achievable accuracy of analog component values remains poor, and is not likely to improve significantly in the near future. Although it is true that a certain amount of tuning and trimming is possible by switching critical resistor and/or capacitor arrays to "ball-park" values, the achievable accuracy of the component values remains quite limited. Whereas in discrete-component design it is "only" a question of cost whether 1% or even 0.1% components are used to achieve critical specifications, on-chip such accuracy is attainable only by laborious and cost-intensive (laser, sand-blasting, etching, etc.) operations. An alternative is to live with the high component tolerances and to try to find circuits that are as insensitive to component values as possible. In active-RC filter design, for example, insensitive circuits do exist, but often a satisfactory degree of tolerance insensitivity is paid for by an increase in component spread. An increase in component spread, however, generally increases component tolerance, which in turn decreases functional accuracy and performance, thus closing a typical vicious cycle so often encountered in analog circuit design. A trade-off is clearly in order, if not inevitable. It is this trade-off loop that is the subject of this chapter. Because sensitivity and noise are somehow, and somewhat elusively related, we shall, toward the end of the chapter, briefly include this additional very important facet of analog design in our discussion.

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11.2. Basics of Sensitivity Theory

The *relative sensitivity* of a function $F(x)$ to variations of a variable x is defined as

$$S_X^{F(x)} = \frac{\mathrm{d}F/F}{\mathrm{d}x/x} = \frac{\mathrm{d}F}{\mathrm{d}x} \cdot \frac{x}{F} = \frac{\mathrm{d}\ln[F(x)]}{\mathrm{d}\ln x} \tag{11.1}$$

This expression provides a value for the relative change of the function $F(x)$ to a relative change of a parameter x, on which $F(x)$ depends. Although the absolute sensitivity of $F(x)$ to x, that is,

$$F' = \frac{\mathrm{d}F}{\mathrm{d}x} \tag{11.2}$$

and the semi-relative sensitivity

$$S_x^F = \frac{\mathrm{d}F}{\mathrm{d}x/x} \tag{11.3}$$

may often be of more relevance to a practical problem, it is the ease of using the sensitivity expression given by (11.1), and the simplicity with which the other two, that is, (11.2) and (11.3), can be derived from it, that is responsible for the importance of the relative sensitivity. This ease of usage is manifest by the table of sensitivity relations shown in Table 11.1. Most expressions in deterministic filter-theory can be broken down into simple expressions, for which the relationships listed in Table 11.1 apply.

We now consider the voltage or current transfer function of an nth-order transfer function, $T(s)$:

$$T(s) = \frac{N(s)}{D(s)} = \frac{b_m s^m + b_{m-1}s^{m-1} + \cdots b_1 s + b_0}{a_n s^n + a_{n-1}s^{n-1} + \cdots a_1 s + a_0} \tag{11.4}$$

where $s = \sigma + \mathrm{j}\omega$ is the complex frequency and $N(s)$ and $D(s)$ are polynomials in s with real coefficients a_i and b_j. Expressing $N(s)$ and $D(s)$ in their factored form, we obtain the zeros z_i and poles p_j of the transfer function, that is,

$$T(s) = K\frac{\prod_{i=1}^{m}(s - z_i)}{\prod_{j=1}^{n}(s - p_j)} \tag{11.5}$$

To obtain the frequency response of the filter in the steady state, we assume a sinusoidal input signal by letting $s = \mathrm{j}\omega$ in (11.5) and obtain:

$$T(\mathrm{j}\omega) = K\frac{\prod_{i=1}^{m}(\mathrm{j}\omega - z_i)}{\prod_{j=1}^{n}(\mathrm{j}\omega - p_j)} = |T(\mathrm{j}\omega)| \cdot \mathrm{e}^{\mathrm{j}\varphi(\omega)} \tag{11.6}$$

Table 11.1. Sensitivity relationships.

$S_x^x = S_x^{cx} = S_{cx}^x = 1$	$S_x^{u+v+\cdots} = \frac{1}{u+v+\cdots}[u \cdot S_x^u + v \cdot S_x^v + \cdots]$
$S_x^{cy} = S_x^y$	$S_x^{e^y} = y \cdot S_x^y$
$S_x^y = \left(S_y^x\right)^{-1}$	$S_x^{\ln y} = \frac{1}{\ln y} \cdot S_x^y$
$S_x^{y^n} = n \cdot S_x^y$	$S_x^y = S_x^{\lvert y\rvert} + \mathrm{j}\varphi_y \cdot S_x^{\varphi_y}$
$S_{x^n}^y = \frac{1}{n} \cdot S_x^y$	where $y = \lvert y\rvert \cdot \mathrm{e}^{\mathrm{j}\varphi_y}$
$S_x^y = S_{u_1}^y \cdot S_x^{u_2} + S_{u_1}^y \cdot S_x^{u_2} + \cdots$	$S_x^{\lvert y\rvert} = \mathrm{Re}\{S_x^y\}$
where $y = y(u_1, u_2, \ldots, u_n)$	$S_x^{\varphi_y} = \frac{1}{\varphi_y}\mathrm{Im}\{S_x^y\}$
$S_x^y = S_{u_1}^y \cdot S_{u_2}^{u_1} \cdot \cdots \cdot S_x^{u_n}$	$S_x^{y^*} = \left(S_x^y\right)^*$
where $y = y\{u_1[u_2[\cdots u_n(x)]]\}$	where $y^* = \lvert y\rvert \cdot \mathrm{e}^{-\mathrm{j}\varphi_y}$
$S_x^{uv} = S_x^u + S_x^v$	$S_x^{\sin y} = y \cdot \mathrm{ctg}\, y \cdot S_x^y$
$S_x^{u/v} = S_x^u - S_x^v$	$S_x^{\cos y} = -y \cdot \tan y \cdot S_x^y$
$S_x^{1/y} = -S_x^y$	$S_x^{\sinh y} = y \cdot \mathrm{ctgh}\, y \cdot S_x^y$
$S_y^{1/x} = -S_x^y$	$S_x^{\cosh y} = y \cdot \tanh y \cdot S_x^y$
$S_x^{y+c} = \frac{y}{y+c} \cdot S_x^y$	

Taking the logarithm of $T(\mathrm{j}\omega)$, we obtain

$$\begin{aligned} \ln T(\mathrm{j}\omega) &= \ln |T(\mathrm{j}\omega)| + j \arg T(\mathrm{j}\omega) \\ &= \alpha(\omega) + \mathrm{j}\varphi(\omega) \end{aligned} \tag{11.7}$$

where $\alpha(\omega)$ and $\varphi(\omega)$ are the gain and phase response of the filter in nepers and degrees, respectively.

Using the sensitivity relations in Table 11.1, we can readily express the sensitivity of $T(s)$ with respect to some component x in terms of the poles and zeros, namely, with (11.1), (11.3) and (11.5)

$$S_x^{T(s)} = S_x^K - \sum_{i=1}^{m} \frac{S_x^{z_i}}{s - z_i} + \sum_{j=1}^{n} \frac{S_x^{p_j}}{s - p_j} \tag{11.8}$$

where the so-called root sensitivity of a root q_ν (where q_ν is a pole or zero) is given by the semi-relative sensitivity:

$$S_x^{q_\nu} = \frac{\mathrm{d}q_\nu}{\mathrm{d}x/x} \tag{11.9}$$

$S_x^{T(s)}$ is often referred to as the transfer sensitivity which, in the form (11.8), is a partial fraction expansion in terms of the roots of $T(s)$. As such, the root sensitivities in (11.8) are the residues of the transfer sensitivity, thus:

$$S_x^{q_\nu} = \mp \mathrm{Res}\left\{S_x^{T(s)}\right\}_{s=q_\nu} = \mp(s - q_\nu)\, S_x^{T(s)}\Big|_{s=q_\nu} \tag{11.10}$$

where the minus sign holds for a zero, the plus for a pole. Letting $s = j\omega$ to obtain the sensitivity of the frequency response, we obtain from (11.1), (11.3), (11.6) and (11.7)

$$S_x^{\alpha(\omega)} = \mathrm{Re}\left[S_x^{T(j\omega)}\right] = S_x^{|T(j\omega)|} \tag{11.11a}$$

and

$$S_x^{\varphi(\omega)} = \mathrm{Im}\left[S_x^{T(j\omega)}\right] = \varphi \cdot S_x^{\varphi(j\omega)} \tag{11.11b}$$

Thus, the amplitude and phase sensitivity function results directly from the real and imaginary part of the transfer sensitivity function $S_x^{T(s)}$, for $s = j\omega$.

Finally, for any pole $p = \sigma_p + j\tilde{\omega}_p$ we have, for the radial pole frequency ω_p, and the pole Q, q_p:

$$\omega_p = \sqrt{\sigma_p^2 + \tilde{\omega}_p^2} \tag{11.12a}$$

and

$$q_p = \frac{\omega_p}{2\sigma_p} \tag{11.12b}$$

Thus, with (11.9) and (11.10), it follows that

$$\frac{\Delta p}{p} = \mathrm{Re}\left[\frac{\Delta p}{p}\right] + j\,\mathrm{Im}\left[\frac{\Delta p}{p}\right] = \frac{1}{p}\left\{\mathrm{Res}\; S_x^{T(s)}\right\}_{s=p} \tag{11.13a}$$

and with the relations in Table 11.1, we obtain:

$$\mathrm{Re}\left[\frac{\Delta p}{p}\right] = \frac{\Delta\omega_p}{\omega_p} \tag{11.13b}$$

and

$$\mathrm{Im}\left[\frac{\Delta p}{p}\right] = \left.\frac{\Delta q_p/q_p}{\sqrt{4q_p^2 - 1}}\right|_{q_p \gg 1} \approx -\frac{1}{2q_p}\frac{\Delta q_p}{q_p} \tag{11.13c}$$

Thus, also the variation of a pole, which can be expressed by the variation ω_p and pole Q, q_p, can be directly obtained from the transfer sensitivity, namely by computing its residue for $s = p$. Conversely, the amplitude and phase sensitivity, and variations due to component tolerances, can be derived from the relative pole (and zero) variation $\Delta p/p$ (and $\Delta z/z$). In general, the pole variation plays a more important role than the zero variation because it is also responsible for the filter (or system) stability, and because the pole variations will effect the filter passband in contrast to the zero variations which effect primarily the filter stopband.

11.3. The Component Sensitivity of Active Filters

We can express the relative variation of the transfer function $T(s)$ of an active RC filter in terms of pole and zero variations with the help of equations (11.1), (11.3) and (11.8). Thus,

$$\frac{\Delta T(s)}{T(s)} = \frac{\Delta K}{K} - \sum_{i=1}^{m} \left(\frac{z_i}{s - z_i} \right) \frac{\Delta z_i}{z_i} + \sum_{j=1}^{n} \left(\frac{p_j}{s - p_j} \right) \frac{\Delta p_j}{p_j} \tag{11.14}$$

Note that the quantities in parentheses depend on the poles and zeros of the initial transfer function $T(s)$. In general, these are given by the filter specifications and cannot be changed. This leaves the quantities $\Delta z_i / z_i$ and $\Delta p_j / p_j$ to be minimized in order to minimize the variation $\Delta T(s)/T(s)$. This quantity, in turn, contains both the amplitude variation $\Delta\alpha(\omega)$ and $\Delta\varphi(\omega)$ when s is set equal to $\mathrm{j}\omega$. This can really be seen from (11.1), (11.3) and (11.7), if we consider the variation of $T(\mathrm{j}\omega)$ caused by the variation of a component x:

$$\begin{aligned} \frac{\Delta T(\omega)}{T(\omega)} &= \frac{\mathrm{d} \ln T(\omega)}{\mathrm{d} \ln x} \frac{\Delta x}{x} = \left[\frac{\mathrm{d} \ln |T(\omega)|}{\mathrm{d} \ln x} + \mathrm{j} \frac{\mathrm{d}\varphi(\omega)}{\mathrm{d} \ln x} \right] \frac{\Delta x}{x} \\ &= \left(\frac{\mathrm{d}\alpha(\omega)}{\mathrm{d} \ln x} + \mathrm{j} \frac{\mathrm{d}\varphi(\omega)}{\mathrm{d} \ln x} \right) \frac{\Delta x}{x} \\ &= \left(S_x^{\alpha(\omega)} + \mathrm{j} S_x^{\varphi(\omega)} \right) \frac{\Delta x}{x} \end{aligned} \tag{11.15}$$

It follows that the amplitude variation $\Delta\alpha(\omega)$ and the phase variation $\Delta\varphi(\omega)$ due to the variation of a component x is given by

$$\Delta\alpha(\omega) = S_x^{\alpha(\omega)} \frac{\Delta x}{x} = \mathrm{Re} \left\{ \frac{\Delta T(\omega)}{T(\omega)} \right\} = \frac{\Delta |T(\omega)|}{|T(\omega)|} \tag{11.16a}$$

and

$$\Delta\varphi(\omega) = S_x^{\varphi(\omega)} \frac{\Delta x}{x} = \mathrm{Im} \left\{ \frac{\Delta T(\omega)}{T(\omega)} \right\} \tag{11.16b}$$

Relating this result to the expression given by (11.14), and considering the variation only in the vicinity of a dominant pole p_{dom} (which is generally in the passband frequency range near the cut-off frequency) we obtain:

$$\frac{\Delta T(\omega)}{T(\omega)} = \alpha(\omega) + \mathrm{j}\varphi(\omega) \approx \left(\frac{p_{\mathrm{dom}}}{\mathrm{j}\omega - p_{\mathrm{dom}}} \right) \frac{\Delta p_{\mathrm{dom}}}{p_{\mathrm{dom}}} \tag{11.17}$$

As mentioned above, the quantity in parentheses is given by filter specifications, and the variation of the dominant pole is given by (12.13). It is this pole variation, and to a lesser degree that of the other non-dominant poles, that can

be minimized in order to minimize the effect on amplitude and phase caused by component variations. In what follows, we shall examine in somewhat more detail, how the pole variation (dominant or otherwise) is effected by component tolerances and variations. To do so, it follows from (12.13) that we must examine in more detail the variations $\Delta\omega_p/\omega_p$ and $\Delta q_p/q_p$ (the absolute value of ω_p and q_p being given by the filter specifications).

From (11.1), it follows that

$$\frac{\Delta\omega_p}{\omega_p} = \sum_{i=1}^{r} S_{R_i}^{\omega_p} \frac{\Delta R_i}{R_i} + \sum_{j=1}^{c} S_{C_j}^{\omega_p} \frac{\Delta C_j}{C_j} + \sum_{k=1}^{g} S_{\beta_k}^{\omega_p} \frac{\Delta\beta_k}{\beta_k} \tag{11.18}$$

where we assume r resistors, c capacitors, and g amplifiers with gain β_k ($k = 1, \ldots, g$) in the filter network. In general, there will be only one or two amplifiers generating a complex-conjugate pole pair. Furthermore, most well-tried circuits are characterized by the fact that the pole frequency can be made to be independent of gain, thereby eliminating the third summation in (11.18). The first two summations will depend on the technology used to fabricate the active RC filter. If a technology is used that permits close tracking, with temperature, say, of the resistors and capacitors, so that within close limits $\Delta R_i/R_i \equiv \Delta R/R$ and $\Delta C_j/C_j \equiv \Delta C/C$, then it can readily be shown that (11.18) simplifies to

$$\frac{\Delta\omega_p}{\omega_p} = -\left(\frac{\Delta R}{R} + \frac{\Delta C}{C}\right) \tag{11.19}$$

This quantity relies for its minimization on the compensation of temperature coefficients (TCR and TCC), aging characteristics and other effects influencing the resistor and capacitor values.

As in (11.18), the relative q_p variation is given by:

$$\frac{\Delta q_p}{q_p} = \sum_{i=1}^{r} S_{R_i}^{q_p} \frac{\Delta R_i}{R_i} + \sum_{j=1}^{c} S_{C_j}^{q_p} \frac{\Delta C_j}{C_j} + \sum_{k=1}^{g} S_{\beta_k}^{q_p} \frac{\Delta\beta_k}{\beta_k} \tag{11.20}$$

In contrast to the expression given by (11.18), in which the ω_p-sensitivity to gain (β_k) variations generally plays an insignificant role (if it plays a role at all), the situation is exactly reversed here. The variation of the resistors and capacitors will effect q_p very little, if at all – as in the case of tracking components. The sensitivity of q_p to gain, however, cannot possibly be eliminated because, as we shall see below, it is through the gain that the complex-conjugate poles, necessary for any kind of filter selectivity, are obtained. This can be illustrated by considering a second-order, single-amplifier active RC filter, often referred to as a single-amplifier biquad (SAB).

Consider, for example, the transfer function of a second-order bandpass filter:

$$T(s) = K\frac{\omega_p s}{s^2 + 2\sigma_p s + \omega_p^2} = K\frac{\omega_p s}{s^2 + (\omega_p/q_p)s + \omega_p^2} \tag{11.21}$$

Assume that the center frequency f_p is 500 Hz and the 3 dB bandwidth B is 50 Hz. It can then readily be shown that $\omega_p = 2\pi \cdot 500\,\text{rad/sec}$ and that $2\sigma_p = 2\pi \cdot B = 2\pi \cdot 50\,\text{rad/sec}$. Introducing the pole $Q, q_p = \omega_p/2\sigma_p = f_p/B$ we obtain $q_p = 10$. Consider now, the case that our bandpass filter is realized by a second-order passive RC network. It can be shown that in this case, a q_p equal to ten is impossible to achieve. In fact, the pole Q of any pole pair realized by a passive RC network is always less than 0.5. We indicate this by designating the pole Q of a pole pair realized by a passive RC network by $\hat{q}_p$. Thus, by definition

$$\hat{q}_p < 0.5 \tag{11.22}$$

It follows from the example above that with a passive RC second-order bandpass filter, the attainable 3 dB bandwidth will always be larger than 1000 Hz. Thus, the filter selectivity, which in the bandpass case is precisely the ratio of center frequency to 3 dB bandwidth, is so extraordinarily poor as to be essentially useless.

How then does an active RC biquad, say with one amplifier of gain β, achieve useful selectivity, that is, a pole Q, q_p which is larger than 0.5 (such as in our example, $q_p = 10$)? The answer is by inserting the passive RC network into a negative or positive-feedback loop, depending on whether the gain β is inverting or non-inverting. (Obviously the topology of the RC network must take the polarity of the amplifier into account.)

If we have *negative* feedback, the passive RC pole Q, $\hat{q}_p$ will be increased to the desired value q_p by an expression of the form:

$$q_p \approx \hat{q}_p \cdot \beta^i \tag{11.23}$$

where i is either 0.5 or unity, depending on the class of biquad used. In any case, the gain β required to obtain q_p is proportional to $q_p/\hat{q}_p$. For our example, for which $q_p = 10$, and a class of biquad for which $i = 1$, the minimum gain β required will be 10/0.5 = 20; depending on how small $\hat{q}_p$ is, the required gain β may also be much larger. Clearly, since amplifier gain cannot be made arbitrarily large, particularly if the pole frequency is increased and the dissipated power is to be limited and – typically, as small as possible – it is important to design the passive RC network such that $\hat{q}_p$ is as large as possible, that is, as close to 0.5 as possible.

If the gain of the active RC filter is obtained by a feedback amplifier, where β is the closed-loop gain and A the open-loop gain, it can readily be shown

that the relative variation of q_p to variations of gain will be:

$$\frac{\Delta q_p}{q_p} = i\frac{\Delta\beta}{\beta}$$

$$\approx i\frac{\beta}{1+\mathrm{LG}}\frac{\Delta A}{A} = i\frac{(q_p/\hat{q}_p)^{1/i}}{1+\mathrm{LG}}\frac{\Delta A}{A} \tag{11.24}$$

where LG is the loop gain of the feedback amplifier and i equals 0.5 or unity, depending on the biquad class used. Thus, also the variation of q_p caused by amplifier variations will be inversely proportional to $\hat{q}_p$, meaning that also with respect to the variations of gain (and, incidentally, of other components as well) $\hat{q}_p$ should be made as large as possible, that is, as close to 0.5 as the RC circuit, that is, the component spread, will permit. How this is achieved will be discussed in the next section. First, however, we shall examine the case for the RC network in a positive-feedback loop, that is, for β realized by a non-inverting amplifier.

For *positive* feedback, it can be shown that the relationship between the desired Q, q_p, and the necessary gain β to achieve it, is:

$$q_p = \frac{\kappa_1}{\kappa_2 - \beta\kappa_3} \tag{11.25}$$

where κ_1, κ_2 and κ_3 depend only on the passive RC network in the feedback loop. Note that the pole Q of the passive RC network is given by:

$$\hat{q}_p = q_p\,(\beta = 0) = \frac{\kappa_1}{\kappa_2} \tag{11.26}$$

Calculating the variation of q_p to variations of β, it follows from the sensitivity relations in Table 11.1 that:

$$\frac{\Delta q_p}{q_p} = \left(\frac{q_p}{\hat{q}_p} - 1\right)\frac{\Delta\beta}{\beta} \tag{11.27}$$

Thus, in the positive-feedback case also, it follows that in order to minimize variations of q_p due to variations of gain and other components, the pole Q of the passive RC network, $\hat{q}_p$, should be as close to 0.5 as possible.

At this point it is of interest to compare the sensitivity of positive and negative feedbacks based filters. From (11.22) and (11.25), it follows that

Negative feedback: $S_\beta^{q_p} = i \quad i = 0.5, 1$ (11.28a)

Positive feedback: $S_\beta^{q_p} = \frac{q_p}{\hat{q}_p} - 1$ (11.28b)

At first glace, it would seem that negative-feedback based circuits have a much smaller sensitivity to gain – and other component – variations than those based on positive feedback. This conclusion is misleading however, if the gain β is obtained as the closed-loop gain of a feedback-based amplifier. To see this we briefly examine the sensitivity of closed-loop gain β to open-loop gain A in a typical operational amplifier. Whether used in the inverting or non-inverting mode, this sensitivity is essentially given by

$$S_A^\beta \approx \frac{1}{1+\mathrm{LG}} \frac{\Delta A}{A}\bigg|_{\mathrm{LG}\gg 1} \approx \frac{1}{\mathrm{LG}} \frac{\Delta A}{A} \tag{11.29}$$

Furthermore, the loop gain LG is readily shown to be approximately

$$\mathrm{LG} \approx \frac{A}{\beta} \tag{11.30}$$

so that

$$\frac{\Delta q_\mathrm{p}}{q_\mathrm{p}} = S_\beta^{q_\mathrm{p}} \cdot S_A^\beta \frac{\Delta A}{A} \tag{11.31}$$

which with (11.29) and (11.30) becomes

$$\frac{\Delta q_\mathrm{p}}{q_\mathrm{p}} \approx \left[\beta \cdot S_\beta^{q_\mathrm{p}}\right] \frac{\Delta A}{A^2} = \Gamma_\beta^{q_\mathrm{p}} \cdot \frac{\Delta A}{A^2} \tag{11.32}$$

In other words, the variation of q_p depends on $\Gamma_\beta^{q_\mathrm{p}}$ which is the *gain–sensitivity product* (GSP) of q_p with respect to β. This changes the conclusion from above quite drastically. If we consider the GSP, which we must, rather than the sensitivity, then instead of (11.28), we now have:

$$\textit{Negativefeedback}: \quad \Gamma_\beta^{q_\mathrm{p}} = i\beta \approx iA \quad i = 0.5, 1 \tag{11.33a}$$

$$\textit{Positivefeedback}: \quad \Gamma_\beta^{q_\mathrm{p}} \approx \beta\left(\frac{q_\mathrm{p}}{\hat{q}_\mathrm{p}} - 1\right) \tag{11.33b}$$

The reason we let $\beta \approx A$ in (11.33a) is that negative-feedback circuits generally operate with the gain in, or close to, the open-loop mode. On the other hand, positive-feedback networks must restrict the closed-loop gain β to values close to unity, that is, from (11.25)

$$\beta < \frac{\kappa_2}{\kappa_3} \tag{11.34}$$

which is generally between unity and two. If we consider the open-loop gain of an op-amp to be in the order of 100 to 1000, it readily follows that the GSP for

positive feedback is certainly comparable to, if not considerably smaller than, that of negative feedback. This explains why the positive-feedback biquads are, in fact, more frequently used than their negative-feedback counterparts. (Incidentally, it should be pointed out already here, and will be discussed briefly in Section 11.7, that minimizing the GSP of an active RC biquad filter also reduces the output thermal noise.)

For higher order filters, it is often difficult to factor the polynomials $N(s)$ and $D(s)$ in equation (11.4) into complex-conjugate pairs, or, equivalently, into expressions involving the radian pole frequencies ω_{p_j} and pole Qs, q_{p_j}, where $j = 1, \ldots, n/2$. (This assumes that n is even. If it is not, then there is still an additional negative real term.) In this case, $T(s)$ is given in the form of (11.4) and its variation is expressed in terms of coefficient sensitivities thus:

$$\begin{aligned}\frac{\Delta T(s)}{T(s)} &= \sum_{i=0}^{m} S_{b_i}^{T(s)} \frac{\Delta b_i}{b_i} + \sum_{j=0}^{n} S_{a_j}^{T(s)} \frac{\Delta a_j}{a_j} \\ &= \sum_{i=0}^{m} S_{b_i}^{N(s)} \frac{\Delta b_i}{b_i} + \sum_{j=0}^{n} S_{a_j}^{D(s)} \frac{\Delta a_j}{a_j} \end{aligned} \tag{11.35}$$

The sensitivity terms in (11.35), which represent the sensitivity of the transfer function to coefficient variations, and are themselves frequency-dependent functions, are given by the filter specifications and the resulting transfer function. It is therefore the sensitivity of the coefficients to circuit components that can be minimized, that is,

$$\frac{\Delta b_i}{b_i} = \sum_{\mu=1}^{r} S_{R_\mu}^{b_i} \frac{\Delta R_\mu}{R_l} + \sum_{\nu=1}^{c} S_{C_\nu}^{b_i} \frac{\Delta C_\nu}{C_\nu} + \sum_{k=1}^{g} S_{\beta_k}^{b_i} \frac{\Delta \beta_k}{\beta_k} \tag{11.36a}$$

and

$$\frac{\Delta a_j}{a_j} = \sum_{\mu=1}^{r} S_{R_\mu}^{a_j} \frac{\Delta R_\mu}{R_\mu} + \sum_{\nu=1}^{c} S_{C_\nu}^{a_j} \frac{\Delta C_\nu}{C_\nu} + \sum_{k=1}^{g} S_{\beta_k}^{a_j} \frac{\Delta \beta_k}{\beta_k} \tag{11.36b}$$

It can be shown that the minimization of these quantities entails a procedure identical to that of maximizing the RC pole Qs, which we have designated by $\hat{q}_{\mathrm{p}}$. The problem is that for higher order filters, breaking the corresponding polynomials $N(s)$ and $D(s)$ into these roots and root pairs becomes quite intractable, so that the $\hat{q}_{\mathrm{p}}$ quantities cannot be analytically obtained. Nevertheless, the procedure for maximizing $\hat{q}_{\mathrm{p}}$ outlined in the next section is valid also for higher order networks, even if the individual $\hat{q}_{\mathrm{p}}$ values cannot be identified.

11.4. Filter Selectivity, Pole Q and Sensitivity

Consider the second-order passive RC bandpass filter shown in Figure 11.1. The transfer function is given by

$$\hat{T}(s) = K\frac{\omega_p s}{s^2 + (\omega_p/\hat{q}_p)s + \omega_p^2} \tag{11.37}$$

where

$$K = \sqrt{\frac{R_2C_2}{R_1C_1}} \tag{11.38a}$$

$$\omega_p = \frac{1}{\sqrt{R_1R_2C_1C_2}} \tag{11.38b}$$

$$\hat{q}_p = \frac{1}{x + 1/x + \varepsilon} \tag{11.38c}$$

$$x = \sqrt{\frac{R_1C_1}{R_2C_2}} \quad \varepsilon = \sqrt{\frac{R_1C_2}{R_2C_1}} \tag{11.38d}$$

To examine the bounds on $\hat{q}_p$, we consider its inverse

$$\frac{1}{\hat{q}_p} = x + \frac{1}{x} + \varepsilon \tag{11.39}$$

The well-known function $x + x^{-1}$ has a minimum of two for $x = 1$. Since (11.39) includes the term ε, this minimum can never be reached; its value will always be larger than two, or, conversely, the value of $\hat{q}_p$ will always be smaller than 0.5. Although this is a specific example, the result is representative for a basic theorem with regard to passive RC networks. This theorem states that *the poles of an RC network are restricted to being single and on the negative-real*

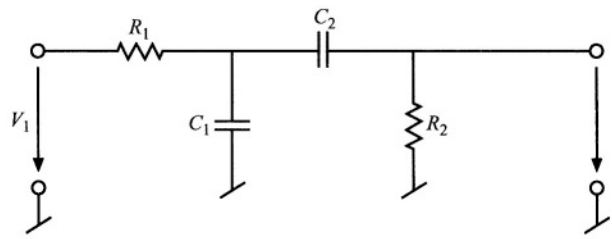


Figure 11.1. Second-order passive RC bandpass filter.

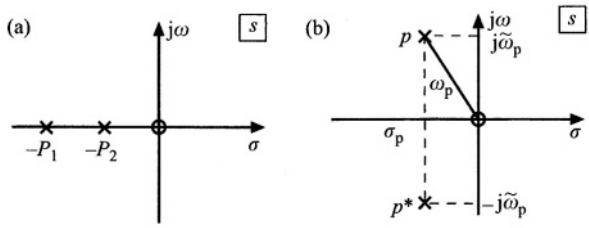


Figure 11.2. Pole–zero pattern of a second-order bandpass filter: (a) passive RC, (b) active RC (or LCR).

axis in the complex frequency plane. Thus, for the two negative real poles P_1 and P_2 in Figure 11.2(a), we obtain a polynomial

$$D(s) = (s + P_1)(s + P_2) = s^2 + (P_1 + P_2)s + P_1 P_2$$
$$= s^2 + \frac{\omega_p}{\hat{q}_p} s + \omega_p^2 \tag{11.40}$$

where

$$\omega_p^2 = P_1 P_2 \tag{11.41a}$$

and

$$\hat{q}_p = \frac{\sqrt{P_1 P_2}}{P_1 + P_2} \tag{11.41b}$$

so that

$$\frac{1}{\hat{q}_p} = \sqrt{\frac{P_1}{P_2}} + \sqrt{\frac{P_2}{P_1}} \tag{11.41c}$$

Thus, $\hat{q}_p$ would reach its unattainable maximum value of 0.5 only if it were possible to make $P_1 = P_2$ which, as we stated above, would mean that we have a double pole on the negative-real axis, and which, with a passive RC network, is not possible. A glance at our example above and of equations (11.38c and d) shows that such a double pole would occur when ε, that is, the ratio R_1/R_2 or C_2/C_1, approaches zero. This, of course, demands a non-realizable spread of the resistors and/or capacitors. How large a spread of these components is acceptable in order to minimize ε and to approach a double pole (or, in other words, to permit $\hat{q}_p$ to approach 0.5) is a question of the technology used. *It represents one of the fundamental trade-offs of low-sensitivity active RC filter – and oscillator – design.*

There is another way of illustrating the importance of trying to approach a double pole, (or the value of $\hat{q}_p = 0.5$) with the passive RC network in a SAB

with closed-loop gain β. Let us assume that the desired bandpass filter biquad, has the transfer function

$$T(s) = K\frac{\omega_p s}{s^2 + (\omega_p/q_p)s + \omega_p^2} \tag{11.42}$$

with the pole–zero pattern in the complex frequency, or s-plane, as shown in Figure 11.2(b). Note that the only difference in the transfer function of the passive RC bandpass filter $\hat{T}(s)$ (see equation (11.37)) and that of the desired active RC bandpass filter $T(s)$ in equation (11.42) is in the pole Q, namely $\hat{q}_p$ and q_p, respectively. By definition, $\hat{q}_p < 0.5$ and, for any useful application, we can assume that $q_p > \hat{q}_p$. This difference will be apparent in the shape of the amplitude response as shown in Figure 11.3. For the passive RC case, the 3 dB bandwidth $\hat{B}$ will be larger than $2f_p$, for the desired active RC filter the 3 dB bandwidth B will, typically be substantially smaller than f_p, thereby providing a filter selectivity that is correspondingly higher. To consider, now, how we obtain the complex-conjugate pole pair of Figure 11.2(b) from the combination of a passive RC network whose poles are as in Figure 11.2(a), combined with an amplifier with (inverting or non-inverting) gain β, we consider a typical root locus of the resulting feedback network with respect to β. This is shown in Figure 11.4. Note that the effect of the gain β is to create a pair of so-called closed-loop poles p, p^* from the open-loop poles P_1 and P_2. It does so by moving the closed-loop poles along the root locus, which will differ according to such factors as the sign of the feedback amplifier (positive or negative), and the type of passive RC network in the feedback path. However, the common feature for all the possible biquad root loci will be that with increasing gain β, the closed-loop poles will first be shifted towards each other on the negative-real frequency axis, away from the negative-real open-loop poles, and towards a coalescence point (point C in Figure 11.4). From there, with increasing gain β, a pair of complex-conjugate poles will be generated, with the required q_p necessary to satisfy the transfer function in equation (11.42). Clearly, the further apart the two open-loop poles P_1 and P_2 are on the negative-real axis in the s-plane, the more gain β is required to

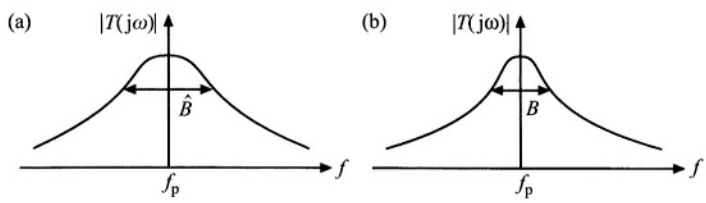


Figure 11.3. Amplitude response of second-order filter: (a) passive RC, (b) active RC (or LCR).

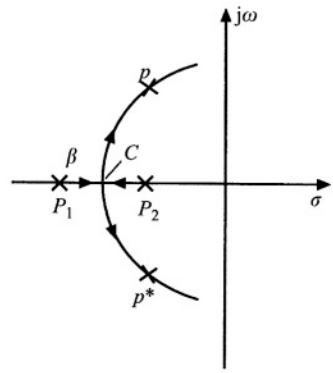


Figure 11.4. Root locus of active RC feedback-based filter with respect to gain β.

reach the final values, namely the closed-loop poles p and p^* on the root locus. Designing open-loop poles far apart is wasteful of gain, since (almost) up to the coalescence point, the passive RC open-loop poles can be obtained by a passive RC network, that is, without any gain at all. Open-loop poles that are far apart on the negative-real axis are also detrimental to the stability of the filter, since the higher the required closed-loop gain, the smaller the stabilizing loop gain (see equation (11.29)), that is, the higher the sensitivity of the closed-loop gain to variations in the open-loop gain. In short, the highest possible $\hat{q}_p$, that is, open-loop poles as close together as possible on the negative-real axis, will minimize the closed-loop gain necessary to obtain the prescribed q_p.

11.5. Maximizing the Selectivity of RC Networks

In the case of a second-order passive RC network, the maximum selectivity that can possibly be obtained is when the pole Q of the network, namely $\hat{q}_p$, approaches 0.5. This is equivalent to obtaining a double pole on the negative-real axis in the s-plane which, as we have seen in the preceding section, can be achieved only in the limit by an infinite component spread; it is therefore impossible to actually realize in practice. We may now ask whether there is a simple way of obtaining a double pole ($\hat{q}_p = 0.5$) if we permit a simple active device to be included in the circuit? The answer is that by inserting a unity-gain amplifier in the RC ladder of Figure 11.1, as in Figure 11.5, we readily obtain a negative-real double pole.

We then obtain the transfer function:

$$T(s) = K\frac{\omega_p s}{(s+\omega_p)^2}$$

$$= K\frac{\omega_p s}{s^2 + 2\omega_p s + \omega_p^2} \tag{11.43}$$

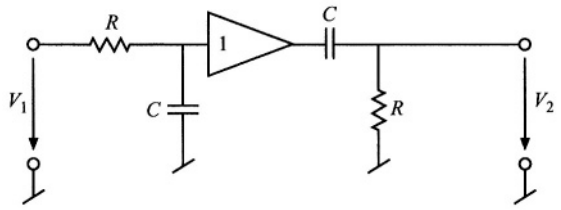


Figure 11.5. Second-order bandpass filter with double poles using a unity gain-buffer amplifier.

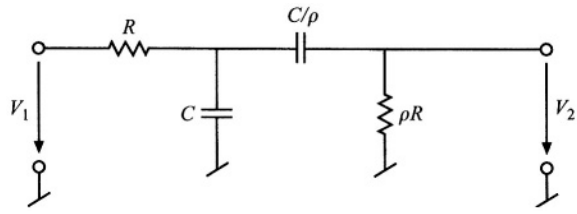


Figure 11.6. Second-order RC bandpass ladder filter with second L section impedance scaled by factor ρ.

where, referring to Figure 11.5, $\omega_p = (RC)^{-1}$ and the corresponding pole Q, $q_p = 0.5$.

The task of the unity-gain buffer is to prevent the second RC ladder section from loading the first. Clearly, an nth-order ladder network with n equal poles would, therefore, require $n - 1$ buffer amplifiers with one in between each RC L-section of the ladder network. Similar decoupling of the individual L-sections of an RC ladder network can be achieved by impedance scaling upwards (or "impedance tapering" , as we shall call it), the second L-section by a factor ρ, as shown in Figure 11.6. From equations (11.38c and d) it follows that in this case $x = 1$ and $\varepsilon = 1/\rho$, thus

$$\hat{q}_p = \frac{1}{2 + 1/\rho} \tag{11.44}$$

which for $\rho \to \infty$ approaches 0.5.

The actual plot of $\hat{q}_p$ versus ρ is shown in Figure 11.7, where we see that already for a value of $\rho = 3$, $\hat{q}_p = 0.43$, and for $\rho = 10$, $\hat{q}_p = 0.48$. For a higher order RC ladder network the third L-section would be impedance scaled by a factor ρ^2 and so on, with the nth section being impedance scaled by a factor ρ^{n-1}. Because each L-section is impedance scaled by a power of ρ higher than the previous section, its impedance level is tapered by an increasing power of ρ from left to right. The higher the impedance tapering factor ρ, the closer the

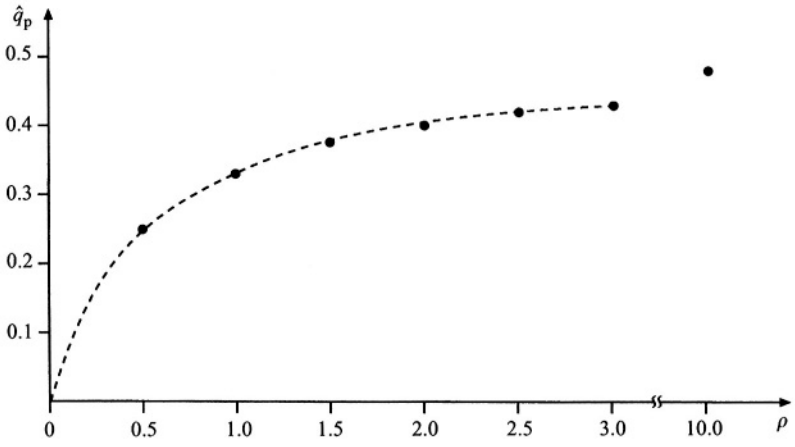


Figure 11.7. Plot of $\hat{q}_p$ versus impedance tapering factor ρ.

n negative-real poles of the RC ladder are clustered together on the negative-real axis of the s-plane, and the closer individual pole pairs are to having a $\hat{q}_p$ approaching 0.5. Thus, for the reasons given earlier, impedance tapering any RC network will minimize sensitivity to component variations by increasing the $\hat{q}_p$ of negative-real pole pairs. This is true not only for RC ladder networks, but for more general RC networks, such as bridged-T and twin-T networks, as well.

Consider for example, the twin-T network shown in Figure 11.8(a). As shown, the transfer function is:[1]

$$\text{Twin-T:} \quad \hat{T}(s) = \frac{s^2 + \omega_N^2}{s^2 + (\omega_N/\hat{q}_N)s + \omega_N^2} \tag{11.45}$$

where the notch frequency ω_N and the corresponding pole Q, $\hat{q}_N$ are, respectively,

$$\omega_N = \frac{1}{RC} \tag{11.46a}$$

$$\hat{q}_N = 0.25 \tag{11.46b}$$

Broken up into two symmetrical sections as in Figure 11.8(b), and impedance scaling the right section by a factor ρ (Figure 11.8(c)), we obtain the so-called

[1] Note that the twin-T network is actually a third-order network, but that for the values shown, the negative-real pole and zero are canceled out.

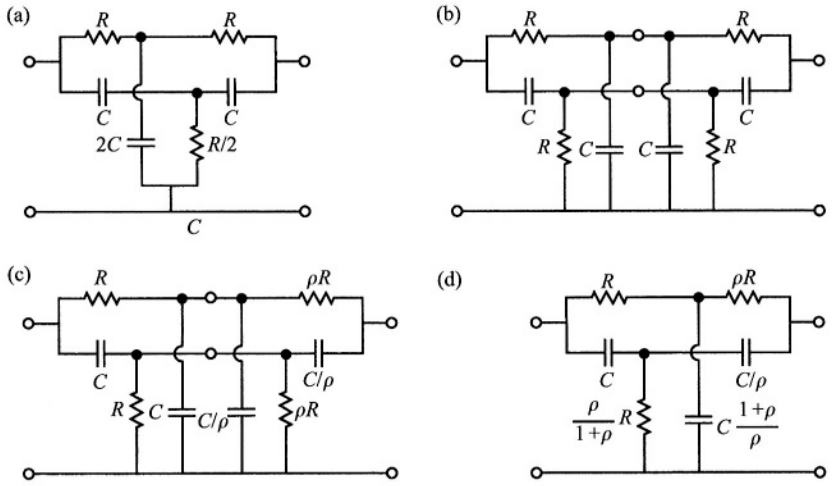


Figure 11.8. Twin-T network: (a) common configuration, (b) broken up symmetrically, (c) impedance tapered, (d) potentially symmetrical.

potentially symmetrical twin-T, where the notch frequency ω_N remains as in equation (11.46a) but $\hat{q}_N$ becomes:

$$\text{Twin-T:} \quad \hat{q}_N\big|_{\text{Potentially symmetrical}} = \frac{1}{2}\frac{\rho}{1+\rho} \tag{11.47}$$

which for $\rho \gg 1$ approaches 0.5. For $\rho = 3$ we obtain $\hat{q}_N = 0.375$, and for $\rho = 10$ we obtain $\hat{q}_N = 0.45$.

Similarly, the bridged-T shown in Figure 11.9(a) has the transfer function:

$$\text{Bridged-T:} \quad \hat{T}(s) = \frac{s^2 + (\omega_N/q_Z)s + \omega_N^2}{s^2 + (\omega_N/\hat{q}_N)s + \omega_N^2} \tag{11.48}$$

where

$$\omega_N = \frac{1}{RC} \tag{11.49a}$$

$$q_Z = 1 \tag{11.49b}$$

$$\hat{q}_N = \frac{1}{3} \tag{11.49c}$$

Deriving the potentially symmetrical bridged-T as shown in Figures 11.9(b)–(d), we obtain the same values for ω_N and q_z as above, but for the pole Q, $\hat{q}_N$ we obtain:

$$\text{Bridged-T:} \quad \hat{q}_N\big|_{\text{Potentially symmetrical}} = \frac{\rho}{1+2\rho} \tag{11.50}$$

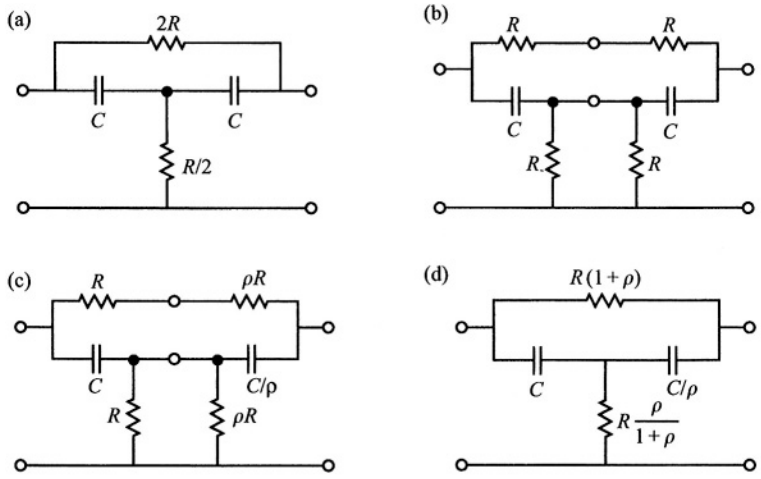


Figure 11.9. Bridged-T network: (a) common configuration, (b) broken up symmetrically, (c) impedance tapered, (d) potentially symmetrical.

For $\rho = 3$ we obtain $\hat{q}_N = 0.43$, and for $\rho = 10$, $\hat{q}_N = 0.48$.

With the examples above, namely of the RC ladder, twin-T and bridged-T networks, we have seen that by impedance scaling (which becomes *impedance tapering* in the case of the ladder, and *potential symmetry* in the case of the twin- and bridged-T networks), we have introduced a type of figure-of-merit, namely $\hat{q}$, which must approach its upper bound of 0.5 in order to minimize sensitivity and maximize selectivity. Approaching this upper bound always entails an increase in component spread by impedance scaling. This impedance scaling is performed in order to provide an impedance mismatch between individual circuit sections such as to minimize the loading of one section of a network on the preceding section. *The degree of mismatch attainable through impedance tapering depends on the degree of component spread permissible for a given technology.* The resulting trade-off can be considered only in the context of a specific application and technological realization, but with any kind of frequency-selective circuit, including various kinds of oscillators, it is bound to come up during the design process.

11.6. Some Design Examples

Consider the second-order lowpass filter shown in Figure 11.10(a). The transfer function is given by

$$T(s) = \frac{\beta\omega_p^2}{s^2 + (\omega_p/q_p)s + \omega_p^2} \tag{11.51}$$

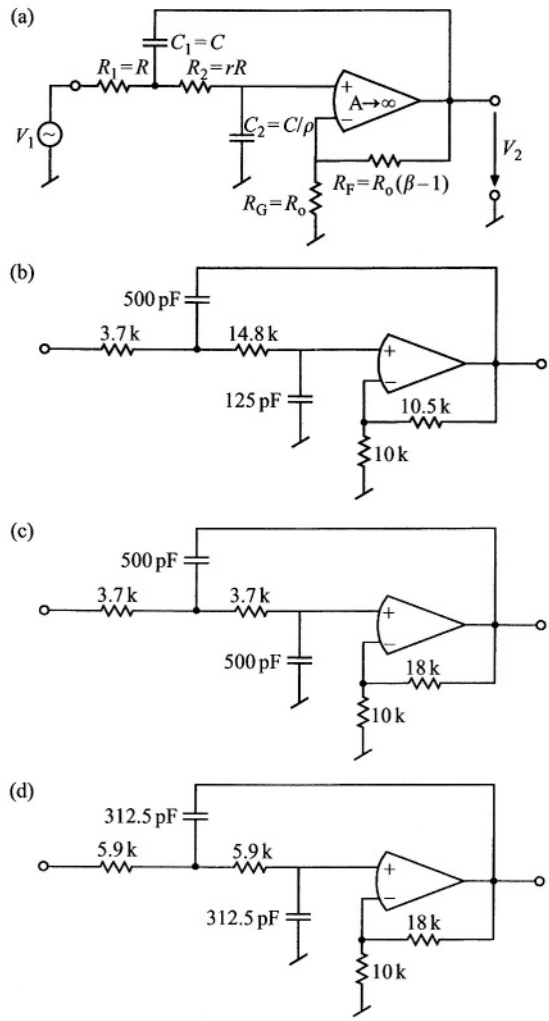


Figure 11.10. Second-order lowpass filter with ideal op-amp and voltage gain β, (a) with tapering factors r and ρ for resistors and capacitors respectively, (b) impedance tapered by $\rho = r = 4$, (c) non-tapered: $\rho = r = 1$, (d) non-tapered with $C_{tot} = 625$ pF.

where

$$\omega_p = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \tag{11.52a}$$

$$q_p = \frac{\kappa_1}{\kappa_2 - \beta\kappa_3} \tag{11.52b}$$

$$\kappa_1 = \sqrt{R_1 R_2 C_1 C_2} \tag{11.52c}$$

$$\kappa_2 = R_1 C_1 + R_2 C_2 + R_1 C_2 \tag{11.52d}$$

$$\kappa_3 = R_1 C_1 \tag{11.52e}$$

and

$$\hat{q}_p = \frac{\sqrt{R_1 R_2 C_1 C_2}}{R_1 C_1 + R_2 C_2 + R_1 C_2} \tag{11.53}$$

Letting

$$R_1 = R; \quad C_1 = C; \quad R_2 = \rho R; \quad C_2 = \frac{C}{\rho} \tag{11.54}$$

and

$$\omega_0 = \frac{1}{RC} \tag{11.55}$$

we obtain

$$\omega_p = \omega_0 = \frac{1}{RC} \tag{11.56}$$

and

$$\beta = 2 + \frac{1}{\rho} - \frac{1}{q_p} \tag{11.57}$$

Assuming the following filter specifications

$$\begin{aligned} \omega_p &= \omega_0 = 2\pi \cdot 86\,\text{kHz} \\ q_p &= 5 \\ C &= 500\,\text{pF} \end{aligned} \tag{11.58}$$

we obtain from (11.56) $R = 3.7\,\text{k}\Omega$. Assuming an impedance tapering factor $\rho = 4$, we obtain, from (11.57), $\beta = 2.05$. The r esulting filter is shown Figure 11.10(b). For the equivalent circuit with $\rho = 1$, we obtain $\beta = 2.8$ and the circuit of Figure 11.10(c). Figure 11.11(a) shows the amplitude response of this filter with ideal nominal components. Figures 11.1 l (b)–(g) show Monte Carlo runs with various combinations of resistor, capacitor and gain tolerances for the circuit tapered with $\rho = 4$, and non-tapered ($\rho = 1$), respectively. Noting the difference in the ordinate scale, it is clear that the tapered circuit is significantly less sensitive to component tolerances than the non-tapered circuit.

We now consider the third-order lowpass filter shown in Figure 11.12. The corresponding transfer function is given by:

$$T(s) = \frac{\beta a_0}{s^3 + a_2 s^2 + a_1 s + a_0} \tag{11.59a}$$

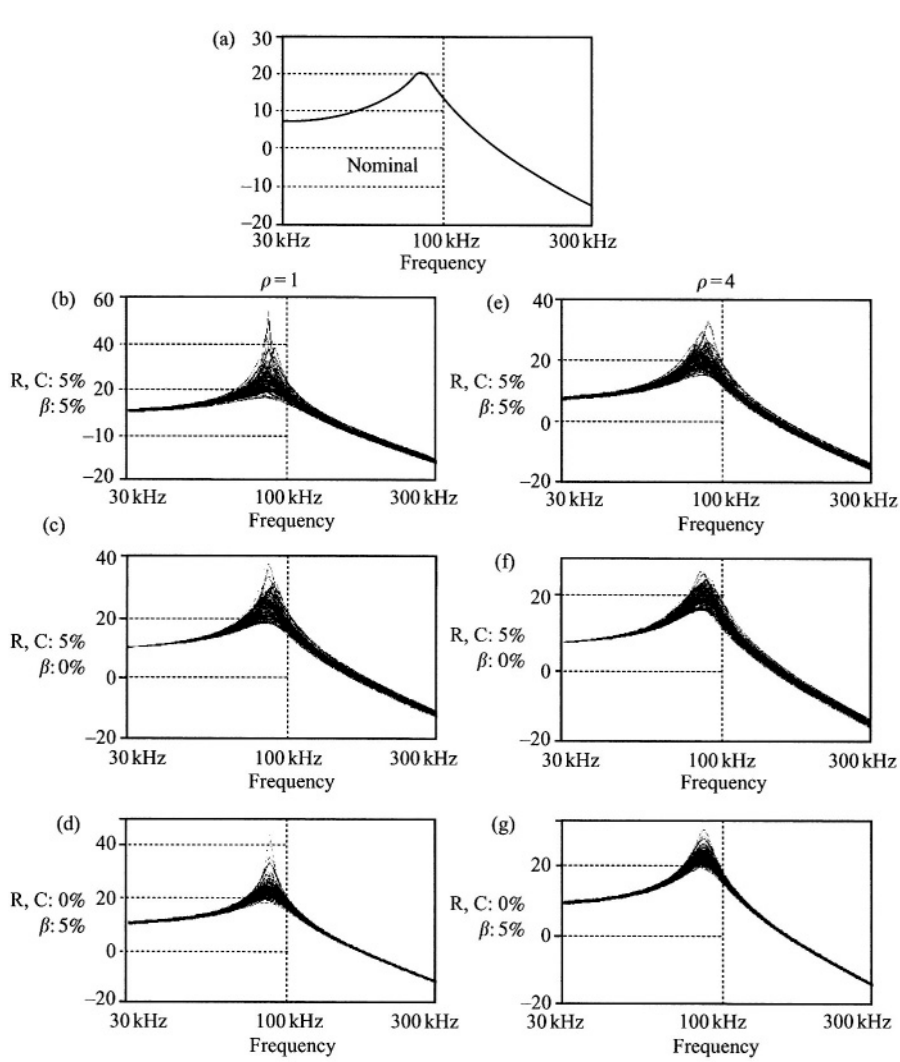


Figure 11.11. (a) Amplitude response of biquad shown in Figure 11.10(b) and (c) (nominal component values); (b–g) Monte Carlo runs for tapering factor $\rho = r = 1$ and $\rho = r = 4$.

where

$$a_0 = \frac{1}{R_1 R_2 R_3 C_1 C_2 C_3} \tag{11.59b}$$

$$a_1 = \frac{R_1 (C_1 + C_2 + C_3) + R_2 (C_2 + C_3) + R_3 C_3 - \beta C_2 (R_1 + R_2)}{R_1 R_2 R_3 C_1 C_2 C_3} \tag{11.59c}$$

$$a_2 = \frac{R_1 R_2 C_1 (C_2 + C_3) + R_1 R_3 C_3 (C_1 + C_2) + R_2 R_3 C_2 C_3 - \beta R_1 R_2 C_1 C_2}{R_1 R_2 R_3 C_1 C_2 C_3} \tag{11.59d}$$

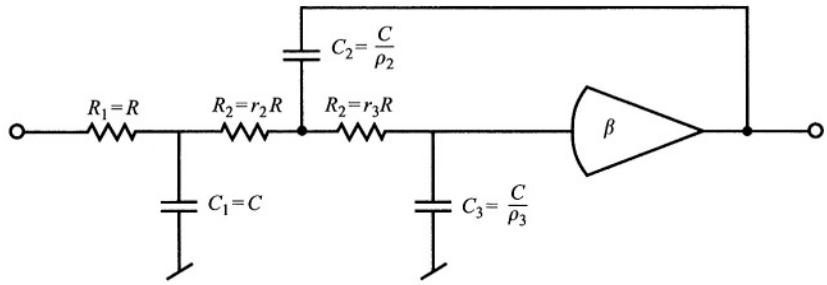


Figure 11.12. Impedance tapering a third-order lowpass filter by r_i and ρ_i, $i = 2, 3$.

Although $T(s)$ can be expressed in terms of a complex-conjugate pole pair with pole frequency ω_p and Q, q_p, as well as a negative-real pole γ, that is,

$$T(s) = \frac{\beta\omega_p^2\gamma}{(s+\gamma)\left(s^2 + (\omega_p/q_p)s + \omega_p^2\right)} \tag{11.60}$$

it is generally very difficult to find the relationship between these quantities and the components (i.e. resistors, capacitors and gain β). It is therefore more convenient to examine the variations of the polynomial coefficients a_i in terms of the component tolerances, that is,

$$\frac{\Delta a_i}{a_i} = \sum_{\mu=1}^{3} S_{R_\mu}^{a_i} \frac{\Delta R_\mu}{R_\mu} + \sum_{\nu=1}^{3} S_{C_\nu}^{a_i} \frac{\Delta C_\nu}{C_\nu} + S_\beta^{a_i} \frac{\Delta\beta}{\beta} \quad i = 0, 1, 2 \tag{11.61}$$

With the sensitivity relations given in Table 11.1, it can readily be shown that the variation of these coefficients can be minimized by tapering the third-order ladder network [1]. However, with networks of higher than second order, a tapering factor ρ can generally not be arbitrarily selected, because the resulting component values may turn out to be non-realizable (e.g. negative or complex). It can be shown that tapering the impedance of only the capacitors, while selecting the two resistors R_2 and R_3 to be equal (or vice versa), is sufficient to desensitize the circuit effectively from the effect of component tolerances.

Consider, for example, a third-order Chebyshev lowpass filter with coefficients

$$\begin{aligned} a_0 &= 0.749 \cdot 10^{17} \\ a_1 &= 0.341 \cdot 10^{12} \\ a_2 &= 0.59 \cdot 10^{6} \end{aligned} \tag{11.62a}$$

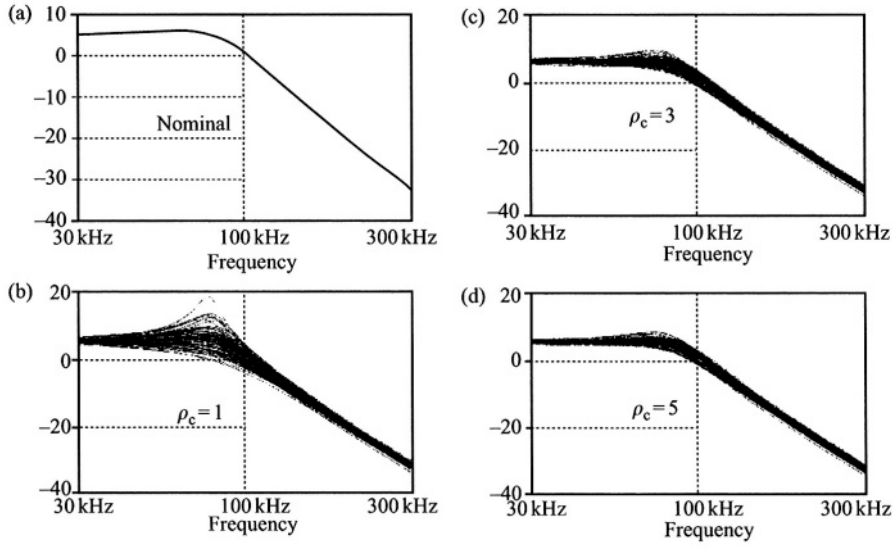


Figure 11.13. (a) Amplitude response of third-order Chebyshev lowpass filter; (b)–(d) Monte Carlo runs for various values of capacitive tapering.

or, with the equivalent dc gain and pole parameters:

$$\begin{aligned} K &= 2 \\ \omega_p &= 0.5037 \cdot 10^6 \\ q_p &= 1.7 \\ \gamma &= 0.295 \cdot 10^6 \end{aligned} \tag{11.62b}$$

This corresponds to a filter with a maximum ripple of 0.5 dB in the passband up to 75 kHz, and a minimum attenuation of 38 dB in the stopband above 300 kHz. The amplitude response of this circuit is shown in Figure 11.13(a) and Monte Carlo runs for 5% component tolerances shown for a non-tapered circuit (Figure 11.13(b)), and a capacitively-tapered circuit in Figure 11.13(c) and (d). Again, the efficacy of tapering in order to reduce the sensitivity to component tolerances is quite apparent from these curves.

11.7. Sensitivity and Noise

It has long been suspected (but never undisputedly proved) that low-sensitivity active RC filters are also low in output thermal noise. A recent publication substantiates this assumption [2]. In what follows, we further demonstrate with two design examples that biquads, designed for minimum

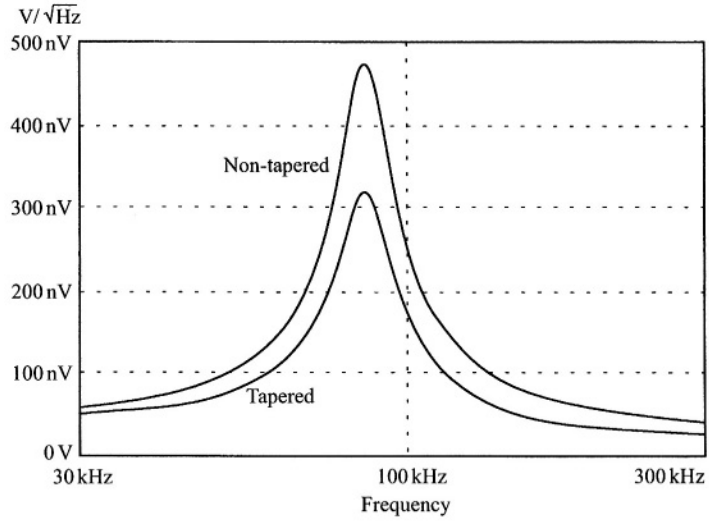


Figure 11.14. Output noise voltage in $V/\sqrt{Hz}$ for the circuit of Figure 11.10(c) (non-tapered) and Figure 11.10(b) (tapered with tapering factor = 4).

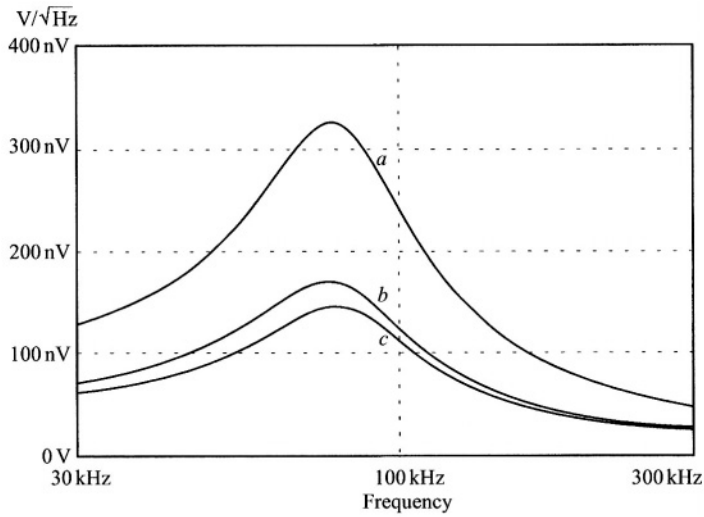


Figure 11.15. Output noise voltage in $V/\sqrt{Hz}$ for the circuit of Figure 11.12: (a) non-tapered, (b) tapered with $\rho_c = 3$, (c) tapered with $\rho_c = 5$.

sensitivity to component tolerances using the impedance tapering methods outlined above, are also superior, in terms of low output thermal noise, when compared with standard designs. In Figure 11.14, the output noise for the circuit of Figure 11.10(c) (non-tapered) and Figure 11.10(b) (tapered with tapering factor of 4) is shown. In Figure 11.15, the output noise for the circuit in Figure 11.12

for non-tapered (a), tapered with $\rho_c = 3$ (b), and tapered with $\rho_c = 5$ (c), is shown. The improvement in output thermal noise reduction is considerable, and comes free of charge, in that, as we have seen above, it requires simply the selection of appropriate component values to implement impedance tapering. It has been shown that the same phenomenon holds also for low-sensitivity (i.e. impedance tapered) higher order filters. As with biquads, they are also low in output thermal noise when desensitized to component variations by the use of impedance tapering. Just how much tapering is possible depends on the permissible component spread and comprises one of the principle trade-offs dealt with in this chapter.

11.8. Summary and Conclusions

We show in this chapter that the sensitivity of active RC filters can be minimized by appropriate impedance mismatching in the form of impedance tapering for RC ladder networks, and potential symmetry for bridged-T and parallel-ladder (e.g. twin-T) networks. This procedure, however, invokes a design trade-off in that it automatically increases the spread between the resistors and capacitors, which is generally constrained by the technology used to manufacture these components. An acceptable trade-off, therefore, depends on the technology used, and on the circuit characteristics, in that the sensitivity to component tolerances may be reduced, while the component quality and their tolerances may actually be increased, by the component spread. The trade-off is worth considering and dealing with, however, because, within the limits of an acceptable component spread, the reduction in sensitivity and output noise of the resulting active RC filters is considerable.

References

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[2] Drazen Jurisic and George S. Moschytz, "Low-noise active-RC low-, high- and band-pass allpole filters using impedance tapering", in *Proceedings of the 10th Mediterranean Electrotechnical Conference MELECON 2000,* vol. II, pp. 591–594, Lemesos, Cyprus, May 2000.

Chapter 12

CONTINUOUS-TIME FILTERS

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12.1. Introduction

As the rest of this book illustrates, analog circuit design is ripe with compromises and trade-offs, some arising from fundamental limitations and some from practical realities. (Actually, many parameters are best pushed to their maximum limits; those just aren't as interesting.) In the following, we will examine several fundamental and practical trade-offs in the design of continuous-time filters. Some issues will only be mentioned; a few others will be illustrated in more detail. We will consider trade-offs in filter design, in circuit topology and in strategies for filter tuning.

When we think about specifications for analog integrated signal processing elements, power dissipation, power-supply voltage, noise, filter accuracy, dynamic range, distortion are the first to spring to mind. However, integrated circuit (IC) chip area, manufacturing cost and yield, testability, and the availability of suitable technologies should not be ignored. Another issue, rarely explicitly considered in such lists of important parameters, is the ease and related cost of design: a simple, under-performing design that is well understood may be superior in practice to one that is too complicated or that takes too long to design. Even esthetic or marketing issues can be important. However, we shall focus here on more practical engineering issues.

Filtering is one of the most important functions in analog signal processing. While many filtering tasks now use digital signal processing, continuous-time filters are still important. Continuous-time filters are commonly used as equalizers for magnetic disk drives and for anti-aliasing and reconstruction filters, etc. Continuous-time filters would be used in many more applications if difficult trade-offs in their design did not limit their usefulness.

12.2. Filter-Design Trade-Offs: Selectivity, Filter Order, Pole Q and Transient Response

To enhance the ability to pass a signal of one frequency while rejecting another (selectivity), we increase the order (number of transfer-function poles) of the filter. Increasing filter order adds complexity, chip area and power.

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High-selectivity filtering also usually requires pole pairs to be complex conjugate, with some pole pairs having high quality factor (Q). The concept of Q is used in many different contexts; its fundamental definition relates total stored energy to energy loss. The Q of a complex pole pair is the ratio of the pole magnitude to twice the real part. Increasing pole Q extends the duration of transient step and impulse responses. Also, it is easy to show [1] that noise power in active filters increases in proportion to Q.

12.3. Circuit Trade-Offs

12.3.1. Linearity vs Tuneability

One key property of a signal processor is its linearity. If a system is linear, when sinusoidal signals are applied as inputs, the output consists only of sinusoids of the same frequencies as the input. The effect of the circuit on the magnitude and phase of each sinusoidal component as a function of frequency is the transfer function. Distortion is a measure of the relative output power at frequencies that were not present in the input. Since in a linear system, the filter transfer coefficients should stay constant as the signal amplitude is varied, linearity can also be characterized by measuring how much these coefficients vary from constancy.

12.3.2. Passive Components

Continuous-time filters can be implemented in a variety of ways. Classic RC active filters use operational amplifiers, with high (nominally infinite) negative-feedback loop-gain, to obtain high linearity using constant-valued passive components. As we will see, integrated continuous-time filters require electronic tuning to correct for manufacturing process variability, temperature and power-supply voltage variations. The dependence of the filter coefficients on passive components thus conflicts with the need for tuneability.

Until a few years ago, integrated circuit technologies were usually designed to optimize the performance of digital circuitry. The shrinking proportion of analog functionality in mixed-signal ICs did not justify including special options useful only for analog. However, with the increasing use of foundry processes, there is pressure to include more options to make processes more general. As digital processes themselves have become more complicated (they often now have four or more metal layers), the relative cost to add process steps decreases. Thus new technologies often allow special analog options to provide linear passive components.

The most important passive components in IC technologies are resistors and capacitors. On-chip resistors can be made using various materials, sometimes using layers that are already available in the IC. The resistance is determined by

the conductivity and geometry of the layer, and so is not usually tuneable, but it can be quite signal independent. High-value resistors usually require large chip areas, and are thus costly. High-resistivity layers that would allow smaller area tend to match poorly, which degrades performance or yield.

Standard CMOS technologies provide limited options for linear capacitors. MOS capacitors using the thin gate oxide of the MOSFET have high capacitance per unit area, but the capacitance is voltage dependent and thus nonlinear. However, the voltage dependence is reduced in the accumulation region of operation, so such MOSCAPs operated in accumulation can be used in low-precision applications, although biasing can be awkward. On the other hand, in applications where tuneability is more important, voltage-dependence may be considered an advantage. In such cases, it is more common to use the well-defined voltage-dependent capacitance of a reverse-biased PN-junction to form a varactor. The metal-oxide metal (MOM) capacitance between wiring layers is quite linear, but to minimize cross talk between layers, these are designed to have low capacitance per unit area. Special processing may allow linear capacitor options for MOM or poly-poly capacitors with relatively high capacitance per unit area.

For processing frequencies in the GHz range, it is practical to include on-chip inductors, although they require a lot of chip area. The inductance is mostly determined by the geometry of the windings, so these are usually not tuneable.

The values of these elements will vary from lot to lot, from wafer to wafer, from die to die and from one location on a die to another. In general, the more "closely related" two nominally matched components are to each other, the closer they will match. Thus lot-to-lot variations in a high-value resistor might average 30% or more, whereas the mismatch of two resistors, carefully laid out close together on the same chip, could match within 0.1%. As we will see, some filter coefficients are dimensionless and others have dimensions of time or frequency. Products of resistance and capacitance or inductance and capacitance determine the time or frequency coefficients. It is because capacitance values do not predictably track resistance or inductance values that continuous-time filters usually require post-fabrication tuning.

12.3.3. Tuneable Resistance Using MOSFETs: The MOSFET-C Approach

The passive elements just considered are all two-terminal elements, which can never be at once both linear and tuneable. For an element to be both linear and tuneable, it must have a separate control input. For example, a MOSFET operated in triode region can implement a voltage-variable resistor. Consider the simple square-law model for the MOSFET, which predicts that a current

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\cdot(V_{gs} - V_t)^2$$

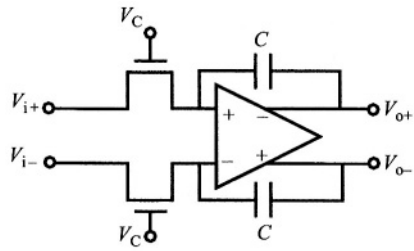


Figure 12.1. MOSFET-C integrator.

in active (saturated) operation ($V_{ds} > V_{Dsat}$) and

$$I_D = \mu C_{ox} \frac{W}{L} \cdot (V_{gs} - V_t - V_{ds}/2) \cdot V_{ds}$$

in the triode region ($V_{ds} < V_{Dsat}$). To the extent that these relationships are exact, there are a variety of ways that MOSFETs can be used to implement tuneable filter elements.

For example, Figure 12.1 shows a simple MOSFET-C integrator in which a pair of matched MOSFETs, operated in triode, are used to implement an electronically tuneable resistor [2]. The differential op-amp holds their sources at the same potential, and the input voltage signal is applied differentially between the drains. A control voltage V_C applied to the gates is used to vary the resistance of the source-drain channel. The MOSFET currents are quadratically related to the input signal voltage, with constant, linear and second-order terms. However, when the currents are subtracted, the constant terms and the nonlinear second-order terms cancel. This is a general property that arises from symmetry: differential operation ideally allows cancelation of all even-order nonlinearities. In practice, of course, because of mismatch, balance is never perfect, and real circuits always produce some odd-order nonlinearities.

The MOSFET-C approach can achieve good linearity at moderate frequencies. However, it requires differential op-amps with common-mode feedback (CMFB). Also, the amps must be able to drive resistive loads, which is difficult in CMOS technologies. Also, as in any active-RC filter, op-amp stability requirements limit use of the MOSFET-C approach for high-frequency applications.

12.4. The Transconductance-C (Gm-C) Approach

Gm-C filtering avoids many of these limitations. In this approach, transistors are used, often with little or no feedback, to implement electronically tuneable

voltage-controlled current sources, along with nominally linear capacitors to implement filter elements.

The ideal transconductor would implement a linear voltage-controlled current source with a predictably adjustable transconductance that is independent of the signal amplitude, with zero input-output phase shift and zero output admittance over all relevant frequencies. In practice, we must accept thermal and flicker noise, limited dynamic range, minimum power-supply voltage, finite output admittance and parasitic phase errors. A wide variety of circuits have been proposed to implement transconductors [3]. Rather than attempt detailed comparison, this survey will compare a few different approaches based on trade-offs in their fundamental operating principles.

12.4.1. Triode-Region Transconductors

The triode-region square-law model predicts that a triode-region transconductor in which a constant V_{ds} controls the transconductance G_m, and V_{gs} is the input, such as shown in Figure 12.2, would be linear even for single-ended operation. Differential operation should further enhance linearity. However, triode-region operation requires a low G_m/I ratio, with correspondingly high V_{gs}. This leads to large vertical electric fields in the transistors, which leads to significant odd-order nonlinearity. These odd-order errors are not improved by differential operation. The op-amp loops in the figure could be replaced by simpler circuits with lower loop gain and higher speed (less parasitic phase shift). However, the reduced feedback raises the resistance seen by M_1 and M_2, which will degrade linearity.

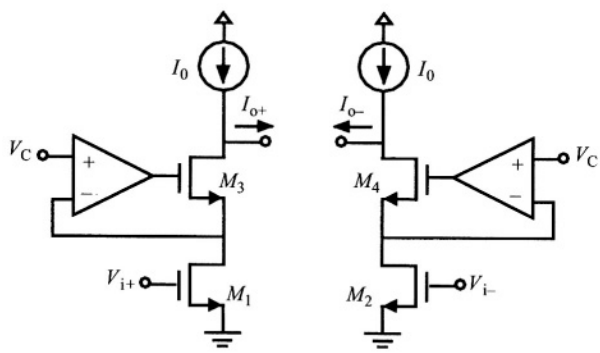


Figure 12.2. A triode-region transconductor.

12.4.2. Saturation-Region Transconductors

A variety of transconductors have been proposed that use differential circuitry to exploit the saturation square-law equation. Since the square-law saturation-region current expression has only second-order nonlinearity, differentially operated saturation-region transconductors can, in this approximation, be perfectly linear. Among MOSFET-based topologies, this class of circuits has the highest transconductance for a given bias current. This leads to lower vertical electric fields and which reduces this source of odd-order nonlinearity. The simplest approach uses differentially operated common-source FETs or even CMOS logic inverters, with tuning provided by the common-mode voltage, which also sets the bias current. Since output resistance in saturation can be high, it may be possible to avoid cascoding the outputs, which would reduce high-frequency phase errors. This trade-off will be discussed later.

12.4.3. MOSFETs Used for Degeneration

The transconductors discussed so far have all used FETs with grounded sources. In such circuits, the common-mode input voltage must be controlled to set the operating currents (usually by CMFB in a previous stage). To allow a range of common-mode inputs, a source-coupled pair with tail-currents sources can be used. Source-coupled MOSFET differential pairs are highly nonlinear. Degeneration using fixed source resistors would improve linearity but reduce tuneability. A useful alternative is to degenerate the circuit using cross-coupled MOSFET's, as shown in Figure 12.3. Simulations and accurate modeling are required to optimize the trade-offs between the sizes of the transistors [4].

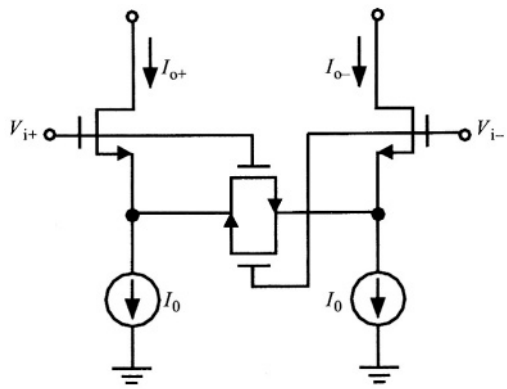


Figure 12.3. Transconductor using FET degeneration.

12.4.4. BJT-Based Transconductors

Bipolar junction transistor (BJT) and BiCMOS technologies are more expensive than CMOS. In processes that include BJTs, they are the best choice for most analog applications, because of their near-optimum G_m/I ratio. However, for transconductor applications, this can actually be a disadvantage. It means that nonlinearities in the current-voltage characteristic become large for very small voltage swings. The Ebers–Moll exponential model for the BJT contains both even and odd-order nonlinearities, so that differential operation cannot eliminate the odd-order distortion components. However, the large transconductance can be traded off for high linearity by including resistive degeneration, as in the MOSFET case, although this reduces tuneability.

To retain the linearity of these degenerated transconductors while providing some tuneability, the output currents can be passed to a translinear multiplier circuit used as a current mirror with electronically variable current gain. Unfortunately, the low input impedance of the multiplier in this approach lowers the input-stage voltage gain and degrades noise performance [5].

12.4.5. Offset Differential Pairs

Another way to linearize and degenerate a BJT-based transconductor uses a parallel connection of multiple differential pairs with intentionally introduced offsets to spread nonlinearities over a wider range of input voltages [6]. The offsets can be introduced by using multiple differential pairs with unequal emitter areas. In the limit of large number of such pairs, with the offsets chosen optimally, this gives the benefits of degeneration while providing wide-range tunability. Using even a few differential pairs significantly enhances linearity. This method does increase the required layout area and the increased capacitance limits frequency response.

12.5. Dynamic Range

The most fundamental trade-offs in Gm-C filter design involve dynamic range. The dynamic range of a signal processor is the ratio of the largest to the smallest signals that can be processed. The amplitude of the largest signals is limited by nonlinearity, which in practice is the amplitude for which some maximum tolerable level of distortion is reached. The lower end of the dynamic range is usually set by noise. Ideally the noise is dominated by unavoidable thermal noise. Flicker noise or extraneous noise injected from other parts of the system may further degrade the signal-to-noise ratio (SNR). While in most systems, dynamic range is equivalent to SNR, in some systems dynamic range may be limited by the ratio of the largest signal to the resulting distortion

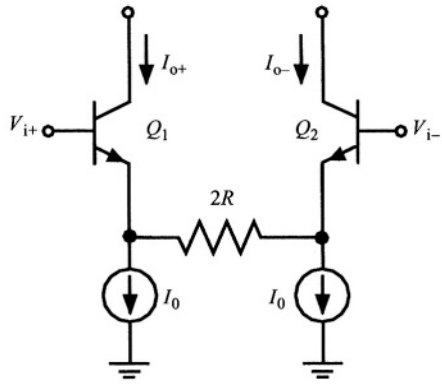


Figure 12.4. Degenerated BJT transconductor.

products rather than by the SNR. Also, as we will see, companding can allow dynamic range to exceed the SNR.

Analysis of the degenerated BJT transconductor (Figure 12.4) illustrates several fundamental trade-offs in continuous-time filter design [7]. The differential equivalent input voltage per unit bandwidth due to thermal noise is given by

$$\begin{aligned}\frac{v_{\text{ein}}^2}{\Delta f} &= 2 \cdot 4kT\left[\frac{1}{2g_{\text{m}}} + \frac{R}{2}\right] \\ &= \frac{4kT}{g_{\text{m}}} \cdot [1 + g_{\text{m}}R] \\ &= \frac{4kT}{G_{\text{m}}}\end{aligned} \tag{12.1}$$

where the transconductance of the circuit can be expressed as $G_{\text{m}} = g_{\text{m}}/(1 + g_{\text{m}}R) = g_{\text{m}}/N$, where $N = 1 + g_{\text{m}}R$ is the degeneration ratio. Now, $g_{\text{m}} = I_0/(kT/q)$ is the maximum transconductance achievable from a transistor. BJTs closely approach this limit. We can also write the degeneration factor as the ratio $N = g_{\text{m}}/G_{\text{m}}$.

If the transconductor drives a differential load capacitor of value C, the result is an integrator with unity-gain frequency $\omega_0 = G_{\text{m}}/C$. This integrator can be used in a first-order low-pass filter. Integrating over the effective noise bandwidth of a first-order low-pass with cut-off frequency ω_0 gives the total squared input noise of kT/C. As with any class A circuit, the maximum current signal is limited by the bias current I_0. The maximum voltage swing is then $V_0 = G_{\text{m}}I_0 = N \cdot kT/C$. From this we can conclude that the maximum

signal-to-noise ratio is

$$\mathrm{SNR}_{\max} = V_0^2 \cdot \frac{C}{8kT} = N^2 k \frac{TC}{8q^2} \tag{12.2}$$

This implies that dynamic range can be increased arbitrarily by increasing the degeneration factor. In practice, the maximum signal swing must be less than the total power supply voltage V_{DD}. When power and cut-off frequency are constrained, the benefits of degeneration are reduced, and the maximum SNR of such a filter is proportional to

$$\mathrm{SNR}_{\max} = \frac{P}{M \cdot kT \cdot f_0} \tag{12.3}$$

where $M = V_{DD}/V_0$ and f_0 is the cut-off frequency.

12.6. Differential Operation

Differential operation does not usually offer much of a trade-off, since its advantages so often overwhelm its disadvantages. Thus, differential operation is common in all aspects of analog signal processing, since in addition to improving linearity, it also enhances rejection of interfering signals transmitted through the substrate and through bias and power-supply lines; such signals are increasingly problematic in mixed-signal circuits where digital circuits, with their fast transitions. The main disadvantage of differential operation is the need for CMFB circuits. Their design can be more challenging than the differential circuits.

12.7. Log-Domain Filtering

A way to work around these noise and signal-range limitations, while providing high linearity in BJT-based filters is the log-domain approach [8,9]. Rather than individually linearize each transconductor, signals within a log-domain filter are allowed to be highly nonlinear, and pre- and post-distortion are used to cancel the nonlinearities of the overall filter.

Log-domain circuits can be arranged to operate in a class AB mode, in which they implement so-called instantaneous companding. Such circuits can process current-mode signals that are much larger than the bias currents. In class A mode, where signals are less than the bias currents, noise power is independent of signal amplitude, so the SNR is proportional to signal amplitude. In class AB operation, the noise increases with the instantaneous signal. As the signal amplitude increases, the average noise increases as well, and the SNR saturates. This noise modulation effect limits the usefulness of instantaneously companding filters in some applications: high-amplitude signals in the filter's

stopband can intermodulate with the noise, producing unacceptable noise in the passband.

12.8. Transconductor Frequency-Response Trade-Offs

Two main effects limit transconductor frequency response. At low frequencies, the main effect arises due to finite output resistance R_{out}, or equivalently, finite low-frequency gain $g_m R_{out}$. Low dc gain typically lowers pole Qs. This is often a cause of limited low-frequency rejection in band-pass filters. The usual way to raise transconductor R_{out} is cascoding, in which the transconductor's signal current is passed through a common-gate transistor. This multiplies the output resistance by the intrinsic gain of the added transistor. However, cascoding tends to degrade the high frequency-response of transconductors, since it adds at least one extra node to the circuit. The parasitic capacitance at the source of the added transistor adds high frequency phase shift that degrades filter response at high frequencies.

To allow filter operation at frequencies into the hundreds of MHz, the intermediate node added by cascoding should be avoided. In a transconductor without such intermediate nodes, phase errors at high frequencies arise only from second-order effects such as transmission-line effects due to distributed time delays along the gate. Without cascoding, however, low-frequency transconductor gain is limited to that of a single gain stage, typically less than 100, too low for any but very low-Q filter applications.

One solution is to use positive feedback using cross-coupled inverting transconductors, as shown in Figure 12.5. In [10], the individual transconductors were implemented using saturation-region transconductors identical to standard CMOS logic inverters. Filter frequencies were set by varying the transconductor V_{DD} inputs. The V_{DD} connections for the cross-coupled

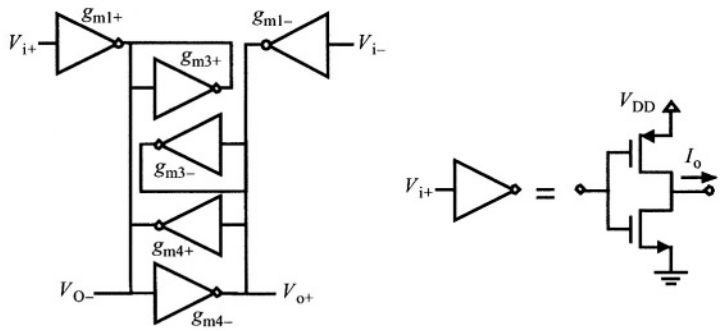


Figure 12.5. Cascode-free transconductor using positive feedback.

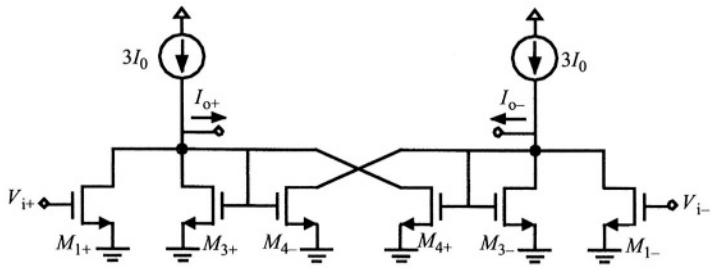


Figure 12.6. Low-voltage cascode-free transconductor.

transconductors had separate V_{DD} inputs, so that G_{m4} could be set independently of G_{m1} and G_{m3}. The differential-mode gain is $A_{DM} = G_{m1}/(G_0 + G_{m3} - G_{m4})$. A Q-tuning circuit was used to adjust G_{m4} to cancel $G_0 + G_{m3}$. Mismatch limits the achievable cancelation.

High loop-gain CMFB is not needed, since the common-mode output resistance of the transconductor is low and the common-mode voltage gain $A_{CM} = G_{m1}/(G_0 + G_{m3} + G_{m4})$ is approximately 1/2.

This approach is well suited for low-voltage operation. The required value of V_{DD} is $2|V_{gs}|$ and the range for nominally linear signal swing is the sum of the NMOS and PMOS threshold voltages, $V_{tN} + |V_{tP}|$. However, the circuitry required to tune V_{DD} means that the actual supply voltage must be much higher than V_{DD}. Another disadvantage of this circuit is the strong dependence of the operating current on V_{DD}, which impairs the power-supply rejection ratio (PSRR).

A circuit variation that addresses many of these limitations is shown in Figure 12.6, which uses a folded signal path with PMOS devices used only for biasing [11]. Frequency tuning is accomplished using current sources, eliminating the overhead for tuning V_{DD}. The minimum supply voltage for the circuit can be as low as $V_{DD\,min} = V_{TN} + V_{DsatN} + |V_{DsatP}|$. The bias currents are no longer strongly affected by V_{DD}, which significantly improves PSRR. As drawn in the figure, there is no way to adjust G_{m4} to maximize Q. A triode-connected FET could be included in M_{4S} source to allow such adjustment, at some cost in linearity.

12.9. Tuning Trade-Offs

Any filter transfer function has several parameters that may require tuning. In a first-order filter, the pole frequency, the passband gain and possibly the stopband gain (or equivalently, a zero's frequency) may require tuning. In higher order filters with complex poles, each biquadratic section potentially has several tuneable parameters: the cut-off frequencies and quality factors or

Q of the poles and those of any complex zeros, as well a gain factor. Pole or zero frequencies are always determined by ratios or products of two independent parameters, such as the G_m/C ratio. These quantities generally do not track each other with temperature or process variations, and thus usually require tuning. Gain and quality factors, being dimensionless, are determined by ratios of like elements such as capacitances or of transconductances. With proper care to ensure adequate matching, such parameter ratios may not need to be tuned. However, the sensitivity of most filter parameter to element variations is proportional to Q^2. In highly selective filters, which usually include high-Q poles, tuning of pole or zero Q may be necessary. Q-tuning circuits often are very complex, and require large chip area. In any event, the effectiveness of any tuning approach is ultimately limited by mismatch. This is the most serious limitation on the use of continuous-time filtering for high-Q applications.

Several tuning strategies may be considered, ranging from no tuning at all to tuning of the frequencies and Qs of multiple poles and zeros.

No tuning. If the specifications are loose enough and the process, temperature and voltage-induced variability is small enough, tuning may be unnecessary. This allows the use of passive conductors or highly degenerated transconductors, potentially offering wide dynamic range.

Off-chip tuning. In this approach, on-chip transconductances are controlled by current or voltage inputs. A feedback loop can be used to force transconductances to track an off-chip conductance whose temperature coefficient is chosen to compensate for the assumed temperature coefficient of on-chip capacitors. The extra pins and external components required are disadvantages of this approach.

One-time post-fabrication tuning. Coarse tuning can be achieved by selecting capacitors from an array using digital post-fabrication tuning or by blowing on-chip fuses. A related approach is to laser-trim an on-chip resistor used as a reference in a feedback arrangement as described in the previous section. Because each must be individually tuned, such strategies increase test and assembly costs. A compromise is to measure the required value for a few samples in each lot and apply the same correction to each part.

Automatic tuning. On-chip tuning strategies often use a phase-locked loop (PLL) in a master–slave arrangement to set cut-off frequencies. In a typical approach, a voltage-controlled oscillator (VCO) is formed using a loop of two identical Gm-C integrators. The VCO is phase-locked to an external frequency reference. The Barkhausen conditions for constant-amplitude oscillations of such a loop require 90-degree phase shift for each integrator, at the unity-gain

frequency. The voltage needed to meet these criteria within the oscillator (the master) is assumed to match that required for transconductors within the filter (the slaves), and can thus be used to tune the unity-gain frequency of the slaved transconductors. An oscillator based on a two-integrator loop generally includes an automatic gain control (AGC) circuitry to keep the amplitude constant. The output of this AGC circuitry can be used to adjust Q.

However, this master–slave arrangement has several fundamental limitations, and requires some difficult compromises. Mismatch between the master and the slave, inevitable in any analog system, leads to errors in tuning. To minimize these mismatches, the master and slave should be as close as possible to each other in all aspects, including their layouts and their operating conditions. This is clearly only approximately possible in a complex filter with multiple pole and zero frequencies. Furthermore, if the PLL operating frequency is close to the filter passband or stopband the PLL is likely to interfere with the filter.

12.10. Simulation Issues

IC design customarily depends heavily on computer simulation. In continuous-time filters, performance depends strongly on the details of transistor operation. The simple transistor models described previously are inadequate for designing continuous-time filters to meet linearity specifications. In particular, MOSFETs with short channels do not follow the square law, and in fact rarely follow any simple equation very accurately. Even in long-channel transistors, mobility reduction and other effects cause nonlinearities that simple models fail to predict. In this regard, BJT's may be easier to design with, as their analytical models correspond fairly closely to their actual behavior.

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Chapter 13

INSIGHTS IN LOG-DOMAIN FILTERING

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13.1. General

Log-domain filter operation is characterized by the absence of linearization schemes. In contrast, for example, to the g_m-C integrated filter design approach which relies upon the implementation of linear transconductors, the log-domain technique treats intrinsic nonlinear (exponential) I–V characteristic of a BJT or a weakly inverted MOST as an asset, which is carefully exploited to produce input–output linear but internally nonlinear frequency shaping networks.

The investigation of the log-domain filtering technique is motivated by its potential for high dynamic range operation under fairly low power supply levels when the input–output linearity is preserved in a large-signal sense. In this way, the processing of large input signals is allowed.

Generally speaking, a log-domain filter consists of:

1 an input current signal I-to-V logarithmic compressor (e.g. a diode-connected device);

2 the main filter body where the devices operate according to their large-signal characteristic and signal processing in the logarithmic domain (log-domain integration) takes place, and

3 the exponential expander (e.g. a single device) situated at the output where a conversion from logarithmically compressed and processed (by the main filter body) voltages to output current signal takes place.

As a firsthand example, let us consider Figure 13.1, which depicts a first-order log-domain filter with the aforementioned stages identified.

The input–output response is linear with the respective transfer function given by

$$\frac{I_{\text{out}}(s)}{I_{\text{in}}(s)} = \frac{(I_0/CV_T)}{s + (I_d/CV_T)} \tag{13.1}$$

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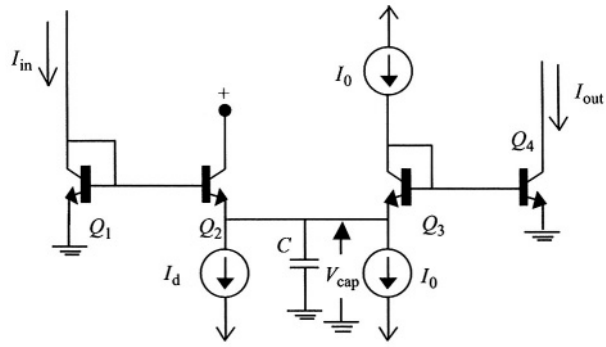


Figure 13.1. A log-domain lossy integrator.

However, the integration capacitor voltage V_{cap} is non-linearly related to the input and output currents $I_{in}(t)$ and $I_{out}(t)$ (the devices are assumed to be matched in terms of I_S and V_T):

$$I_{out}(t) = I_S \exp\left[\frac{V_T \ln(I_0/I_S) + V_{cap}}{V_T}\right] = I_0 \exp\left(\frac{V_{cap}}{V_T}\right) \tag{13.2a}$$

$$I_d + C\dot{V}_{cap} = I_S \exp\left[\frac{V_T \ln(I_{in}/I_S) - V_{cap}}{V_T}\right] = I_{in} \exp\left(\frac{-V_{cap}}{V_T}\right) \tag{13.2b}$$

Observe that every device involved operates obeying its exponential (large-signal) I–V characteristic. Recalling that

$$\frac{d}{dt}\left[\exp\left(\frac{V_{cap}}{V_T}\right)\right] = \exp\left(\frac{V_{cap}}{V_T}\right)\left(\frac{\dot{V}_{cap}}{V_T}\right)$$

it can be deduced for the input and the output currents:

$$I_d \frac{I_{out}}{I_0} + (CV_T)\frac{\dot{I}_{out}}{I_0} = I_{in} \tag{13.2c}$$

which is a linear differential equation (DE) with constant in-time coefficients leading to (13.1).

The above example enables the reader to realize that in log-domain filtering, a substantial amount of design effort needs to concentrate on the systematic articulation of synthesis paths, which embody in full the nonlinear (exponential) device characteristic, while preserving the input–output linearity of higher order transfer functions.

Expressing a general transfer function in its equivalent state-space formulation and considering its g_m-C implementation, its input–output linearity is preserved by the successful implementation of linear building blocks (g_m) from

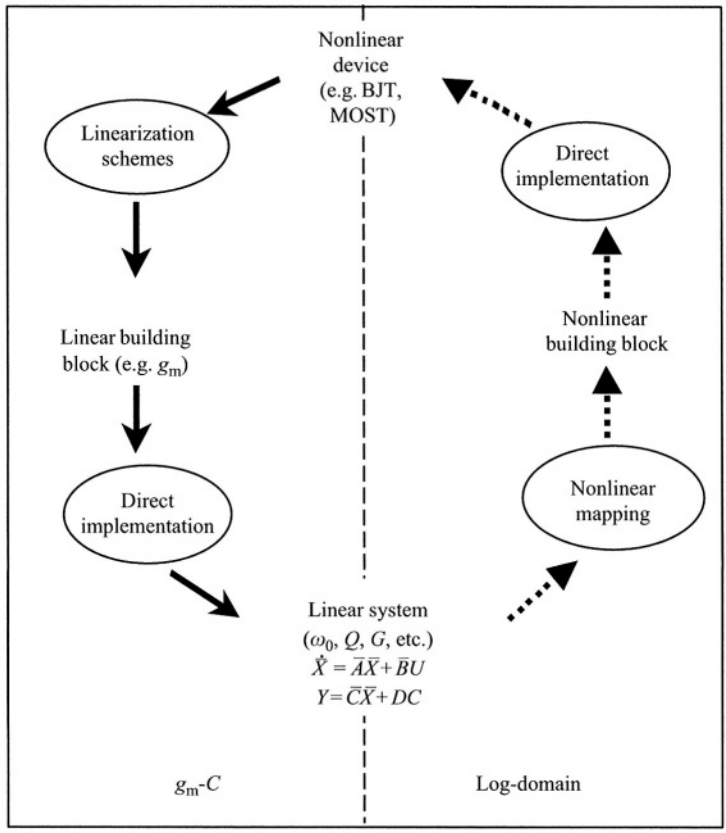


Figure 13.2. Log-domain as opposed to g_m-C design philosophy.

nonlinear devices. In contrast, the log-domain circuit paradigm allows for the realization of an input–output linear filter by exploiting the device nonlinearity without resorting to linearization schemes (see Figure 13.2). The scope of linearization schemes is to extend the linear region of operation of the g_m, enabling the accommodation of larger differential input signals which generally leads to an increased input dynamic range.

Emitter degeneration is such an indicative linearization scheme (see Figure 13.3(a) and (b)). Observe that at the expense of increased power consumption, chip area, additional parasitic capacitances and output signal gain, the higher the value of R_E, the larger the input signal for which the input–output relation remains linear. A detailed distortion analysis would confirm that the third-order harmonic distortion component – which is of practical significance for fully differential topologies – is reduced when emitter degeneration is applied. Referring to Figure 13.4(b), if V_Q and V_p are the quiescent and

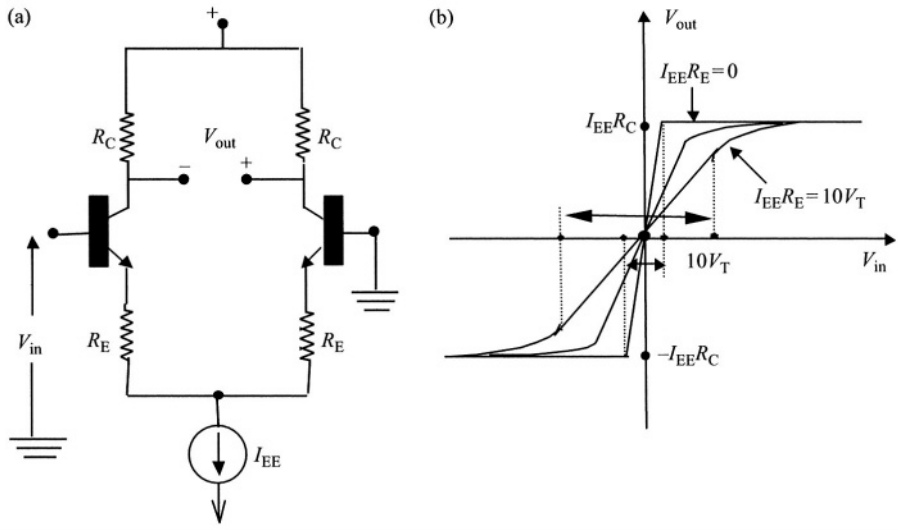


Figure 13.3. Emitter feedback (via R_E) in (a) an emitter coupled pair and (b) its linearization effect [1].

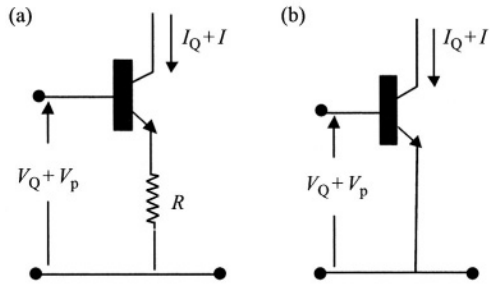


Figure 13.4. A common emitter configuration (a) with and (b) without emitter degeneration.

incremental input-signal values, respectively, then it can be shown that the third-order harmonic component is given by [2]:

$$\mathrm{HD_3} = \frac{1}{24}\left(\frac{V_p}{V_T}\right)^2 \tag{13.3a}$$

When emitter degeneration is applied (see Figure 13.4(a))

$$\mathrm{HD_3} = \frac{1}{24}\left[\frac{1-2(I_Q R/V_T)}{(1+(I_Q R/V_T))^4}\right]\left(\frac{V_p}{V_T}\right)^2 \tag{13.3b}$$

In both cases, V_p is the peak value of the incremental signal.

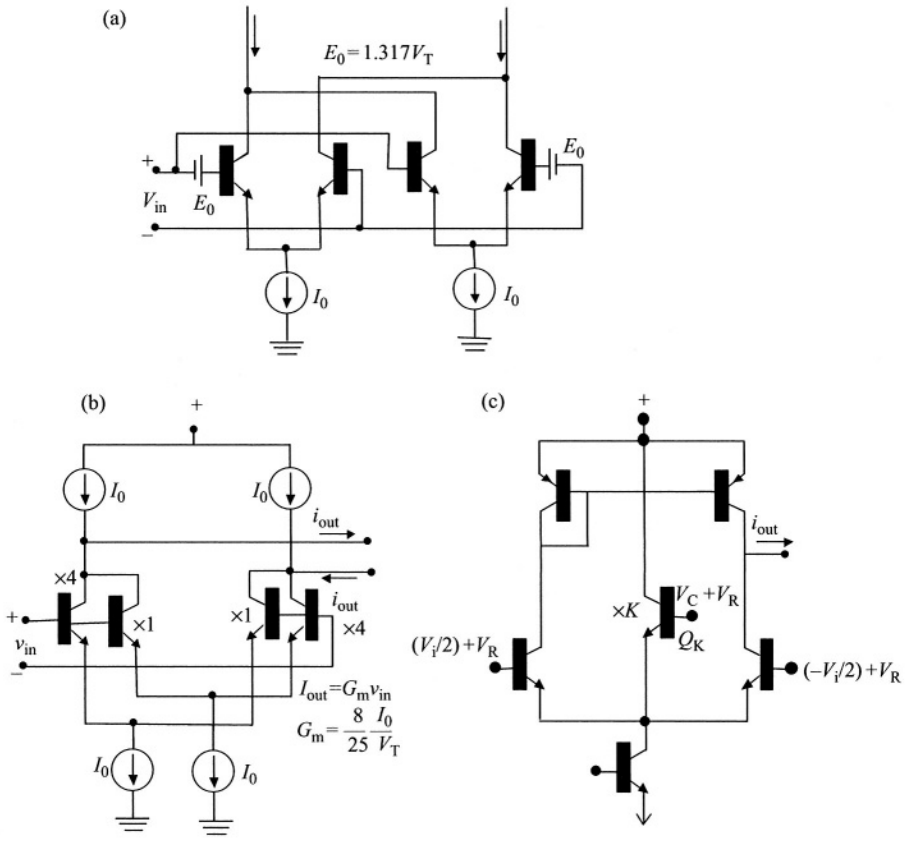


Figure 13.5. Indicative circuit techniques for obtaining a linear transconductor with increased dynamic range.

For example, if $I_Q R$ (the quiescent voltage drop across the degeneration resistor) is $4V_T$, then the expression in (13.3b) is ninety times smaller than that in (13.3a).

A second indicative linearization scheme involves the connection of two or more emitter coupled pairs in parallel. For the case of Figure 13.5(a), linearization takes place by means of a constant offset voltage E_0, and the linear input range becomes three times greater $(96\,\mathrm{mV_{(p-p)}})$ than that of a single differential pair $(32\,\mathrm{mV_{(p-p)}})$ for an output current THD of 1%. For the circuit in Figure 13.5(b), a similar increase in the linear input range is achieved by means of unequal-sized differential pairs when the area scaling ratio is 4 [3,4]. Another interesting linearization technique involves the realization of "triple-tail currents" comprised of three transistors driven by a

single-tail current (see Figure 13.5(c)) [5,6]. The optimum tuning voltage for the transconductance to be maximally flat at $V_i = 0$ is $K \exp(V_C/V_T) = 4$ with K, V_C denoting the emitter area scaling factor of Q_K and the tuning voltage, respectively. Clearly, if $K = 4$, then $V_C = 0$.

Linearization techniques of this kind are not needed for the case of filtering in the log-domain. Nevertheless, as it will become clear in the next section, the price paid for this is a significant increase in the mathematical burden associated with the articulation of systematic log-domain filter synthesis methods.

13.2. Synthesis and Design of Log-Domain Filters

1 The seed of the log-domain approach was presented in 1979 by Adams [7]. Adams' conceptual basic lowpass filter circuit is shown in Figure 13.6; it comprises two opamps, a few diodes and two current sources. Assuming that the I–V characteristic of a diode can be written $I_D = I_S \exp(V_D/V_T)$, where I_S is the reverse saturation current and V_T the thermal voltage, then from Figure 13.6 it can be deduced:

$$\begin{aligned} V_B(t) &= V_T \ln\left(\frac{I_{in}(t)}{I_S}\right) \\ i_{cap}(t) &= I_s \exp\left(\frac{V_{in}(t) - V_{cap}(t)}{V_T}\right) - I_d = C\dot{V}_{cap}(t) \\ I_{out}(t) &= I_0 \exp\left(\frac{V_{cap}(t)}{V_T}\right) \end{aligned} \tag{13.4}$$

Assuming the diodes have the same I_S and V_T, then equation (13.4) can be combined to give:

$$C\dot{V}_{cap} \exp\left(\frac{V_{cap}(t)}{V_T}\right) + I_d \exp\left(\frac{V_{cap}(t)}{V_T}\right) = I_{in}(t) \tag{13.5}$$

Since

$$\exp\left(\frac{V_{cap}(t)}{V_T}\right) = \frac{I_{out}(t)}{I_0} \Rightarrow \frac{\dot{V}_{cap}(t)}{V_T}\frac{I_{out}(t)}{I_0} = \frac{\dot{I}_{out}}{I_0} \tag{13.6}$$

then the nonlinear differential equation (13.5) can be written as (compare with (13.2c))

$$CV_T\dot{I}_{out} + I_d I_{out} = I_0 I_{in} \tag{13.7}$$

The application of the Laplace transform to (13.7) – *which is linear with constant coefficients* – reveals that the output current I_{out} is a first-order *linearly* filtered version of the input I_{in}, despite the fact that the *internal* currents are subject to the *nonlinear* exponential law dictated by the p–n junction physics. The

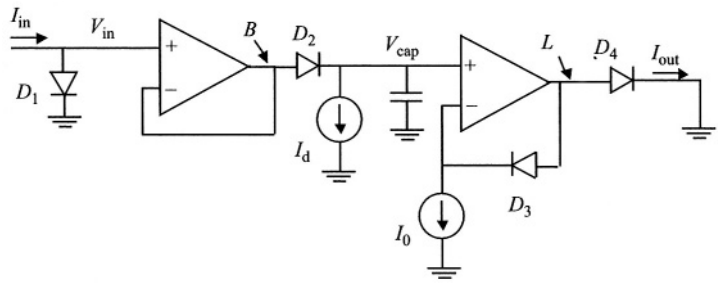


Figure 13.6. Adams' original design of a first-order log-domain filter.

above circuitry clearly indicates the feasibility of creating frequency shaping networks which exhibit a linear input–output relation while allowing the individual devices to operate in a nonlinear large signal (exponential) mode; thus, the internal signal processing becomes nonlinear. This approach had the benefit that voltage swings in the circuit are kept small, thus minimizing slew-rate limitations.

Although Adams's idea was attractive, the incorporation of the op-amps and use of discrete components rendered it fairly impractical in terms of power consumption, high-frequency operation and matching requirements for I_S and V_T. In 1990, Seevinck proposed the BJT-only integrator shown in Figure 13.7 [8]. This integrator was referred to as a "companding current-mode integrator", since the input current signals are compressed to logarithmic voltages, and the output currents stem from the exponential expansion of a pair of internal voltages. The circuit comprises two cross-coupled translinear loops, each incorporating one capacitor where the nonlinear integration takes place. The BJTs operate as large-signal exponential transconductors; a routine analysis confirms that the differential current-input/differential current-output relation corresponds to that of a linear integrator:

$$i_{out1} - i_{out2} = \frac{I_0}{C V_T} \int (i_{in1} - i_{in2})\, dt \tag{13.8}$$

again, assuming that I_S and V_T (for all devices) and the capacitors C are matched.

The exponential dependence of a BJT collector current on the base–emitter voltage difference allows for the conversion of *large* input currents to *logarithmically* compressed voltages. The internal signal processing is nonlinear and the output transistors finally convert the *compressed* voltage signals to *exponentially expanded* output currents. The circuit operation is based on the small differences of the interconnected base–emitter junctions (delta-V_{BE}s), with the compressed voltages being processed in a low-impedance environment. This

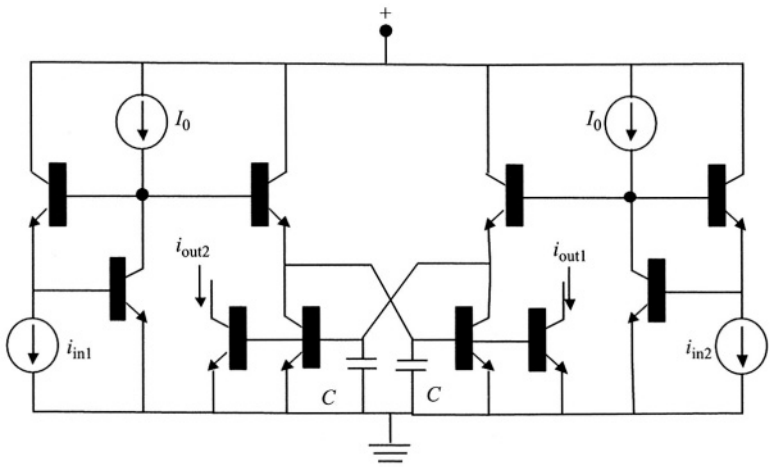


Figure 13.7. Seevinck's integrator.

is a benefit for high-speed operation, since the effect of parasitic capacitors charging and discharging is reduced. This integrator can be used as the basic building block of conventional continuous-time filter architectures. However, the compression/expansion is carried out by each constituent integrator, rather than just at the filter input and output [9,10].

2 It was Frey [11,12] who managed to tackle the problem of generalizing the concept of log-domain filtering introduced by Adams. Frey advanced the field: *he resorted to a state-space description of a linear input/output transfer function, and imposed a nonlinear mapping on the state-variables.* In this way, the internal signal processing becomes systematically nonlinear (with the internal node voltages being instantaneously and successively compressed and expanded, i.e. companded) but the input–output relation is bound to conform to the input/output linear relation guaranteed by the state-space infrastructure.

Suppose that the state-space description of the desired transfer function corresponding to a single-input single-output system is given by the following matrix equations [13]

$$\begin{aligned} \dot{\bar{X}} &= \overline{AX} + \bar{B}\,U \\ Y &= \overline{CX} + DU \end{aligned} \tag{13.9}$$

with U being the scalar input, Y being the scalar output and $\bar{X} = (x_1, x_2, \ldots, x_N)^T$ the state-variable vector. (The desired transfer function corresponds to $H(s) = \bar{C}\,(s\bar{I} - \bar{A})^{-1}\,\bar{B} + D$.) Now suppose that a nonlinear

mapping is imposed on the state-variables according to the scheme [13]:

$$x_i = f(V_i) \quad \text{with} \quad f'(V_i) \neq 0 \text{ for finite } V_i \tag{13.10}$$

By taking into consideration, the above generic mapping and its derivatives and appropriately substituting into (13.9), the following expressions are obtained ($V_0 = f^{-1}(U)$):

$$C_i \dot{V}_i = \sum_{j=1}^{N} C_i A_{ij} \frac{f(V_j)}{f'(V_i)} + C_i B_i \frac{f(V_0)}{f'(V_i)} \tag{13.11a}$$

$$Y = \sum_{j=1}^{N} C_{0j} \frac{f(V_j)}{f'(V_{N+1})} + D_0 \frac{f(V_0)}{f'(V_{N+1})} \tag{13.11b}$$

A_{ij} is the ij-th element of the state matrix $\bar{A}$, and C_{0j}, D_0 are scaling constants. An examination of the above equations reveals that they can be interpreted as nodal KCL equations, where V_i (or V_j) denotes the ith (internal) node voltage of the circuit. Then, the LHS of (13.11a) would correspond to the current flowing through a grounded capacitor connected at node i (it is implied that the dimensions of the quantities C_i is F(arad)). The RHS, which contains expressions of the form $f(V_j)/f'(V_i)$, could be implemented by means of special "transconductors" whose output current would be proportional to $f(V_j)/f'(V_i)$. Similar thoughts hold for (13.1 1b) as well.

The synthesis procedure outlined above is best clarified by means of a low-order synthesis example. Consider the following state-space description of a second-order lowpass filter on whose state-variables an exponential mapping is imposed:

$$\begin{aligned} \dot{x}_1 &= -\omega_0 x_2 + \omega_0 u \\ \dot{x}_2 &= -\frac{\omega_0}{Q} x_2 + \omega_0 x_1 \\ y &= x_2 \end{aligned} \tag{13.12}$$

and

$$\begin{aligned} x_1 &= I_0 \exp(aV_1) \\ x_2 &= I_0 \exp(aV_2) \\ a &= (2V_T)^{-1} \end{aligned} \tag{13.13}$$

Substitution of (13.13) into (13.12) yields after rearrangement ($I_0 = \omega_0 C/a$ and $u = I_0 \exp(a\, V_{\text{in}})$ [13]):

$$\begin{aligned} C\dot{V}_1 &= -I_0 \exp[a(V_2 - V_1)] + I_0 \exp[a(V_{\text{in}} - V_1)] \\ C\,\dot{V}_2 &= -\frac{I_0}{Q} + I_0 \exp[a(V_1 - V_2)] \\ y &= I_0 \exp(aV_2) \end{aligned} \tag{13.14}$$

The terms which are proportional to the exponentials of voltage differences can be implemented via the "exponential transconductors" shown in Figure 13.8. Terms corresponding to currents flowing into the integration node are implemented with the E+ Cell, whereas terms corresponding to currents sourced from the integration node are implemented via the E– Cell. The final log-domain topology which realizes the nonlinear KCL equations (13.14) is shown in Figure 13.9 ($u = I_{\text{in}}$, $y = I_{\text{out}}$).

If a different – other than pure exponential – mapping was chosen, then alternative nonlinear transconductors would be required to realize the same transfer function. If the mapping is exponentially related, for example $x_i \sim \sinh(aV_i)$ or $x_i \sim \tanh(aV_i)$, then a novel class of filters termed as exponential state-space (ESS) is generated [13].

The log-domain filters introduced by Frey have several attractive features since they

- consist of transistors and capacitors only and are thus suited for IC integration;

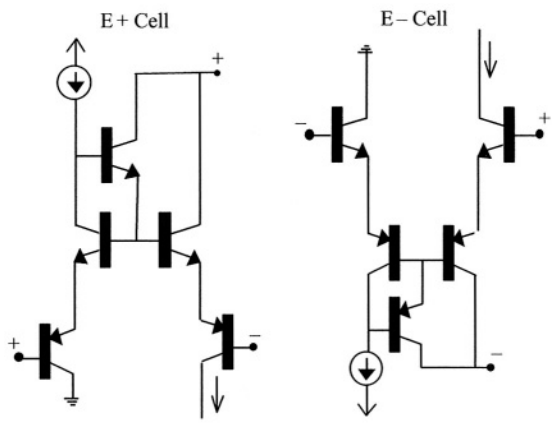


Figure 13.8. Frey's "exponential transconductors" [13].

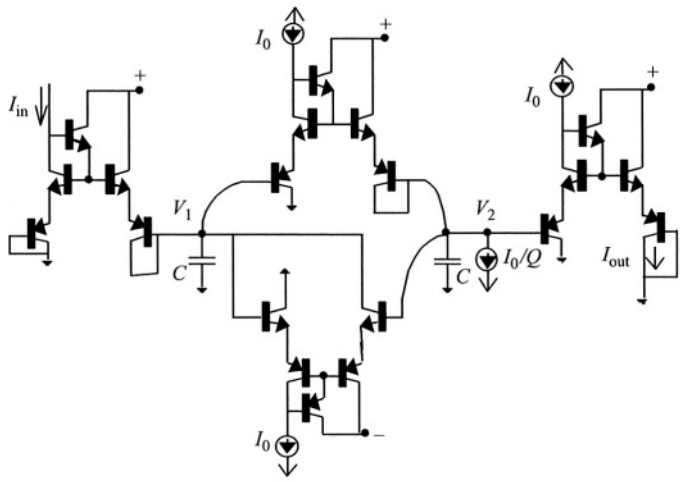


Figure 13.9. A second-order log-domain lowpass biquad designed according to Frey's state-space method.

- are not limited to small-signal operation, thus exhibiting wide dynamic range;
- are fully tuneable over a wide range by I_0;
- favor high-frequency operation due to simple structures and low-voltages swings;
- operate at fairly low power-supply levels.

However, Frey's design *method depends on the state-space mapping selection, and there are no rules for the optimal selection of the mapping coefficients when it comes to the synthesis of high-order filters; in* [14], *for example, it was set* $x_j = (I_S^2/I_0)\exp(aV_j)$ *with* I_S *denoting the reverse saturation current.* Furthermore, it is difficult for the designer both to express the desired transfer function in state-space form and to manipulate the large number of transformed state-space equations. *Additionally, the method does not seem to be easily reversed to allow the analysis of a given log-domain structure.* Thus, it would be fair to argue that although Frey's approach is ingenious, it provides flexibility and design freedom only to a well-experienced designer.

3 C. Perry and Roberts [15,16] attempted a more modular approach for the synthesis of high-order log-domain filters. Rather than a linear state space description, their starting point was the signal flow graph (SFG) representation of an LC ladder filter. LOG–EXP functions are inserted into the ladder in pairs to maintain overall linearity. Their method was based on the fact that *the internal log-domain signals are successively exponentiated, added, integrated*

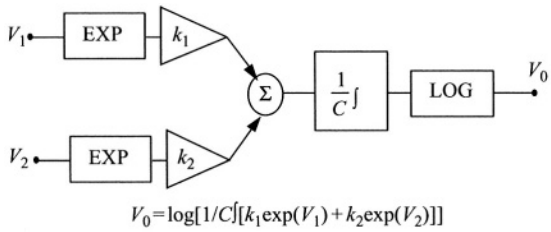


Figure 13.10. The succession of processing of log-domain signals [16].

and finally logged according to the scheme illustrated in Figure 13.10. The EXP and LOG functions (see Figure 13.10) can be realized via the E Cells of Figure 13.8. The SFG which corresponds to the desired transfer function can be transformed to log-domain, as long as the following set of rules is taken into consideration:

- place a LOG block after each integrator;
- place an EXP block at the input to each summer (before the multiplier);
- place an EXP block at the output of the system;
- place a LOG block at the input to the system.

Figure 13.11(a) shows the transformed SFG which corresponds to the design of a fifth-order Chebychev lowpass filter. The final circuit is shown in Figure 13.11(b).

This method, despite its modularity, is not as straightforward as it might first appear, particularly for higher order structures. In practice, the transformed SFG usually contains redundancies that have to be identified and be dealt with quite carefully [16]; once this has taken place, the designer has to further identify which of the combinations of EXP and LOG blocks are conveniently implemented by means of single E Cells. *This is not easy since some of the* EXP *or the* LOG *blocks might belong to the same* E *Cell.* In a situation like this, the designer's experience is of primary significance. Additionally, the method had to be re-expressed and an extended "super-set" of rules was elaborated [17]. As a general observation, it should be underlined that the task of finding a suitable SFG representation of the desired transfer function is equivalent to the task of finding an appropriate SS description, since both the SFG and the SS are described by a set of equivalent differential/integral equations. In fact, if the exponential mapping suggested by Frey is imposed on the SFG variables, that is, on the inductor currents and the capacitor voltages, then the final topology is revealed since terms implementable via E Cells can be identified.

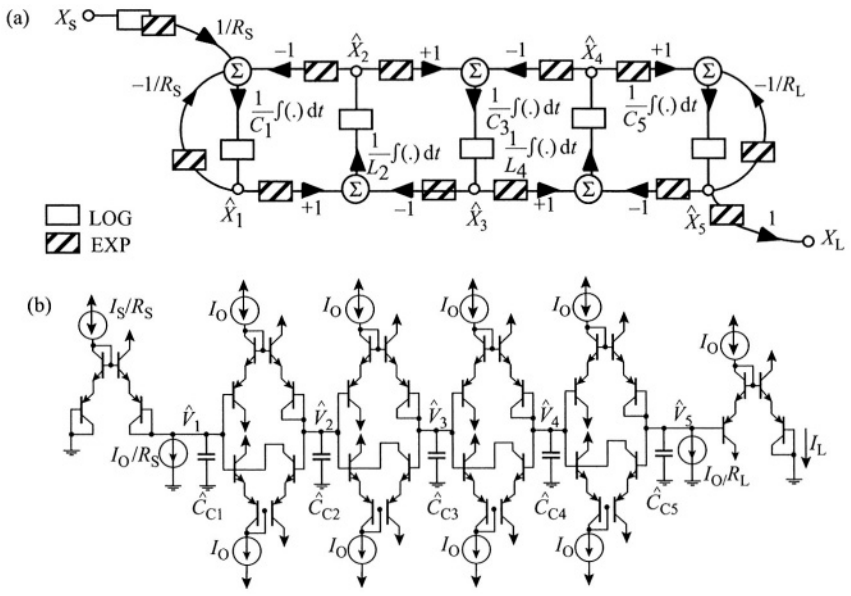


Figure 13.11. Perry–Roberts' log-domain SFG of a (a) doubly-terminated fifth-order Chebyschev lowpass filter and (b) its hardware implementation [16].

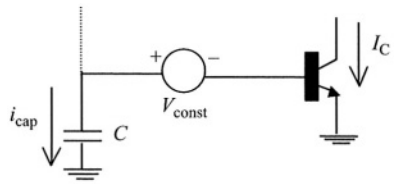


Figure 13.12. Subcircuit depicting the "Dynamic Translinear Principle".

4 Mulder, Serdijn et al. have classified log-domain filters – and ESS topologies in general – as "Dynamic Translinear Circuits" (DTL) governed by the "Dynamic Translinear Principle". These terms were introduced by Mulder, Serdijn et al. in a series of publications [18–21]. The subcircuit of Figure 13.12 illustrates the operational principle of DTL circuits; routine analysis reveals that

$$C V_T \dot{I}_C(t) = I_C(t)\, i_{cap} \tag{13.15}$$

Equation (13.15) states the DTL principle: "A time-derivative of a current is equivalent to a product of currents". Relations of the form (13.15) were used for the development of a current-mode analysis method of DTL circuits since they allow the expression of capacitor currents in terms of (collector)

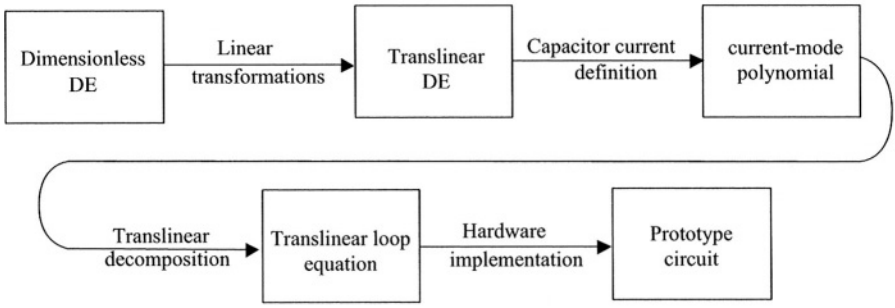


Figure 13.13. DTL circuit synthesis route [22].

currents internal to the (dynamic translinear) circuit. A method suitable for the synthesis of DTL circuits was also developed. The basic steps are shown in Figure 13.13:

The method is described in detail in [20–22]; it starts with a dimensionless DE which describes the desired behavior in the time-domain, and after the "time" and "signal" transformations, a translinear DE is provided. The "time" transformation has the form:

$$\frac{\mathrm{d}}{\mathrm{d}\tau} = \frac{CV_\mathrm{T}}{I_0}\frac{\mathrm{d}}{\mathrm{d}t} \tag{13.16}$$

with τ denoting the "dimensionless time" and I_0 an appropriate biasing current. The "signal" transformation has the form:

$$x_j = \frac{I_j}{I_k} \tag{13.17}$$

with x_j denoting a dimensionless "signal" present in the original dimensionless DE. I_j and I_k are currents physically present in the final circuit implementation. Commenting on the transformations (13.16) and (13.17), it should be noted that although the "time" transformation is justifiable logically, there are no explicitly articulated rules for the selection of the physical currents used for the transformation of the original "signals". Furthermore, there are no explicitly articulated rules for the definition of the capacitor currents in terms of physical currents present in the final circuit implementation; this step is crucial for the transition from the Translinear DE stage to the current-mode polynomial stage (see Figure 13.13). In [21], for example, the capacitor currents are defined in terms of additional intermediate (auxiliary) currents present in the final circuit implementation, whereas in [20] one capacitor current is defined in terms of another capacitor current.

The above remarks suggest that the synthesis method depicted in Figure 13.13 requires a remarkable degree of experience in order to be applied

successfully. However, the intended close resemblance of the DTL synthesis method with synthesis routes for the case of static TL circuits [23], is claimed to allow the application of the existing knowledge on static TL circuits directly to DTL circuits [22]. *(The field of static translinear circuits has been pioneered by B. Gilbert; the interested reader can find an excellent epitomy of translinear circuits in [24]. Gilbert first identified the significance of the translinear circuits and coined the term for the homonymous principle.)*

5. An alternative transistor-level synthesis (and analysis) path is based upon the realization that the collector current of a BJT whose emitter is connected to a linear grounded capacitor complies with the general nonlinear Bernoulli differential equation; the derivation of this differential equation stems directly from the fact that the BJT collector current depends exponentially upon the base–emitter voltage. Thus, the combination of a BJT and an emitter connected linear grounded capacitor (shaded area of Figure 13.1) is termed a Bernoulli Cell (BC).

The feature that characterizes Bernoulli's DE is that though it is nonlinear, it can always be represented in a linearized way. This fact suggests that the BC could be used as a building element for the realization of linear time-invariant "log-domain" filters. The dynamics of a cascade of appropriately interconnected BCs implement a system of coupled differential equations of the Bernoulli form which, when considered in their linearized form, give rise to a system of differential equations termed "Log-Domain State-Space" (LDSS) [25,26].

The LDSS constitutes a possible alternative theoretical framework for the study of log-domain circuits, because it can be considered as the starting point for both the systematic analysis and synthesis of log-domain filters (and circuits in general). It is believed that this alternative transistor-level approach sheds light on the class of log-domain circuits from a different perspective.

Figure 13.14 shows a possible cascade of appropriately interconnected simple (i.e. single base–emitter junction) BCs; such a cascade is characterized by the following set of LDSS relations:

$$C_1 V_T \dot{w}_1(t) + [u_1(t) - v_1(t)]\, w_1(t) = I_{in}(t) \tag{13.18a}$$

$$C_2 V_T\, \dot{w}_2(t) + [u_2(t) - v_2(t)]\, w_2(t) = w_1(t) \tag{13.18b}$$

$$C_3 V_T \dot{w}_3(t) + [u_3(t) - v_3(t)]\, w_3(t) = w_2(t) \tag{13.18c}$$

$$\vdots$$

$$C_m V_T \dot{w}_m(t) + [u_m(t) - v_m(t)]\, w_m(t) = w_{m-1}(t) \tag{13.18d}$$

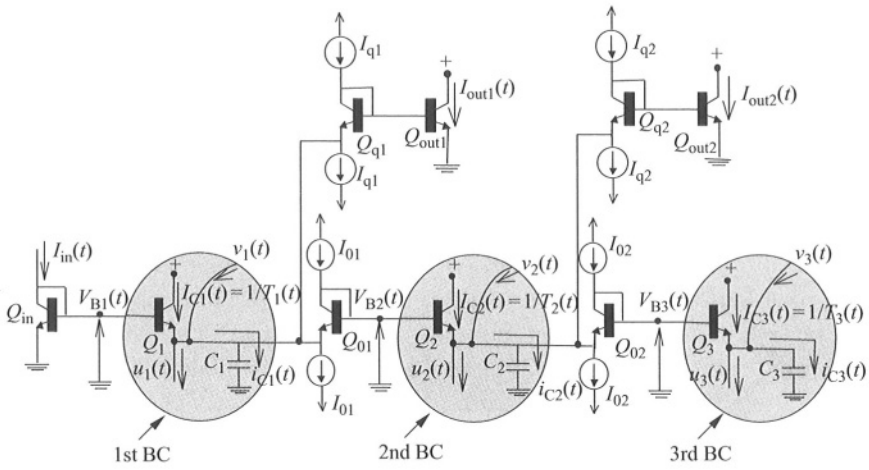


Figure 13.14. Interconnection of simple BCs.

with

$$w_1(t) = T_1(t) I_{\text{in}}(t) \tag{13.19a}$$

$$w_2(t) = T_2(t) T_1(t) I_{\text{in}}(t) = T_2(t)\, w_1(t) \tag{13.19b}$$

$$w_3(t) = T_3(t) T_2(t) T_1(t) I_{\text{in}}(t) = T_3(t)\, w_2(t) \tag{13.19c}$$

$$\vdots \tag{13.19d}$$

$$w_m(t) = T_m(t) w_{m-1}(t) \tag{13.19e}$$

a set *of new w-variables* for which, in addition to (13.19a–e) it also holds (λ_j is a positive constant of appropriate dimensions):

$$w_j(t) = \lambda_j \exp\left(\frac{V_{\text{cap}}\, j}{V_{\text{T}}}\right) \tag{13.20}$$

The quantity $1/T_j(t)$ equals the jth BC collector current, that is,

$$I_j(t) = \frac{1}{T_j(t)} \tag{13.21}$$

The TL loops $Q_{in}Q_1Q_{q1}Q_{out1}$, $Q_{in}Q_1Q_{01}Q_2Q_{q2}Q_{out2}$, etc., dictate the following current product equalities:

$$I_{in}(t)\, I_{q1} = \frac{1}{T_1(t)}\, I_{out1}(t) \tag{13.22a}$$

$$I_{in}(t)\, I_{01}\, I_{q2} = \frac{1}{T_1(t)}\,\frac{1}{T_2(t)}\, I_{out2}(t) \tag{13.22b}$$

$$I_{in}(t)\, I_{01}\, I_{02}\, I_{q3} = \frac{1}{T_1(t)}\,\frac{1}{T_2(t)}\,\frac{1}{T_3(t)}\, I_{out3}(t) \tag{13.22c}$$

$$\vdots$$

$$I_{in}(t)\, I_{01}\, I_{02} \ldots I_{0\,m-1}\, I_{qm} = \frac{1}{T_1(t)}\,\frac{1}{T_2(t)}\,\frac{1}{T_3(t)} \cdots \frac{1}{T_m(t)}\, I_{outm}(t) \tag{13.22d}$$

Equations (13.22a–d) can be rewritten equivalently (substituting for the w variables (recall (13.19a–e):

$$I_{out1}(t) = I_{q1}\, w_1(t) \tag{13.23a}$$

$$I_{out2}(t) = I_{01} I_{q2}\, w_2(t) \tag{13.23b}$$

$$I_{out3}(t) = I_{01} I_{02} I_{q3}\, w_3(t) \tag{13.23c}$$

$$\vdots$$

$$I_{outm}(t) = I_{01} I_{02} \ldots I_{0\,m-1} I_{qm}\, w_m(t) \tag{13.23d}$$

Hence, the output currents $I_{out\,j}(t)$ "sense" the $w_j(t)$ variables respectively. A cascade of compound (i.e. formed by two or more base–emitter junctions BCs) is characterized by a similar, *though not identical,* set of LDSS relations.

The exploitation of LDSS as a starting point for the synthesis of a particular linear and time-invariant system is straightforward once its respective state-space representation or SFG are known. The synthesis procedure is based on the direct comparison of the required dynamics of the original prototype system with those codified by the LDSS equations; the scope of this comparison is to identify the necessary time-domain relations that the products $[u_j(t) - v_j(t)]\, w_j(t)$ should comply with, so that the LDSS dynamics become identical to the desired ones. For the case of LTI systems described by a set of first-order linear DEs with constant coefficients, this comparison procedure usually results in the realization that product terms $[u_j(t) - v_j(t)]\, w_j(t)$ present in the set of LDSS equations should satisfy time-domain relations of the form

$$[u_j(t) - v_j(t)]\, w_j(t) = \pm p_j w_j \pm p_k w_k \pm p_l w_l \pm \cdots \tag{13.24}$$

with $j \neq k \neq l$ and p_j, p_k, p_l constant in time quantities. When every product of the form $[u_j(t) - v_j(t)]\, w_j(t)$ becomes an appropriate linear (time-invariant) combination of the w variables – as indicated by (13.24) – then the generally linear and time-varying LDSS equations reduce to a set of simple linear DEs with constant in time coefficients, which realize the desired LTI prototype system dynamics. At the circuit level, relations of the form (13.24) usually correspond to the addition of constant in time current sources at the respective jth BC capacitor node and/or the formation of complete TL loops interrelating the w variables; these constant currents and TL loops provide the u and v current s necessary for the implementation of the required dynamics.

As a quick example, let us consider the synthesis of a lowpass biquad. A possible state-space representation of a lowpass biquad is as follows:

$$\dot{x}_1(t) + \omega_0 x_2(t) = U(t) \tag{13.25a}$$

$$\dot{x}_2(t) + \left(\frac{\omega_0}{Q}\right) x_2(t) = \omega_0 x_1(t) \tag{13.25b}$$

$$y(t) = k\,\omega_0\, x_2(t) \tag{13.25c}$$

Since a second-order system is to be realized, two LDSS state equations are considered:

$$C_1 V_T \dot{w}_1(t) + [u_1(t) - v_1(t)] w_1(t) = I_{in}(t) \tag{13.26a}$$

$$C_2 V_T \dot{w}_2(t) + [u_2(t) - v_2(t)] w_2(t) = w_1(t) \tag{13.26b}$$

In order for the above LDSS equations to implement the required dynamics, a direct comparison is necessary. In (13.25a) the second term is proportional to the second state-variable $x_2(t)$, thus in (13.26a) the second term must be proportional to the second state-variable $w_2(t)$, that is,

$$u_1(t) w_1(t) \propto w_2(t) \quad \Rightarrow \quad u_1(t)\,\frac{1}{T_2(t)} = \text{constant} = \mu_1 \tag{13.27a}$$

$$v_1(t) = 0 \tag{13.27b}$$

Similarly, comparing (13.25b) and (13.26b):

$$u_2(t)\, w_2(t) \propto w_2(t) \quad \Rightarrow \quad u_2(t) = \text{constant} = \mu_2 \tag{13.27c}$$

$$v_2(t) = 0 \tag{13.27d}$$

The general LDSS equations (13.26a and b) thus become:

$$C_1 V_T \dot{w}_1(t) + \mu_1 w_1(t) = I_{in}(t) \tag{13.28a}$$

$$C_2 V_T \dot{w}_2(t) + \mu_2 w_2(t) = w_1(t) \tag{13.28b}$$

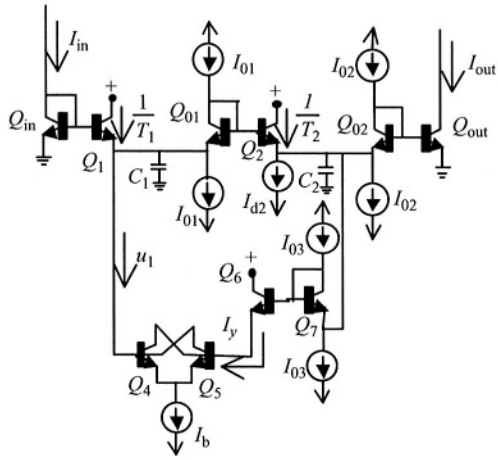


Figure 13.15. A log-domain lowpass biquad.

The above equations realize the required dynamics (13.25a–c) when in addition to (13.27a–d) it also holds:

$$I_{out}(t) = I_{01} I_{q2} w_2(t) \tag{13.28c}$$

[compare with (13.25c)].

The necessary time-domain relation (13.27a) corresponds to a product of currents and can be fulfilled by the formation of an auxiliary TL loop; (13.27c) is met by simply adding a constant current source I_{d2} at the emitter of the second BC BJT. The final topology is shown in Figure 13.15.

Applying the TLP along the complete TL loop $Q_2 Q_{01} Q_4 Q_5 Q_6 Q_7$ yields:

$$u_1(t) \frac{1}{T_2(t)} = I_{01} I_{03} = \mu_1 \tag{13.28d}$$

and (13.27a) is met. The insertion of the constant current source

$$u_2(t) = I_{d2} = \mu_2 \tag{13.28e}$$

fulfills (13.27c). The TL loop $Q_{in} Q_1 Q_{01} Q_2 Q_{02} Q_{out}$ yields:

$$\begin{aligned} I_{in}(t) I_{01} I_{02} &= \frac{1}{T_1(t)} \frac{1}{T_2(t)} I_{out}(t) \\ \Rightarrow I_{out}(t) &= I_{01} I_{02} [T_2(t) T_1(t) I_{in}(t)] \\ &= I_{01} I_{02} w_2(t) \end{aligned} \tag{13.28f}$$

and (13.27c) is also met (in this case $I_{q2} = I_{02}$).

Incorporating (13.28a and b) in the LDSS equations:

$$C_1 V_T \dot{w}_1(t) + I_{01} I_{03} w_2(t) = I_{in}(t) \quad (13.29a)$$

$$C_2 V_T \dot{w}_2(t) + I_{d2} w_2(t) = w_1(t) \quad (13.29b)$$

Applying the Laplace Transform to (13.29a and b), solving for $W_2(s)$ and substituting in (13.28c) finally yields the following lowpass biquadratic transfer function:

$$\frac{I_{out}(s)}{I_{in}(s)} = \frac{I_{01} I_{02} / C_1 C_2 V_T^2}{s^2 + (I_{d2} / C_2 V_T) s + I_{01} I_{03} / C_1 C_2 V_T^2} \quad (13.30)$$

The LDSS can be applied for the systematic synthesis of high-order transfer-functions [27,28] and the systematic analysis of log-domain structures or other topologies where BCs can be identified [29]. Furthermore, the identification of the BC-based dynamics seems to extend the potential of the log-domain technique to the systematic synthesis of nonlinear networks (e.g. the electronic representation of the memristive Hodgkin–Huxley nerve-axon dynamics, [29–32]). However, the BC-based LDSS relations can be exploited as a synthesis tool for the realization of log-domain topologies; they cannot lead to the implementation of more general ESS structures.

From the several log-domain filter synthesis routes presented in this section, it should be clear that when compared with more conventional approaches (e.g. g_m-C), the log-domain technique shifts considerably the design effort from the building-block level (e.g. realization of linear transconductor) to system level (e.g. realization of input–output linear though internally nonlinear frequency shaping network). *The articulation of systematic synthesis paths in log-domain is associated with a considerable unavoidable increase of mathematical burden originating from the fact that the circuits are not restricted to small-signal operation since the active devices are allowed to operate in accordance to their exponential (large-signal) characteristic.*

13.3. Impact of BJT Non-Idealities upon Log-Domain Transfer Functions: The Lowpass Biquad Example

Approximate, though modular, methods for evaluating the effect of certain primary process-dependent transistor non-idealities upon transfer functions implemented by means of the log-domain technique are possible. For example, considering a log-domain filter topology as an interconnection of Frey's E± Cells, the effect of the combined BJT non-idealities upon a certain transfer function can be found by deriving the circuit's operational equations using modified expressions for the E+ and the E– Cells. These expressions incorporate the effect of the BJT non-idealities on the response of the E± Cells [33].

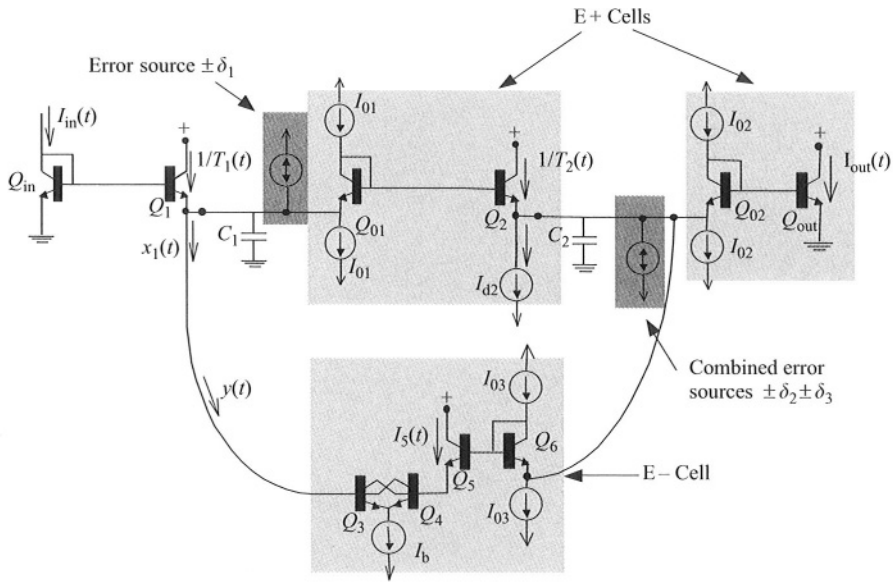


Figure 13.16. A log-domain lowpass biquad.

Let the lowpass log-domain biquad of Figure 13.16 be considered. Appropriately interconnected npn-only E± Cells produce the desired frequency shaping response. Table 13.1 shows the effect of the parasitic emitter resistance r_E, the parasitic base resistance r_B and finite beta upon the ideal operation of the E± Cells whereas Table 13.2 provides the respective modified second-order lowpass transfer functions. These transfer functions can be derived from a transistor-level manipulation of the modified set of state-space relations when the non-ideal operation of the E± Cells is taken into consideration. From Table 13.2 it is clear that the parasitic voltage drops, associated with the existence of r_E, r_B and the beta current, manifest their impact by altering the effective V_T value; the combined effect of r_E, r_B and β stems from the ideal transfer function shown in row 1 of Table 13.2 when the thermal voltage V_T is substituted by $V_T + I_0\,(r_E + r_B/\beta)$.

(It is worth mentioning that the modified transfer functions related to the parasitic role of r_E, r_B and β could be derived directly from the ideal transfer function shown in row 1 of the Table 13.2, once it is realized that (for $I_d = I_{01} = I_{02} = I_{03} = I_0$) the quantity I_0/V_T denotes the ideal *small-signal* transconductance g_{mi} whose effective value is reduced to $g_{meff} = g_{mi}/[1 + (g_{mi}r_E + g_{mi}r_B/\beta)]$ when the parasitic resistances are taken into consideration.)

The fourth row of Table 13.2 shows the effect of component mismatches upon the same transfer function. Emitter area variations (photolithographic

Table 13.1. Effect of r_B, r_E upon E± Cells.

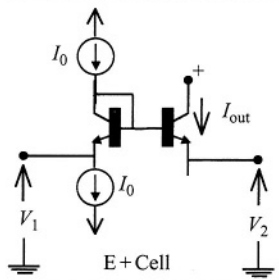
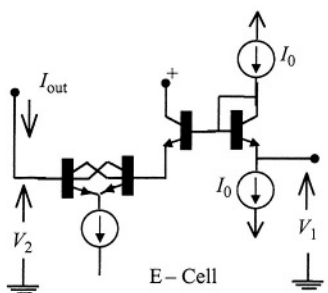
	Ideal behavior	*Effect of* r_E	*Effect of* r_B
	$I_{out} = I_0 \exp\left(\frac{V_1 - V_2}{V_T}\right)$	$I_{out} = I_0 \exp\left(\frac{V_1 - V_2}{V_T + I_0 r_E}\right)$	$I_{out} = I_0 \exp\left(\frac{V_1 - V_2}{V_T + (I_0/\beta) r_B}\right)$
	$I_{out} = I_0 \exp\left(\frac{V_1 - V_2}{V_T}\right)$	$I_{out} = I_0 \exp\left(\frac{V_1 - V_2}{V_T + I_0 r_E}\right)$	$I_{out} = I_0 \exp\left(\frac{V_1 - V_2}{V_T + (I_0/\beta) r_B}\right)$

Table 13.2. Effect of several BJT non-idealities upon a second-order lowpass TF.

	Transfer function
Ideal	$\frac{I_{out}(s)}{I_{in}(s)} = \frac{\frac{I_{01}I_{02}}{C_1C_2V_T^2}}{s^2+\left(\frac{I_d}{C_2V_T}\right)s+\frac{I_{01}I_{03}}{C_1C_2V_T^2}}$
Effect of r_E ($I_{01} = I_{02} = I_{03} = I_d = I_0$)	$\frac{I_{out}(s)}{I_{in}(s)} = \frac{\frac{I_0^2}{C_1C_2[V_T+I_0r_E]^2}}{s^2+\left(\frac{I_0}{C_2[V_T+I_0r_E]}\right)s+\frac{I_0^2}{C_1C_2[V_T+I_0r_E]^2}}$
Effect of r_B, β ($I_{01} = I_{02} = I_{03} = I_d = I_0$)	$\frac{I_{out}(s)}{I_{in}(s)} = \frac{\frac{I_0^2}{C_1C_2[V_T+\frac{I_0}{\beta}r_B]^2}}{s^2+\left(\frac{I_0}{C_2[V_T+\frac{I_0}{\beta}r_B]}\right)s+\frac{I_0^2}{C_1C_2[V_T+\frac{I_0}{\beta}r_B]^2}}$
Effect of component mismatches	$\frac{I_{out}(s)}{I_{in}(s)} = \frac{k_2\frac{I_{01}I_{02}}{C_1C_2V_T^2}}{s^2+\left(\frac{I_d}{C_2V_T}\right)s+k_1\frac{I_{01}I_{03}}{C_1C_2V_T^2}}$ $k_1 = \frac{I_{S_4}I_{S_5}I_{S_2}}{I_{S_3}I_{S_{01}}I_{S_6}}$ $k_2 = \frac{I_{S_1}I_{S_2}I_{S_{out}}}{I_{S_{in}}I_{S_{01}}I_{S_{02}}}$
Effect of current source mismatches	$\frac{I_{out}(s)}{I_{in}(s)} = \frac{\frac{I_{01}I_{02}}{C_1C_2V_T^2}}{s^2+\left(\frac{I_d\pm\delta_2\pm\delta_3}{C_2V_T}+\frac{\pm\delta_1}{C_1V_T}\right)s+\frac{I_{01}I_{03}\pm\delta_1(I_d\pm\delta_2\pm\delta_3)}{C_1C_2V_T^2}}$

delineation errors) and integrated base charge variations (process variations) lead, in general, to I_S variations. This type of non-ideality affects the operation of the translinear loops within the circuit. Referring again to the lowpass biquad in Figure 13.16, the application of the translinear principle along the loops $Q_{01}Q_3Q_4Q_5Q_6Q_2$ and $Q_{in}Q_1Q_{01}Q_2Q_{02}Q_{out}$ yields respectively (the BC-based LDSS is used):

$$x_1(t)w_1(t) = k_1 I_{01} I_{03} w_2(t) \tag{13.31a}$$

$$I_{out}(t) = k_2 I_{01} I_{02} w_2(t) \tag{13.31b}$$

with

$$k_1 = \frac{I_{S_4} I_{S_5} I_{S_2}}{I_{S_3} I_{S_6} I_{S_{01}}} \tag{13.31c}$$

and

$$k_2 = \frac{I_{S_1} I_{S_2} I_{S_{out}}}{I_{S_{in}} I_{S_{01}} I_{S_{02}}} \tag{13.31d}$$

By incorporating the above modified equations into the LDSS relations describing the dynamics of the biquad, a routine analysis reveals the modified transfer function shown in the fourth row of Table 13.2.

Mismatches of the current sources used for biasing of the diode connected BJTs can be modeled by inserting small, constant in-time current sources at the respective node (see Figure 13.16) whose magnitude equals the "error" δ. A transistor-level analysis reveals that this kind of error modifies the LDSS expressions for the lowpass biquad:

$$C_1 V_T \dot{w}_1(t) + [x_1(t) \pm \delta_1] w_1(t) = I_{in}(t) \tag{13.32a}$$

$$C_2 V_T \dot{w}_2(t) + [I_d \pm \delta_2 \pm \delta_3] w_2(t) = w_1(t) \tag{13.32b}$$

The last row of Table 13.2 shows the transfer function for this case resulting via routine calculations when the remaining translinear relations are taken into consideration.

The finite current gain β, apart from modifying the transfer function when combined with the finite parasitic resistance r_B, also limits the low frequency (dc) gain that can be achieved by a specific log-domain topology. This kind of impact is best illustrated by means of the following example. The simple lowpass biquad of Figure 13.17 is characterized by the ideal transfer function

$$\frac{I_{out}(s)}{I_{in}(s)} = \frac{I_{01} I_{02} / C_1 C_2 V_T^2}{s^2 + [I_{d1}/C_1 V_T + I_{d2}/C_2 V_T] s + I_{d1} I_{d2} / C_1 C_2 V_T^2}$$

Resorting to a small-signal and low-frequency analysis of the specific topology, it can be derived that the current gain $i_{out}(t)/i_{in}(t)$ equals (when $\beta \gg 1$,

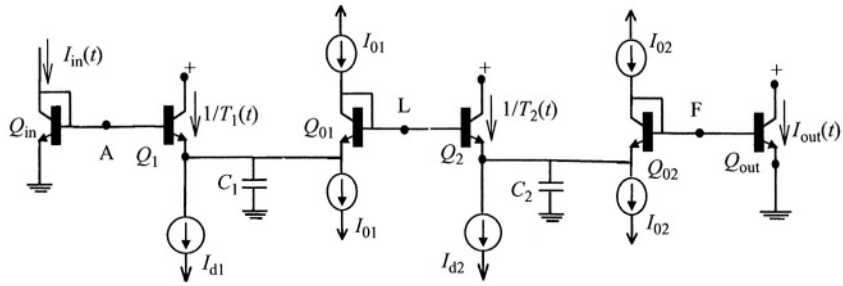


Figure 13.17. A simple log-domain lowpass biquad.

$I_{01} = I_{02} = I_0 = g_{m0} V_T$ and $I_{d1} = I_{d2} = I_d = g_m V_T$):

$$\frac{i_{out}(t)}{i_{in}(t)} = \frac{g_{m_{out}}}{g_{m_{in}}} \frac{\beta_{out}/g_{m_{out}}}{1/g_m + 1/g_{m0} + \beta_{out}/g_{m_{out}}} \tag{13.33a}$$

When high dc gain values are desired, $I_0 \gg I_d \Rightarrow 1/g_{m0} \ll 1/g_m$ and (13.33a) reduces to the following relation (the translinear relation $g_{m_{in}} g_{m0}^2 = g_m^2 g_{m_{out}}$ is also taken into account):

$$\frac{i_{out}(t)}{i_{in}(t)} = \frac{(g_{m0}/g_m)^2}{1 + \left((g_{m0}/g_m)^2 (g_{m_{in}}/g_m)\right)/\beta_{out}} = \frac{(I_0/I_d)^2}{1 + \left((I_0/I_d)^2 (D/I_d)\right)/\beta_{out}}$$

$$= \frac{K_{dc,ideal}}{1 + \left(K_{dc,ideal}(D/I_d)\right)/\beta_{out}} = K_{dc} \tag{13.33b}$$

When the dc component D of the input current equals the damping current(s) I_d, then (13.33b) can be further simplified to:

$$\frac{i_{out}(t)}{i_{in}(t)} = \frac{\beta_{out} K_{dc,ideal}}{\beta_{out} + K_{dc,ideal}} = K_{dc} \tag{13.33c}$$

From (13.33c), it can be deduced that a very high dc gain $K_{dc,ideal}$ is prohibited by the output BJT finite beta.

This section has outlined the particular ways in which the most important transistor non-idealities affect a lowpass log-domain biquadratic response. A direct observation of Table 13.2 shows that in most cases both ω_0 and Q values of the ideal transfer function are modified as a result of the presence of the various transistor non-idealities. Evidently, the higher the order of the response, the more complex the way in which the transistor non-idealities affect the location of the poles and the zeros on the s-plane. However, this kind of low-level treatment of low-order topologies eases the designer's insight as far as deviations from ideality are concerned.

13.4. Floating Capacitor-Based Realization of Finite Transmission Zeros in Log-Domain: The Impact upon Linearity

Class A single-ended log-domain filters which simulate the operation of passive ladder prototypes have been proposed. According to [16] the realization of log-domain topologies which simulate the operation of passive LC ladders with finite transmission zeros is feasible by implementing the corresponding all-pole ladder dynamics, and then adding a floating capacitor of appropriate value C_{par} between the appropriate capacitor nodes. Figure 13.18 shows a passive ladder prototype implementing an elliptic response whereas Figure 13.19 illustrates a floating-capacitor npn-only log-domain structure which simulates the dynamics of the prototype; the floating capacitor C_{par} is connected between the capacitors C_1 and C_3. (It would be useful to observe that the absence of the floating capacitor leads to a third-order all-pole response.)

In the following section, we explain why the presence of the floating capacitor does not accurately simulate the required ladder dynamics. The LDSS relations will constitute our analysis tool.

The current through the floating capacitor is given by

$$x_1'(t) = v_3(t) = C_{par}(\dot{\hat{V}}_1 - \dot{\hat{V}}_3) \tag{13.34}$$

with $\hat{V}_1$, $\hat{V}_3$ the C_1, C_3 capacitor node voltages, respectively.

Recalling that

$$w_1(t) = \mu_1 \exp\left[\frac{\hat{V}_1(t)}{V_T}\right] \tag{13.35a}$$

$$w_3(t) = \mu_3 \exp\left[\frac{\hat{V}_3(t)}{V_T}\right] \tag{13.35b}$$

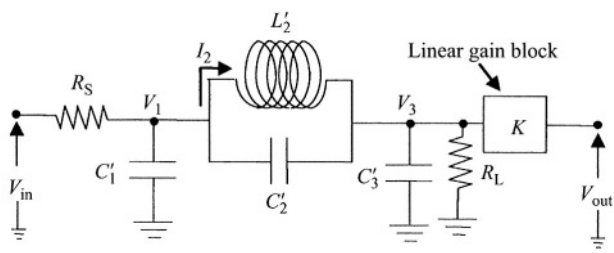


Figure 13.18. A passive LC ladder corresponding to an elliptic response.

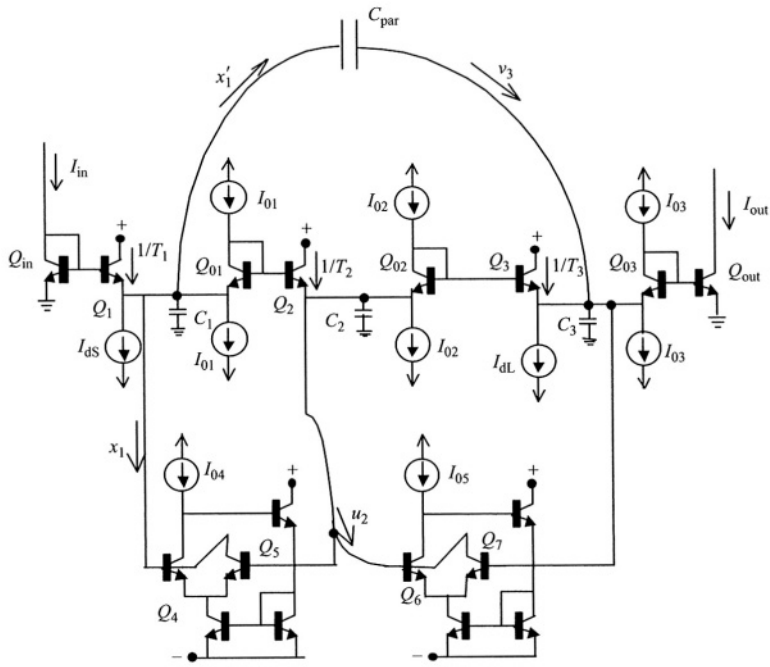


Figure 13.19. Floating capacitor elliptic response.

yields from (13.34):

$$x_1'(t) = v_3(t) = C_{par} V_T \left[\frac{\dot{w}_1(t)}{w_1(t)} - \frac{\dot{w}_3(t)}{w_3(t)} \right] \tag{13.36}$$

Incorporating (13.36) in the LDSS relations corresponding to the operation of the log-domain topology in Figure 13.19 yields:

$$C_1 V_T \dot{w}_1(t) + I_{dS} w_1(t) + I_{01} I_{04} w_2(t) + C_{par} V_T \dot{w}_1(t) - C_{par} V_T \left(\frac{w_1(t)}{w_3(t)} \right) \dot{w}_3(t) = I_{in}(t) \tag{13.37a}$$

$$C_2 V_T \dot{w}_2(t) + I_{02} I_{05} w_3(t) = w_1(t) \tag{13.37b}$$

$$C_3 V_T \dot{w}_3(t) + I_{dL} w_3(t) + C_{par} V_T \dot{w}_3(t) - C_{par} V_T \left(\frac{w_3(t)}{w_1(t)} \right) \dot{w}_1(t) = w_2(t) \tag{13.37c}$$

$$I_{out}(t) = I_{01} I_{02} I_{03} w_3(t) \tag{13.37d}$$

Clearly the above dynamical equations do not correspond to a linear time-invariant system; due to the presence of the terms $C_{par} V_T (\dot{w}_3(t)/w_3(t))\, w_1(t)$ and $C_{par} V_T (\dot{w}_1(t)/w_1(t))\, w_3(t)$ in (13.37a) and (13.37c) respectively, not all the DEs of the system are characterized by constant in-time coefficients. Thus, the topology of Figure 13.19 is inaccurate as far as the operational simulation of the desired dynamics is concerned, despite the fact that an ac analysis would confirm realization of the desired small-signal transfer function (in this case elliptic).

In contrast to the above approach, the exact realization of finite transmission zeros can be achieved by means of log-domain integrators [34–36]. Returning to Figure 13.19, a direct comparison of the general LDSS equations with the required ladder prototype elliptic dynamics reveals that in addition to the necessary conditions which realize the all-pole ladder dynamics, it is not a floating capacitor that is needed but two more currents which are fed into the capacitors C_1 and C_3; these currents have the form

$$v_1(t) \propto \frac{\dot{w}_3(t)}{w_1(t)} \tag{13.38a}$$

$$v_3(t) \propto \frac{\dot{w}_1(t)}{w_3(t)} \tag{13.38b}$$

with v_1 fed into the capacitor C_1 and v_3 fed into the capacitor C_3. The realization of these currents would lead to the exact operational simulation of the desired dynamics. One non-canonical way – *though not the only one* – of realizing these specific currents was provided in [37]. When both log-domain circuits – that is, the one with the floating capacitor and the one with the appropriate currents present – were simulated, it was verified that the floating capacitor topology was characterized by higher distortion levels.

Figure 13.20 illustrates a considerable improvement as far as the THD linearity levels (obtained by means of large-signal transients) of lowpass elliptic responses are concerned, when floating capacitors are not used. The results of Figure 13.20 correspond to two different specifications (namely cutoff frequency 1 MHz, passband ripple 0.18 dB and stopband rejection of 12 (plot (a)) or 19dBs (plot (b)). Each specification was realized both by floating capacitors and in an exact way. Figure 13.19 shows how the input tone modulation index m (defined as the peak of the input tone over the dc level present at the input) affects the distortion levels of single tones situated close to the passband edge. The linearity improvement, when floating capacitors are not used, is pronounced for low and medium level modulation indices m. The improved linearity performance should be attributed to the fact that the distorting terms present in (13.37a and c) vanish when the elliptic dynamics are implemented in an exact way. Conversely, the THD results shown in Figure 13.20 could be

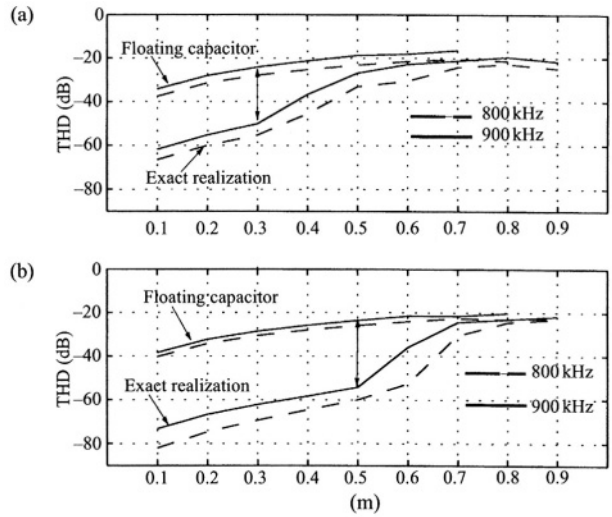


Figure 13.20. Passband edge distortion levels for elliptic responses implemented with and without floating capacitors.

interpreted as offering a comparative evaluation of the impact of the undesired terms upon the output linearity. Hence, though the use of floating capacitor structures exhibit a *small-signal* response close to the theoretically predicted one [16], the linearity price paid is considerable.

13.5. Effect of Modulation Index upon Internal Log-Domain Current Bandwidth

Log-domain filters are large-signal circuits in the sense that the active devices are allowed to operate in accordance with their large-signal exponential I–V characteristic. As mentioned in Section 13.1, the input stage of a log-domain structure consists of a logarithmic I-to-V compressor (usually a diode-connected transistor). The output stage of a log-domain filter is composed of an exponential V-to-I expander (usually a single transistor) which restores the signal dynamic range at the output. The main body of the filter, situated between the input and the output stages, processes logarithmically compressed voltages in such a way that the overall input–output linearity behavior is preserved. Given the above facts, it is easy to understand that the currents internal to a log-domain topology will exhibit a strongly nonlinear behavior, despite the fact that the output will be a shifted and scaled version of the input sinusoid. *In other words, currents internal to a logdomain filter are nonlinear by design, intentionally.*

This section deals briefly with the nonlinear character of transistor currents internal to an input–output linear log-domain filter structure. Consider for example the log-domain biquad of Figure 13.15. It can be shown [29] that the collector currents of the first and second BC are given respectively by the following relations (when every dc biasing current (including the input dc level) involved equals I_0, and the capacitors have a common value C):

$$I_{C_1}(t) = \frac{1}{T_1(t)} = \frac{D\,[1 + m\sin(\omega t)]}{[1 + m\,P_x\,\sin(\omega t + \varphi_1)]} \tag{13.39a}$$

$$I_{C_2}(t) = \frac{1}{T_2(t)} = D\,\frac{[1 + mP_x\sin(\omega t + \varphi_1)]}{[1 + mR_x\sin(\omega t + \varphi_2)]} \tag{13.39b}$$

with

$$P_x = \frac{\sqrt{1 + x^6}}{(1 - x^2)^2 + x^2} \tag{13.40a}$$

$$R_x = \frac{1}{\sqrt{(1 - x^2)^2 + x^2}} \tag{13.40b}$$

$$\tan(\varphi_1) = -\left(\frac{\omega}{\omega_0}\right)^3 = -x^3 \tag{13.41a}$$

$$\tan(\varphi_2) = -\frac{\omega_0\,\omega}{{\omega_0}^2 - \omega^2} = -\frac{x}{1 - x^2} \tag{13.41b}$$

and

$$x = \frac{\omega}{\omega_0} \tag{13.41c}$$

The quantity $x = \omega/\omega_0$ depends on both the input tone frequency ω and the pole frequency $\omega_0 = I_0/CV_T$. The input signal modulation index is denoted again by m. The closed-form expressions for the collector currents have been derived exploiting the LDSS relations. The strongly nonlinear character of the two collector currents in question is fairly evident given the fact that they are expressed as the ratio of two sinusoids. Figure 13.22(a)–(d) illustrate the waveforms of the two BC collector currents ($1/T_1$ and $1/T_2$) and the two capacitor currents (i_{C1} and i_{C2}) for low, medium and high m values, as obtained from simulations with realistic device models. Observe the very good agreement between the theoretical and the simulated waveforms for all values of m and that the time-domain "profile" of the collector currents for large m values differs noticeably from that for low values of m. The results of Figure 13.22 correspond to an input signal frequency of 10 MHz and a lowpass biquad pole frequency of about 50 MHz, leading to an x value of 0.2 [29].

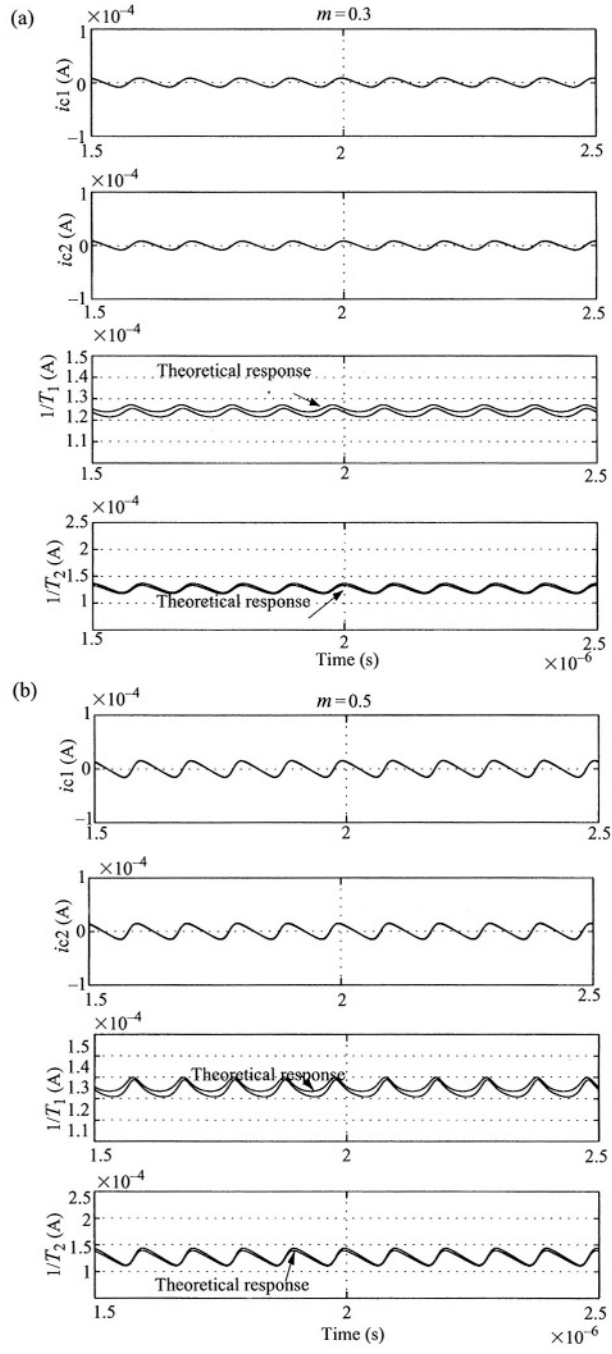


Figure 13.21. Continued.

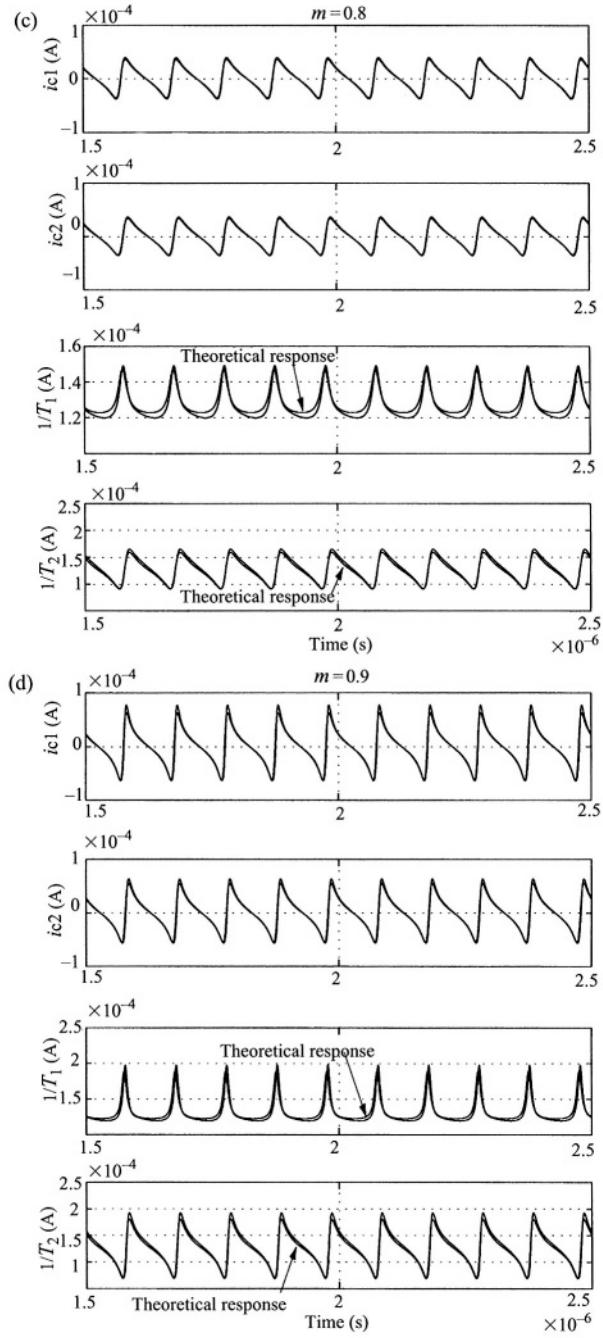


Figure 13.22. Theoretical and simulated internal current waveforms ($f_{in} = 10\,\text{MHz}$).

What is interesting to investigate is the effect of the modulation index (i.e. the input signal strength) upon the spectral content of the collector currents. How is the bandwidth of currents internal to the topology – *which are intentionally nonlinear* – affected by large m values? Bearing in mind the relations (13.39a and b), approximating quantities of the form

$$\frac{1}{1+\xi} \cong 1 - \xi + \xi^2 - \xi^3 + \xi^4 - \cdots \qquad |\xi| \leq 1$$

(with $\xi = m P_x \sin(\omega t + \varphi_1)$ or $\xi = m R_x \sin(\omega t + \phi_2)$) by means of a fifteen-term expansion and using a symbolic calculator package, the effect of the modulation index m upon the spectral content of the log-domain currents can be substantiated. Figures 13.23 and 13.24 show the line spectra of $1/T_1$ for $x = 0.2$ and $x = 1$ for small, medium and large modulation index values. Bear in mind that different x values correspond to different relative positioning in the passband; recall (13.41c). *Although these results are indicative only and should not be generalized for other topologies, they highlight the increased bandwidth requirements when input signals with large modulation index values are applied.* Qualitatively speaking, the rich spectral content of log-domain currents can be understood in a different way by realizing that when the input current signal is converted to a logarithmically compressed voltage, this voltage is characterized by several harmonic components which have to be processed in the logarithmic domain by the main body of the filter.

It can be shown that for high m values (**e.g.** $m \cong 80\%$), 95% of the (*desired*) THD levels of the currents $1/T_j$ ($j = 1, 2$) is contained within a bandwidth of 3ω, with ω denoting the input signal frequency. Consequently, the design of a lowpass biquad filter (like the one illustrated in Figure 13.15) with a pole frequency B, would require the transistors Q_1 and Q_2 to exhibit a bandwidth of at least $3B$ if they were to process their nonlinear signals without significant deviation from ideality. As a result of this "spectrally rich" behavior, the transition frequency f_T of Q_1 and Q_2 should satisfy the approximate relation $f_T/10 > 3B$ when the filter processes signals with large modulation index. This result embodies the price paid for the internal nonlinearity of log-domain filters: when high-level input signals are applied, then the bandwidth of the transistors processing current signals internal to the topology should be higher than for the case of an equivalent "linear" filter. It is not yet clear however "if" and "how much" the input–output linearity of log-domain filters is affected by transistor bandwidth limitations which suppress the (intentional) higher order harmonics. Such a study should incorporate the individual transistor non-idealities and consider input frequencies close enough to $f_T/10$ so that the internal current spectra are affected by the device frequency limitations; note that in such a case, beta-related errors would also increase.

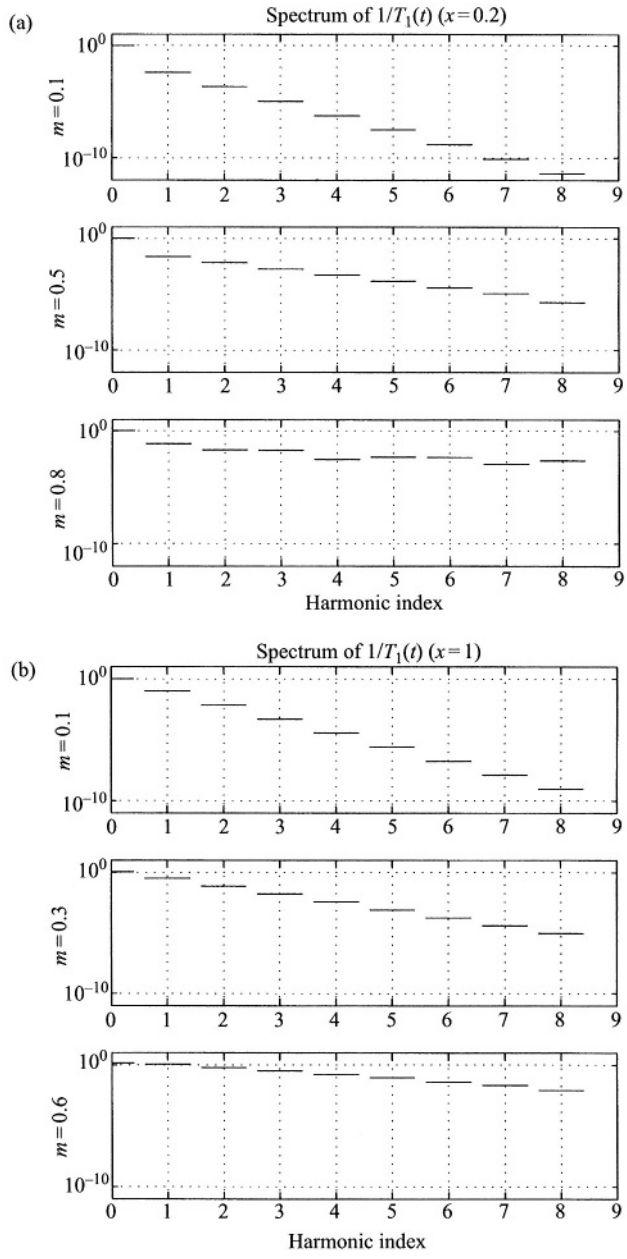


Figure 13.23. The spectrum of $1/T_1(t)$ for (a) $x = 0.2$ and (b) $x = 1$.

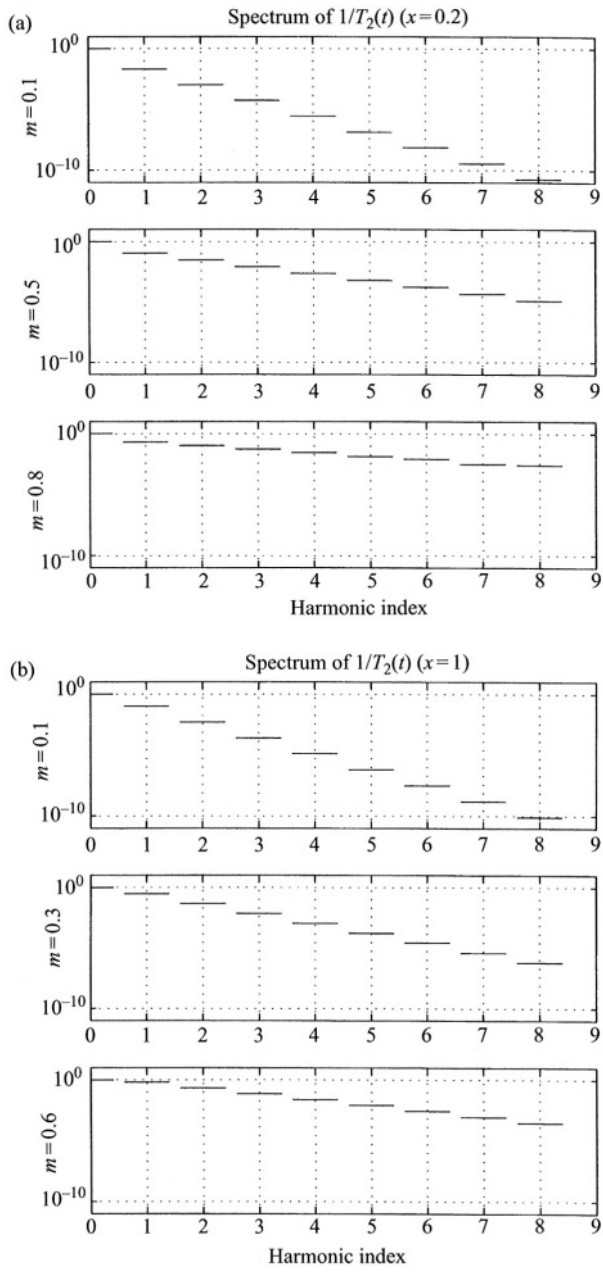


Figure 13.24. The spectrum of $1/T_2(t)$ for (a) $x = 0.2$ and (b) $x = 1$.

13.6. Distortion Properties of Log-Domain Circuits: The Lossy Integrator Case

The internally nonlinear character of log-domain topologies complicates the determination of their finite linearity levels. The incorporation of very detailed, large-signal models like the Ebers–Moll or the Gummel–Poon model [38] are intended for computer-aided design where the precision of the simulated circuits "takes precedence over conceptual or computational simplicity". A quick examination of the complete large-signal Gummel–Poon model for example, would reveal that at least eleven different parameters are needed for the successful modeling of a single BJT, making a symbolic calculation of distortion levels formidable and practically impossible. We may ask the question why is a symbolic calculation of distortion levels needed? What would it offer? The question is evidently rhetoric. If it is possible to correlate the finite log-domain linearity levels with the *primary* transistor non-idealities, then the designer would have a much clearer picture of the process-parameter dependent linearity limitations of the log-domain technique. Clearly, the more realistic the modeling, the more accurate the result.

Which are the primary BJT non-idealities as far as log-domain topologies are concerned (and why)? Practically any deviation from an assumed logarithmic (exponential) conformity would lead to distortion. Most attempts focus mainly on the effect of the parasitic base and emitter resistances and the finite beta of the devices. This is adequately justified by the fact that those three non-idealities *affect the base–emitter junction of each active device, and the parasitic voltage drops associated with their presence distorts the dynamic operation of the complete translinear loops (encountered in log-domain) in a direct way.* Since the role of the translinear loops is to "linearize" the input–output behavior of a log-domain circuit, it would be both expected and logical that any deviation from their ideal behavior would lead to the generation of harmonic distortion terms.

However, the question remains: what kind of moderate-level complexity model should be used for the representation of the active devices and a subsequent symbolic harmonic distortion analysis?

Since small-signal models ignore the very nature of log-domain circuits and cannot lead to the calculation of harmonic distortion coefficients, while detailed large-signal models – though accurate – are of such complexity that their use for hand-purpose calculations is practically prohibited, one of the remaining options is the adoption of the medium-level complexity charge-control model (CCM). Discussion of the CCM is beyond our scope here. For an excellent treatment of the particular model, the interested reader is referred to [39]. The CCM can be viewed as a basic "framework for BJT equations that is especially useful for time-dependent analysis. The most extensive use of the

CCM equations is for the solution of large-signal transient problems" [39]. In contrast to the nonlinear formulae correlating currents and voltages used for the construction of the Ebers–Moll or the Gummel–Poon model, the CCM models the BJT's dynamic operation as a set of linear DEs where the BJT terminal currents are related to charges stored in the transistor.

In an attempt to evaluate the distortion levels anticipated from the log-domain technique, a CCM-based distortion analysis of a basic log-domain circuit – that of the log-domain lossy integrator implemented by alternating (*not stacked*) V_{BE} junctions (see Figure 13.1) – was performed. The analysis is symbolic and manages to correlate distortion levels with basic process-dependent parameters. The analysis was based on expressing the transistor currents as Fourier series, stating the parasitic voltage drops associated with each device as a function of these currents, and then balancing the respective harmonic coefficients. A detailed outline of the approach can be found in [40]. Here we concentrate on some indicative results bearing in mind certain factors which limit the accuracy of the approach. Such factors are the simplicity of the model used, the quasi-static approximation under which the model is valid and the fact that the depletion capacitances were omitted.

The particular lossy integrator had a pole frequency at about 122 MHz, and was realized by equal biasing current values of $I_Q = 200\,\mu A$ and a capacitor value C = 10pF. It was verified that the second harmonic distortion was the dominant distortion (class A operation). It was also verified that despite the model simplicity and certain simplifications, the distortion levels predicted by the symbolic analysis for the particular device parameters were in fairly good agreement (within 3 dBs) with the passband distortion levels calculated by means of HSPICE transient analysis when the full device models were used. Furthermore, it was verified that the dependence of the symbolically predicted distortion upon the input modulation index m was in good agreement with HSPICE results.

As expected, the analysis shows (see Figure 13.25) that the stronger the input signal (i.e. the higher the modulation index value m), the higher the distortion, which for the particular device model used peaks smoothly at a frequency of about 60 MHz. The strong influence of m upon distortion is very clear for the entire passband; the distortion increases by approximately 14 dBs when the modulation index changes from m = 10% to m = 50%. The graphs of Figures 13.26 and 13.27 were obtained for an input signal frequency of 60 MHz, that is, where the distortion exhibits its maximum. Figure 13.26 reveals the variation of the second harmonic distortion (the dominant distortion for the class A integrator) for different r_B and m values; the combination of high r_B and m values leads to a pronounced increase in the distortion which varies smoothly. For m = 50%, an increase of about 5.6dBs is predicted when r_B varies from its minimum to its maximum value. Figure 13.27 shows the variation in the

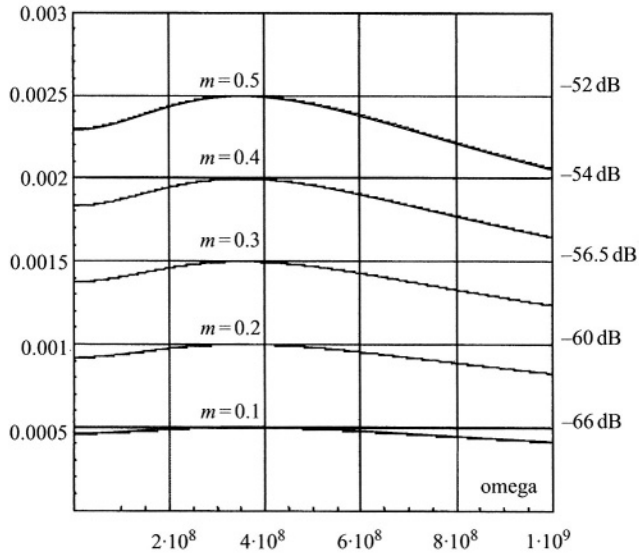


Figure 13.25. Frequency dependence fof calculated second harmonic distortion for different input levels.

distortion levels against beta for different input signal levels. The results of Figure 13.27 reveal that low beta values ($\beta < 60$) lead to a considerable increase in distortion. In general, for $\beta \geq 60$ and $m \leq 50\%$, the distortion levels remain below 1%. Commenting on this behavior, it is trivial to realize that when the capacitor is not present (an assumption approximately valid when input tones placed deep in the passband are considered), the remaining four BJTs constitute the *beta immune* "Type A" Gilbert Cell.

On the other hand, what is interesting to note is the slow improvement in the predicted distortion levels for high beta values. *It should be emphasized though that the above beta-related dependence of the distortion levels cannot be generalized for other more complicated topologies.* The variation of the distortion levels with the parasitic emitter resistance r_E is intriguing. Simulations and symbolic calculations predict a strong "shift to the left" of the frequency response when r_E – and consequently the respective parasitic voltage drop – increases (as shown in Table 13.2). As the pole frequency of the response reduces with increased r_E values, harmonics of a fixed input frequency would move gradually from the passband to the stopband; thus the filtering action can lead to reduced distortion levels in this case [40]. Speaking qualitatively again, a different way of understanding this behavior is to realize that increased r_E values, apart from reducing the effective transcondutance of a device for a

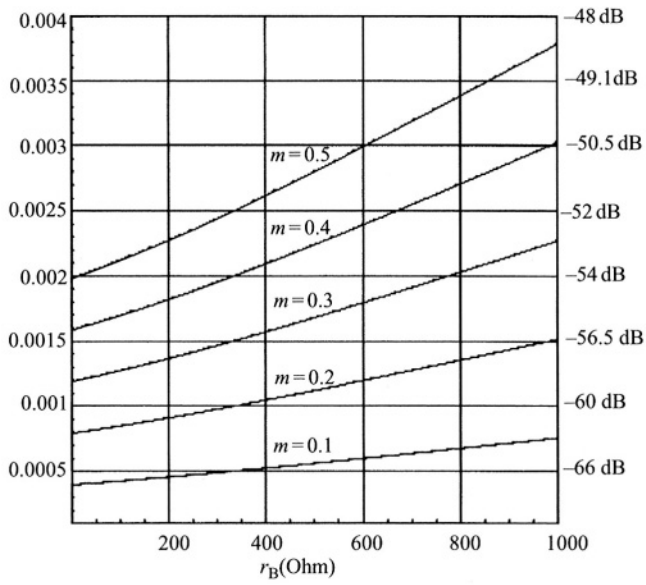


Figure 13.26. Effect of r_B upon distortion for different input levels ($f_{in} = 60$ MHz).

given current level (compare with $g_{m\,eff}$ in Section 13.3), also provide a certain degree of linearization via emitter degeneration.

13.7. Noise Properties of Log-Domain Circuits: The Lossy Integrator Case

Due to their internally nonlinear character, log-domain circuits exhibit noise characteristics which are not trivial to analyze: noise at internal point is subject to nonlinear signal processing. Since the devices undergo large signal variations it would be erroneous for their operating point to be considered as "fixed"; hence classic (small-signal) ac noise calculations based on constant g_m are not applicable.

1 A very illustrative qualitative discussion dealing with the general properties of companding processors (a special case of which are the log-domain topologies) has been offered by Tsividis [41]. Tsividis has classified log-domain filters as belonging to the general class of Externally Linear Internally Nonlinear (ELIN) structures.

In [41], Tsividis considers the operation of a general ELIN integrator modeled as shown in Figure 13.28: the output y is generated by the operation of the function $f()$ upon an intermediate variable w, which appears at the output of the integrator and which at the same time updates the gain of the predistortion

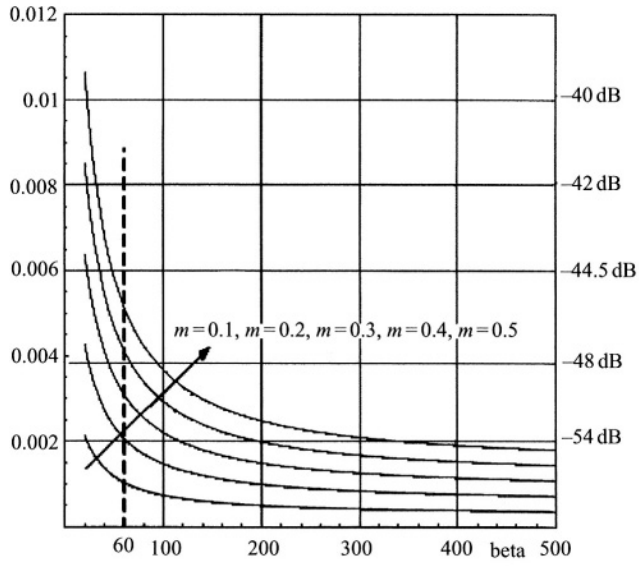


Figure 13.27. Effect of β upon distortion for different input levels ($f_{in} = 60$ MHz).

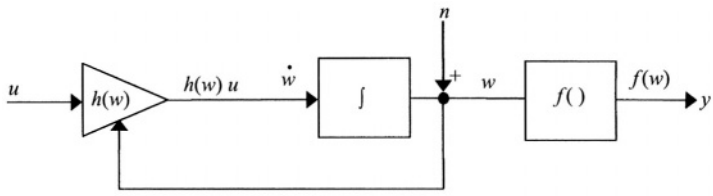


Figure 13.28. Tsividis' general ELIN companding integrator [41].

block $h()$ in an appropriate way, such that:

$$h(w)\frac{\mathrm{d}f}{\mathrm{d}w} = K = \text{constant} \tag{13.42}$$

This operational condition leads to the relation

$$\dot{y}(t) = \frac{\mathrm{d}f}{\mathrm{d}w}\dot{w}(t) = \left[\frac{\mathrm{d}f}{\mathrm{d}w}h(w)\right]u(t) \quad \Rightarrow \quad y(t) = K\int u(t)\,\mathrm{d}t \tag{13.43}$$

which corresponds to an ideal integrator. When the signals u, $h(w)u$, y denote currents, the variable w corresponds to a capacitor voltage which is non-linearly related to the input (output) signal $u(y)$. In a log-domain circuit, $f()$ is an exponential, leading to an elegant implementation with bipolar transistors. As

an illustrative example, let it be supposed that the $f()$ function corresponds to a general sinh function given by:

$$f(w) = \frac{\exp(w) - \exp(-w)}{2} \tag{13.44a}$$

Because of the operational condition (13.42), in this case (for $K = 1$):

$$h(w) = \frac{2}{\exp(w) + \exp(-w)} \tag{13.44b}$$

Now, in order for the noise properties of this elementary companding processor to be understood, let us assume the presence of an additive noise source at the output of the integrator block just before the $f()$ function block. This noise will also undergo the impact of the nonlinearity $f()$, resulting in a total output signal

$$y = f(w + n) \cong f(w) + f'(w)\, n \tag{13.45}$$

where a first-order expansion has been assumed; the quantity $f(w)$ corresponds to the noise-free component of the signal whereas the term $f'(w)n$ corresponds to the noise present at the output. It can be observed that the initial noise n appears at the output scaled by a time-varying multiplicative factor $f'[w(t)]$ which modulates the noise. For small-signal inputs, $f'[w(t)]$ remains approximately constant and the noise response is similar to classical small-signal approaches. However, considering large w values, from (13.44a) it will hold:

$$f(w) = \pm\frac{\exp(|w|)}{2} \tag{13.46a}$$

leading to

$$f'(w) = \frac{df}{dw} = \frac{\exp(\,|w|\,)}{2} = \pm f(w)(= \text{signal } y) \tag{13.46b}$$

From (13.45) and (13.46a) it can be written:

$$\text{output noise} = (\text{noise at the input}) \times (\text{magnitude of output signal}) \tag{13.47a}$$

The above statement codifies the essence of the noise behavior of companding processors such as the general ELIN integrator depicted in Figure 13.28. Summarizing the above discussion, it is clear that the output noise originating from noise or interference present at internal points will

- be modulated by the signal, producing intermodulation products, and
- depend both on the signal level and shape.

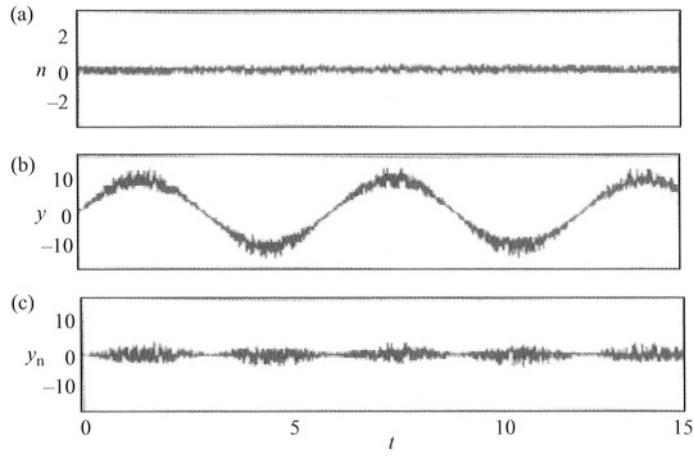


Figure 13.29. (a) Injected noise, (b) noisy output and (c) output noise for the ELIN integrator ase with $f()$,$h()$ given by (13.7.3.a,b) (compare with Figure 13.27) [14-41].

Tsividis' simulation results verify the increase of the output noise in proportion to the signal magnitude; Figures 13.29(a)–(c) illustrate his results. Observe the scale difference of the noise graphs.

The additive noise considered so far might be considered as corresponding to any kind of noise generated randomly within the system or induced by external interference. Noise corresponding to equivalent input noise sources of the $h()$ and $f()$ blocks would in general be signal dependent, since "the nonlinear I–V characteristics of the devices used to implement the $h()$ and/or $f()$ blocks are exercised over a wide range". In other words, instantaneous currents and voltages within the $h()$ and $f()$ blocks vary widely, thus their internal equivalent noise sources will vary similarly.

The above qualitative discussion has aimed to make clear that the noise floor is signal dependent; this can lead to a potentially very troublesome situation: referring to the input of the $f()$ block, suppose the co-existence of two signals; one of which is small and constitutes the desired signal, while the second is large (i.e. an adjacent channel interferer). The large signal will drive the characteristic $f(w)$ – given for example by (13.44a) – into regions of high $\mathrm{d}f/\mathrm{d}w$ values, augmenting the noise at the output. This will happen even if the adjacent channel signal will eventually be rejected (due to the filtering action, for example). Consequently, the elevated (due to the large signal) noise floor will reduce the small-signal SNR. This kind of behavior has also been confirmed by simulations as shown in Figures 13.30(a) and (b).

For the particular case that the noise is wide-sense stationary and white with zero mean, the input is periodic and the noiseless system has reached its steady

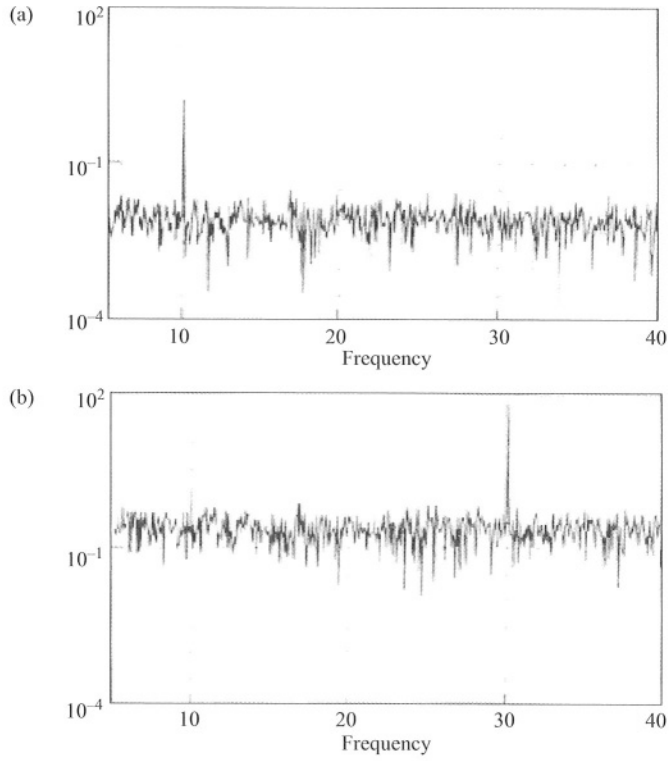


Figure 13.30. Noise floor elevation in the presence of a strong input signal (b); compare with (a) when only a weak input signal is present [41].

state then – according to Toth et al. [42] – the output PSD will be given by

$$S_{\text{out}}(\omega) = \Theta S_{\text{I}} \tag{13.47b}$$

with S_{I} the additive noise PSD and

$$\Theta = \frac{1}{T}\int_0^T \left\{f'[w(\tau)]\right\}^2 \mathrm{d}\tau \tag{13.47c}$$

T denotes the input signal period.

For the specific case of a log-domain integrator excited by a current signal $D\ [1 + m\ \sin(\omega t)]\ (m < 1)$ and producing at the output the linear tone $D_{\text{out}} + A\ \cos(\omega t + \phi)$, Θ is given by:

$$\Theta = \frac{D_{\text{out}}^2}{V_{\text{T}}^2} + \frac{[A^2/2]}{V_{\text{T}}^2} \tag{13.47d}$$

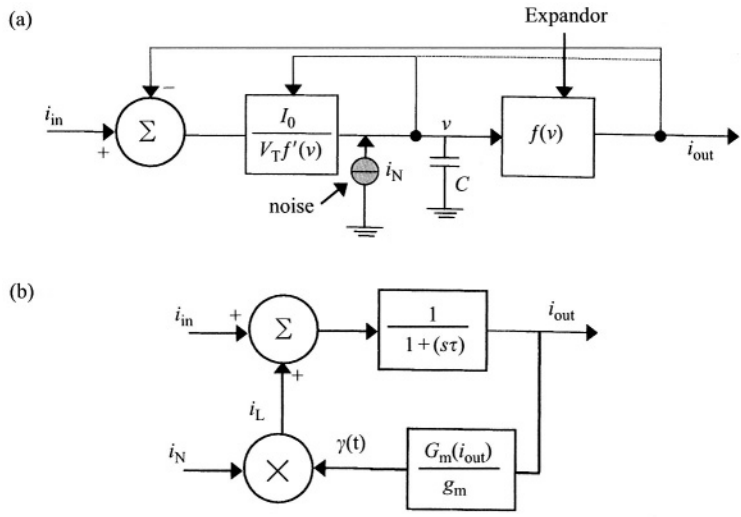


Figure 13.31. Enz et al. noise-model of the log-domain lossy integrator [43].

($D_{out} = (I_0/I_d)D$ and $A = (I_0/I_d)(m\, D\sqrt{1+(CV_T\omega/I_d)^2})$ with I_d and I_0 representing the damping and the gain controlling current respectively; see Figure 13.1, for example). From (13.47d) it can be seen that Θ expresses "nothing but the average of $[g_m(t)]^2$ over the input signal period, with $g_m(t)$ denoting the instantaneous transconductance of the output device which operates as an exponential expander". From (13.47d), it is clear that, for the class A log-domain lossy integrator, the variation of noise is not strong since $\Theta_{max}/\Theta_{min} = 1.5$. The situation though is substantially different for class AB.

2 Another attempt in quantifying noise behavior in log-domain circuits has been presented by Enz, Punzenberger et al. [43,44]. The block diagrams given in Figure 13.31(a) and (b) corresponds to the case of the log-domain lossy integrator; Figure 13.31 (b) models the noise behavior of the system: a noise current source $i_N(t)$ which is assumed stationary and with power spectral density (PSD) $S_N(f)$, is modulated by the signal $\gamma(t)$ for which

$$\gamma(t) = \frac{f'(v)}{g_m} = \frac{G_m(i_{out})}{g_m} \tag{13.48a}$$

This leads to the modified DE for the circuit:

$$\tau \frac{di_{out}}{dt} + i_{out} = i_{in} + \gamma(t) i_N \tag{13.48b}$$

In (13.48a) g_m denotes the fixed, signal-independent transconductance which determines the cut-off frequency and $G_m(i_{out})$ denotes the (time-varying)

transconductance of the expanding device, which is proportional to the instantaneous value of the output current i_{out}. Accordingly, (13.48a) reduces to:

$$\gamma(t) = \frac{i_{\text{out}}(t)}{I_0} \tag{13.48c}$$

Assuming that the noise signal $i_{\text{N}}(t)$ *is not correlated with the input current* $i_{\text{in}}(t)$, the PSD of the noise signal $i_{\text{L}}(t)$ can be calculated as [43]:

$$S_{\text{L}}(f) = \sum_{n=-\infty}^{+\infty} |\Gamma_n|^2 S_{\text{N}}(f - nf_{\text{in}}) \tag{13.49}$$

In other words, due to the modulation process, the noise S_{L} appears to be a frequency translated and weighted version of the input noise S_{N} with spectral components at the harmonics of the output signal; the component located at a frequency nf_{in} is weighted by the power $|\Gamma_n|^2$ of this component (normalized to I_0). For the simplified case of white noise $S_{\text{N}}(f) = S_0$,

$$S_{\text{L}}(f) = \left\{ \sum_{n=-\infty}^{+\infty} |\Gamma_n|^2 \right\} S_0 = \Gamma_{\text{rms}}^2 S_0 \tag{13.50}$$

with thequantity Γ_{rms}^2 readily definable from (13.50), and corresponding to the normalized power of the modulation signal $\gamma(t)$. For the case of an alternating output current superimposed on the dc bias current I_0 [43],

$$\Gamma_{\text{rms}}^2 = \frac{I_0^2 + I_{\text{sig,rms}}^2}{I_0^2} \tag{13.51}$$

For the PSD $S_{\text{out}}(f)$ of the output noise it holds that:

$$S_{\text{out}}(f) = \frac{S_{\text{L}}(f)}{1 + (2\pi f \tau)^2} \tag{13.52a}$$

The total output noise power is derived as follows (when (13.50) is taken into consideration):

$$I_{\text{N}_{\text{out}}}^2 = \int_0^{+\infty} S_{\text{out}}(f)\, \mathrm{d}f = \Gamma_{\text{rms}}^2\, S_0\, \frac{1}{4\tau} \tag{13.52b}$$

with $1/4\tau$ being the noise bandwidth of the filter. Considering (13.51) and assuming (collector current) shot noise only with $S_0 = 2q\, I_0$, (13.52b) yields:

$$I_{\text{N}_{\text{out}}}^2 = \frac{q^2}{2kTC}\left[I_0^2 + I_{\text{sig,rms}}^2\right] \tag{13.52c}$$

It must be underlined that the above treatment considers the noise contributions of all transistors as being constant in time; a hypothesis which simplifies the analysis but is not in practice realistic, since collector currents in the circuit depend strongly on the input signal, thus the shot noise varies similarly. This "constant noise" assumption in conjunction with neglected correlations between noise sources constitute significant approximations of the above analysis.

From (13.52c), it can be seen that the output noise power depends on both the square of the dc bias current present at the output, and on half the squared amplitude of the output sinusoidal tone when the input is excited sinusoidally (compare with (13.47d)). For class A operation, the noise floor is practically determined by the output bias current since the alternating signal is limited by it. For class AB operation however, when the signal rms value becomes much larger than the bias current, the noise will increase proportionally to the signal. Thus, from (13.52c) it can be concluded that in general

$$\mathrm{SNR} \cong \mathrm{SNR}_{\max} \frac{I_{\mathrm{sig,rms}}^2}{I_0^2 + I_{\mathrm{sig,rms}}^2} \tag{13.53a}$$

or, when $I_{\mathrm{sig,rms}} \ll I_0$,

$$\mathrm{SNR} \cong \mathrm{SNR}_{\max} \left(\frac{I_{\mathrm{sig,rms}}}{I_0} \right)^2 \tag{13.53b}$$

with

$$\mathrm{SNR}_{\max} = \frac{2kTC}{q^2} \tag{13.54}$$

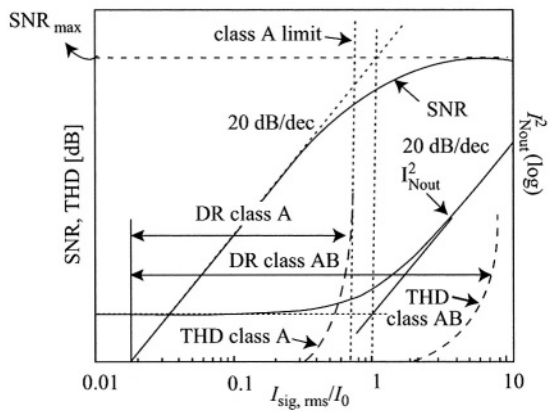


Figure 13.32. Enz et al. SNR calculation results [42].

Figure 13.32 shows the SNR (and THD) variation which rises with a slope of 20 dB/decade as the signal increases. Observe the anticipated potential of extended dynamic range under class AB operation compared to the class A case; *this though, happens at the expense of a flattened SNR. The SNR does not increase beyond* $\mathbf{SNR_{max}}$ *for class AB operation case.*

An advanced and very detailed noise analysis of the log-domain lossy integrator was also offered by Mulder–Kouwenhoven–Serdijn et al. in [45]. Their analysis takes into consideration the correlation of noise sources internal to the lossy log-domain integrator and considers time-averages of time-dependent noise spectra. A detailed elaboration of their studies here though is beyond the scope of this chapter.

13.8. Summary

This chapter has elaborated several issues related to log-domain filters beginning with a discussion of the design philosophy behind the various log-domain synthesis techniques. In contrast to more conventional approaches, the increased mathematical complexity associated with the log-domain technique, and stemming from the exploitation of the large-signal device characteristic, was underlined. The effect of important BJT parasitics (e.g. finite current gain, base and emitter resistances) upon both the transfer functions and the output distortion levels was next addressed, while the impact upon linearity when realizing finite transmission zeros by means of floating capacitors was also explained. The effect of input signal modulation index upon the bandwidth of (nonlinear) currents internal to a log-domain topology was elaborated. The chapter concluded with the intriguing properties of noise in log-domain.

It is genuinely hoped that this chapter can serve as an insightful introduction to a further in-depth study of filtering in the log-domain.

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Chapter 14

TRADE-OFFS IN THE DESIGN OF CMOS COMPARATORS

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14.1. Introduction[1]

Comparators are used to *detect* whether an *analog* signal $x_+(t)$ is larger or smaller than other $x_-(t)$,[2] and to *codify* the outcome in digital domain as follows:

$$y = \begin{cases} 1_D & \text{for } x_+(t) > x_-(t) \\ 0_D & \text{for } x_+(t) < x_-(t) \end{cases} \tag{14.1}$$

where y is the output signal, 0_D represents the logic zero and 1_D is the logic one. Ideal comparators should be capable of detecting arbitrarily small differences between the input signals. However, in practice, these differences must be larger than a characteristic *resolution* parameter ξ for proper detection. For a given comparator circuit, the value of this resolution parameter changes depending upon the operating conditions. If the temporal window allocated for comparison is long enough, ξ takes an absolute minimum value which is inherent in the comparator device and which defines its maximum accuracy. As the temporal window shrinks, the value of ξ increases above its absolute minimum value and, hence, the comparator accuracy worsens. It highlights a trade-off between *accuracy* and *speed* of operation; the larger the speed the smaller the accuracy. As in any other analog circuit, this trade-off is also influenced by power consumption and area occupation.

Comparators are the very basic building blocks of analog-to-digital converters. They are hence crucial components to realize the front-ends of the newest generations of *mixed-signal* CMOS electronic systems [1,2]. Other comparator

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[2] In many applications one of the inputs is a reference value, say $x_-(t) = E$, and the comparator detects whether the signal applied to the other input, say $x_+(t) \equiv x(t)$, is larger or smaller than such reference.

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applications include such diverse areas as signal and function generation [3], digital communications [4], or artificial neural networks [5], among others.

This chapter first presents an overview of CMOS voltage[3] comparator architectures and circuits. Starting from the identification of the comparator behavior, Section 14.2 introduces several comparator architectures and circuits. Then, Section 14.3 assumes these topologies, characterizes high-level attributes, such as static gain, unitary time constant, etc., and analyzes the resolution–speed trade-off for each architecture. Such analysis provides a basis for comparison among architectures. These previous sections of the chapter neglect the influence of circuit dissymmetries. Dissymmetries are covered in Section 14.4 and new comparator topologies are presented to overcome the offset caused by dissymmetries. Related high-level trade-offs for these topologies are also studied in this section.

14.2. Overview of Basic CMOS Voltage Comparator Architectures

Figure 14.1(a) shows the static transfer characteristic of an ideal comparator where $x \equiv x_+(t) - x_-(t)$ and E_{OH} and– E_{OL} are levels that correspond to the logic one and zero, respectively. From now on, we will implicitly assume that comparator inputs and output are voltages. The case where inputs are currents and the output is a voltage – current comparators – will also be considered in this chapter.

From Figure 14.1(a) it is seen that an ideal voltage comparator must exhibit infinite *voltage gain* around the zero value of the differential input *x*. Obviously, this cannot be achieved by any real device. Figure 14.1(b) shows a better

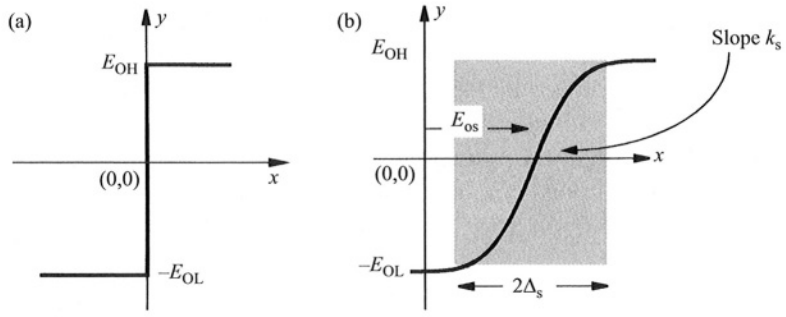


Figure 14.1. Comparator transfer characteristics: (a) ideal, (b) first-order non-ideal.

3 This is used here to mean that inputs and output are all voltages.

approximation of the static transfer characteristics exhibited by actual comparators. There, the transfer characteristic is assumed to have a *finite* static gain, k_s, around an *input offset* voltage, E_{os}. On the basis of this nonlinear characteristic, the minimum value of the resolution, called herein *static resolution,* is

$$\xi_s \approx |E_{os}| + \frac{E_{OH} + E_{OL}}{2k_s} \approx |E_{os}| + \left.\frac{E_{OH}}{k_s}\right|_{\text{for } E_{OL} \approx E_{OH}} \tag{14.2}$$

where the random nature of the offset has been accounted for by including its module, and it has been assumed that the shaded transition interval is symmetrical around the input offset.[4] For any input level inside the interval $[-\xi_s, \xi_s]$ the comparator digital output state is uncertain. Otherwise, any input level outside this interval, called an *overdrive,* generates an unambiguous digital state at the comparator output. The overdrive variable measures how far from this interval the actual input is, $|x_{ovd}| = |x| - \xi_s$.

14.2.1. Single-Step Voltage Comparators

Voltage comparators are basically *voltage gain* devices. Hence, they can be implemented with the same circuit topologies employed for voltage amplifiers. Figure 14.2(a)–(c) shows three CMOS alternatives which are all *single-stage* Operational Transconductance Amplifiers (OTA) [6]. Those in Figure 14.2(a) and (b) have differential input and single-ended output and will be called, respectively, Asymmetric Operational Transconductance Amplifier Comparator (AOTAC) and Symmetric Operational Transconductance Amplifier Comparator (SOTAC). On the other hand, that in Figure 14.2(c) is a fully-differential topology where the output is obtained as the difference between the voltages at the output terminals of a symmetrically loaded differential pair. In this structure, called Fully-Differential Operational Transconductance Amplifier Comparator (FDOTAC), the bias current of the differential pair must be controlled through a feedback circuitry in order to stabilize and set the quiescent value of the common-mode output voltage [7]; this common-mode regulation circuitry has not been included in Figure 14.2(c).

All circuits in Figure 14.2(a)–(c) use the same mechanism for achieving voltage gain. Figure 14.2(d) shows a first-order conceptual model for approximating the behavior underlying such mechanism around the input transition point. There, the transconductance g_m models the operation of the differential

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[4] For more accurate calculation of ξ_s, the levels which guarantee unambiguous interpretation of the logic zero and one, namely $E_{RH} < E_{OH}$ and $-E_{RL} > -E_{OL}$, should be used instead of E_{OH} and $-E_{OL}$. Also, the gain should not be considered constant over the transition interval. Finally, two different transition intervals should be considered, one for positive excursions Δ_{s+} and another for negative excursions Δ_{s-}.

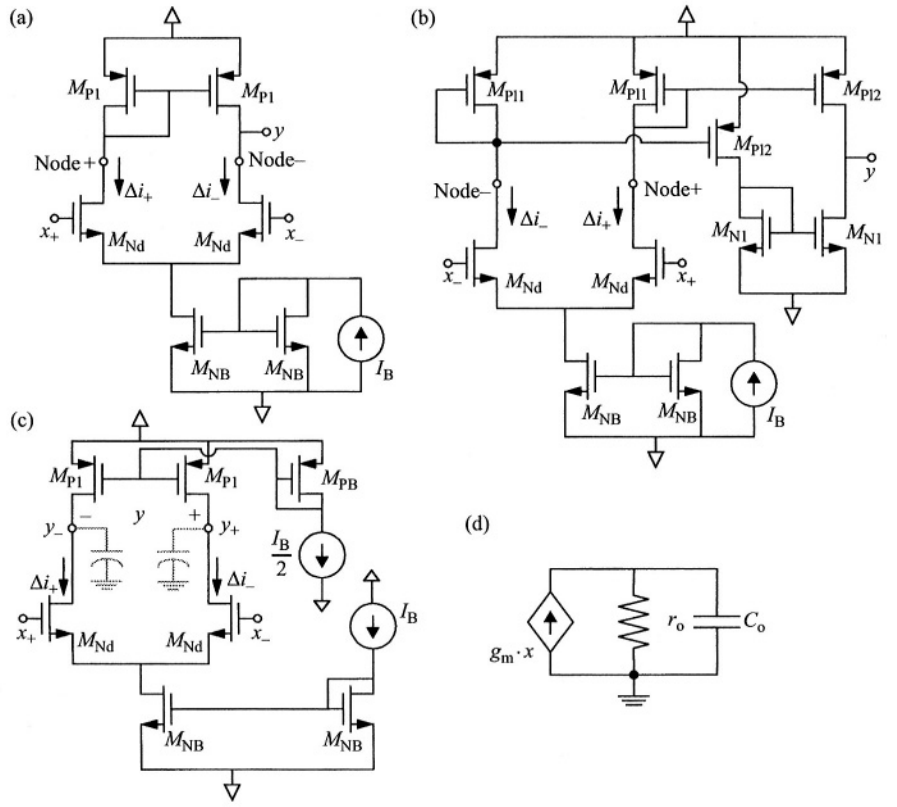


Figure 14.2. (a)–(c) CMOS single-step comparator topologies, (d) first-order small-signal model around the input offset voltage.

pair formed by the *matched*[5] transistors M_{Nd} and the associated biasing transistors M_{NB}, the resistance r_o models the combined action of the output resistances of all transistors, and the capacitance C_o models the combined effect of external capacitive loads and transistor parasitics at the output node. The three first rows in Table 14.1 include expressions for these model parameters in terms of the transistor sizes, the large-signal MOST transconductance density β_0, and the MOST Early voltage V_A – see the Appendix for a simplified MOST model.

In all three circuits of Figure 14.2 the static gain is given by

$$k_s = g_m \cdot r_o \tag{14.3}$$

5 The term matched here means that the transistors are designed to be equal, that is, same sizes, same orientation, same surrounding, etc. In practice, the transistors are mismatched. Actually, mismatch is the main source of input offset.

Table 14.1. Model parameters of one-step CMOS comparator structures.

Parameters→ *Structure* ↓	g_m	$g_o = r_o^{-1}$	C_o
AOTAC		$\frac{I_B}{2} \cdot \left(\frac{1}{V_{ANd}} + \frac{1}{V_{API}}\right)$	$C_L + \nu_{Nd} \cdot W_{Nd} \cdot C_{GD0Nd} + \nu_{PI} \cdot W_{PI} \cdot C_{GD0PI}$
SOTAC		$\frac{I_B}{2} \cdot \left(\frac{1}{V_{ANI}} + \frac{1}{V_{API2}}\right)$	$C_L + \nu_{NI} \cdot W_{NI} \cdot C_{GD0NI} + \nu_{PI2} \cdot W_{PI2} \cdot C_{GD0PI2}$
FDOTAC	$\sqrt{2 \cdot \frac{\beta_{0Nd}}{n_{Nd}} \cdot \left(\frac{W}{L}\right)_{Nd} \cdot I_B}$	$\frac{I_B}{2} \cdot \left(\frac{1}{V_{ANd}} + \frac{1}{V_{API}}\right)$	$C_L + \nu_{Nd} \cdot W_{Nd} \cdot C_{GD0Nd} + \nu_{PI} \cdot W_{PI} \cdot C_{GD0PI}$
FOTAC		$\frac{1}{4 \cdot V_{ANI} \cdot V_{ACN}} \sqrt{\frac{I_B^3}{2 \cdot \frac{\beta_{0CN}}{n_{CN}} \cdot \left(\frac{W}{L}\right)_{CN}}} + \frac{1}{4 \cdot V_{API} \cdot V_{ACP}} \sqrt{\frac{I_B^3}{2 \cdot \frac{\beta_{0CP}}{n_{CP}} \cdot \left(\frac{W}{L}\right)_{CP}}}$	$C_L + \nu_{CN} \cdot W_{CN} \cdot C_{GD0CN} + \nu_{CP} \cdot W_{CP} \cdot C_{GD0CP}$

which, using the expressions of Table 14.1, and assuming that Early voltages are proportional to transistor lengths, yields the following dependence of the static gain on design parameters,

$$k_s \propto \frac{\sqrt{W_{Nd}} \cdot \sqrt{L}}{\sqrt{I_B}} \tag{14.4}$$

These structures are well suited to provide static gains around 40dB, which from equation (14.2), neglecting for the moment the input offset, and assuming $E_{OH} \approx 1\,V$, results in an absolute value of the static resolution of around 10 mV.

The limited resolution due to low static gain values can be overcome by resorting to the use of cascode transistors. The circuit of Figure 14.3(a), labeled Folded Operational Transconductance Amplifier Comparator (FOTAC), is a representative example. The first-order model of Figure 14.2(d) is still valid but now the resistance parameter r_o is increased in a factor approximately equal to the gain of the cascode devices M_{CN} and M_{CP}. Then, assuming that all transistors have the same channel length, it follows that

$$k_s \propto \frac{\sqrt{W_{Nd}} \cdot \sqrt{W_C} \cdot \sqrt{L^3}}{I_B} \tag{14.5}$$

which renders this structure appropriate for obtaining static gains up to around 80 dB and, hence, Δ_s around 0.1 mV.

Further gain enhancement can be achieved by enforcing the cascode action through the incorporation of local feedback amplifiers – illustrated in Figure 14.3(b) [8].

14.2.2. Multistep Comparators

Essentially, in the structures of Figures 14.2 and 14.3, the gain needed for the comparison function is built in a *single step*.[6] Later in the chapter it will be shown that this results in a disadvantageous resolution–speed trade-off. To relax this trade-off, multistep structures are employed that achieve the voltage gain into multiple steps, through the multiplication of several $g_m \cdot r_o$ gain factors [9,10]. Figure 14.4(a) shows such a multistep architecture at the conceptual

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6 We understand that the basic mechanism to achieve voltage gain is multiplying a small-signal transconductance g_m by a small-signal resistance r_o. The product $g_m \cdot r_o$ defines the basic voltage gain factor. In the simplest OTA, the gain is equal to the product of just one transconductance by one resistance; that is, it is equal to single gain factor $g_m \cdot r_o$. This is the reason why we say that these structures obtain the gain into one step. It can be argued that this does not apply to cascode architectures, where the gain is enhanced through multiplying r_o by the gain of the cascode transistors. However, for convenience we also consider cascode architectures as single-step comparators.

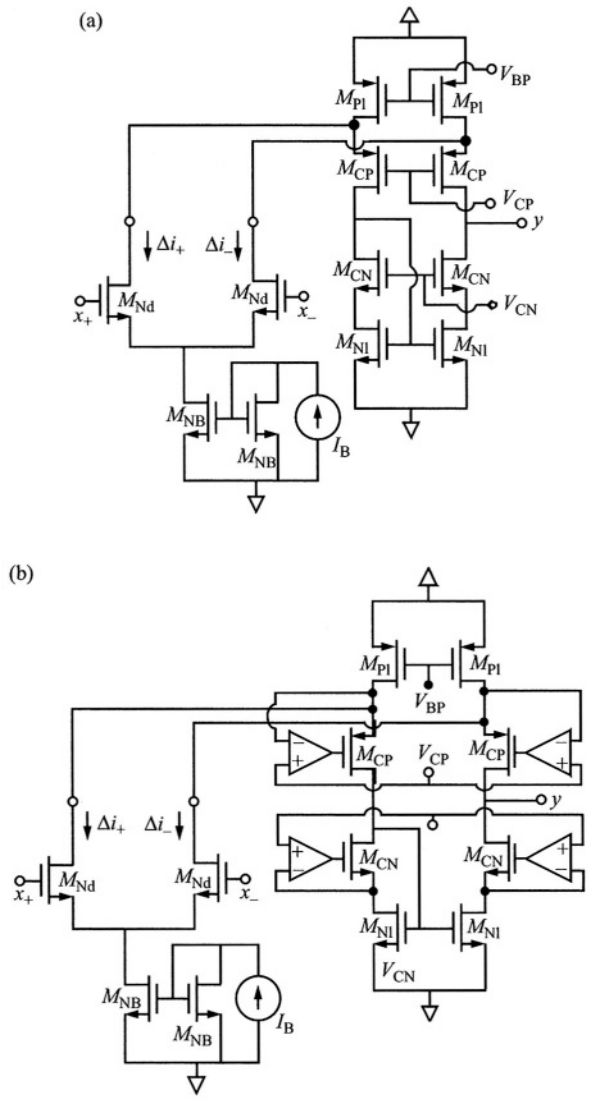


Figure 14.3. **Single-step comparators with cascode transistors.**

level. Assuming for illustration that the N stages are identical, each having a gain $k_s = g_m/g_o$, the following expression is calculated for the static resolution:

$$\xi_s \approx |E_{os}| + E_{OH} \cdot \left(\frac{g_o}{g_m}\right)^N \tag{14.6}$$

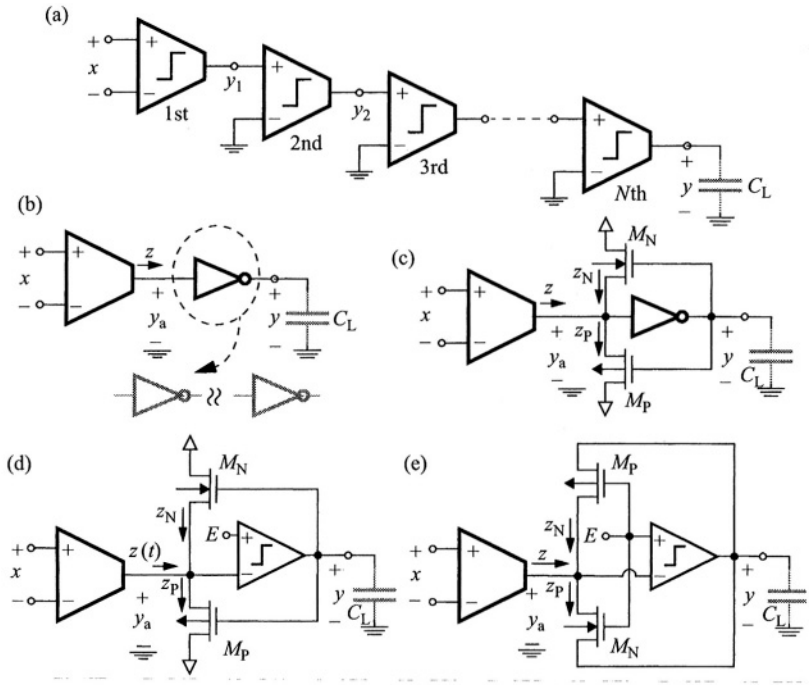


Figure 14.4. Multistep voltage comparators at the conceptual level.

where $|E_{OS}|$ is the offset voltage of the first stage of the cascade. The offset of each of the remaining stages is neglected because it is attenuated by the gain of the preceding stages in the chain. In comparison with equation (14.2), equation (14.6) shows that the impact of the static gain on the static resolution is much smaller than for single-step architectures. Actually, for large enough N the static resolution of multistep architectures is basically limited by the offset voltage, and the influence of the static gain becomes negligible.

The stages employed in a multistep comparator are generically different. Figure 14.4(b) shows a typical topology consisting of a front-end OTA followed by a CMOS inverter. Similar to what is done for buffering logic signals, several CMOS inverters with properly scaled transistor dimensions can be cascaded to enhance the speed of the logic transitions for a given capacitive load – as illustrated in the figure inset. Figure 14.5(a) shows an actual CMOS implementation of one of such topologies [11].

We can think of a CMOS inverter as a current comparator [12]. Any positive current driving the inverter is integrated by the input capacitor – see Figure 14.4(b) – increasing voltage y_a, and driving the output voltage to the logic zero; reciprocally, any negative current driving this node makes voltage

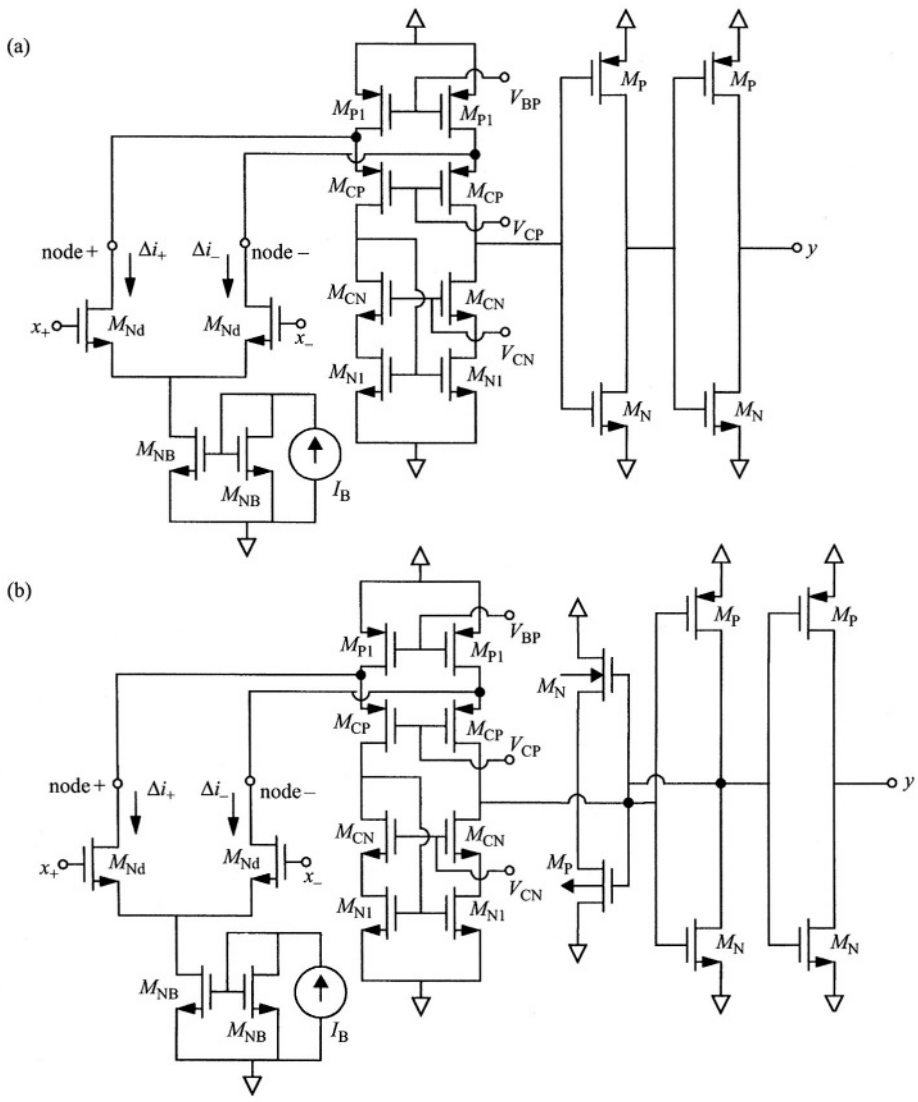


Figure 14.5. Some multistep CMOS voltage comparators.

y_a decrease and drives the output to the logic one. Thus, the operation of the two-step topology of Figure 14.4(b) can be described as follows: the front-end OTA transforms the input voltage difference x into a current $z = g_m \cdot x$, whose sign is then detected by the CMOS inverter operating as a current comparator. Based on this view, improved multistep comparator architectures can be obtained by simply replacing the CMOS inverter by high-performance CMOS current comparators [12].

Figure 14.4(c) presents a circuit based on this principle that requires just two extra transistors, labelled M_N and M_P. This circuit has three operating regions. For small changes around the *quiescent point*[7] ($z = 0$ and $y_a \approx 0$), transistors M_N and M_P are OFF, the inverter practically operates in open-loop configuration, and node y_a is capacitive. For $z > 0$, the voltage y_a is pulled up and the amplifier forces the voltage at node y to decrease; thus, M_P becomes ON, and the subsequent feedback action clamps the voltage y_a to

$$y_a \approx \frac{|V_{TP}|}{1 + A_0} \equiv \Delta_H \tag{14.7}$$

where A_0 denotes the inverter gain, and V_{TP} stands for the threshold voltage of the PMOS device. The dual situation occurs for $z < 0$, when y_a is pulled down, y increases, M_N becomes ON, and the feedback action clamps y_a to

$$y_a \approx -\frac{V_{TN}}{1 + A_0} \equiv -\Delta_L \tag{14.8}$$

Thus, it is seen that y_a changes into a rather small interval $[-\Delta_L, \Delta_H]$, which may render important speed advantages. Figure 14.4(d) achieves better control of the location of this interval, together with further reduction of its amplitude, by replacing the inverter by a differential input amplifier. There, the virtual ground action of this amplifier forces y_a to remain very close to E, regardless of the magnitude of the input signal difference. A proper choice of the value of E can help to improve the operation of the front-end OTA by conveniently biasing its output transistors.

The structures of Figure 14.4(c) and (d) have the drawback that the transient behavior is largely dominated by the capacitor across the nodes y_a and y [11]. The circuit of Figure 14.4(e) circumvents this problem by decoupling the amplifier input and output nodes. Its static operation follows similar principles to those of Figure 14.4(d). When $z = 0$, transistors M_P and M_N are OFF and the circuit exhibits capacitive-input behavior. Positive currents are integrated in the input capacitor increasing voltage y_a and, consequently, decreasing y until the transistor M_N becomes conductive, drawing the input current and stabilizing the output. The other way around, M_P is the conductive transistor for negative input currents.

A common feature of the comparator circuits in Figure 14.4(c)–(e) is that the output voltage swings a rather limited interval of amplitude $\approx V_{TN} + |V_{TP}|$. Then, additional CMOS inverters in series with the output node may be necessary in order to restore the logic levels as shown in Figure 14.5(b).

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[7] Quiescent point is used across this chapter to denote the point around which the comparator gain is built. We assume that comparators are perfectly balanced when biased at the quiescent point and that detection happens around this point.

14.2.3. Regenerative Positive-Feedback Comparators

Although the very operation of voltage comparators consists of building voltage gain stages, there are significant differences among amplifiers themselves and comparators. Amplifiers are usually employed to achieve linear operation in closed-loop configurations, which requires careful compensation of the dynamic response to avoid unstable operation when feedback is applied. On the contrary, the dynamic of the gain mechanism employed for comparators does not even need to be stable in open loop. Actually, *positive feedback* can be employed to implement mechanisms with *unstable,*[8] very fast gain-building mechanisms [13]. Actually, in Section 14.3 it will be shown that regenerative comparators are inherently faster than other types.

Consider, for illustration purposes, the incorporation of positive feedback to single-step comparators. Figure 14.6(a) shows a circuit implementation where positive feedback action is exercised by the OTA, whose small-signal transconductance is g_{mpf}, during the *active* clock phase ϕ_a. At this point, let us accept without explanation the use of clock-controlled switches in this circuit. Note that the controlling clock has two non-overlapped phases, as shown in Figure 14.6(a). Comparisons take place only when the clock phase ϕ_a is in the

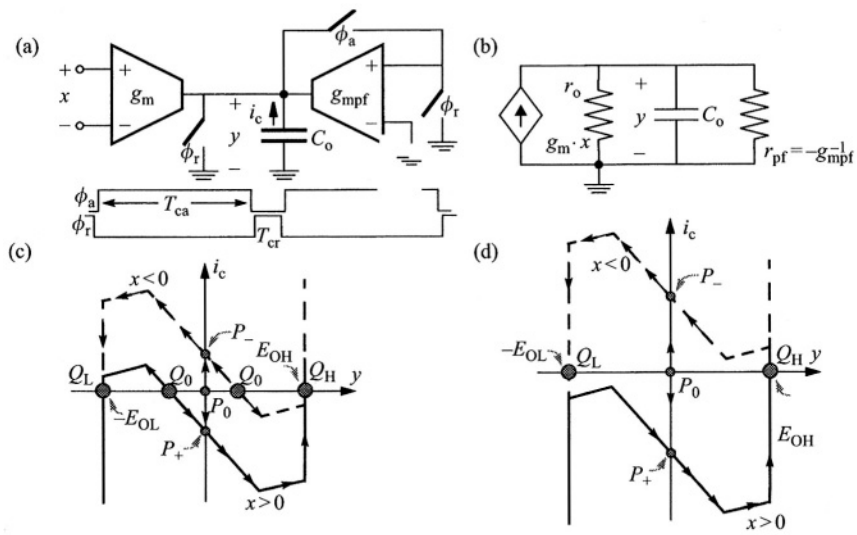


Figure 14.6. Including positive feedback into single-step comparators.

[8] Here unstable means that the small-signal model around the quiescent point has poles in the right-hand side of the complex frequency plane.

high state, and consequently switches controlled by this phase are ON, while the others are OFF.

Figure 14.6(b) shows a first-order model to represent the behavior of Figure 14.6(a) around its quiescent point $y = 0$, when the clock phase ϕ_a is in the high state. Positive feedback is modeled by the negative resistance $r_{pf} = -g_{mpf}^{-1}$ which counterbalances the negative feedback action exercised by the resistance r_o. Provided that $g_{mpf} > g_o = r_o^{-1}$, the global feedback around the quiescent point is positive and, hence, the global behavior is unstable.

For better understanding of the qualitative operation of Figure 14.6(a), it is helpful to consider the plots of Figure 14.6(c) and (d). There, we depict the approximate resistive characteristics "seen" by capacitor C_o during the comparison phase due to the combined action of the two OTAs of Figure 14.6(a), and taking into account the OTA non-linearities.[9] Figure 14.6(c) corresponds to "small" values of the input x, whereas Figure 14.6(d) corresponds to "large" input values. The actual characteristic seen in each case depends on the sign of the input applied during the comparison phase; continuous traces correspond to positive input trajectories whereas dashed traces represent negative input trajectories. Independently of the input being large or small, positive or negative, during the *reset* phase the output is driven to the central point P_0, for which $y = 0$. This defines the quiescent point, where the small-signal model of Figure 14.6(b) is applicable.

Consider now that a "small" input is applied during the comparison phase. For $x > 0$, the capacitor sees the bottom characteristics of Figure 14.6(c) which includes three *equilibrium points*:[10] two stable, Q_L and Q_H, and the other unstable, Q_0. Because the capacitor charge cannot change instantaneously, the initial state at $y = 0$ corresponds to the point P_+ on the characteristic, which is located on the right-hand side of Q_0. From P_+ the repulsion action exercised by Q_0, precludes the left-hand stable equilibrium at Q_L to be reached, and the trajectory becomes attracted toward the right-hand stable equilibrium at Q_H, where $y = E_{OH}$. On the other hand, for $x < 0$, the central point pushes the trajectory toward the equilibrium at Q_L, where $y = -E_{OL}$. In both cases, the dynamic evolution around the central point is governed by the model of

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9 Here two basic non-linearities are considered, namely saturation of the OTA transconductance and saturation of the OTA output voltage [14].

10 At the intersection points the current through the capacitor is null and hence $dy/dt = 0$. These points are equilibrium states where $y(t) = cte$ and the circuit may remain static [15]. In practice, the circuit will actually remain static as long as the slope of the i_o vs y curve is positive around the point (stable equilibrium) and will not otherwise (unstable equilibrium). Starting from any arbitrary initial value of y, the circuit trajectory toward steady-state is determined by the attraction exercised by stable equilibrium points, and the repulsion exercised by unstable equilibrium points.

Figure 14.6(b) and, hence, realized at high speed due to the positive feedback action.

For "large" input values, the characteristic of Figure 14.6(d) applies. In such a case, there is only one stable equilibrium point for each sign of x, and the description of the transient evolution is similar to the previous one.

Note that the qualitative description above remains valid for whatever input magnitude. It suggests that, unlike for single-step topologies, the resolution of this type of comparators is not limited by the static gain. Unfortunately, the offset limitation is more important here [14].

At this point, we have the ingredients needed to understand why the circuit of Figure 14.6(a) is clocked: if the circuit were operated in continuous-time instead of discrete-time (DT), *hysteresis* would arise. In order to understand this, let us return to Figure 14.6(c) and (d). Consider that at a certain time instant, a positive input is applied such that the circuit is at the stable equilibrium point Q_H, and consequently the output is high. Assume now that the input decreases. Figure 14.6(c) tells us that Q_H remains as a stable equilibrium point even when the input becomes negative; only for large enough negative inputs, Q_H ceases to be a stable equilibrium point, as Figure 14.6(d) illustrates. It means that large enough negative values must be applied to counterbalance the circuit "inertia" to remain in the high state and, thereby, force its evolution toward the low state. This inertia, which is a consequence of the circuit memory, is eliminated by employing switches to place the circuit at the unstable equilibrium point P_0 before comparison is actually made [14]. This operation, realized during the reset clock phase, is equivalent to erasing the memory of the circuit and it is the key to guarantee that hysteresis will not appear.

DT regenerative comparators are commonly built by cross-coupling a pair of inverters to form a *latch* – a circuit structure often used as sense amplifier in dynamic RAMs [16]. Figure 14.7(a) shows the concept of regenerative comparison based on a latch, where the blocks labeled "τ" model delays in the transmission of voltages around the feedback loop. The inverters amplify the differential input $x_{a+} - x_{a-}$ to obtain the saturated differential output $y_+ - y_-$ according to the characteristics drawn with solid line in Figure 14.7(b). During the reset phase (ϕ_r high), the differential input is stored at the input sampling capacitors and the circuit is driven to the central state Q_0. During the active phase (ϕ_a high), the differential input is retrieved, forcing an initial state either on the right ($x > 0$) or on the left ($x < 0$) of Q_0. From this initial state, the action of positive feedback forces the output to evolve either toward Q_H, for $x > 0$, or toward Q_L, for $x < 0$, as illustrated through the gray-line trajectories in Figure 14.7(b).

Figure 14.8(a)–(d) shows some examples of CMOS latches reported in literature [17–21]. For those in Figure 14.8(a) and (b), transistors M_{NB} and M_{PB} are OFF during the reset phase, so that the latch is disabled. In this phase,

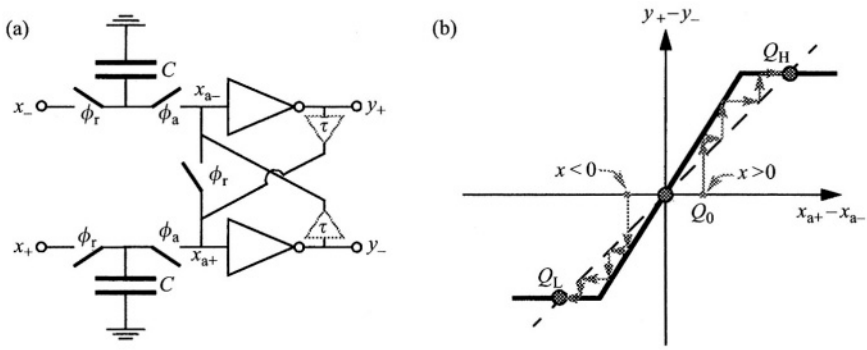


Figure 14.7. Conceptual latch circuit model and illustrative dynamic operation.

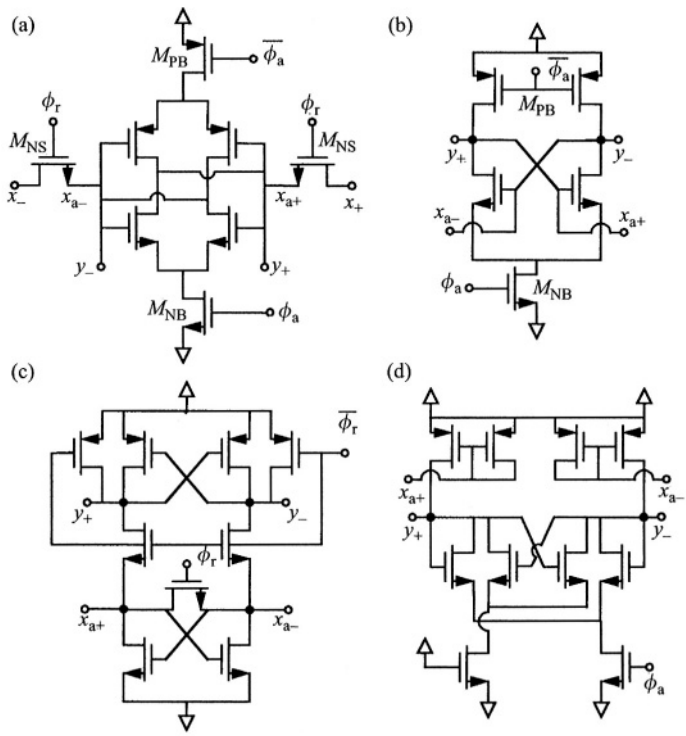


Figure 14.8. Some CMOS latches.

nodes x_{a+} and x_{a-} are in high-impedance state and input voltages can be sampled therein; transistors M_{NS} in Figure 14.8(a) are used for that purpose. Next, the voltage difference is amplified when the latch is enabled during the active phase. Alternatively, nodes x_{a+} and x_{a-} can be driven during the active phase

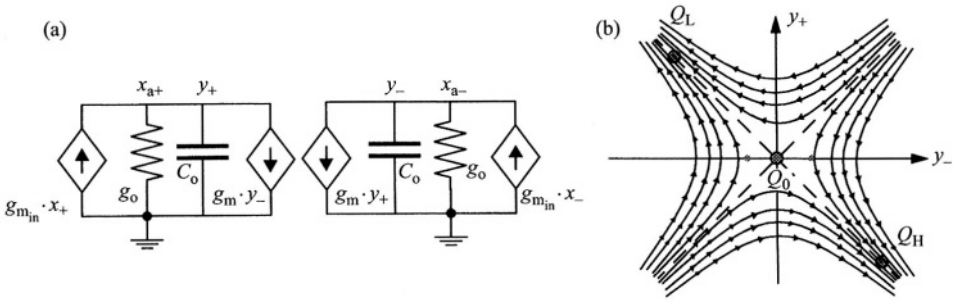


Figure 14.9. (a) Small-signal model around the quiescent point and (b) state diagram.

with currents obtained from the input voltages by means of transconductors. This is the unique excitation alternative for the latches of Figure 14.8(c) and (d).

Figure 14.9(a) shows a first-order small-signal model for the CMOS latches of Figure 14.8(c) and (d) around the quiescent point. The action of the excitation transconductors mentioned above, represented by transconductances $g_{m_{in}}$, is also modeled for completeness, although they are not shown in the actual CMOS circuits of Figure 14.8. Figure 14.9(b) shows the state diagram (y_+ vs y_-) with the three equilibrium points of the system[11] and different dynamic trajectories around the quiescent point. It is seen that these trajectories are "separated" by the bisecting lines so that half of the plane converges toward Q_H and the other half toward Q_L. Hence, following the setting of the system at Q_0 during reset phase, the unbalance established during comparison phase combined with the separating action exercised by the unstable equilibrium point will force a transient evolution toward the correct stable equilibrium point.

14.2.4. Pre-Amplified Regenerative Comparators

Ideally, the static resolution of regenerative comparators is unlimited; that is, even arbitrarily small input unbalances could be detected.[12] In practice, their resolution is limited by dissymmetries and other second-order phenomena. Moreover, errors caused by dissymmetries are much larger in comparators with positive feedback than in other types [1, 9]. Thus, in order to keep the

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11 The small-signal model only accounts for the central, unstable equilibrium point Q_0. Nonlinearities must be brought into the picture in order to account for the stable equilibrium points Q_L and Q_H.

12 Even in such an ideal case, detection of infinitely small inputs would require infinitely long detection times, as the formulae of the next section will show.

speed advantages of a regenerative comparator and simultaneously improve its resolution, a pre-amplifier is usually placed in front of the regenerative core.

This is the strategy employed in the conceptual schematic of Figure 14.10(a). There, the inverters in the latch are self-biased during the reset phase. During the active phase, the input signal $x_+ - x_-$ is first amplified by a factor A_{in}, and then added to the quiescent input voltages of the inverters prior to enabling the positive feedback loop. Input signal amplification occurs during the first part of the active phase (ϕ_{a1} high). Positive feedback is enabled during the last portion of the active phase (ϕ_{a2} high), whose rising edge is delayed with respect to that of ϕ_{a1} in order to guarantee that a *large enough* input unbalance is built prior to closing the positive feedback loop. Thus, the resolution improvement of this architecture as compared to the one without pre-amplifier is roughly proportional to A_{in}.

Preamplification is also the role played by the two transconductances labeled $g_{\text{m}_{\text{in}}}$ in the model of Figure 14.9(a). Figure 14.10(b) shows a CMOS circuit implementation of this concept using the CMOS latch of Figure 14.8(c) [17].

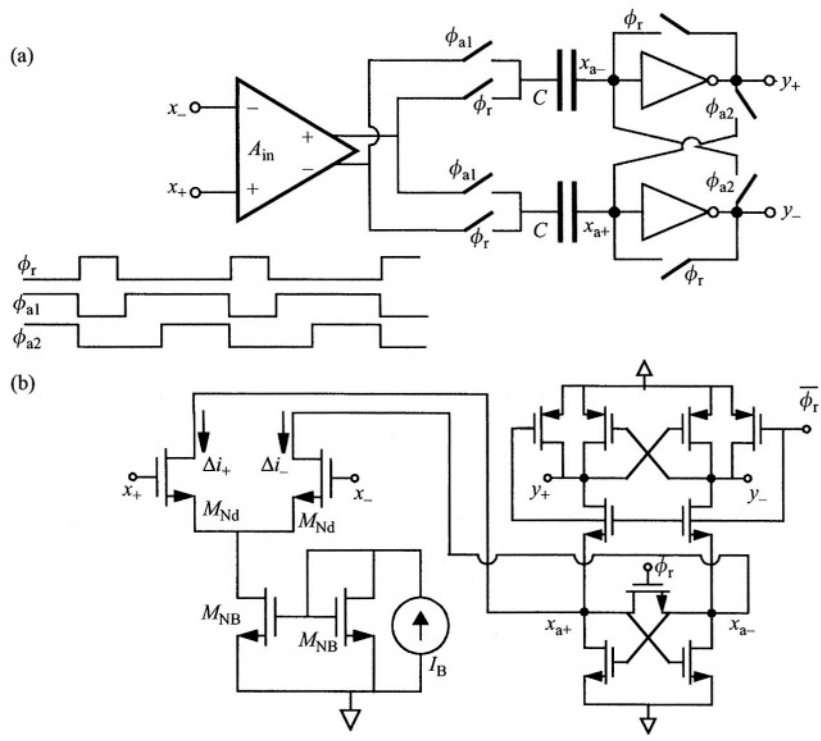


Figure 14.10. Pre-amplified regenerative comparators.

14.3. Architectural Speed vs Resolution Trade-Offs

The resolution–speed trade-off can be studied at different levels. At the transistor level, we would like to know how speed and resolution are influenced by design parameters such as transistor sizes and bias current. Instead, this section follows another approach where comparators are characterized by high-level parameters, such as static gain, unitary time constant, etc., and the trade-off is formulated as a function of these parameters. This approach enables us to draw comparisons among the architectures.

For any of the comparator topologies mentioned so far, for instance Figure 14.4, let us assume that the comparator is perfectly balanced for $x = 0$; that is, that the output is in the quiescent point with y = 0. It means that input offsets are ignored by now. Let us then consider that a step stimulus of value Δ_d is applied at $t = 0$. By using small-signal models around the quiescent point, the output waveform can be calculated as

$$y(t) = \Delta_d \cdot k_d(t) \tag{14.9}$$

where $k_d(t)$, called *dynamic gain,* depends upon the actual comparator structure being considered. For each structure, $k_d(t)$ reflects the time needed to build a given amount of gain. Particularly, for a given Δ_d we are interested in knowing the time needed to build the necessary gain so that the output reaches the restoring logic level. This time, called *quiescent comparison time* T_c, is calculated from

$$E_{OH} = \Delta_d \cdot k_d(T_c) \tag{14.10}$$

This equation defines a resolution–speed trade-off which is different for each architecture. Generally speaking, the larger T_c – that is, the slower the comparator – the smaller Δ_d – that is, the more accurate the comparator. However, the actual dependence between T_c and Δ_d changes from one architecture to another, as the curves depicted in Figure 14.11 suggest. The meaning of these curves is explained in the following sections.

14.3.1. Single-Step Comparators

Let us first focus on single-step voltage comparators, and assume that the dynamic behavior around the quiescent point is represented by the model of Figure 14.2(d). This first-order model accounts for the static gain and the unitary frequency of the gain mechanism. Consider that the capacitor C_o in Figure 14.2(d) is discharged at $t = 0$ and that a step excitation of amplitude Δ_d is applied around the input threshold voltage. The output waveform is

$$y(t) = \Delta_d \cdot k_s \cdot \left(1 - e^{-t/\tau_o}\right) \quad \tau_o \equiv \frac{C_o}{g_o} \tag{14.11}$$

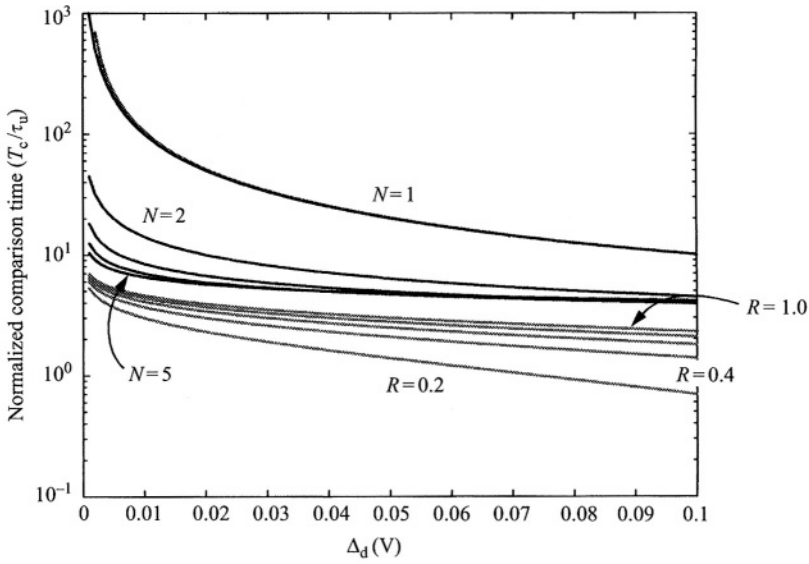


Figure 14.11. Illustrating the resolution–speed trade-off.

Assume now that Δ_d is large enough in comparison with Δ_s defined in Figure 14.1(b), so that $\Delta_d \cdot k_s \gg E_{OH}$. Then, analysis of equation (14.11) shows that $y(t)$ reaches the restoring level E_{OH} into a small fraction of τ_o. Taking this into account, equation (14.11) can be series-expanded and approximated to obtain

$$y(t) \approx \Delta_d \cdot k_s \cdot \frac{t}{\tau_o} \tag{14.12}$$

Comparing this result with equation (14.9), the dynamic gain is expressed as

$$k_d(t) = k_s \cdot \frac{t}{\tau_o} = \frac{g_m}{g_o} \cdot \frac{g_o}{C_o} \cdot t \equiv \frac{t}{\tau_u} \tag{14.13}$$

where $\tau_u \equiv C_o/g_m$ is the *unitary time constant* of the amplifier. Correspondingly, the resolution–speed trade-off is given by

$$\Delta_d \cdot \frac{T_c}{\tau_u} \approx E_{OH} \tag{14.14}$$

The curve labeled as $N = 1$ in Figure 14.11 illustrates this trade-off for $E_{OH} = 1\,V$.

As Δ_d decreases, equation (14.14) shows that T_c increases at the same rate. However, this equation is valid only if $\Delta_d \cdot k_s \gg E_{OH}$. As the input approaches

the static resolution limit, that is, as $\Delta_d \to \Delta_s \equiv E_{OH}/k_s$, it is not possible to assume $T_c \ll \tau_o$, and the trade-off is recalculated as

$$\Delta_d \cdot \frac{T_c}{\tau_u} = E_{OH} \cdot \left[\left(\frac{k_s \cdot \Delta_d}{E_{OH}} \right) \ln \frac{1}{1 - (1/k_s \cdot E_{OH}/\Delta_d)} \right] \tag{14.15}$$

Consider $\Delta_d \approx \Delta_s \cdot (1 + \varepsilon)$ with $\varepsilon \ll 1$. Equation (14.15) can be simplified to obtain a relationship between the static gain and the time needed to obtain such limiting sensitivity:

$$\frac{T_c}{\tau_u} = A_0 \cdot \ln \left(\frac{1}{\varepsilon} \right) \tag{14.16}$$

where for the sake of homogeneity with the text in the following subsection, the static gain has been renamed as A_0. In the limit, as $\Delta_d \to \Delta_s$ and $\varepsilon \to 0$, it follows that $T_c \to \infty$. Let us consider for illustration purposes an example with $k_s = 2 \times 10^3$, $\tau_u = 10\,\text{ns}$ and $E_{OH} = 1\,\text{V}$. Thus, $\Delta_d = 10\,\text{mV}$ requires from equation (14.14) $T_c \approx 1\,\mu\text{s}$, while $\Delta_d = 1\,\text{mV}$ requires from equation (14.15) $T_c \approx 14\,\mu\text{s}$. On the other hand, if the static resolution limit has to be approached within 1%, equation (14.16) yields $T_c \approx 92\,\mu\text{s}$.

Summing up, we can state that the single-step comparator, under normal operation conditions (i.e. $\Delta_d \ll E_{OH}$), reacts at much lower speed than the underlying gain mechanism, that is, T_c is much larger than τ_u.

14.3.2. Multistep Comparators

Let us focus now on multistep comparators – see Figure 14.4. Consider for illustration purposes that all stages are identical, ignore again the input offset voltages, and assume that all capacitors are discharged at $t = 0$, and that an input step valued Δ_d is applied at that time instant. Laplace-domain analysis shows that

$$Y(s) = \left(\frac{k_s}{1 + s \cdot \tau_o} \right)^N \cdot \frac{\Delta_d}{s} \qquad \tau_o \equiv \frac{C_o}{g_o} \tag{14.17}$$

Assuming $\Delta_d \cdot k_s^N \gg E_{OH}$ results in $T_c \ll \tau_o$, and hence equation (14.17) can be simplified into,

$$Y(s) \cong \Delta_d/(s^{N+1}\tau_u^N) \Rightarrow y(t) \approx \frac{\Delta_d}{\tau_u^N} \cdot \frac{1}{N!} \cdot t^N \tag{14.18}$$

and the resolution–speed trade-off becomes

$$\Delta_d \cdot \left(\frac{T_c}{\tau_u} \right)^N \approx N! \cdot E_{OH} \tag{14.19}$$

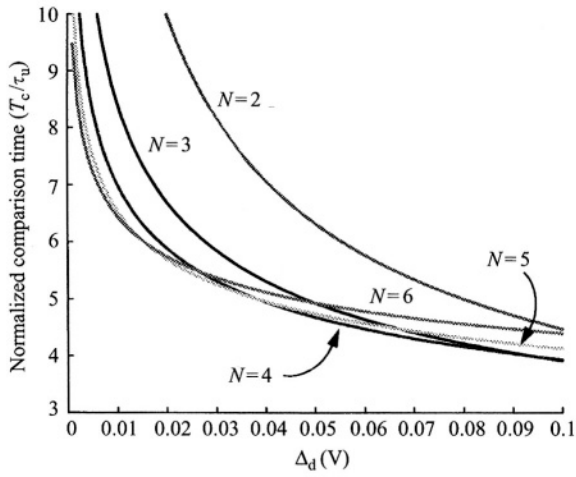


Figure 14.12. Zoom of resolution–speed trade-off for multistep comparators.

The curves corresponding to $N = 2$ and $N = 5$ in Figure 14.11 illustrate this trade-off for $E_{OH} = 1\,V$. Note that the multistep architecture obtains smaller values of T_c than the single-step architecture. For instance, for $\tau_u = 10\,ns$, $E_{OH} = 1\,V$ and $\Delta_d = 10\,mV$ equation (14.19) yields $T_c \approx 141$ ns for $N = 2$, $T_c \approx 65$ ns for $N = 5$, and $T_c \approx 67$ ns for $N = 8$ – always smaller than for the single-step case.

Figure 14.12 is a zoom of the resolution–speed curves for the multistep comparator. It shows that, for each Δ_d, there is an optimum value of N that minimizes T_c. For $\Delta_d > (10^{-3} \cdot E_{OH})$ this optimum number is given by [9],

$$N_{opt} \approx 1.1 \cdot \ln\left(\frac{E_{OH}}{\Delta_d}\right) + 0.79 \qquad (14.20)$$

For instance, for $\Delta_d \approx 10^{-2} \cdot E_{OH}$, maximum speed is achieved by using $N = 6$. Using either less or more stages in the cascade results in slower operation.

14.3.3. Regenerative Comparators

Let us first consider Figure 14.6(a); assume the same conditions as in the previous section, and use the model of Figure 14.6(b) around the quiescent point. Assuming further that g_{mpf} is larger that $g_o = r_o^{-1}$ and defining

$g_{oeq} \equiv g_{mpf} - g_o$ yields

$$y(t) = \Delta_d \cdot \frac{g_m}{g_{oeq}} \cdot \left(e^{t(g_{oeq}/C_o)} - 1\right) \qquad k_d(t) = \frac{g_m}{g_{oeq}} \cdot \left(e^{t(g_{oeq}/C_o)} - 1\right) \tag{14.21}$$

By comparing these expressions with equations (14.11) and (14.14) and/or equation (14.15), we note that g_{oeq} contains a term which is proportional to a transconductance.[13] We can assume that $g_{oeq} \approx g_{mpf}$ and consider that $g_{mpf} = g_m$ so that

$$\Delta_d \cdot e^{T_c/\tau_u} \approx E_{OH} \tag{14.22}$$

Due to the exponential dependence, this equation anticipates much smaller values of T_c than those obtained from equations (14.14) and (14.19). This is confirmed by the curve labeled as $R = 1$ in Figure 14.11; the meaning of the parameter R will be explained below. In any case, the set of curves in Figure 14.11 confirm that regenerative comparators feature faster operation speed than either single-step or multistep comparators.

Note that, except for the influence of second-order effects, the operation described above is valid no matter how small the input signal magnitude is; only the input sign is meaningful. It means that ideally regenerative comparators might be capable of building infinitely large dynamic gain values – a feature shared neither by single-step nor by multistep comparators whose maximum dynamic gain is smaller than the static one. In either case, as Δ_d decreases, T_c increases according to

$$\frac{T_c}{\tau_u} \approx \ln\left(\frac{E_{OH}}{\Delta_d}\right) \tag{14.23}$$

which for $\Delta_d \to 0$ yields $T_c \to \infty$.

The previous analysis can be extended to a latch by using the small-signal model of Figure 14.9(a), which assumes full symmetry (equal positive and negative parameters) and can be represented by the following state equation,

$$\begin{aligned} C_o \cdot \frac{dy_+}{dt} &= -g_o \cdot y_+ - g_m \cdot y_- + g_{m_{in}} \cdot x_+ \\ C_o \cdot \frac{dy_-}{dt} &= -g_m \cdot y_+ - g_o \cdot y_- + g_{m_{in}} \cdot x_- \end{aligned} \tag{14.24}$$

By combining the two equations above, we have

$$C_o \cdot \frac{d(y_+ - y_-)}{dt} = g_m \cdot (Y_+ - y_-) - g_o \cdot (y_+ - y_-) + g_{m_{in}} \cdot (x_+ - x_-) \tag{14.25}$$

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[13] For any OTA, the transconductance g_m is usually much larger than the output conductance g_o.

In the right-hand side of this expression, the first term accounts for the positive feedback effect, the second one for the negative feedback, and the last term represents the input contribution. Further, consider $(g_m/g_o) \gg 1$. Then, assuming that the circuit is initialized at $t = 0$, so that $y(0) = y_+(0) - y_-(0) = 0$, and that a differential input step of value $\Delta_d \equiv x_+ - x_-$ is applied at this time instant, the differential output waveform can be approximated by

$$y(t) \equiv y_+(t) - y_-(t) \approx \Delta_d \cdot \frac{g_{m_{in}}}{g_m} \cdot e^{t(g_m/C_o)} \equiv \Delta_d \cdot \frac{g_{m_{in}}}{g_m} \cdot e^{(t/\tau_u)} \quad (14.26)$$

A similar equation is found when the latch is driven during the reset phase, establishing a voltage unbalance $y(0) = y_+(0) - y_-(0) \equiv \Delta_d$, and no input is applied during the comparison phase. In such a case,

$$y(t) \approx \Delta_d \cdot e^{t/\tau_u} \quad (14.27)$$

and the associated resolution–speed trade-off is represented by equation (14.22). On the other hand, from equation (14.26) the following resolution–speed trade-off is found

$$\Delta_d \cdot e^{T_c/\tau_u} \approx E_{OH} \cdot \frac{g_m}{g_{m_{in}}} \quad (14.28)$$

Figure 14.11 illustrates this trade-off for different values of $R \equiv g_m/g_{m_{in}}$.

The analysis above can be easily extended to pre-amplified regenerative comparators. Actually, equation (14.28) is representative of the behavior of the circuits belonging to this class. Bear in mind that this equation has been obtained for Figure 14.9(a), which is a first-order model of the pre-amplified regenerative comparator of Figure 14.10(b). By comparing this equation with equation (14.22), it can be concluded that pre-amplification relaxes the trade-off proportionally to the $g_{m_{in}}/g_m$ ratio, as anticipated. This result can be extended to the circuit of Figure 14.10(a), where the improvement will be proportional to A_{in}.

However, this is an oversimplified approach because it ignores the dynamic behavior of the circuit used for pre-amplification. More realistic calculations can be made by considering that the latch starts operating with some delay with respect to the pre-amplifier. Hence, by assuming that this delay is fixed, say of value T_{CP} and the pre-amplifier behaves as a single-step comparator, the following resolution–speed trade-off is derived:

$$\Delta_d \cdot \frac{T_{CP}}{\tau_u} \cdot e^{T_c/\tau_u} \approx E_{OH} \quad (14.29)$$

14.4. On the Impact of the Offset

Previous calculations have assumed that comparators are perfectly balanced at the quiescent point so that even arbitrarily small input signals drive the comparator output in the correct direction. However, in practice, there are different errors degrading such an ideal picture. Among these errors, the lack of symmetry of the comparator circuitry results in an equivalent input offset voltage [6]. This offset sets a limitation on the minimum achievable comparator resolution; input signals whose amplitude is smaller than the input offset voltage will not be properly detected by the comparator.

The offset has two different components. *Deterministic offset* is due to asymmetries of the comparator circuit structure itself; for instance, the FDOTAC structure of Figure 14.2(c) is symmetric, while the AOTAC structure formed of Figure 14.2(a) is asymmetric. Consequently, the output voltage at the quiescent point Y_Q will be typically different from zero, thus making $E_{os} = Y_Q/k_s$. However, because Y_Q could be, at worst, of the same order of magnitude as E_{OH}, the role played by the deterministic offset component is similar to that of the static gain. On the other hand, *random offset* contemplates asymmetries caused by random deviations of the transistor sizes and technological parameters, and it is observed in both asymmetrical and symmetrical circuit topologies. These deviations make nominally identical transistors become mismatched, the amount of mismatch being inversely proportional to the device area and directly proportional to the distance among them. Assuming that the area-dependent contribution dominates mismatch among devices,[14] the statistical variances of the deviations on the zero-bias threshold voltage and the intrinsic large-signal transconductance density between two nominally identical MOSTs are formulated as [22]:

$$\sigma^2(\Delta V_{T0}) \approx \frac{\alpha^2 V_{T0}}{W \cdot L}$$
$$\sigma^2\left(\frac{\Delta\beta_0}{\beta_0}\right) \approx \frac{\alpha_{\beta_0}^2}{W \cdot L} \tag{14.30}$$

where W and L are the channel width and length of the MOSTs, $\alpha_{V_{T0}}^2$ and $\alpha_{\beta_0}^2$ are technological constants,[15] and it has been assumed that parameter variations of individual transistors are non-correlated.

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[14] The distance contribution to mismatch accounts for the effect of process-parameter gradients on the wafer and can be largely attenuated through proper layout techniques (e.g. common-centroid structures).

[15] Typical values in a 0.5 μm technology are $\alpha_{V_{T0}}^2 \approx 10^{-5} V^2\,\mu m^2$ and $\alpha_{\beta_0}^2 \approx 10^{-4}\,\mu m^2$.

With equation (14.30) and the large-signal MOST model of Appendix, a simple variational analysis can be performed to estimate the random offset voltages of single-step topologies in terms of transistor dimensions, technological parameters and biasing conditions. It is worth noting that results are also extensible to multistep comparators because, as indicated in equation (14.6), the overall offset voltage is dominated by that of the front-end stage.

For the sake of conciseness, only the AOTAC structure, Figure 14.2(a), will be considered herein. In this topology, contributions to the random offset voltage arise from mismatches in the differential input pair, formed by transistors M_{Nd}, and imbalance in the active load circuitry, formed by transistors M_{Pl}. Such contributions can be estimated by calculating the input voltage required to compensate any current unbalance through the comparator branches as a result of transistor mismatch. Considering the differential pair mismatch alone, the variance of its contribution to the random offset is found to be

$$\sigma^2(E_{os})\big|_{DP} = \frac{2 \cdot \alpha^2_{V_{T0DP}}}{W_{DP} \cdot L_{DP}} + \frac{I_B \cdot n_{DP}}{4 \cdot \beta_{0DP}} \cdot \frac{\alpha^2_{\beta_{0DP}}}{W^2_{DP}} \tag{14.31}$$

and, in case of the active load alone, we have

$$\sigma^2(E_{os})|_{AL} = \beta_{0DP} \frac{2 \cdot \beta_{0AL} \cdot n_{DP}}{n_{AL}} \cdot \frac{L_{DP}}{W_{DP}} \cdot \frac{\alpha^2_{V_{T0AL}}}{L^2_{AL}} + \frac{I_B \cdot n_{DP}}{4 \cdot \beta_{0DP}} \cdot \frac{L_{DP}}{W_{DP}} \cdot \frac{\alpha^2_{\beta_{0AL}}}{W_{AL} \cdot L_{AL}} \tag{14.32}$$

Assuming that both contributions are uncorrelated, the variance of the random offset voltage of the AOTAC structure is, thus, obtained as

$$\begin{aligned} \sigma^2(E_{os}) &= \sigma^2(E_{os})|_{DP} + \sigma^2(E_{os})|_{AL} \\ &= \frac{k_1}{W_{DP} \cdot L_{DP}} + \frac{k_2 \cdot I_B}{W^2_{DP}} + \frac{k_3 \cdot L_{DP}}{W_{DP} \cdot L^2_{AL}} + \frac{k_4 \cdot L_{DP}}{W_{DP}} \cdot \frac{I_B}{W_{AL} \cdot L_{AL}} \end{aligned} \tag{14.33}$$

where parameters

$$\begin{aligned} k_1 &= 2 \cdot \alpha^2_{V_{T0DP}} \quad k_2 = \frac{n_{DP}}{4 \cdot \beta_{0DP}} \alpha^2_{\beta_{0DP}} \\ k_3 &= \frac{2 \cdot \beta_{0AL}}{\beta_{0DP}} \cdot \frac{n_{DP}}{n_{AL}} \cdot \alpha^2_{V_{T0AL}} \quad k_4 = \frac{I_B \cdot n_{DP}}{4 \cdot \beta_{0DP}} \cdot \alpha^2_{\beta_{0AL}} \end{aligned} \tag{14.34}$$

are constant for a given technology.

This result can be exploited to examine the resolution–speed trade-off in terms of design variables and technological parameter variations as follows. Let us define the comparator *dynamic resolution* as $\xi_d = |E_{os}| + \Delta_d$, in consonance with the static resolution defined in equation (14.2). Then, each of the contributing terms to ξ_d is expressed in terms of the physical parameters

involved in the topology. On the one hand, it can be conveniently assumed that $|E_{os}| \approx 3\sigma(E_{os})$, where $\sigma(E_{os})$ is obtained by square-rooting equation (14.33). On the other, taking into account equation (14.14) and Table 14.1, we can express Δ_d as

$$\Delta_d \approx \frac{E_{OH} \cdot \tau_u}{T_c} = \frac{E_{OH}}{T_c} \cdot \frac{[C_L + \nu_{DP} \cdot W_{DP} \cdot C_{GD0DP} + \nu_{AL} \cdot W_{AL} \cdot C_{GD0AL}]}{\sqrt{2 \cdot \frac{\beta_{0DP}}{n_{DP}} \cdot \left(\frac{W}{L}\right)_{DP} \cdot I_B}} \tag{14.35}$$

Hence, ξ_d can be defined as a function of T_c, and also of the device dimensions and biasing. Figure 14.13 illustrates such a relationship by individually representing ξ_d against the variables implicated. It is worth pointing out that

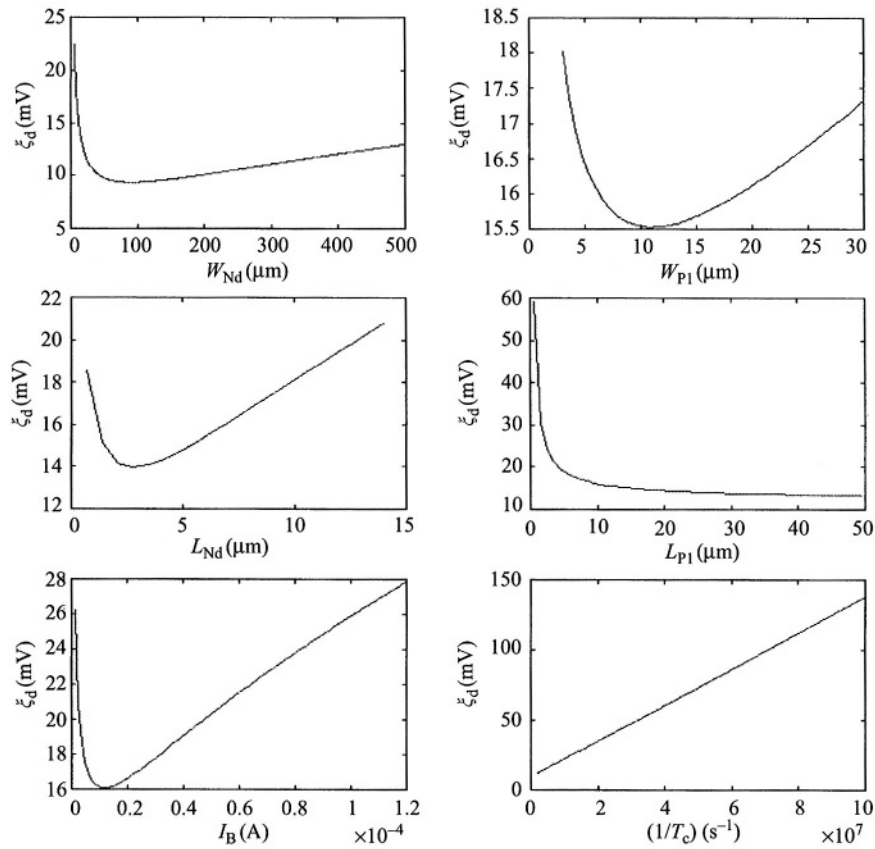


Figure 14.13. Illustration of the resolution–speed trade-off in terms of device dimensions and biasing.

such representations exhibit minima that indicate the values of corresponding variables for which an optimum resolution–speed performance can be obtained.

Let us now briefly consider the effect of asymmetries on the performance of DT regenerative comparators. Spurious differential signals, coupling between the two latch branches and mismatches between their parameters preclude correct amplification of small Δ_d values. Their influence can be assessed by studying the equilibrium points, eigenvalues and eigenvectors of the state equation:

$$\begin{aligned}
&(C_{o+} + C_c) \cdot \frac{dy_+}{dt} \\
&\quad = -g_{o+} \cdot y_+ - g_{m+} \cdot y_- + g_{m_{in+}} \cdot x_+ + g_{m+} \cdot \frac{E_{os}}{2} + C_c \cdot \frac{dy_-}{dt} \\
&(C_{o-} + C_c) \cdot \frac{dy_-}{dt} \\
&\quad = -g_{m-} \cdot y_+ - g_{o-} \cdot y_- + g_{m_{in-}} \cdot x_- - g_{m-} \cdot \frac{E_{os}}{2} + C_c \cdot \frac{dy_+}{dt}
\end{aligned} \tag{14.36}$$

where C_c must be added in Figure 14.9(a) in order to model the coupling between the two output nodes. This is out of the scope of this chapter and only some remarks will be given. Note from equation (14.36) that the influence of the offset voltage E_{os} is similar to that observed in single-step and multistep comparators. However, asymmetries between transconductances g_{m+} and g_{m-}, as well as between capacitors C_{o+} and C_{o-}, produce much larger errors for regenerative comparators than for single-step and multistep comparators. It can be shown that the error depends on the common-mode value of the input signal $x_{cm} = (x_+ + x_-)/2$ [12]. For zero common-mode, equation (14.36) does not reveal any limitation on Δ_d. However, as the common-mode increases up to half of the swing range, $|\Delta_d|$ has to be larger than $\approx 30\,\text{mV}$ for correct codification of the input signal polarity. This value increases up to $\approx 50\,\text{mV}$ if 10% mismatches are considered for transconductances and capacitances. Clearly, this poses a hard constraint on the comparator resolution – not shared by either single-step or multistep comparators. As it was already mentioned, this problem is overcome by placing a pre-amplifier in front of the regenerative core and using offset-compensation techniques.

14.5. Offset-Compensated Comparators

Although input offset voltage can be compensated through transistor sizing, these techniques can hardly obtain offsets lower than a few millivolts – not small enough for many practical applications. This drawback can be overcome by adding offset-cancelation circuitry; thus residual offset values as small as

0.1 mV can be obtained [23]. Out of the different offset-cancelation strategies – component trimming, error integration and feedback through an offset nulling port, etc. – here we focus only on the use of dynamic biasing.

14.5.1. Offset-Compensation Through Dynamic Biasing

A simple, yet efficient offset correction technique uses dynamic self-biasing in order to, first, extract and store the offset, and then annul its influence [24–25]. Figure 14.14(a) and (c) shows the circuit implementation of this technique for single-ended and FDOTAs, respectively. As it can be seen, both circuits operate in DT, under the control of a clock with two non-overlapped phases as indicated in Figure 14.14(a). When the clock phase ϕ_a is in the low state, and correspondingly ϕ_r is in the high state, switches controlled by ϕ_r are ON, the others are OFF, and the comparator is *self-biased* – reset phase. In this phase, referring to Figure 14.14(a), the output voltage evolves toward a steady-state value $x_{a-}|_r = E_{os}\cdot(1+k_s^{-1})$ defined by the intersection of the amplifier transfer characteristic and the bisecting line $y = x_{a-}$, as Figure 14.14(b) illustrates. Provided that the *reset* interval is long enough for the transient to vanish, this value is stored at capacitor C, so that $v_{C_r} = x_+ - x_{a-}|_r$. Note that for $k_s \gg 1$ it yields $x_{a-}|_r \approx E_{os}$; hence, during the reset phase, the plate of the capacitor

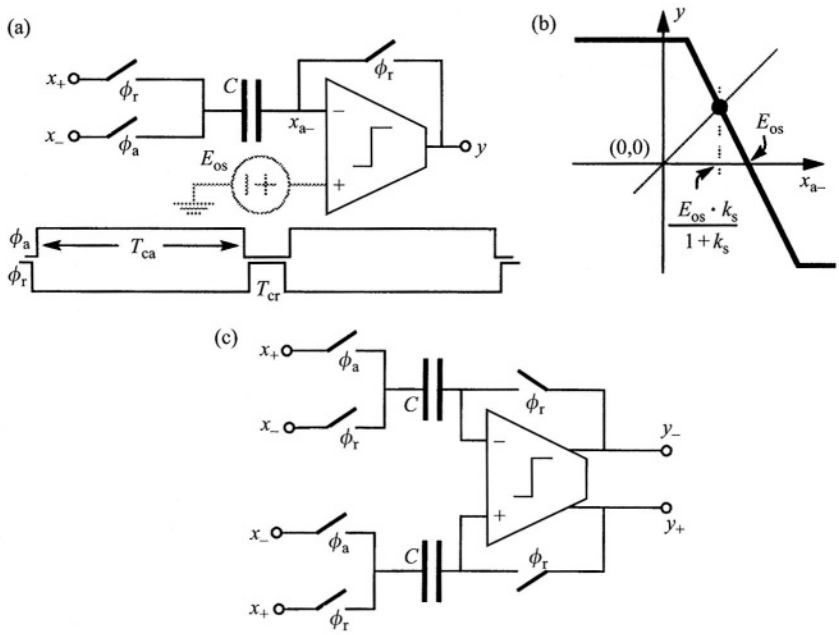


Figure 14.14. Offset cancelation in single-step voltage comparators.

connected to the non-inverting terminal of the OTA samples a voltage very close to the offset.

On the other hand, when ϕ_a is in the high state, and correspondingly ϕ_r is in the low state, switches controlled by ϕ_r are OFF, the others are ON, and C keeps its charge – comparison or active phase. In this phase, the comparator input $x_a \equiv x_{a+} - x_{a-}$ evolves to a steady-state $x_a = E_{os} - (x_- - v_{C_r}) = E_{os} - x_{a-}|_r + (x_+ - x_-)$, where the offset is subtracted from its previously sampled voltage. This results in the following static resolution expression:

$$\xi_S \approx \frac{|E_{os}|}{1+k_s} + \frac{E_{OH}}{k_s} = \frac{|E_{os}|}{1+g_m/g_o} + E_{OH} \cdot \frac{g_o}{g_m} \qquad (14.37)$$

which shows that the offset error is attenuated by a factor $1 + k_s$ as compared to the uncompensated comparator – see equation (14.2).

The circuits in Figure 14.14 correct the offset by sampling-and-holding its value at the comparator input node. Alternatively, the offset can be compensated through a sample-and-hold operation at the output node. In the circuit of Figure 14.15(a) such an operation is realized in the voltage domain. During the reset phase, the output offset voltage $k_s \cdot E_{os}$ is stored at the node y_a, while the output node is tied to the analog ground. Then, during the active phase, the inputs are applied yielding $y_a = k_s \cdot E_{os} + k_s \cdot (x_+ - x_-)$ and since no current is circulating through the capacitor C, $y = k_s \cdot (x_+ - x_-)$. Obviously, for proper offset correction k_s must be low enough to guarantee that the OTA remains operating within its linear region, that is, that its output is not saturated during the reset phase. The circuit of Figure 14.15(b) employs a different offset storage mechanism that overcomes this problem. There, the output offset current, instead of the voltage, is stored during the reset phase, and then subtracted during the comparison phase. Current storage is realized by transistor M_{OS}, which operates as a current memory. Note that during the reset phase this transistor operates as a nonlinear resistor, setting the OTA output node at low impedance. This yields a significant attenuation of the voltage gain

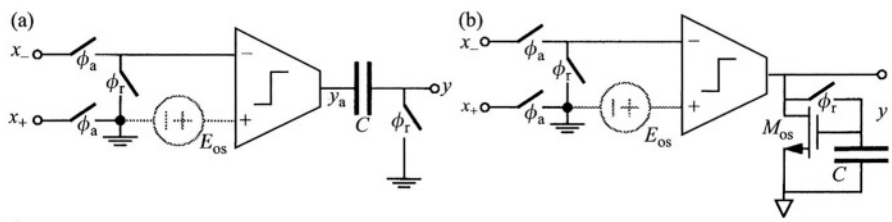


Figure 14.15. Offset compensation through storage at the output node: (a) voltage storage and (b) current storage.

during the reset phase, thereby reducing the excursions of the output voltage and guaranteeing operation within the OTA linear region.

14.5.2. Offset Compensation in Multistep Comparators

Dynamic self-biasing can be also applied to cancel out the offset of multistep comparators. However, unless compensation circuitry is added, the high-order dynamics will cause instabilities when a direct feedback connection is established between the overall output node and the negative input – similar to the problem found in two-stage opamps [6,26]. Instabilities can be avoided by making each stage to store its own offset, as shown in Figure 14.16, so that only second-order offset terms generated at the different stages remain. These offset terms can be further attenuated through a proper sequential timing of the switches used for self-biasing. The inset of Figure 14.16 shows this timing. Note that the stages are switched ON at different, consecutive time instants. Consequently, the residual offset of each stage is stored at the input capacitor of the next one while this latter remains grounded, and hence the output remains unaltered. In this way only the residual offset – see next section – of the last stage $|E_{osdN}|$ contributes to the output. Since this offset is amplified only by the last stage itself, while the signal is amplified by all the stages, the following

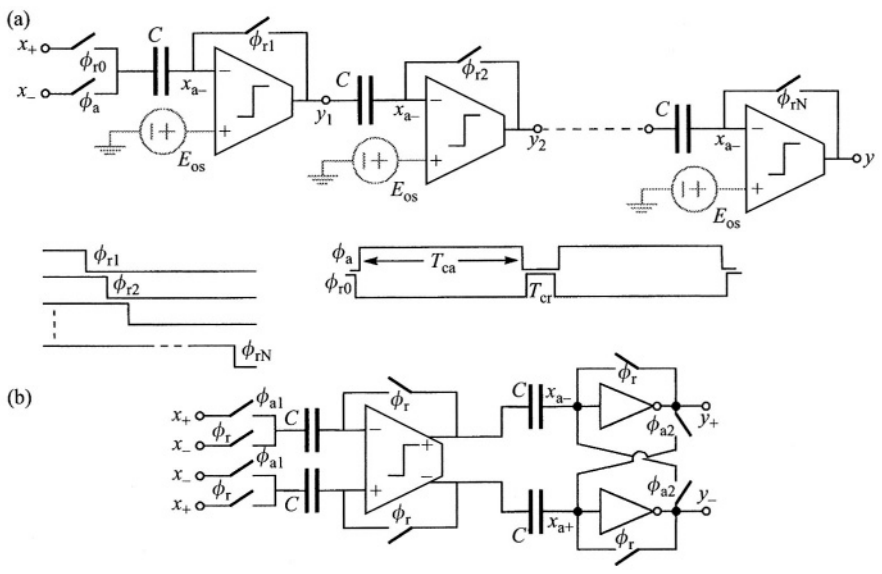


Figure 14.16. Offset compensation in multistep voltage comparators.

expression is obtained for the static resolution:

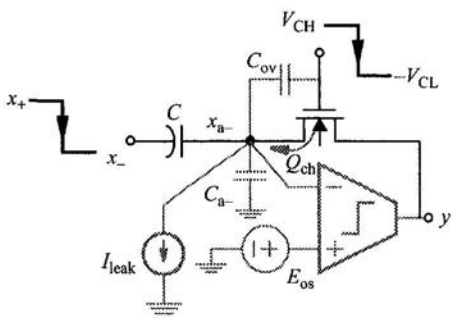
$$\xi_s \approx \frac{|E_{osdN}|}{k_s^{N-1}} + \frac{E_{OH}}{k_s^N} \tag{14.38}$$

Offset compensation applies also to multistep topologies formed by cascading a preamplifier and a latch. It is illustrated through the circuit depicted in Figure 14.16(b) consisting of the cascade of a self-biased single-step comparator and a self-biased latch [9,27].

14.5.3. Residual Offset and Gain Degradation in Self-Biased Comparators

There are several second-order phenomena that modify the voltage stored at node x_{a-} in Figure 14.14(a), and consequently degrade the static resolution of self-biased comparators. The two most important effects that take place during the ON $\rightarrow$ OFF transition of the reset feedback switch, are: (a) the feedthrough of the clock signal that controls this switch and (b) the injection of its channel charge. They make the voltage stored at note x_{a-} experiment a finite jump during the ON $\rightarrow$ OFF transition so that its value at the active phase differs from that stored during the reset phase, that is, $x_{a-}|_a \approx x_{a-}|_r - \Delta x_{a-}$. Also, during the active phase this value continues degrading due to the switch leakage current, I_{leak}. Figure 14.17 shows a simplified model to evaluate all these degradations. In addition to the nominal capacitor C, this model includes a parasitic capacitor, C_{a-}, between node x_{a-} and ground, and a parasitic capacitor, C_{ov}, between node x_{a-} and the control terminal of the feedback switch. Analysis using this model provides the following expression for the static resolution:

$$\xi_s \approx |V_{CH} + V_{CL}| \cdot \frac{C_{ov}}{C} + \frac{|Q_{ch}|}{C} + \frac{|I_{leak}|}{C} \cdot t + \frac{|E_{os}|}{\alpha_C \cdot (1 + k_S)} + \frac{E_{OH}}{\alpha_C \cdot k_S} \tag{14.39}$$



$$Q_{ch} = C_{ox} \cdot W_S \cdot L_S \left(V_{CH} - V_{T0} - n \cdot \frac{E_{os} \cdot A_o}{(1 + A_o)} \right)$$

Figure 14.17. Showing the feedthrough and the leakage current influence.

where $\alpha_C = C/(C + C_{ov} + C_{a-})$; V_{CH} and V_{CL} are, respectively, the high and low state levels of the clock signal; Q_{ch} is the charge accumulated in the switch channel when it is ON (during the reset phase), and t is the time measured from the instant when the ON → OFF transition happens. Note that equation (14.39) shows a residual offset term,

$$|E_{osd}| = |V_{CH} + V_{CL}|\frac{C_{ov}}{C} + \frac{|Q_{ch}|}{C} + \frac{|I_{leak}|}{C}t \qquad (14.40)$$

that is not attenuated by the comparator gain. If capacitance C is chosen very small, $|E_{osd}|$ may become larger than the original offset $|E_{os}|$. Also, small values of this capacitance may result in small values of α_C, thus making the last term in equation (14.39) increase, and producing additional resolution degradation.

The above equation shows that resolution degradations caused by residual offset are attenuated by increasing C and decreasing C_{ov}, Q_{ch} and I_{leak}. These three latter parameters are related to the ON resistance of the transistor switch. On the one hand,

$$Q_{ch} = \frac{1}{\mu} \cdot \frac{L_S^2}{R_{ON}} \qquad (14.41)$$

On the other, both C_{ov} and I_{leak} are proportional to the width W_S of the transistor switch, and hence inversely proportional to R_{ON}. Thus, the measures for reducing the residual offset make this resistance increase; consequently, the time constants increase as well and a resolution–speed trade-off appears.

14.5.4. Transient Behavior and Dynamic Resolution in Self-Biased Comparators

During the active phase of self-biased comparators, the transient response follows an exponential behavior similar to equation (14.11); the difference is that the static resolution, k_S, is now attenuated by α_C – see equation (14.39). Hence, the resolution–speed trade-off discussed in relation to equation (14.15) also applies in this case.

On the other hand, another trade-off stems from the transient during the reset phase, related to the onset of an additional residual offset component. The dynamic behavior within the reset phase can be calculated using the model of Figure 14.18(a). Two different transients are observed. First of all, there is a very fast charge redistribution transient, dominated by the ON resistances of the switches. The output value $y(0)$ at the end of this transient will be, at worst, equal to one of the saturation levels. Let us assume $y(0) = E_{OH}$. From this value, the output evolves toward the steady-state located at $E_{os} \cdot (1 + k_s^{-1})^{-1}$ through a second transient which is dominated by the comparator dynamics. Figure 14.18(b) provides a global view of this second transient. It consists of a

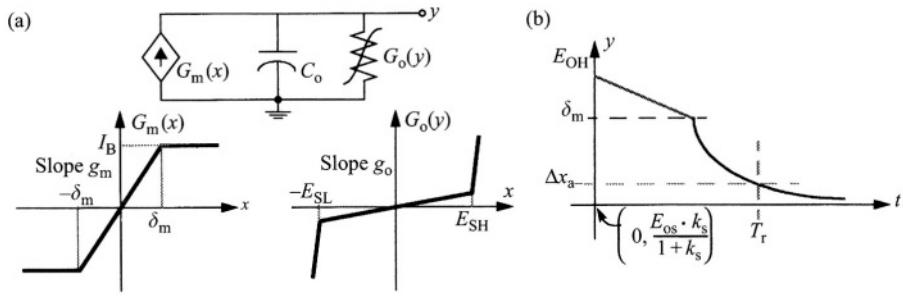


Figure 14.18. Non-linear model for the one-step comparator reset phase.

linear part, where the transconductor is in the saturation region and y evolves from $y(0)$ to δ_m with a fixed slew-rate, δ_m/τ_u, followed by an exponential part with time constant:

$$\tau_{ur} = \frac{C + C_{a-} + C_o}{g_m + g_o} \approx \frac{C}{g_m} \equiv \tau_u \tag{14.42}$$

Thus, the *reset time,* T_r, needed to reach a final Δx_{a-} above the steady-state value is given by:

$$T_r \approx \frac{E_{OH} - \delta_m}{\delta_m} \cdot \tau_u + \tau_u \cdot \ln\left(\frac{\delta_m}{\Delta x_{a-}}\right) \tag{14.43}$$

Note that Δx_{a-} will remain as a residual offset after cancelation.

This equation shows another resolution–speed trade-off. The smaller Δx_{a-}, and hence the error, the larger the time T_r needed for reset. Considering the typical values of $k_s = 2 \times 10^3$, $\tau_u = 10\,\text{ns}$, $E_{OH} = 1\,\text{V}$ and $\delta_m = 250\,\text{mV}$, equation (14.43) obtains $T_r \approx 8.5\,\mu\text{s}$ for 1 mV residual offset. Note that this time is shorter than the amplification time ($T_c \approx 14\,\mu\text{s}$) required to obtain $\Delta_d = 1\,\text{mV}$ from equation (14.15).

At this point new error sources should be considered for completeness. Particularly, noise is an issue in the case of self-biased comparators, although it is usually less important than offset for those comparators which are not self-biased. For considerations related to noise, readers are referred to other chapters of this book.

14.6. Appendix. Simplified MOST Model

MOS transistors exhibit different operation depending on the current and voltage levels. Through the article we consider the MOST model only under *strong* channel inversion, and describe its first-order behavior using a model

with four parameters, namely: zero-bias *threshold voltage* V_{T0}, *slope factor n, intrinsic transconductance density* β_0, and *equivalent Early voltage* V_A [28]. Two subregions are considered within strong inversion:

- *Triode* (*or ohmic*) *region.* In this regime, the source and drain voltages V_S, V_D remains below $V_p = (V_G - V_{T0})/n$, where V_G is the gate voltage (all voltages are referred to the local substrate). The drain current takes the form:

$$I_D = 2\beta_0 \cdot \frac{W}{L} \cdot \left[V_G - V_{T0} - \frac{n}{2} \cdot (V_D + V_S)\right] \cdot (V_D - V_S) \quad (14.44)$$

  where W/L is the aspect ratio of the transistor.

- *Saturation region.* Assuming forward operation, this regime is reached when $V_S < V_p < V_D$ and the drain current amounts to

$$I_D = \beta_N \cdot (V_G - V_{T0} - nV_S)^2 \cdot \left[1 + \frac{V_D - V_p}{V_A}\right] \quad (14.45)$$

  where $\beta \equiv \frac{\beta_0}{n} \cdot \frac{W}{L}$.

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Chapter 15

SWITCHED-CAPACITOR CIRCUITS

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15.1. Introduction

Switched-Capacitor (SC) technique is one of the most popular design approaches to implement analog functions in integrated circuit form. This popularity, gained since the last 1970s [1,2], is due to the fact that SC technique allows to implement analog filters with accurate frequency response and, more generally, analog functions with large gain accuracy. This is because SC filter performance accuracy is based on the matching of integrated capacitors (and not on their absolute values). In a standard CMOS process, the capacitor matching error can be lower than 0.2%, without component trimming. For the same reason, temperature and aging coefficients track, reducing performance sensitivity to temperature and aging variations. Such a wide popularity has been further increased since SC circuits can be realized with the same standard CMOS technology used for digital circuits [3]. In fact, the infinite input impedance of the op-amp is obtained using a MOS input device. MOS transconductance amplifiers are used since only capacitive load is present, precise switches are realized with MOS transistor, and capacitors are available in the MOS process. This allows realizing fully integrated low-cost high-flexibility mixed-mode systems. Other important reasons of the large popularity of SC networks are the possibility of processing large swing signals (thanks to the SC closed-loop structures) with consequent large dynamic range (DR), and the possibility of realizing long time-constants SC filters without using large capacitors and resistors (this gives a significant chip area saving, with respect to active-RC filter implementations). On the other hand, these advantages are in trade-off with the typical major drawbacks of SC technique as summarized in the following points:

1 In order to process a fully analog signal, a SC system has to be preceded by an anti-aliasing filter (AAF) and followed by a smoothing filter, which will complicate the overall system and increase power, and die size.

2 The op-amps embedded in a SC system have to perform a large dc-gain and a large unity-gain bandwidth, much larger than the bandwidth of the signal to be processed. This limits the maximum signal bandwidth.

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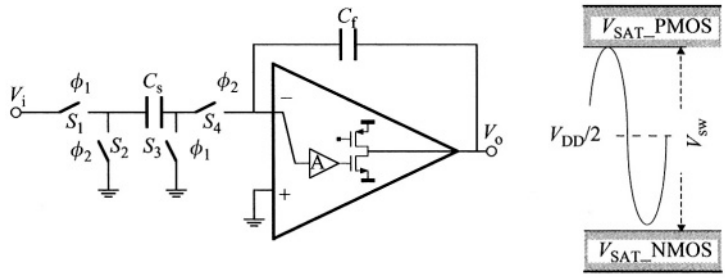


Figure 15.1. Standard SC integrator.

3 The power of noise of all the sources in a SC system is folded in the base-band $[0-F_s/2]$. Thus their noise power density is increased by the factor $F_{NB}/(F_s/2)$, where F_s is the sampling frequency and F_{NB} is the noise bandwidth at the source.

From its first proposals the SC technique has been deeply developed. Many different circuits solutions have been realized with SC technique not only in analog filtering, but also in analog equalizers, sample and hold, track and hold, analog-to-digital and digital-to-analog conversion (including in particular, the oversampled $\sum \Delta$ converters), etc. Op-amps, switches and capacitors compose SC circuits. For instance, Figure 15.1 shows a SC integrator, which is the fundamental building block for the design of SC filters. Its performances are strongly dependent on the performance of its components, which in some cases are in trade-off between their self.

In literature, a number of publications deal with the typical trade-offs present in the "standard" design of SC circuits. For instance, some of these fundamental trade-offs are:

1 dc-gain (to be maximized) vs unity-gain bandwidth (to be maximized) in the op-amp design [4,5];

2 signal bandwidth (to be maximized) vs noise bandwidth (to be minimized) [6–8];

3 switch-on resistance (to be minimized) vs switch charge injection (to be minimized);

4 power consumption vs DR (SNR and THD) [9,10].

These arguments have been deeply studied in a large number of papers and so they will not be addressed in the following. This chapter will deal with the research activity, which is working to extend the SC circuit implementation to

applications up to now not feasible. In this scenario, the SC technique has to face two main trends in the present electronics world:

1 The use of scaled technologies (strongly motivated by the realization of mixed-signal systems in which the digital section is larger and dominates the technology choice).

2 The development of wideband/high-frequency signal processing (strongly motivated by the realization of telecommunication systems).

These two trends will be studied in the following, with attention to the various trade-off to be faced by the designers of the SC sections.

15.2. Trade-Off due to Scaled CMOS Technology

In the recently developed mixed-mode integrated systems, the analog signal processing is reduced to small interfaces at the input (with mainly analog-to-digital conversion purpose) and at the output (with mainly digital-to-analog conversion purpose). This results in a very large digital part (even larger than 90%) and in a small analog section. SC circuits are embedded in the analog section in which they have an important role due to their sampled-data nature, which improves their front-end and back-end action for the digital section. This predominance of the digital part gives the digital designer the possibility to force the technology choice and this leads to the use of the most scaled technology available. This is because the use of a smaller minimum gate size results in:

1 reduced supply voltage, which can be sustained by the MOS devices. Figure 15.2 shows the foreseen maximum supply voltage for the future scaled technology in the next years [11]. This supply reduction results in a reduction of the power consumption of the digital part which is:

$$P = f \cdot C \cdot V_{DD}^2 \tag{15.1}$$

where C is the capacitive load, which is reduced by the use of smaller devices, and V_{DD} is the supply voltage, which is reduced for the technology yield;

2 increased number of devices, and therefore, of implemented functions on a single chip with an acceptable yield.

Analog section has to accept this trend even if this could avoid the achievements of the same performance previously obtained with larger device technology. This is because scaled-down technologies present a trend for a number of analog parameters, which is detrimental for the analog designer, as follows.

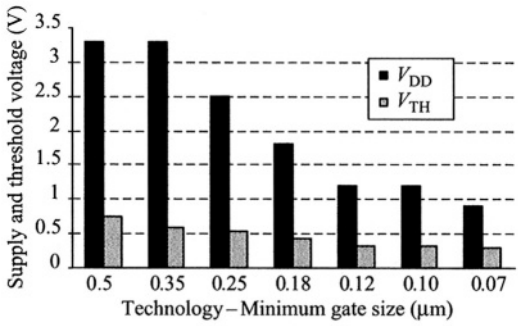


Figure 15.2. Supply and threshold voltage trend for different technologies.

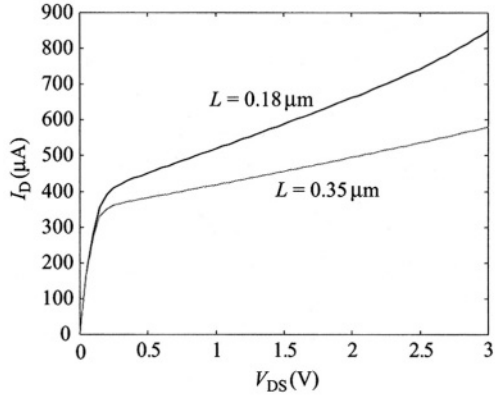


Figure 15.3. Output characteristics for different minimum length technologies.

15.2.1. Reduction of the MOS Output Impedance (r_o)

In scaled-down technology, the Early voltage (V_A) and, as a consequence, the output impedance (r_o) are getting lower, as it can be seen in Figure 15.3, where the output characteristics of two MOS devices from different technologies are compared. A smaller r_o gives a lower dc-gain, even in presence of a larger g_m. The performance of SC circuits is strongly dependent on the op-amp dc-gain and so the r_o reduction is detrimental for SC circuits. For instance, for the SC integrator of Figure 15.1, the magnitude $m(\omega)$ and phase $\theta(\omega)$ errors due to finite op-amp gain (A_o) are the following:

$$m(\omega) = -\frac{1}{A_o}\left(1 + \frac{C_s}{C_f}\right) \quad \theta(\omega) = \frac{C_s}{2C_f A_o \tan(\omega T/2)} \tag{15.2}$$

These errors affect the frequency response of high-order SC structures embedding finite gain op-amps ($m(\omega)$ is typically responsible for pole frequency error, while $\theta(\omega)$ is typically responsible for pole quality factor error).

Such a gain reduction due to the technological r_o reduction can be compensated:

1 by using stacked configuration (cascode, triple cascode, etc …) but this is in trade-off with the available output swing;

2 by using several stages in cascade but, to achieve op-amp stability, this is in trade-off with the op-amp bandwidth;

3 by using MOS devices with non-minimal length, but this is in trade-off with the effective advantage of using a scaled-down technology in analog sections.

15.2.2. Increase of the Flicker Noise

With a smaller device size, the flicker ($1/f$) noise increases. In SC circuits, the white noise is folded in the baseband and this results in an "effective" reduction of the $1/f$ corner frequency. However, for a number of applications (typically high-performance oversampled ADC and DAC with 16–18 bit accuracy) the $1/f$ noise is still the limiting factor for the DR. For instance, concerning the output noise, a basic trade-off appears in the realization of ADC and DAC. In fact, two noise sources are present: the flicker and the thermal noise. Flicker noise can be strongly canceled by using Correlated Double-Sampling technique. This, however, corresponds to process both the above noise components with a $(1 - z^{-1})$ transfer function (t.f.), which exhibits a gain factor of two for medium and high frequency, that is, for the thermal noise [12]. In these cases, it is then necessary to spend additional power to reduce thermal noise level. This is, however, the usual trade-off between noise performance and power consumption.

Notice that another effect of the increase of the $1/f$ noise appears in the clock phase generators. In fact a larger $1/f$ noise results in an increase of the jitter in clock phase which, as a consequence, increases the white noise level of the SC circuits.

15.2.3. Increase of the MOS Leakage Current

High-speed low-threshold devices, as required by digital applications, typically perform an increased leakage current. This is, however, strongly detrimental for SC circuits in which the information to be processed corresponds to the stored charge. For instance, for the SC integrator of Figure 15.1, the charge stored on the integrating capacitor C_f can be lost through the leakage current

flowing through the MOS devices implementing switch S_4. For this reason, in recent mixed-signal technology two or more possible oxide thicknesses are available. This allows the designer to have devices with different leakage current and/or threshold voltage, allowing optimum operation for both analog and digital circuits.

15.2.4. Reduction of the Supply Voltage

The supply voltage is required to be reduced both for technological and for application reasons. The technology scaling imposes a supply reduction as shown in Figure 15.2. This occurs in conjunction with a slight reduction of the MOS threshold voltages and so it is still possible to design an analog circuit at the reduced supply voltage, even if some of them exhibit reduced performance. The use of standard SC design technique is possible for a supply voltage V_{DD} as follows:

$$V_{DD} > 2 \cdot V_{TH} + 2 \cdot V_{SAT} \tag{15.3}$$

where V_{SAT} is upper and lower saturation voltage of the output stage (see Figure 15.1). An important consequence of the supply reduction is that, for analog systems, the power consumption increases for a given DR. In fact, for a given supply V_{DD}, the maximum swing possible is about:

$$SW = [V_{DD} - 2 \cdot V_{SAT}] \tag{15.4}$$

The power consumption (P) can be written as (I is the total current):

$$P = V_{DD} \cdot I \tag{15.5}$$

On the other hand, the noise is assumed to be thermal noise limited (kT/C) and then it is inversely proportional to a part of the current $\alpha \cdot I$ (i.e. $N^2 \sim 1/(\alpha \cdot I) = V_{DD}/(\alpha \cdot P)$). The DR can then be written as follows:

$$\begin{aligned} DR &\sim \frac{SW^2}{N^2} \sim \frac{[V_{DD} - 2 \cdot V_{SAT}]^2}{1/(\alpha \cdot I)} \\ DR &\sim [V_{DD} - 2 \cdot V_{SAT}]^2 \cdot \alpha \cdot \frac{P}{V_{DD}} \end{aligned} \tag{15.6}$$

For a given DR, the required power consumption is:

$$P \sim \frac{DR \cdot V_{DD}}{\alpha (V_{DD} - 2 \cdot V_{SAT})^2} \tag{15.7}$$

Thus it appears that the analog power increases for V_{DD} decreasing, as qualitatively shown in Figure 15.4 (this trend is demonstrated for technology with minimum device length smaller than $0.35\,\mu m$ [13]). This can be also seen

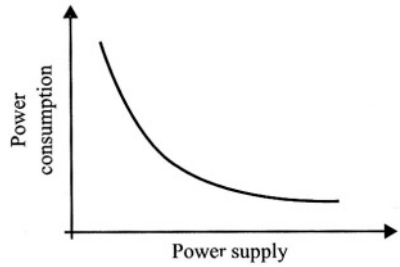


Figure 15.4. The qualitative dependence of the power consumption vs power supply, for a given DR.

Table 15.1. Performance comparison.

Reference	*Year*	V_{DD}	*DR (dB)*	*BW (kHz)*	*P (mW)*	*F* ($\times 10^6$)
Peluso [14]	98	0.9	,7	16	0.040	330
Williams [15]	94	5	104	50	47	445
Nys [16]	97	5	112	0.4	1.3	800

from Table 15.1, where the performance of some significant analog systems is compared. They are all $\sum \Delta$ modulators, but their performance is limited by thermal noise (i.e. they can be considered as fully analog systems). They are compared using the following figure of merit:

$$F = \frac{4 \cdot k \cdot T \cdot \mathrm{DR}^2 \cdot \mathrm{BW}}{P} \tag{15.8}$$

It appears that the figure of merit of systems operating at 5 V (even if realized with technology not at the present state-of-the-art) is better than that of more recent implementations at low voltage with better technologies.

The second possible reduction of the supply voltage can be due to the application requirements. Several applications are battery operated and they have to work with a single cell (i.e. with a nominal supply of 1.2 V, and with a worst case supply of 0.9 V). For a number of technologies, this supply value does not satisfy the relationship of equation (15.3). Thus a number of analog circuit configurations, typically adopted in SC circuits, cannot be anymore designed in the same way as with higher supply. This is the case, for instance, for op-amps and switches. A trade-off between the use of low-voltage supply and the possible circuit solution is then present. Concerning the op-amp design, cascode op-amp is no more possible, and large op-amp gain can be achieved only by cascading several gain stages, and these configurations would exhibit a smaller bandwidth for the compensation. Concerning the switch design, with

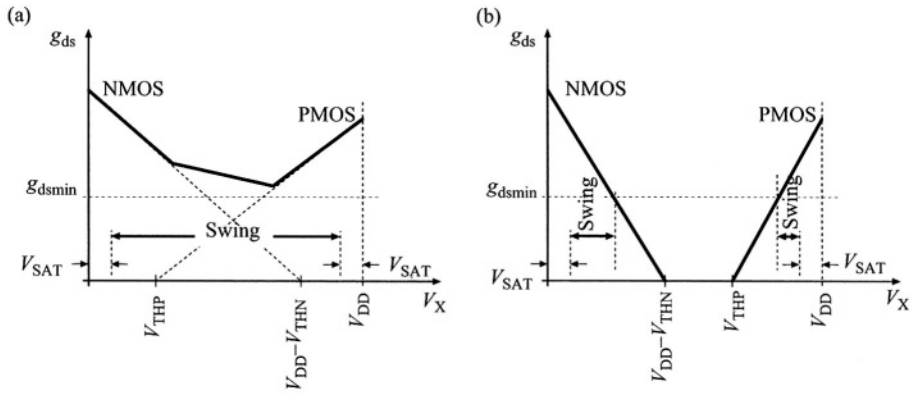


Figure 15.5. Switch conductance with (a) $V_{DD} = 5\,V$ and (b) $V_{DD} = 1\,V$.

the supply voltage reduction, the MOS switches overdrive voltage is lowered, and this inhibits the proper operation of classical transmission gate. The switch conductance for different input voltages depends on the supply voltage V_{DD} as shown in Figure 15.5(a) ($V_{DD} = 5\,V$) and in Figure 15.5(b) ($V_{DD} = 1\,V$). For $V_{DD} = 1\,V$, a critical voltage region centred on $V_{DD}/2$ is present where no switch is conducting. However, rail-to-rail output swing (which is mandatory at low voltage) can be achieved only if the output of the op-amp crosses this critical region, where the switches are not properly operating. Several solutions have been proposed to properly operate switches also at reduced supply voltage. However, each of them achieves proper operation with a trade-off in some other circuit features.

From a general point of view it can be demonstrated that, using proper (non-standard) design solutions, the minimum supply voltage to operate a SC circuit (V_{DDmin}) is:

$$V_{DDmin} = V_{TH} + 2 \cdot V_{SAT} \tag{15.9}$$

A first proposal is to use an on-chip supply voltage multiplier to power both op-amps and switches [17]. This should give excellent circuit performance, but it suffers from the technology robustness (a large electric field is applied to the devices), from the need of an external capacitor (to supply a dc current to the op-amps from the multiplied supply), and from the conversion efficiency of the charge-pump (which is much lower 100%, limiting the application of this approach in battery operated portable systems).

A second and more feasible alternative to operate low-voltage SC filters is the use of on-chip clock multiplier [18] to drive only the switches, while the op-amps operate from the low-supply voltage. This design approach, like the previous one, suffers from the technology limitation associated to the gate

oxide breakdown. However, this approach is very popular since it allows the SC circuits to operate at high sampling frequency. This design solution can be improved by driving all the switches with a fixed $V_{GS}-V_{TH}$ [19]. In this case, a constant switch conductance is ensured and this reduces also signal-dependent distortion. It, however, requires a specific charge-pump for each switch, increasing area, power consumption and substrate noise injection.

In order to avoid any kind of voltage multiplier, a third approach called *Switched-Op-amp* (SOA) technique is proposed [20,21]. It consists in connecting all the switches to ground or to the supply. The critical switches connected to the op-amp output nodes are replaced by turning on and off the driving force of the op-amps, This technique suffers due to the following drawbacks:

1 An SOA structure uses an op-amp which is turned on and off: the op-amp turn on time results to be the main limitation in increasing the sampling frequency.

2 To proper bias the SC structure, a noisy SC level shift is implemented and this increases the switches noise by a factor 1.5.

3 The output signal of an SOA structure is available only during one clock phase, while during the other clock phase, the output is set to zero. If the output signal is read as a continuous-time waveform, the zero-output phase has two effects: a gain loss of a factor of 2, and an increased distortion, due to the large output steps. However, when the SOA integrator precedes a sampled-data system (like an ADC), the SOA output signal is sampled only when it is valid and both the above problems are canceled.

15.3. Trade-Off in High-Frequency SC Circuits

Large bandwidth systems have to use high-frequency SC sections. This corresponds, for instance, to 12b ADCs with few MHzs band for XDSL applications, to 12bit $\sum\Delta$ modulators with sampling frequencies in the hundreds of MHz range for IF blocks in telecom, and 6b ADCs and filters with hundreds of MHz band for Hard-Disk Drive.

In high-frequency SC circuits, the main limitations come from the op-amps and from the input samplers. In the op-amp design, a basic trade-off exists between large bandwidth and large dc-gain. This strongly imposes a consequential trade-off in the performance of SC circuits. Equation (15.2) gives the SC circuit errors due to op-amp finite dc-gain. Similar equations can be written also for the op-amp finite bandwidth [4,5]. Therefore a high-frequency SC circuit designer has to face the op-amp design problem. First of all, the op-amps have to settle in the time slot allowed by the sampling frequency. This corresponds to the requirement that the op-amp unity-gain bandwidth frequency be in the order of few tens higher than the signal maximum frequency. This has

to be reached by a sufficiently large op-amp bandwidth with the consequent op-amp gain (which typically results to be low). In the following, some possible solutions are briefly introduced to overcome this trade-off. The other key limitation comes from the input signal sampling operation which is damaged by non-accurate clock phase: the jitter error appearing in the input sampling switch results in a white noise in the full $[0 - F_s/2]$ band whose value is:

$$N_{jit} = \frac{1}{\sqrt{2}} \cdot A \cdot 2\pi \cdot f_{in} \cdot \sigma_{jit} \tag{15.10}$$

where A is the signal amplitude, f_{in} is the signal frequency and σ_{jit} is the jitter rms value. This value is small, and then negligible for low-frequency applications while it becomes dominant for high-frequency systems. A big design effort is then required for a good input sampler, which corresponds to have excellent clock phase generator (i.e. with low jitter) and switch configuration (i.e. signal amplitude independent).

15.3.1. Trade-Off Between an IIR and a FIR Frequency Response

For a generic SC filter, a given frequency mask can be satisfied using an IIR or an FIR t.f.s. Typically SC circuits implement IIR transfer functions which allow to satisfy a given frequency mask with a lower order structure than FIR ones do. The use of FIR t.f.s is then limited to some passive polyphase input structures to place zeros in specific position. However, IIR structures are more sensitive to the op-amp non-idealities (an uncompleted settling of the SC structure can be due to op-amp gain, bandwidth, slew-rate, etc …). A possible solution to realize IIR SC circuits able to operate with low-gain op-amps is given by the Precise Op-amp Gain design approach [22]. It consists in using wideband amplifiers with low but precisely known dc-gain. This accurate op-amp gain value is taken into account while sizing the capacitors. Therefore, no idle phase is necessary for gain compensation and double sampling technique can be implemented.

The other alternative is to implement FIR t.f.s. In fact, in FIR structures, the finite op-amp gain affects only the overall gain while it is not important for the zeros' positions, that is, the frequency response. It is therefore possible to optimize the op-amp bandwidth to the needs of the system sampling frequency and to operate with the consequent dc-gain. This is the reason for which in some high-frequency applications, SC technique can be applied with FIR structures [23]. These solutions are also possible in the applications at very high frequency because typically limited performances (6-bit accuracy) are needed (otherwise the limited dc-gain should result important also for distortion, etc….). About architecture trade-off, several solutions are possible

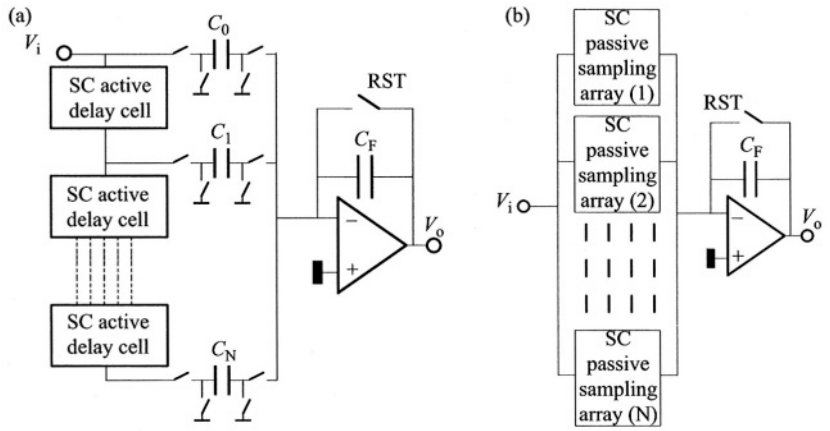


Figure 15.6. (a) Scheme FIR1 for an SC FIR filter and (b) scheme FIR2 for an SC FIR filter .

to implement the same FIR t.f. For instance, Figure 15.6(a) and (b) show two possible architectures implementing the same FIR frequency response. Their comparison makes evident the trade-off present in both of them. The FIR1 (Figure 15.6(a)) includes an active analog delay line to generate the input samples. This active delay line includes op-amps whose low gain has a detrimental effect on the frequency response, since a gain error is accumulated in the delay chain, and in the overall t.f. On the other hand, FIR2 (Figure 15.6(a)) avoids these errors since it presents a number of parallel passive sampling arrays. This corresponds also to a smaller power consumption (no op-amp is needed to generate delay). However, it suffers from the path mismatch resulting from the capacitor mismatch in the different array. This gives tones in the frequency response. This problem is, on the other hand, not present in FIR1.

15.3.2. Trade-Off in SC Parallel Solutions

From the previous example, it is clear that a possible step to operate with extremely large sampling frequency of an SC circuit is to implement parallel structures (double-sampling is the basic paralleling solution). These are basically possible due to sampled-data nature of the SC technique signal processing. IIR structures (which, in any case, are less preferable at high frequency) are not easily paralleled because they intrinsically need the output sample at the immediately precedent time slot to elaborate the present sample. On the other hand, this is not the case of FIR structures, which, analogously to the digital case, can be easily paralleled [23]. However, in these cases another trade-off appears. In fact, the frequency response of parallel structure is affected by the mismatch between the elements in the different channels, which can be due,

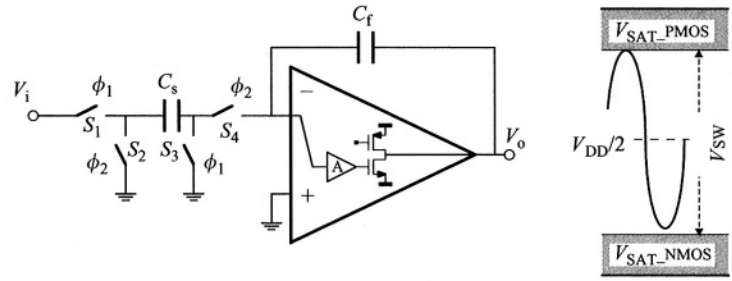


Figure 15.7. Output spectrum for a 4-path sample.

for instance, to: capacitor mismatch, gain mismatch (mainly important if the gain is low), and op-amp offset mismatch. These mismatch sources result in tones at the image frequency of the reduced sampling rate of each channel. For instance, Figure 15.7 shows the output spectrum of a 4-path parallel SC sampler. In this case, a random 0.5% mismatch is assumed in the path mismatch and for an input tone, three tones at –52 dB result. These tones for the system are noise and then the system DR result to be limited by the channel mismatch [24,25]. Notice that this effect is limiting the performance of all the analog systems, which present a parallel structure, like some topologies of ADC and DAC. And this is worse in high-frequency applications, where the used small capacitor values present a larger mismatch, reducing the DR.

15.3.3. Trade-Off in the Frequency Choice

In some cases, the SC designer can choose the sampling frequency to be used. However, for large signal bandwidth and/or for signal with narrow bandwidth but centered at high frequency (this is the classical case of telecommunication systems), a significant trade-off appears between SC circuit requirements and op-amp requirements. In fact, a given maximum input signal component f_{in} imposes a minimum sampling frequency given by $F_{sMIN} = 2 \cdot f_{in}$. For a number of reasons, to achieve optimum SC section performance (frequency response, op-amp slew-rate, image components), a sampling frequency F_s much larger than F_{sMIN} should be adopted. However, the sampling frequency is limited by the settling time of the op-amps embedded in the SC structure. Thus as f_{in} increases, the ratio F_s/f_{in} decreases, and the SC structure starts to suffer for the following reasons:

1 A low F_s/f_{in} ratio implies that the aliasing (image) component for frequency f_{in} is at frequency $F_s - f_{in}$, which results to be very close to f_{in}. A highly selective AAF is, therefore, needed and this filter could present

requirements comparable to those of the main SC filter (in this case, the use of SC filter should be no more motivated).

2 A low F_s/f_{in} ratio implies that a large inaccuracy in the *s-to-z* transformations results. Therefore, the design procedure starting from the prototype in the *s*-domain to be translated in the *z*-domain is less efficient and a synthesis in the z-domain should be preferable. In these cases, digital filter synthesis tools can be used.

A solution sometimes adopted to avoid the increasing of the required F_s due to the increasing of f_{in} is the use of subsampling SC structures. These have been adopted both for filters [26–28] and ADC [29–31]. Their functionality is based on the concept that all the frequencies f_{al} given by:

$$f_{al} = k \cdot F_s \pm f_{in} \quad \text{with } k = 1, 2, 3, \ldots \tag{15.11}$$

when they are sampled at F_s, give the same sequence of samples. Once the input sample sequence is generated (provided that the signal band is limited in a $[k \cdot (F_s/2) - (k+1) \cdot (F_s/2)]$ range by the AAF), a signal at high frequency can be processed with a low-F_s SC circuit. A possible parameter for the following discussion is the Sub-Sampling Factor (SSF), defined as:

$$\text{SSF} = \frac{f_{in}}{F_s/2} \tag{15.12}$$

In "standard" cases, SSF is lower than unity, while it is larger than unity for sub-sampling systems. In these cases, at the low-F_s SC filter output, the signal is finally reconstructed with a smoothing filter, which can be:

1 identical to the AAF: the output signal is at the same frequency of the input one;

2 in a different $[0 - F_s/2]$ band: the input signal is translated to the output frequency which is centered into the smoothing filter band.

The basic advantages of the sub-sampling technique are:

1 It is possible to elaborate high-frequency bandpass signals.

2 Signal down-conversion can be automatic.

3 Pole Q-factor is sized for the $[0 - F_s/2]$ band t.f. This corresponds to a Q-factor SSF times higher for the sub-sampled signal: high-frequency high-Q systems can then be realized. Notice that this requires an improved frequency accuracy in the filter t.f.

These advantages are in trade-off with the following disadvantages:

1 The complete input spectrum noise is folded in the $[0 - F_s/2]$ band: a reduced DR could results for the large input noise, which is folded in the signal band.

2 Proper AAF is needed because it has to reject the aliasing component given in equation (15.11). In the best case (i.e. operating with $f_{in} = F_s \cdot (2 \cdot k + 1)/4$) the AAF Q-factor has to be:

$$Q_{AAF} > \frac{f_{in}}{\Delta F} = \frac{f_{in}}{F_s} = \text{SSF} \tag{15.13}$$

The AAF complexity could then be comparable to that of the main SC filter. In addition, the AAF requirements also include noise performance which could become critical, due to the folding of SSF sidebands of the input noise spectrum. A cascade structure with several sub-sampling sections can be adopted in order to reduce AAF requirements. This is, however, in trade-off with the in-band folded noise, which is increased [26].

3 $\sin(x)/x$ effect becomes important if the output waveform is read in continuous-time manner and this imposes using a small SSF value (i.e. limiting the advantage of sub-sampling).

4 Clock jitter is becoming a relevant limitation.

15.4. Conclusions

In this chapter, some trade-offs to be faced by an SC circuit designer are proposed. SC technique gained a large popularity in the past and it seems to be mature to be able to give excellent response for the future requirements of mixed-signal systems. However, the actual trends towards scaled-down technology, low-voltage and/or high-frequency systems impose an increased effort in finding new solutions for the SC circuits in order to achieve the required performance in the new conditions.

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Chapter 16

COMPATIBILITY OF SC TECHNIQUE WITH DIGITAL VLSI TECHNOLOGY

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16.1. Introduction

For several decades, the switched-capacitor (SC) technique has been the dominant circuit technique for voltage-mode sampled-data signal processing. High precision has usually been achieved through the use of high-quality capacitors that could be implemented only with special IC processes. Such processes required several steps more than in a standard VLSI process, and this has made conventional SCs incompatible with digital VLSI processing.

In this chapter, circuit techniques which make SC circuits compatible with standard digital VLSI process are discussed. First, various capacitor structures available in the digital VLSI process are described. Then, compatibility of an operational amplifier to standard digital VLSI processes is discussed. This is followed by a description of charge-domain processing approach which is independent of the technological type of capacitor structure. Next, techniques to alleviate the error that results from the use of these capacitors are presented. Finally, factors influencing practical accuracy limitations of the circuits using these techniques are examined.

16.2. Monolithic MOS Capacitors Available in Digital VLSI Processes

In SC circuits, capacitors are key components which limit the performance. Transfer functions are defined by ratios of capacitors, which can be accurately controlled, rather than by their absolute values. Therefore, high precision circuits have become practicable and have gained popularity. The accuracy of such circuits lies on linearity of the capacitors. For silicon gate MOS technology,

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highly linear capacitors are normally implemented by one of the two following structures.

16.2.1. Polysilicon-over-Polysilicon (or Double-Poly) Structure

Figure 16.1(a) and (b) shows the cross-sectional view of a double-poly (deposited polycrystalline silicon) capacitor structure. In this structure, the two plates of the capacitor are formed by layers of polysilicon separated by the dielectric (silicon dioxide layer). This structure can only be produced by using several steps beyond the usual single polysilicon process. The rough nature of the oxide–polysilicon interface limits the allowable dielectric thickness and this in turn limits the maximum specific capacitance that can be obtained. However, for scaled technologies with thinner oxides, this capacitor structure has become difficult to incorporate [1].

16.2.2. Polysilicon-over-Diffusion Structure

Another high-quality capacitor structure is formed by using a single layer of polysilicon for the top plate of the capacitor, and using diffusion as the bottom plate. However, for capacitor types using diffusion as the bottom plate, the capacitor value is dependent on the applied voltage. In order to achieve a low voltage-dependent capacitor, the bottom plate is formed by utilizing a heavily doped diffusion region in the silicon substrate, as shown in Figure 16.1(c) and (d). The impurity concentration in the plate is relatively high so that variations in surface potential, when the voltage is applied to the gate, are then small. However, in standard silicon gate processes, such a heavily doped diffusion is

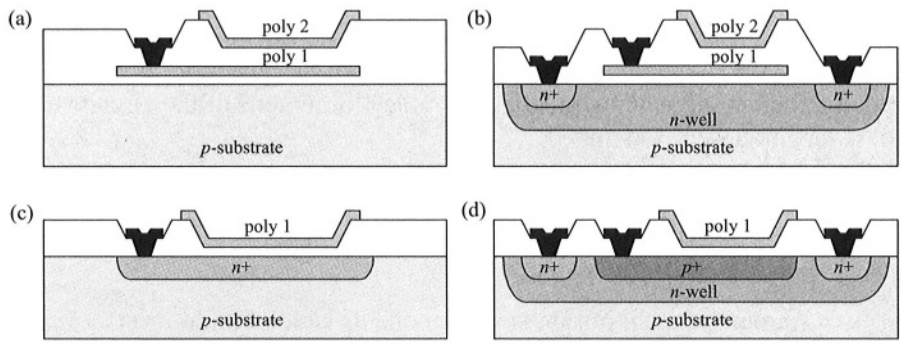


Figure 16.1. Analog CMOS capacitor structure (a) double-poly capacitor (b) double-poly capacitor with a well as bottom shield, (c) poly-diffusion capacitor, (d) poly-diffusion capacitor with a well as bottom shield.

not normally available underneath the polysilicon. This is because the polysilicon layer is deposited before the heavily doped source–drain diffusions are performed. So this structure requires an additional masking and processing step to insert the heavily doped diffusion region under the polysilicon and thin oxide layer. The capacitor dielectric is the thermally grown gate oxide, and hence exhibits good thickness uniformity. However, the heavily doped diffusion becomes less viable for very thin oxides since extremely high doses become necessary to realize good performance [1]. The higher dopant concentrations required to realize low voltage-dependence are not easily achieved using thermal cycles consistent with VLSI processing. In addition, it can also lead to a reduced dieletric breakdown.

For self-aligned silicon gate processes, which are the standard for VLSI, neither the additional layer of polysilicon nor the heavily doped diffusion are available. In order to achieve low voltage coefficient capacitors, inner metal can be used as an alternative to implement capacitors. The capacitor structures that incorporate the inner metal are: metal-over-metal and metal-over-polysilicon structures.

16.2.3. Metal-over-Metal Structure

Figure 16.2(a) and (b) show the metal-over-metal capacitor structure. Capacitors fabricated with metal plates exhibit low voltage dependence since their surfaces do not accumulate or deplete. One advantage of using metal plates is that they result in lower resistive loss compared to silicon plates. However, using metal as the bottom plate requires the use of a low-temperature

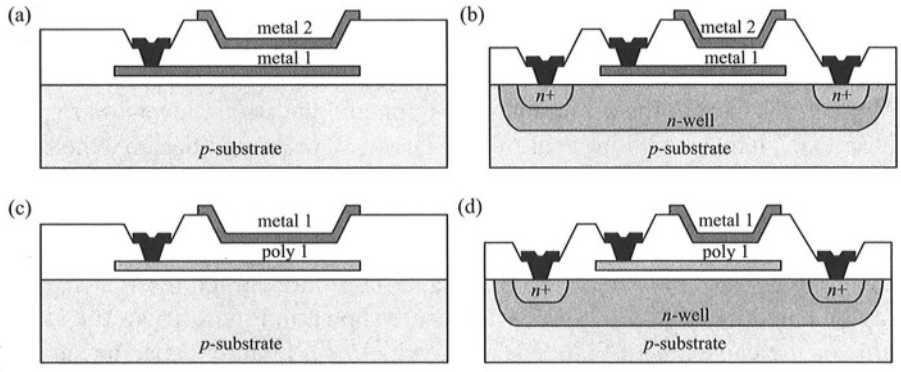


Figure 16.2. Inner metal digital CMOS capacitor structure (a) metal–metal capacitor, (b) metal–metal capacitor with a well as bottom shield, (c) metal–poly capacitor, (d) metal–poly capacitor with a well as bottom shield.

CVD dielectric, since aluminum has a low melting point [1]. This results in poor thickness uniformity control and leakage. Capacitors fabricated with this structure therefore have poor matching, as well as occupying large area which in turn produces large parasitics.

16.2.4. Metal-over-Polysilicon Structure

The inner metal can alternatively be used with the first poly layer, as shown in Figure 16.2(c) and (d). However, the thermal oxide grown on the first poly will then not be protected from subsequent process steps such as formation of the polysilicon gate sidewalls and the source and drain implants [1]. Mixing metal and semiconductor plates also has a disadvantage in terms of electrical performance. Since the space-charge capacitance associated with each surface is not equal, this results in an incomplete cancelation of the voltage-dependence. Hence, this capacitor structure exhibits a moderate voltage coefficient. In addition, the properties of the deposit oxide grown on the metal plate are still the same as the metal-over-metal capacitor structure, and so results in poor matching.

16.2.5. MOSFET Gate Structure

Using the gate oxide for the capacitor dielectric ensures good oxide uniformity and produces a more accurate value of absolute capacitance than other oxide types. Without the heavily doped diffusion underneath the gate oxide, the polysilicon-over-diffusion capacitance is basically the gate-to-source capacitance of a MOSFET. Since the underlying substrate is lightly doped, a large amount of surface potential variation occurs with change in applied voltage. This results in a high voltage-dependence of the capacitors. The relationship between the total MOSFET gate capacitances to the applied voltages is shown in Figure 16.3. In both the accumulation region and the strong inversion region, these capacitances exhibit weak nonlinearity. With proper biasing, the nonlinearity of the MOSFET capacitor can thus be greatly reduced. Using the MOSFET gate capacitance as a capacitor, therefore, requires a bias voltage to keep the capacitors operating in either the accumulation or strong inversion region. Four possible MOSFET gate capacitor structures that can be implemented in a *n*-well CMOS process are shown in Figure 16.4. The structures of the capacitor in Figure 16.4(a), which is a floating capacitor, and in Figure 16.4(b), which is a grounded capacitor, work in the accumulation region. The others work in the strong inversion region, where the capacitor structure in Figure 16.4(c) is a floating capacitor and the structure in Figure 16.4(d) is a grounded capacitor.

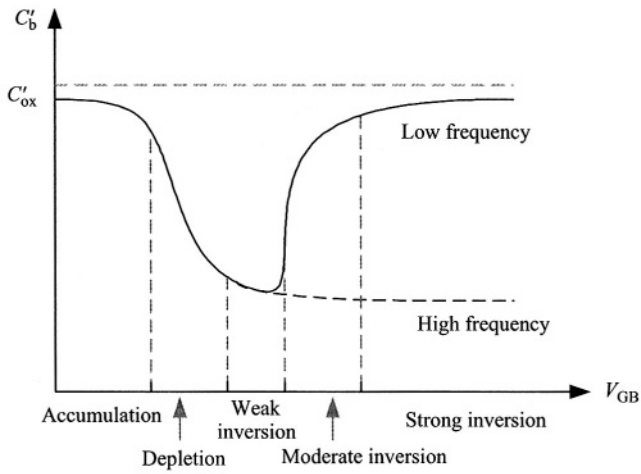


Figure 16.3. Total gate capacitances of MOSFET transistor over all regions of operation.

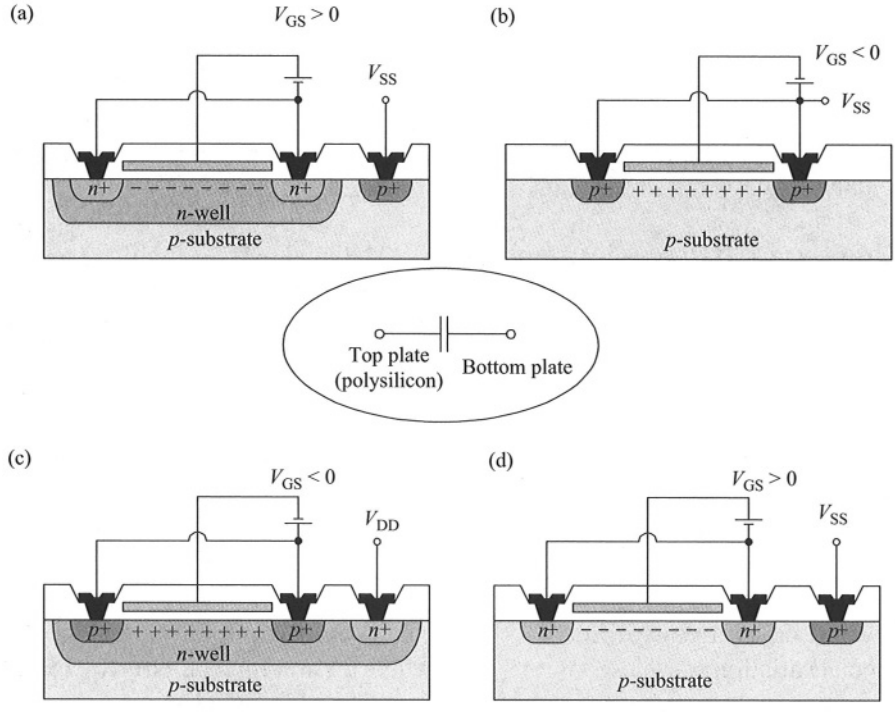


Figure 16.4. Four MOSFET gate capacitor structure in a *n*-well CMOS processes.

16.3. Operational Amplifiers in Standard VLSI Processes

Implementation of an operational amplifier generally does not require any special processes. However, for high performance operational amplifiers, passive components such as capacitors are often employed in order to control the closed-loop stability. This depends on the operational amplifier structures. In addition, a fully differential amplifier topology requires a common-mode feedback (CMFB) circuit to define its operation. Low power dynamic common-mode feedback using SCs normally employs linear capacitors. These unavoidable requirements make the operational amplifiers conventionally not fully compatible with the standard VLSI processes.

Operational amplifier architectures that can be implemented in standard VLSI technology will be discussed, and followed by their impact on the performance of SC circuits.

16.3.1. Operational Amplifier Topologies

The choice of operational amplifier topology is strongly dependent on the desired performance and circuit application. Design of an operational amplifier hence poses many trade-offs between parameters which eventually require a multi-dimensional compromise in the overall implementation. These fundamental trade-off parameters are: gain, bandwidth, output swing, linearity, offset, noise and power supply rejection. Four common structures which are widely employed in SC circuits will be discussed as follows.

Single-stage (telescopic) amplifier. The single-stage amplifier consisting of a single transistor or differential pair is the most basic amplifier structure. This type of amplifier exhibits one dominant pole, and hence provides a higher speed than the other types of amplifier. The high gain can be achieved by stacking a cascode transistor [2] and is often called a telescopic amplifier. Figure 16.5 shows the configuration of the telescopic amplifier. This structure, though providing the highest speed, retains the disadvantage that the output swing is very small. In modern circuit design, for low supply voltage the limited output swing is not adequate. In this case, the amplifier is often designed with other topologies.

Folded cascode amplifier. The folded cascode amplifier topology is a special variation of a telescopic amplifier where the amplifier employs a cascode transistor with an opposite type from the input differential pair, and hence achieves more headroom for the output swing than the telescopic structure. This type of amplifier is basically classified as a single-stage amplifier, and therefore exhibits reasonably high frequency response with a moderate gain at a cost of high power consumption and noise [3,4].

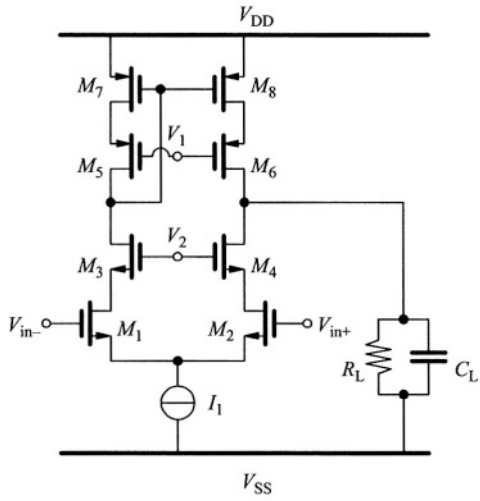


Figure 16.5. Telescopic operational amplifier.

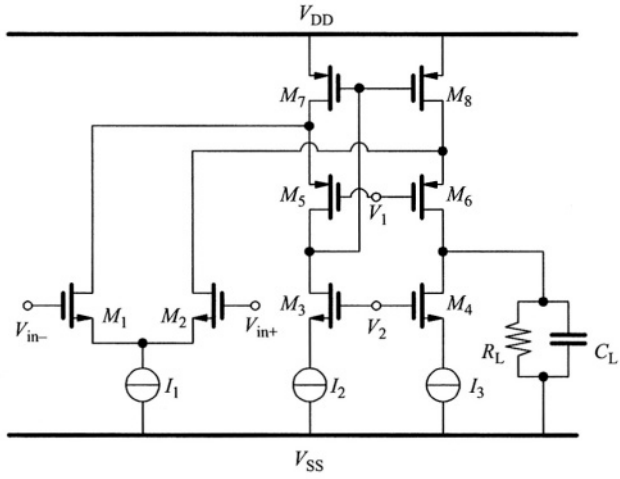


Figure 16.6. Folded cascode operational amplifier.

The configuration of a folded cascode amplifier is shown in Figure 16.6. This structure has widely been employed in SC circuits, particularly for high-speed applications [5].

Gain-boosting amplifier. The limited output swing of the telescopic and folded cascode amplifiers make these structures not favorable in a low-voltage

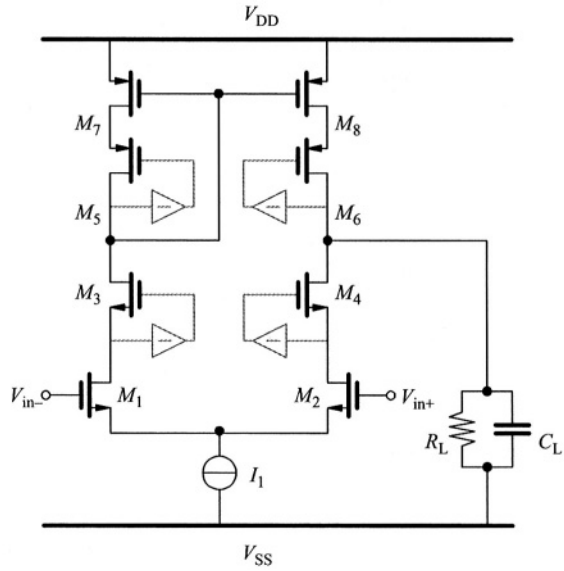


Figure 16.7. Gain-boosting operational amplifier.

environment. Instead of stacking a cascode transistor to achieve high-gain, the gain of an amplifier can also be boosted by applying feedback [6], which is called regulated cascode or gain-boosting [7,8]. Figure 16.7 shows the configuration of a gain-boosting amplifier. This type of amplifier provides reasonably high gain with moderate speed but retains some difficulty to design due to the effect of the doublet for its stability [9].

Two-stage amplifier. The high-gain provided by other amplifier topologies mentioned above often results in a limited output swing. In some applications, particularly in a low voltage environment, the limited output swing is not adequate. A two-stage amplifier structure offers an isolation of the gain and output swing requirement and hence offers the advantage of having the highest output swing and gain. Figure 16.8 shows the configuration of a two-stage amplifier. In this structure, the first stage provides a high-gain while the second stage provides a high-output swing. Since each stage introduces a dominant pole, the two-stage amplifier can be modeled with a two-pole system. The first pole at the output of the amplifier is located at:

$$p_1 = -\frac{1}{R_L C_L} \tag{16.1}$$

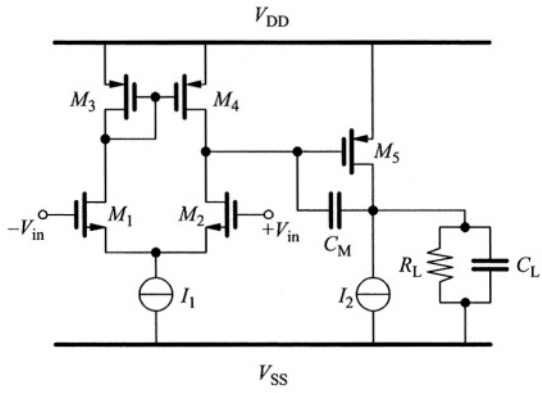


Figure 16.8. Two-stage operational amplifier.

and the second pole at the output of the input stage is located at:

$$p_2 = -\frac{1}{r_{ds2}c_{gs5}} \tag{16.2}$$

To ensure its stability when using the two-stage amplifier in feedback situations, frequency compensation is required.

16.3.2. Frequency Compensation

Frequency compensation is employed to control the amplifier's pole locations in the open-loop transfer characteristic such that the close-loop operation is stable. This can be accomplished by moving the poles so that the amplifier performs like a one-pole system up to its unity-gain frequency. Most of the frequency compensation methods generally incorporate passive components, such as capacitors and resistors, to compensate the amplifier. Various types of frequency compensation will be discussed regarding their compatibility with the standard VLSI processes.

Miller compensation. Miller compensation [10,11], often referred as pole splitting, has commonly been employed for frequency compensation in a two-stage amplifier. In this scheme, the dominant pole is moved toward the origin, while the non-dominant pole is pushed out to a high frequency. The unity-gain bandwidth is therefore defined by the non-dominant pole. Figure 16.8 shows the configuration of a two-stage amplifier employing Miller compensation.

The compensation capacitor, C_M, provides negative feedback around the output stage, and shifts the non-dominant pole to:

$$p_1' = -\frac{g_{m5}}{C_L\left(1+\frac{c_{gs5}}{C_M}\right)+c_{gs5}} \tag{16.3}$$

while the dominant pole is shifted to:

$$p_2' = -\frac{1}{r_{ds2}g_{m5}R_L C_M} \tag{16.4}$$

At high frequency, the Miller capacitor also gives a direct feedforward path through the transistor M_5 to the output. This results in a zero which is situated in the right half-plane:

$$z = \frac{g_{m5}}{C_M} \tag{16.5}$$

This zero introduces an additional phase shift since it is located in the right-half plane. This makes the amplifier's stability severely degraded, particularly when the load capacitor is of the same order as the compensation capacitor.

Miller compensation incorporating source follower. The standard Miller compensation has one drawback of having a right half-plane zero due to the feedforward path through the compensation capacitor, C_M. To eliminate the right half-plane zero, a unity gain-buffer (source follower) is inserted in series with the compensation capacitor [12]. Figure 16.9 shows the configuration of the mentioned scheme. This method was used by Yoshizawa et al. [13] for realizing a MOSFET-only amplifier, where the source follower provides a DC

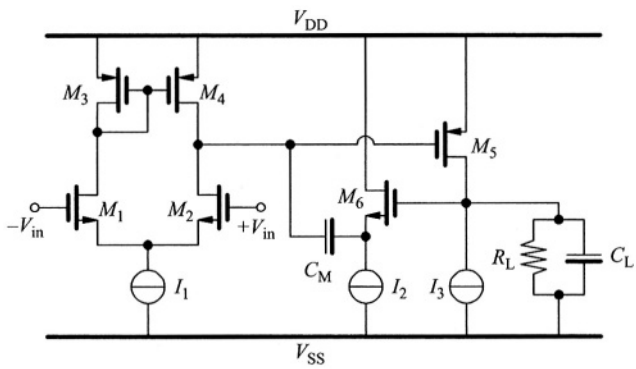


Figure 16.9. Miller compensation incorporating source follower.

bias voltage to keep the compensation MOSFET capacitor operated within its accumulation region.

However, one primary drawback issue of this scheme is that the source follower limits the lower end of the output voltage of the second stage to $V_{GS6} + V_{dsI2}$. This reduces the headroom for the output swing of the amplifier, since V_{GS} is typically about 1 V which is excessively large, particularly in a low-voltage environment.

Cascode Miller compensation. Due to the feedforward path in the classical Miller compensation, the amplifier's performance is degraded if the capacitive load is of the same order as the compensation capacitor. This feedforward path also displays a zero at the dominant pole frequency for the operational amplifier in unity-gain configuration causing poor power supply rejection.

Cascode Miller compensation [14,15] was used to improve the bandwidth of the amplifier over the conventional Miller compensation scheme. Figure 16.10 shows the technique. In this configuration, the compensation capacitor is connected from the output node of the second stage to the cascode of the first stage. Hence, the capacitor closes a feedback loop around a two-pole system, instead of a one-pole feedback loop as in standard Miller compensation. The non-dominant pole is shifted to

$$p_1' = -\frac{C_M}{c_{gs9}} \frac{g_{m9}}{C_L + C_M} \tag{16.6}$$

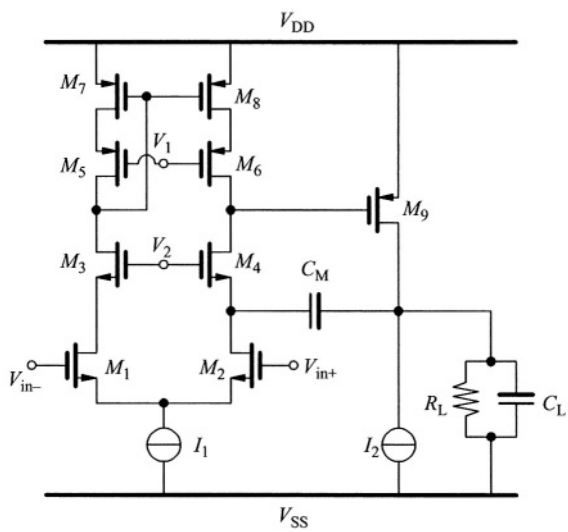


Figure 16.10. Cascode Miller compensation.

The cascode Miller loop also introduces another non-dominant pole due to the finite-impedance at the source of the cascode transistor. The pole is located at

$$p_2' = -g_{m4}\frac{C_L + C_M}{C_L C_M} \tag{16.7}$$

and the dominant pole is shifted to

$$p_3' = -\frac{1}{g_{m9} R_L r_{ds4} C_M} \tag{16.8}$$

The technique also provides better positive power supply rejection ratio (PSRR) by eliminating the high-frequency path to the positive supply. (In the case of PMOS transistor being used as an input differential pair, the zero will occur through the negative power supply hence causing poor negative PSRR.)

The effect of using a MOSFET-capacitor for frequency compensation is to produce a frequency variation in the operational amplifier. This only affects dynamic behavior of SC circuits without contributing any distortion if dynamic condition is satisfied. If the dynamic condition is very tight (to save current consumption), an internal metal–metal capacitor type can be used. However, MOSFET-capacitor still can be used. The operational amplifier frequency variation is reduced by biasing the compensation MOSFET-capacitor into its weak nonlinear region. The Miller compensation incorporating a source follower [13] is one way to keep the compensation MOSFET-capacitor in its accumulation region in order to reduce the operational amplifier's frequency variation. However, the output signal swing of the operational amplifier will be reduced. In an application where large output swing is required, one solution is to use a composite capacitor branch where the MOSFET-capacitors are biased into their weak nonlinearity region. The detail of the composite capacitor branch will be described later in this chapter.

16.3.3. Common-Mode Feedback

A fully differential operational amplifier requires CMFB capacitors to establish the common-mode voltage at its high-impedance output nodes. Figure 16.11 depicts a configuration of a fully differential amplifier employing CMFB. Sensing the common-mode voltage level using either resistors [16] or source follower often suffers from a limited linear output swing. The dynamic CMFB approach using SCs [17,18] for sensing the common-mode level, on the other hand, provides larger output swing as well as consuming less power. This technique is often employed in SC circuits. Figure 16.12 depicts an example of such a scheme.

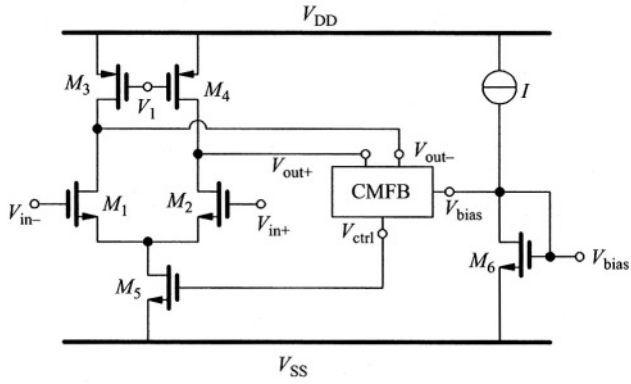


Figure 16.11. Fully differential amplifier incorporating CMFB.

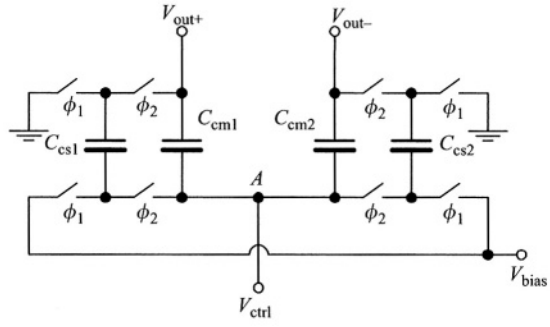


Figure 16.12. Switched capacitors common-mode feedback.

The structure works as follows: common-mode sensing capacitors, C_{cm1} and C_{cm2}, provide an AC feedback path from the output of the amplifier to node A. The DC level of the sensing capacitors, C_{cm1} and C_{cm2}, is defined and refreshed by capacitors C_{cs1} and C_{cs2} via the reference M_6 every cycle. Using linear capacitors, the average of the differential voltage at node A is zero, while any common-mode signals appear as an offset at node A. Then, the voltage at node A is compared with a reference voltage, and any difference will be fed back to control the current source, M_5.

One impact of using a MOSFET-capacitor for the sensing capacitors is to give rise to an imbalance of the signal voltage at node A which contributes an error voltage when the differential signals are applied. This error is voltage-dependent due to the MOSFET capacitors' characteristic, and hence results in a nonlinearity error at the output of the amplifier. The error due to this

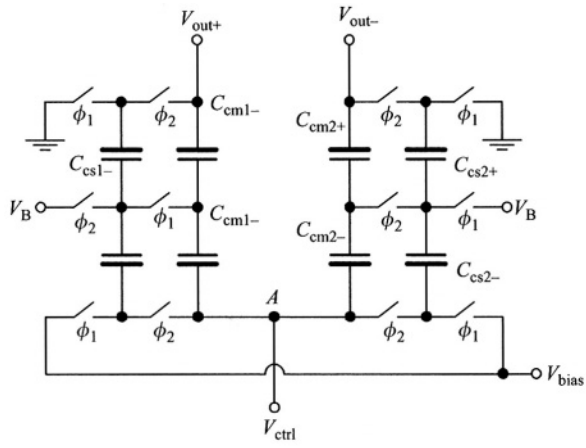


Figure 16.13. Series compensation CMFB capacitor branches.

MOSFET-capacitor can be avoided in the same way as the frequency variation of operational amplifiers. One way is to employ a metal–metal capacitor type. Since the sensing capacitors are normally small, the extra area penalty is negligible. Another is to use a composite linearity enhancement capacitor branch [13], as shown in Figure 16.13 where the capacitors are biased into weak nonlinear region by the bias voltage, V_B. More details of this capacitor arrangement will be given later in this chapter.

16.4. Charge-Domain Processing

Analog sampled-data signal processing requires only three basic operations: signal summation, scaling and delay. Since the summation of voltage signals is rather difficult to achieve directly, SC circuits make use of their amplifier's virtual earth input to sum current/charge and then convert this back to voltage at the amplifier's output. Usually, high-quality linear capacitors are needed to convert each input voltage to charge and then convert the summed charge back to a voltage, and this requirement has limited the compatibility of the technique with standard VLSI processes.

It has been shown [19] that provided voltage is linearly converted to charge at the input interface and from charge to voltage at the output interface, the signal processing core may operate in the charge-domain with voltage-dependent capacitors to produce an overall linear transfer characteristic. Consider the circuit in Figure 16.14(a). Given that all the capacitors are implemented with uniformly doped MOSFET gate structures, the voltage coefficients of all the capacitors are identical. The charge stored on the feedback capacitor, C_F, and

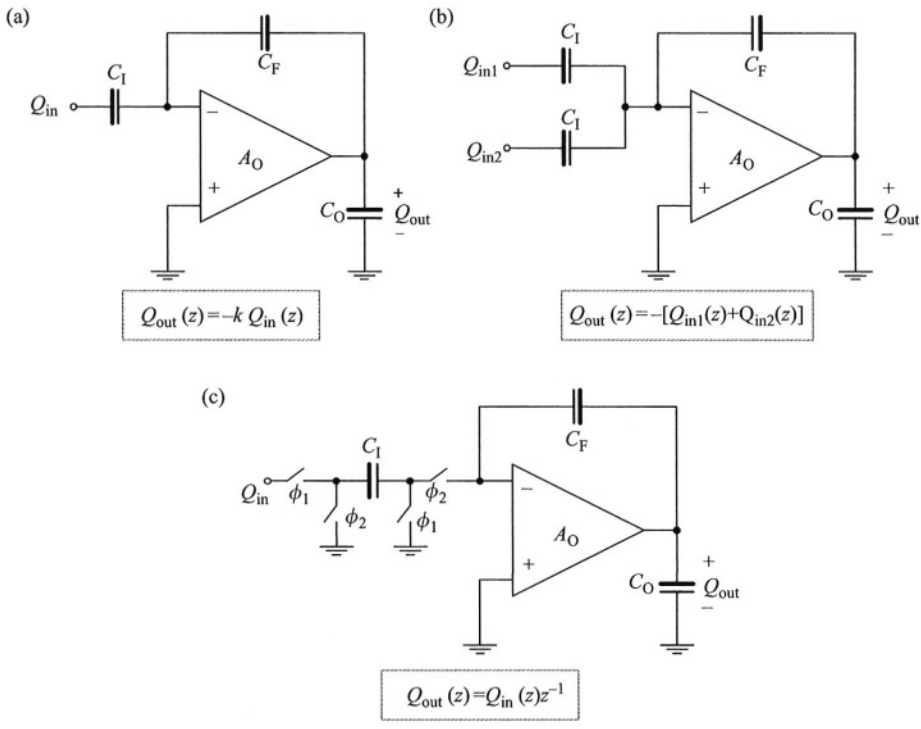


Figure 16.14. Three basic charge-domain processing operations.

the output capacitor, C_O, will be

$$Q_F = \int_0^{v_o} C_F(1 + \alpha_1 V + \alpha_2 V^2)dV$$

$$= C_F\left(1 + \frac{\alpha_1}{2}v_o + \frac{\alpha_2}{3}v_o^2\right)v_o \tag{16.9}$$

$$Q_{out} = \int_0^{v_o} C_O(1 + \alpha_1 V + \alpha_2 V^2)dV$$

$$= C_O\left(1 + \frac{\alpha_1}{2}v_o + \frac{\alpha_2}{3}v_o^2\right)v_o \tag{16.10}$$

Given $C_F = C$ and $C_O = kC$, where k is the area ratio of the output capacitor over the feedback capacitor. The charge transfer function is then given by

$$\frac{Q_{out}}{Q_F} = \frac{C_O\left(1 + \frac{\alpha_1}{2}v_o + \frac{\alpha_2}{3}v_o^2\right)v_o}{C_F\left(1 + \frac{\alpha_1}{2}v_o + \frac{\alpha_2}{3}v_o^2\right)v_o} = k \tag{16.11}$$

Therefore, the linear scaling of charge can be defined by the area ratio and is independent of the technological process.

$$Q_{out}(z) = -kQ_{in}(z) \tag{16.12}$$

From charge conservation, the summation and delay operations can also be achieved independently of the technology type of capacitor structure. Figure 16.14(b) shows the implementation of the summation operation. Given that the feedback capacitor C_F is equal to the output capacitor C_O, the charge stored on C_O is given by :

$$Q_{out}(z) = -(Q_{in1}(z) + Q_{in2}(z)) \tag{16.13}$$

The implementation of the delay cell is shown in Figure 16.14(c). Given that the feedback capacitor C_F is equal to the output capacitor C_O, the charge stored on C_O is given by

$$Q_{out}(z) = Q_{in}(z)z^{-1} \tag{16.14}$$

Hence, all the basic operations needed to perform sampled-data signal processing can be implemented in a standard digital CMOS process. Utilizing the MOSFET gate capacitors in the charge-domain processing circuit core is thus feasible without contributing any distortion. The accuracy of the charge-domain SC circuits will be affected by other component nonidealities, such as operational amplifier and switches, as with voltage-domain SC circuits.

Having the signal processing core implemented in the charge-domain, interfacing with the application voltage environment through charge/voltage converters still requires the use of high-quality linear capacitors. Possible options for these linear capacitors that are available in standard digital CMOS processes are *metal-over-metal* or *metal-over-poly* structures. Despite the larger area requirement of these types of capacitor structures over that of the *double-poly* structures, the entire system area will usually be smaller than with all *double-poly* capacitors being employed in the conventional SC system. For VLSI capacitor structures, area saving can be achieved when the required total internal core capacitance is at least ten times more than the input/output capacitance required for charge/voltage conversion.

One drawback when using the *metal-over-metal* or *metal-over-poly* capacitor structures at the front-end is that matching different types of capacitor structures accurately is virtually impossible. This makes the use of the MOSFET gate capacitors for the whole system more favorable. Yet, owing to their high voltage-dependence, linearity enhancement is consequently required for implementing the linear charge/voltage converters.

16.5. Linearity Enhanced Composite Capacitor Branches

High precision SC circuits employ high-quality floating capacitors to perform linear voltage-to-charge and charge-to-voltage conversion. These linear capacitors exhibit relatively constant capacitance over the total operating range of the signal voltages. Even so, the variation of capacitance value due to applied voltages gives rise to both gain error and nonlinearity. The nonlinearity of the capacitors can be modeled with a Taylor expansion as

$$C(V) = C_o\left(1 + \alpha_1 V + \alpha_2 V^2 + \cdots\right) \tag{16.15}$$

where α_1 is the first-order voltage coefficient and α_2 is the second-order voltage coefficient. For most applications, the first three terms are sufficient to represent the capacitor nonlinearity with reasonable accuracy.

Consider the case of the SC sample-and-hold amplifier (SHA), as shown in Figure 16.15. During the sampling phase, ϕ_1, input voltage, v_{in}, is sampled onto the capacitor C_S. Thus, the sampled charge, Q_i, on the capacitor is

$$\begin{aligned} Q_i &= \int_0^{v_{in}} C_S(1 + \alpha_1 V + \alpha_2 V^2)\mathrm{d}V \\ &= C_S v_{in}\left(1 + \frac{\alpha_1}{2} v_{in} + \frac{\alpha_2}{3} v_{in}^2\right) \end{aligned} \tag{16.16}$$

On the holdling phase, ϕ_2, the bottom plate of C_S is connected to ground, while the top plates of C_S and the feedback capacitor, C_F, are connected to the

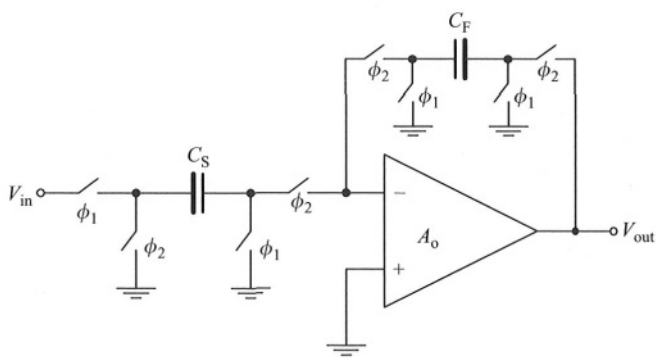


Figure 16.15. Switched-capacitor sample-and-hold amplifier.

amplifier's virtual earth. Charge, Q_o, flows onto the capacitor, C_F, given by

$$\begin{aligned} Q_o &= \int_0^{v_{out}} C_F(1+\alpha_1 V+\alpha_2 V^2)\mathrm{d}V \\ &= C_F v_{out}\left(1+\frac{\alpha_1}{2}v_{out}+\frac{\alpha_2}{3}v_{out}^2\right) \end{aligned} \tag{16.17}$$

From charge conservation, $Q_o = Q_i$ and so

$$\begin{aligned} v_{out} &= \frac{C_S}{C_F}v_{in}\frac{\left(1+\frac{\alpha_1}{2}v_{in}+\frac{\alpha_2}{3}v_{in}^2\right)}{\left(1+\frac{\alpha_1}{2}v_{out}+\frac{\alpha_2}{3}v_{out}^2\right)} \\ &\approx \frac{C_S}{C_F}v_{in}\left\{1+\frac{\alpha_1}{2}\left(1-\frac{C_S}{C_F}\right)v_{in}\right. \\ &\quad \left.+\left[\left(1-\left(\frac{C_S}{C_F}\right)^2\right)\frac{\alpha_2}{3}-\frac{C_S}{C_F}\frac{\alpha_1^2}{4}\right]v_{in}^2\right\} \end{aligned} \tag{16.18}$$

Letting $v_{in} = A\sin(\omega t)$, the second and third harmonics are

$$HD_2 = \left(1-\frac{C_S}{C_F}\right)\alpha_1\frac{A}{4} \tag{16.19}$$

$$HD_3 = \left[\left(1-\left(\frac{C_S}{C_F}\right)^2\right)\frac{\alpha_2}{3}-\frac{C_S}{C_F}\frac{\alpha_1^2}{4}\right]\frac{A^2}{4} \tag{16.20}$$

The effect of the capacitors' voltage coefficients on the linearity of the SC SHA is shown in Figure 16.16. Any non-zero voltage coefficient of the capacitance will result in an error in the sampled charge which contributes to gain error, as well as nonlinearity. For *double-poly* capacitor structures, the capacitors exhibit very low voltage coefficients (less than 200 ppm/V [20]). Hence, their effects on linearity can generally be neglected.

In standard digital CMOS processes, although the *metal-over-metal* and *metal-over-poly* capacitor structures exhibit reasonably low voltage-coefficients, their large area requirement and poor matching property make them unattractive. Particularly, when used to implement the linear voltage-to-charge and charge-to-voltage converters for the input/output interface, the ratio of these capacitor types is not accurately matched with the MOSFET gate capacitors in the circuit core. MOSFET gate capacitors are therefore preferred for their better area and matching. Unfortunately, the MOSFET gate capacitors are highly voltage-dependent. Hence, linearity enhancement is consequently needed when using these capacitors to perform linear voltage-to-charge and charge-to-voltage conversion.

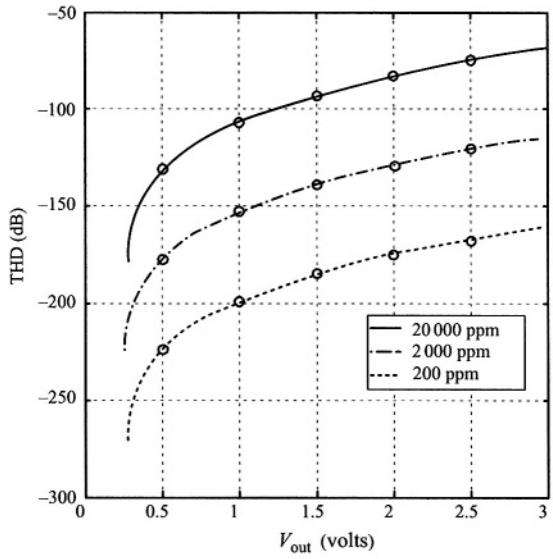


Figure 16.16. Effect of capacitor's voltage coefficient on linearity of switched-capacitor SHA.

In order to alleviate the nonlinearity effects of the MOSFET gate capacitor, a proper bias voltage must be provided to keep the capacitors operating either in the accumulation or inversion region [19]. Under these two operating regions, the MOSFET gate capacitors will exhibit only weak nonlinearity (Appendix A). The capacitor nonlinearity can therefore approximately be reduced to

$$C(V) = C_o(1 + \alpha V) \tag{16.21}$$

where α is the capacitor's first-order voltage coefficient. In practice, the choice of operating the MOSFET gate capacitor in the accumulation region is favorable. This is because less bias voltage is needed to keep the MOSFET capacitor operating in the accumulation region than in strong inversion for the same value of voltage coefficient.

Figure 16.17 shows the effect of voltage coefficient on the linearity of a SHA employing MOSFET capacitors biased into the accumulation region, assuming the other circuit components are ideal. As can be seen, simply biasing the MOSFET gate capacitors into the accumulation region can reduce higher order harmonic distortions. However, for high-precision SC circuits, further cancelation of the first-order harmonic distortion is still required. This is because, the simple biasing still suffers from the large value of the first-order voltage dependence (equation (16.15)), even when biased deep into the accumulation region. In addition, the SC circuit incorporating only the simple biasing technique requires an operational amplifier with large common-mode

input range to accommodate the bias voltage. This feature makes designing high-performance operational amplifiers very difficult, particularly in the low-voltage environment.

16.5.1. Series Compensation Capacitor Branch

The series compensation capacitor branch [21] has been proposed to further reduce the first-order nonlinearity, as well as avoid the need for large common-mode input range operational amplifiers. The series compensation capacitor branch, shown in Figure 16.18 is configured to keep the MOSFET capacitors in the accumulation region to perform first-order nonlinearity cancelation. In this technique, a conventional double-poly capacitor is replaced by two MOSFET

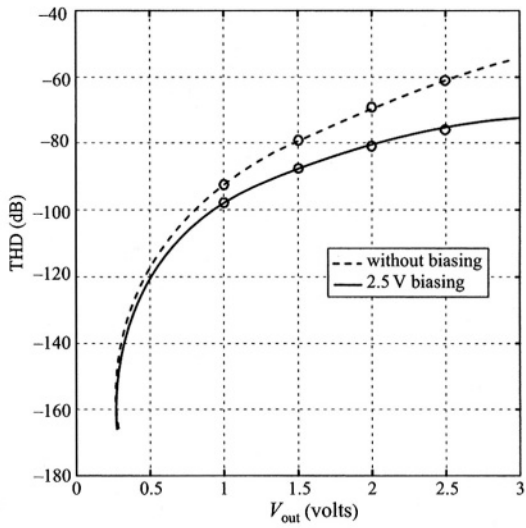


Figure 16.17. Effect of capacitor's voltage coefficient on linearity of simple biasing switched-capacitor SHA.

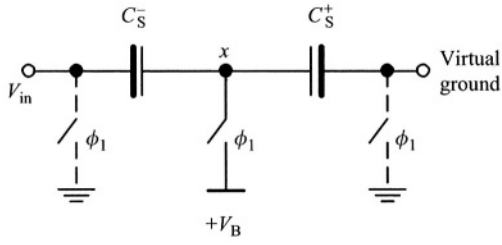


Figure 16.18. Series compensation capacitor branch.

gate capacitors connected back-to-back. Since the capacitors are connected in series, the voltage swing across each capacitor is smaller, resulting in a smaller operating range with consequent benefit to linearity.

Its operation is as follows: during the discharge phase, ϕ_1, the capacitor top plates are connected to the bias voltage, V_B, keeping them in the accumulation region. Then, in the output phase, ϕ_2, the input signal is applied at the input node while the other node is connected to virtual ground. Given both capacitors, C_S^+ and C_S^-, are equal to C_S and assuming that the voltage across each capacitor is half the input voltage, then the voltage at the floating node, x, will be given by

$$v_x = V_B + \frac{v_{in}}{2} \tag{16.22}$$

Thus, the charge stored on each capacitor is given by

$$\begin{aligned} Q_- &= \int_{v_{in}}^{v_x} C_B^+(1+\alpha V)\mathrm{d}V \\ &= C_S^- \left(V_B - \frac{v_{in}}{2}\right) + \frac{\alpha C_S^-}{2}\left(V_B - \frac{v_{in}}{2}\right)^2 \end{aligned} \tag{16.23}$$

$$\begin{aligned} Q_+ &= \int_0^{v_x} C_B^+(1+\alpha V)\mathrm{d}V \\ &= C_S^+ \left(V_B + \frac{v_{in}}{2}\right) + \frac{\alpha C_S^+}{2}\left(V_B + \frac{v_{in}}{2}\right)^2 \end{aligned} \tag{16.24}$$

Since the capacitors are connected in series, on the output phase, ϕ_2, they pass the same charge ΔQ due to v_{in}, given by

$$\begin{aligned} \Delta Q &= \frac{Q_+ - Q_-}{2} \\ &= \frac{C_S}{2}(1+\alpha V_B)v_{in} \end{aligned} \tag{16.25}$$

Since the bias voltage, V_B, is constant, the total charge exhibits only gain error because the nonlinear terms cancel. In practice, since the capacitors are voltage-dependent, the voltage across each capacitor in the series configuration will not be exactly half the voltage across the branch. Hence, from equations (16.23) and (16.24), the charge stored on each capacitor can be modeled as

$$\begin{aligned} Q_- &= C_S^-(V_B - v_{in} + v_x) + \frac{\alpha C_S^-}{2}(V_B - v_{in} + v_x)^2 \\ Q_+ &= C_S^+(V_B + v_x) + \frac{\alpha C_S^+}{2}(V_B + v_x)^2 \end{aligned} \tag{16.26}$$

where v_x is the signal voltage at the floating node. The delivered charge is given by

$$\Delta Q = \frac{C_S}{2}(1 + \alpha V_B + \alpha v_x)v_{in} - \frac{\alpha C_S}{4}v_{in}^2 \tag{16.27}$$

For nonlinear capacitors connected in series, when the input voltage, v_{in}, is applied, the voltage at the floating node, v_x, will approximately be

$$v_x = \left(1 + \frac{\alpha}{4}v_{in} - \frac{\alpha^2}{8}v_{in}^2\right)\frac{v_{in}}{2} \tag{16.28}$$

Hence, the delivered charge is

$$\Delta Q = \frac{C_S}{2}(1 + \alpha V_B)v_{in} + \frac{\alpha^2 C_S}{16}v_{in}^3 \tag{16.29}$$

The third-order harmonic will be

$$HD_3 = \frac{(\alpha A)^2}{32(1 + \alpha V_B)} \tag{16.30}$$

The magnitude of this nonlinearity error depends on the magnitude of the voltage coefficient of the capacitors and the parasitic capacitances at the floating node, *x*. Since the capacitors, C_S^+ and C_S^-, are connected in series, the required area of each capacitor has to be twice as large as that of the single capacitor realization for the same kT/C noise level [13]. Larger parasitic capacitances associated with the required area will result in larger nonlinearity, as well as extra power consumption required to drive these parasitic capacitances.

16.5.2. Parallel Compensation Capacitor Branch

Another technique with equivalent cancelation of capacitor nonlinearity is developed in the parallel compensation capacitor branch [22] as shown in Figure 16.19. This structure is based on the anti-parallel connection of two series compensation capacitor branches. In parallel compensation, two MOSFET gate capacitors are cascaded with two bias-holding capacitors, C_H, and then combined in parallel. When the input signal is applied to the capacitors, the voltage across one of the capacitors is increased, while the other is decreased. Therefore, the first-order nonlinearity of the transferred charge is canceled out. This structure still suffers from the capacitors' voltage coefficients and the parasitic capacitances at the floating nodes, x_1 and x_2, as in the series structure. Moreover, their effects are worse still in the parallel configuration because one of the two floating nodes is connected to the bottom plate of the MOSFET gate capacitor. The effect of the parasitic capacitances is much greater, and so reduces the accuracy as well as linearity.

16.5.3. Balanced Compensation Capacitor Branch

In both series and parallel compensation structures, the nonlinearity cancelation occurs on the phase when the input signal is applied. Hence, they can only be applied to non-delay SC circuits, such as the inverting integrator and amplifier [13,23]. In an attempt to include also delay circuits, that is, the noninverting and SHA, the balanced compensation capacitor branch [24] has been proposed as an alternative approach to correspondingly suppress the first-order nonlinearity. Figure 16.20 shows the proposed balanced compensation capacitor structure. The technique's cancelation occurs on the output phase and this makes it suitable for the delay class of circuits. As with the series compensation, the bias voltages, V_B, are provided to keep the sampling capacitors, C_B^+ and C_B^-, operating in the accumulation region. Instead of connecting the

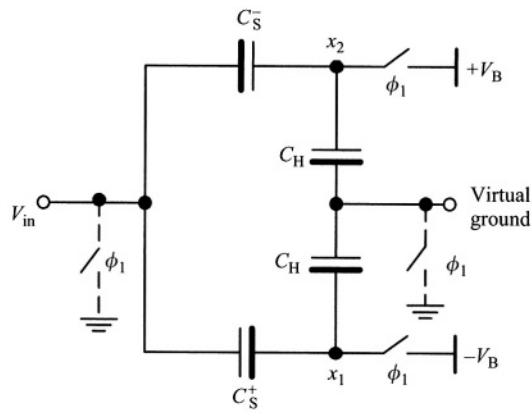


Figure 16.19. Parallel compensation capacitor branch.

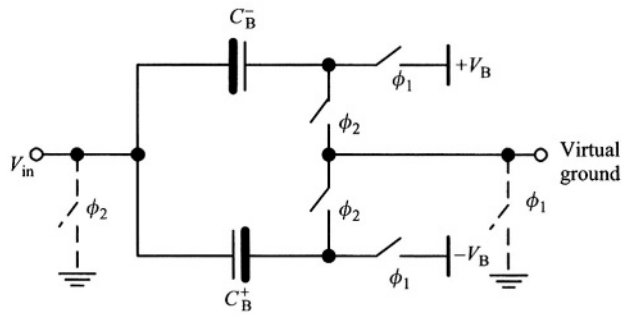


Figure 16.20. Balanced compensation capacitor branch.

capacitors in series, they are connected in anti-parallel to achieve first-order nonlinearity cancelation. The configuration of the balanced structure is similar to the parallel structure, but with no holding capacitor.

Its operation is as follows: during the sampling phase, ϕ_1, the top plate of the sampling capacitor C_B^+ is connected to the positive bias voltage, $+V_B$, while the bottom plate of the sampling capacitor C_B^- is connected to the negative bias voltage, $-V_B$. The input voltage V_{in} is sampled directly onto the bottom plate of the capacitor C_B^+ and the top plate of the capacitor C_B^-. The bias voltages keep both MOSFET gate capacitors operating in the accumulation region while the input signal is sampled and so the capacitors exhibit only weak nonlinearity. The sampled charge Q_- stored on the sampling capacitor C_B^- is

$$\begin{aligned} Q_- &= \int_{v_{in}}^{V_B} C_B^-(1+\alpha V)\mathrm{d}V \\ &= C_B^-\left(V_B - v_{in}\right) + \frac{\alpha C_B^-}{2}\left(V_B - v_{in}\right)^2 \end{aligned} \tag{16.31}$$

while the sampled charge Q_+ stored on the sampling capacitor, C_B^+ is

$$\begin{aligned} Q_+ &= \int_{-V_B}^{v_{in}} C_B^+(1+\alpha V)\mathrm{d}V \\ &= C_B^+\left(V_B + v_{in}\right) + \frac{\alpha C_B^+}{2}\left(V_B + v_{in}\right)^2 \end{aligned} \tag{16.32}$$

At the end of the sampling phase, ϕ_1, the bias voltages are disconnected from the capacitors. The top plate of the capacitor C_B^+ is connected to the bottom plate of the capacitor C_B^-, and then connected to the feedback capacitor at the virtual ground. Assuming the capacitors C_B^+ and C_B^- are equal to C_B, the delivered charge ΔQ that flows into the feedback capacitor is given by

$$\begin{aligned} \Delta Q &= Q_+ - Q_- \\ &= 2C_B\left(1+\alpha V_B\right)v_{in} \end{aligned} \tag{16.33}$$

The first-order nonlinearity is canceled out, leaving only a gain error with the same magnitude as that of the series structure. The total charge possesses a gain of two, because of the parallel structure, and the required capacitor area of the balanced structure is then four times less than that of the series structure for the same kT/C noise level. Consequently, the balanced structure has lower parasitic capacitance, better area efficiency and lower power consumption.

16.6. Practical Considerations

Any imperfections of the components will degrade the accuracy of all of the linearity enhancement composite capacitor branches. Practical mismatches of these components are unfortunately inevitable and random in nature, and will result in non-ideal cancelation. Their effects on accuracy can be examined through the approximate analyses [25] as follows.

16.6.1. Bias Voltage Mismatch

Any mismatch in the bias voltages will affect only the parallel and balanced capacitor structures. Sources of these mismatches can be divided into static and random mismatches. The static mismatch arises through the bias line variation causing static voltage errors. The random mismatch is due to noise on the bias lines. If supply voltages are used as bias voltages, the effects of the bias voltage mismatch due to noise will be greater. Given $+V_B = V$ and $-V_B = -(V+\delta V)$ in the balanced compensation structure, from equation (16.31) and (16.32), the charges stored on each capacitor will then be

$$Q_- = C_B(V - v_{in}) + \frac{\alpha C_B}{2}(V - v_{in})^2$$

$$Q_+ = C_B(V + \delta V + v_{in}) + \frac{\alpha C_B}{2}(V + \delta V + v_{in})^2 \qquad (16.34)$$

Thus, the total charge stored on the capacitor branch is given by

$$\Delta Q = (1+\alpha V)\delta V C_B + 2C_B\left(1 + \alpha\left(V + \frac{\delta V}{2}\right)\right)v_{in} + \frac{\alpha C_B}{2}(\delta V)^2 \qquad (16.35)$$

The mismatch voltage, δV, is composed of the static mismatch of the bias voltages which is fixed, and the mismatch due to noise which is time varying. So static mismatch contributes only offset and gain error, whereas noise contributes additional spurious signals. To reduce this, a fully differential topology should be employed in the circuits, since the noise and offset are then common-mode.

16.6.2. Capacitor Mismatch

As the nonlinearity cancelation operation is similar in the series and balanced compensation techniques, the effects of capacitor mismatch in both structures will be the same. Given $C_B^- = C$ and $C_B^+ = C + \delta C$ in the balanced compensation structure, from equation (16.31) and (16.32), the charges stored on each capacitor are

$$Q_- = C(V_B - v_{in}) + \frac{\alpha C}{2}(V_B - v_{in})^2$$

$$Q_+ = (C + \delta C)(V_B + v_{in}) + \frac{\alpha}{2}(C + \delta C)(V_B + v_{in})^2 \qquad (16.36)$$

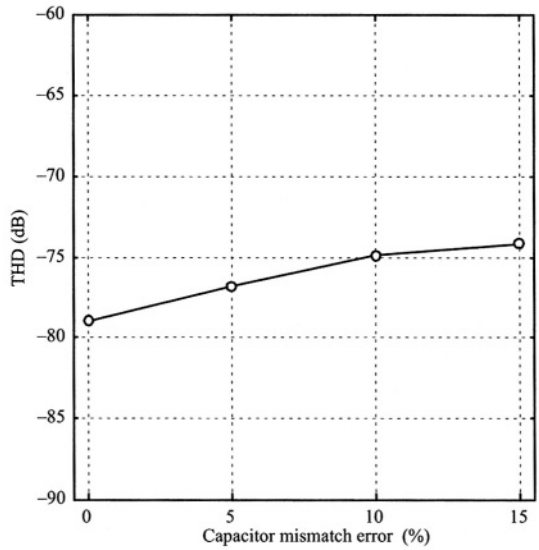


Figure 16.21. Effect of capacitor mismatch on linearity.

Therefore, the total charge stored on the balanced capacitor branch is given by

$$\Delta Q = \delta C V_B + (\delta C + 2C)(1 + \alpha V_B)v_{in} + \frac{\alpha \delta C}{2} V_B^2 + \frac{\alpha \delta C}{2} v_{in}^2 \qquad (16.37)$$

Capacitor mismatch results in offset, gain and nonlinearity errors. Figure 16.21 shows the simulated effect of capacitor mismatch on linearity. It can be seen that capacitor mismatch as large as 15% decreases the linearity by 5%. Fortunately, this nonlinearity depends upon the matching of two capacitors rather than their absolute value, where the capacitors can be matched as accurate as 0.1%. With proper layout the nonlinearity error caused by capacitor mismatch is therefore negligible. Consequently, to a first-order approximation the capacitor mismatch contributes only offset and gain errors.

16.6.3. Parasitic Capacitances

Parasitic capacitances can usually be rendered ineffective by utilizing stray-insensitive structures. This is the case with the balanced structure, but not with the series or parallel structures. In the series structure, although the parasitic capacitances from the bottom plate are placed at the stray-insensitive node, the top plate parasitic capacitances are not. Since nonlinearity cancelation in the series structure requires the balancing of the voltages across each capacitor, the effect of parasitic capacitance will be to add an error voltage to the floating node, *x,* and hence, contribute nonlinearity as in equation (16.37). The magnitude of

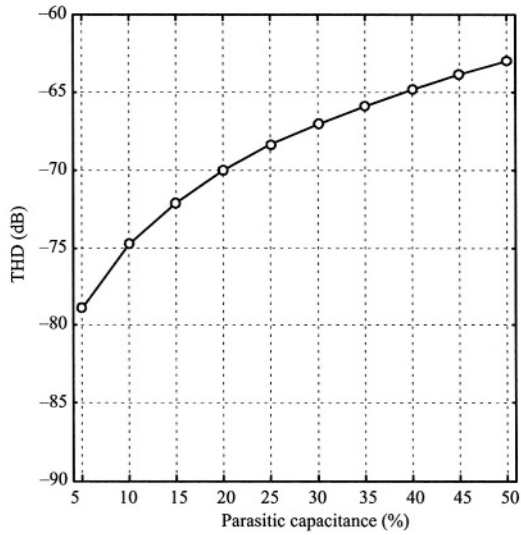


Figure 16.22. Effect of parasitic capacitances on linearity.

this error depends on the amount of parasitic capacitance at the floating node, and the voltage coefficient of the capacitors.

Figure 16.22 shows the simulated effect of parasitic capacitance on linearity at the floating node, *x,* of the series structure (Figure 16.18). From the simulution results, bottom plate parasitic capacitance at the floating node as large as 50% decreases the linearity by 15%. Since the bottom plate parasitic capacitance of the MOSFET capacitor is usually large, the floating node must then be connected to the capacitors' top plates to avoid the undesired distortion. However, the effect of the parasitic capacitance is worse still in the parallel configuration where one of the two floating nodes is unavoidably connected to the bottom plate of the MOSFET gate capacitor. The effect of the parasitic capacitance is much greater, and so reduces the accuracy as well as linearity.

16.7. Summary

Compatibility of SC circuits with standard VLSI processes is feasible using MOSFET gate capacitors. In this chapter, the charge-domain principle has been discussed, where the signal is processed within charge signal variables. Thus, the linearity of the transfer function is preserved as long as the circuit structures fulfill the required condition. Three basic operations have been presented, where their extensions to implement the more systematic applications will be discussed in Chapter 17. Interfacing the charge-domain processors with the voltage environment can be obtained by employing the linearity enhancement composite capacitor branches. Simulated verifications were carried out to

demonstrate the effectiveness of these techniques and have shown significant improvement.

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Chapter 17

SWITCHED-CAPACITORS OR SWITCHED-CURRENTS – WHICH WILL SUCCEED?

John Hughes and Apisak Worapishet

17.1. Introduction

Since its introduction in the late 1980s [1–5], "switched-currents" (SI) has become the main contender to supercede the ubiquitous "switched-capacitors" (SC). Its main claim has always been that it is a technique requiring only the same basic CMOS IC process, that is, used for digital signal processing, a property that made it highly suitable as the sampled analog signal processing technique for mixed-signal systems. This came about because of SI's "MOSFET-only" circuit style, made possible through its use of charge *storage,* rather than the charge *transfer* used by many SC circuits, and this could be performed on grounded, non-linear capacitances of the sort that occur naturally at the gate of any MOS transistor. So, SI has always promised cost savings through the use of the cheapest possible CMOS processing.

Early SI circuits were very simple. The basic track-and-hold function required only a pair of complementary MOS transistors, one as the storage device and the other to provide its bias current, and a few MOS switches to effect sampling. The cell merged the properties of storage and buffering into the same physical area (the memory transistor) whereas SC required separate storage (usually linear floating capacitors) and buffering (OTAs). So, further economies could be expected through reduction of chip area. The simplicity of the circuits also suggested that SI was capable of higher sampling frequencies than SC which was limited by compensation and slewing in its OTAs. This promised SI a good future for video and higher frequency applications [6].

During the development of SI, CMOS processing experienced regularly increasing chip complexity made possible by continual reductions in feature sizes. This phenomenon could only be sustained through a reduction of supply voltage and analog circuits have had to respond to this. The performance of SC was directly impacted, since with reduced signal *voltage* swings, signal-to-noise ratio (SNR) could only be maintained by a reduction in noise which required larger capacitors. With SI, there was no such restriction to the signal *current* swings, but instead the reduced supply voltage necessitated the use of higher (trans)conductance devices which generated more noise. Nevertheless,

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it was hoped that ways could be found for SI to benefit from this trade-off at lower supply voltage.

With such a promise, it is perhaps surprising that SI has not yet found full acceptance in the industry. One explanation for this is that, apart from a few exceptions (e.g. [7]), the reported level of SI performance has not yet reached that of SC and the shortfall has outweighed SI's cost advantage. Another is that SC also has made great strides to adapt itself to "MOSFET-only" solutions [8]. So, is the case for SI purely anecdotal? Are there fundamental reasons that restrict the performance of SI? In this chapter, we attempt to answer this through a rigorous theoretical analysis of SI and SC to examine the underlying differences that influence the debate and we attempt to answer the question "How do the performances of SI and SC compare in today's processes and how will they compare in the future?". We start by justifying our choice of cells for the performance comparison and outline our strategy of assessing performance through a figure-of-merit (FoM). Next, we analyze the limiting clock frequency, power consumption and SNR for each cell and derive expressions for the FoM. This FoM is then used to compare current performance and to predict the performance trend with future CMOS processing.

17.2. Test Vehicles and Performance Criteria

Making comparisons in an even-handed manner is never easy and comparing SC and SI is no exception. We could have simply compared published performance but this would have suffered from reliance on the level of designer skill and the state of the technique's development. Instead, we chose to adopt an analytic approach to enable comparison based on fundamental considerations.

The first choice to be made was that of circuit topology. Sampled analog circuits, either SC or SI, are used primarily to interface to the digital domain, performing such functions as filtering and data conversion. The filters are usually of low order, often conditioning the signals before or after data conversion. While the chosen sampled analog technique must have a capability for all such functions, the designer's highest priority will usually be for the data converter and for this reason we have chosen the track-and-hold as our test vehicle. This is an essential component of any pipeline ADC, of the sample-and-hold function and, in the case of SI, is the primitive cell used in the filter's integrators as well. The track-and-hold cell (also called the memory cell or current copier in SI) has been highly developed over the years in both SC and SI techniques, but rather than focus on sophisticated cells we prefered to compare the simplest versions so that circuit complication would not detract from fundamental issues.

The circuit vehicles are shown in Figure 17.1. For SC, the basic class A stage shown in Figure 17.1(a) was chosen as this has a simple MOS complementary pair as its buffer amplifier. A more practical circuit might deploy an OTA as

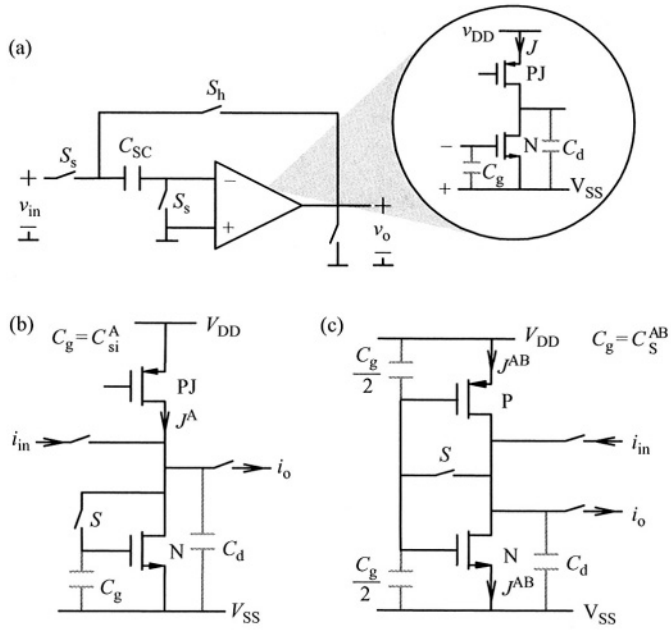


Figure 17.1. Test circuits (a) SC (b) class A SI and (c) class AB SI memory cells.

simple as a telescopic OTA or as complex as a gain-boosted OTA. For SI, the basic class A and class AB stages shown in Figure 17.1(b) and (c) were chosen because they use the same simple MOS complementary pair for buffering and memory. A more practical circuit might use an enhancement technique such as two-step sampling [9] or zero-voltage switching [10].

Having chosen the circuit vehicles to be used for this comparison, our next task was to decide on the performance vectors. A full set might have included clock (i.e. sampling) frequency, power consumption, SNR, precision, harmonic distortion, power supply rejection and cost. These are all subject to design trade-offs and assume different priorities depending on the demands of the application. Some are difficult to calculate and others are highly technology-dependent. So, to ease these difficulties we decided to conduct our appraisal based on the three principal performance vectors, clock frequency (F_c), signal-to-noise ratio (SNR) and power consumption (P), combined into a figure-of-merit (FoM) defined as,

$$\text{FoM} = F_c \frac{\text{SNR}}{P} \tag{17.1}$$

A more comprehensive FoM embracing both noise and distortion may be possible using the concepts described in [11] but this is not attempted here.

In the following sections, we will develop expressions for FoM for each of the test circuits and throughout the analyses will be performed in the context of a 1 bit/stage pipeline ADC.

17.3. Clock Frequency

First, the operation of the test cells is described with reference to Figure 17.2. The SC circuit (Figure 17.2(a)) has a sampling or input phase ϕ_1 during which the buffer amplifier (N,PJ) is open loop while the sampling capacitor C_{SC} samples the input voltage v_{in}. On the hold or output phase ϕ_2, the buffer

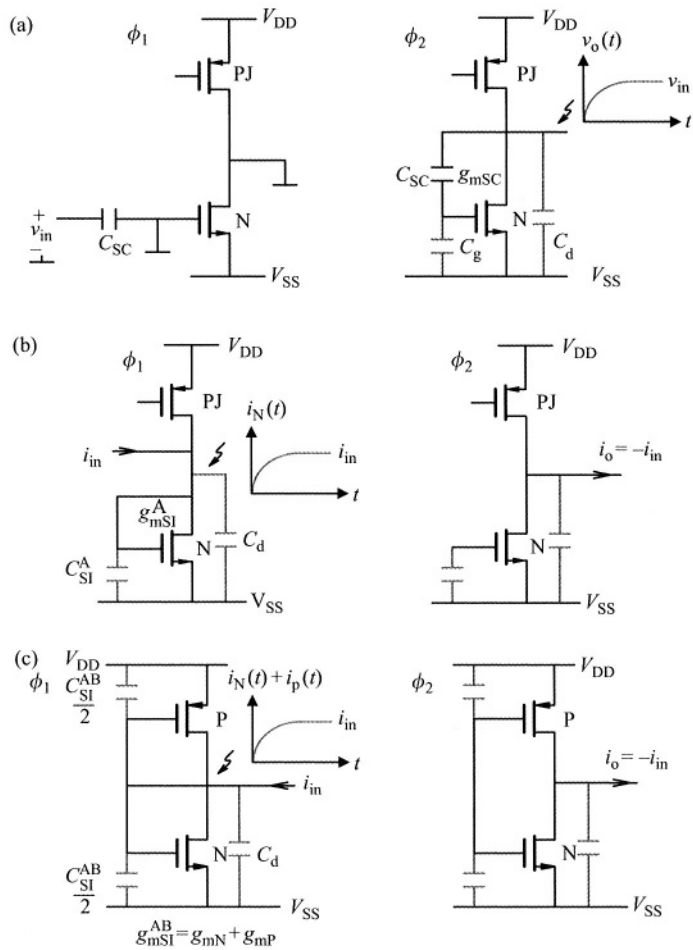


Figure 17.2. Operation of the memory cells (a) SC (b) class A SI and (c) class AB SI circuits.

amplifier's feedback loop is closed by the connection of C_{SC} and the loop settles to produce the output voltage v_o, which is close to v_{in}.

The SI circuits (Figure 17.2(b) and (c)) have a sampling phase ϕ_1 during which the buffer amplifier is in a closed loop due to the closure of the memory switch *S*. The voltage on its sampling capacitor(s) ($C_g = C_{SI}^{A(AB)}$) settles to a value determined by the input current i_{in} and the transconductance of the memory transistor(s) $g_{mSI}^{A(AB)}$. On the hold phase ϕ_2, the buffer amplifier is open loop and the voltage held on C_g together with the same transconductance $g_{mSI}^{A(AB)}$ produces an output current i_o which is close to i_{in}.

Clearly, the cells' operation demonstrates the duality that exists between voltage and current mode circuits. The SC circuit presents a high input impedance with its buffer amplifier's loop open on its sampling phase and a low output impedance with the loop closed and settling on its output phase. On the other hand, the SI circuits present a low input impedance with their buffer amplifier's loop closed and settling on their sampling phase and a high output impedance with their loops open on their output phase. The allowed clock frequency will be determined by the settling behavior when the buffer amplifier's loop is closed, that is, during the SC's ϕ_2 phase or during the SI's ϕ_1 phase.

17.3.1. Switched-Capacitor Settling

This section focuses on the analysis of the settling behavior during the hold phase ϕ_2 of the SC circuit. The small-signal model used for the SC settling analysis is shown in Figure 17.3. Its configuration represents a section of a pipeline where the $(n-1)$th stage is settling while its output is loaded by the nth stage. All relevant parasitic components of the switch and buffer are included.

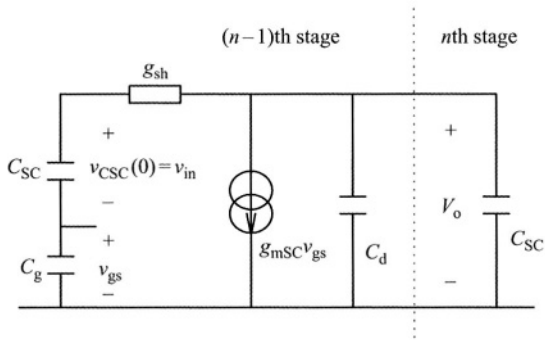


Figure 17.3. Small-signal model for cascaded SC memory cells during the hold phase of the $(n-1)$th stage.

The output voltage during the hold phase can be expressed in the s-domain as,

$$v_o(s) = \frac{v_{C_{SC}}(0)\left(C_g/g_{mSC} + 1/s\right)}{(C_{SC}/g_{sh})\left(\left(C_{SC}+C_g\right)/g_{mSC}\right)s^2 + \left(\left(\left(C_d + 2(C_{SC}+C_g)\right)\right)/g_{mSC}\right)s + 1} \tag{17.2}$$

where $v_{C_{SC}}(0) = v_{in}$ is the output voltage of the $(n-1)$th stage which is subsequently stored on C_{SC} of the nth stage at the end of the sampling phase, C_d is the capacitance at the common drain node, C_g is the gate capacitance of the amplifier transistor N in Figure 17.1(a), g_{sh} is the conductance of the hold switch S_h and g_{mSC} is the transconductance of the transistor N. Putting $C_d = \alpha C_g$ (where the proportionality constant α is dependent on the geometry of the memory cell layout), it has been shown that the condition for minimum settling in the SC circuit is $C_g = C_{SC}/\sqrt{\alpha}$ and hence $C_d = \sqrt{\alpha}C_{SC}$ [12]. Thus, the response in equation (17.2) may be rewritten as

$$v_o(s) = \frac{v_{in}\left(\tau_3 + 1/s\right)}{\tau_1\tau_2 s^2 + \tau_1 s + 1} \tag{17.3}$$

where

$$\begin{aligned} \tau_1 &= \left(\sqrt{\alpha} + 2 + \frac{2}{\sqrt{\alpha}}\right)\cdot\frac{C_{SC}}{g_{mSC}} \\ \tau_2 &= \frac{\left(1 + 1/\sqrt{\alpha}\right)}{\left(\sqrt{\alpha} + 2 + 2/\sqrt{\alpha}\right)}\cdot\frac{C_{SC}}{g_{sh}} \\ \tau_3 &= \frac{1}{\sqrt{\alpha}}\cdot\frac{C_{SC}}{g_{mSC}} \end{aligned} \tag{17.4}$$

The equation can be further simplified by neglecting $\tau_3 < \sqrt{\tau_1\tau_2}$.[1] From equation (17.3), the settling time may be minimized by choosing the switch on-conductance g_{sh} so that $\tau_1 = 4\tau_2$ to make the loop critically damped. This value of g_{sh} is given by

$$g_{sh} = \frac{4\left(1 + 1/\sqrt{\alpha}\right)}{\left(\sqrt{\alpha} + 2 + 2/\sqrt{\alpha}\right)^2}\cdot g_{mSC} \tag{17.5}$$

Under this critically damped condition, equation (17.3) can then be expressed as

$$v_o(s) = \frac{v_{in}}{s\left((\tau_1/2)s + 1\right)^2} \tag{17.6}$$

---

[1] Numerical calculation shows that this approximation results in less than 5% error.

where τ_1 is as defined in equation (17.4). From the simplified transfer function given in equation (17.6), it can be shown that the stage requires a minimum settling time of $\sim 4.5\tau_1$ to settle to within the 0.1% accuracy. Assuming that the sampling time T_s and the hold time T_h of the memory circuit are equal, the maximum clock frequency $F_c = T_c^{-1} = (2T_h)^{-1}$ in the SC memory cell then becomes

$$F_{SC} = \frac{1}{2 \times 4.5\tau_1} = \frac{1}{9\left(\sqrt{\alpha} + 2 + 2/\sqrt{\alpha}\right)} \cdot \frac{g_{mSC}}{C_{SC}}$$
$$= \frac{1}{9\left(\sqrt{\alpha} + 2 + 2/\sqrt{\alpha}\right)} \cdot \frac{2J}{V_{gtSC} C_{SC}} \tag{17.7}$$

where $g_{mSC} = 2J/V_{gtSC}$, and J and V_{gtSC} are the bias current and the gate–source overdrive voltage of the amplifier transistor N of the SC cell shown in Figure 17.1(a).

17.3.2. Switched-Currents Class A Settling

The small-signal model for the class A SI settling analysis is shown in Figure 17.4. As with the SC model, its configuration represents a section of a pipeline but in this case the nth stage is settling while being loaded at its input by the $(n-1)$th stage. Again, all relevant parasitic components of the switches and amplifier are included.

The s-domain response can be expressed as

$$i_o(s) = \frac{i_{in}}{(2C_d/g_s)(C_g/g_{mSI}^A)s^2 + ((2C_d + C_g)/g_{mSI}^A)s + 1} \tag{17.8}$$

where i_{in} is output current of the $(n-1)$th stage which is supplied as a step input to the nth stage, g_s is the conductance of the sampling switch S and g_{mSI}^A is

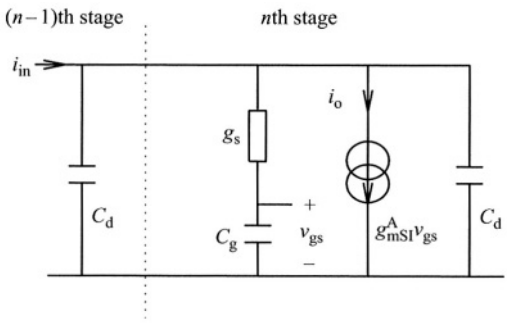


Figure 17.4. Small-signal model for cascaded SI memory cells during the sampling phase of the nth stage.

the transconductance of the memory transistor N in Figure 17.1(b). By putting $C_d = \alpha C_g = \alpha C_{SI}^A$, the response in equation (17.8) may be rewritten as

$$i_o(s) = \frac{i_{in}}{\tau_1 \tau_2 s^2 + \tau_1 s + 1} \tag{17.9}$$

where

$$\begin{aligned} \tau_1 &= (1 + 2\alpha) \cdot \frac{C_{SI}^A}{g_{mSI}^A} \\ \tau_2 &= \frac{2\alpha}{(1 + 2\alpha)} \cdot \frac{C_{SI}^A}{g_s} \end{aligned} \tag{17.10}$$

From equation (17.9), the settling time may be minimized by choosing the switch on-conductance g_s so that $\tau_1 = 4\tau_2$ to make the loop critically damped. The value of conductance g_s needed is given by

$$g_s = \frac{8\alpha}{(1 + 2\alpha)^2} \cdot g_{mSI}^A \tag{17.11}$$

Under this critically damped condition, equation (17.9) can be expressed as,

$$i_o(s) = \frac{i_{in}}{((\tau_1/2)s + 1)^2} \tag{17.12}$$

As in the case of the SC memory cell, under a step input i_{in}, this is the response which gives maximum clock frequency in the SI memory cell. This maximum clock frequency is given by

$$\begin{aligned} F_{SI}^A &= \frac{1}{2T_s} = \frac{1}{9\tau_1} = \frac{1}{9(1 + 2\alpha)} \cdot \frac{g_{mSI}^A}{C_{SI}^A} \\ &= \frac{1}{9(1 + 2\alpha)} \cdot \frac{2J^A}{V_{gtSI}^A C_{SI}^A} \end{aligned} \tag{17.13}$$

where $g_{mSI}^A = 2J^A / V_{gtSI}^A$, J^A and V_{gtSI}^A are the bias current and the gate–source overdrive voltage in the memory transistor N of the class SI cell shown in Figure 17.1(b).

17.3.3. Switched-Currents Class AB Settling

As the small-signal model for analyzing the settling behavior of the class AB memory cell shown in Figure 17.1(c) is identical to that for the class A cell in Figure 17.1(b), the expression for the maximum clock frequency in equation

(17.13) may also be applied in this case but with g_{mSI}^{AB} equal to the sum of the transconductances in memory transistors N and P of Figure 17.1(c), that is,

$$F_{SI}^{AB} = \frac{1}{9(1+2\alpha)} \cdot \frac{g_{mSI}^{AB}}{C_{SI}^{AB}} = \frac{1}{9(1+2\alpha)} \cdot \frac{4J^{AB}}{V_{gtSI}^{AB} C_{SI}^{AB}} \tag{17.14}$$

where $g_{mSI}^{AB} = g_{mN} + g_{mP} = 4J^{AB}/V_{gtSI}^{AB}$ (assuming $g_{mN} = g_{mP}$), J^{AB} and V_{gtSI}^{AB} are the quiescent bias current and the gate–source overdrive voltage of the memory transistor N or P.

17.4. Power Consumption

17.4.1. Switched-Capacitors and Switched-Currents Class A Power Consumption

Due to the class A operation, the power consumptions in the circuits are simply equal to,[2]

$$P_{SC} = JV_{DD} \tag{17.15}$$

$$P_{SI}^{A} = J^{A}V_{DD} \tag{17.16}$$

17.4.2. Switched-Currents Class AB Power Consumption

The relationship between the power consumption and the quiescent bias current J^{AB} in this case is not as simple as that in the class A cells due to the signal-dependent supply current variation in class AB operation. For a balanced configuration of the class AB SI circuit in Figure 17.1(c) with a *peak* sinusoidal input current $(= 4J_{AB})$, it can be shown that the *average* power consumption in one-half of the circuit is given by

$$P_{SI}^{AB} = \frac{3}{2} J^{AB} V_{DD} \tag{17.17}$$

17.5. Signal-to-Noise Ratio

Noise errors in both the SC and SI memory cells result from the thermal and flicker or $1/f$ noise inherent in MOS transistors. During the operation

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[2] Only the power in the nth stage is considered.

of all the memory cells in Figure 17.1, the input signal is sampled on one clock phase and then held on the other. Any noise introduced with the signal or from its own MOS transistors undergoes the same sampling process. Noise with frequency components higher than the Nyquist rate $(F_c/2)$, such as thermal noise, being undersampled, is aliased back into the baseband (0 to $F_c/2$). This noise is called "sampled noise". Although the sampling process reshapes the noise power spectral density (NPSD) this occurs without changing its power. Noise with relatively low frequency components compared to the Nyquist rate, particularly the $1/f$ noise, is oversampled and easily removed from the baseband by correlated double sampling in either SC or SI. Hence, in the following analysis we have only considered thermal noise.

Considering only thermal noise, the single-sided NPSD of a noise current i_{nT} from a saturated transistor is given by

$$S_{nT} = \frac{\overline{i_{nT}^2}}{\Delta f} = \frac{8}{3} kT g_m \quad 0 < f < \infty \tag{17.18}$$

and a MOS switch has an associated noise voltage v_{nS} with NPSD given by

$$S_{nS} = \frac{\overline{v_{nS}^2}}{\Delta f} = \frac{4kT}{g_s} \quad 0 < f < \infty \tag{17.19}$$

where k is Boltzmann's constant, T is the absolute temperature, g_m is the transconductance of the transistor and g_s is the switch on-conductance.

During the hold phase of the memory cell (either SC or SI) the sampled noise is delivered to the output as an error signal. In addition, the same noise sources which were just sampled are still active and create extra unsampled noise, called "direct noise", to flow from the output where it adds to the noise error samples. In the context of our pipeline ADC, the noise error samples propagate without further processing down the pipeline where they accumulate with noise samples from other stages. In the noise analyses that follow, we must focus on the process by which all active noise is sampled. This will include both the active noise within the stage on its sampling phase (say the nth stage) and the "direct noise" from the previous stage (the $(n-1)$th stage).

17.5.1. Switched-Capacitors Noise

The model for examining noise in SC cells is shown in Figure 17.5. As with the models used for the settling analyses, these include all relevant switch and amplifier parasitics. The memory switch noise is represented by the noise voltage source, v_{nSh}, and the amplifier noise by the current noise sources, i_{nN} and i_{nJ}. Each of these noise sources contributes to the "direct noise" power leaving the $(n-1)$th stage to be sampled onto C_{SC} of the nth stage. The noise

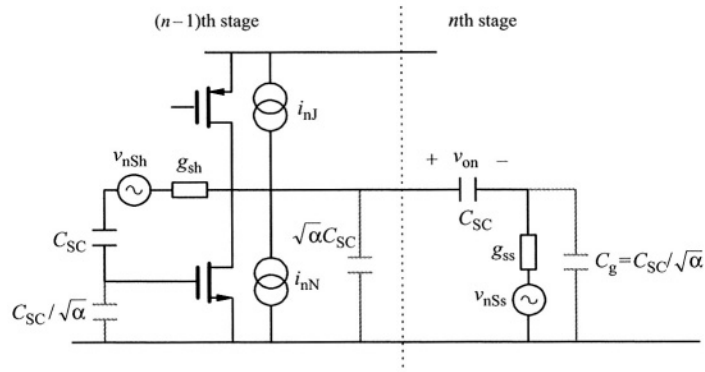


Figure 17.5. Small-signal model for noise calculation in SC memory cell.

powers arriving at C_{SC} from each noise source are found by multiplying each of the noise source's power by the square of the transfer response to the output. The total noise power is found by summing the individual output noise powers.

Saturated transistor noise power. From the model in Figure 17.5, it can be shown that the noise transfer characteristic from i_{nN} (or i_{nJ}) to the output $v_{onN(J)}$ of the $(n-1)$th stage is

$$H(s) = \frac{v_{on}(s)}{i_{nN(J)}(s)} = \frac{\left(1 + 1/\sqrt{\alpha}\right)}{g_{mSC}} \cdot \frac{1}{\tau_1 \tau_2 s^2 + \tau_1 s + 1} \tag{17.20}$$

where τ_1 and τ_2 are as defined in equation (17.4) and the approximation $g_{ss} = \infty$ has been used to simplify this analysis. By describing the noise transfer characteristic in this form, the sampled noise power in the baseband can be simply evaluated by using the concept of equivalent noise bandwidth $\mathbf{BW_n}$ [13]. Thus, the output noise power resulting from i_{nN} (or i_{nJ}) is equal to

$$\begin{aligned}
\bar{v}^2_{onN(J)} &= \int_0^\infty S_{nN(J)} |H(j2\pi f)|^2 \, df \\
&= S_{nN(J)} \cdot \frac{\left(1 + 1/\sqrt{\alpha}\right)^2}{g^2_{mSC}} \cdot \mathrm{BW_n} \\
&= S_{nN(J)} \cdot \frac{\left(1 + 1/\sqrt{\alpha}\right)^2}{g^2_{mSC}} \cdot \frac{1}{4\tau_1} \\
&= \frac{2}{3} \frac{\left(1 + 1/\sqrt{\alpha}\right)^2}{\left(\sqrt{\alpha} + 2 + 2/\sqrt{\alpha}\right)} \frac{kT}{C_{SC}} \cdot \frac{g_{m(J)}}{g_{mSC}}
\end{aligned} \tag{17.21}$$

Memory switch noise power. From Figure 17.5, the noise transfer characteristic from v_{nSh} (hold switch g_{sh}) to the output of the $(n-1)$th stage is found to be

$$\frac{v_{on}(s)}{v_{nSh}(s)} = \frac{1+\tau_3 s}{\tau_1\tau_2 s^2 + \tau_1 s + 1} \tag{17.22}$$

By ignoring $\tau_3 (< \sqrt{\tau_1\tau_2})$ and using the equivalent bandwidth concept, the output noise power resulting from v_{nSh}, assuming critical damping, becomes

$$\begin{aligned}\bar{v}^2_{onSh} &= S_{nSh} \cdot \frac{1}{4\tau_1} \\ &= \frac{\left(\sqrt{\alpha} + 2 + 2/\sqrt{\alpha}\right)}{4\left(1 + 1/\sqrt{\alpha}\right)} \cdot \frac{kT}{C_{SC}}\end{aligned} \tag{17.23}$$

Input switch noise power. During the sampling phase of the nth stage, the noise transfer function from the sampling switch g_{ss} to the output v_{on} (ignoring the output impedance of the $(n-1)$th stage), is approximately given by

$$\frac{v_{on}(s)}{v_{nSs}(s)} \approx \frac{1}{((C_{SC} + C_g)/g_{ss})s + 1} \tag{17.24}$$

Using the equivalent noise bandwidth, the total noise power across the capacitors C_{SC} and C_g due to the switch is

$$\bar{v}^2_{nSs} = S_{nSs} \cdot \frac{g_{ss}}{4(C_{SC} + C_g)} = \frac{kT}{C_{SC} + C_g} \tag{17.25}$$

with a corresponding noise charge of $\bar{q}_{ns} = (C_{SC} + C_{SC}/\sqrt{\alpha})\bar{v}_{nSs}$.

On the next hold phase of the nth stage, all of this charge is transfered to the capacitor C_{SC} connected in its feedback position, and produces an output noise power of

$$\bar{v}^2_{onSs} = \frac{\bar{q}^2_{ns}}{C^2_{SC}} = \left(1 + \frac{1}{\sqrt{\alpha}}\right)\frac{kT}{C_{SC}} \tag{17.26}$$

Total noise power. Since all the noise sources in the model of Figure 17.5 are uncorrelated, the total noise power sampled by the nth stage is simply equal to the sum of all the individual noise powers. From equations (17.21), (17.23) and (17.26), this total noise power becomes,

$$\bar{v}_{on}^2 = \underbrace{\bar{v}_{onN}^2 + \bar{v}_{onJ}^2 + \bar{v}_{onSh}^2}_{\substack{\text{Direct noise from} \\ (n-1)\text{th stage}}} + \underbrace{\bar{v}_{onSs}^2}_{\substack{\text{Noise in} \\ n\text{th stage}}}$$

$$= (1 + k_s + k_h + k_j)\frac{2}{3}\frac{\left(1 + 1/\sqrt{\alpha}\right)^2 kT}{\left(\sqrt{\alpha} + 2 + 2/\sqrt{\alpha}\right) C_{SC}} \tag{17.27}$$

where

$$k_s = \frac{3}{2}\frac{\left(\sqrt{\alpha} + 2 + 2/\sqrt{\alpha}\right)}{\left(1 + 1/\sqrt{\alpha}\right)}$$

$$k_h = \frac{3}{8}\frac{\left(\sqrt{\alpha} + 2 + 2/\sqrt{\alpha}\right)^2}{\left(1 + 1/\sqrt{\alpha}\right)^3} \tag{17.28}$$

$$k_j = \frac{g_{mJ}}{g_{mSC}}$$

Signal-to-noise ratio. The SNR of a SC circuit may be defined as the ratio of the signal output power of a sinusoid with peak voltage $v_{o,peak}$ and the power of the total output noise voltage, v_{on}. So, from equation (17.27), SNR is given by

$$\text{SNR}_{SC} = \frac{v_{o,peak}^2}{2\bar{v}_{on}^2}$$

$$= \frac{v_{o,peak}^2}{(1 + k_s + k_h + k_j)(4/3)\left(\left(1 + 1/\sqrt{\alpha}\right)^2 kT\right) / \left(\left(\sqrt{\alpha} + 2 + 2/\sqrt{\alpha}\right) C_{SC}\right)}$$

$$= \frac{(V_{DD} - V_{gtSC} - V_{gtJSC})^2}{\left(1 + k_s + k_h + V_{gtSC}/V_{gtJSC}\right)\frac{16}{3}(kT/C_{SC}^T)} \tag{17.29}$$

where

$$C_{SC}^T = \frac{\left(\sqrt{\alpha} + 2 + 2/\sqrt{\alpha}\right)}{\left(1 + 1/\sqrt{\alpha}\right)^2} C_{SC} \tag{17.30}$$

and V_{gtJSC} is the gate–source overdrive voltage in the bias transistor PJ.

17.5.2. Switched-Currents Class A Noise

A model for a cascade of the class A SI memory cells in Figure 17.1(b) with associated noise sources is shown in Figure 17.6. The buffer amplifiers

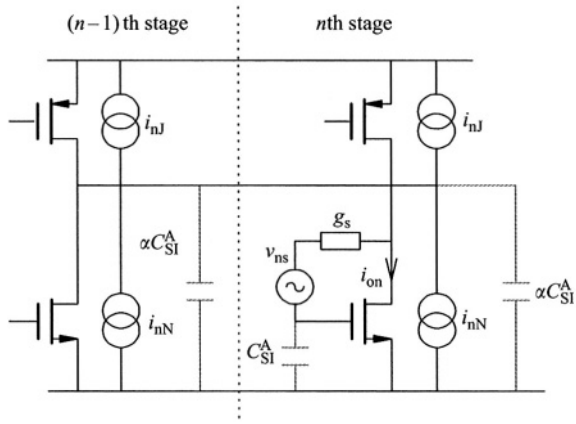


Figure 17.6. Small-signal model for noise calculation in class A SI memory cell.

in the $(n-1)$th and the nth stages each have noise current sources i_{nN} and i_{nJ} while the nth stage memory switch has a noise voltage v_{nS}. These noise sources contribute noise power to the nth stage memory current, i_{on}, and we proceed in much the same manner as before to find the output noise powers arising from each of the individual noise sources.

Saturated transistor noise power. From the model in Figure 17.6, it can be shown that the noise transfer characteristic from i_{nN} (or i_{nJ}), in either the $(n-1)$th or the nth stage, to the output i_{on} is

$$H(s) = \frac{i_{on}(s)}{i_{nN(J)}(s)} = \frac{1}{\tau_1\tau_2 s^2 + \tau_1 s + 1} \tag{17.31}$$

where τ_1 and τ_2 are defined in equation (17.10). By applying the equivalent noise bandwidth concept to equation (17.31), the output noise power resulting from i_{nN} (or i_{nJ}) is given by

$$\bar{i}^2_{onN(J)} = \frac{2}{3(1+2\alpha)} \frac{kT}{C_{SI}^A} \cdot g_{mSI}^A \cdot g_{m(J)} \tag{17.32}$$

Switch noise power. The noise transfer characteristic from v_{nS} to the output is found to be

$$\frac{i_{on}(s)}{v_{nS}(s)} = g_s \cdot \frac{\tau_3 s}{\tau_1\tau_2 s^2 + \tau_1 s + 1} \tag{17.33}$$

where τ_1, τ_2 are as defined in equation (17.10) and $\tau_3 = 2\alpha C_{SI}^A / g_s$. By applying the equivalent bandwidth to the transfer function in equation (17.33) the output

sampled noise power from v_{nS}, for critical damping, becomes

$$\begin{aligned}\bar{i}^2_{onS} &= S_{nS} \cdot g_s^2 \cdot BW_n \\ &= S_{nS} \cdot g_s^2 \cdot \frac{\tau_3^2}{4\tau_1^2\tau_2} \\ &= \frac{2\alpha}{(1+2\alpha)} \cdot \frac{kT}{C^A_{SI}} \cdot (g^A_{mSI})^2 \end{aligned} \tag{17.34}$$

Total output noise power. Using equations (17.32) and (17.34), the total output noise power becomes

$$\begin{aligned}\bar{i}^2_{on} &= \underbrace{\bar{i}^2_{onN} + \bar{i}^2_{onPJ}}_{\substack{\text{Direct noise from} \\ (n-1)\text{th stage}}} + \underbrace{\bar{i}^2_{onS} + \bar{i}^2_{onN} + \bar{i}^2_{onPJ}}_{\substack{\text{Noise in} \\ n\text{th stage}}} \\ &= (1 + k_s + k_j)\frac{4}{3}\frac{kT}{(1+2\alpha)C^A_{SI}} \cdot (g^A_{mSI})^2 \\ &= (1 + k_s + k_j)\frac{4}{3}\frac{kT}{C^T_{SI}} \cdot (g^A_{mSI})^2 \end{aligned} \tag{17.35}$$

where

$$\begin{aligned} k_s &= \frac{3\alpha}{2} \\ k_j &= \frac{g_{mJ}}{g^A_{mSI}} \\ C^T_{SI} &= (1+2\alpha)C^A_{SI} \end{aligned} \tag{17.36}$$

Signal-to-noise ratio. SNR in SI memory cells may be defined as the ratio between the power of a sinusoid with peak output current $i_{o,peak}$ and the power of the total output noise current i_{on}. Therefore, using equation (17.35), SNR in SI memory cells can be expressed as,

$$SNR_{SI} = \frac{i^2_{o,peak}}{2\bar{i}^2_{on}} = \frac{i^2_{o,peak}}{(1 + k_s + k_j)\frac{8}{3}(kT/C^T_{SI})(g^A_{mSI})^2} \tag{17.37}$$

By putting $i_{o,peak} = J^A$ (which is the limiting value to just avoid clipping of the memory current, that is, the modulation index $m_i = 1$), $g^A_{mSI} = 2J^A/V^A_{gtSI}$ and $g_{mJ} = 2J^A/V_{gtJ}$, we obtain

$$SNR^A_{SI} = \frac{(V^A_{gtSI})^2}{\left(1 + k_s + V^A_{gtSI}/V_{gtJ}\right)\frac{32}{3}\left(kT/C^T_{SI}\right)} \tag{17.38}$$

where V_{gtSI}^{A} and V_{gtJ} are the gate–source overdrive voltages of the memory transistor N and the current source PJ respectively. So, SNR_{SI}^{A} may be maximized by first putting V_{gtSI}^{A} to

$$V_{gtSI}^{A} = \frac{V_t}{\sqrt{2}} \tag{17.39}$$

which ensures that the memory transistor N of the $(n-1)$th stage remains in saturation at its maximum drain current, and then putting V_{gtJ} to

$$V_{gtJ} = V_{DD} - V_t - V_{gtSI}^{A}\sqrt{2} \tag{17.40}$$

to minimize the noise from the current source PJ, and finally substituting these values for V_{gtSI}^{A} and V_{gtJ} in equation (17.38).

17.5.3. Switched-Current Class AB Noise

Figure 17.7 shows the class AB SI memory cell model with associated noise sources for a cascade of memory cells from Figure 17.1(c).

Total output noise. The contribution of each individual noise source to the output is analyzed by following the same procedure as for the class A cell. In this way, it can be shown that the total output noise power in the class AB circuit is given by

$$\begin{aligned} \bar{i}_{on}^{2} &= (1+k_s)\frac{4}{3}\frac{kT}{(1+2\alpha)C_{SI}^{AB}} \cdot (g_{mSI}^{AB})^2 \\ &= (1+k_s)\frac{4}{3}\frac{kT}{C_{SI}^{T}} \cdot (g_{mSI}^{AB})^2 \end{aligned} \tag{17.41}$$

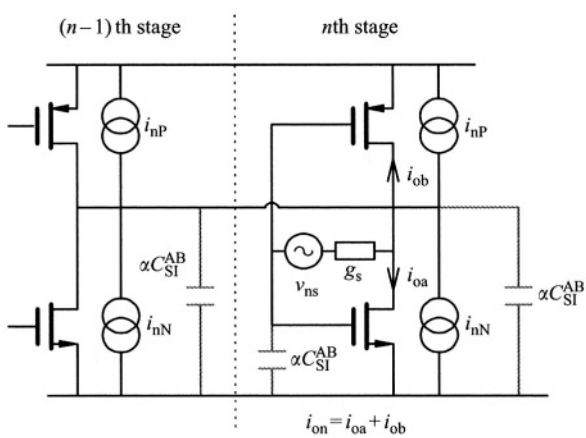


Figure 17.7. Small-signal model for noise calculation in class AB SI memory cell.

where $g_{mSI}^{AB} = g_{mN} + g_{mP}$ and $C_{SI}^{T} = (1 + 2\alpha)C_{SI}^{AB}$. Note that the term k_j is absent because both saturated transistors are acting as memories.

Signal-to-noise ratio. Using the same definition for SNR described in equation (17.37) and $i_{o,peak}$ is determined by the input current level just sufficient to cut-off either transistor N or P, and this corresponds to $2\beta(V_{gtSI}^{AB})^2$ or $4J^{AB}$. Setting $k_j = 0$ and substituting these expressions in equation (17.37) yields

$$SNR_{SI}^{AB} = \frac{(V_{gtSI}^{AB})^2}{(1 + k_s)\frac{8}{3}(kT/C_{SI}^{T})} \tag{17.42}$$

As in the class A cell, the gate–source overdrive V_{gt}^{AB} of the memory transistors N–P is limited by the circuit conditions on both the sampling and hold phases. On the sampling phase, both N and P are unconditionally saturated throughout the entire range of input currents. However, during the hold or output phase when the memory cell has to deliver the maximum current to the subsequent cell, it can be shown that the inequality

$$V_{gtSI}^{AB} = \frac{1}{2}(V_{DD} - 2V_t) \leq \frac{V_t}{2} \tag{17.43}$$

must hold in order to keep N and/or P saturated. Since SNR_{SI}^{AB} increases with V_{gtSI}^{AB}, the maximum V_{gtSI}^{AB} in the class AB cell is $V_t/2$ and this corresponds to the optimum supply voltage V_{DD} of

$$V_{DD,opt} = 3V_t \tag{17.44}$$

17.5.4. Comparison of Signal-to-Noise Ratios

Having derived the SNR equations, we are now able to study the SNR characteristics of all the memory cells in detail. In order to generalize the discussion, the equations for SNR_{SC}, SNR_{SI}^{A} and SNR_{SI}^{AB} should be normalized to the term kT/C^{T}, which yields,

$$\begin{aligned} SNR_{SC}^{norm} &= \frac{kT}{C_{SC}^{T}} \cdot SNR_{SC} \\ SNR_{SI}^{A,norm} &= \frac{kT}{C_{SI}^{T}} \cdot SNR_{SI}^{A} \\ SNR_{SI}^{AB,norm} &= \frac{kT}{C_{SI}^{T}} \cdot SNR_{SI}^{AB} \end{aligned} \tag{17.45}$$

Figure 17.8 shows plots of the normalized SNR vs V_{gt} characteristics, using SNR_{SC}^{norm} from equation (17.29), $SNR_{SI}^{A,norm}$ from equations (17.38)–(17.40)

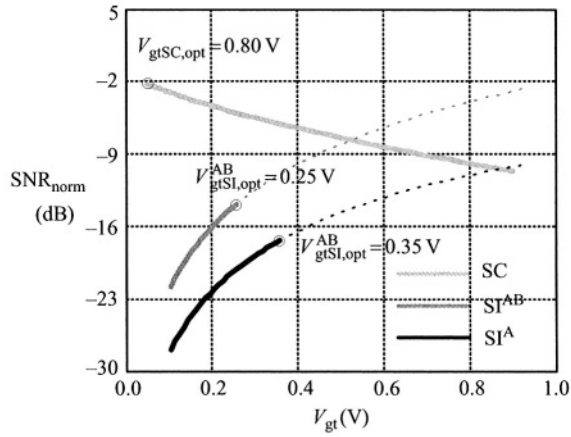


Figure 17.8. Typical SNR Characteristics in SC and SI memory cells ($V_{DD} = 3.3\,V$).

and $SNR_{SI}^{AB,norm}$ from equations (17.42)–(17.44), all in dB, for parameters typical of a 3.3V CMOS process ($V_{DD} = 3.3\,V, V_t = 0.5\,V$), and with $V_{gtSC} = V_{gtJSC}, \alpha = 1$ (or $C_d = C_g$). For the horizontal axis in the figure, V_{gt} represents V_{gtSC}, V_{gtSI}^{A} and V_{gtSI}^{AB}. Note that these plots are merely used to illustrate the individual SNR characteristic without implying total performance. The following conclusions can be made from the curves.

1 The SNR of the SC circuit (SNR_{SC}) is improved as the gate–source overdrive V_{gtSC} is reduced because this allows greater voltage swing in the circuit. The limit, which sets the maximum SNR, is determined by the need to maintain saturated operation of the amplifier transistors. There is a theoretical minimum value of V_{gtSC}, which is independent of processing, of about 80 mV [15] below which operation will enter the weak inversion or sub-threshold regions.

2 The SNR of the class A SI circuit (SNR_{SI}^{A}) increases with V_{gtSI}^{A} since the voltage available to represent the signal at the gate of the memory transistor N is increased. SNR_{SI}^{A} will keep increasing with V_{gtSI}^{A} until it reaches a maximum beyond which noise from the current source PJ starts to dominate (off-scale in Figure 17.8). However, the maximum V_{gtSI}^{A} and hence the peak SNR is determined by interstage coupling constraints at a value below that maximum, that is, at $V_{gtSI}^{A} \approx 0.35\,V$ for $V_t = 0.5\,V$.

3 The SNR of the class AB SI circuit (SNR_{SI}^{AB}) increases monotonically with V_{gtSI}^{AB} due to the increased voltage swing without reaching the maximum experienced by the class A circuit because there is no bias

transistor. Again, the limit is set by the interstage voltage constraint. For $V_t = 0.5\,\text{V}$, the optimum operating point for the class AB cell is at $V_{SI,opt}^{AB} = V_{gtSI,max}^{AB} = V_t/2 = 0.25\,\text{V}$ and the corresponding $V_{DD,opt}$ is $3V_t = 1.5\,\text{V}$.

Up to this point, the class A and class AB SI memory cells in Figure 17.1(a)–(c) have been analytically investigated, providing all the relations necessary to quantify the circuit performance in terms of SNR, F_c and P. The optimum operating conditions which give the peak SNR performance in each memory cell have also been discussed. Therefore, based on the derived relations, a comparative study among the SC, class A and class AB SI at their optimum operating points is now possible and this is the subject of Section 17.6.

17.6. Figure-of-Merit

For sampled analog systems, we have defined our FoM as,

$$\text{FoM} = F_c \frac{\text{SNR}}{P} \tag{17.46}$$

where F_c is the sampling frequency, SNR, the signal-to-noise ratio and P, the power dissipation. It enables the performances of the SC and SI memory cells to be easily compared. By applying the relations derived in the previous sections, the FoMs for the memory cells of Figure 17.1(a)–(c) at their optimum operating conditions are now given.

17.6.1. Switched-Capacitors

At the optimum operating point, the FoM in the SC circuit can be obtained by combining equations (17.7), (17.15) and (17.29), that is,

$$\text{FoM}_{SC} = \frac{1}{24\left(1 + 1/\sqrt{\alpha}\right)^2 \left(1 + k_s + k_h + V_{gtSC,opt}/V_{gtJSC}\right) kT} \times \frac{(V_{DD} - V_{gtSC,opt} - V_{gtJSC})^2}{V_{gtSC,opt} V_{DD}} \tag{17.47}$$

where k_s and k_h are defined in equation (17.28). From Figure 17.8, putting $V_{gtSC,opt} = V_{gtJSC} = 80\,\text{mV}$, equation (17.47) may be rewritten as

$$\text{FoM}_{SC} = \frac{1}{75\left(1 + 1/\sqrt{\alpha}\right)^2 (2 + k_s + k_h) kT} \cdot \frac{(6.25 V_{DD} - 1)^2}{V_{DD}} \tag{17.48}$$

17.6.2. Switched-Currents Class A

$\mathrm{FoM}_{\mathrm{SI}}^{\mathrm{A}}$ can thus be found by subsituting (17.13), (17.16) and (17.38) at $V_{\mathrm{gtSI}}^{\mathrm{A}} = V_{\mathrm{t}}/\sqrt{2}$ into the FoM definition, and this yields

$$\mathrm{FoM}_{\mathrm{SI}}^{\mathrm{A}} = \frac{1}{48\sqrt{2}\left(1 + k_{\mathrm{s}} + V_{\mathrm{t}}/\left(\sqrt{2}\,(V_{\mathrm{DD}} - 2V_{\mathrm{t}})\right)\right)kT} \cdot \frac{V_{\mathrm{t}}}{V_{\mathrm{DD}}} \tag{17.49}$$

where k_{s} is defined in (17.36). It can be shown that the above FoM equation exhibits a peak at an optimum supply voltage of,

$$V_{\mathrm{DD,opt}} = V_{\mathrm{t}}\left(2 + \frac{1.2}{\sqrt{(1 + k_s)}}\right) \tag{17.50}$$

At the optimum operating supply, $\mathrm{FoM}_{\mathrm{SI}}^{\mathrm{A}}$ is equal to

$$\mathrm{FoM}_{\mathrm{SI}}^{\mathrm{A}} = \frac{1}{48\left(1 + 1.7\sqrt{(1 + k_{\mathrm{s}})}\right)^2 kT} \tag{17.51}$$

Note from (17.51) that $\mathrm{FoM}_{\mathrm{SI}}^{\mathrm{A}}$ at the optimum V_{DD} is independent of the threshold voltage level.

17.6.3. Switched-Currents Class AB

For the class AB circuit, $\mathrm{FoM}_{\mathrm{SI}}^{\mathrm{AB}}$ can be expressed by using (17.14), (17.17) and (17.42), that is,

$$\mathrm{FoM}_{\mathrm{SI}}^{\mathrm{AB}} = \frac{V_{\mathrm{DD}} - 2V_{\mathrm{t}}}{18(1 + k_{\mathrm{s}})kT\,V_{\mathrm{DD}}}, \quad V_{\mathrm{DD}} \leq 3V_{\mathrm{t}} \tag{17.52}$$

At the optimum $V_{\mathrm{DD}} = 3V_{\mathrm{t}}$, (17.52) becomes

$$\mathrm{FoM}_{\mathrm{SI}}^{\mathrm{AB}} = \frac{1}{54(1 + k_{\mathrm{s}})kT} \tag{17.53}$$

17.7. Comparison of Figures-of-Merit

Perhaps the most interesting feature of the FoM equations of the last Section 17.8 is that they are all independent of the total load capacitance of the circuits. This means that we may use the load capacitance ($C_{\mathrm{SC}}^{\mathrm{T}}$, $C_{\mathrm{SI}}^{\mathrm{T}}$) as a parameter for trading-off between SNR, F_{c} and P within the FoM design space.

We now wish to make a numerical performance comparison of our three circuits using the FoMs described in equations (17.48)–(17.53). First, we calculate the FoMs vs V_{DD} for a 3.3 V CMOS process (a 1995 process) and this yields

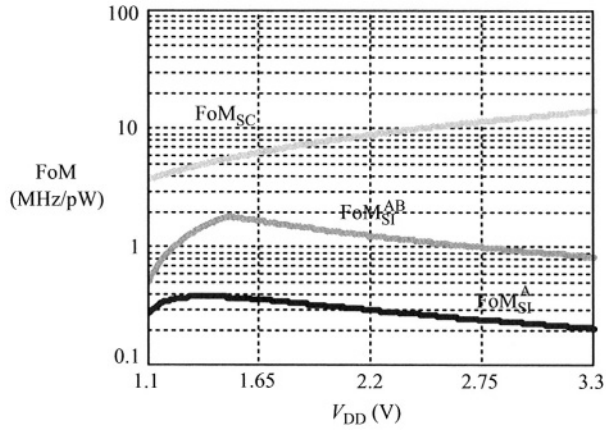


Figure 17.9. Figure-of-merits in SC and SI memory cells vs operating supply voltages in 0.35 μm CMOS technology with $V_t = 0.5$ V.

the plots in Figure 17.9. We see that when V_{DD} increases beyond about 1.5 V the performance of the SI circuits worsens while that of the SC circuit improves monotonically. At the full V_{DD} of 3.3 V the SC performance is about 30 times (14.8 dB) better than the class A SI and about six times (7.8 dB) better than the class AB SI, each at their optimum V_{DD}. This large performance difference at high supply voltage is mainly the result of the primitive SI cells' inabiltity to realize their SNR potential because their V_{gt} is restricted by interstage coupling constraints. SI cells employing techniques which generate a virtual earth at their inputs (e.g. S^3I [16] or zero-voltage switching [10]) alleviate this problem and the performance difference with SC will be less marked in practice.

Next, we calculate how the performances compare with CMOS processes that can be expected in the future. CMOS technology generations between 1991 and 2011 are summarized in Table 17.1. This is based on the 1999 Semiconductor Industries Association (SIA) roadmap and expected trends in threshold voltage [17]. For each generation, it is possible to calculate the optimum V_{DD} for each of our circuits and this is shown in Figure 17.10. Next, we compute the performances at these optimum V_{DD}s and the corresponding V_t for each technology generation and this is plotted in Figure 17.11. We now see a very different picture. We see the performance of SC falling with future CMOS generations while that of SI is almost unaffected. The performance of SC is given for V_{gtSC} at its optimum value of 0.08 V and at a more practical value of 0.16V and we see that the performance is very sensitive to this choice.

This performance behavior can be explained intuitively with the help of the approximate comparison given in Table 17.2. We consider the CMOS process

Table 17.1. Forecast of CMOS technology generations.

Year	*Technology* (μm)	*Process supply voltage (V)*	*Threshold voltage (V)*
1991	0.80	5.0	0.80
1993	0.50	3.3	0.60
1995	0.35	3.3	0.50
1997	0.25	2.5	0.45
1999	0.18	1.8	0.35
2002	0.13	1.5	0.30
2005	0.10	1.2	0.25
2008	0.07	0.9	0.25
2011	0.05	0.6	0.20

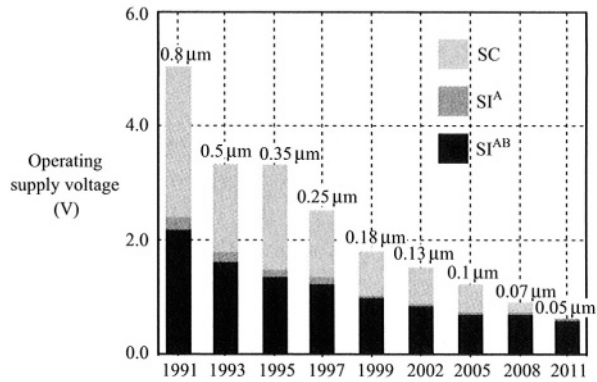


Figure 17.10. Operating supply voltage levels for SC and SI memory cells at their optimum conditions.

V_{DD} falling from 5 to 0.6V (K falling from say unity to 0.12) with constant supply current and total capacitance, C^T. For SC, the gate overdrive V_{gt} stays constant at its minimum value and so the transconductance, g_m also stays constant. The signal power falls by K^2 because the signal voltage falls by K but the noise power stays constant because g_m stays constant. The SNR falls by K^2 and the power consumption by K. The clock frequency stays constant because both g_m and C^T remain constant. Consequently, the figure-of-merit falls by K.

For SI, if we assume simplistically that the threshold voltage falls linearly with the process supply voltage (reasonable until V_{DD} reaches 0.9 V in 2008) the gate overdrive, V_{gt}, falls by K to ensure saturated operation and so the transconductance, g_m, increases by $1/K$. The signal power remains constant

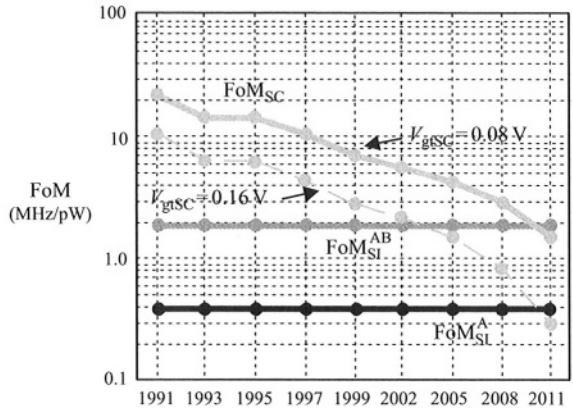


Figure 17.11. Figure-of-merits in SC and SI memory cells at different CMOS technology generations in Table 1.

Table 17.2. Approximate performance scaling with process supply voltage, V_{DD}.

Performance	*SC*	*SI*
Supply voltage, V_{DD}	K	K
Supply current, I_{DD}	1	1
Total capacitance, C^T	1	1
Gate overdrive, V_{gt}	1	K
Transconductance, g_m	1	$1/K$
Signal power	K^2	1
Noise power	1	$1/K^2$
Signal-to-noise ratio, SNR	K^2	K^2
Power consumption, P	K	K
Clock frequency, F_c	1	$1/K$
FoM, SNR $\cdot$ F_c/P	K	1

because the supply current remains constant but the noise power increases by $1/K^2$ because the increase in g_m increases both the noise power spectral density and the noise bandwidth by $1/K$. The SNR falls by K^2 and the power consumption falls by K. The clock frequency increases by $1/K$ because g_m increases by $1/K$ and C^T remain constant. Consequently, the FoM stays constant.

Clearly, the SNR and power consumption fall by K^2 and K, respectively for both SC and SI. However, while the clock frequency remains constant for SC it increases by $1/K$ for SI. Of course, this gain of clock frequency can be traded for SNR or power consumption if desired but in any case the FoM is unaffected. The performance superiority enjoyed by SC at higher supply voltage is steadily

eroded and during the next decade class AB SI performance can be expected to match and then surpass that of SC.

17.8. Conclusions

The performances of SC and SI have been compared. Using a set of primitive track-and-hold cells, each with the same complementary pair voltage amplifier, various performance vectors were analyzed. This analysis assumed square-law MOS behavior and was developed in the context of a pipeline analog-to-digital converter. Absolute maximum signals, with no engineering safety margins, was assumed throughout and each cell was optimized to its own best advantage. The performance vectors, SNR, F_c and P, were found and subsequently combined into a single FoM to express overall performance.

Using forecast process data for CMOS generations through the period 1991–2011, the FoMs of the SC and SI primitive cells were evaluated. It was found that at the start of this period (1991), SC performed about ten times (10 dB) better than class AB SI and about 50 times better (17 dB) than class A SI. However, as processing heads towards lower power supply voltage the performance of SC falls steadily while that of SI remains almost constant. During the course of the next decade, class AB SI can be expected to match and eventually pass that of SC.

Ultimately, it will be high performance versions of these primitive cells, designed with properly engineered trade-offs and safety margins, that will be compared. These may suffer extra problems (e.g. SC may suffer slew limited settling) not encountered in our primitive cells and this will color our comparison of primitive cells. Nevertheless, the result is a strong one and indicates several things. It goes some way to explaining why SI has been outperformed in older, higher voltage CMOS processes. It also indicates that SI may have been ahead of its time and in due course should offer both cost and performance advantages.

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Chapter 18

DESIGN OF INTEGRATED LC VCOs

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18.1. Introduction

Wireless transceiver designers have enjoyed an explosive development of the field over the last decade, spurred by the rapidly growing portable equipment market. The recent quest for a *system-on-a-chip* is a response to the demand for lower cost and continued market growth. However, several essential building blocks of wireless transceivers stand in the way of achieving high-level integration as they limit the system performance when integrated. Integrated LC voltage-controlled oscillators (VCOs) are one of the most challenging obstacles.

Due to exponentially increasing demand for the bandwidth, specifications imposed on the spectral purity of local oscillators are very stringent. However, the lossy on-chip spiral inductors are impediments to satisfying such constrictive specifications. Moreover, design of integrated LC VCOs requires simultaneous optimization of multiple variables, many of which are introduced by the on-chip spiral inductors. For these reasons, despite the endeavors to improve the phase noise performance of integrated LC VCOs of recent years [1–23], transceiver designers still have difficulties in optimizing the circuits and have to resort to an *ad hoc* fashion of circuit design in many cases.

Computer-aided optimization methods which have recently emerged [24,25] help to find the optimum design for certain LC oscillator topologies efficiently. In spite of their efficiency, however, they provide limited physical insight into choosing the optimum design, as they rely totally on the computer to perform the optimization. Therefore, even in the presence of such CAD tools, firm understanding of the underlying trade-offs among the parameters in the circuit design is essential to enhance circuit innovations and increase design productivity. This is especially important when the number of design parameters is large, as any optimization tool *unjustifiably* exploits the limitations of the models used.

To address this issue, the authors have recently developed a graphical optimization methodology utilizing *graphical nonlinear programming* (GNP) in design of integrated LC VCOs [26]. Graphical visualization of the design constraints provides essential intuitions in finding the optimum design for a group

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of strongly coupled design variables. It allows simultaneous optimization of multiple variables to minimize phase noise subject to certain design constraints. Especially, a method of selecting on-chip spiral inductors is devised in the course of the oscillator optimization.

This chapter is a review of the work using GNP in design of integrated LC VCOs and is organized in the following manner. Section 18.2 illustrates the methods of GNP with an example. In Section 18.3, a specific oscillator topology is chosen as a design example, design constraints are imposed on the oscillator and the expressions describing phase noise of the oscillator are provided. Section 18.4 explains the details of our design and optimization process using GNP. Section 18.5 further discusses the main result of integrated LC VCO optimization from fundamental physical points of view. Elaborate simulation results of the optimized VCO are presented in Section 18.6 with accurate prediction of phase noise. Section 18.7 presents the experimental results and compares the performance of our VCO to that of other reported LC oscillators to prove the adequacy of our design methodology.

18.2. Graphical Nonlinear Programming

In this chapter, we will use a generalization of the well-known *Linear programming* (LP) [27] to optimize a nonlinear objective function subject to multiple nonlinear constraints by graphically visualizing the objective function and constraints. We will refer to this generalized approach as GNP. In this section, the method of GNP is illustrated through an example containing both linear and nonlinear constraints:

Use GNP to minimize an objective function $g(x, y) = \frac{1}{4}x^2 + y$ *subject to*

$$y \geq x - 1 \tag{18.1}$$

$$y \leq -x + 1 \tag{18.2}$$

$$y \leq -x^2 + 1 \tag{18.3}$$

The constraints given in (18.2) are visualized as the shaded area in the *xy*-plane of Figure 18.1. The objective function can be visualized using curves described by $g(x, y) = k$ for different values of k. The minimum of $g(x, y)$ can be found by changing the parameter k in $g(x, y) = k$ and moving the corresponding curve in the *xy*-plane, while maintaining a part of it in the shaded area. The objective function $g(x, y)$ reaches its minimum when $k = -2$ and the curve $g(x, y) = k$ touches point A as shown in Figure 18.1.

In the case of multi-variable optimization, this method can still be used by partitioning the optimization space into multiple 2D subspaces and applying the same method locally. However, unless the problem structure is exploited, this approach becomes formidable with many variables. Phase noise optimization

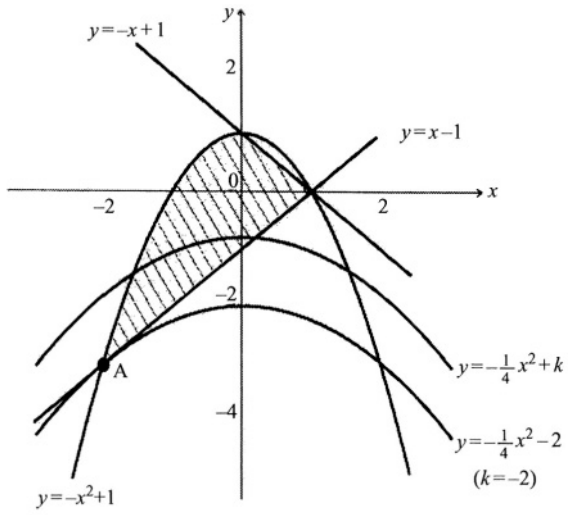


Figure 18.1. Example of GNP with 2 variables.

is an example of such simplification using the structure of the problem, as shown in detail in Section 18.4.

18.3. LC VCO Design Constraints and an Objective Function

The commonly used cross-coupled LC oscillator of Figure 18.2 is selected as a design example through which we demonstrate our optimization process. The oscillator fully exploits the merits of differential operation, reducing undesirable common-mode effects such as extrinsic substrate and supply noise amplification and up-conversion. The oscillation amplitude of this structure is approximately a factor of two larger than that of the NMOS-only structure owing to the PMOS pair, which results in a better phase noise performance for a given tail current [28–30]. The oscillator incorporates the rise and fall time symmetry to further reduce the $1/f$ noise up-conversion [28].

There are 12 independent design variables associated with this specific oscillator topology: transistor dimensions (W_n, W_p, L_n, and L_p), geometric parameters of on-chip spiral inductors (metal width *b,* metal spacing *s,* number of turns *n,* and lateral dimension *d*), maximum and minimum value of the varactors ($C_{v,max}$ and $C_{v,min}$), load capacitance (C_{load}) and tail bias current in the oscillator core (I).

The equivalent small-signal model of the oscillator is shown in Figure 18.3 where the broken line in the middle represents the common mode. The

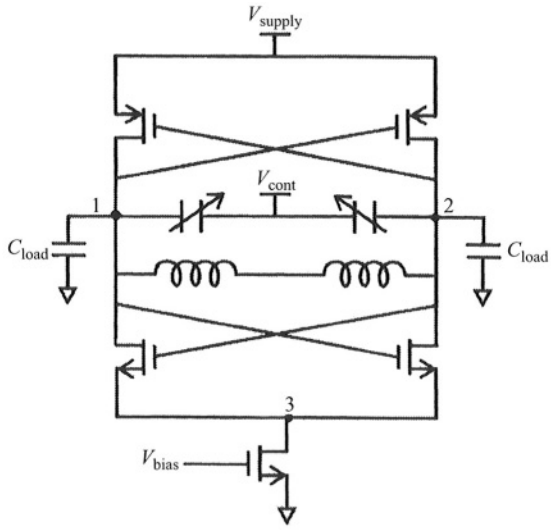


Figure 18.2. LC VCO schematic.

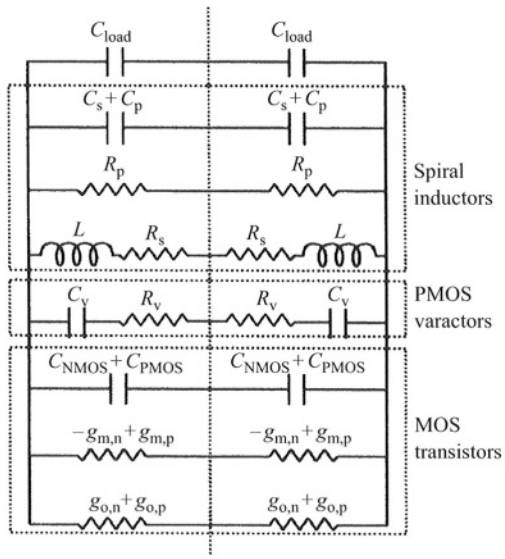


Figure 18.3. Oscillator tank model.

symmetric spiral inductor model of Figure 18.4 [31] with identical RC loading on both terminals is used as a part of the tank model. Varactors are made out of the gate channel capacitor of standard PMOS transistors in inversion mode. They are modeled with a capacitor C_v in series with a resistor R_v as in

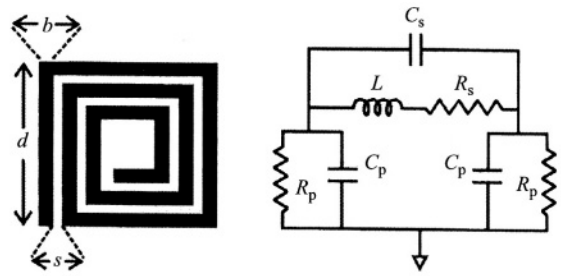


Figure 18.4. Symmetric spiral inductor model.

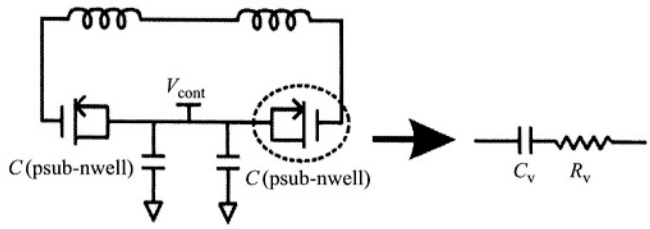


Figure 18.5. LC tank and MOSCAP varactor.

Figure 18.5, which is used as a part of the tank model. In Figure 18.3, g_m and g_o represent transconductance and output conductance of transistors, respectively, and C_{NMOS} and C_{PMOS} are total parasitic capacitance of NMOS and PMOS transistors, respectively.[1] All the electrical parameters in the equivalent model can be expressed in terms of design variables, by utilizing existing formulae for transistor parameters [32] and on-chip resonator parameters [24,25].

The frequently appearing parameters in our optimization process are the tank load conductance, g_{tank}, tank negative conductance $-g_{active}$, tank inductance, L_{tank}, and tank capacitance, C_{tank}, which are given by

$$2g_{tank} = g_{o,n} + g_{o,p} + g_v + g_L \tag{18.4}$$

$$2g_{active} = g_{m,n} + g_{m,p} \tag{18.5}$$

$$L_{tank} = 2L \tag{18.6}$$

$$2C_{tank} = C_{NMOS} + C_{PMOS} + C_s + C_p + C_v + C_{load} \tag{18.7}$$

respectively, where g_L and g_v are the effective parallel conductance of the inductors and varactors, respectively.[2] Note that g_{tank} and C_{tank} assume

---

1 $C_{NMOS} = C_{gs,n} + C_{db,n} + 4C_{gd,n}$ and $C_{PMOS} = C_{gs,p} + C_{db,p} + 4C_{gd,p}$.

2 $g_L = 1/R_p + R_s/(L\omega)^2$ and $g_v = C_v\omega/Q_v$.

certain range of values as the varactor capacitance varies. Their maximum and minimum values will be denoted by subscripts "max" and "min".

18.3.1. Design Constraints

Design constraints are imposed on the bias current, voltage swing, tuning range, start-up condition, and lateral dimension of spiral inductors: First, the bias current is required to be less than maximum allowed current $I_{\max}$, that is,

$$I \leq I_{\max} \tag{18.8}$$

Second, the voltage swing is required to be larger than a certain value $V_{\mathrm{sw,min}}$ to reduce phase noise and guarantee the driving capability of the oscillator, that is,

$$V_{\mathrm{sw}} = \frac{I}{g_{\mathrm{tank,max}}} \geq V_{\mathrm{sw,min}} \tag{18.9}$$

where $g_{\mathrm{tank,max}}$ imposes the worst-case constraint. Third, the tuning range in excess of $x\%$ with a given center frequency ω is expressed as

$$L_{\mathrm{tank}} C_{\mathrm{tank,min}} \leq \omega_{\max}^{-2} \tag{18.10}$$

$$L_{\mathrm{tank}} C_{\mathrm{tank,max}} \geq \omega_{\min}^{-2} \tag{18.11}$$

where $(\omega_{\max} - \omega_{\min})/\omega = x/100$ and $(\omega_{\max} + \omega_{\min})/2 = \omega$. Fourth, the start-up condition with a small-signal loop gain of at least $\alpha_{\min}$ is given by

$$g_{\mathrm{active}} \geq \alpha_{\min} g_{\mathrm{tank,max}} \tag{18.12}$$

where the worst-case condition is imposed by $g_{\mathrm{tank,max}}$. Finally, we specify a maximum lateral dimension for the spiral inductor as $d_{\max}$, that is,

$$d \leq d_{\max} \tag{18.13}$$

in order to limit the die area.

18.3.2. Phase Noise as an Objective Function

Our design goal is to minimize phase noise subject to constraints given in (18.8)–(18.13). This task requires an explicit expression for the phase noise in terms of design variables. In the $1/f^2$ region, the phase noise is given by [28]:

$$\mathcal{L}\{f_{\mathrm{off}}\} = \frac{1}{8\pi^2 f_{\mathrm{off}}^2} \cdot \frac{1}{q_{\max}^2} \cdot \sum_n \left(\frac{\bar{i}_n^2}{\Delta f} \cdot \Gamma_{\mathrm{rms},n}^2 \right) \tag{18.14}$$

where f_{off} is the offset frequency from the carrier and $q_{\max} = C_{\mathrm{tank}} V_{\mathrm{sw}}$ is the total charge swing of the tank. The $\bar{i}_n^2/\Delta f$ terms in the sum represents drain

current noise, gate noise, inductor noise and varactor noise. Each $\Gamma_{\mathrm{rms},n}$ is the *rms* average of the *impulse sensitivity function* (ISF) [28] for each noise source and is $1/\sqrt{2}$ for an ideal sinusoidal waveform. It can be evaluated more accurately from simulations as shown in Section 18.6. The equivalent differential noise power spectral density due to the drain current noise, gate noise, inductor noise and varactor noise is given by [13,33,34]

$$\frac{\bar{i}^2_{\mathrm{M,d}}}{\Delta f} = 2kT\gamma(g_{\mathrm{d0,n}} + g_{\mathrm{d0,p}}) \tag{18.15}$$

$$\frac{\bar{i}^2_{\mathrm{M,g}}}{\Delta f} = \frac{2kT\delta\omega^2}{5}\left(\frac{C^2_{\mathrm{gs,n}}}{g_{\mathrm{d0,n}}} + \frac{C^2_{\mathrm{gs,p}}}{g_{\mathrm{d0,p}}}\right) \tag{18.16}$$

$$\frac{\bar{i}^2_{\mathrm{ind}}}{\Delta f} = 2kTg_{\mathrm{L}} \tag{18.17}$$

$$\frac{\bar{i}^2_{\mathrm{var}}}{\Delta f} = 2kTg_{\mathrm{v,max}} \tag{18.18}$$

respectively. $\gamma \approx 2/3$ and $\gamma \approx 2.5$ for long and short channel transistors, respectively and $\delta \approx 2\gamma$ [33,34]. g_{d0} is the channel conductance at zero V_{DS} and it is equal to g_{m} for long channel transistors while it is given by $2I_{\mathrm{drain}}/(L_{\mathrm{channel}}E_{\mathrm{sat}})$[3] and assumes a different value from g_{m} for short channel transistors [35]. Note that $g_{\mathrm{v,max}}$ is used to express the worst-case noise in (18.18).

18.3.3. Phase Noise Approximation

While (18.12) should be used when an accurate phase noise calculation is required, an approximate, yet insightful expression for phase noise can be obtained by taking only the dominant drain current noise into account. Using (18.12) and (18.15) while replacing ω and q_{max} with $2\pi f$ and $V_{\mathrm{sw}}/(L_{\mathrm{tank}}\omega^2)$, respectively, we obtain the following phase noise expression

$$\mathcal{L}\{f_{\mathrm{off}}\} \approx 16\pi^2 kT\gamma \cdot \left[\frac{1}{(L_{\mathrm{channel}}E_{\mathrm{sat}})_{\mathrm{p}}} + \frac{1}{(L_{\mathrm{channel}}E_{\mathrm{sat}})_{\mathrm{n}}}\right] \times \frac{f^4}{f^2_{\mathrm{off}}} \cdot \frac{L^2 I}{V^2_{\mathrm{sw}}} \tag{18.19}$$

Note that g_{d0} was replaced with $2I_{\mathrm{drain}}/(L_{\mathrm{channel}}E_{\mathrm{sat}})$ for short channel transistors and Γ^2_{rms} was approximated with $1/2$ for a pure sinusoidal wave.

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[3] E_{sat} is the electric field at which the carrier velocity reaches half its saturation velocity.

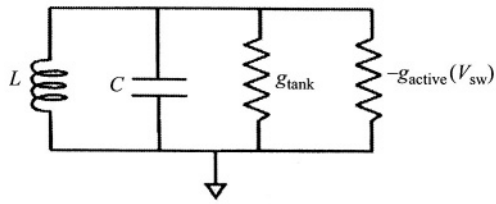


Figure 18.6. A simple oscillator model.

The dominance of drain-current noise is an inherent feature of any properly designed CMOS LC oscillator. An LC oscillator in the steady state can be modeled as a parallel LC tank as shown in Figure 18.6, where g_{tank} represents the tank load conductance including output conductance of active circuits and $-g_{active}(V_{sw})$ is the amplitude-dependent, effective negative conductance of active circuits.[4] The current noise density due to the inductor and varactor is less than $4kTg_{tank}$, that is,

$$\frac{\overline{i}^2_{tank}}{\Delta f} < 4kTg_{tank} \tag{18.20}$$

where the inequality stands since g_{tank} consists of not only noise-contributing inductor and varactor conductance but also zero-noise small-signal output conductance of transistors. The drain current noise of transistors, which is normally much larger than the transistor gate noise, is bounded by

$$\frac{\overline{i}^2_{drain}}{\Delta f} \geq 4kT\gamma g_{active} \tag{18.21}$$

where $\gamma \approx 2/3$ and $\gamma \approx 2.5$ for long and short channel transistors, respectively. The equality in (18.21) holds good only for long channel transistors for which $g_m = g_{d0}$. For short channel transistors, the ratio of g_m to g_{d0} is less than 1 by definition of the short channel regime, that is,

$$\frac{g_m}{g_{d0}} = \frac{L_{channel}E_{sat}}{2(V_{GS} - V_{TH})} < 1 \tag{18.22}$$

which explains the inequality of (18.21). Now the ratio of the total tank noise density to the total drain noise density can be bounded using (18.20) and (18.21), that is,

$$\frac{\overline{i}^2_{tank}/\Delta f}{\overline{i}^2_{drain}/\Delta f} < \frac{4kTg_{tank}}{4kT\gamma g_{active}} \leq \frac{1}{\gamma\alpha_{min}} \tag{18.23}$$

---

[4] Note that for the specific topology of Figure 18.2, g_{tank} and g_{active} are given by (18.4) and (18.5).

where the last inequality originates from the start-up condition $g_{\text{active}} \geq \alpha_{\min} g_{\text{tank}}$, which is a necessary condition for any oscillator to work. Equation (18.23) predicts that with $\alpha_{\min} = 3$, the drain current noise contributes more than 66% and 88% of the circuit noise for long and short channel transistors, respectively. This theoretical prediction on the dominance of the drain current noise well agrees with the simulation results shown later.

While the voltage swing of LC oscillators increases with an increasing bias current near up to supply voltage (*current-limited regime*), above this point, the voltage swing is saturated about at the supply voltage with further increase of the bias current (*voltage-limited regime*) [28]. Noting that $V_{\text{sw}} = I g_{\text{tank}}^{-1}$ in the current-limited regime and $V_{\text{sw}} = V_{\text{supply}}$ in the voltage-limited regime, (18.17) can be rewritten in the following form

$$\mathcal{L}\{f_{\text{off}}\} \approx \begin{cases} \eta L^2 g_{\text{tank}}^2 / I & \text{current-limited} \\ \eta L^2 I / V_{\text{supply}}^2 & \text{voltage-limited} \end{cases} \tag{18.24}$$

where $\eta \equiv (16\pi^2 kT\gamma)((L_{\text{channel}} E_{\text{sat}})_{\text{p}}^{-1} + (L_{\text{channel}} E_{\text{sat}})_{\text{n}}^{-1}) \cdot f^4 / f_{\text{off}}^2$. The phase noise expressions are for the simplified case in which cyclostationary noise effects are ignored. A more rigorous treatment taking the cyclostationary noise into account [28] shows that phase noise reaches a plateau with the further increase of current in the voltage-limited regime. Reflecting this notion, the phase noise approximation (18.22) can be reshaped into

$$\mathcal{L}\{f_{\text{off}}\} \approx \begin{cases} \eta L^2 g_{\text{tank}}^2 / I & I \leq I_{\text{edge}} \\ \eta L^2 I_{\text{edge}} / V_{\text{supply}}^2 & I \geq I_{\text{edge}} \end{cases} \tag{18.25}$$

where I_{edge} represents the bias current for which oscillation occurs at the edge of the voltage-limited regime. The phase noise approximation of (18.23) serves a crucial role in our optimization process in the next section.

18.3.4. Independent Design Variables

Appropriate design considerations can reduce the number of design variables from the 12 initial design variables mentioned earlier. First, in the cross-coupled MOS transistors, both channel-length L_{n} and L_{p} are set to the minimum allowed in the process technology to reduce parasitic capacitances and achieve the highest transconductance. Also, a symmetric active circuit with $g_{\text{m,n}} = g_{\text{m,p}}$ is used to improve the $1/f^3$ corner of phase noise [28], which establishes a relation between W_{p} and W_{n}. Therefore, MOS transistors introduce only one independent design variable, W_{n}, which will be shown as w from now on. Second, in the spiral inductors, the constraint imposed on the lateral dimensions in (18.13) is always tight since a larger d results in a smaller series resistance

and therefore d should be set to $d_{\max}$.[5] Thus, we have three independent design variables for spiral inductors, that is, b, s and n. Third, MOSCAP varactors introduce only one design variable $C_{v,\max}$ since in a typical varactor, the ratio $C_{v,\max}/C_{v,\min}$ remains constant as it is primarily determined by underlying physics of the capacitor for a scalable layout. $C_{v,\max}$ will be denoted as c from this point on. Fourth, the size of the output driver transistors can be pre-selected so that they can drive a $50\,\Omega$ load at 0 dBm with the minimum voltage swing $V_{sw,\min}$. This results in an output differential pair with a specific ratio of W/L and thus a specific value for C_{load}, excluding it from the set of design variables. Finally, the tail bias current I adds an additional design variable and it will be denoted as i from this point on.

Summarizing, we have six independent design variables to optimize: w from MOS transistors, c from MOSCAP varactors, b, s and n from spiral inductors, and i from the bias current. The design constraints (18.8) to (18.13) and phase noise in (18.12) are then expressed in terms of the six design variables, w, c, i, b, s and n.

18.4. LC VCO Optimization via GNP

We will demonstrate the details of our optimization process via GNP to design integrated LC VCOs in this section. In order to exploit methods of GNP, phase noise and design constraints need to be visualized in the 6D optimization space, which is practically impossible. Fortunately, the problem structure is such that we can select the 2D cw-plane as our optimization space by parametrizing the design variables from inductors, that is, b, s, n, and the bias current i for our optimization purpose.

This section is organized in the following order. In Subsection 18.4.1, specific numerical design constraints in accordance with Subsection 18.3.1 are imposed to provide a design example. In Subsection 18.4.2, we select a specific inductor to fix b, s and n and perform GNP to minimize phase noise in the cw-plane for various bias current i. Subsection 18.4.3 investigates how the design constraints change in the cw-plane for different inductors with *a fixed inductance value and different losses,* leading to a method of minimizing phase noise for *a fixed inductance.* Subsection 18.4.4 utilizes the phase noise approximation (18.23) to devise a method to find the optimum inductance value in the most general case. Combination of the two methods from Subsections 18.4.3 and 18.4.4 leads to an insightful general optimization process for integrated LC VCO design, which is summarized in Subsection 18.4.5. Subsection 18.4.6 discusses final fine-tuning of the design to account for the non-idealities of the actual design.

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[5] This assumption can be violated for very large spiral inductors.

Before embarking on the VCO optimization using GNP, words of caution are necessary. In our optimization process, the ISF are simply replaced with $1/\sqrt{2}$ and cyclostationary effects are neglected as was seen in the previous section. Thus, the optimization process should be understood to lead to a *near-optimum* design, after which a careful simulation should be performed to fine-tune the design to accurately evaluate the ISF and cyclostationarity.

18.4.1. Example of Design Constraints

We now impose specific design constraints on the bias current, voltage swing, tuning range, start-up condition and lateral dimension of spiral inductors in accordance with Subsection 18.3.1 to demonstrate a typical design problem. In this particular example, the oscillator is designed to draw a maximum of 4mA of current from a 2.5 V supply, that is, $I_{\max} = 4\,\mathrm{mA}$ in (18.8) and $V_{\mathrm{supply}} = 2.5\,\mathrm{V}$. We specify a minimum voltage swing of 2 V, that is, $V_{\mathrm{sw,min}} = 2\,\mathrm{V}$ in (18.9). A tuning range in excess of 15% with a center frequency of 2.4 GHz is specified and therefore, $f_{\max} = 2.58\,\mathrm{GHz}$ in (18.10) and $f_{\min} = 2.22\,\mathrm{GHz}$ in (18.11). We impose a rather conservative start-up condition with a small-signal loop gain of at least three, and hence $\alpha_{\min} = 3$ in (18.12). Finally, we specify a maximum lateral dimension of spiral inductors as $200\,\mu\mathrm{m}$ and therefore, $d_{\max} = 200\,\mu\mathrm{m}$ in (18.13).

18.4.2. GNP with a Fixed Inductor

In this subsection, the 6D optimization space is reduced to 2D cw-plane with a fixed inductor while bias current, i, becomes a parameter. In the particular example of the 2.4 GHz oscillator, this is a 2.7 nH inductor with a quality factor, Q, of 8.9. GNP is performed with this specific inductor in the cw-plane to demonstrate how to obtain the minimum phase noise for a given inductor.

The design constraints given by (18.9)–(18.12) are visualized in Figures 18.7 and 18.8 in the cw-plane for the bias current of 4 mA and 5 mA, respectively, where w is in $\mu\mathrm{m}$ and c is in pF.[6] The voltage swing line is obtained from (18.9). The voltage swing is larger than $V_{\mathrm{sw,min}} = 2\,\mathrm{V}$ below the voltage swing line. The broken lines with one dash and three consecutive dots in the figures represent the *regime-divider line* (supply-voltage (2.5 V) swing line), below which the oscillation occurs in the voltage-limited regime with the saturated voltage swing of 2.5 V. The regime-divider line is obtained from the following

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[6] Even though the maximum allowed current is 4 mA from the given design constraints, we investigate the case of I = 5 mA just to observe how the design constraints vary depending upon the current.

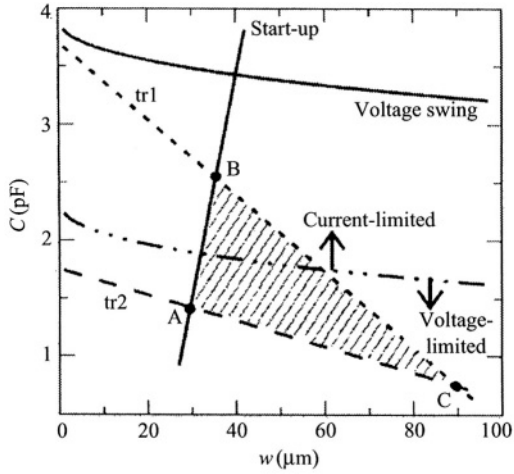


Figure 18.7. Design constraints with $I = 4\,\text{mA}$.

equation

$$\frac{I}{g_{\text{tank,max}}} = 2.5\,\text{V} \tag{18.26}$$

The trl and tr2 lines are obtained from (18.10) and (18.11), respectively. A tuning range of at least 15% with a center frequency of 2.4 GHz is achieved if a design point lies below the trl line and above the tr2 line. The start-up line is obtained from (18.12). On the right-hand side of the start-up line, the small-signal loop gain is over $\alpha_{\text{min}} = 3$ to guarantee start-up. The shaded regions in the figures satisfy all the constraints in (18.9) to (18.12) and therefore represent sets of feasible design points.

The tuning range constraints remain the same irrespective of the bias current. Also, the start-up constraint is almost independent of the bias current as the transconductance of short channel transistors shows little dependence on the bias current. On the other hand, the voltage swing constraint shows high sensitivity to the bias current. As the bias current decreases, the voltage swing line translates downward quickly and shaded areas will disappear.

Methods of GNP are applied to minimize phase noise with the given constraints. In order to seek the minimum phase noise, the *equi-phase-noise contour* represented by $\mathcal{L}\{f_{\text{off}}\}(c, w; i) = k$ is moved in the cw-plane by changing the parameter k while maintaining a part of the contour in the plausible design area, where $\mathcal{L}\{f_{\text{off}}\}(c, w; i)$ is given by (18.12).[7] For example, for

[7] Equation (18.12) is used to draw equi-phase-noise contours in the cw-plane and find minimum phase noise through GNP. However, phase noise approximations (18.23) will be

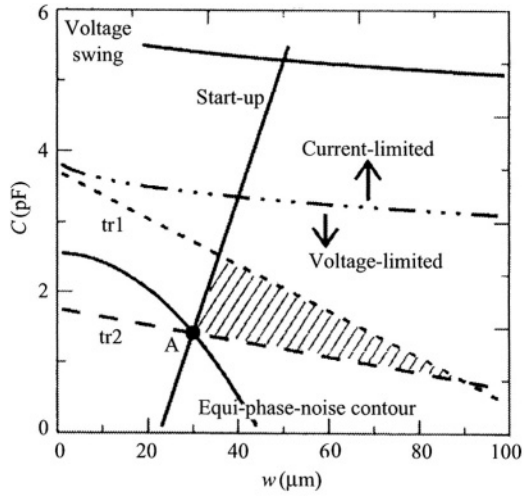


Figure 18.8. Design constraints with $I = 5$ mA.

$I = 5$ mA, the minimum phase noise is obtained at point A where the equi-phase-noise contour with the smallest phase noise value touches the region of feasibility as in Figure 18.8. At the optimum design point A, the minimum phase noise at 600kHz offset from a 2.4 GHz carrier is –118 dBc/Hz, and point A lies in the voltage-limited regime. For $I = 4$ mA, the same method of GNP shows that the minimum phase noise at 600kHz offset from a 2.4 GHz carrier is –119 dBc/Hz at point A still in the voltage-limited regime as seen in Figure 18.7.

The example above shows that in the voltage-limited regime, increase of the bias current results in increase of phase noise. This result is based upon the phase noise formula which does not take the time-varying cyclostationary noise into account. As stated earlier, a rigorous treatment [28] considering the cyclostationary effects shows that phase noise reaches a plateau with the further increase of the bias current in the voltage-limited regime, which is well reflected in (18.23). A valuable observation here is that *the lowest phase noise with the highest power efficiency is achieved when a design point lies at the edge of the voltage-limited regime, that is, on the regime-divider line.* Therefore, the *final* optimum design should be sought at the edge of the voltage-limited regime. If a design point lies in the voltage-limited regime, the design will suffer from *waste of power.* Placing the optimum design point at the edge of the voltage-limited

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appealed to in order to gain more insight into the results and provide key ideas in advancing the optimization process.

regime can be accomplished by appropriately choosing the inductor and the bias current as will be seen later.

Due to the dominant contribution of drain current noise to phase noise, the dependence of phase noise on transistor width, w, and maximum capacitance of varactors, c, is weak. This fact is well reflected in phase noise approximation (18.23), which suggests the strong dependence of phase noise on choice of inductor and bias current and resultant voltage swing rather than c and w. For example, in Figure 18.7, phase noise at points B and C are no more than 1dB and 0.5 dB higher than phase noise at point A. The larger 1 dB difference can be attributed to the larger voltage swing difference between A and B. Henceforth, unless the shaded region drawn for a given inductor and bias current experiences a large voltage swing difference across it, the phase noise variation within the shaded area is insignificant. Thus, in the following two sections, we investigate effects of inductor selection upon the design constraints, voltage swing and phase noise. Once an inductor is selected, the method of GNP of this section can be used to optimize the design by properly selecting w and c.

18.4.3. GNP with a Fixed Inductance Value

In this subsection, we vary structures of inductors for *a fixed value of inductance L* and *a fixed bias current I* and investigate the resultant changes in the minimum phase noise.

We first appeal to an example with two inductors where Inductor-1 is the one used in the previous subsection while Inductor-2 is chosen to have the same inductance, yet different geometric parameters such that it has higher loss, that is, $g_{L1} < g_{L2}$. Design constraints with Inductor-2 are drawn in Figure 18.9 with a bias current of 4mA. When compared to Figure 18.7 which shows design constraints with Inductor-1 and the same bias current of 4mA, the downward translation of the voltage swing line in Figure 18.9 makes a conspicuous contrast. Due to the lowered voltage swing line, Figure 18.9 has no single feasible design point. This high sensitivity of voltage swing to g_L comes from the direct coupling of g_{tank} and g_L in (18.4).

If the voltage swing constraint is ignored, the oscillator with Inductor-2 has feasible design points satisfying all the remaining constraints inside the triangle in Figure 18.9. Figure 18.10 shows the design constraints of Figure 18.7 and Figure 18.9 simultaneously in the same cw-plane. The figure shows that the increase in g_L leads to a considerable right-shift of the start-up line as well as the downward translation of the voltage swing line. This high sensitivity of the start-up condition to g_L can be attributed to the strong coupling between g_{tank} and g_L as well.

By applying the method of GNP to Figure 18.9, we see that the minimum phase noise at 600kHz offset from a 2.4 GHz carrier is 3 dB higher than the

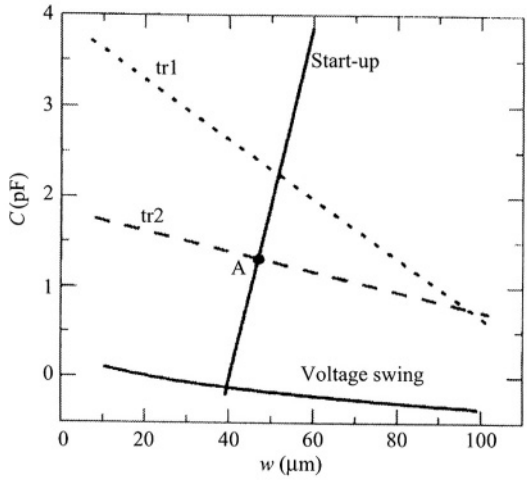


Figure 18.9. Inductor-2, 4 mA.

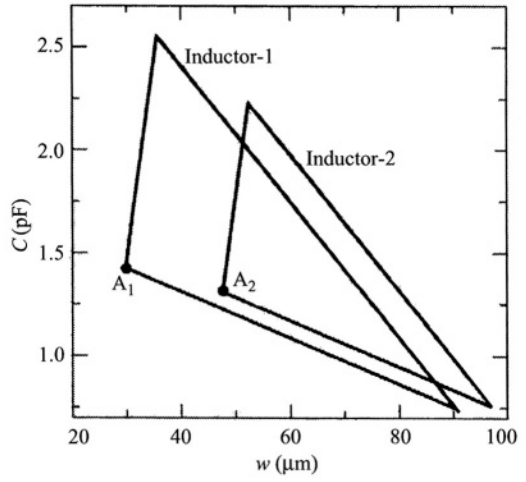


Figure 18.10. Constraint change due to inductor change.

minimum phase noise with Inductor-1 under otherwise the same conditions. The difference in phase noise mainly comes from the change in the voltage swing due to the difference in loss of the two inductors. Also, the optimum design point shift from A_1 to A_2 in Figure 18.10 due to the right shift of the start-up line with increasing g_L also explains part of the phase noise difference. A remarkable notion is that *even though the inductor noise per se is not important due to its small contribution to phase noise, the selection of inductor affects*

phase noise performance considerably, mainly due to the high sensitivity of voltage swing to inductor loss.

In more general terms, the decrease of g_L with a fixed inductance and a fixed bias current translates the voltage swing line upward and the start-up line to the left, resulting in an enhanced voltage swing, an easier start-up and thus a lower minimum phase noise. Once oscillation reaches the voltage-limited regime with the decrease of g_L, further reduction in g_L does not augment the voltage swing any more. However, it is still important to minimize g_L as it will make more room for inductance reduction, which is a crucial step in our optimization process as will be seen in the following subsection. Summarizing, *for a fixed inductance, L, and a fixed bias current, I, an optimum inductor to minimize the phase noise is the one that has the minimum* g_L. The minimum g_L for a given inductance L will be denoted as $g_L\{\min\}$.

Minimization of g_L for a given inductance L can be done in various ways. For instance, the method of geometric programming is used to maximize the inductor quality factor Q_L for a given inductance L in [24], and minimization of g_L for a given inductance L can be done in a similar fashion. By using the data of maximum Q_L versus inductance from [24] and using the approximate relationship between Q_L and g_L, $Q_L \approx (\omega L g_L)^{-1}$, it can be easily seen that the $g_L\{\min\}$ monotonically increases with the decrease of inductance as in Figure 18.11. This monotonicity is of crucial importance in the inductance optimization process in the following subsection.

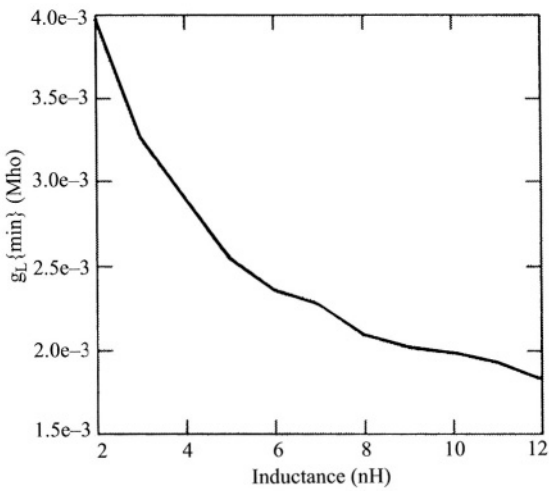


Figure 18.11. $g_L\{\min\}$ versus inductance value.

18.4.4. Inductance and Current Selection

As we know how to find the optimum inductor for a given inductance, the next step is to select *an optimum inductance* to globally minimize phase noise.

Phase noise is proportional to L^2 according to (18.23). This suggests that if two different inductors L_1 and L_2 with $L_1 < L_2$ can result in the same voltage swing for the same bias current in the voltage-limited regime, the inductor with the inductance of L_1 should be selected to obtain a better phase noise performance. Although this may seem counter-intuitive at first, physical intuition can be obtained by resorting to the concept of total charge swing, $q_{\max}$, conceived in [28] and shown in (18.12). For a fixed oscillation frequency, a smaller inductance makes the tank capacitance larger, which accordingly augments the total charge swing in the course of oscillation. Intuitively, a larger total charge swing makes the tank less sensitive to perturbation from noise sources, resulting in a better phase noise performance.

The design strategy to select an optimum inductance value for the minimum phase noise is based upon the observation above and phase noise approximation (18.23) and is stated as follows. *Phase noise reaches near-minimum if not minimum by first setting the bias current to the maximum specified and second finding the minimum inductance that is still capable of producing the maximum voltage swing allowed by the design constraints and does not violate the start-up constraint.* The use of the word *near-minimum* is due to the approximate nature of (18.23). The *maximum voltage swing allowed by the design constraints* is, if the available power is enough to achieve the maximum voltage swing of V_{supply}, nothing but V_{supply}. We proceed our discussion after supposing that available power is enough and $V_{\text{sw,max}} = V_{\text{supply}}$.

The unique existence of such minimum inductance, $L_{\min}$, can be proven by considering the monotonic increase of $g_L\{\min\}$ with the decrease of inductance which is shown in Figure 18.11. As the inductance decreases, $g_L\{\min\}$ and corresponding g_{tank} increase monotonically. In excess of a certain critical $g_L\{\min\}$, either the maximum voltage swing requirement $V_{\text{sw,max}} = V_{\text{supply}}$ or the start-up constraint will be violated as can be easily seen from (18.4), (18.12) and (18.24). The inductance corresponding to this critical $g_L\{\min\}$ is the minimum inductance $L_{\min}$. For any inductor whose inductance is less than $L_{\min}$, $g_L\{\min\}$ is larger than the critical value due to the monotonicity and, therefore, either the voltage swing requirement or the start-up condition cannot be satisfied. If an inductance L larger than $L_{\min}$ is used, the design will suffer from *waste of inductance* by the amount of $\Delta L = L - L_{\min}$.

The reason to set the bias current to $I_{\max}$ is provided by (18.23). A larger current not only directly lowers the phase noise by increasing the tank amplitude, but also lowers $L_{\min}$, further decreasing the phase noise. This is because $g_L\{\min\}$ becomes larger to achieve a required voltage swing with a larger

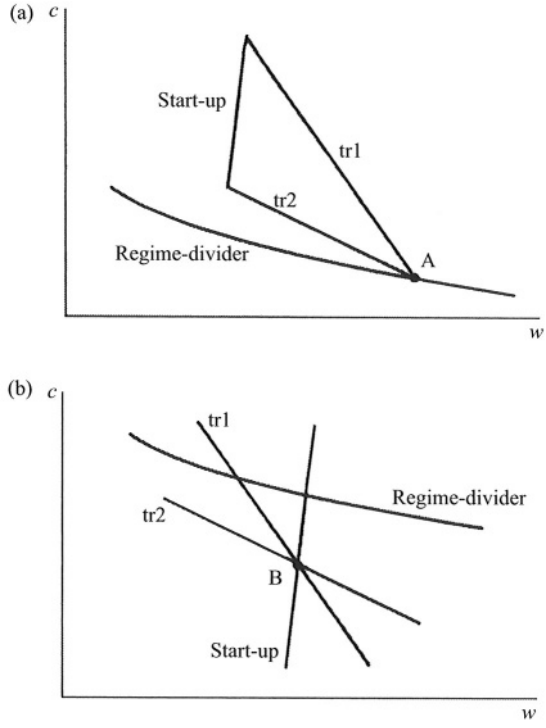


Figure 18.12. Constraints with $L = L_{\min}$: (a) supply-voltage-limited, (b) start-up-limited.

current. The underlying assumption is that the rate of decrease in L^2 is fast enough to overcome the increase in I_{edge}[8] in (18.23) to improve phase noise. However, the design may suffer from *waste of power* with the use of maximum current unless the design guided by the optimization strategy leads to an oscillation at the edge of the voltage-limited regime. Henceforth, it is important to check if the optimization strategy achieves design at the edge of the voltage-limited regime.

If further reduction of the inductance below $L_{\min}$ results in a voltage swing below V_{supply}, the optimization method places the design point on the regime divider line. The design constraints at $L = L_{\min}$ in the cw-plane for this *supply-voltage-limited* case are depicted in Figure 18.12(a). A slight reduction of inductance below $L_{\min}$ will translate the regime-divider line downward and the voltage swing will drop below V_{supply}. As the optimum design A lies on

[8] The eventual design should lie at the edge of the voltage-limited regime. In this sense, we can replace I with I_{edge}.

the regime-divider line, we achieve the optimum design at the edge of the voltage-limited regime.

When the start-up constraint limits further reduction of the inductance below $L_{\min}$, the design achieved with this optimization strategy suffers from *waste of power.* The design constraints at $L = L_{\min}$ in the cw-plane for this *start-up-limited* case are depicted in Figure 18.12(b) where the unique feasible design point is B. A slight decrease in the inductance from $L_{\min}$ will translate the start-up line to the right and the start-up constraint will be violated. In this case, the design point A resides below the regime-divider line and the oscillation occurs in the voltage-limited regime, suffering from *waste of power.* Fortunately, a simple *current readjustment* leads to an optimum design, overcoming the waste of power. As mentioned earlier, the start-up and tuning range lines show little or no dependence on the bias current. Thus, the bias current can be reduced from $I_{\max}$ until the regime-divider line translates downward to have the point A on it, without altering other lines. The amount of the current reduction is normally not significant since the voltage swing is very sensitive to the current.

18.4.5. Summary of the Optimization Process

The design optimization process can be summarized as the following. First, the bias current is set to $I_{\max}$. Second, an inductance is fixed at a certain value and an inductor that minimizes g_L for the fixed inductance value is selected. Third, using the selected inductor, the design constraints are drawn in the cw-plane. If there exists feasible design points in the cw-plane, we decrease the inductance and repeat the same procedure in the second and third step until the feasible design area shrinks to a single point in the cw-plane as in Figure 18.12. Recall that feasible design points must satisfy $V_{sw} = V_{supply}$, which implies that the inductance decreasing procedure occurs in the voltage-limited regime.[9] The single design point in the cw-plane represents the optimum c and w and the corresponding inductor with $L = L_{\min}$ is the optimum inductor. In the supply-voltage-limited case, the optimum current is $I_{\max}$. In the start-up-limited case, the optimum current is obtained by reducing I from $I_{\max}$ until the regime-divider line has the single feasible design point on it in the cw-plane in Figure 18.12(b).

The optimization procedure can be easily understood by introducing the inductor *3D-bsn* optimization space shown in Figure 18.13, where the lateral dimension of spiral inductors, *d,* was set to $d_{\max}$. In Figure 18.13, the hypothetical shaded region in the inductor optimization space represents the set of points (*b, s, n*) for which feasible design points exist in the cw-plane where the feasible design points also satisfy $V_{sw} = V_{supply}$. The surfaces labeled with L_n

[9] Thus, the initial selection of inductance should be large enough.

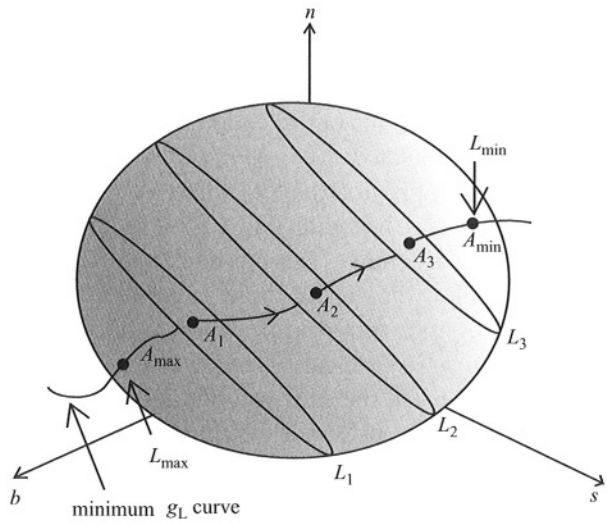


Figure 18.13. Inductor optimization space.

for $n = 1, 2, 3$ denote the *equi-inductance surfaces* in which the inductance is constant yet geometric structures of inductors can vary. The only point of concern on each surface is the point at which g_L becomes minimum. Such points are denoted by A_n for $n = 1, 2, 3$ in the figure and the curve connecting all the possible minimum g_L points is shown in the same figure. The inductance decreases in the direction indicated by the arrow while $g_L\{\min\}$ increases monotonically along the curve in the same direction. The optimum inductor occurs at the intersection of the minimum g_L curve with the boundary of the shaded region at point A_{min}. With the optimum inductor given with point A_{min}, the design constraints in the cw-plane look like either Figure 18.12(a) or (b), depending upon which of the supply-voltage-limited and start-up-limited case is encountered first.

18.4.6. Remarks on Final Adjustment and Robust Design

Due to approximate nature of (18.23), the design may need final fine-tuning before implementation. As an example, consider the supply-voltage-limited case. Due to the high sensitivity of the voltage swing to g_L, a slight increase of inductance by ΔL from L_{min} will lead to a new configuration of design constraints in the cw-plane as shown in Figure 18.14, while $\Delta L/L_{min} \ll 1$. The new optimum design point A is also at the edge of the voltage-limited regime dissipating the same bias current as the previous design, while the inductance is slightly larger. This slight change of inductance does not cause

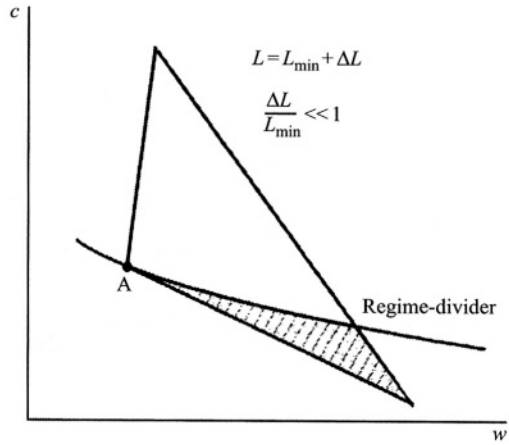


Figure 18.14. $L = L_{min} + \Delta$ and constraints.

a large phase noise increase and hence the change can be accepted if one prefers smaller size of transistors. Furthermore, as (18.23) is an approximation ignoring the dependence of phase noise on the transistor size and the MOSCAP capacitances, for the small-scale change of inductance, lowering transistor size may reduce the phase noise a little further. Indeed, our oscillator was optimized as in Figure 18.14. Equation (18.12) predicts a phase noise of – 119 dBc/Hz at 600kHz offset from the 2.4 GHz center frequency dissipating 4 mA from 2.5 V supply for the designed oscillator. The noise contribution of drain current noise, gate noise, inductor noise and varactor noise is 90%, 2%, 6% and 2%, respectively. Note that most of the circuit noise is contributed from the drain current noise of cross-coupled transistors, as predicted earlier. We will compare this result to simulations and measurements later.

The graphical visualization of design constraints can help coping with possible process variations, leading to a robust design. Figure 18.15 depicts the process variation and the resultant hypothetical design constraint change. The broken lines represent design constraints in the *slow process corner* while the solid lines represent design constraints in the *fast process corner.* The robust design points are selected in the inside of the inner triangle, sides of which consist of broken lines. The shaded area in the figure represents unreliable design, which cannot meet all the design constraints in the presence of process variations.

18.5. Discussion on LC VCO Optimization

One of the most important results of the previous section is that the minimum phase noise is obtained by minimizing inductance as far as the voltage swing

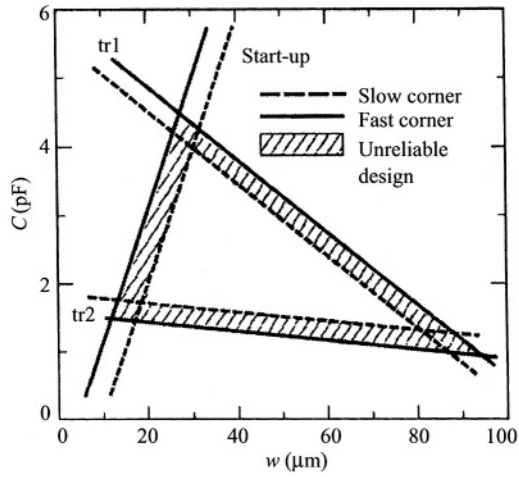


Figure 18.15. Process variations and corresponding design constraints.

is kept at the largest value allowed. The existence of such optimum inductance can be easily understood by realizing that phase noise is the ratio of noise to signal. While increasing inductance results in a larger voltage swing in the current-limited regime, it also increases the tank noise, which was justified previously using the charge swing concept.

While many publications on LC oscillators are aware that a larger inductance helps increase voltage swing, they mostly do not consider that tank noise increases with an increasing inductance as well. This certainly leads to a misconception, as in [7], that a maximized inductance within self-resonance frequency and tuning range consideration results in a better phase noise.

The increase of oscillator tank noise with the increase of inductance or decrease of capacitance for a fixed oscillation frequency can be given a fundamental explanation based upon thermodynamics. The voltage across a capacitor in parallel with a resistor at temperature T is a random process, and its probability distribution function is given according to the *canonical distribution* [36]

$$p(v) \propto \exp\left(-\frac{E}{kT}\right) = \exp\left(-\frac{Cv^2}{2kT}\right) \tag{18.27}$$

where the proportionality constant is $\sqrt{C/(2\pi kT)}$ for a proper normalization. Then the average of the squared noise voltage across the capacitor becomes

$$\langle v^2 \rangle = \int_{-\infty}^{\infty} v^2 p(v)\, dv = \frac{kT}{C} \tag{18.28}$$

This is the well-known *kT* / *C-noise* of RC switch circuits, but the generality kept at the derivation above tells that the *kT* / *C*-noise is a much more general feature than has been thought in any circuit including capacitors, for example, LC oscillators. Equation (18.27) is *approximately true* in LC oscillators since the introduction of inductors makes the probability distribution function of the noise voltage across the LC tank more complicated than (18.27). However, (18.28) still captures the essential feature of the tank noise of LC oscillators: *an LC tank consisting of a larger capacitor and a smaller inductor for a fixed resonance frequency is less sensitive to perturbations and has smaller noise voltage across it.* Another way of deriving the *kT* / *C*-noise dependence is resorting to *equipartition theorem* [36] of thermodynamics which states that each independent degree of freedom of a system in equilibrium has a mean energy of *kT* / 2, that is,

$$\tfrac{1}{2}C\langle v^2\rangle \approx \tfrac{1}{2}kT \tag{18.29}$$

which again results in the approximate *kT* / *C-noise* dependence of LC tanks.

This approximate *kT* / *C*-noise dependence of the LC tank delivers a statistical idea via the number of charge carriers oscillating in the LC tank. When the inductance is smaller or the capacitance is larger, more charge carriers are populated in the LC tank according to $Q = CV$ for a given voltage swing and are participating in the oscillation. More numbers of oscillating electrons make the LC tank less sensitive to perturbations as the ratio of the number of injected charge carriers due to noise to the number of oscillating electrons is smaller.

An insightful mechanical analogy to the phase noise optimization of LC oscillators can be made using a mass-spring oscillatory system suspended in water and subject to random bombardment of water molecules. The loss due to the friction of water is compensated by a trembling hand, which follows the oscillation of the mass and continuously injects accordingly energy to the system.[10] In this analogy, the mass *m* corresponds to the capacitance *C,* the random movement of water molecules corresponds to the tank noise, the hand trembling corresponds to the transistor drain current noise, and the velocity of the mass corresponds to the oscillator output voltage. As the force imposed on the mass by the hand is larger than the friction of water to sustain the oscillation, the corresponding hand trembling noise dominates over the water molecule bombardment noise. This is in analogy with the fact that the transistor drain current noise dominates in LC oscillators. Now for a given energy, a smaller mass results in a larger maximum velocity. Considering only the velocity or signal aspect, it is appealing to use a smaller mass to get a better noise performance. However, a smaller mass is more sensitive to the hand trembling

[10] In analogy with Colpitts oscillators, however, the hand taps the mass when its motion instantaneously ceases.

noise. So balancing well between the signal and noise aspects and finding an optimum mass is essential to lead to the optimum noise performance.

18.6. Simulation

The phase noise obtained in the previous section is approximate for several reasons. The value for E_{sat} is estimated from device data, Γ_{rms} is approximated with $1/\sqrt{2}$, cyclostationary effects are ignored and all the variables used are derived from small-signal analysis while some constraints such as voltage swing require a more general large-signal approach. Also, the phase noise due to the tail current source was not taken into account. Finally, the symmetric inductor model used as a part of the tank model is approximate, as it does not consider the physical asymmetry of the spiral structure mainly due to the metal underpass [37]. In this section, an accurate phase noise simulation is performed [38] on the VCO designed using our optimization process.

A more accurate non-symmetric equivalent circuit for spiral inductors is depicted in Figure 18.16 and used in simulations. This non-symmetric model was developed using ASITIC to address the physical asymmetry of the spiral structure [37].

Phase noise simulation is performed at 2.22 GHz with a tail current of 4 mA. The ISF of various noise sources are obtained by performing the charge injection simulation [28] and are depicted in Figure 18.17 for PMOS, NMOS and tail transistors. The cyclostationary effect of the drain current noise due to the periodic operating point change can be captured by the *noise modulating function* (NMF), which is proportional to g_{d0} [28]. The simulated NMF and the effective ISF which is the product of the ISF and NMF for the drain current noise are depicted in Figures 18.18 and 18.19, respectively, for PMOS and NMOS transistors.

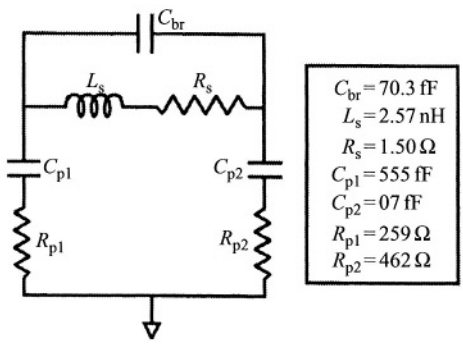


Figure 18.16. Non-symmetric spiral inductor model.

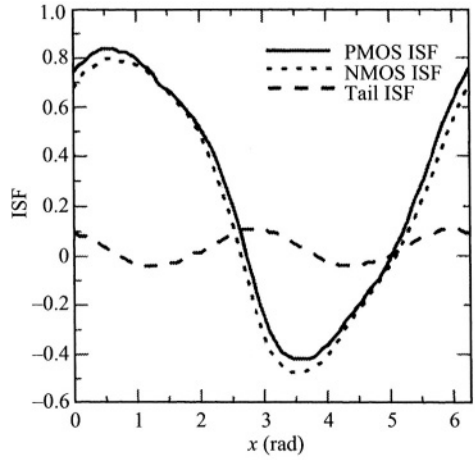


Figure 18.17. ISF.

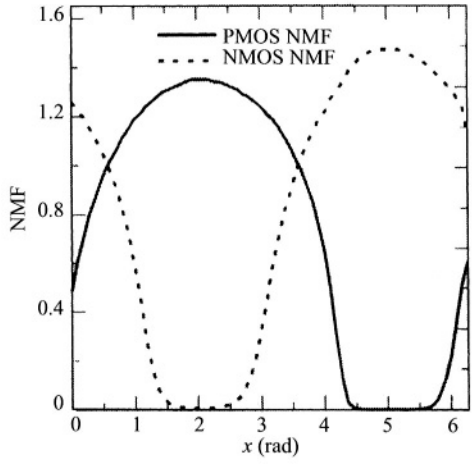


Figure 18.18. NMF.

The total simulated phase noise is – 120 dBc/Hz at 600kHz offset from a 2.22 GHz carrier. The circuit noise contributions from each noise source are shown in Table 18.1. The simulation result shows 1 dB difference from the prediction made using (18.12).

18.7. Experimental Results

Table 18.2 summarizes performance of the VCO, which was implemented in three-metal, 0.35 μm BiCMOS technology, only using MOS transistors.

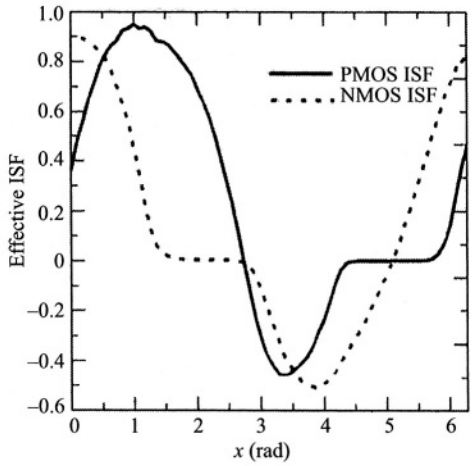


Figure 18.19. Effective ISF.

Table 18.1. Simulated result of noise contributions from each noise source.

Noise source	*PSD* (A^2/Hz)	*Contribution (%)*
Drain current	6.90×10^{-23}	86
Gate	1.20×10^{-24}	1.5
Inductor	4.49×10^{-24}	5.6
Varactor	1.77×10^{-24}	2.2
Tail current	3.73×10^{-24}	4.7

Figure 18.20 shows the VCO chip photograph. A tuning range of 26% is achieved as shown in Figure 18.21. Phase noise is measured using an HP8563 spectrum analyzer with phase noise measurement utility. The measured phase noise at 2.2 GHz is about 3 dB higher than the simulated phase noise. This 3 dB difference can be attributed to the uncertain channel noise factor, γ, degradation of voltage swing caused by the parasitic resistors in metal layers and high sensitivity of the oscillation frequency to extrinsic supply and control line noise due to the high VCO gain at this frequency.

To measure the phase noise more accurately, we increased the control voltage up to 3.5 V which further reduces the oscillation frequency down to 1.91 GHz where the VCO gain is very low. Figure 18.22 shows a plot of measured phase noise vs offset frequency from the 1.91 GHz carrier. The phase noise measurement at 600 kHz offset from the 1.91 GHz carrier yields – 121 dBc/Hz.

To compare the performance of our oscillator to recently reported results [1–23], we use two figures of merit defined in [39]. First,

Table 18.2. VCO performance summary.

Supply voltage	2.5 V
Current (core)	4 mA
Center frequency	2.33 GHz
Tuning range	26%
Output power	0 dBm
Phase noise (f_c = 1.91 GHz @600 kHz)	−121 dBc/Hz
Phase noise (f_c = 2.03 GHz @600 kHz)	−117 dBc/Hz
Phase noise (f_c = 2.63 GHz @600 kHz)	−115 dBc/Hz

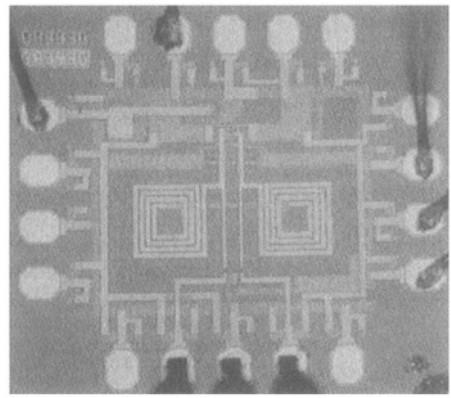


Figure 18.20. VCO chip photograph.

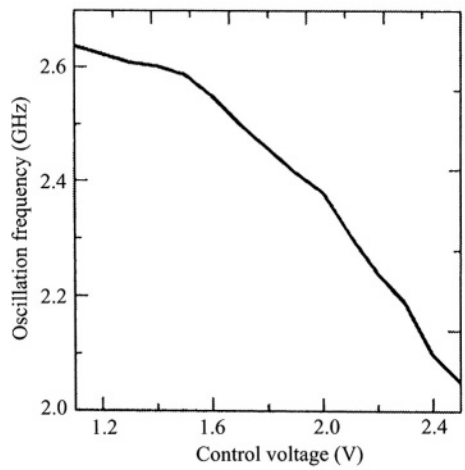


Figure 18.21. Frequency tuning.

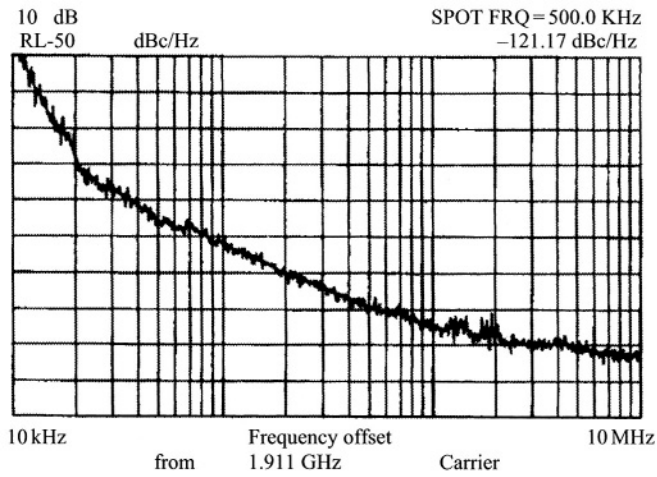


Figure 18.22. Phase noise vs f_{off} at 1.91 GHz.

power-frequency-normalized (PFN) figure of merit:

$$\text{PFN} = 10\log\left[\frac{kT}{P_{\text{sup}}}\cdot\left(\frac{f_0}{f_{\text{off}}}\right)^2\right] - \pounds\{f_{\text{off}}\} \tag{18.30}$$

was devised noting that phase noise of an oscillator measured at an offset f_{off} from a carrier at f_0 is proportional to f_0^2 and inversely proportional to f_{off}^2 [40] as well as the power dissipated in the resistive part of the tank. As the power dissipated in the resistive part of the tank cannot be easily calculated from the VCO specification, phase noise is normalized to kT/P_{sup} in (18.30), where P_{sup} is the total dc power dissipated in the VCO. PFN is a unit-less figure of merit and a larger PFN corresponds to a better oscillator.

To take tuning range into account for comparison among oscillators, the second figure of merit called, *power-frequency-tuning-normalized* (PFTN)

$$\text{PFTN} = 10\log\left[\frac{kT}{P_{\text{sup}}}\cdot\left(\frac{f_{\text{tune}}}{f_{\text{off}}}\right)^2\right] - \pounds\{f_{\text{off}}\} \tag{18.31}$$

was devised where $f_{\text{tune}} = f_{\max} - f_{\min}$. Note that PFTN is a normalization of PFN to the tuning range, $(f_{\text{tune}}/f_0)^2$. Again a larger PFTN corresponds to a better oscillator.

Using these two figures of merit, this work is compared to oscillators reported in [1–23] in Figures 18.23 and 18.24. Our oscillator has the second largest PFN and the largest PFTN among the oscillators with on-chip inductors where our PFTN was reported using the phase noise at the center frequency.

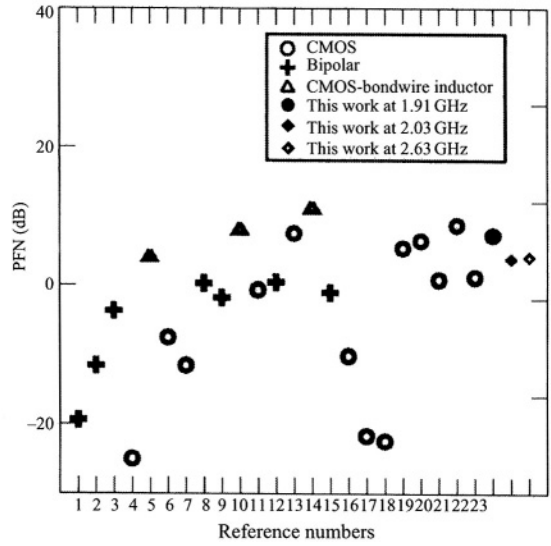


Figure 18.23. PFN for various oscillators.

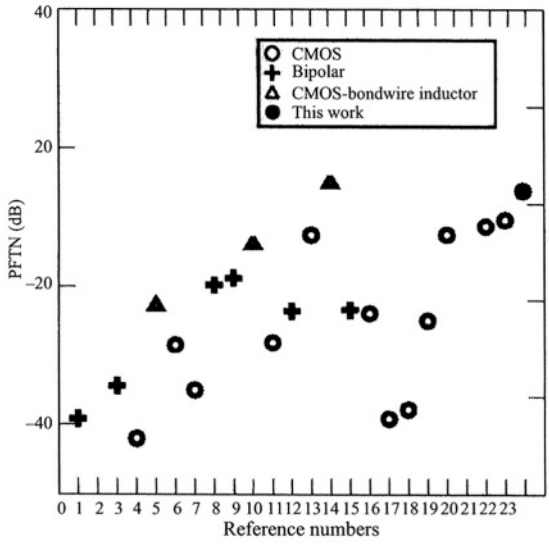


Figure 18.24. PFTN for various oscillators.

18.8. Conclusion

A general and insightful optimization technique to design integrated LC VCOs utilizing GNP was reviewed. A method for selecting the optimum inductor to minimize phase noise was emphasized. A 2.4 GHz fully integrated

LC VCO was designed using our optimization technique and implemented as a design example. A tuning range of 26% was achieved with the inversion mode MOSCAP tuning. The measured phase noise was –121, –117 and –115 dBc/Hz at 600 kHz offset from 1.91, 2.03 and 2.60 GHz carriers, respectively. The designed VCO dissipates only 4 mA from a 2.5 V supply voltage. Comparison with other oscillators using two figures of merit, PFN and PFTN, supports the adequacy of our design methodology.

Acknowledgments

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Chapter 19

TRADE-OFFS IN OSCILLATOR PHASE NOISE

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19.1. Motivation

The frequency spectrum is a valuable commodity as the ever increasing number of wireless users demand more efficient usage of the already scarce frequency resources. Communication transceivers rely heavily on frequency conversion using local oscillators (LOs) and, therefore, the spectral purity of the oscillators in both the receiver and the transmitter is one of the factors limiting the maximum number of available channels and users. For that reason, a deeper understanding of the fundamental issues limiting the performance of oscillators, and development of design guidelines to improve them, are necessary [1–48].

In digital applications, the timing accuracy of the clock signal determines the maximum clock rate and hence the maximum number of operations per unit time. In microprocessors and other synchronous very large-scale digital circuits, the clock signal is generated by on-chip oscillators locked to an external oscillator. Ring oscillators are commonly used for on-chip clock generation due to their large tuning range and ease of integration. In the IC environment, there are additional sources affecting the frequency stability of the oscillators, namely, substrate and supply noise arising from switching in the digital circuitry and output drivers. This new environment and the delay-based nature of ring oscillators demand new approaches to the modeling and analysis of the frequency stability of the oscillators.

We will start this chapter with an introduction to the definitions, describing some of the different methods for quantifying frequency instability in an oscillator. Next, we will introduce a time-variant model for phase noise, using *impulse sensitivity functions* (ISFs), from which the phase response of an oscillator to an arbitrary noise source is determined. Next, we will talk about phase noise trade-offs and design implications in LC and ring oscillators.

19.2. Measures of Frequency Instability

Any practical oscillator has fluctuations in its amplitude and frequency. Short-term frequency instabilities of an electrical oscillator are mainly due to inherent device noise (such as thermal and flicker noise) as well as interference sources (such as supply and substrate noise sources). These sources result in

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frequency instabilities. In this section, we give an introduction to frequency instabilities, their destructive effects on the performance of analog and digital systems, and the definitions of jitter and phase noise.

The output of an ideal oscillator may be expressed as $V_{out}(t) = V_0 \cos[\omega_0 t + \phi_0]$, where the amplitude V_0, the frequency ω_0, and phase reference ϕ_ω are all constants. The one-sided spectrum of an ideal oscillator with no random fluctuations consists of an impulse at ω_0 as shown in Figure 19.1. In a practical oscillator, however, the output is more generally given by

$$V_{out}(t) = V_0 \cdot [1 + A(t)] \cdot f[\omega_0 t + \phi(t)] \tag{19.1}$$

where $\phi(t)$ and $A(t)$ are functions of time, V_0 is the maximum voltage swing and f is a periodic function which represents the shape of the steady-state output waveform of the oscillator. The output spectrum has power around harmonics of ω_0 if the waveform, f, is not sinusoidal. More importantly, as a consequence of the fluctuations represented by $\phi(t)$ and $A(t)$, the spectrum of a practical oscillator has sidebands close to the frequency of oscillation, ω_0, and its harmonics, as shown in Figure 19.1. These sidebands are generally referred to as *phase noise* sidebands.

The destructive effect of phase noise can be best seen in the front-end of a radio receiver. Figure 19.2 shows a typical front-end block diagram, consisting of a low noise amplifier (LNA), a mixer, and an LO. Suppose the receiver tunes to a weak signal in the presence of a strong signal in an adjacent channel. If the LO has large phase noise, as shown in Figure 19.3, some down-conversion of the interfering signal into the same intermediate frequency (IF) as that of the desired signal will occur as shown in Figure 19.3. The resulting interference significantly degrades the dynamic range of the receiver. Therefore, improving

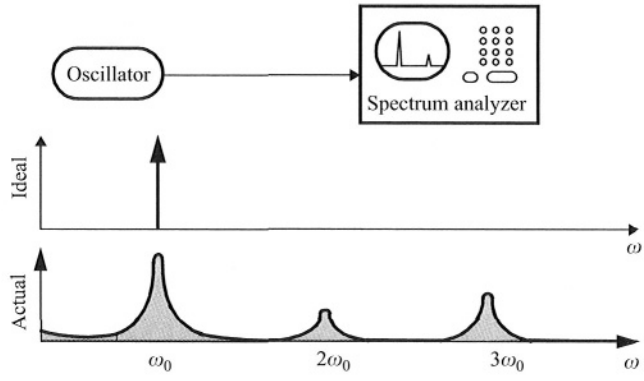


Figure 19.1. The spectrum of an ideal and a practical oscillator.

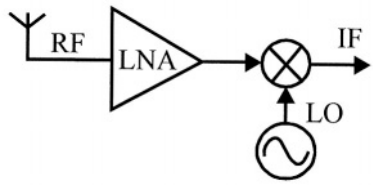


Figure 19.2. Simplified model for the front end of a radio receiver.

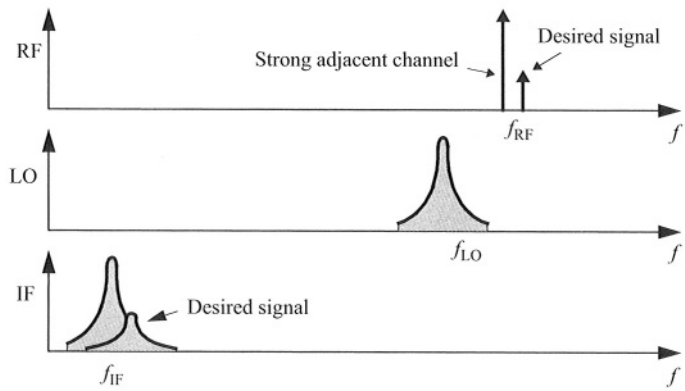


Figure 19.3. The effect of phase noise in presence of adjacent strong channel.

the phase noise of the oscillator clearly improves the signal-to-noise ratio of the desired signal.

In the time-domain viewpoint, the spacing between transitions is ideally constant. In practice, however, the transition spacings will be variable due to fluctuations in $\phi(t)$. This uncertainty is known as *timing jitter* and can be seen in Figure 19.4. In a synchronous digital circuit such as a microprocessor, there is a clock signal that controls the operation of different logic blocks. To emphasize the importance of timing jitter, consider the example of a flip-flop. If the clock signal has zero timing jitter as shown with the solid line in Figure 19.4, the data needs to be stable only for $t_{\text{setup}} + t_{\text{hold}}$. However, if the clock line shows a peak-to-peak jitter of τ_{max}, then the data line needs to be stable for a period of time $2\tau_{\text{max}}$ longer, as shown in Figure 19.4. This decrease in the timing margins will reduce the maximum achievable frequency of operation for the digital circuit.

The harmful effect of clock jitter can also be seen in the sample-and-hold circuit of Figure 19.5, where the accuracy of the sampling process is affected by jitter in the clock. If there is uncertainty in sampling time (i.e. clock jitter), it translates directly to uncertainty in the sampled value (i.e. noise) as shown in Figure 19.5 .

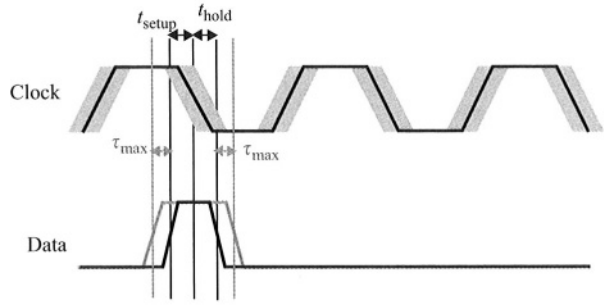


Figure 19.4. The effective timing margin in presence of jitter.

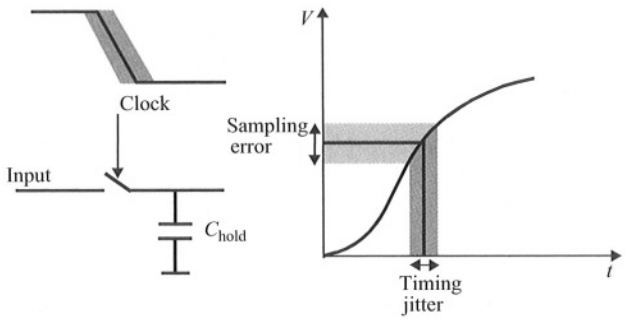


Figure 19.5. The effect of timing jitter sampling error.

19.2.1. Phase Noise

In the frequency-domain viewpoint, an oscillator's short-term instabilities are usually characterized in terms of the single sideband noise spectral density. Units of decibels below the carrier per Hertz (dBc/Hz) are conventionally used and is defined as:

$$\mathcal{L}_{\text{total}}\{\Delta\omega\} = 10 \cdot \log\left[\frac{P_{\text{sideband}}(\omega_0 + \Delta\omega, 1\,\text{Hz})}{P_{\text{carrier}}}\right] \tag{19.2}$$

where P_{sideband} $(\omega_0 + \Delta\omega,$ 1 Hz) represents the single sideband power at a frequency offset, $\Delta\omega$ from the carrier in a measurement bandwidth of 1 Hz as shown in Figure 19.6, and P_{carrier} is the total power under the power spectrum. Note that the definition of (19.2) includes the effect of both amplitude and phase fluctuations, $A(t)$ and $\phi(t)$.

Spectral density is usually specified at one or a few offset frequencies. To be a meaningful parameter, both the noise density and the offset need to be reported, for example, –100 dBc/Hz at 10 kHz offset from the carrier.

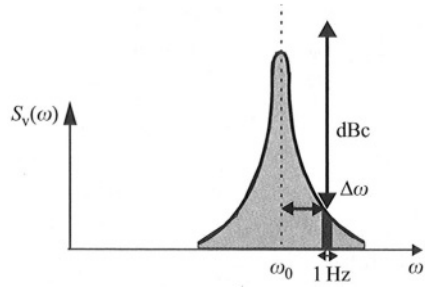


Figure 19.6. The phase noise per unit bandwidth.

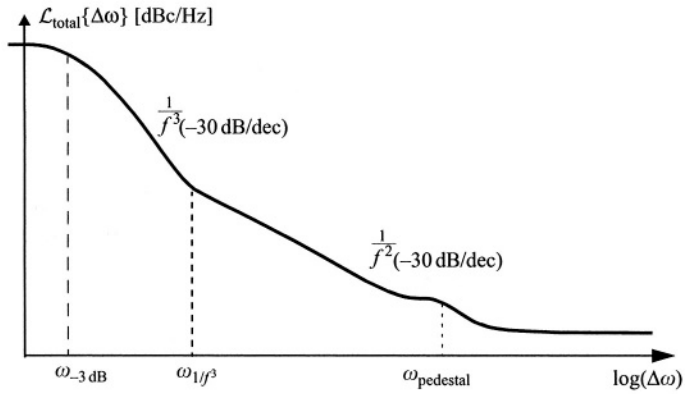


Figure 19.7. A typical phase noise plot for a free running oscillator.

The advantage of $\mathcal{L}_{\text{total}}\{\Delta\omega\}$ in (19.2) is its ease of measurement. Its disadvantage is that it shows the sum of both amplitude and phase variations; it does not show them separately. It is often important to know the amplitude and phase noise separately because they behave differently in a circuit. For instance, the effect of amplitude noise can be reduced by amplitude limiting, while the phase noise cannot be reduced in an analogous manner. Therefore, in most practical oscillators, $\mathcal{L}_{\text{total}}\{\Delta\omega\}$ is dominated by its phase portion, $\mathcal{L}_{\text{phase}}\{\Delta\omega\}$, known as phase noise, which will be simply denoted as $\mathcal{L}\{\Delta\omega\}$, unless specified otherwise.

If one plots $\mathcal{L}_{\text{total}}\{\Delta\omega\}$ for a free-running oscillator as a function of $\Delta\omega$ on logarithmic scales, regions with different slopes may be observed as shown in Figure 19.7. At large offset frequencies, there is a flat noise floor. At small offsets, one may identify regions with a slope of $1/f^2$ and $1/f^3$, where the corner between the $1/f^2$ and $1/f^3$ regions is $0\ \omega_{1/f^3}$. Finally, the spectrum becomes

flat again at very small offset frequencies. The mechanisms responsible for these features will be discussed in great detail in subsequent chapters.

There are different methods of measuring phase noise and, depending on the particular method used to measure it, parts of the spectrum of Figure 19.7 may or may not be observed. For example, if a spectrum analyzer is used to measure the phase noise, $\omega_{-3\,\mathrm{dB}}$ will be easily observed. However, if the phase noise is measured using a phase-locked loop, the nonlinear transfer function of the phase detector will change the measured $\omega_{-3\,\mathrm{dB}}$. A very complete review of these measurement techniques and their properties can be found in [42–48].

19.2.2. Timing Jitter

As mentioned earlier, uncertainties in the transition instants of a periodic waveform are known as clock jitter. For a free-running oscillator, it increases with the measurement interval τ (i.e. the time delay between the reference and the observed transitions). This increase is illustrated in the plot of timing variance shown in Figure 19.8 [32].

This growth in variance, that is, "jitter accumulation", occurs because any uncertainty in an earlier transition affects all the following transitions, and its effect persists indefinitely. Therefore, the timing uncertainty when τ seconds have elapsed includes the accumulative effect of the uncertainties associated with the transitions.

A log–log plot of the timing jitter, σ_τ, versus the measurement delay, τ, for a free-running oscillator will typically exhibit regions with slopes of $\frac{1}{2}$ and 1 as shown in Figure 19.9. In the region with the slope of $\frac{1}{2}$, the standard deviation

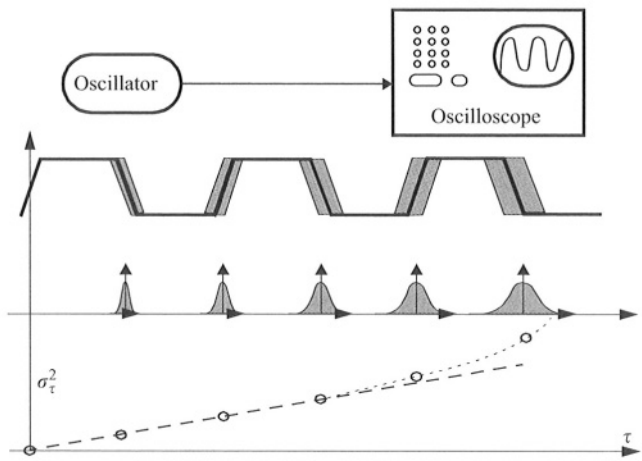


Figure 19.8. Clock jitter increasing with distance from the reference edge.

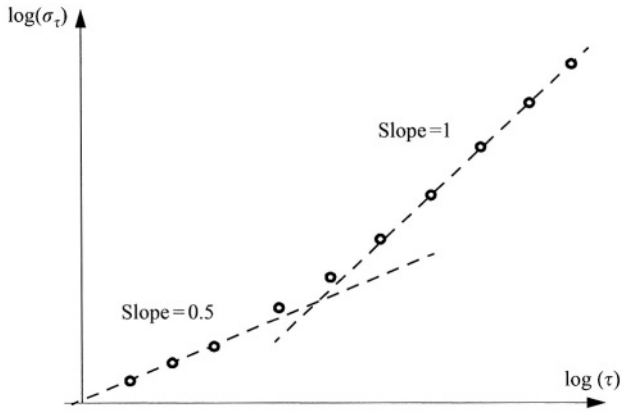


Figure 19.9. Rms jitter vs measurement time on a log–log plot.

of the jitter after τ seconds is [32]

$$\sigma_\tau = \kappa\sqrt{\tau} \tag{19.3}$$

where κ is a proportionality constant determined by circuit parameters. In a similar fashion, the standard deviation of the jitter in the region with the slope of 1 may be expressed as

$$\sigma_\tau = \zeta \cdot \tau \tag{19.4}$$

where ζ is another proportionality constant.

In most digital applications, it is desirable for σ_τ to decrease at the same rate as the frequency increases, to keep constant the ratio of the rms timing jitter to the period. Therefore, phase jitter, defined as

$$\sigma_{\Delta_\phi} = 2\pi\frac{\sigma_\tau}{T} = \omega_0\sigma_\tau \tag{19.5}$$

is a more useful measure in many applications. In (19.5), T is the period of oscillation.

19.3. Phase Noise Modeling

We now give a brief introduction to the time-variant phase noise model [27, 33]. In an oscillator, each perturbation source affects both amplitude and phase of the output signal as shown by the variations in excess phase, $\phi(t)$, and amplitude, $A(t)$, defined by (19.1). Hence, an equivalent system for phase, can be defined, whose input is a perturbation current (or voltage) and its output is the excess phase, $\phi(t)$, as shown in Figure 19.10. Figure 19.11 shows the simplified model of a parallel LC tank oscillating with voltage amplitude, $V_{\max}$.

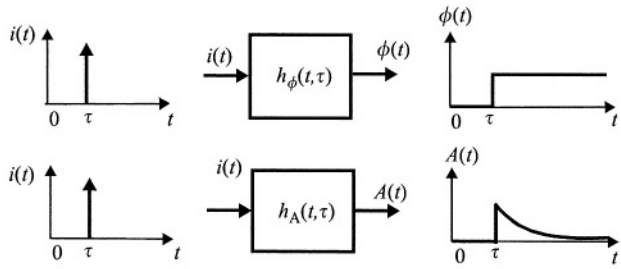


Figure 19.10. Equivalent systems for phase and amplitude.

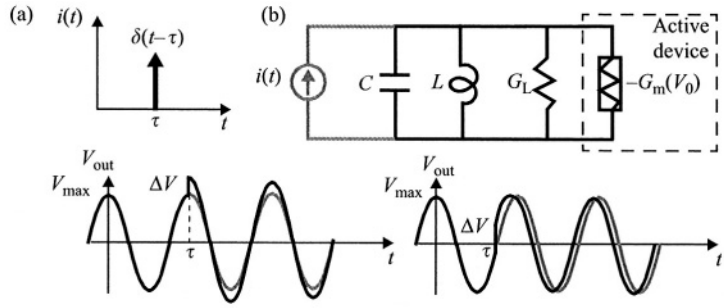


Figure 19.11. Impulse response of an ideal LC oscillator.

A current impulse at the input only affects the voltage across the capacitor with no effect on the current through the inductor. This in turn results in an instantaneous change in the tank voltage and hence a shift in the amplitude and phase depending on the time of injection. For a linear capacitor, the instantaneous voltage change ΔV is given by

$$\Delta V = \frac{\Delta q}{C_{\text{total}}} \tag{19.6}$$

where Δq is the total charge injected by the current impulse and C_{total} is the total capacitance in parallel with the current source. The resultant change in $A(t)$ and $\phi(t)$ is time dependent, as depicted in Figure 19.11. In particular, if the impulse is applied at the peak of the voltage across the capacitor, there will be no phase shift and only an instantaneous amplitude change will result. On the other hand, if this impulse is applied at the zero crossing, it has the maximum effect on the excess phase, $\phi(t)$, and the minimum effect on the amplitude.

There is an important difference between the phase and amplitude responses of practical oscillators. In response to a current impulse, the excess amplitude

undergoes some transient behavior but finally converges to zero because the nonlinear amplitude restoring mechanism existing in any practical oscillator will restore the amplitude to its steady-state value. On the other hand, fluctuations in the excess phase are not quenched by any restoring force and therefore persist indefinitely.

Based on the foregoing argument, a current impulse injecting charge at $t = \tau$ results in a step change in phase, as shown in Figure 19.11. The height of this step will depend on the instant of charge injection. It is important to note that regardless of the size of the injected charge, the equivalent systems of Figure 19.10 remain time-variant. The injected charge induces a voltage change, ΔV, which corresponds to a phase shift, $\Delta\phi$, as shown in the figure. For small injected charge (small area of the current impulse), the resultant phase shift is proportional to the voltage change, ΔV, and hence to the injected charge, Δq. Therefore, $\Delta\phi$ can be written as

$$\Delta\phi = \Gamma(\omega_0\tau)\frac{\Delta V}{V_{\max}} = \Gamma(\omega_0\tau)\frac{\Delta q}{q_{\max}} \quad \Delta q \ll q_{\max} \tag{19.7}$$

where $V_{\max}$ is the voltage swing across the capacitor and $q_{\max} = C_{\text{node}} V_{\max}$ is the maximum charge swing. The function, $\Gamma(x)$, is the time-varying, dimensionless, frequency and amplitude-independent "proportionality factor". It is called the ISF [27], since it determines the sensitivity of the oscillator to an impulsive input. It describes the amount of excess phase shift resulting from application of a unit impulse at any point in time. Figure 19.12 shows the ISF for an LC and a ring oscillator. The ISF for an LC oscillator with a cosine waveform is approximately a sine function. For the ring oscillator, the ISF is maximum during transitions and minimum during the times that the stage of interest is saturated [33].

The current-to-phase transfer function is linear for small injected charge, even though the active elements may have strongly nonlinear voltage–current behavior. The linearity of the current-to-phase system of Figure 19.10 does

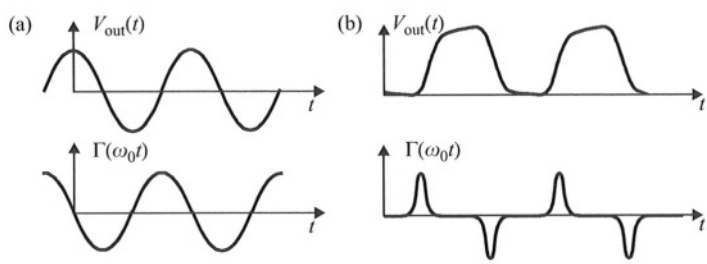


Figure 19.12. Typical ISF for (a) LC and (b) ring oscillators.

not imply linearization of the nonlinearity of the voltage–current characteristics of the active devices. In fact, this nonlinearity affects the shape of the ISF and, therefore, has an important influence on phase noise. Thus, as long as the injected charge is small, the equivalent systems for phase and amplitude can be fully characterized using their linear time-variant unit impulse responses, $h_\phi(t, \tau)$ and $h_A(t, \tau)$. Noting that the introduced phase shift persists indefinitely, the unity phase impulse response can be easily written as:

$$h_\phi(t, \tau) = \frac{\Gamma(\omega_0 \tau)}{q_{\max}} u(t - \tau) \tag{19.8}$$

where $u(t)$ is the unit step. For small arbitrary perturbation current injection, $i(t)$, the output excess phase, $\phi(t)$, can be calculated using the superposition integral, that is,

$$\phi(t) = \int_{-\infty}^{\infty} h_\phi(t, \tau) i(\tau)\, d\tau = \int_{-\infty}^{t} \frac{\Gamma(\omega_0 \tau)}{q_{\max}} i(\tau)\, d\tau \tag{19.9}$$

Since the ISF is periodic, it can be expanded in a Fourier series:

$$\Gamma(\omega_0 \tau) = c_0 + \sum_{n=1}^{\infty} c_n \cos(n\omega_0 \tau + \theta_n) \tag{19.10}$$

where the coefficients c_n are real-valued, and θ_n is the phase of the nth harmonic. As will be seen later, θ_n is not important for random input noise and is thus neglected here. Using this expansion in the superposition integral and exchanging the order of summation and integration, individual contributions to the total $\phi(t)$ for an arbitrary input current, $i(t)$, injected into any circuit node can be identified in terms of the various Fourier coefficients of the ISF. This decomposition can be better seen with the equivalent block diagram shown in Figure 19.13. Each branch of the equivalent system in this figure acts as a bandpass filter and a down-converter in the vicinity of an integer multiple of the oscillation frequency. For example, the second branch weights the input by c_1, multiplies it with a tone at ω_0 and integrates the product. Hence, it passes the frequency components around ω_0 and down-converts the output to the baseband. As can be seen, components of perturbations in the vicinity of integer multiples of the oscillation frequency play the most important role in determining $\phi(t)$. The output voltage, $V(t)$, is related to the phase, $\phi(t)$, through a phase modulation (PM) process as shown in Figure 19.13. The complete process thus can be viewed as a cascade of multiple parallel LTV system that converts current (or voltage) to phase, with a nonlinear system that converts phase to voltage. The evolution of device noise into phase noise due to this process is visualized in Figure 19.14 [27].

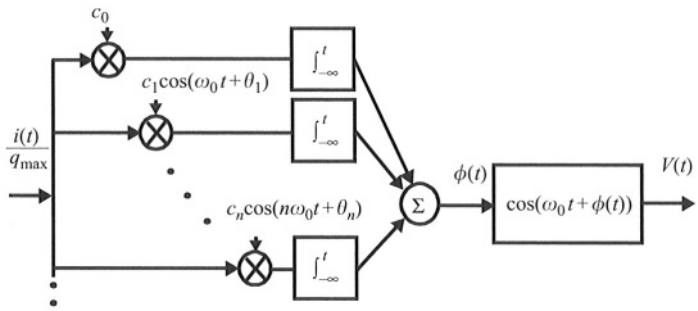


Figure 19.13. The equivalent system for ISF decomposition.

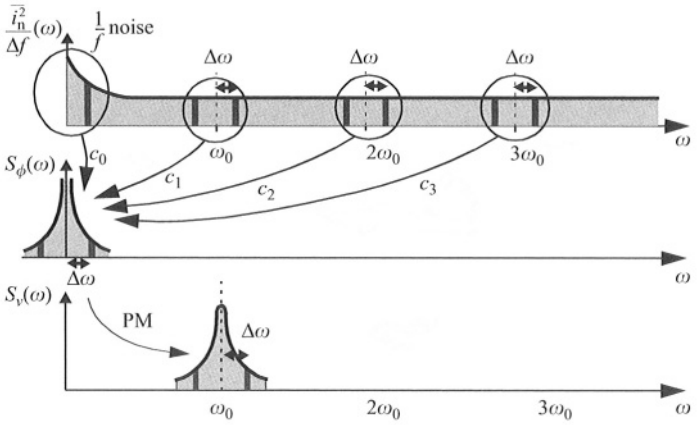


Figure 19.14. Conversion of noise to phase fluctuations and phase noise sidebands.

Consider a random noise current source, $i_n(t)$, whose power spectral density has both a flat region and a $1/f$ region, as shown in Figure 19.14. Noise components located near integer multiples of the oscillation frequency are weighted by Fourier coefficients of the ISF and integrated to form the low-frequency noise sidebands for $S_\phi(\omega)$. These sidebands in turn become close-in phase noise in the spectrum of $S_v(\omega)$ through PM. The total $S_\phi(\omega)$ is given by the sum of phase noise contributions from device noise in the vicinity of the integer multiples of ω_0, weighted by the coefficients c_n. This is shown in Figure 19.15, which shows the spectrum of $\phi(t)$ on log–log scales.

The theory predicts the existence of $1/f^3$ and $1/f^2$ regions in the phase noise power spectrum as well as a flat noise floor due to the device amplification noise as shown in Figure 19.15. Low-frequency noise, such as flicker noise, is weighted by the coefficient c_0 and ultimately produces a $1/f^3$ phase noise

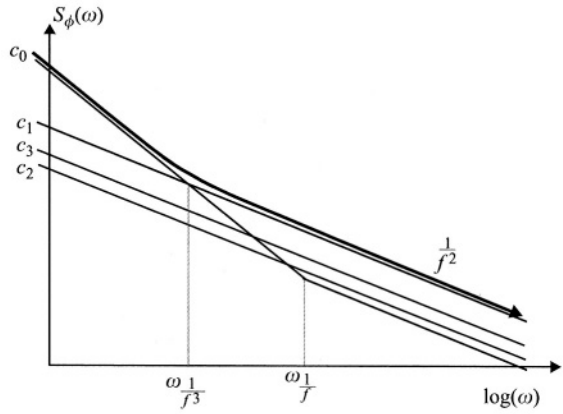


Figure 19.15. $S_\phi(\omega)$ on a log–log axis.

region. White noise terms are weighted by the rms value of the ISF (usually dominated by c_0) and give rise to the $1/f^2$ region of phase noise spectrum. The total sideband noise power in the $1/f^2$ region is the sum of the individual terms, as shown by the bold line in the same figure and will be given by [27]:

$$\mathcal{L}\{\Delta\omega\} = 10\log\left[\frac{\Gamma_{\text{rms}}^2}{q_{\max}^2}\cdot\frac{\bar{i}_n^2/\Delta f}{2\cdot\Delta\omega^2}\right] \tag{19.11}$$

19.3.1. Up-Conversion of $1/f$ Noise

Many active devices exhibit low-frequency noise with a power spectrum that is approximately inversely proportional to the frequency, usually referred to as $1/f$ noise. It is important to note that nothing in the foregoing development implies that the $1/f^3$ corner of the phase noise and the $1/f$ corner of the device noise are the same. In fact, from Figure 19.15, it should be apparent that the relationship between these two corner frequencies depends on the specific values of c_0 and Γ_{rms}. The $1/f^3$ corner of phase noise, $\Delta\omega_{1/f^3}$, is smaller than the device $1/f$ noise corner, $\omega_{1/f}$, by a factor determined by the ratio of the dc to rms value of the ISF [27], that is,

$$\Delta\omega_{1/f^3} = \omega_{1/f}\cdot\left(\frac{c_0}{\Gamma_{\text{rms}}}\right)^2 \tag{19.12}$$

The dc value of the ISF is directly affected by certain symmetry properties of the waveform, such as rise and fall time symmetry [27,33,39]. Exploiting these symmetry properties, oscillators with smaller c_0 can be designed to minimize

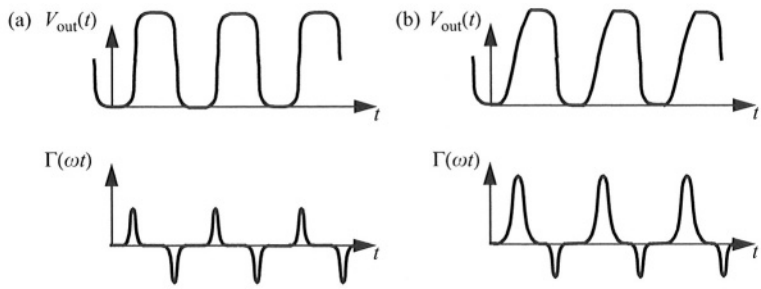


Figure 19.16. Waveform and ISF for (a) the symmetric waveform and (b) the asymmetric waveform.

the up-conversion of $1/f$ noise. Recognizing this fact allows us to identify the design parameters that minimize the up-conversion of low-frequency noise, through proper device sizing, for example.

Symmetry is important to minimize the effect of low-frequency noise, particularly when using surface devices such as MOSFETs. This extra degree of freedom can be exploited to suppress the effect of low-frequency noise on the osillator phase noise. To understand what affects c_0, consider two ring oscillators, with waveforms shown in Figure 19.16. The first waveform has symmetric rising and falling edges, that is, its rise-time is the same as its fall-time. The sensitivity of this oscillator to a perturbation during the rising edge is the same as its sensitivity during the falling edge, except for a sign. Therefore, the ISF has a small dc value. The second case corresponds to an asymmetric waveform with slow rising edge and a fast falling edge. In this case, the phase is more sensitive during the rising edge, and is also sensitive for a longer time; therefore, the positive lobe of the ISF will be taller and wider as opposed to its negative lobe which is short and thinner, as shown in Figure 19.16. It can be shown through simulations and experimentally that the waveform of Figure 19.16(b) results in a larger low-frequency noise up-conversion [27,33].

19.3.2. Time-Varying Noise Sources

The time-varying noise sources have an extremely important impact on the phase noise of an oscillator and can be properly modeled using the time-varying approach. In practical oscillators, the statistical properties of some of the random noise sources change with time in a periodic manner. These sources are referred to as cyclostationary. For instance, the channel noise of a MOS transistor in an oscillator is cyclostationary because the periodically time-varying gate–source overdrive modulates the drain noise power. As an example, consider the Colpitts oscillator of Figure 19.17(a). The simulated drain voltage and current of the transistor are shown in Figure 19.17(b). Note that the drain

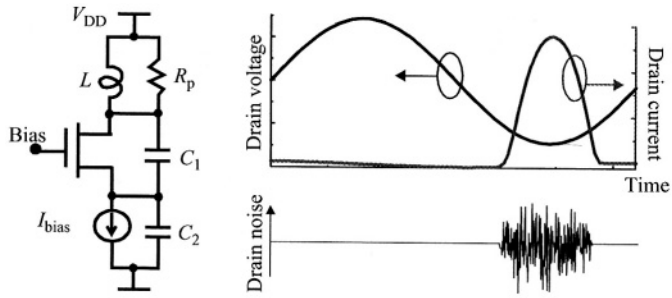


Figure 19.17. MOS Colpitts oscillator.

current consists of a short period of large current followed by a quiet interval [52]. Instantaneous drain current of the transistor controls channel thermal noise power density; therefore, it is the largest during the peak of drain current. Figure 19.17 also shows a sample of drain current noise. The cyclostationary noise current $i_n(t)$ is decomposed as $i_n(t) = i_{n0}(t) \cdot \alpha(\omega_0 t)$, where $i_{n0}(t)$ is a white *stationary* process and $\alpha(\omega_0 t)$ is a deterministic periodic function describing the noise amplitude modulation and, therefore, is referred to as the *noise modulating function* (NMF). The cyclostationary noise can be treated as a stationary noise applied to a system with a new ISF given by

$$\Gamma_{\text{eff}}(x) = \Gamma(x) \cdot \alpha(x) \tag{19.13}$$

where $\alpha(\omega_0 t)$ can be derived easily from device noise characteristics and the noiseless steady-state waveform. Note that there is a strong correlation between the cyclostationary noise source and the waveform of the oscillator. The maximum of the noise power always recurs at a certain point of the oscillatory waveform, thus the average of the noise may not be a good representation of the noise power.

The relative timing of the NMF with respect to the ISF can drastically change the effect of those noise sources. For the Colpitts oscillator of Figure 19.17, the surge of drain current occurs at the minimum of the voltage across the tank, where the ISF is small. The channel noise reaches its maximum power for maximum drain current. This lowers the phase noise degradation due to the channel noise, because the maximum noise power always coincides with the minimum phase noise sensitivity. This concept can be more accurately described using the rms value of the effective ISF. Functions $\Gamma(x)$, $\alpha(x)$ and $\Gamma_{\text{eff}}(x)$ for this oscillator are shown in Figure 19.18. Note that, in this case, $\Gamma_{\text{eff}}(x)$ has a much smaller rms value than $\Gamma(x)$, and hence the effect of cyclostationarity is very significant for the LC oscillator and cannot be neglected.

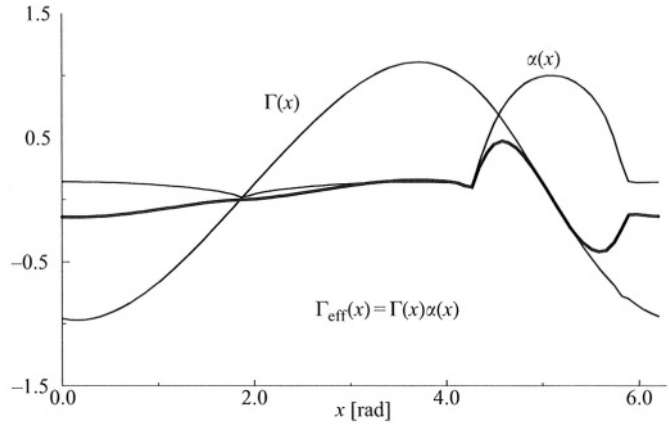


Figure 19.18. $\Gamma(x)$, $\alpha(x)$ and $\Gamma_{\mathrm{NMF}}(x)$ for the Colpitts oscillator of Figure 19.17.

19.4. Phase Noise Trade-Offs in LC Oscillators

Due to their relatively good phase noise, ease of implementation and differential operation, LC oscillators play an important role in high-frequency circuit design [35–41]. We now present design implications in single-ended and differential oscillators.

19.4.1. Tank Voltage Amplitude

Tank voltage amplitude has an important effect on the phase noise, as emphasized by the presence of $q_{\max}$ in the denominator of (19.11). In this subsection, we will derive expressions for the tank amplitude of different types of LC oscillators. The effect of the nonlinearity on the oscillator amplitude can be evaluated using describing function analysis [49–54].

Consider the forward path transconductance block, G, in the two-port model of Figure 19.19(a). It will be assumed that it comprises a memoryless nonlinearity as shown in Figure 19.19(b). In an oscillator with a reasonably high tank Q, the output voltage of the frequency selective network of Figure 19.19 will be very close to a sinusoidal voltage even for a periodic non-sinusoidal input current, as shown in Figure 19.20.

Since the output voltage of the frequency selective network is the input to the nonlinear transconductance block, the response of the nonlinear block, G, to a sinusoidal input should be characterized. Although the output current of the nonlinear transconductance will not be sinusoidal, the frequency selective network will mainly pass the fundamental term of the input since it will attenuate all the other harmonics significantly. Therefore, it is the gain from the

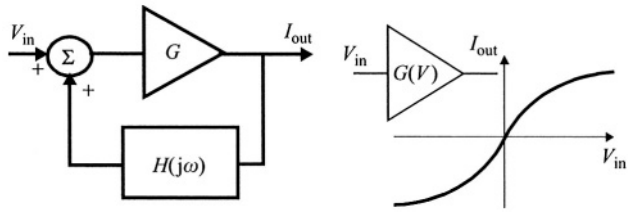


Figure 19.19. Simplified two-port model of an oscillator.

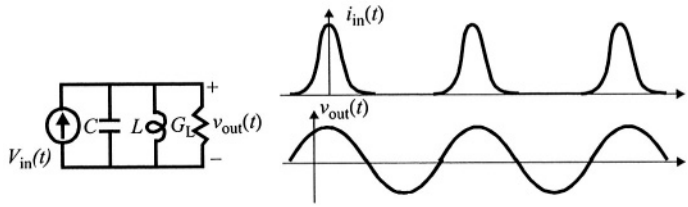


Figure 19.20. The input current and output voltage for a high Q tank.

input sinusoidal voltage to the fundamental component of the output current that determines the loop gain.

Based on the foregoing observations, the nonlinear transconductance is assumed to be driven with a sinusoidal input of amplitude V_1. In the most general case, the output will have all the terms of the Fourier series. Thus, for an input voltage of the following form:

$$v_{in}(t) = V_1 \cos(\omega_0 t) \tag{19.14}$$

the output current can be written as

$$i_{out}(t) = \sum_{n=1}^{\infty} I_n \cos(n\omega_0 t) \tag{19.15}$$

The amplitude ratio of the fundamental output component to the input is the magnitude of the describing function, which will be denoted as $G_m(V_1)$, or G_m for short. Thus,

$$G_m(V_1) = \frac{I_1}{V_1} \tag{19.16}$$

This naming convention underscores that G_m is the effective large signal transconductance of the nonlinear block at ω_0.

Although it is possible to derive the large signal transconductance, G_m, for various active devices [52], investigating the two extreme cases of very large

and very small values of V_1 provides important information. For very small-values of V_1, the small-signal assumption holds and the output grows linearly with input. Therefore,

$$G_m(V_1) = g_m = \frac{I_{tail}}{V_T} \quad V_1 \ll V_T \tag{19.17}$$

where g_m is the small-signal transconductance of the transistor.

For large input amplitude, the output current will consist of sharp spikes of current, whose average value necessarily equals I_{bias}. Therefore, the fundamental component of the output current can be approximated by

$$I_1 = \frac{2}{T}\int_0^T i(t)\cos(\omega_0 t)\,dt \approx \frac{2}{T}\int_0^T i(t)\,dt = 2I_{bias} \tag{19.18}$$

where T is the period of the oscillation. For large values of V_1, the spikes will be very thin and tall and will occur at the peak of the cosine function. This approximation holds as long as the spikes are sharp enough so that the cosine can be approximated as one for the duration of the spike. Hence, the describing function for large values of V_1 can be written as

$$G_m(V_1) = \frac{2I_{tail}}{V_1} \quad V_1 \gg V_T \tag{19.19}$$

As can be seen, the large signal transconductance is inversely proportional to the input voltage amplitude for large values of input voltage. This inverse proportionality provides a negative feedback mechanism that stabilizes the amplitude of oscillations by reducing the effective gain as the amplitude grows.

It is noteworthy that (19.19) is valid for other types of devices with monotonic nonlinearity, such as MOS transistors, vacuum tubes, etc., as long as V_1 is larger than a characteristic voltage that depends on the particular device of interest. This universality holds because the only assumption used to obtain (19.19) is that the spikes are so thin that the cosine function can be approximated as one for the duration of the spike.

Describing function analysis can be applied to calculate the amplitude and frequency of oscillation. As an example, consider the common gate MOS Colpitts oscillator of Figure 19.17. The large signal equivalent circuit for the oscillator of Figure 19.17 can be shown as in Figure 19.21. The tank voltage amplitude is related to V_1 through

$$V_1 = V_{tank}\frac{C_1}{C_1 + C_2} = nV_{tank} \tag{19.20}$$

where

$$n = \frac{C_1}{C_1 + C_2} \tag{19.21}$$

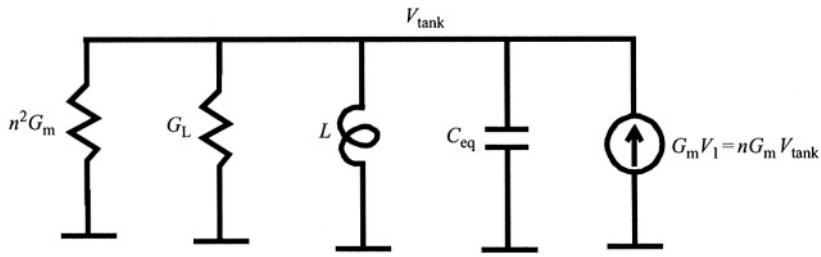


Figure 19.21. The simplified large-signal equivalent circuit.

is the capacitive voltage division ratio. In steady state, tank current is related to the tank voltage through

$$I_{tank} = Y_{tank}V_{tank} = \left(n^2G_m + G_L + jC_{eq}\omega + \frac{1}{jL\omega}\right)V_{tank} = nG_mV_{tank} \tag{19.22}$$

where Y_{tank} and G_L are the admittance and effective parallel conductance of the tank, respectively. For (19.22) to hold, we should have

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{19.23}$$

and

$$G_L = n(1-n)G_m \tag{19.24}$$

Using (19.19) and (19.20), the tank voltage amplitude is calculated to be

$$V_{tank} = 2R_LI_{tail}(1-n) \tag{19.25}$$

As can be seen from (19.25), for small C_1/C_2 ratios, the tank voltage amplitude is about twice the product of tail current and effective tank resistance. This mode of operation is usually referred to as *current limited.*

Note that (19.25) breaks down for small values of I_{tail} in accordance with (19.17). It also fails for *large* values of I_{tail} as V_{tank} approaches V_{DD}. This failure happens as the MOS transistor enters the ohmic region (or saturation for a bipolar transistor) for part of the period, therefore violating the assumptions leading to (19.25). The value of V_{tank} for which this happens depends on the supply voltage, and therefore this regime of operation is known as *voltage limited.*

A simple expression for the tank amplitude of the differential complemetary CMOS LC oscillator of Figure 19.22 can be obtained by assuming that the differential stage switches quickly from one side to another. Figure 19.22 shows

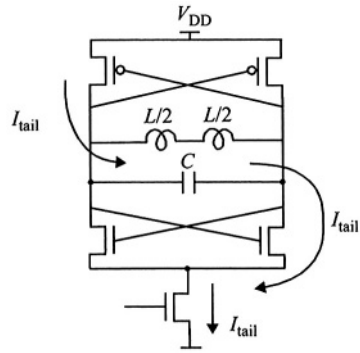


Figure 19.22. Differential CMOS LC oscillator.

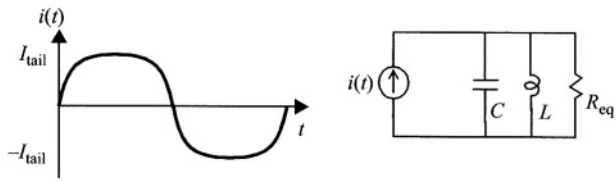


Figure 19.23. The equivalent circuit for the differential oscillator of Figure 19.22.

the current flowing in the complementary cross-coupled differential LC oscillator [36,39] when it is completely switched to one side. As the tank voltage changes, the direction of the current flow through the tank reverses. The differential pair thus can be modeled as a current source switching between I_{tail} and $-I_{tail}$ in parallel with an RLC tank, as shown in Figure 19.23. R_{eq} is the equivalent parallel resistance of the tank.

At the frequency of resonance, the admittances of the L and C cancel, leaving R_{eq}. Harmonics of the input current are strongly attenuated by the LC tank, leaving the fundamental of the input current to induce a differential voltage swing of amplitude $(4/\pi)I_{tail}R_{eq}$ across the tank if one assumes a rectangular current waveform. At high frequencies, the current waveform may be approximated more closely by a sinusoid due to finite switching time and limited gain. In such cases, the tank amplitude can be better approximated as

$$V_{tank} \approx I_{tail}R_{eq} \tag{19.26}$$

This current-limited regime of operation since in this regime, the tank amplitude is solely determined by the tail current source and the tank equivalent resistance. Note that (19.26) loses its validity as the amplitude approaches the supply voltage because both NMOS and PMOS pairs will enter the triode region at the

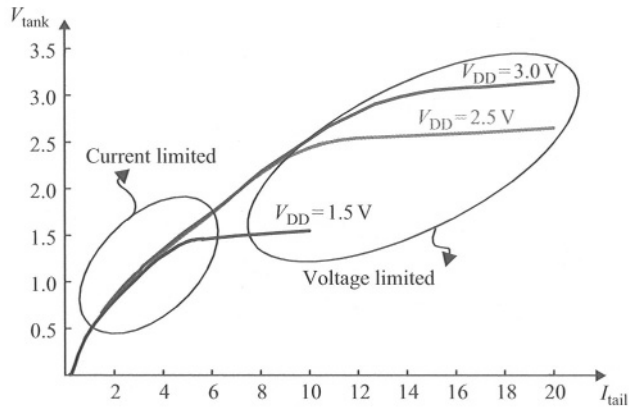


Figure 19.24. Simulated tank voltage vs tail current.

peaks of the voltage and the oscillator will operate in the voltage-limited regime. Also, the tail NMOS transistor may spend most (or even all) of its time in the linear region. The tank voltage will be clipped at V_{DD} by the PMOS transistors and at ground by the NMOS transistors, and hence cannot significantly exceed V_{DD}. Note that since the tail transistor is in the triode region, the current through the differential NMOS transistors can drop significantly when their drain–source voltage becomes very small.

Figure 19.24 shows the simulated tank voltage amplitude as a function of tail current for three different values of V_{DD}. As can be seen, the tank amplitude is proportional to the tail current in the current-limited region, while it is limited by V_{DD} in the voltage-limited regime.

19.4.2. Noise Sources

In general, noise sources in an oscillator are cyclostationary because of the periodic changes in currents and voltages of the active devices. In this subsection, the noise sources in the cross-coupled LC oscillator of Figure 19.22 and the single-ended Colpitts oscillator of Figure 19.17 will be examined.

Stationary noise approximation. Figure 19.25 depicts the noise sources in the complementary differential LC oscillator. The noise power densities for these sources are required to calculate the phase noise. In a simplified stationary approach, the power densities of the noise sources can be evaluated at the most sensitive time (i.e. the zero-crossing of the differential tank voltage) to estimate the effect of these sources. Figure 19.26(a) shows a simplified model of the sources in this balanced case for the differential LC oscillator. Converting the current sources to their Thévenin equivalent and writing KVL,

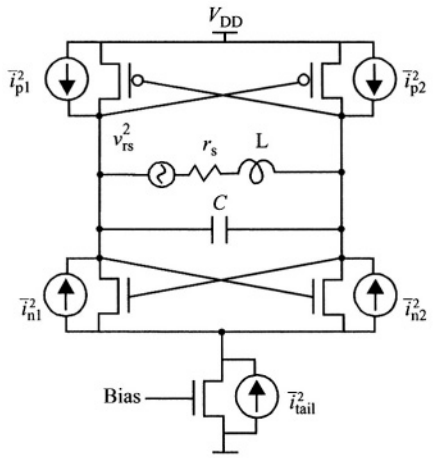


Figure 19.25. The noise sources in the differential CMOS LC oscillator.

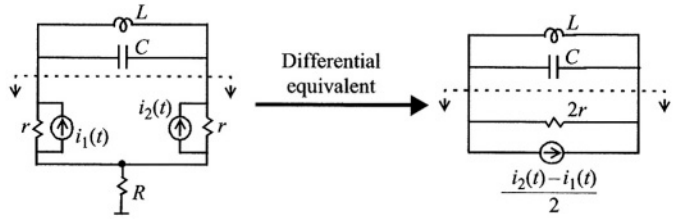


Figure 19.26. (a) Simplified model for transistor noise sources and (b) differential equivalent circuit.

one obtains the equivalent differential circuit shown in Figure 19.26(b). Note that the parallel resistance is canceled by the negative resistance provided by the positive feedback. Therefore, the total differential noise power due to the four cross-coupled transistors is

$$\overline{i_{cc}^2} = \frac{1}{4}\left(\overline{i_{n1}^2} + \overline{i_{n2}^2} + \overline{i_{p1}^2} + \overline{i_{p2}^2}\right) = \frac{1}{2}\left(\overline{i_n^2} + \overline{i_p^2}\right) \tag{19.27}$$

where $\overline{i_n^2} = \overline{i_{n1}^2} = \overline{i_{n2}^2}$ and $\overline{i_p^2} = \overline{i_{p1}^2} = \overline{i_{p2}^2}$. Noise densities $\overline{i_n^2}/\Delta f$ and $\overline{i_p^2}/\Delta f$ are given by [55]

$$\overline{i_n^2}/\Delta f = 4kT\gamma\mu C_{ox}\frac{W}{L}(V_{GS} - V_T) \tag{19.28}$$

where μ is the mobility of the carriers in the channel, C_{ox} is the oxide capacitance per unit area, W and L are the width and length of the MOS transistor,

respectively, V_{GS} is the dc gate-source voltage and V_T is the threshold voltage. Equation (19.28) is valid for both short and long-channel regimes of operation. However γ is around 2/3 for long-channel transistors while it may be between 2 and 3 in the short-channel region [56].

In addition to these sources, the contribution of the effective series resistance of the inductor, r_s, caused by ohmic losses in the metal and substrate is given by

$$\bar{i}_{rs}^2/\Delta f = 4kT\frac{r_s C}{L} = \frac{4kT}{R_p} \tag{19.29}$$

where $R_p \approx Q^2 r_s = (L\omega_0)^2/r_s$ is the equivalent parallel resistance at the frequency of oscillation.

Cyclostationary noise sources. To investigate the effect of cyclostationary noise source and see the effect of fast switching in the transistors, the single-ended Colpitts oscillator of Figure 19.17 was simulated for various channel mobilities, while keeping other parameters constant. The higher mobility results in larger transconductance and hence a faster switching time, without affecting the tank amplitude significantly. The amplitude remains constant as in the current-limited regime, the tail current and tank loss determinee the amplitude according to (19.25). The simulated NMF and the effective ISFs for various values of mobility are shown in Figure 19.27. The drain voltage and the oscillation frequency do not change significantly, as predicted by (19.25) and hence the ISF does not change.

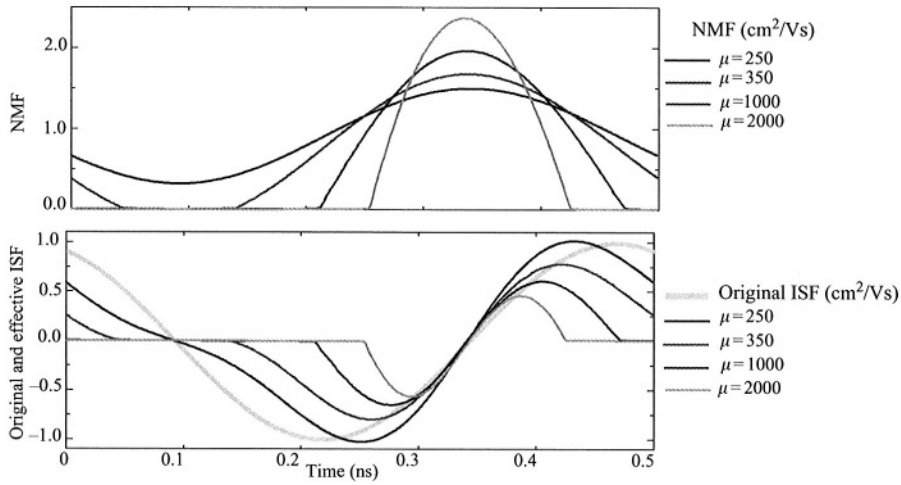


Figure 19.27. The simulated NMF and the effective ISF for the Colpitts oscillator.

Table 19.1. Phase noise improvement for different channel mobilities due to cyclostationary noise alignment.

μ (cm^2 V s)	*Phase noise improvement (dB)*
250	0.4
350	3.5
1000	6.7
2000	9.2

Note that the lobes of the effective ISF, $\Gamma_{\text{eff}}(x)$ become shorter and thinner for larger mobility (or equivalently for higher transconductance per current). The fast switching of the transistors is essential to achieve current pulses as sharp as possible, and hence transistors with lowest parasitic capacitance per maximum deliverable current are highly desirable. This will in turn result in a much lower channel noise contribution. The simulated phase noise improvements for the Colpitts oscillator of Figure 19.17, are summarized in Table 19.1. The improvements are measured in reference to the stationary noise source due to the same bias current. As can be seen, significant improvements in the phase noise can be achieved using devices with higher mobility. This suggests that a class C operation is desirable for the oscillator to achieve the best phase noise performance. Phase noise improvement for different channel mobilities due to cyclostationary noise alignment.

19.4.3. Design Implications

To gain more insight about the trade-offs involved, the complimentary differential LC VCO of Figure 19.22 was fabricated. The phase noise at 600 kHz offset is measured for different values of the tail current, as shown in Figure 19.28. As can be seen from this graph, increasing the tail current will improve the phase noise due to the increase in oscillation amplitude. Also, the improvement slows down as the tank voltage amplitude approaches the supply voltage. It can also be shown [39] that the phase noise has a weak dependence on the supply voltage, improving somewhat for lower voltages. This behavior may be attributed to smaller voltage drops across the channel on the MOS transistors which reduces the effect of velocity saturation in the short-channel regime and hence lowers γ.

The power dissipation increases as the operation point moves toward higher tail currents and supply voltage. If the design goal is to achieve the minimum phase noise without any concern for power dissipation, the oscillator should be operated at high supply voltage and high current to allow the maximum possible tank voltage amplitude. However, power usually is a concern, so a

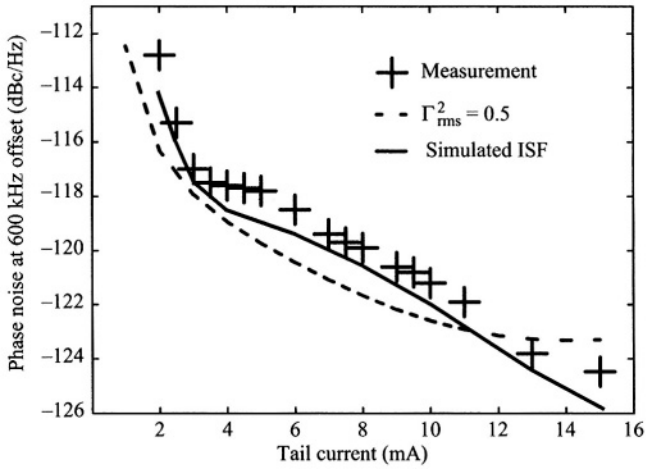


Figure 19.28. The phase noise at 600 kHz offset for different tail currents.

more practical goal maybe to achieve the best phase noise for a given power. Equation (19.11) suggests that it is desirable to operate at the largest tank amplitude for a given power dissipation. However, the tank amplitude cannot be increased beyond V_{DD} due to voltage limiting. Therefore, according to this simple model, it is desirable to operate at the edge of the voltage-limited mode of operation.

19.5. Phase Noise Trade-Offs for Ring Oscillators

Due to the ease of integration and large tuning range, ring oscillators have become an essential building block in many digital and communication systems. In this section, we will derive closed-form expressions for the rms and dc values of the ISF for ring oscillators. These approximate rms and dc values are used to obtain closed-form expressions for phase noise and jitter in ring oscillators. Finally, design trade-offs such as the question of single-ended vs differential implementation of ring oscillators and the optimum number of stages are addressed.

19.5.1. The Impulse Sensitivity Function for Ring Oscillators

To calculate phase noise and jitter using (19.11) and (19.12), one needs to know the dc and rms values of the ISF. In this subsection, approximate closed-form equations for the dc and rms values of the ISF of ring oscillators will be obtained.

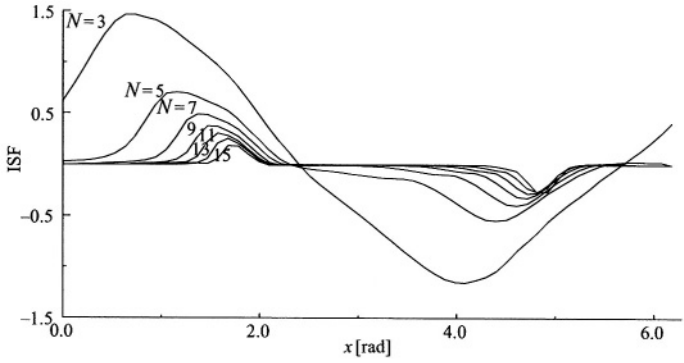


Figure 19.29. The ISF for ring oscillators of the same frequency with different number of stages.

It is instructive to look at the actual ISF of ring oscillators to gain insight into what constitutes a good approximation. Figure 19.29 shows the shape of the ISF for a group of single-ended CMOS ring oscillators. The frequency of oscillation is kept constant (through adjustment of channel length), while the number of stages is varied from 3 to 15 (in odd numbers). The ISF is calculated by injecting very short pulses of current and measuring the resultant phase shift.

As can be seen, increasing the number of stages reduces the peak value of the ISF. The reason is that the transitions of the normalized waveform become faster for larger N in this constant frequency scenario. Since the sensitivity is inversely proportional to the slope, the peak of the ISF drops. Also, the widths of the lobes of the ISF decrease as N becomes larger since each transition occupies a smaller fraction of the period. Based on these observations, the ISF of ring oscillators with equal rise and fall times can be approximated as two identical triangles, as shown in Figure 19.30.

The ISF has a maximum of $1/f'_{\max}$, where $f'_{\max}$ is the maximum slope of the normalized waveform f in (19.1) Also, the width of the triangles is approximately $2/f'_{\max}$ and hence the slopes of the sides of the triangles are ± 1. Therefore, assuming equality of the rise and fall times, $\Gamma_{\rm rms}$ can be estimated as

$$\Gamma_{\rm rms}^2 = \frac{1}{2\pi}\int_0^{2\pi} \Gamma^2(x)\,dx = \frac{4}{2\pi}\int_0^{1/f'_{\max}} x^2\,dx = \frac{2}{3\pi}\left(\frac{1}{f'_{\max}}\right)^3 \qquad (19.30)$$

On the other hand, stage delay is proportional to the rise-time:

$$\hat{t}_{\rm D} = \frac{\eta}{f'_{\max}} \qquad (19.31)$$

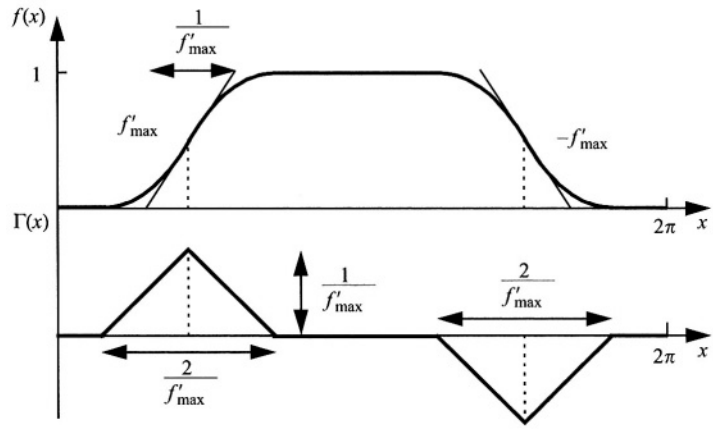


Figure 19.30. Approximate waveform and ISF for a ring oscillator.

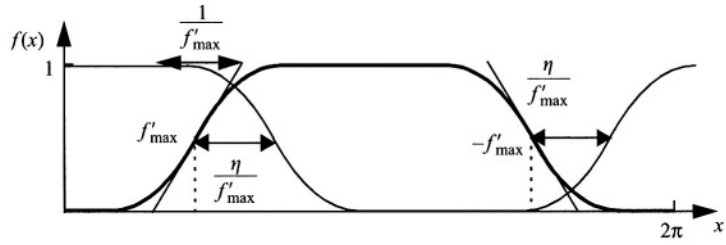


Figure 19.31. The relationship between rise time and delay.

where $\hat{t}_D$ is the stage delay normalized to the period and η is a proportionality constant, which is typically close to one, as can be seen in Figure 19.31.

The period is $2N$ times longer than a single stage delay, that is,

$$2\pi = 2N\hat{t}_D = \frac{2N\eta}{f'_{max}} \tag{19.32}$$

Using (19.30) and (19.32), the following approximate expression for Γ_{rms} is obtained:

$$\Gamma_{rms} \approx \sqrt{\frac{2\pi^2}{3\eta^3}} \cdot \frac{1}{N^{1.5}} \tag{19.33}$$

Note that the $1/N^{1.5}$ dependence of Γ_{rms} is independent of the value of η. Figure 19.32 illustrates Γ_{rms} vs the number of stages for the ISFs shown in

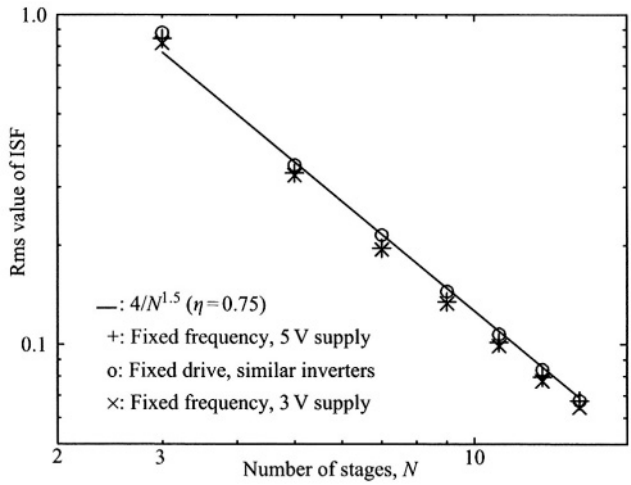


Figure 19.32. Rms values of the ISFs for various single-ended ring oscillators vs number of stages.

Figure 19.29 with plus signs on log–log axes. The solid line shows the line of $\Gamma_{\text{rms}} \approx 4/N^{1.5}$, which is obtained from (19.33) for $\eta = 0.75$. To verify the generality of (19.33), a second set of simulations was performed in which a fixed channel length is maintained for all the devices in the inverters while varying the number of stages to allow different frequencies of oscillation. Again $\Gamma(x)$ is directly simulated and its rms value is plotted in Figure 19.32 with circles. This simulation is repeated with a different supply voltage (3 V as opposed to 5 V) and the result is shown with crosses. As can be seen, the values of Γ_{rms} are almost identical for these three cases.

It should not be surprising that Γ_{rms} is primarily a function of N because the effect of variations in other parameters, such as $q_{\max}$ and device noise, have already been decoupled from $\Gamma(x)$; the ISF is a unitless, frequency and amplitude independent function.

Equation (19.33) is valid for differential ring oscillators as well, since in its derivation no assumption specific to single-ended oscillators was made. Figure 19.33 shows Γ_{rms} for three sets of differential ring oscillators, with a varying number of stages (4–16). The data shown with plus signs correspond to oscillators in which the total power dissipation and drain voltage swing are kept constant by scaling the tail current sources and load resistors as N changes. Members of the second set of oscillators have a fixed total power dissipation and fixed load resistors, which result in variable swings, and for whom data are shown with circles. The third case is that of a fixed tail current for each stage and constant load resistors, whose data are illustrated using crosses. Again,

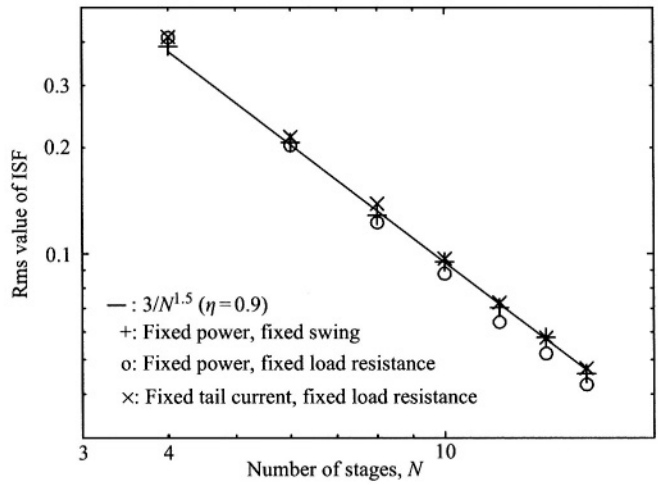


Figure 19.33. Rms values of the ISFs for various differential ring oscillators vs number of stages.

despite the diverse variations of frequency and other circuit parameters, the $1/N^{1.5}$ dependency of Γ_{rms} and its independence from other circuit parameters still holds. In the case of a differential ring oscillator, $\Gamma_{\text{rms}} \approx 3/N^{1.5}$, which corresponds to $\eta = 0.9$, is the best fit approximation for Γ_{rms}. This is shown with the solid line in Figure 19.33.

Although Γ_{rms} decreases as the number of stages increases, one should not conclude that the phase noise can be reduced using a larger number of stages, because the number of noise sources, as well as their magnitudes, also increases, for a given total power dissipation and frequency of oscillation. The question of optimal number of stages is, therefore, a bit involved, and will be addressed in the subsequent sections.

In the case of unequal rise and fall times, a similar approximation can be used to calculated the dc and rms value of the ISF and hence relating the $1/f^3$ phase noise corner to the device $1/f$ noise corner through [33]

$$f_{1/f^3} = f_{1/f} \cdot \frac{3}{2\eta N} \cdot \frac{(1-A)^2}{1-A+A^2} \tag{19.34}$$

where A represents the asymmetry of the waveform and is defined as

$$A \equiv \frac{f'_{\text{rise}}}{f'_{\text{fall}}} \tag{19.35}$$

where f'_{rise} and f'_{fall} are the maximum slope during the rising and falling edges, respectively.

In the case of asymmetric rising and falling edges, both Γ_{rms} and c_0 will change. The $1/f^3$ corner of the phase noise spectrum is inversely proportional to the number of stages. Therefore, the $1/f^3$ corner can be reduced either by making the transitions more symmetric in terms of rise and fall times or by increasing the number of stages. Although the former always helps, the latter has important implications on the phase noise in the $1/f^2$ region, as will be shown later.

19.5.2. Expressions for Phase Noise in Ring Oscillators

It is desirable to express phase noise and jitter in terms of design parameters such as power dissipation and frequency to be able to investigate the design trade-offs more readily. Throughout this subsection, we will focus on the white noise as it is assumed that the symmetry criteria for minimizing the up-conversion of $1/f$ noise are already met. For CMOS transistors, the drain current noise spectral density is given by (19.28), which is valid in both short and long-channel regimes, as long as an appropriate value for γ is used. The first case considered is a single-ended CMOS ring oscillator with equal-length NMOS and PMOS transistors. Assuming $V_{TN} = V_{TP}$, the maximum total channel noise from the NMOS and PMOS devices, when both the input and output are at $V_{DD}/2$, is given by

$$\frac{\overline{i_n^2}}{\Delta f} = \left(\frac{\overline{i_n^2}}{\Delta f}\right)_N + \left(\frac{\overline{i_n^2}}{\Delta f}\right)_P = 4kT\gamma\mu_{eff}C_{ox}\frac{W_{eff}}{L}\Delta V \tag{19.36}$$

where

$$W_{eff} = W_n + W_p \tag{19.37}$$

and

$$\mu_{eff} = \frac{\mu_n W_n + \mu_p W_p}{W_n + W_p} \tag{19.38}$$

and ΔV is the gate overdrive in the middle of the transition, that is, $\Delta V = V_{DD}/2 - V_T$.

During one period, each node is charged to q_{max} and then discharged to zero. In an N-stage single-ended ring oscillator, the power dissipation associated with this process is $Nq_{max}V_{DD}f_0$. However, during the transitions, some extra current, also known as crowbar current, is drawn from the supply. This current does not contribute to charging and discharging the capacitors since it goes directly from supply to ground through both transistors. These two components of the total current drawn from supply are shown in Figure 19.34. In a symmetric ring oscillator, these two components are comparable and their difference will

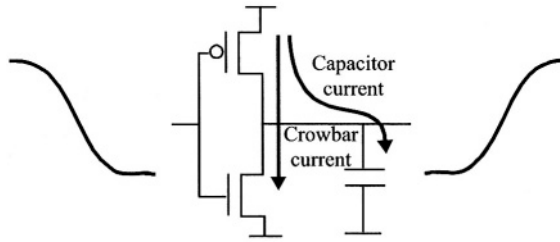


Figure 19.34. Capacitor and crowbar current in an inverter.

depend on the ratio of the rise-time to stage delay; therefore, the total power dissipation is approximately given by

$$P = 2\eta N V_{DD} q_{max} f_0 \tag{19.39}$$

Assuming $\mu_n W_n = \mu_p W_p$ to make the waveforms symmetric to first order, the frequency of oscillation for long-channel devices can be approximated by

$$f_0 = \frac{1}{2N t_D} = \frac{1}{\eta N (t_r + t_f)} \approx \frac{\mu_{eff} W_{eff} C_{ox} \Delta V^2}{8\eta N L q_{max}} \tag{19.40}$$

where t_D is the delay of each stage and t_r and t_f are the rise and fall-time associated with the maximum slope during a transition.

Assuming that the thermal noise sources of the different devices are uncorrelated, and assuming that the waveform (and hence the ISF) of all the nodes are the same except for a phase shift, the total phase noise due to all N noise sources is N times the value given by (19.11). Taking only these inevitable noise sources into account, (19.11), (19.33), (19.36), (19.39) and (19.40) result in the following expression for phase noise:

$$\mathcal{L}\{\Delta\omega\} \approx \frac{8}{3\eta} \cdot \frac{kT}{P} \cdot \frac{V_{DD}}{V_{char}} \cdot \frac{\omega_0^2}{\Delta\omega^2} \tag{19.41}$$

where V_{char} is the *characteristic voltage* of the device. For long-channel devices, $V_{char} = \Delta V/\gamma = (V_{gs} - V_T)/\gamma$. Any extra disturbance, such as substrate and supply noise, or noise contributed by extra circuitry or asymmetry in the waveform, will result in a larger number than (19.41). As can be seen, the phase noise is inversely proportional to the power dissipation and grows quadratically with the oscillation frequency. Further, note the lack of dependence on the number of stages (for a given power dissipation and oscillation frequency). Evidently, the increase in the number of noise sources (and in the maximum power due to the higher transition currents required to run at the same frequency) essentially cancels the effect of decreasing Γ_{rms}

as N increases, leading to no net dependence of phase noise on N. Also in using (19.41), one should verify the validity of the assumptions leading to this expression. To calculate the phase noise of an arbitrary oscillator, (19.11) should be used.

A similar calculation for the short-channel case can be carried out. For such devices, phase noise will be still given by (19.41), except for a new V_{char}:

$$V_{\text{char}} = \frac{E_c L}{\gamma} \tag{19.42}$$

which results in a larger phase noise than the long-channel case by a factor of $\gamma \Delta V / E_c L$. As before, note the lack of dependence on the number of stages in the case of short-channel devices.

Now consider a differential MOS ring oscillator with resistive load. The total power dissipation is

$$P = N I_{\text{tail}} V_{\text{DD}} \tag{19.43}$$

where N is the number of stages, I_{tail} is the tail bias current of the differential pair, and V_{DD} is the supply voltage. The frequency of oscillation can be approximated by

$$f_0 = \frac{1}{2N t_{\text{D}}} \approx \frac{1}{2\eta N t_{\text{r}}} \approx \frac{I_{\text{tail}}}{2\eta N q_{\max}} \tag{19.44}$$

The noise of the tail current source in the vicinity of f_0 does not affect the phase noise. Rather, its low frequency noise as well as its noise in the vicinity of *even* multiples of the oscillation frequency affect the phase noise [33,39]. Tail noise in the vicinity of even harmonics can be significantly reduced by a variety of means, such as with a series inductor or a parallel capacitor. As before, the effect of low frequency noise can be minimized by exploiting symmetry. Therefore, only the noise of the differential transistors and the load is taken into account, as shown in Figure 19.35. The total current noise on each single-ended node is given by

$$\frac{\overline{i_{\text{n}}^2}}{\Delta f} = \left(\frac{\overline{i_{\text{n}}^2}}{\Delta f}\right)_{\text{N}} + \left(\frac{\overline{i_{\text{n}}^2}}{\Delta f}\right)_{\text{load}} = 4kT I_{\text{tail}} \left(\frac{1}{V_{\text{char}}} + \frac{1}{R_{\text{L}} I_{\text{tail}}}\right) \tag{19.45}$$

where R_{L} is the load resistor, $V_{\text{char}} = (V_{\text{GS}} - V_{\text{T}})/\gamma$ for a balanced stage in the long-channel limit and $V_{\text{char}} = E_c L/\gamma$ in the short-channel regime. Assuming zero correlation among the various noise sources, the phase noise due to all $2N$ noise sources is $2N$ times the value given by (19.11). Using (19.33), the expression for the phase noise of the differential MOS ring oscillator is

$$\mathcal{L}_{\min}\{\Delta\omega\} \approx \frac{8}{3\eta} \cdot N \cdot \frac{kT}{P} \cdot \left(\frac{V_{\text{DD}}}{V_{\text{char}}} + \frac{V_{\text{DD}}}{R_{\text{L}} I_{\text{tail}}}\right) \cdot \frac{\omega_0^2}{\Delta\omega^2} \tag{19.46}$$

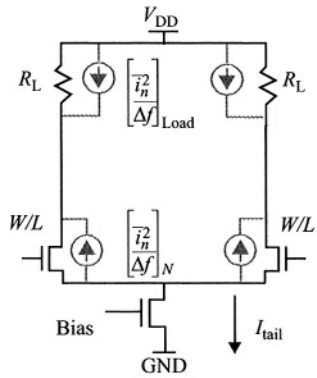


Figure 19.35. The noise sources in the differential buffer stage.

The foregoing equations are valid in both long and short-channel regimes of operation with the right choice of V_{char}.

Note that in contrast with the single-ended ring oscillator, a differential oscillator does exhibit a phase noise and jitter dependency on the number of stages, with the phase noise degrading as the number of stages increases for a given frequency and power dissipation. This result may be understood as a consequence of the necessary reduction in charge swing that is required to accommodate a constant frequency of oscillation at a fixed power level as N increases. At the same time, increasing the number of stages at a fixed total power dissipation demands a proportional reduction of tail current sources, which will reduce the swing, and hence q_{max}, by a factor of $1/N^2$.

19.5.3. Substrate and Supply Noise

Noise sources on different nodes of an oscillator may be strongly correlated. This correlation can be due to various reasons. Two examples of sources with strong correlation are substrate and supply noise. These noise sources usually arise from current switching in other parts of the chip. The current fluctuations induce voltage fluctuations across the series resistance and inductance of the bondwires and pins. These fluctuations on the supply and substrate will induce a similar perturbation on different stages of the ring oscillator.

To understand the effect of this correlation, consider the special case of having identical noise sources on all the nodes of the ring oscillator as shown in Figure 19.36. If all the inverters in the oscillator are the same, the ISF for different nodes will differ only in phase by multiples of $2\pi/N$, as shown in Figure 19.37 for $N = 5$. Therefore, the total phase due to all the sources is

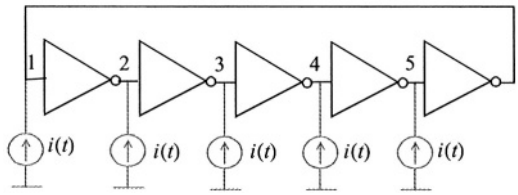


Figure 19.36. Five-stage ring oscillator with identical noise sources on all nodes.

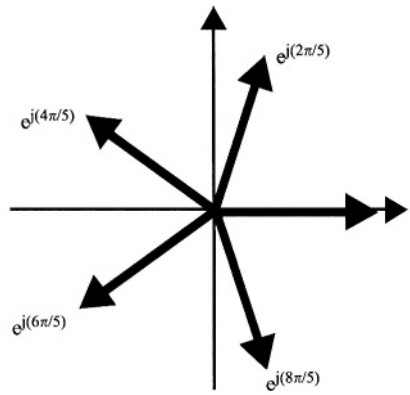


Figure 19.37. Phasors for noise contributions from each source.

determined by superposition, that is,

$$\phi(t) = \frac{1}{q_{\max}} \sum_{n=0}^{N-1} \int_{-\infty}^{t} i(\tau)\Gamma\left(\omega_0\tau + \frac{2\pi n}{N}\right) d\tau$$

$$= \frac{1}{q_{\max}} \int_{-\infty}^{t} i(\tau)\left[\sum_{n=0}^{N-1} \Gamma\left(\omega_0\tau + \frac{2\pi n}{N}\right)\right] d\tau \qquad (19.47)$$

Expanding the term in brackets in a Fourier series, it can be observed that it is zero except at dc and multiples of $N\omega_0$, that is,

$$\phi(t) = \frac{N}{q_{\max}} \sum_{n=0}^{\infty} c_{(nN)} \int_{-\infty}^{t} i(\tau)\cos(nN\omega_0\tau)\, d\tau \qquad (19.48)$$

which means that for fully correlated sources, only noise in the vicinity of integer multiples of $N\omega_0$ affects the phase.

19.5.4. Design Trade-Offs in Ring Oscillators

A commonly asked question is the preferred topology for MOS ring oscillators, that is, which one of the single-ended or the differential topologies results in better jitter and phase noise performance for a given center frequency, f_0, and total power dissipation, P.

Equations (19.41) and (19.46) can be used to compare the phase noise performance of single-ended and differential MOS ring oscillators in the thermal noise limited case. As can be seen for N stages, the phase noise of a properly designed differential ring oscillator is approximately $N[1 + V_{\text{char}}/(R_{\text{L}} I_{\text{tail}})]$ times larger than the phase noise of a single-ended oscillator of equal N, P and f_0. Since the minimum N for a regular ring oscillator is three, even a properly designed differential CMOS ring oscillator underperforms its single-ended counterpart, with disparity increasing with the large number of stages. This difference is even more pronounced if proper precautions to reduce the noise of the tail current are not taken.

The difference in the behavior of these two types of oscillators with respect to the number of stages can be traced to the way they dissipate power. The dc current drawn from the supply is independent of the number and slope of the transitions in differential ring oscillators. On the contrary, inverter-chain ring oscillators dissipate power mainly on a *per transition* basis and, therefore, have a better phase noise for a given power dissipation. This difference becomes even larger as the number of stages increases. However, a differential topology may still be preferred in ICs with a large amount of digital circuitry because of the lower sensitivity to substrate and supply noise, as well as lower noise injection into other circuits on the same chip. The decision of which architecture to use should be based on both of these considerations.

Another commonly debated question concerns the optimum number of inverter stages in a ring oscillator to achieve the best jitter and phase noise for a given f_0 and P. As seen in (19.41), for single-ended oscillators, the phase noise and jitter in $1/f^2$ region are not strong functions of the number of stages for single-ended CMOS ring oscillators. However, if the symmetry criteria are not well satisfied, and/or the process has large $1/f$ noise, (19.34) predicts that a larger N will reduce the phase noise. In general, the choice of the number of stages must be made on the basis of several design criteria, such as $1/f$ noise effect, the desired maximum frequency of oscillation, and the influence of external noise sources, such as supply and substrate noise, that may not scale with N.

The phase noise behavior is different for differential ring oscillators. As (19.46) suggests, phase noise increases with an increasing number of stages. Hence, if the $1/f$ noise corner is not large, and/or proper symmetry measures have been taken, the minimum number of stages (3 or 4) should be used to give the best performance. This recommendation holds even if the power dissipation

is not a primary issue. It is not fair to argue that burning more power in a larger number of stages allows the achievement of better phase noise, since dissipating the same total power in a smaller number of stages with larger devices results in better phase noise, as long as it is possible to maximize the total charge swing.

Substrate and supply noise are among other important sources of noise and can be dominant in large digital environments. There are two major differences between these noise sources and internal device noise. First, the power spectral density of these sources is usually non-white and often demonstrates strong peaks at various frequencies [57]. Even more important is that the substrate and supply noise on different nodes of the ring oscillator have a very strong correlation.

A very important insight can be obtained from (19.48). It shows that for the correlated part of the noise, only the c_n values associated with integer multiples of number of stages, *N,* contribute to total phase fluctuations. Therefore, every effort should be made to *maximize* the correlated part of substrate and supply noise. This can be done by making the inverter stages and the noise sources on each node as similar to each other as possible by proper layout and circuit design.

The layout should be kept symmetrical. The inverter stages should be laid out close to each other so that substrate noise appears as a common-mode source. This consideration is particularly important in the case of a lightly doped substrate, since such a substrate may not act as a single node. It is also important that the orientation of all the stages be kept identical. The interconnecting wires between the stages must be identical in length and shape.

The circuit should be designed so that the same supply line goes to all the inverter stages. Also the loading from the stages being driven should be kept identical for all the nodes, for example, by using dummy buffer stages on all the nodes. A larger number of stages will also be helpful because a smaller number of c_n coefficients will affect the phase noise. Finally, the low-frequency portion of the substrate and supply noise plays an important role in the jitter and phase noise. Fortunately, the effect of low-frequency noise can be reduced by exploiting symmetry to minimize c_0.

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Chapter 20

SYSTEMATIC DESIGN OF HIGH-PERFORMANCE DATA CONVERTERS

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20.1. Introduction

In the present day, the design of heterogeneous microelectronic systems on one chip is becoming feasible due to the ever decreasing feature size of the silicon technology. These systems implement functions that require both digital blocks (DSPs, microprocessors, reconfigurable digital blocks), memories (RAM/ROM) as well as analog macrocells (D/A and A/D converters, drivers, front-end, etc.). The use of cores and other intellectual property (IP) blocks as well as new methodologies such as platform-based design promise the design productivity boost that is needed to generate these systems in the shortening time to market constraints. The design of analog functional blocks, however, requires a large amount of effort compared to digital or DSP systems, especially when large and complex blocks as for instance high-accuracy converters are considered.

To tackle this problem, a number of approaches have been proposed. Analog synthesis tools promise an automated solution for the design of analog building blocks [1]. These tools use a top-down, constraint-driven design methodology to refine system-level block specifications into a fully completed transistor-level design. The application range of most analog synthesis tools today, however, is limited to usually one or a few types of circuits [2–5], and only few approaches cover the complete design flow from specification down to layout. Nevertheless, full automation of the design of analog macrocells is only useful for those types of blocks that show a high level of topological reuse. Examples are Delta–Sigma converters, pipelined converters, etc. For the more high-performance designs with ever changing topological variations by definition no automation can be provided. Nonetheless a tool-supported systematic design methodology may also drastically reduce the design time for these cutting-edge designs as will be illustrated in this chapter for one particular class of analog macrocells.

A systematic design methodology is proposed and demonstrated for the efficient design of high-accuracy current-steering D/A converters. The design

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methodology covers the complete design flow and is supported by software tools to speed up the task significantly. A generic behavioral model is used to explore the D/A converter's specifications during high-level system design and exploration. The inputs to the design methodology are the specifications of the D/A converter and the technology process. The result is a generated layout and the corresponding extracted behavioral model that allows the inclusion of the converter in system simulations for final verification. The systematic design method allows one to speed up the generation of new designs for given specifications, or to easily port designs to new technology processes. Using this approach, the design time was experimentally reduced from 11 weeks to less than one month. The presented approach, although not fully automated, offers as much flexibility of the topology used, for instance towards the switching scheme: from simple row–column decoding (8–10 bits) to complex switching schemes like the quad-quadrant random-walk switching scheme (14 bits), in this way covering a broad range of performance requirements.

The chapter is organized as follows. Section 20.2 explains the proposed systematic design methodology. In Section 20.3, the architecture of the D/A converter and its parameters are described. Section 20.4 presents the developed behavioral model for system-level design. The sizing synthesis is explained to full extent in Section 20.5. Section 20.6 describes the layout generation process with the Mondriaan tool, and Section 20.7 presents the extracted behavioral model. Finally Section 20.8 presents the experimental results and measurements of three implemented designs. Section 20.9 then provides conclusions.

20.2. Systematic Design Flow for D/A Converters

In the design of analog functional blocks as part of a large system on silicon (SoC), a number of different phases are identified as depicted in Figure 20.1. The first phase in the design is the specification phase. During this phase the analog functional block is analyzed in relation to its environment, the surrounding system, to determine the system-level architecture and the block's required specifications. With the advent of analog hardware description languages such as VHDL-AMS or VERILOG-A/MS, the obvious implementation for this phase is a generic analog behavioral model. This model has to be parameterized with respect to the specifications of the functional block.

The next phase in the design procedure is the actual design (synthesis) of the functional block (see center of Figure 20.1), consisting of sizing and layout. The design methodology used here is top-down performance-driven [6]. This design methodology has been accepted as the de facto standard for systematically designing analog building blocks [1]. The analog design flow is grouped on the left in the center of Figure 20.1; the corresponding digital flow is grouped on

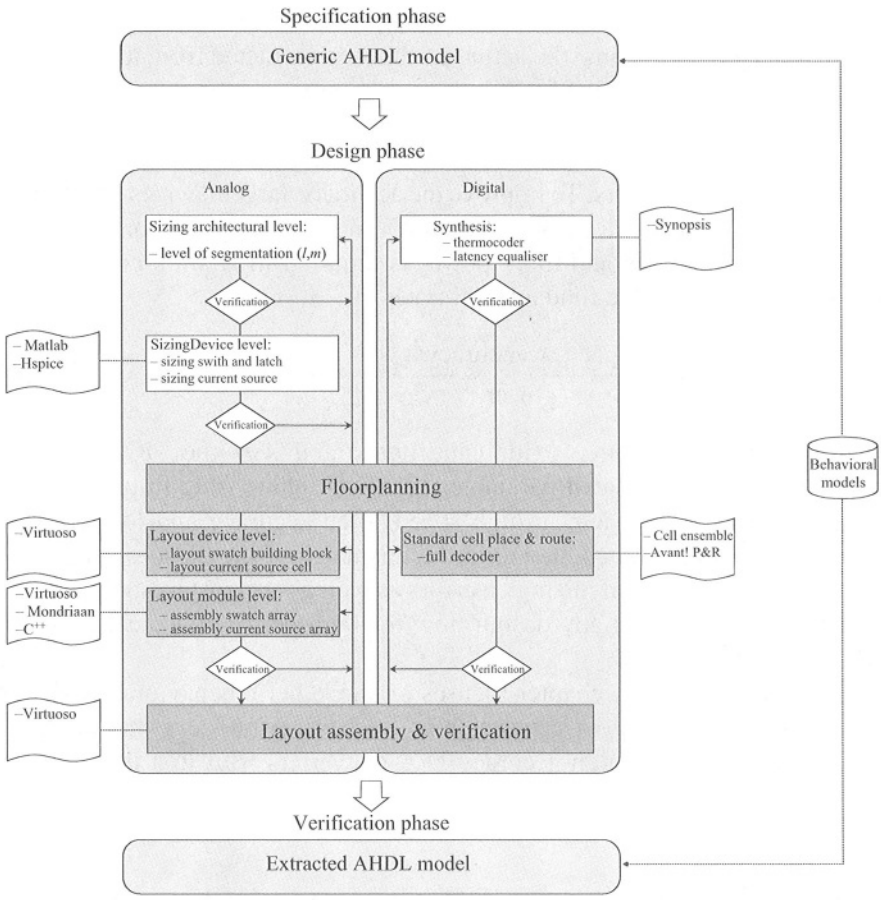


Figure 20.1. Presented systematic design flow for a current-steering D/A converter.

the right. The analog flow consists of a sizing at two levels: the architectural level and the device level. The digital synthesis completes the sizing part of the mixed-signal design. The design steps are verified using classical approaches (numerical verification with a simulator, at the behavioral, device and gate level respectively). The floorplanning is done jointly for analog and digital blocks, after which the analog layout is generated and standard cell place and route is used to create the digital layout. Both layouts are separately verified. The blocks are assembled at the module level and again a module-level verification is done with classical tools.

When the full converter design is finished and verified in the final verification phase, the complete system in which the functional block is applied, must be verified in the final verification phase, as shown at the bottom in Figure 20.1. For

this again a behavioral model for the analog functional block (D/A converter) is constructed, but this time the actual parameters extracted from the generated layout are used to verify the functioning of the block within the system.

The performance of Nyquist-rate converters is restricted by the trade-off between speed, power and accuracy [7]. The accuracy is limited by the mismatch between transistors. To improve the accuracy, larger devices are required that have better matching, but at the same time the capacitive loading on the circuit nodes increases and more power is required to attain a certain speed performance. Hence, the fundamental trade-off:

$$\frac{\text{speed} \times \text{accuracy}^2}{\text{power}} \approx \frac{1}{C_{ox} \cdot A_{VT}^2} \tag{20.1}$$

where C_{ox} is the unit-area oxide capacitance and A_{VT} the MOS transistor threshold voltage mismatch parameter [8]. This relationship implies that for today's circuits, which aim at high speed, high accuracy and low power, a technological limit is encountered in the mismatch of the devices. Therefore, the handling of statistical mismatch errors as well as any systematic errors that limit accuracy is key in any design flow for high-performance converters as will be illustrated below.

The remainder of the chapter focuses on the generic behavioral modeling, the sizing synthesis, layout generation and behavioral model extraction steps in the design flow for high-accuracy D/A converters. But first the proposed D/A converter architecture and its important design parameters are described briefly.

20.3. Current-Steering D/A Converter Architecture

For high-speed, high-accuracy D/A converters, a segmented current-steering topology is usually chosen, as it is intrinsically faster and more linear than other architectures [9,10]. The conceptual block diagram of this type of D/A converter is depicted in Figure 20.2: the l least significant bits are implemented in a binary way while the m most significant bits steer a unary current source array.

The general specification list for a current-steering D/A converter is given in Table 20.1. The specifications can be divided into four categories: *static, dynamic, environmental* and *optimization* specifications. In the case of a D/A converter the *static* parameters include resolution (i.e. number of bits), integral non-linearity (INL), differential non-linearity (DNL) and yield. The *dynamic* parameters include settling time, glitch energy, spurious-free dynamic range (SFDR) and sampling frequency. The *environmental* parameters include the power supply, the digital levels, the output load and the input/output range. The power consumption and area are the optimization targets and need to be

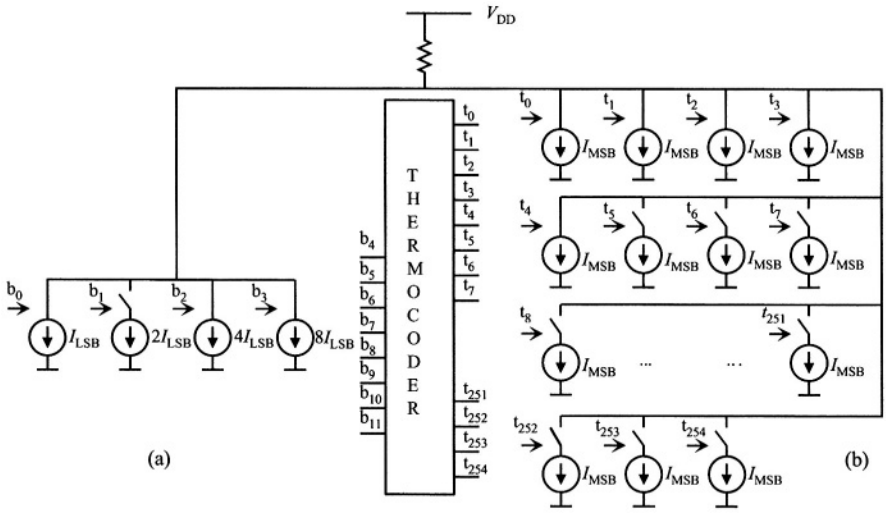


Figure 20.2. Principle block diagram of a 12-bit segmented current-steering D/A converter. The l (=4) least significant bits steer the binary-weighted current sources directly. The m (=8) most significant bits are fed into the thermometer decoder (thermocoder), which steers the unary current-source array. (a) Binary-weighted current cells and (b) unary current cells.

minimized for a given technology. This specification list serves as input for the design process as will be explained in the following sections.

The conceptual block diagram of Figure 20.2 is implemented by the proposed segmented architecture shown in Figure 20.3. The *current source* is implemented either by a cascoded ($\mathbf{M_{casc}}$, $\mathbf{M_{cur_src}}$) or non-cascoded MOS transistor ($\mathbf{M_{cur_src}}$). The current generated by the current sources is switched to one of the two differential output nodes by switch transistors $\mathbf{M_{sw_a}}$ and $\mathbf{M_{sw_b}}$. These are steered by a latch to control the synchronization of the switching. The *full decoder* comprises the thermometer encoder (thermocoder), that generates the steering signals for the unary latches out of the digital input word, and a latency equalizer block. This latency equalizer block ensures correct timing for the steering signals of the binary latches. One of the important architectural choices is how many bits are implemented using binary weighted current sources and how many using unary weighted sources.

The basic floorplan of the proposed architecture is also shown in Figure 20.3. The switches and latch are implemented as one unit cell, and placed in an array, referred to as the *swatch array* in the middle of Figure 20.3. The current source transistors and optional cascode transistors are also placed in an array, the *current-source array* at the bottom. The full decoder block is at the top. The three large modules (full decoder, swatch array and current-source array) are connected by signal busses. A *clock driver* completes the D/A converter.

Table 20.1. Specification list for a current-steering D/A converter with typical values, and measured values of designs 1–3 to be presented later on.

Specification	*Unit*	*Value*	*Design*		
			1	2	3
Static					
Number of bits (n)	—	14	12	14	14
INL	LSB	0.5	0.5	2.5	0.3
DNL	LSB	0.5	<1	0.5	0.2
Parametric yield	%	99.9	NM	NM	NM
Dynamic					
Glitch energy	pV s	1.0	0.8	0.3	NM
Settling time (10–90%)	ns	10	NM	1	0.9
SFDR at 500 kHz	dB	80	69	NM	84
Sample frequency	MHz	100	200	200	150
Environmental					
Output range (V_{swing})	V	0.5	0.5	0.5	0.5
R_{Load}	Ω	25	25	25	25
Digital levels	—	CMOS	CMOS	CMOS	CMOS
Power supply	V	2.7	2.7	2.7	2.7
Technology	—	0.5μm 1P3M	0.5μm 1P3M	0.5μm 1P3M	0.5μm 1P3M
Optimization					
Power	mW	Min. (300)	140	300	300
Area	mm^2	Min. (10)	3.5 × 4	3.5 × 3.5	3.2 × 4.1

NM = not measured.

The last important architectural design parameter of a current-steering D/A converter is the switching scheme. The switching scheme has two components. A unary current source consists of one or more parallel units spread out over the current-source array, as shown in Figure 20.4. By splitting the unary current sources the spatial errors due to any systematic gradients are averaged out, which is necessary for high-accuracy applications. The second parameter of the switching scheme is the switching sequence. In [11,12], it is shown that the remaining spatial errors are not accumulating when the current sources are switched on in an optimal way. The approach proposed here is quite general in that the switching scheme is fully flexible and can be programmed when generating the layout, to optimally compensate for systematic errors that would otherwise deteriorate the targeted linearity. The designable parameters of the proposed architecture are summarized in Table 20.2.

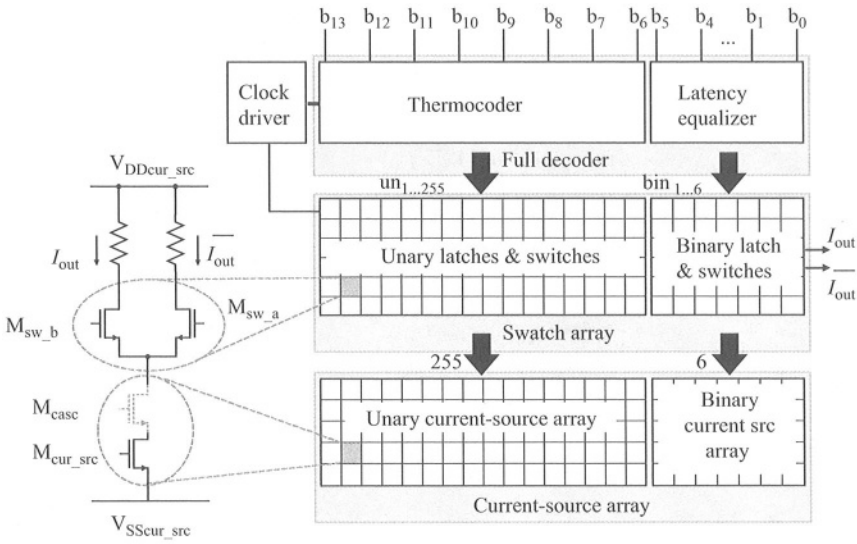


Figure 20.3. Block diagram and floorplan of the proposed segmented CMOS current-steering D/A converter architecture.

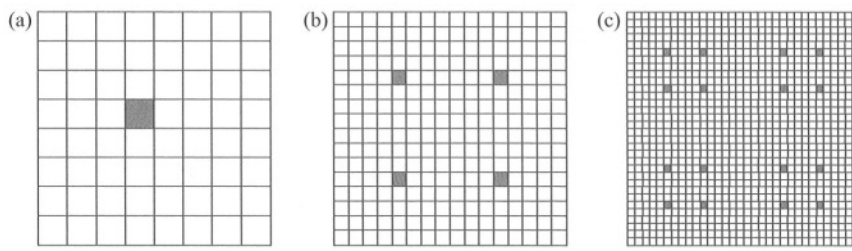


Figure 20.4. Three different switching schemes: (a) unary current source implemented as one unit; (b) unary current source implemented as four units in parallel; (c) unary current source implemented as 16 units in parallel.

20.4. Generic Behavioral Modeling for the Top-Down Phase

By using a complete mixed-signal hardware description language model of the system's block, the designer can explore different solutions on the system level in terms of performance, power and area consumption. In this way, the high-level specifications of the system can be translated into specifications for the D/A converter, as well as for the other blocks in the system.

Table 20.2. The designable parameters of the proposed D/A converter architecture.

Architectural level
l (number of LSBs)
m (number of MSBs)
Module level
1/4/16 units for unary current source
Switching sequence
Circuit level
$W_{\text{Mcur_src}}$, $L_{\text{Mcur_src}}$, $(V_{\text{gs}} - V_{\text{t}})_{\text{Mcur_src}}$
Insert M_{casc} or not?
W_{Mcasc}, L_{Mcasc}, $(V_{\text{gs}} - V_{\text{t}})_{\text{Mcasc}}$
W_{Msw}, L_{Msw}
Latch transistor sizes
Clock driver

The generic behavioral model of the D/A converter [13] is divided in a digital thermocoder (which performs the translation from binary to thermometer code) implemented in VHDL, and an analog core that incorporates the latches and switches and the current-source arrays and which was implemented in SpectreHDL. The generic model for the glitch energy and settling time (transient simulation) is presented next.

For the dynamic (transient) behavior of the D/A converter, two key specifications are taken into account: settling time t_{s} and glitch energy E_{gl}. The settling time is mainly determined by the capacitance on the output node C_{out} and can be modeled as such in the behavioral model. The glitch on the other hand is not only dependent on the number of current sources switched when going from level_i to level_j, but also on the choice of the number of bits l that steer the binary-weighted current-source array.

A generic model of the glitch can be obtained by superposition of an exponentially damped sine and a shifted hyperbolic tangent [13] (see Figure 20.5):

$$i_{\text{out}} = A_{\text{gl}} \sin\left(\frac{2\pi}{t_{\text{gl}}}(t - t_0)\right) \exp\left(-\text{sign}(t - t_0)\frac{2\pi}{t_{\text{gl}}}(t - t_0)\right) + \frac{\text{level}_{i+1} - \text{level}_i}{2} \tanh\left(\frac{2\pi}{t_{\text{gl}}}(t - t_0)\right) + \frac{\text{level}_{i+1} + \text{level}_i}{2} \quad (20.2)$$

in which i_{out} is the output current, A_{gl} is the amplitude and t_{gl} the period of the glitch signal, and level_i and level_{i+1} are the code levels between which the converter switches. The glitch energy is defined as the integrated area indicated

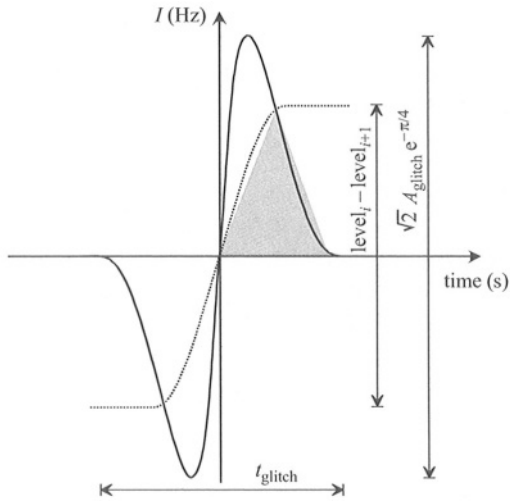


Figure 20.5. Calculation of the amplitude of the damped sine A_{gl} in terms of the glitch energy E_{gl}.

in gray in Figure 20.5. Using (20.2) this area can be approximated by:

$$\frac{E_{gl}}{2R_{load}}\mathrm{nr}_{switched} = \left[A_{gl}\sin\left(\frac{2\pi}{5}\right)\exp\left(-\frac{2\pi}{5}\right) + \frac{1}{2}\frac{\mathrm{level}_{i+1} - \mathrm{level}_i}{2} \times \left(\tanh\left(\frac{2\pi}{5}\right) - 1\right)\right]\frac{t_{gl}}{4} \tag{20.3}$$

where $\mathrm{nr}_{switched}$ is the number of current sources switched when going from level_i to level_{i+1}, R_{load} is the resistive load applied to the converter and E_{gl} is the glitch energy.

Using this generic model the required specifications for the D/A converter can be derived by performing simulations at the system level.

20.5. Sizing Synthesis of the D/A Converter

The specifications that have been derived during the top-down specification phase are now input to the sizing synthesis of the converter itself. The design of the converter is performed hierarchically, as indicated in Figure 20.1. First some decisions at the architectural level have to be taken. Next the sizing of the transistors at the device level has to be performed.

20.5.1. Architectural-Level Synthesis

The two architectural-level parameters (l, m) are determined during architectural-level sizing synthesis. Two important performance criteria, as listed in Table 20.1, are taken into account: static and dynamic performance.

Static performance. The *static behavior* of a D/A converter is specified in terms of INL and DNL. A distinction has to be made between *random errors* and *systematic errors.* The random errors are solely determined by mismatches. The systematic errors are caused by process, temperature and electrical gradients. In optimally designed D/A converters the INL and DNL should be limited by random errors (i.e. mismatch) only. A small safety margin (10% of INL) is reserved to allow for systematic contributions. The systematic errors are layout determined and are thus minimized during layout generation by optimizing the switching scheme and switching sequence. This optimization is explained in Section 20.6. Here, we explain how the random error is kept under control.

The maximum acceptable random error can be calculated from yield simulations [14]. Figure 20.6 depicts the yield simulation (using a Matlab program) for a 14-bit D/A converter: to achieve a targeted yield of 99.9% (INL < 0.5 LSB), the relative standard deviation of current matching for the unit current cell (1 LSB) has to be smaller than 0.1%.

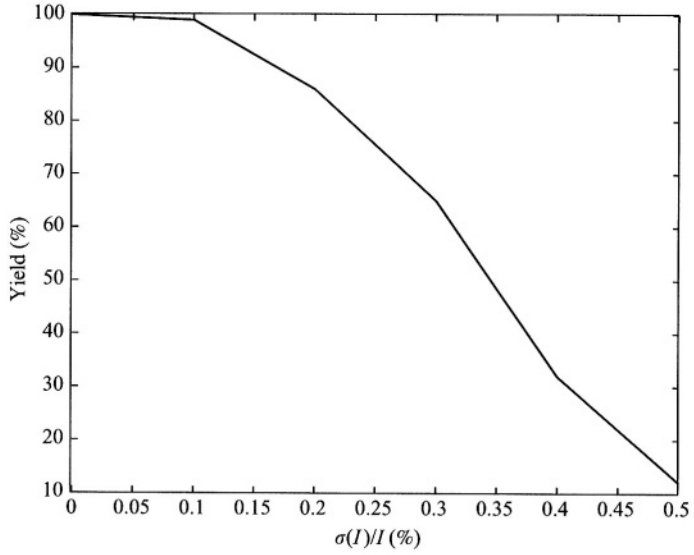


Figure 20.6. Yield as a function of the unit current source, current variance for a 14-bit D/A converter (INL < 0.5 LSB).

From the full swing (V_{swing}), the number of bits (n) and the load resistance (R_{load}), the current of one LSB (I_{LSB}) is calculated as:

$$I_{\text{LSB}} = \frac{V_{\text{swing}}}{R_{\text{load}} 2^n} \tag{20.4}$$

Then, an estimate for the active area of the current-source transistor can be calculated based on the mismatch model [8,14]:

$$W * L = \frac{1}{2\sigma^2(I)/I^2} \left[A_\beta^2 + \frac{4A_{\text{VT}}^2}{(V_{\text{GS}} - V_{\text{T}})^2} \right] \tag{20.5}$$

where $\sigma(I)/I$ is the unit current source standard deviation and A_β, A_{VT} are technology constants. For minimal area the $V_{\text{gs}} - V_{\text{t}}$ is maximized. The lower bound for the area is given by

$$(W * L)_{\text{lowerbound}} \approx \frac{1}{2\sigma^2(I)/I^2} A_\beta^2 \tag{20.6}$$

The total current source array area ($\text{area}_{\text{cur_src,est}}$) can then be estimated:

$$\text{area}_{\text{cur_src,est}} \approx 2^n (W * L)_{\text{lowerbound}} f_{\text{routing}} \tag{20.7}$$

where f_{routing} is the routing overhead factor. The static performance places a strict minimum on the area of the current source array.

Dynamic performance. The *dynamic behavior* of a D/A converter is usually specified in terms of admissible *glitch energy*. This specification is mainly determined by (1) the number of bits implemented in a unary/binary way, and (2) the way the current sources are synchronized when switched on/off. The largest glitch will occur when switching off all binary implemented bits and switching on the first unary current source. This implies that the decision on the number of bits l to be implemented in a binary way and the number of bits m to be implemented in a unary way determines the worst-case glitch.

The lowest possible glitch energy is obtained when a full unary implementation is chosen [15]. This would, however, result in a large area increase because of the complex binary-to-thermometer encoder. The total chip area ($\text{area}_{\text{total_est,est}}$) is estimated as

$$\begin{aligned} \text{area}_{\text{total,est}} &= \text{area}_{\text{cur_src,est}} + \text{area}_{\text{swatch,est}} \\ &\quad + \text{area}_{\text{decoder,est}}(l, m) + \text{area}_{\text{routing,est}}(l, m) \end{aligned} \tag{20.8}$$

The area of the current source array is fixed by equation (20.7) as is the area of the swatch array ($\text{area}_{\text{swatch,est}}$). However, the area of the thermocoder increases

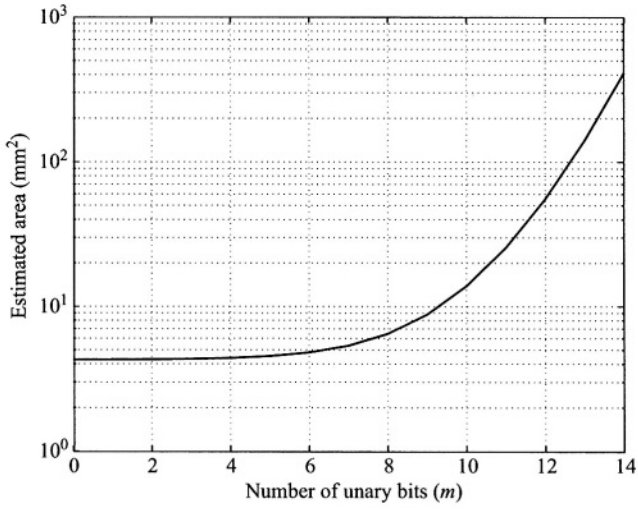


Figure 20.7. Estimated area of the D/A converter as a function of the number of unary bits (m).

($\sim 2^m$), as does the size of the routing busses connecting the three modules, if the number of unary bits (m) is increased. Figure 20.7 shows that in today's technologies an optimal number of unary implemented bits is around 8 for 14 bits of resolution, otherwise the area grows unacceptably large. This choice will ultimately limit the dynamic performance of the D/A converter.

20.5.2. Circuit-Level Synthesis

The circuit-level synthesis determines the circuit-level design parameters (see Table 20.2). Again, the two performance constraints – static and dynamic – are taken into account.

Static performance. The active area of the unit current-source array has been calculated from mismatch constraints (see equation (20.5)). A high biasing voltage ($V_{gs} - V_t$) is preferred for mismatch reasons. The upper limit for the biasing voltage is determined by the output swing (switching transistors $\mathbf{M_{sw}}$ need to be in the saturation region) and by the power supply. From equations (20.4) and (20.5), W_{cur_src} and L_{cur_src} can be calculated for some choice of $V_{gs} - V_t$.

A second source of non-linearity is the finite output impedance of the current source. The output impedance of the D/A converter is given by [9]

$$R_{total} = R_{load} \parallel \frac{R_{cur_src}}{code}, \quad code: 0 \rightarrow 2^n - 1 \tag{20.9}$$

where R_{load} is the external load, R_{cur_src} is the output impedance of the current source, and code is the number of sources switched to the output. This impedance varies with the code. This non-linearity causes deterioration of the INL. The cascode transistor M_{casc} is inserted if the output impedance is too low.

These calculations, which result in the sizing of the current-source transistors (M_{cur_src} and M_{casc}), have been implemented in a Matlab script. For a 14-bit converter this script gives a $W/L = 1.1\,\mu m/104.5\,\mu m$ in a standard $0.5\,\mu m$ CMOS technology.

Dynamic performance. In order not to deteriorate the dynamic performance, the following factors are taken into account in the circuit-level synthesis [16]: (1) synchronize the control signals of the switching transistors, (2) reduce the voltage fluctuation in the drains of the current sources during switching, (3) carefully switch the current-source transistor on/off. The synchronization of the control signals is achieved by adding a latch immediately in front of the switching transistors M_{sw} (see Figure 20.3). The voltage fluctuation at the drain changes the current from the current source because of the finite output impedance of the current source transistor M_{cur_src}. The problem can be solved by using a large channel length for the current-source transistor, and tuning the crossing point of the switching control signals such that both switches are never switched off simultaneously [17].

Using a device-level simulator (HSPICE) within an optimization loop, the latch and the switches are sized automatically, taking the crossing point and speed as constraints in the optimization process.

20.5.3. Full Decoder Synthesis

As the architectural parameters (l, m) and the latch transistor sizes are now known, the digital thermometer decoder can be synthesized. The remaining l LSBs are delayed by the equalizer block to have the same overall delay. The full decoder is synthesized from a VHDL description using a logic synthesis tool.

20.5.4. Clock Driver Synthesis

The clock driver generates the clock signals for the full decoder and swatch array. Both blocks have been sized above and thus their capacitive clock input load is known. Two inverter chains (scaled exponentially) are designed to drive this load including the wiring capacitance.

20.6. Layout Synthesis of the D/A Converter

Current-steering D/A converters are a typical example of layout-driven analog design. The sized schematic alone does not constitute an operational

converter. An important part of the performance is determined by the handling of layout-induced parasitics and error components (i.e. systematic errors). All classical countermeasures for digital to analog coupling (guard rings, shielding, separate supplies, etc.) and standard matching guidelines (equal orientation, dummies, etc.) have been applied and will not be discussed further. We will concentrate here on the extra required layout measures and the Mondriaan layout tool, specially developed for such regular layout structures.

20.6.1. Floorplanning

The floorplan proposed in Figure 20.3 is now refined. First of all, the global aspect ratio constrains the aspect ratio of the blocks. In general, a square or near-square chip layout is preferred. Secondly, at the chip level the connections between the blocks are extremely important: a fixed pitch must be chosen to route the busses across the different modules. Otherwise large area loss in the routing of the different busses is inevitable (e.g. the need for river routing).

20.6.2. Circuit and Module Layout Generation

The layouts of the current-source array and swatch array are generated next.

Current-source array layout generation. The sizes of the unit current source have been determined. From this the sizes of all other weighted current sources and the unary current source are derived. For optimal matching the current source must be built up from identical basic units. This basic unit is laid out manually. It contains a current source and optionally a cascode transistor.

How these units are connected and where they are placed are the last designable parameters of the design (see Table 20.2). The splitting of the unary current source as shown in Figure 20.4 is required for 12-bit or 14-bit linearity. At least 4 units are required for 12-bit linearity [18] and 16 units for 14-bit [11] in the technology used.

The switching sequence is then optimized, using a branch and bound search algorithm, to reduce the accumulation of remaining systematic errors. The result is shown in Figure 20.8. On the left, a manually derived switching sequence has been simulated which was sufficient for the 12-bit converter in [17]. With the same spatial errors but an optimal (smallest INL) switching scheme [11], the remaining systematic errors do not accumulate anymore, resulting in an INL of 0.2 LSB instead of 2.1 LSB. The search algorithm has been implemented using the C programming language.

The placement of the basic units in the array is now known. The current source array is then generated automatically with Mondriaan [19]. The Mondriaan tool is a dedicated analog layout synthesis tool targeted to the automated layout generation of highly regular array-type analog modules. It takes

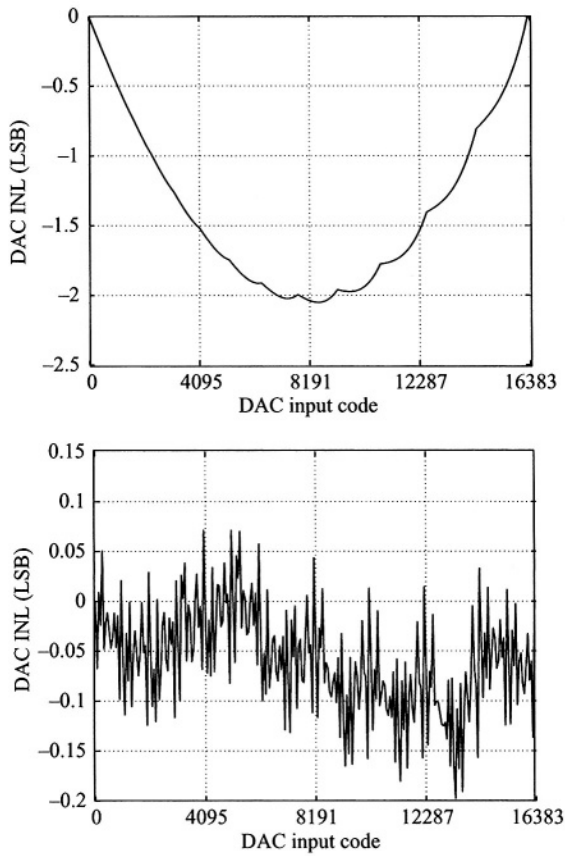


Figure 20.8. Prediction of the INL of a 14-bit D/A converter obtained with two different switching sequences. Above a manually derived (suboptimal) switching sequence; Below the computer-generated optimized switching sequence. The same error profile (extracted from a test chip) has been applied in both cases.

the complex switching scheme as input, and performs a floorplanning, symbolic routing and technology mapping to generate the physical layout of the current-source array.

Swatch array layout generation. The basic swatch cell has been laid out manually. The placement and routing of the swatch array is then done automatically with the Mondriaan tool [19] as well. Inputs to the tool are the pin list of the current-source array, the netlist and the swatch cell.

Full decoder standard cell place and route. Finally, the layout of the digital full decoder is generated using a digital standard cell place and

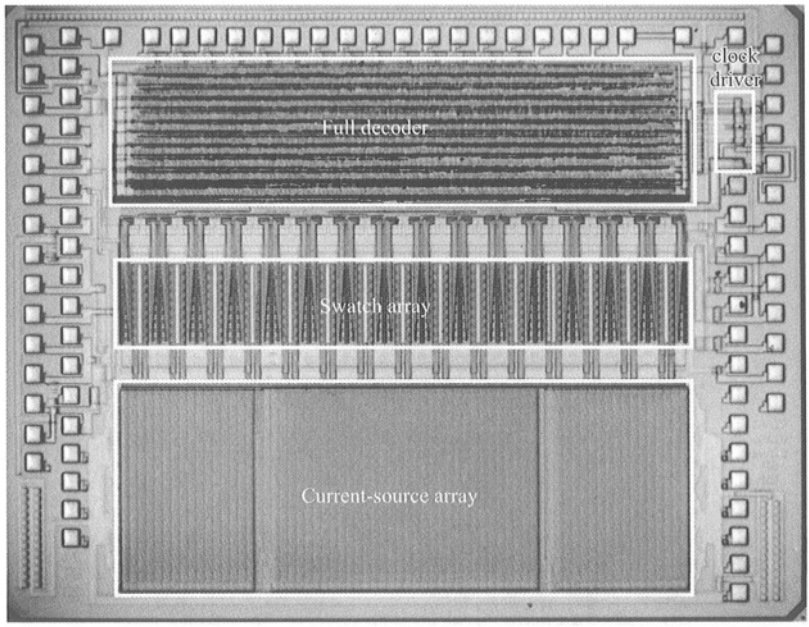


Figure 20.9. Layout of a 14-bit segmented current-steering D/A converter (design 2).

route tool. The pin list obtained from the swatch array layout is input to the floorplanning phase of the layout generation. The cells are then placed and routed.

20.6.3. Converter Layout Assembly

The modules are then stacked on top of each other. The bus generators of the Mondriaan tool [19] are used to generate the connections between the three modules (full decoder, swatch array and current source array). Trees are used to collect the output signals and distribute the clocking signal from the clock driver to the swatch array to have equal delay.

The bonding pads are placed and manually connected to all the external pins of the D/A converter. For a particular 14-bit D/A converter design described later on (design 2), this results in the layout shown on the microphotograph in Figure 20.9.

20.7. Extracted Behavioral Model for Bottom-Up Verification

After the layout is completed, a behavioral model is generated in which the model parameters are extracted from the designed circuit. The resulting model

is used for final system verification of systems in which the D/A converter is used as embedded functional block.

The glitch model as presented in Section 20.4 was extended to reflect better the actual design. First, a separate damped sine was used for switching on ($A_{gl,on}$ & $t_{gl,on}$) or off ($A_{gl,off}$ & $t_{gl,off}$) a current source (see equation (20.2)). The number of current sources that are switched on or off can readily be computed from the chosen topology (i.e. the choice of the number of bits l that steer the binary-weighted current-source array). Switching on or off current sources is thus modeled separately and then combined at the output node.

Secondly, the amplitude and the time constant of the damped sine of the left-hand side and the right-hand side (see Figure 20.5) are controlled separately ($A_{gl,left}$ & $t_{gl,left}$ and $A_{gl,right}$ & $t_{gl,right}$). This results in eight parameters for the final model, that can easily be extracted from SPICE-type circuit simulations by switching one bit on and off. The comparison between a circuit-level HSPICE simulation and the response of the extracted behavioral model for the same digital input is depicted in Figure 20.10. The extracted model has an accuracy better than 99%, or an error less than 1%. The HSPICE simulation required 4:37 min of CPU time on a HP 712/100 whereas the behavioral model only took 12s.

This concludes the complete design process of the D/A converter as an embedded functional block in larger systems. The methodology has been applied to three different converters, that have all been fabricated and measured, as will be explained next.

20.8. Experimental Results

Three designs were generated using the proposed design methodology. The measurement results on the fabricated chips are listed in the last three columns of Table 20.1. First a 12-bit D/A converter with a 200 M samples/s update rate was implemented [17]. While developing this chip, the layout tool Mondriaan [19] still lacked functionality resulting in large routing overhead, which explains the larger chip area, compared to the second and third design that are 14-bit versions. Secondly, a 14-bit D/A converter with a 200 M samples/s update rate was implemented. The chip has an INL of 2.5 LSB and a very low glitch of 0.3 pVs. Finally, a second 14-bit D/A converter was implemented [11]. The update rate of this converter is 150 M samples/s. The chip has an INL of 0.3 LSB and a DNL of 0.2 LSB. This proves that the approach of using an optimized switching scheme is absolutely needed for 14-bit accuracy. In Figure 20.11, the spectrum at the output of this converter is shown for a full-scale input signal at 5 MHz. A SFDR of 61 dB is obtained for this third design.

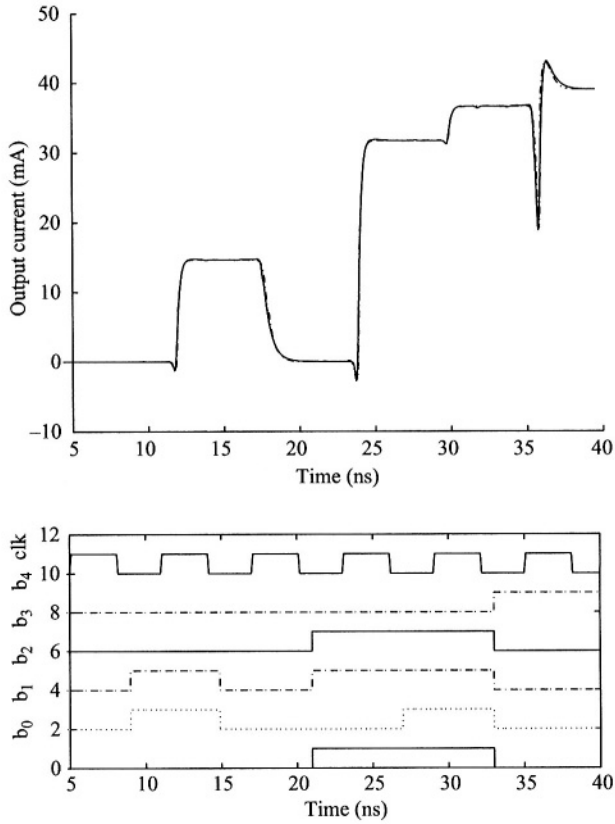


Figure 20.10. Comparison between the extracted behavioral model (- - -) and the numerical device-level HSPICE simulation (—) of the time response of a current-steering D/A converter.

The time spent on the different steps in the proposed design methodology have been summarized in Table 20.3. During the course of the first design the different design trade-offs were explored and encoded afterwards in the presented Matlab scripts. Using these scripts for the second and the third design, the design time could be reduced from 4 weeks down to 1 week. The layout time was reduced considerably using the Mondriaan tool [19]. The layout of the swatch array was done manually for the first design, as the layout tool Mondriaan was still under development at that time. Two weeks were needed to draw the swatch cell and array manually. In the second design, the swatch cell was laid out manually in 1 week, the generation of the swatch array itself took only a few hours for exploring different iterations with the Mondriaan tool. For the third design, the basic cells were modified, and the arrays were generated with Mondriaan. Although the switching scheme was completely different, the

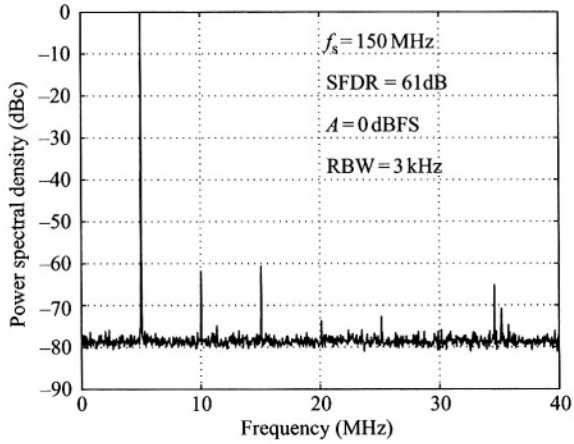


Figure 20.11. Output spectrum measurement of design 3. The applied signal frequency is approximately 5 MHz at full scale.

Table 20.3. Time spent on design, layout and verification of the three designs, indicating the realized productivity gain.

	Design 1	*Design 2*	*Design 3*
Sizing & Synthesis			
High level	2 weeks	1 week	1 day
Current source	1 week	1 hour	—
Swatch array	1 week	2 days	—
Thermocoder	1 day	1 day	1 day
Layout			
Floorplan	2 days	1 hour	1 hour
Current source	3 days	1 day	1 hour
Swatch array	2 weeks	1 week	7 hours
Thermocoder	4 days	4 days	4 days
Assembly	3 days	3 days	3 days
Verification			
Sizing	1 week	1 week	1 week
Layout	1 week	1 week	1 week
Total person effort	11 weeks	7 weeks	4 weeks

layout generation took only 8 h (current source and swatch array). The layout assembly of the different blocks was done manually for all designs. DRC and LVS checking were done to verify the generated layout. Parasitics were extracted and the sizing was verified using HSPICE. All these verifications

required 2 weeks in all three designs – a time that we did not succeed to cut down. As shown in Table 20.3, the overall design time was reduced from 11 weeks to 4 weeks of total person effort. This is a reduction by a factor of 2.75 ×, experimentally indicating the boost in productivity in the design of analog macrocells obtained by means of the presented design methodology.

20.9. Conclusions

A systematic design methodology for high-speed high-accuracy D/A converters has been demonstrated. The methodology covers the complete design flow starting from the specification phase of the converter as macrocell in a larger system down to a fully synthesized and laid out implementation followed by a verification of the entire system with a behavioral model extracted from the actual designed converter. The well established performance-driven top-down design methodology is used to synthesize the D/A converter. Both commercially available and newly developed software tools (such as the Mondriaan layout tool for analog circuits with regular array-type layout patterns) support this methodology. The correctness and effectiveness of the methodology has been proven by the fabrication and measurement of three high-speed high-accuracy D/A converters. During the designs, the methodology was refined and supporting tools were developed, which finally resulted in a design productivity improvement by a factor of 2.75 ×.

Acknowledgments

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Chapter 21

ANALOG POWER MODELING FOR DATA CONVERTERS AND FILTERS

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21.1. Introduction

The design of future mixed-signal systems on a chip (SoC) is a difficult task. The systems are becoming more and more complex, with ever increasing performance requirements, and at the same time the available design time is shrinking due to tightening time-to-market constraints. Often the specifications have to be cutting-edge and this at a minimal power consumption and/or chip area for the total system. Therefore, the choice of the system-level architecture and the definition of the building block specifications are typically performed by one or a group of very experienced system designers. Even then, the new design is usually based on an existing design to which at most minimal modifications have been introduced. Yet, this conservative approach may not result in the best overall solution for new emerging applications.

Therefore, research is being conducted to construct CAD tools that help system designers in this architectural decision process by formalizing and speeding up system architectural exploration and design while minimizing a given cost function such as power consumption [1]. Using simulations different architectural alternatives can easily be analyzed and compared without fully having to design them first. A good example of a typical problem is shown in Figure 21.1. A digital telecom application has to transmit bits correctly over the channel (ether, telephone line, cable . . .). Given the requirements for the system in terms of specifications like the bit error rate (BER), the following decisions have to be taken as to the system architectural solution:

- what is the optimum transmitter and receiver architecture (a kind of high-level block diagram) for the given application ?
- what are the optimum specifications for each of the subblocks within the selected architecture (e.g. the number of bits and sampling rate of the A/D converter, etc.) ?
- related questions such as the optimal analog–digital partitioning, frequency planning, etc.

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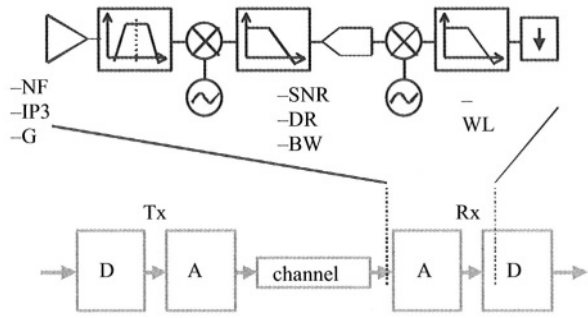


Figure 21.1. System-level architectural design for digital telecom applications: determine the most appropriate transmitter and receiver architecture.

Such system exploration and trade-off analysis cases can only be checked rapidly, without going to an actual design. If an architectural exploration environment exists that contains an efficient high-level simulation method, accurate high-level performance models as well as high-level power estimators for all the building blocks involved (both analog and digital) [1].

In digital microelectronics complete tools like for instance PowerMill exist that estimate the power needed to perform a digital function. In analog microelectronics, efforts to construct power estimators are found to be more sporadic up till now. This chapter addresses this problem, proposes methods for analog power estimation and applies them to two different classes of analog circuits.

The chapter is organized as follows. Section 21.2 introduces different methodologies that can be used for developing analog power estimators. Section 21.3 describes a power estimator for high-speed ADCs, while Section 21.4 presents a power estimator for analog continuous-time filters. Finally, Section 21.5 provides conclusions.

21.2. Approaches for Analog Power Estimators

A power estimator is a function that returns an estimated value for the power consumed by a functional block when given only some relevant input specifications, including the target technology, without knowing the detailed implementation of the block:

$$\text{Power}_{\text{ESTIMATED}} = f(\text{high-level specifications}) \tag{21.1}$$

For power estimators to be useful for high-level system design, the following requirements must hold:

- The estimators may have as input parameters only high-level block parameters that correspond to the typical performance specifications of that

block. For an A/D converter, this could be for instance the required resolution and sampling rate.

- The accuracy of the estimated value with respect to the exact, finally measured power consumption of an implementation of the block does not have to be 100% exact, but it is acceptable if it is in the right ballpark. An exact value is only needed when a chosen architecture is examined in greater detail. It is clear that the more information is used about the final implementation, the more accurate the power estimates should be. On the other hand, the trend of the estimator function when the performance requirements are varied has to be accurate to allow correct trade-offs between different architectural candidates, which is the goal of high-level architecture exploration. For instance, if two bits are added to the resolution of the A/D converter, then the increase of power should be predicted correctly.

Basically, two methods are available for developing analog building block power estimators: the bottom-up method and the top-down method:

- In the *bottom-up* method, a certain topology is selected and from this exactly known schematic equations are derived. In this way the behavior of the analog block is modeled in more detail. The advantage is that the models and estimators are more exact, and therefore, are more accurate with respect to real designs. The most obvious disadvantage of this approach is that first a topology has to be chosen, which is not the situation we have in architectural exploration where we don't know the final implementation of the blocks yet when designing the system at the architectural level.
- The *top-down method* is much more suited for real system-level design. First of all, no assumptions are made regarding the topology of the building block leaving all solutions open. Secondly, the obtained power models are in general simpler and therefore better for implementation in fast system exploration tools. The drawback, however, is that the accuracy of the models is often difficult to achieve due to the large range of possible circuit implementations with consequently widely varying power consumptions. Therefore, it is more difficult to obtain general, topology-independent power models. The use of fitting parameters fitted to real designs typically compensates this shortcoming to some extent. But generality will always have its price.

In practice, there will often be some combination of these methods, and the amount of circuit implementation detail that will be needed to reach acceptable accuracy may be different from one type of analog circuits to another.

The proper strategy to develop power estimation models is therefore to try a generic topology-independent approach first, but if this has insufficient accuracy then to exploit somewhat more information about the implementation, restricting the model to only that type of implementation. In the remainder of this chapter, two examples of power estimation methods are described for high-speed Nyquist-rate ADCs and continuous-time analog g_m-C filters, respectively, which are two key blocks in many mixed-signal applications.

21.3. A Power Estimation Model for High-Speed Nyquist-Rate ADCs

The proposed solution for a power estimation function for high-speed Nyquist-rate CMOS ADC's is a top-down approach with fitting parameters. The model is quite generic as it covers almost the full range of high-speed Nyquist-rate ADCs (independent of the actual implementation: flash, folding/interpolating or pipelined), and it is also scalable with respect to technology.

The input parameters of the power estimator are the most important specification parameters for an A/D converter, that is, the sample rate (clock) and the accuracy (effective number of bits (ENOB) at a given input frequency). Subsection 21.3.1 derives the power model. Subsection 21.3.2 then presents experimental results.

21.3.1. The Power Estimator Derivation

The power is proportional to the supply voltage times the charge that is being drained at the frequency of operation:

$$P = V_{dd} \cdot I = V_{dd} \cdot f \cdot \text{Charge} \tag{21.2}$$

This is quite trivial but the question is what frequency should be considered when talking about ADCs and then which charge is being drained. A high-speed ADC always has two parts: comparators and (pre) processing circuitry (the digital decoding logic is considered to behave as the comparators). The comparator is clocked at F_{sample} (and reset every clock cycle) and the processing circuit varies at the frequency of the input signal. In pipelined ADCs also the Sample & Hold and the DAC are clocked at F_{sample} but the charges internally vary with the signal frequency amplitude. So it is better to split equation (21.2) up in two parts as well:

$$P = P_{\text{comparators@F}_{sample}} + P_{\text{processing circuit@F}_{signal}} \tag{21.3}$$

The charge is stored on internal capacitances, hence for each part of the ADC the following is valid:

$$P = V_{dd} \cdot \text{freq} \cdot (\text{Voltage swing}) \cdot C \tag{21.4}$$

The voltage swing for the comparators is always the full supply voltage (digital values). For the rest of the circuitry the swing depends on the signal swing, but if it is a good design, it will be as large as possible and therefore approximately also V_{dd} can be taken. This results in an expression of the following form for both parts of (21.3):

$$P = V_{dd}^2 \cdot C \cdot \text{freq} \tag{21.5}$$

Little can be said about the capacitances without going into topology details, which has to be avoided to have a good top-down estimator. Therefore, the equality is replaced by proportionality and the capacitance is taken proportional to the technology's minimal transistor channel length, which yields the following equation for the total power estimator:

$$P \propto V_{dd}^2 \cdot L_{min} \cdot (F_{sample} + F_{signal}) \tag{21.6}$$

So far, the accuracy parameter has not been included yet, but it is clear that accuracy is inversely related to the size of the transistors (due to mismatch and noise) and hence also to the internal circuit capacitances. Using larger devices results in a higher accuracy, but also increases the total capacitance, thus limiting the speed and increasing the power consumption. The accuracy is expressed here as the effective number of bits (ENOB) which is given by the well known [2] equation:

$$\text{ENOB} = \frac{20 \cdot \log(\text{SNDR}) - 1.76}{6.02} \tag{21.7}$$

The accuracy (21.7) is related to the size of the devices and in this way to the power (21.6). This correlation has been extracted from fitting to real converter power data. To this end, 75 data points have been collected from almost all CMOS ADCs published in the *IEEE Journal of Solid State Circuits* from December 1994 up till recently as well as in the proceedings of the ISSCC conferences from 1996 to 1998. This gives a total of 23 designs. In most publications, a measured graph showing the ENOB as a function of F_{signal} is included. For every design several points of these curves were taken in order to incorporate the frequency-dependent behavior of ENOB increasing the total number of data points to 75.

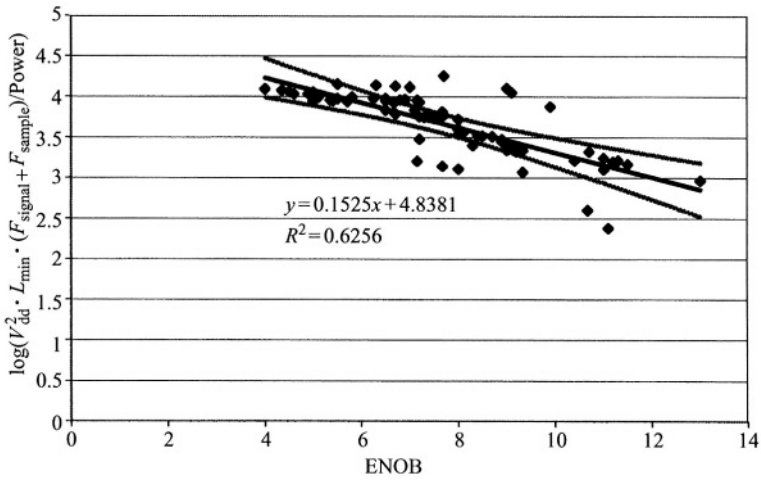


Figure 21.2. Fit results between power, accuracy (ENOB) and clock and signal frequencies: the linear regression line and its 90% confidence band.

These 75 data points are shown in Figure 21.2 and the fitting has resulted in the following regression relation [3]:

$$\log\left(\frac{V_{dd}^2 \cdot L_{min} \cdot (F_{sample} + F_{signal})}{Power}\right) = -0.1525 \cdot ENOB + 4.8381 \quad (21.8)$$

The correlation coefficient r for this linear regression approximation is also given in Figure 21.2 and is 0.791. The mean square error equals 0.2405 and a 90% confidence band for the regression line is drawn. From this regression fit the final power estimator valid for the complete class of CMOS Nyquist-rate high-speed ADCs can be derived as:

$$P = \frac{V_{dd}^2 \cdot L_{min} \cdot (F_{sample} + F_{signal})}{10^{(-0.1525 \cdot ENOB + 4.838)}} \quad (21.9)$$

This estimator combines the simplicity of the top-down approach with the flexibility of the bottom-up approach. It is indeed a continuous technology-scalable (V_{dd} and L_{min}) function, it is valid for many different ADC topologies and it can easily be extended towards other (or new) designs by adding the corresponding data and deriving a new fit. In addition, having a closed analytical function allows easy integration in a system-level design tool and makes it well suited for system exploration [4].

21.3.2. Results of the Power Estimator

In Figure 21.3 the power estimated with the model derived above (equation (21.9)) is compared to the published power. The relative power difference values are plotted in ascending order. It can be seen that 85% of all the data points (i.e. samples 6 up to 71) fall within a factor of 2.2×. A factor 2.2× corresponds to about 1.44 times the standard deviation calculated from the linear regression analysis. This result is accurate enough for a first-order system-level design where the power can be represented as a nominal (estimated) value with a certain margin around this value.

A second way to demonstrate the accuracy of the estimator is to take a design that was not used to derive the estimation function and to check the result. A design that expresses the ENOB as a function of F_{sample} and F_{signal} was found in [5]. The estimated power consumption is calculated with (21.9) to be 166 mW and the published power consumption is 225 mW. The relative power error equals (166 – 225)/225 = –0.26 which is about a factor 1.35 (well below the uncertainty margin of 2.2). Another design of a flash ADC that was overlooked when deriving the estimator is found in [6]. Now the estimated power consumption is 331 mW and the published amount is 307 mW. Now the error is only a factor 1.08×. These results demonstrate the feasibility and reliability of the estimator. The estimator was also tested in industry and resulted in power predictions with an error less than a factor 1.71× for 10 out of 11 industrial designs considered.

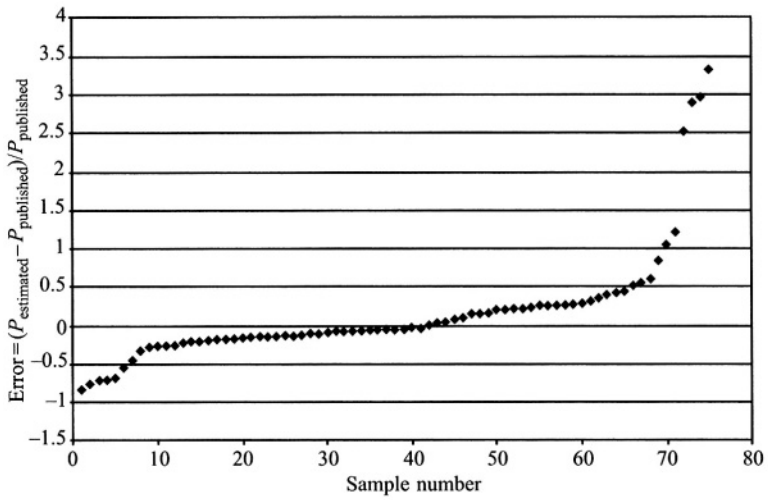


Figure 21.3. The relative error between the estimated power value and the real reported power value in ascending order for the considered 75 data points.

21.4. A Power Estimation Model for Analog Continuous-Time Filters

This section focuses on the construction of a power estimator for analog continuous-time filters that can be used in an architectural system design exploration tool. Initially, some attempts were performed to generate a generic estimator valid for all types of filter implementations, only using information such as the desired type of filter function and the order of the filter. These attempts were based on theoretical formulas similar to those found in literature [7,8] which were then fitted to real data. An example is the following equation:

$$P = \eta kT Q f_c \left(\frac{S^2}{N}\right) \tag{21.10}$$

where Q is the desired quality factor of the filter, f_c the cut-off frequency, S the signal power, N the maximum allowed noise power, and η the fit parameter. Such formulas however only provided power estimates that were off with up to three orders of magnitudes for a wide range of filters [9].

Therefore, an alternative approach had to be adopted [10] that exploits additional information about the filter implementation such as the filter topology and the type of the filter, still however without going to the other extreme of selecting a full device-level implementation. This explains why this power model is restricted to one class of filter implementations. Basically, three main active filter realizations exist: the multiple-loop feedback realization, the ladder simulation realization and the cascaded biquad realization [11]. In ACTIF the cascade realization is implemented (although the other implementations will be added later on), and for the biquads transconductance-C (OTA-C or g_m-C) stages are used. This choice for continuous-time OTA-C filters is motivated by the fact that these high-frequency analog filters are frequently used blocks in many applications, including telecommunications, to filter out undesired signals. Typical examples are anti-alias filters, preconditioning filters in hard disk drives, image reject filters in telecom frontends, etc . . . The frequency range covered by these filters ranges from tens to a few hundred megahertz.

Most steps of the derived power estimator are programmed in Matlab but user interaction is still required to use them together. The combination of these steps forms an actual tool that in the future can be expanded to cover most filter types. The tool has been named ACTIF after the analog continuous-time filters that are being covered. The next sections will now describe the approach in detail and will present experimental results.

21.4.1. The ACTIF Approach

Analog continuous-time filters estimates the power consumed by an analog continuous-time OTA-C filter when given as input only a limited set of

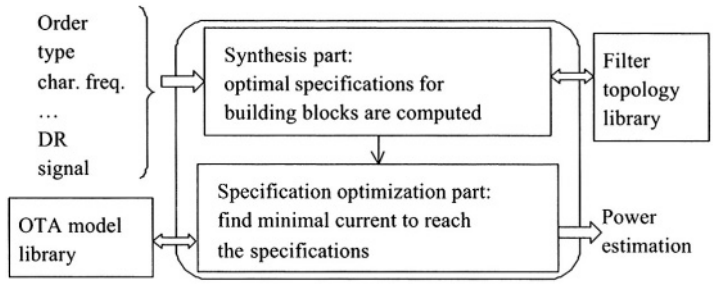


Figure 21.4. Overview of the ACTIF flow for power estimation of continuous-time g_m-C filters.

high-level system parameters besides the process technology: the filter transfer function, the desired dynamic range (DR) and the maximal (differential) signal amplitude. The output is the estimated power consumption needed to realize the given transfer function in the specified technology. The ACTIF tool is divided in two major parts: the filter synthesis part and the OTA stage optimization part (see Figure 21.4). Linked to these are a filter topology library and an OTA model library. Details of both parts are given in the subsequent sections.

The art of finding a good analog power estimator is finding that exact level of abstraction at which one can disconnect the topology information from all that comes below that abstraction level down to the transistor level. For continuous-time OTA-C filters, this level was found at the transconductor level. Finding the high-level specifications for the transconductors (g_m and distortion) starting from the filter specifications is done in the first step, the *filter synthesis part.* This step makes use of the filter topology library. In the second step, the *OTA optimization part,* optimization techniques are used in combination with behavioral models for the OTAs to find the minimal current needed to achieve the derived OTA specifications. The behavioral OTA models link the high-level specifications of the OTAs (g_m and distortion) to the design parameters. This modeling is done off-line and the results are stored in the OTA model library. This significantly speeds up the estimation process.

21.4.2. Description of the Filter Synthesis Part

The synthesis workflow of ACTIF, as illustrated in Figure 21.5, is as follows. On the top left part, the wanted filtering function (e.g. a fourth-order elliptic bandpass filter) is entered to the tool. The filter transfer function is then split in a first-order stage (in case the order is odd) and a number of second-order stages. These stages are mapped on a biquad topology and for each section the state–space matrices are constructed. Next, the total system state–space matrices are calculated. Using the desired dynamic range and the input signal level,

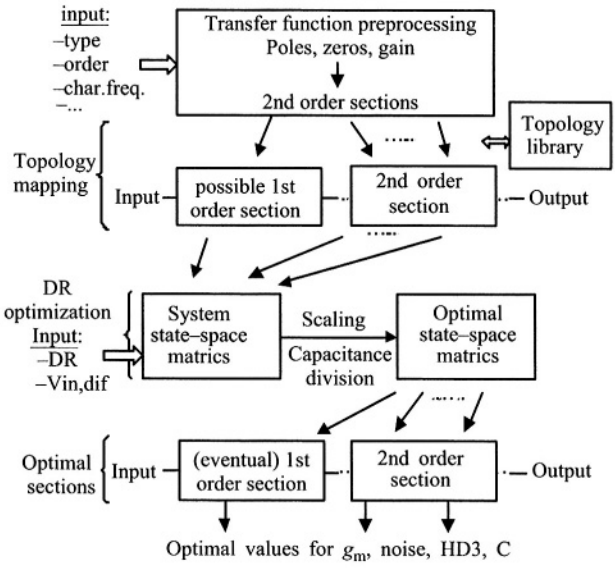


Figure 21.5. Synthesis workflow of ACTIF.

the optimal system state–space matrices are obtained after scaling and optimal capacitance distribution. The result is then broken up again into second-order sections and the optimal values for the needed OTA specifications are derived. This workflow is now discussed in more detail.

In Figure 21.6 an example of an implemented general biquad type is given together with its state–space matrices and its transfer function. The biquad is drawn in single-ended version but within ACTIF actually differential implementations are used, as it gains 6 dB in DR. Once a suitable topology with its description is found, the coefficient mapping is done. The system state-space matrices are constructed from the state–space matrices of the individual stages in the following way:

$$B_{\mathrm{sys}_i} = B_i \cdot \prod_{j=1}^{i-1} D_j$$

$$C_{\mathrm{sys}_i} = \prod_{j=i+1}^{n} D_j \cdot C_i$$

$$D_{\mathrm{sys}} = \prod_{i=1}^{n} D_i$$

$$\begin{cases} A_{\mathrm{sys}_{ij}} = B_i \cdot C_j \cdot \prod_{k=j+1}^{i-1} D_k : i < j \\ A_{\mathrm{sys}_{ij}} = A_i : i = j \\ A_{\mathrm{sys}_{ij}} = 0 : i > j \end{cases} \qquad (21.11)$$

where n is the number of stages. To obtain the wanted DR, the total capacitance budget available for the filter is swept from a maximal desirable value until the

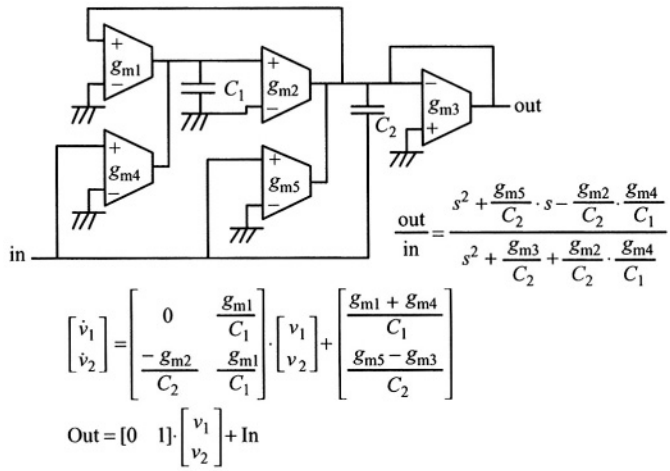


Figure 21.6. General OTA-C biquad, its transfer function and state–space representation.

goal is reached or until a minimum limit value is reached. For every capacitance value, scaling and optimal capacitance distributions are performed after which the DR is calculated. If the DR is fine, the sweep stops; if not, then a new total capacitance value is taken and the loop is repeated. Formulas needed for scaling, capacitance distribution as well as the calculation of the DR are taken from [12]. The optimization does not alter the topology of the filter stages.

From the now transformed and optimized system matrices, the state–space matrices of the stages are reconstructed by proper division or multiplication with the scaling or transformation matrix. The g_m values are obtained directly; the noise levels at the outputs of the internal integrators are calculated from the system state–space matrices, the signal swing and the DR:

$$V_{n,i}^2 = \frac{2 \cdot kT \cdot \xi_i \cdot \left(\left| B_{\text{sys}_i} \right| + \sum_j \left| A_{\text{sys}_{ij}} \right| \right) \cdot \max_j K_{\text{sys}_{jj}}}{\text{Cap}_i \cdot C_{\text{sys}} K_{\text{sys}} C_{\text{sys}}^T} \tag{21.12}$$

where Cap_i is the capacitance of integrator i, K_{sys} is the system controllability Gramian matrix and ξ_i is the noise figure of integrator i. The noise figure is assumed to be one or optimal. If a more accurate estimation is wanted, this value can be one for the first estimation, after which a better value is calculated using the information of the first results and the estimation process is repeated with the new value. The maximum distortion of each OTA can now be set equal to the noise floor:

$$\text{HD3}_i = 10 \log_{10} \left(V_{\text{in,dif}}^2 / V_{n,i}^2 \right) \tag{21.13}$$

or alternatively to a maximum of 1% of the signal level. Note that only the third-order harmonic distortion HD3 is taken into account because higher-order terms are typically smaller, the second-order term is canceled out in optimal differential designs, and the intermodulation product is obtained from the harmonic distortion term.

From here on the g_m and distortion levels of each OTA are known and are given to an optimizer, which determines the minimal current needed to reach these values in practical OTA implementations.

21.4.3. OTA Behavioral Modeling and Optimization for Minimal Power Consumption

For each OTA the bias current has to be minimized when given the above-calculated constraints on g_m and distortion. This means that for g_m and HD3, models have to be developed that relate g_m and HD3 of an OTA topology to its design parameters. To develop this library, five different OTA stages have been simulated in a $0.35\,\mu m$ CMOS process with varying design parameters and varying input voltage amplitude. The design parameters are characteristic for each gm topology. For example, for a source-degenerated differential pair, three parameters are used in the model: I_{DS} and $V_{GT} = (V_{GS} - V_T)$ of the input transistors and the degenerating resistance R. In total four parameters are sufficient for the five OTAs:

$$\begin{aligned} g_m &= f(I_{DS}, V_{GT}, w, R) \\ \text{HD3} &= f(I_{DS}, V_{GT}, w, R) \end{aligned} \tag{21.14}$$

where w, some device width, is one of the circuit design parameters. The five topologies suitable for a 3.3 V power supply are: a simple differential pair, a differential pair with source degeneration and three others that are found in [13–15]. This is a rather arbitrary choice that tries to span a large frequency and linearity range, but any other topology can be added to ACTIF.

Modeling of the transconductances. The models used for the different OTAs are based on existing hand formulas, which have been fitted to the simulated data. For a degenerated differential pair for example, the expression for g_m becomes:

$$g_m = \frac{1.77 \cdot I_{DS}/V_{GT}}{V_{GT} + I_{DS} \cdot R} = \frac{1.77 \cdot I_{DS}}{V_{GT} + I_{DS} \cdot R} \tag{21.15}$$

For the OTA structure from [15], the expression becomes:

$$g_m = \frac{I_{DS} \cdot V_{GT}}{V_{GT}^2 + I_{DS}/w} \tag{21.16}$$

Because a filter is a linear signal processing block, the small-signal g_m is modeled. All deviations from the ideal linear behavior for large signals are taken into account in the expressions for the distortion.

The distortion model. For each different OTA topology an expression for the third-order harmonic distortion is derived. The inputs to the model are the design parameters of the OTA and the signal swing, and the output is the distortion level. Theoretical expressions exist that do this for the used topologies but unfortunately they are only valid for very small signals, while the distortion is also needed for large signals. Therefore new distortion models were built. A typical simulated third-order distortion behavior for the OTA of [13] is plotted in Figure 21.7 (top) with the solid line. For small input signals,

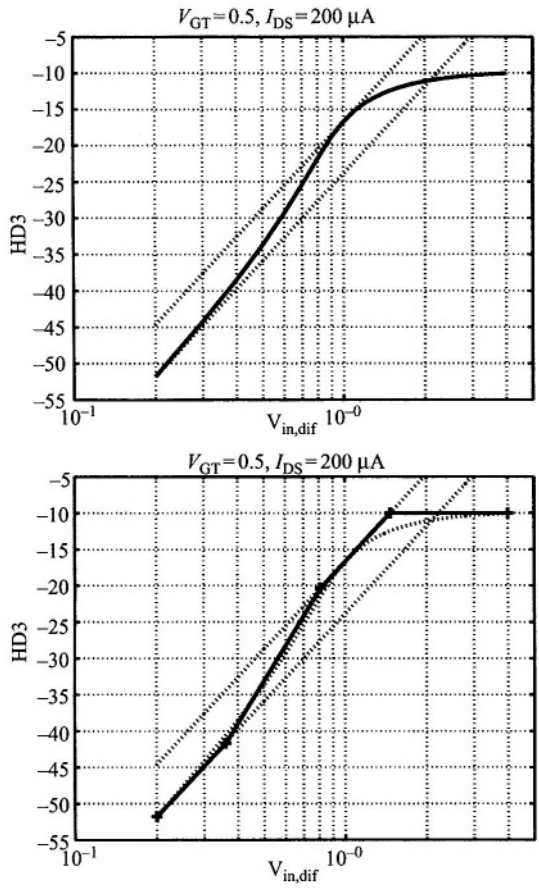


Figure 21.7. Third-order distortion profile as a function of the input signal for a given OTA [15]: simulated (top), modeled (bottom).

the line follows a nice slope of 40 dB/decade as expected, indicated by the lower dotted line. For larger signals the distortion degrades faster than this slope predicts due to large-signal behavior and at a certain signal amplitude the distortion is clipped at a certain value of (in the figure) about –10 dB. This behavior is modeled quite well by the solid line (bottom Figure 21.7) which is the model taken in ACTIF. For some OTAs, the two dotted lines experimentally turn out to be virtually the same and the four-region model changes in a two-region model. This distortion model together with the g_m model is then used in an optimizer to find the minimal power consumption needed to achieve the g_m and distortion specs.

Optimization. The OTA optimization flow is shown in Figure 21.8. For a given OTA parameter set, the boundaries of the regions in the HD3 model are calculated. If the region is known, then the expression for HD3 is known for that set of parameters. For example for the left region of the model:

$$\mathrm{HD3} = f(I_{DS}, V_{GT}, w, R) + 40\log_{10}(V_{in,dif}) \qquad (21.17)$$

With the expression for g_m added, the constrained-based gradient search optimization as implemented in Matlab™ can start looking for that parameter set for the asked g_m and HD3 values that yields minimal current I_{DS}. However, it is possible that the new set of parameters changes the model region of the HD3 model. So a kind of rule-based optimization was programed that notices when region oscillation occurs and handles it.

The output of the optimization is the optimized current needed for each OTA in the filter to achieve the specified values. From this the total power of the filter is then calculated and returned by ACTIF. It is typical that the g_m specification

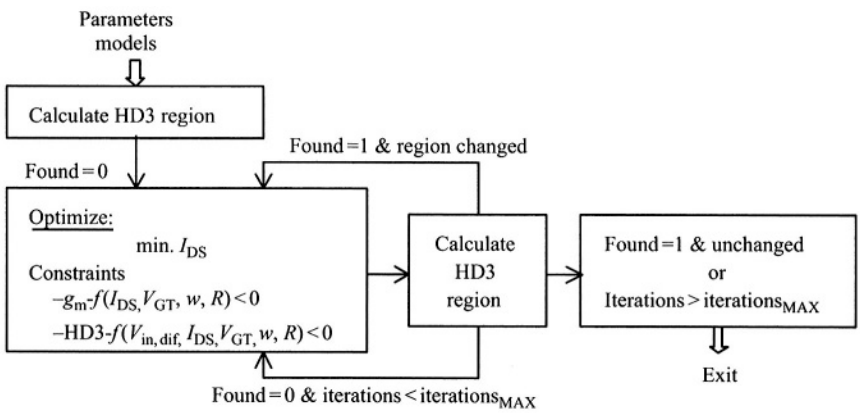


Figure 21.8. OTA optimization flow.

can easily be obtained and that the distortion specification is the limiting factor for the power. This stresses the importance of including the distortion behavior of the OTAs in the power estimation of filters.

21.4.4. Experimental Results

Two examples are given to illustrate the capabilities of ACTIF. Power estimation time for each example is about 6 min using a SUN SPARC-30 running Matlab™.

Example 21.1. A seventh-order phase-equiripple $0.35\,\mu m$ CMOS low-pass filter with a cut-off frequency of 70 MHz was presented in [16]. It consumes 55 mW, including the control circuitry, the DR is 42 dB and the differential input swing is $400\,mV_{PP}$. When given to ACTIF, the estimated power using high-speed OTA topologies is 34.9 mW. This is quite close to the reported 55 mW, considering that the control circuitry is still missing in our estimator. Including tuning strategies in the estimator is subject of further work.

Example 21.2. A fifth-order $0.8\,\mu m$ CMOS low-pass filter with a 4 MHz cut-off frequency, a DR of 57.6 dB, a differential input swing of 0.625 V_{PP}, a total intermodulation distortion of 40 dB and a power consumption of 10 mW was presented in [17]. This is a good example because the distortion level is lower than the DR and it is not a biquad implementation. It is realized in a different technology than the OTA models used in ACTIF but also with a 3 V supply voltage, which is the main limiting factor for distortion. If the correct distortion level is given to ACTIF, the outcome is that a total estimated power consumption of about 3.5 mW is needed for the most suited OTA topologies and about 10.6 mW for the worst one, again without tuning taken into account. For a high-level power estimation, this is close enough to the published power consumption of 10 mW, despite the fact that a different filter topology was used in the real implementation compared to the cascade-of-biquads approach of ACTIF. If, as an experiment, the filter would be redesigned by increasing the distortion specification up to the DR, then ACTIF predicts that the filter would require a total power of 88.8 mW.

21.5. Conclusions

This chapter has presented techniques to estimate the power consumed by an implementation of an analog block given only the specification requirements before knowing the detailed circuit implementation as needed in high-level architectural system exploration. Basically, two approaches exist to develop such estimators. In the top-down method, no information about the topology is used; only relevant high-level specifications are involved and solely determine

the consumed power to realize the wanted analog signal processing function. In the bottom up method on the other hand, the full topology information is used and thus every detail is potentially important, eventually in combination with the high-level specifications, to estimate the power. Most practical estimators are a combination of both approaches.

This was then illustrated for two different classes of analog circuits. First, a power estimator for the range of Nyquist-rate high-speed CMOS A/D converters has been presented. The estimator is simple and independent of the topology used (flash, pipelined, folding, interpolating) and it can easily be updated when new designs are published. Also, it is an analytical, continuous and technology-scalable function allowing reliable system exploration during the system-level design phase. The estimator experimentally was shown to have an accuracy of better than a factor $2.2\times$ for most of the considered ADC designs.

Next, a high-level tool called ACTIF was presented that estimates the power consumed by an analog continuous-time OTA-C filter. The inputs are high-level filter specifications (type, order, . . .), dynamic range and input signal amplitude. The output is an estimate of the power needed to realize the filtering function when an optimal implementation is used. The approach involves a filter synthesis step and an OTA stage power optimization step. Experimental results have shown a good accuracy for the power predictions of this ACTIF tool.

Acknowledgment

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Chapter 22

SPEED VS. DYNAMIC RANGE TRADE-OFF IN OVERSAMPLING DATA CONVERTERS

Richard Schreier, Jesper Steensgaard and Gabor C. Temes

22.1. Introduction

State-of-the-art VLSI technology, especially a fine-linewidth CMOS fabrication process, offers many advantages for the IC designer. These include high component density and high-speed operation. Unfortunately, from the analog circuit designer's viewpoint, these advantages come at a high price. Finer linewidth reduces the allowable supply voltages, and hence the maximum signal amplitudes in the analog stages. This leads to a deterioration of the *S/N* ratio. Hence, in new entertainment and communication applications, especially those using digital signal processing (DSP), the required resolution often exceeds the practical limitations of the analog peripheral circuitry. The problem is particularly severe for the data converters needed to implement the transition between the analog and digital signal domains. In a brute-force approach to data conversion, say in a simple resistive digital-to-analog converter (DAC) (Figure 22.1), the output voltage is derived from a resistor string. To perform an 18-bit data conversion, as needed for example in digital audio applications, the circuit must contain an impractical number (262,144) resistors. Also, the least-significant-bit (LSB) voltage (i.e. the difference between adjacent tap voltages) will be about $3.8 \times 10^{-16} V_{\text{ref}}$, where V_{ref} is the supply

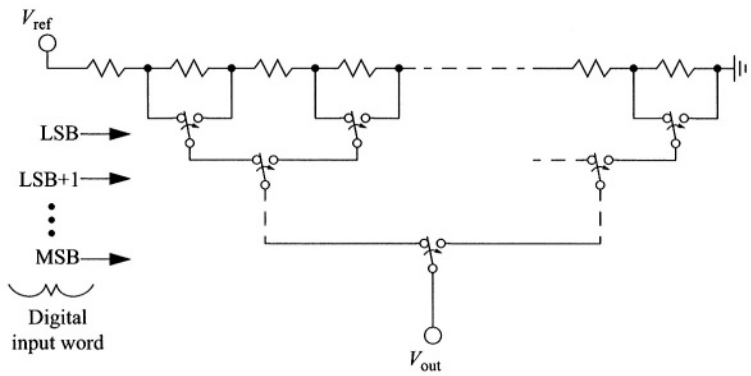


Figure 22.1. A resistor-string DAC.

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voltage. The accuracy of the output must be less than one half of the LSB voltage. The maximum matching error of the resistors in the string must then be less than 1.9×10^6. For a 1.8 V reference voltage, this leads to a voltage error of about $3.4\,\mu V$ and a required resistor matching accuracy of 2 ppm. These are clearly impractical values. Similar conclusions can be drawn for other brute-force conversion schemes, both A/D and D/A ones.

A strategy which can successfully overcome this problem is based on a trade-off between resolutions in amplitude and time. It has been known for a long time that by sampling an analog signal at a significantly higher rate f_s than that required by Nyquist's rule, the *S/N* conditions in its subsequent processing can be improved. This occurs because the energy of random noise, due, for example, to wideband thermal noise or uncorrelated quantization errors, is distributed over a wider bandwidth if the sampling rate is increased. Even more importantly, oversampling allows the filtering of both signal and noise, since the signal band now forms only a small part of the frequency range (between dc and $f_s/2$) in which the spectra of signal and noise can be modified. It will be shown how this added freedom can be used to suppress the quantization error energy in the signal band, and hence to increase drastically the in-band *S/N* ratio. The operation involves shaping the spectrum of the quantization error, and hence became termed (inaccurately) *noise-shaping*.

The price paid for this improvement includes the higher speed (typically, 64–1024 times faster) operation of the analog circuit, which usually requires more complex circuitry and more supply power. Also, the filtering associated with the sampling rate changes necessitates the inclusion of a DSP stage which may be fairly complex, and which requires added chip area and power. However, for high-resolution (>13 bit) data converters, the oversampling and noise-shaping approach usually turns out to offer an advantageous trade-off between relaxed analog matching accuracy and added chip area and power consumption. The operation of oversampling data converters and the trade-offs which they offer are discussed in Section 22.2.

A similar trade-off is encountered in the design of the internal DAC of both oversampling DACs and oversampling ADCs. This DAC, which usually needs only very low resolution, must nonetheless meet stringent linearity requirements. Except in the case of single-bit DACs, which are inherently linear, the linearity requirements are impractical to achieve directly. Section 22.3 shows how a combination of oversampling and noise- shaping can be used to achieve low in-band error despite the unavoidable nonlinearity of the internal DAC.

22.2. Oversampling Data Converters

22.2.1. Quantization Error

Digital signals can only have a limited number of amplitudes, and hence represent analog signals with a quantization error *e*. As illustrated in Figure 22.2,

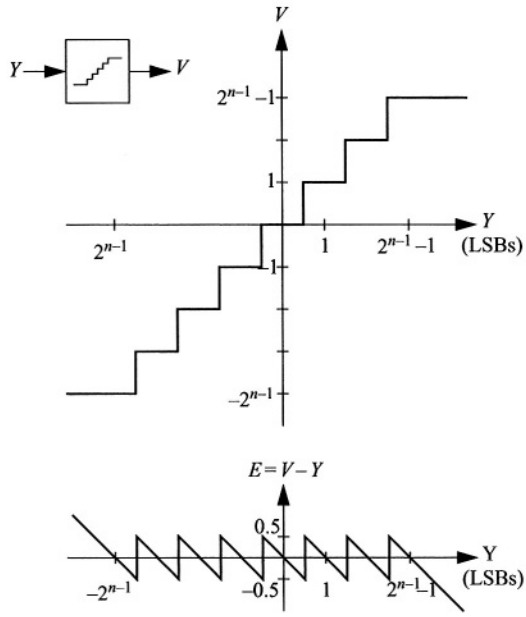


Figure 22.2. Quantization error of an ideal n-bit quantizer ($n = 3$ is shown).

for an ideal A/D converter, the input-referred value of the error satisfies $|e| \leq V_{\mathrm{LSB}}/2$. Often, it is permissible to make a number of simplifying assumptions about e. These are

1 The probability of any e value in its range of $[-V_{\mathrm{LSB}}/2, V_{\mathrm{LSB}}/2]$ is the same. From this, it follows [1] that its power (i.e. mean square value) is $V_{\mathrm{LBS}}^2/12$.

2 The power spectral density (PSD) $E(f)$ of the sequence $e(k)$ is white. Using one-sided spectral densities, this means that the power equals $E(f) \cdot (f_s/2) = V_{\mathrm{LSB}}^2/12$. Hence, the PSD is $E(f) = V_{\mathrm{LSB}}^2/6(f_s)$.

These assumptions lead to good approximations if the ADC input signal varies randomly from sample to sample by amounts larger than V_{LSB}. These conditions often hold for the circuits which will be discussed in this chapter.

Next, it will be shown how the trade-off between amplitude and temporal resolutions can be used for achieving better *S/N* performance in the presence of large internal quantization errors.

22.2.2. Feedback Quantizers

Figure 22.3 shows the block diagram of a feedback quantizer. It will be assumed that the feedback loop is stable; Chapter 4 of ref. [1] provides information on how to achieve and ascertain stability of the loop. For

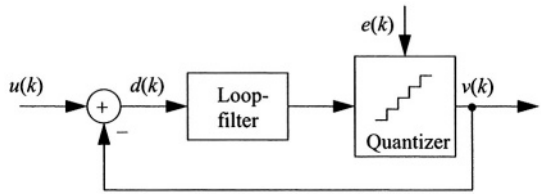


Figure 22.3. A feedback quantizer.

higher-order loops, this is a difficult issue due to the presence of a strong nonlinearity (the quantizer) in a feedback loop.

The loop incorporates a filter in the forward path, which amplifies selectively in the signal band the difference $d(k)$ between the input signal $u(K)$ and the output $v(k)$, that is, $d(K)$ is the output error. The loop filter is followed by a quantizer (if the loop-filter is analog, as is the case for an ADC) or a truncator (if the loop-filter is digital, as is the case for an all-digital loop, needed for a DAC). The digital output of the quantizer/truncator has very short word length: typical values are 1–3 bits. Hence, the quantizer is easily and economically realizable. However, since its V_{LSB} is large, it introduces a large error $e(k)$ into the signal. But this error is generated after the loop-filter, and hence in the z-domain its input-referred value is only $E(z)/\text{LF}(z)$, where $\text{LF}(z)$ is the transfer function of the loop-filter. By making $|\text{LF}(z)|$ large in the frequency region of the signal, the in-band PSD of the input-referred quantization "noise" can be reduced to a very small value. Thus, a high SNR is possible without extreme matching accuracy in the internal quantizer.

Notice that the mean square value of the output error $d(k)$ is large for a low-resolution quantizer, since its V_{LSB} is large. Hence, the integral of the PSD of $d(k)$ over the 0 to $f_s/2$ range is large. Therefore, the PSD can be suppressed only over a small part of this range. In conclusion, the signal band can only be a small fraction of the Nyquist range. This indicates again the trade-off between SNR and the oversampling ratio OSR. OSR is defined as the ratio between $f_s/2$ and the signal bandwidth.

An approximate calculation can be used to make the prediction of the described trade-off specific. It will be assumed (as everywhere in this chapter) that the signal band is around dc. In many feedback quantizers, the noise transfer function $\text{NTF}(z)$, from the quantizer output where the quantization error is generated to the output of the loop, is chosen as the maximally flat high-pass filter function

$$\text{NTF}(z) = (1 - z^{-1})^L \tag{22.1}$$

where L is the order of the loop-filter. From equation (23.1), using the approximations discussed in Section (22.2.1) to find the PSD of the quantization error,

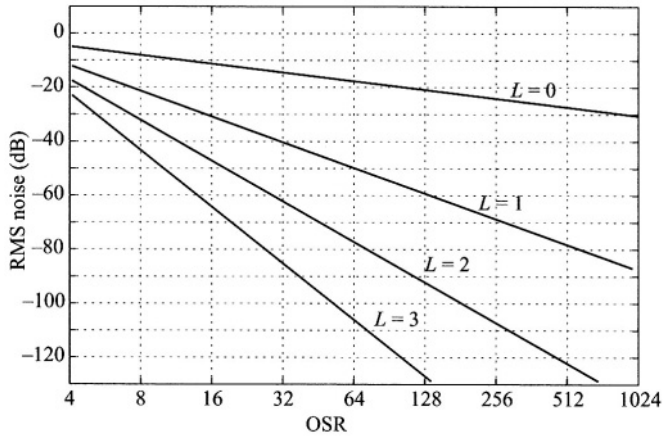


Figure 22.4. RMS in-band quantization error for NTFs of the form $(1 - z^{-1})^L$. The reference (0 dB) level is the in-band error of a Nyquist-rate ADC without noise-shaping.

it follows that the filtered (shaped) error PSD present at the output of the loop is

$$E_0(f) = \left(\frac{V_{\text{LSB}}^2}{12}\right)(2T)(2\sin(\pi f T))^{2L} \tag{22.2}$$

where $T = 1/f_s$.

The in-band noise power can be obtained by integrating $E_0(f)$ in the signal band. Figure 22.4 illustrates the result in a graphical form [1]. It gives the relative value of the RMS in-band noise for various loop-filter orders L, as a function of OSR. Zero dB corresponds to the RMS quantization error of an ADC without feedback loop and with Nyquist sampling (OSR = 1). As equation (22.2) and Figure 22.4 illustrate, the in-band noise can be reduced, and the SNR enhanced, by the following actions:

1 *Reducing* V_{LSB}: adding one more bit to the resolution of the internal quantizer reduces V_{LSB} by a factor of 2, and hence increases the SNR by 6 dB. (It also enhances the stability of the loop, and hence the improvement is likely to be larger than 6 dB.)

2 *Increasing L:* as Figure 22.4 illustrates, increasing the order of the loop-filter increases the SNR by an amount which depends on the OSR; the improvement is greater for higher OSR values. Increasing *L* reduces the stability margin, so the effective rise in the SNR will be lower than what Figure 22.4 predicts.

3 *Increasing the OSR:* the in-band noise is reduced, and hence the SNR increased, by $3(2L - 1)$ dB for every doubling of the clock frequency and thus the OSR.

The above derivations and results assume that the loop remains stable, and the quantizer is not overloaded.

22.2.3. Oversampling D/A Converters

Figure 22.5(a) shows the block diagram of an oversampling digital-to-analog converter [1]. The input $x(k)$ is a digital signal sampled at close to the Nyquist rate (i.e. $f_B \approx f_N/2$). It is next oversampled by a sampling signal with a frequency

$$f_s = (\text{OSR})\, f_N \tag{22.3}$$

and its spectral replicas centered around $f_N, 2f_N, \ldots, (\text{OSR} - 1) f_N$ are suppressed by the interpolation filter. The resulting signal enters the noise-shaping loop, where it is truncated to a few (typically, 1–3) bits. The PSD of the resulting quantization error in the output will be shaped such that it will have low values in the signal band, and large values out of band. Figure 22.5(b) illustrates the spectra of signals in the system.

The output signal of the noise-shaping loop can be converted into analog form by the internal DAC following the noise-shaping loop. The DAC has only a low (1–3 bit) resolution, and hence it can be realized economically.

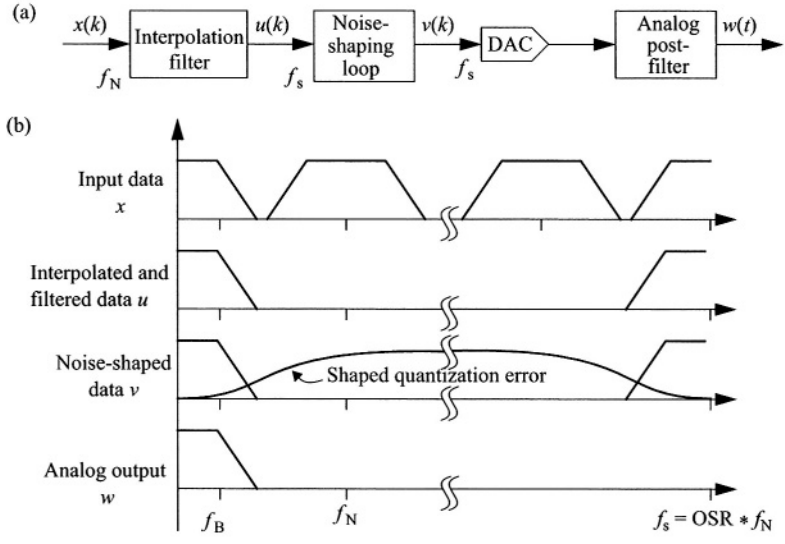


Figure 22.5. Block diagram of an oversampling DAC plus associated spectra.

However, the linearity and low noise of this DAC are critical, since any noise and nonlinearity error enters the signal without any additional shaping. In Section 22.3, several techniques will be described to achieve very high effective linearity for such low-resolution DACs. These techniques are also based on trade-offs between the desired linearity on the one hand, and oversampling and/or digital complexity on the other.

The output of the DAC is typically a stream of pulses, or a sampled-and-held waveform with large steps. It contains the desired signal in analog form, but also a large amount of out-of-band noise. The noise is then removed using the analog post-filter.

The trade-off between accuracy and oversampling is implemented by the (digital) noise-shaping loop, which reduces the in-band energy noise introduced when the digital signal is truncated to a few bits. Figure 22.6 illustrates two possible configurations for this loop. The first one (Figure 22.6(a) is sometimes called a delta–sigma structure, since it implements a subtraction (delta) operation at its input, followed by accumulators (sigma) in its loop filter. The output signal of the loop-filter is truncated to $n = 1$–3 bits, which are fed to the DAC for conversion to analog form, and also subtracted from the input signal. Linear analysis reveals that its signal transfer function is

$$\mathrm{STF}(z) = \frac{V(z)}{U(z)} = \frac{\mathrm{LF}(z)}{\mathrm{LF}(z)+1} \tag{22.4}$$

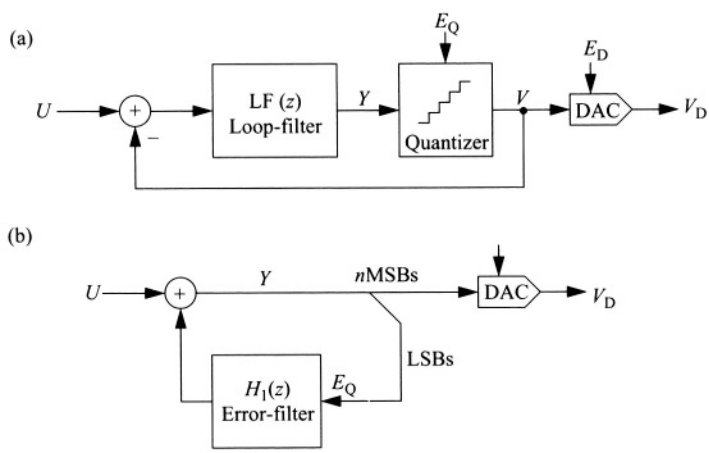


Figure 22.6. Two possible configurations for the noise-shaping loop: (a) delta–sigma structure, (b) error-feedback structure.

and its noise transfer function is

$$\mathrm{NTF}(z) = \frac{V(z)}{E(z)} = \frac{1}{\mathrm{LF}(z) + 1} \tag{22.5}$$

For values of z on the unit circle in the signal band, by design $|\mathrm{LF}(z)| >> 1$, and to a good approximation

$$\mathrm{STF}(z) \approx 1 \tag{22.6}$$

while

$$\mathrm{NTF}(z) \approx \frac{1}{LF(z)} \tag{22.7}$$

Thus, by choosing $\mathrm{LF}(z)$ as a high-gain low-pass filter function, the noise can be highpass filtered and thereby suppressed in the signal band. As an illustration, Figure 22.7(a) shows a fifth-order delta–sigma loop, with a 1-bit output signal. Figure 22.7(b) shows a possible pole–zero pattern for its noise transfer function.

Another possible configuration for the noise-shaping loop is shown in Figure 22.6(b). It is called the error-feedback structure. In this loop, the output

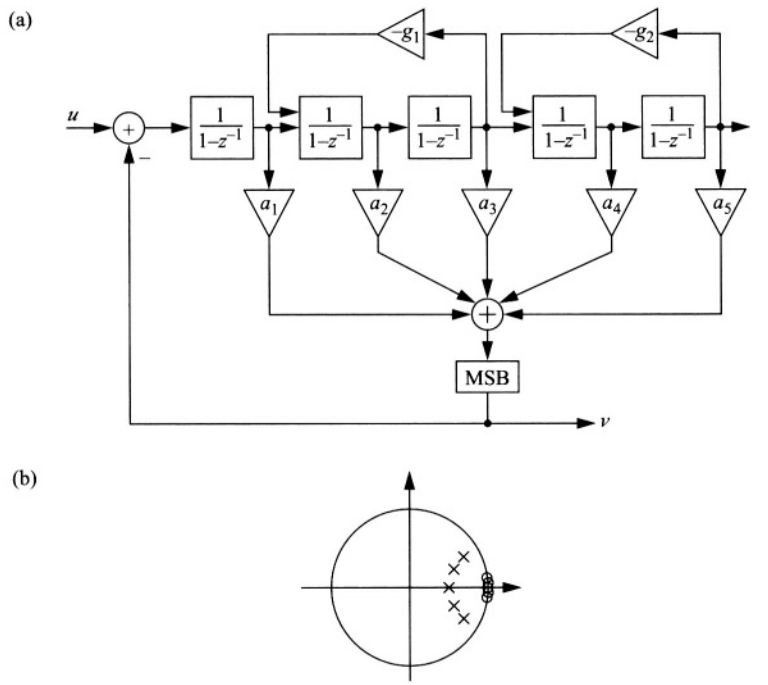


Figure 22.7. A fifth-order delta–sigma loop and a pole–zero plot of its NTF.

words of the input adder are partitioned: the N most significant bits (MSBs) are fed to the DAC, while the rest are filtered by the $H_1(z)$ transfer function, and then added to the input signal $x(k)$. Linear analysis shows that now the loop transfer functions are

$$\mathrm{STF}(z) = 1 \tag{22.8}$$

and

$$\mathrm{NTF}(z) = 1 - H_1(z) \tag{22.9}$$

Both configurations lead to practical architectures; for low-order loops, the error-feedback scheme usually gives simpler structures.

22.2.4. Oversampling A/D Converters

The block diagram of an Oversampling A/D converter is shown in Figure 22.8(a). The analog input signal is filtered in the anti-aliasing filter AAF, which is usually a very simple circuit since Oversampling allows a wide transition band between its pass- and stopbands. The output signal of AAF is sampled by the fast clock signal and entered into the noise-shaping loop. Here, the circuitry of the noise-shaping loop contains a sampled-data analog loop-filter, an internal quantizer (ADC) and an internal DAC in the feedback path (Figure 22.9). Unlike the noise-shaping loop of the Oversampling DAC of Figure 22.5, internal converters are needed because the input and output signals

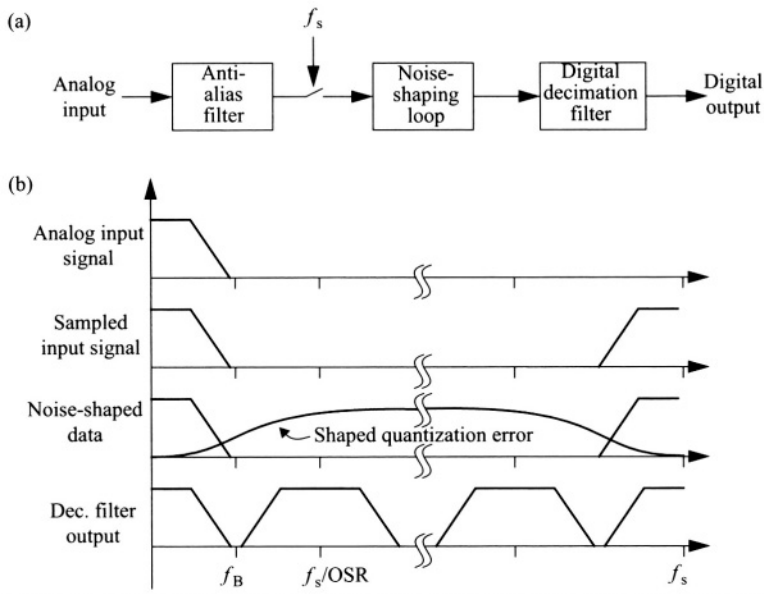


Figure 22.8. Block diagram of an oversampling ADC system and its associated spectra.

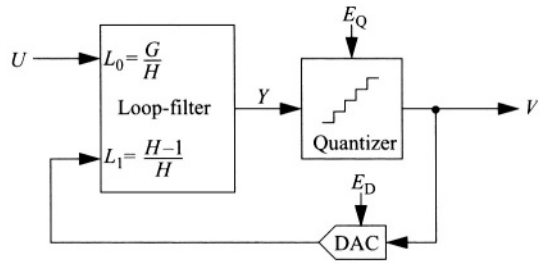


Figure 22.9. The noise-shaping loop of an ADC system.

of the ADC are of a different nature: the input is analog while the output is digital.

The noise-shaping loop is followed by a digital filter which removes the out-of-band portion of the quantization noise present in the output signal of the noise-shaping loop, and allows the sampling rate reduction (decimation) back to Nyquist rate of the final output signal without aliasing. Figure 22.8(b) illustrates the spectra.

The circuitry used in the NL of the ADC (Figure 22.9) is a generalization of the delta–sigma configuration of Figure 22.6 which allows independent control of the noise transfer function (H in the figure) and the signal transfer function (G). The error-feedback configuration is not practical for ADC loops, since inaccuracies in the subtractor, the filter and the input adder cause errors which enter the signal band without spectral shaping.

22.2.5. Multibit Quantization

In Section 22.22, the performance of an oversampled converter with a noise transfer function of the form $\mathrm{NTF}(z) = (1 - z^{-1})^L$ was described. However, 1-bit modulators employing NTFs of this form are stable only if $L \leq 2$. For higher values of L, the poles of the NTF must be shifted away from $z = 0$ toward $z = 1$. This shift in pole location results in a reduced NTF attenuation near DC and furthermore limits the SNR that can be achieved at a given oversampling ratio. According to Figure 22.10 [2], the theoretical SNR at an oversampling ratio of 16 is limited to approximately 70dB, while at an oversampling ratio of 8 the SNR is limited to a mere 40 dB. Thus, at low oversampling ratios, increasing the modulator order in a bid to increase performance offers a poor trade-off. Only if OSR is above 30 or so does increasing the modulator order yield significant SNR improvement.

If the application demands a combination of high SNR and high signal bandwidth, the requisite OSR may be impractical. In this case, the simplicity of a single-loop topology employing single-bit quantization must be foregone.

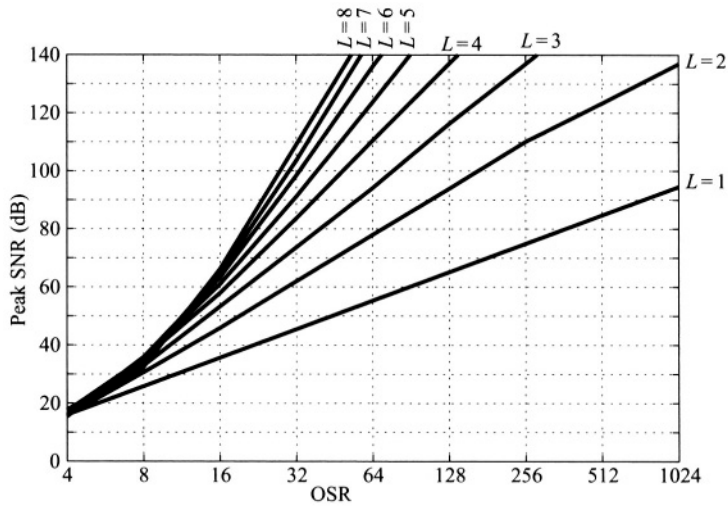


Figure 22.10. SNR limits for 1-bit modulators.

A multi-stage or multi-loop topology suffers from increased sensitivity to analog imperfections such as finite op-amp gain or component tolerances, while a multibit modulator places stringent linearity demands on its internal multibit DAC. Circuit techniques can be used to enhance op-amp gain, and calibration/compensation schemes can be used to achieve the required component accuracy or DAC linearity. However, a signal-processing technique, *mismatch shaping,* is especially attractive in the context of oversampled data conversion. Mismatch shaping can be implemented in a variety of ways, several of which will be presented in the next section.

Figures 22.11 and 22.12 are similar to Figure 22.10 in that they plot the theoretical SNR versus OSR for modulators up to order 8, but in these figures $n = 2$ and $n = 3$, respectively, where n is the number of quantizer bits. Note that the SNR which can be achieved at a given OSR increases dramatically as n is increased. For example, at OSR = 8 the theoretical SNR increases from less than 40 dB to over 60 dB and then to nearly 90 dB as n is increased from 1 to 2 and then to 3. Thus, wideband ADCs, which can only realize low OSR values, can nonetheless use noise shaping to achieve very high levels of performance if multibit quantization is used.

For a particular SNR and OSR, the designer can increase n in exchange for a reduction in the modulator order, L. This degree of freedom allows the designer to optimize performance parameters such as area or power consumption. Since increasing the modulator order by 1 is accomplished by adding one integrator to the back end of the modulator, while adding a bit to the quantizer doubles the complexity of the internal flash converter and/or DAC, the number of quantizer

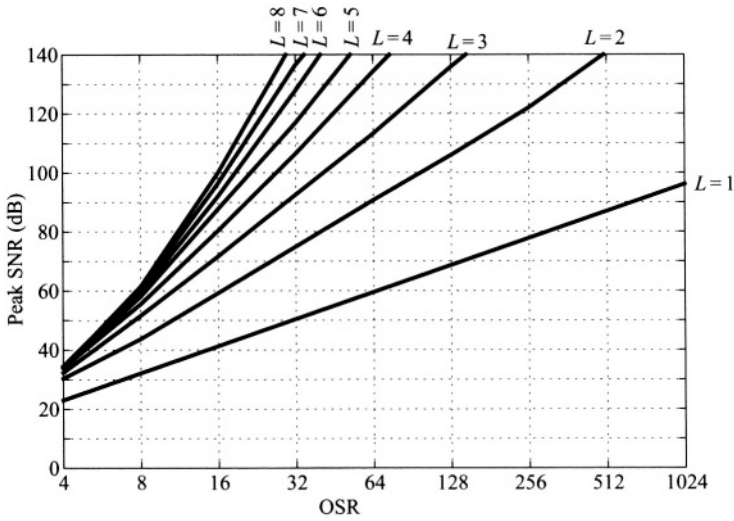


Figure 22.11. SNR limits for 2-bit modulators.

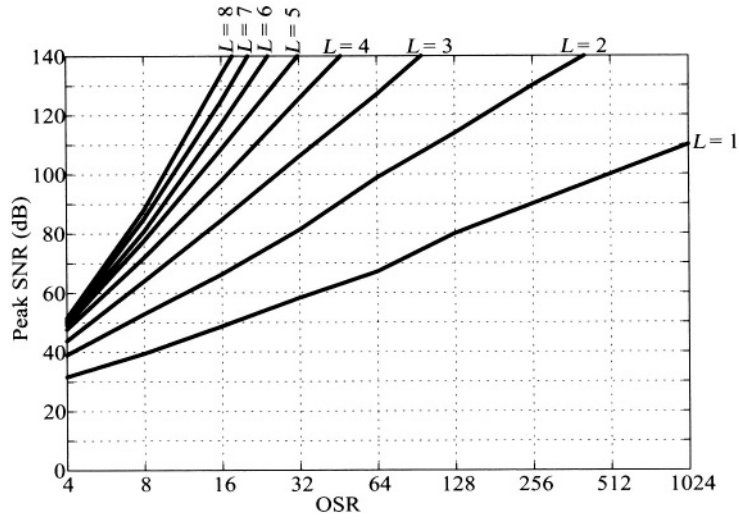


Figure 22.12. SNR limits for 3-bit modulators.

bits tends to be small. The optimum number depends on the cost of a quantizer bit relative to the cost of an integrator, and so depends on both the technology and on whether one is implementing an ADC or DAC system.

In an ADC system, the amount of power consumed by an integrator in the back end is small while the complexity and power of the flash ADC increases

exponentially with the number of quantizer bits. Thus an ADC favors a small number of quantizer bits, typically 5 or fewer. However, in a DAC system the power associated with an integrator in the back end is comparable to that of one located in the front end, the complexity of the truncator is virtually independent of *n,* and the analog post-filter is simplified if the unfiltered DAC output closely resembles the desired output waveform. These considerations tend to favor larger numbers of quantizer bits in DAC systems than in comparable ADC systems. The complexity of the internal DAC must be dealt with, but the fact that this DAC is at the output in a DAC system, rather than in the feedback path as in an ADC system, means that latency is unimportant, and consequently that multi-step DAC architectures can be used.

To illustrate the relationship between SNR and the quality of the unfiltered output, Figure 22.13 plots the SNR achievable with an order-L modulator operated at OSR = 8 and driven by a 1-LSB input [4]. The number of quantizer levels (2^n) determines both the level-of-significance of an LSB and the SNR of a full-scale input. As an example of how Figure 22.13 can be applied, consider the task of achieving 110 dB SNR at OSR = 8 while constraining the unfiltered error to have an rms value less than 1% of full-scale. The desire for low power in the unfiltered error implies that n must be moderately large, that is, 7 or higher. Table 22.1 compares the system parameters for $n \in [7, 10]$. For $n = 7$, the specification for low unfiltered error power is a very tight constraint and the design is only barely feasible. For $n = 8$, the unfiltered error constraint is less stringent, while for $n = 9$ and $n = 10$ the LSBs are so small that this constraint is irrelevant. This example illustrates one reason why it is desirable to have a large number of bits in the quantizer of a DAC system.

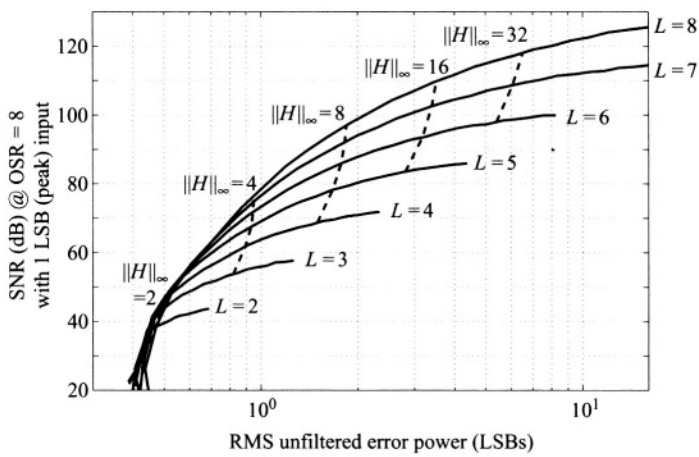


Figure 22.13. SNR vs. unfiltered error power for various modulator orders.

Table 22.1. System parameters for a SNR = 110 dB, OSR = 8 system with a constraint on the power of the unfiltered error.

Number of quantizer bits, n	7	8	9	10
1% of full-scale (LSBs)	1	2	5	10
SNR @1LSB peak input for 110dB SNR @ full-scale input (dB)	74	68	62	56
Minimum modulator order, from Figure 22.13	7	4	4	3
Unfiltered error (% of FS), from Figure 22.23	1	0.8	0.3	0.1

22.3. Mismatch Shaping

Crossing multi-bit quantization with oversampling allows the designer to combine the high degree of linearity characteristic of a delta–sigma converter with the wide bandwidth characteristic of a Nyquist-rate converter. The key to success in this approach is a very accurate DAC. Since the matching of like components in an integrated circuit is excellent, a DAC architecture which exploits many identical elements is the preferred starting point.

With careful layout, the raw matching of DAC elements can be reduced to the 12-bit level. To reliably realize converters with 14-bit or better performance, the element mismatch must be reduced further. Calibration can be used to correct or compensate element error, but is subject to drift. A technique described by Kenney and Carley [5,6], *dynamic element matching,* selects elements at random and thereby whitens the noise caused by element mismatch, but does not reduce the in-band power of the mismatch noise. In the remainder of this section, several schemes which impart a noise-shaped spectrum to the mismatch-induced noise are described. Since the existence of element selection strategies which spectrally shape the noise caused by the (unknown) element errors is at first glance counter intuitive, the simplest of the schemes is presented first and described from several viewpoints.

22.3.1. Element Rotation

A highly practical scheme which results in first-order shaped mismatch errors is the element rotation scheme [7–11], a conceptual realization of which is depicted in Figure 22.14. From the figure, it is clear that $V_D(z) = KV(z) + (1 - z^{-1})E_D(z)$, where K is the DAC gain, so DAC errors are first-order shaped. Unfortunately, the diagram is not directly realizable since the integrator which precedes the DAC produces arbitrarily large outputs for DC inputs and thus the DAC needs to have an infinite number of levels.

However, a DAC with an infinite number of levels can be mimicked by a finite number of elements arranged in a ring, or, as shown in the diagram, stacked end-to-end. Also, by merging the differentiation operation with the

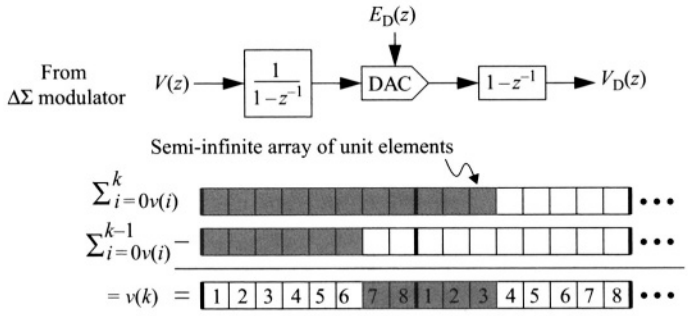


Figure 22.14. Conceptual derivation of element rotation.

DAC as illustrated in the figure, the output can be formed by simply combining $v(k)$ adjacent elements ($v(k)$ is required to be an integer in the range [0, m]). A direct calculation shows that the e_D sequence is

$$e_D(k) = \sum_{i=1}^{\gamma(k)} ee_i \tag{22.10}$$

where ee_i is the error of element i (defined as the difference between the actual element value and the average of all the elements) and

$$\gamma(k) = \text{mod}\left(\sum_{i=0}^{k} v(i), M\right) \tag{22.11}$$

Note that e_D is differentiated in the final output.

A second way to see how element errors can be made to produce shaped noise is shown in Figure 22.15. In this figure, m binary DACs are driven by m binary modulators and the DAC outputs are added together. Since the output of each DAC is a noise-shaped rendition of the input, the sum will be similarly noise-shaped.

This simple scheme works in the sense that linearity is not limited by element mismatch, but the system fails to exploit the two key advantages of multibit quantization: aggressive noise-shaping (each modulator is binary and thus subject to stringent stability constraints) and an output waveform that is close to the desired output waveform (the modulators do not coordinated their quantization decisions).

22.3.2. Generalized Mismatch-Shaping

To overcome the above drawbacks, one can impose the constraint that the number of elements enabled at any instant must equal v, the output of an

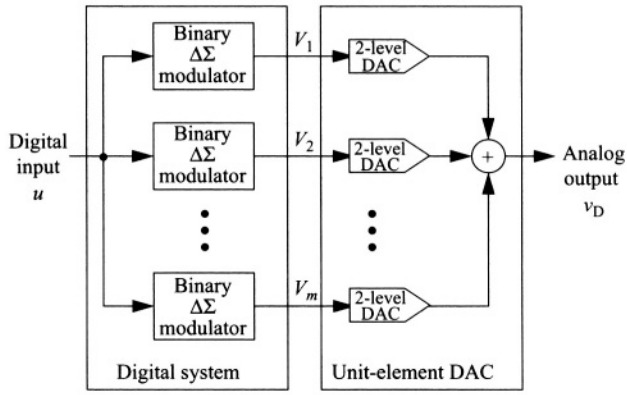


Figure 22.15. A mismatch-insensitive multi-bit DAC.

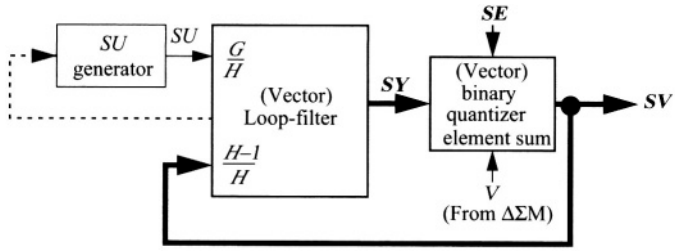


Figure 22.16. Canonical structure for producing a mismatch-shaping selection.

(m + 1)-level delta–sigma modulator. This choice links the binary modulators and results in the system of Figure 22.16 [12]. (As before, v is an integer in the range [0, m].) In this figure, the modulators' loop-filters and the (coupled) quantizers are represented with single blocks whose inputs and outputs are, in general, vectors. The vector nature of signals is indicated by heavy lines and bold text. The fact that an external (m + 1)-level delta–sigma modulator dictates a constraint on the number of elements chosen by the quantizer is represented by the V input in the figure.

Using a $\Delta\Sigma$ modulator-like structure to drive each element is responsible for the mismatch-shaping. However, the element sum constraint ensures that, in the absence of element mismatch, the output of the DAC will be that of a (high-order and aggressive) multibit modulator.

To see that the above statements are correct requires only a few definitions and some algebra. Let $\boldsymbol{ee}$ be an m-element vector whose components are the element errors ee_i. Since the element errors are defined as the difference between the actual element values and the average of all element values, the sum of the

element errors is zero:

$$\sum_{i=1}^{m} ee_i = [1\ 1 \cdots 1] \cdot \boldsymbol{ee} = 0 \tag{22.12}$$

where • represents dot product. Now define the *selection vector,* $\boldsymbol{sv}$, as an m-element vector of ones and zeros specifying which elements are enabled in an m-element DAC. Since the error in the output of the DAC is simply the sum of the errors of the elements which are "on", the error in the DAC output is

$$de(k) = \boldsymbol{sv}(k) \cdot \boldsymbol{ee} \tag{22.13}$$

To model the behavior of the system shown in Figure 22.16, observe that the system is simply a vector version of the general modulator structure of Figure 22.9. More explicitly, the system of Figure 22.16 consists of m identical binary modulators driven by a common input, SU. By absorbing the G factor into the SU-generator block, the vector version of $V = GU + HE$ can be written immediately:

$$\boldsymbol{SV}(z) = SU(z)[1 \cdots 1] + H(z)\boldsymbol{SE}(z) \tag{22.14}$$

The z-transform of the DAC error $E_D(z)$ is therefore

$$\begin{aligned} E_{\mathrm{D}}(z) &= \boldsymbol{SV}(z) \cdot \boldsymbol{ee} \\ &= (SU(z)[1 \cdots 1] + H(z)\boldsymbol{SE}(z)) \cdot \boldsymbol{ee} \\ &= SU(z)[1 \cdots 1] \cdot \boldsymbol{ee} + H(z)\boldsymbol{SE}(z) \cdot \boldsymbol{ee} \\ &= H(z)(\boldsymbol{SE}(z) \cdot \boldsymbol{ee}) \end{aligned} \tag{22.15}$$

If the $\boldsymbol{se}(k)$ sequence is bounded, then $\boldsymbol{E_D}(z)$ is equal to $H(z)$ times the z-transform of a bounded signal. The error induced by element mismatch will, therefore, be shaped by $H(z)$.

The foregoing discussion shows that as long as the element selection logic (ESL) is stable, the element mismatch will be shaped, independent of the algorithms used to implement either the quantizer or the SU-generator blocks. However, the stability of the ESL is tied to the algorithms used to implement the quantizer and SU generator, as well as to $H(z)$. For a given $H(z)$, some element selection strategies may result in stable ESL while others may not.

Figure 22.17 shows an error-feedback implementation of the structure in Figure 22.16, and indicates explicit methods for computing the su and $\boldsymbol{sv}$ signals. The rationale for the algorithms suggested in Figure 22.17 are

1 Setting $su(k)$ to the negative of the minimum value of the output of the $H(z) - 1$ block makes all the components of the $\boldsymbol{sy}(k)$ vector as small as

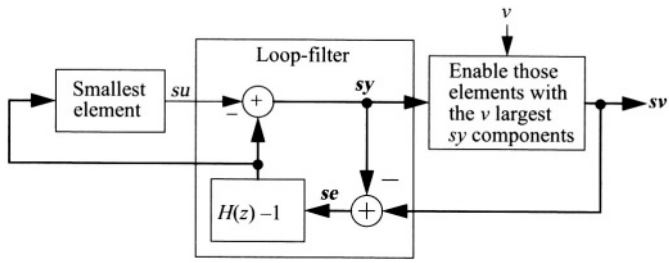


Figure 22.17. An implementation of Figure 22.16.

possible while keeping them positive. This "normalization step" removes a common constant from all components of the $\boldsymbol{sy}(k)$ vector and helps to keep the components finite,

2 Enabling the DAC elements which correspond to the $v(k)$ largest components of $\boldsymbol{sy}(k)$[1] minimizes the norm of the $\boldsymbol{se}(k)$ vector, and thus helps to keep signals finite. Since this choice makes the element selection independent of the normalization step described above, there is little to be gained by alternative choices for *su.* However, other selection strategies are certainly possible and may result in superior performance or a simpler realization.

Although the stability of this system is an open question, simulations indicate that the system is stable for a variety of $H(z)$ which satisfy $\max |H(e^{j\omega})| < 1.5$, provide the v input does not stay too close to the extremes of the DAC range (0 and m) for too long.

A simple choice for the mismatch-shaping transfer function is $H(z) = 1 - z^{-1}$. It is easy to show that this choice results in a stable system whose dynamics reduce to the element rotation scheme described in the previous section when the arbitration scheme described in footnote is applied. In this sense, the system of Figure 22.17 may be considered to be a generalization of the element rotation scheme.

More elaborate mismatch-shaping transfer functions result in complex element selection hardware. In particular, the sorting operation called for in the embodiment of Figure 22.17 is a hardware-intensive block. Introducing latency in this block to simplify the hardware is acceptable if the ESL is used in a DAC system, but is not tolerable in an ADC system. A partial-sorting scheme [13,14]

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[1] If several components of $\boldsymbol{sy}(k)$ are equal, the $v(k)$ largest components need not be unique. Choosing among elements with the same "desired usage" can be done arbitrarily; the simulations presented here give first priority to the first elements in the element array.

can be used to simplify the hardware; the price paid is a slight decrease in system performance.

All the usual tricks from the delta–sigma modulator literature can be applied to the element selection logic depicted in Figure 22.17. Dither can be added (at the quantizer input, for example) to eliminate tones caused by the deterministic operation of the loop; multibit quantization in the vector quantizer can be used if (as in the case of a switched-capacitor DAC) the elements can be used several times in a single clock cycle; and multi-stage modulation can be used if an LSB DAC is added to the system [16]. Lastly, for DACs where element dynamics limit the performance, the modified mismatch-shaping technique [17] can be useful.

22.3.3. Other Mismatch-Shaping Architectures

Two architectural alternatives to the above canonical form which trade performance for hardware simplicity are described briefly in this section. Galton's hierarchical mismatch-shaping structure [18] supports a variety of mismatch-shaping transfer functions with reduced hardware complexity but requires that the number of unit element be a power of 2, while Hernandez's structure [19] is an even more hardware-efficient method which works at the bit-level but shapes only the low-order mismatch-induced error terms.

The hierarchical mismatch-shaping DAC structure is shown in Figure 22.18. At each level of the hierarchy, a DAC is decomposed into a signal splitter and two sub-DACs. The sub-DACs are then further decomposed until each DAC is a single-bit DAC, at which point the recursion terminates. The shaped sequence generator (SSG) shown in Figure 22.18(b) produces two noise-shaped sequences which drive the two sub-DACs. Since each sub-DAC splits its input into two more noise-shaped sequences which in turn drive two sub-DACs, and since this decomposition continues until the DACs are single elements, the elements DACs at the end of the tree are all driven by noise-shaped sequences and thus the mismatch errors of the elements are noise-shaped.

In order for the operations shown in Figure 22.18(a) to yield integer results for $v_1(k)$ and $v_2(k)$, the SSG must produce a signal that is even when $v_0(k)$ is even and odd when $v_0(k)$ is odd. Furthermore, since the SSG output must be such that $v_1(k)$ and $v_2(k)$ are in the range $[0,\ 2^{m-1}]$, the absolute value of the output of the SSG must be less than $2^m - |v_0(k)|$. The SSG is thus akin to a delta–sigma modulator with zero input and several constraints on its output (i.e. on its quantizer). This interpretation leads directly to the implementation shown in Figure 22.18(b).

Hardware efficiency is achieved by avoiding a global sorting operation, but simulations indicate that the structure is not stable with as aggressive a

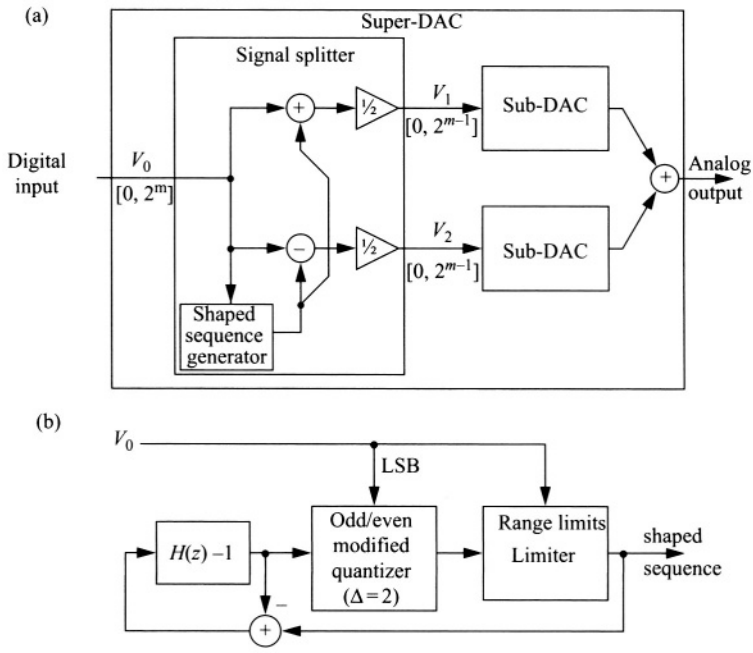


Figure 22.18. A hierarchical mismatch-shaping DAC. (a) Decomposition of a super DAC. (b) Details of the shaped sequence generator.

mismatch-transfer function as the canonical form can support. This will be illustrated with an example in the next section.

The binary-weighted mismatch-shaping DAC is depicted in Figure 22.19. In this system, a reference current is split into two (nominally equal) currents, one of which is routed to the next cell and the other of which is used to form the output current (under the control of the appropriate data bit). The selection of which current is used for which purpose is controlled by the c_i bits which are produced by a digital logic block The logic block is moderately complex and so will not be described here. The key feature of this block is that its complexity grows linearly with the number of DAC bits, rather than exponentially as in the preceding schemes. The main drawbacks of the method are that it only shapes the low-order error terms and that a straight-forward implementation of the current-splitters using MOS devices requires a large amount of headroom.

22.3.4. Performance Comparison

This section compares the performance of several mismatch-shaping techniques in the context of 17-level DAC system which uses a sixth-order NTF optimized for OSR =16 whose infinity norm is 4. The DAC system is driven

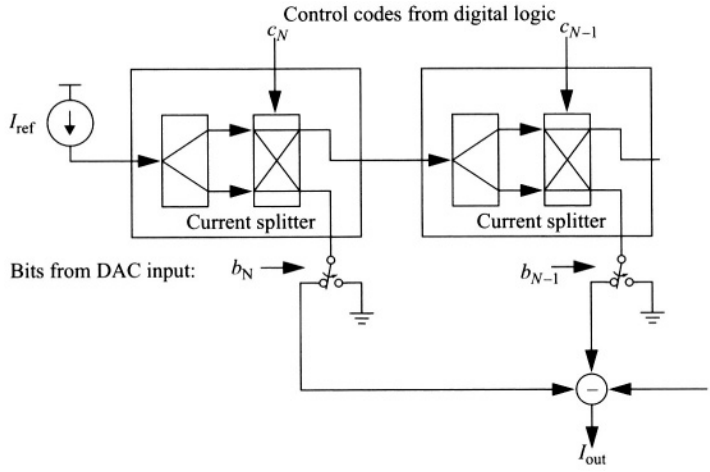


Figure 22.19. An implementation of a binary-weighted mismatch-shaping DAC.

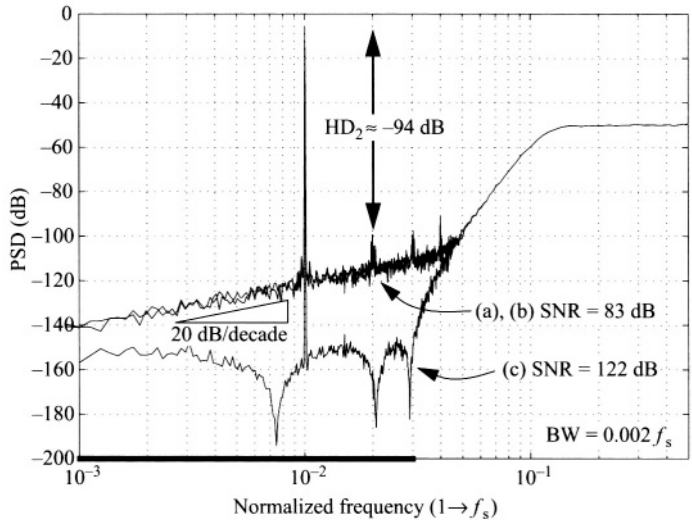


Figure 22.20. SNR and spectra for first-order mismatch-shaping schemes with 1% mismatch: (a) hierarchical (Figure 22.18), (b) element rotation (Figure 22.14) and (c) ideal DAC.

with a half-scale input and the DAC element values have a standard deviation of 1%. As Figure 22.20 shows, 1% mismatch is sufficient to reduce the ideal SNR from 122 dB to a mere 60 dB in the absence of mismatch shaping, with harmonic distortion being the dominant form of SNR degradation.

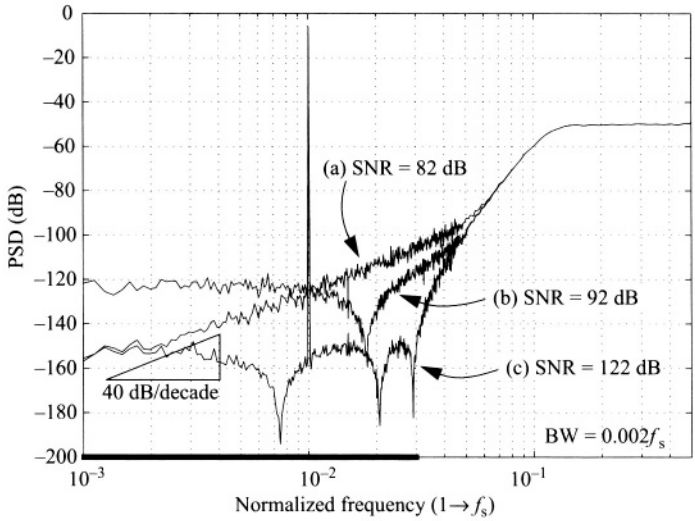


Figure 22.21. Spectra for second-order mismatch-shaping schemes: (a) hierarchical form with H(z) given by equation (22.16), (b) canonical form with H(z) given by equation (22.17), (c) ideal output spectrum.

As Figure 22.20 shows, first-order mismatch shaping causes the SNR to improve to about 83 dB, although harmonic distortion is still evident at about the –90 dB level. Observe also that the 20 dB/decade slope of the noise floor is consistent with the fact that the MTF is first-order, and that the element-rotation (Figure 22.14) and hierarchical (Figure 22.18) schemes provide virtually identical spectra even though their raw element usage patterns can be very different.

Figure 22.21 compares the spectra for two second-order mismatch-shaping systems. The first system [18] uses the hierarchical form of Figure 22.18 with

$$H(z) = \frac{z^2 - 2z + 1}{z^2 - 1.25z + 0.5} \tag{22.16}$$

This MTF has an out-of-band gain of about 1.5 and $|H(e^{j\omega})| \approx 4\omega^2$ for $\omega \ll 1$. As Figure 22.21 shows, this second-order MTF yields a SNR which is marginally worse than that achieved with a first-order MTF, even though the slope of the noise is higher (40dB/decade). The reason is simply that at low oversampling ratios, the SNR advantage of a high-order MTF is eroded. However, the figure indicates that a second-order MTF has the advantage of producing less harmonic distortion than a first-order MTF. The lower tone level is thought to be a result of the fact that the element usage patterns are more

exotic than the concatenation of adjacent elements which is characteristic of the first-order systems.

The second system whose output spectrum is plotted in Figure 22.21 uses the structure of Figure 22.17 with

$$H(z) = 1 - 1.987z^{-1} + z^{-2} \tag{22.17}$$

This MTF has an out-of-band gain of about 4 and $|H(e^{j\omega})| \approx \omega^2$ (12dB lower than the preceding MTF) for $\pi/(\mathrm{OSR}) \ll \omega \ll 1$. Non-coincident transmission zeros further enhance the attenuation in the band of interest and thus the SNR of this second-order system is able to achieve an improvement of nearly l0 dB over the first-order systems. As was the case with the preceding second-order system, no tones are visible in the passband (the vertical line near $f = 0.015 f_s$ is a dip in the upper curve and not a spike of the lower curve).

Since the two second-order systems presented above use different MTFs, it would appear that the comparison is unfair. However, simulations show that if the MTF of equation (22.17) is used in the element-shuffling system, then the element selection logic is unstable and mismatch-shaping does not occur. The system of Figure 22.17 appears to tolerate a more aggressive MTF, which in turn implies that this system has a performance advantage over the element-shuffling approach.

Thus, for the ultimate in DAC performance the hardware-intensive canonical form yields the greatest attenuation of mismatch-induced noise. If the OSR is high, then the simple element rotation scheme is likely to provide adequate mismatch attenuation, while if the OSR is modest and hardware constraints are important, then one of the other mismatch- shaping architectures described in this section might prove to be effective.

22.4. Reconstructing a Sampled Signal

The trade-offs involved in designing delta–sigma data converters have changed significantly as new technologies and signal-processing techniques have become available. Particularly the development of mismatch-shaping techniques has changed fundamentally the boundaries for the optimization process.

This section will consider the design of D/A converters that produce an analog output signal which is continuous in both time and magnitude. The digital input signal is inherently discrete in time and magnitude, and hence reconstructing the waveform involves interpolation in these two dimensions.

Signals that are sampled at the Nyquist rate may potentially exhibit full-scale sample-to-sample transitions. This worst-case situation is relevant because such signals occur frequently in applications where high information density is

desirable, for example, when storing signals on compact disks (CDs) or other digital media.

22.4.1. The Interpolation Process

Interpolation in time involves increasing the sampling frequency. Ultimately, we must generate a continuous-time signal, which from one viewpoint may be construed as an analog signal sampled at an infinitely high frequency. The transition from discrete-time (DT) to continuous-time (CT) signals is a critical step, which we shall refer to as the DT/CT conversion process.

"Interpolation in time by a factor of N" shall be defined as the process of inserting $N - 1$ zero-valued samples between each of the original signal's samples, whereby the sampling frequency is increased by a factor of N. Clearly, the inserted samples should ideally have the values that would stem from sampling the ideal waveform at the higher sampling frequency. "Interpolation in magnitude" shall refer to the process of adjusting the samples' values to better approximate the ideal sequence.

An interpolation system example. Figure 22.22 shows the general concept of interpolating in time and magnitude. A signal $x(t)$ is represented by a sampled sequence $x_1(k) = x(k/f_1)$; it is assumed that the sampling frequency f_1 just barely fulfills Nyquist's rule. Provided that aliasing did not occur in the sampling process, the signal's waveform is reproducible from the sequence $x_1(k)$, which is uniquely characterized by its frequency spectrum $X_1(f)$, $|f| < f_1/2$. (Recall that the spectrum of any real-valued sampled sequence is periodic with the sampling frequency as the period, that is, $X_1(f)$ is periodic with period $f = f_1$.)

By interpolating $x_1(k)$ in time by a factor of two, we obtain the signal $x_2(k)$ shown in Figure 22.22(b). The frequency spectrum of $x_2(k)$ is identical to that of $x_1(k)$, which confirms that the two signals have exactly the same information and energy.

Ideal interpolation of $x_2(k)$ in magnitude is obtained by filtering the signal with an ideal filter eliminating all spectral components not in the signal band. In this case the filter should eliminate every other spectral replica of $x(t)$ in $X_2(f)$, which yields the signal $x_3(k)$ shown in Figure 22.22(c). Notice that $x_3(k)$ is identical to the signal that would be obtained by sampling $x(t)$ at the higher sampling frequency $f_2 = 2f_1$.

Ideal interpolation in magnitude, however, is not practically feasible because that would require a filter of infinitely high order. Using a filter of reasonable complexity, we are able to suppress the undesired spectral replicas by only, say, 40 or 60 dB. Hence, when interpolating $x_2(k)$ in magnitude we will realistically obtain a signal that qualitatively is similar to $x_4(k)$ shown in Figure 22.22(d).

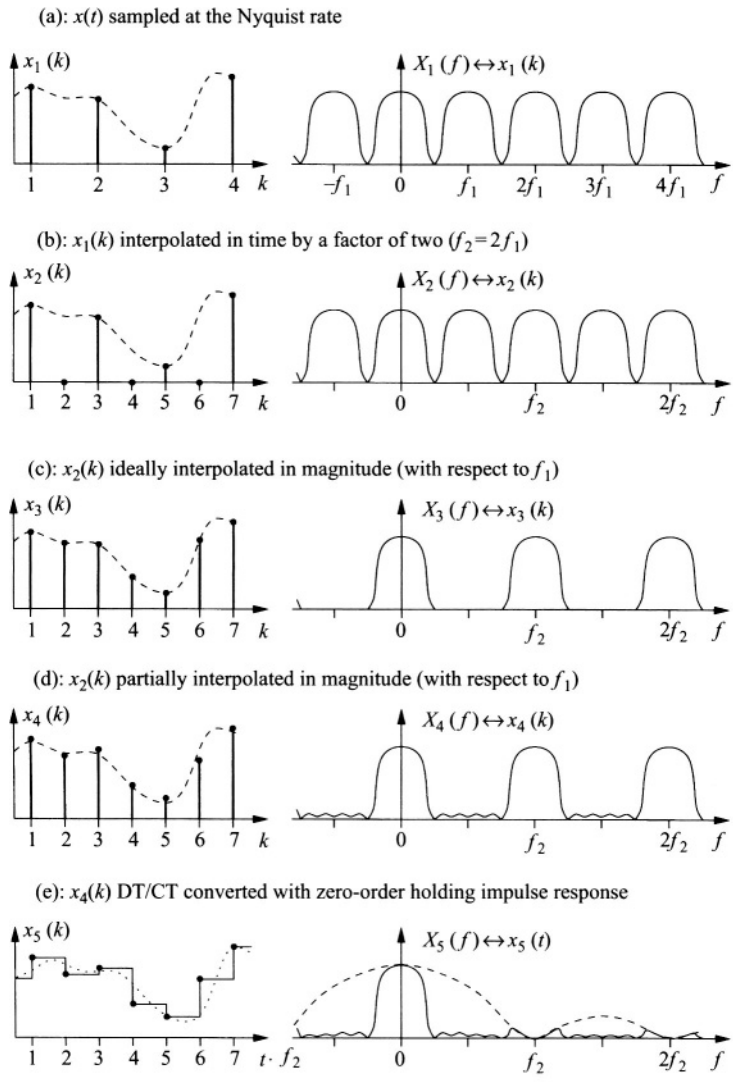


Figure 22.22. The interpolation process discussed in Section 22.4.1.

The dislocation of the samples' values reflect the filter's non-ideal frequency response, which is a *linear* non-ideality that does not cause distortion. For critical applications, such as audio, the filter's frequency response must be linear in phase, which often necessitates the use of FIR filters of very high order.

Usually, the initial sequence $x_1(k)$ is interpolated stepwise (cascading several interpolation stages), but here we shall assume that $x_4(k)$ is DT/CT converted directly with a sample-and-hold circuit characterized by a zero-order holding impulse response (i.e. an impulse response of value 1 for $0 < t \cdot f_2 < 1$,

and otherwise 0). That will generate the staircase signal $x_5(t)$ shown in Figure 22.22(e). In the frequency domain, the DT/CT conversion process is equivalent to a linear filter, that is, the spectral composition of $x_5(t)$ can be calculated as the product of $X_4(f)$ and the Fourier transform of the DT/CT conversion process's impulse response (shown with a dashed line in Figure 22.22(e) on top of $X_5(f)$).

The original waveform *x(t)* is also shown in Figure 22.22(e) with a dotted line. It is shifted slightly in time to compensate for the DT/CT conversion process's delay (the DT/CT conversion effectively delays the signal by $0.5/f_2$). We observe that the signals are similar, but clearly not identical.[2] This difference stems primarily from the incomplete elimination of the out-of-band energy that was introduced by sampling the signal in the first place $(x(t) \rightarrow x_1(k))$.

Although the signal-band information of $x_5(t)$ is intact (albeit possibly filtered), the large vertical steps, which represent substantial high-frequency energy, make it very difficult to process $x_5(t)$ using continuous-time circuitry. High-frequency spectral components made subject to filter nonlinearities may, for example, fold back into the signal band and thereby considerably deteriorate the overall performance. The step size of $x_5(t)$, that is, the sample-to-sample variations in $x_4(k)$, may be used as a measure for the "difficulty" involved in processing the staircase signal. Generally we would want the step size to at most one tenth of full scale, preferably much less. Assuming that the interpolation is performed ideally in all steps but in the DT/CT conversion (which is assumed to the characterized by a zero-order holding impulse response), we find that the worst-case,[3] normalized, maximum step size is approximately π/OSR. Hence, we may conclude that, regardless of how we are going to implement the D/A conversion process itself, we would like to oversample the signal by at least 32 times, preferably even more.

22.4.2. Fundamental Architectures for Practical Implementations

The order of the D/A and DT/CT conversions is the only fundamental constraint imposed on the signal reconstruction process. Some of the more subtle trade-offs in the design of oversampled D/A converters relate to where and how we choose to interpolate the signal, and exactly where in the signal path we choose to make the transition to the analog domain.

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2 The difference will remain even if we, more correctly, compare $x_5(t)$ to $x(t)$ filtered by the same steps that characterize the overall interpolation process.

3 Calculated for a full-scale oversampled sinusoidal signal at the edge of the signal band.

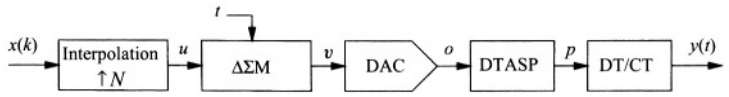


Figure 22.23. Single-bit delta–sigma DAC system.

Single-bit delta–sigma modulation. Figure 22.23 shows the conventional delta–sigma topology. From a signal processing point of view, we may regard the delta–sigma modulator (as a system that adds a noise-like truncation signal $t(k)$ to $u(k)$, such that $v(k)$ will be of the desired low resolution).[4] (Notice that $t(k)$ is merely $e(k)$ filtered by NTF(z).)

Although the power spectral density (PSD) of $t(k)$ is supposedly negligible in the signal band, the signal may indeed contain significant out-of-band power, particularly if the resolution of $v(k)$ is but a few bits. If the resolution of $v(k)$ is low, we must interpolate $o(k)$ in magnitude, such that $p(k)$ is suitable for DT/CT conversion and subsequent CT analog signal processing. This interpolation must obviously be performed using discrete-time analog signal processing (DTASP), which therefore is an inherent part of single-bit delta–sigma D/A conversion. The out-of-band portion of $o(k)$ may consist primarily of $t(k)$, but may also contain residual higher-order spectral replicas of $x(k)$, the suppression of which in the interpolation process is often relaxed due to the subsequent masking by $t(k)$.

Multibit delta–sigma modulation. As discussed above, the use of DTASP is imperative when $v(k)$ is of low resolution. The relatively high thermal noise floor and power consumption associated with DTASP, however, is often a considerable (sometimes even unacceptable) trade-off for the low circuit complexity and robustness that characterizes single-bit delta–sigma DACs. The only viable way to avoid the use of DTASP is to increase the resolution of $v(k)$ and use a relatively high oversampling ratio (32 or higher).

Figure 22.24 shows the typical topology of a multibit delta–sigma DAC system not using DTASP. The sample–to–sample variations in $v(k)$ must be small enough to facilitate the use of continuous–time analog signal processing (CTASP) implemented by active circuitry. Based on the above discussion, we may thus conclude that the resolution (in levels, not bits) of $v(k)$ should be at least $\mathrm{OSR}/\pi > 10$.

We rely on CTASP to suppress not only the residual spectral replica images of $v(k)$, but also the added truncation signal $t(k)$, all of which are present in

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[4] We here tacitly assume that the signal transfer function (STF) is unity. The result is nevertheless universally valid because the STF can be referred to the interpolation filter.

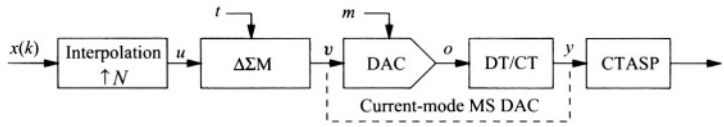


Figure 22.24. Multibit delta–sigma DAC system not using DTASP.

$y(t)$. The specifications of the CT filter can be quite difficult to meet for low OSRs, because the PSD of $t(k)$ will increase very rapidly just outside the signal band, and hence the filter's transition band need be very narrow.

We observe that the signal-band performance is limited by the mismatch–induced noise $m(k)$ (represented by the traces a and b), whereas the out-of-band spectral composition is dominated by the truncation signal $t(k)$ (represented by trace c). This observation is generic for essentially all well-designed multibit delta–sigma DAC systems, when the resolution of $v(k)$ is low to moderate (say, 6 bits or less).

High-resolution oversampled D/A converters. If the DAC's dynamic range is more important than its peak SNR, it is advantageous to increase the resolution of v as much as possible. This is because the noise power induced by clock jitter in the DT/CT conversion process is approximately proportional to the power of $p(k)$, which will be large even for small $x(k)$ unless $t(k)$ is also small, that is, unless $v(k)$ is of high resolution. DACs with a dynamic range of more than 110dB, which are to be driven by consumer-grade, low-cost, crystal-based oscillators, may require that the resolution of $v(k)$ be as high as 8–10 bits, which only recently has become feasible to do [20]. (Notice that the required low thermal noise level generally is not practically feasible for DACs using DTASP; the power consumption would be enormous.)

Now when mismatch-shaping DACs of 10 bits and even higher resolutions can be implemented at low cost and complexity (as discussed below), we once again find ourselves in a situation where evolution has fundamentally changed the constraints within which oversampled D/A converter systems can be designed. New advantageous trade-offs can be made. Again referring to Figure 22.24, we note that the fundamental advantage of using high-resolution signal representation throughout the system is that the added truncation signal's overall power $\overline{|t(k)^2|}$ can be made comparable to, or even less than, the mismatch-induced error's power $\overline{|m(k)^2|}$. Because both signal's are noise-like and $\overline{|t(k)^2|} \leq \overline{|m(k)^2|}$, we conclude that it is not necessary or advantageous to spectrally shape $t(k)$ to a greater extent than $m(k)$ can be spectrally shaped; a simple first or second-order delta–sigma modulator will suffice for nearly all practical purposes.

The overall powers of $t(k)$ and $m(k)$ can generally be made so small that only rarely will it be necessary to suppress subsequently either signal. Analog-domain filtering is required only if we need to suppress further the sampled signal's spectral replica images; that is, to the extent the signal can be sufficiently oversampled, the analog filter can be replaced by interpolation in the digital domain.

In conclusion: when using high-resolution D/A converters, the need for analog-domain signal processing is reduced to the lowest possible level; it is no longer a required step to overcome imperfections associated with the D/A conversion itself. We have to the extent possible traded off digital circuit complexity for analog circuit complexity.

22.4.3. High-Resolution Mismatch-Shaping D/A Converters

The complexity of unit-element mismatch-shaping DACs is exponentially related to their resolution in bits, and they are therefore not suitable for D/A conversion of signals of more than 5 or perhaps 6 bits of resolution. To facilitate a simple one-step D/A conversion of high-resolution signals, we must consider implementations based on adding signals from an array of scaled analog sources. The big question is how we can address these DAC elements to obtain mismatch-shaping operation.

A fresh look on mismatch shaping. Mismatch-shaping is essentially all about encoding the signal $u(k)$ that is to be D/A converted. In a traditional binary-weighted DAC; for example, we encode $u(k)$ into a set of binary bit signals $u(k) = v_0(k) + v_1(k) + \cdots + v_N(k)$, where $v_0(k)$ is the most-significant bit of $u(k)$ and $v_N(k)$ is the least-significant bit of $u(k)$. (Notice that scaling is included in the bit signals, for example, they may respectively attain only the values: 0/1, 0/2, 0/4, 0/8, etc.) The bit signals are D/A converted individually and linearly using binary DACs with the same nominal gain K, and their outputs are added to generate the analog signal $o(K)$ that nominally has the value $K \cdot u(k)$. It is well known that harmonic distortion will result if just one of these DACs (say, the DAC converting $v_i(k)$) has a gain which is not exactly the nominal value. More precisely, the error signal induced by one DAC's gain mismatch equals $\Delta K_i \cdot v_i(k)$, which is nonlinearly related to $u(k)$ precisely because $v_i(k)$ is nonlinearly related to $u(k)$.

Now consider a similar, but more general, DAC system where $u(k)$ somehow is separated into a set of (not necessarily binary) subsignals $u(k) = \sum v_i(k)$, which again are D/A converted individually and added in the analog domain. By negating the above observation for binary-weighted DACs, we find that the DAC system will be insensitive to the mismatches of the individual DACs'

gains if, and only if, each of the subsignals are *linearly* related to $u(k)$. The requirement can be expressed as follows:

$$u(k) = \sum_i v_i(k) \tag{22.18}$$

where for all i, $v_i(k) = \mathcal{L}_i\{u(k)\}$, $\mathcal{L}_i$ are linear functions. Unfortunately, this does not lead to DAC systems of any particular interest. However, if we consider a somewhat similar requirement:

$$u(k) = \sum_i v_i(k) \tag{22.19}$$

where for all i, $v_i(k) = \mathcal{L}_i\{u(k)\} + t_i(k)$, where $\mathcal{L}_i$ are linear functions and $t_i(k)$ are noise-like signals with only negligible power in the signal band, we find that it is precisely the foundation on which most mismatch-shaping DACs are based. For example, for all unit-element DACs we find that $\mathcal{L}_i\{u(k)\} = u(k)/M$, where M is the number of unit elements. If one of the DAC's gain is mismatched, we may calculate the thereby induced error as

$$\Delta K_i \cdot \frac{u(k)}{M} + \Delta K_i \cdot t_i(k) \tag{22.20}$$

The first term merely reflects a slight change in the DAC system's overall gain (which is a linear error that generally is not of concern), whereas the second term is part of the system's mismatch-induced, noise-like error signal $m(k)$ (see Figure 22.24).

In unit-element DACs, each of the subsignals are binary and therefore linearly D/A converted using single-bit DACs. Hence, only gain mismatch errors of the type represented by equation (22.20) will be induced (besides a trivial offset). In the more general situation where $v_i(k)$ may be multibit signals, we must also require that each subsignal be converted linearly. This requirement can be fulfilled quite easily by using mismatch-shaping DACs for the conversion of each subsignal. A set of noise-shaped errors will thereby be induced in addition to the gain errors represented by equation (22.20). A thorough analysis of such systems verifies that all errors induced by mismatches in such DAC systems will be noise-like and have only negligible power in the signal band [22]. In other words, the DAC system is a mismatch-shaping one.

Practical implementations. The main issue at this point is how can we easily and most effectively separate $u(k)$ according to equation (22.19). Assuming that the subsignals will be D/A converted by unit-element DACs, we must also require (for low circuit complexity) that each subsignal be of relatively low resolution.

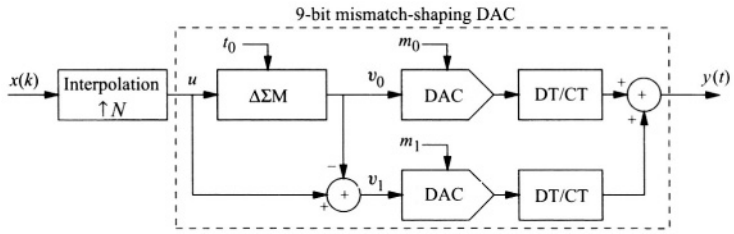


Figure 22.25. A simple segmented mismatch-shaping D/A converter system.

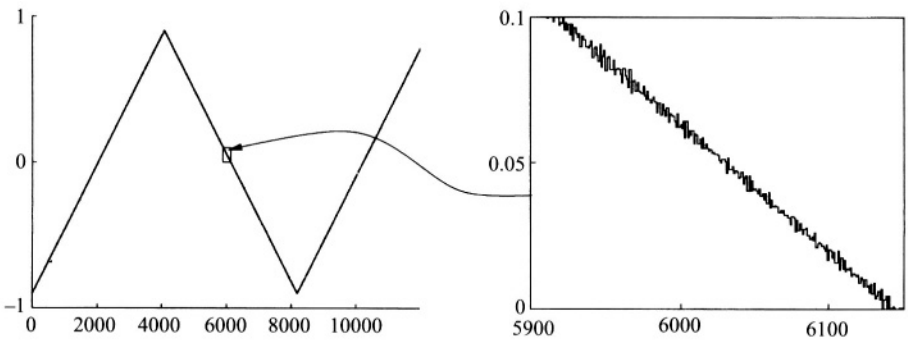


Figure 22.26. Output waveform generated by a high-resolution mismatch-shaping DAC converting a highly-oversampled sawtooth signal.

If we consider the operation of the delta–sigma modulator in Figure 22.24 (still assuming that STF(z) = 1), we observe that it implements

$$v(k) = u(k) + t(k) \tag{22.21}$$

which is very similar to equation (22.19) for $v(k) = v_0(k)$, $u(k) = \mathcal{L}_0\{u(k)\}$, and $t(k) = t_0(k)$. Hence, in the very simplest case, we may separate $u(k)$ into two parts according to equation (22.19) by simply choosing $v_0(k) = v(k)$ and $v_1(k) = u(k) - v(k) = -t(k)$. Notice that $0 = \mathcal{L}_1\{u(k)\}$ is a linear function (the null function). We know that the magnitude of $t(k)$ largely is proportional to the LSB of $v(k)$. Hence, using a conservatively designed delta–sigma modulator, we may separate a 9-bit signal $u(k)$ into two 5-bit signals $v_0(k)$ and $v_1(k)$ [20,21]. This most useful concept is shown in Figure 22.25. When comparing Figures 22.24 and 22.25, we observe that the extra 5-bit unit-element mismatch-shaping DAC is effectively an advantageous trade-off for the generally more complex and power-consuming CTASP block.

Generally, the interpolation process will yield a signal $u(k)$ of resolution higher than 9 bits. To overcome the difficulty of interfacing the two blocks, we

may either use an extra delta–sigma modulator to truncate $u(k)$ to the appropriate resolution [16], or generalize the mismatch-shaping DAC's topology to accommodate signals of arbitrarily high resolution [21]. The latter approach is very attractive when $-t_0(k)$ is separated into a set of 3-level subsignals $v_1(k)$, $v_2(k), \ldots, v_N(k)$, which are particularly simple to D/A convert. The details of how to implement this and many other practical encoders can be found in [21,22].

Figure 22.26 shows the output waveform generated by a high-resolution mismatch-shaping DAC without any subsequent analog-domain signal processing. The input signal is a highly-oversampled digital sawtooth signal. Notice the small magnitude of the mismatch-induced error signal (the random mismatch of full-scale analog sources is here in the order of 0.1%); subsequent filtering is clearly not necessary to reconstruct the signal's waveform.

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Chapter 23

POWER-CONSCIOUS DESIGN OF WIRELESS CIRCUITS AND SYSTEMS

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23.1. Introduction

Power consumption is perhaps the major engineering concern in the design of mobile wireless devices. User expectations of what they will accept as mobile in terms of weight and volume have sharply risen in the last few years, spurred on by advances in consumer devices such as portable tape recorders and CD players, notebook computers and PDAs and mobile telephones. Weight and physical volume principally determine whether a device may be called "mobile", but it must offer sophisticated features as well.

To prolong the time between battery recharge, mobile telephones must use power-conscious ICs for RF, baseband and DSP, supervised by sophisticated power management algorithms. However, as human speech is highly redundant and time-inefficient, devices such as mobile telephone which support this form of communication fundamentally do not make the best use of the energy source which powers them. At a minimum, the ideal continuously "online" communicator should be capable of receiving brief messages in an efficient binary format, and like that other familiar electronic device, the wristwatch, it should be wearable on the human body, and should worry its user least on the state of charge of its battery. The radio pager, which predates the mobile telephone, is one such device. Another is the wireless transceiver attached to a remote sensor, which must communicate a possibly seldom-occurring event to a command center. These two examples have much in common, although pagers are often receive-only, while sensor communicators are usually two-way.

A new generation of wireless paging receivers is now approaching this ideal shape and size. Entire receivers are built into a wristwatch, where the antenna consists of a filament of wire embedded into the bezel.

The energy storage element, the battery, almost entirely determines the final volume and weight of the wireless communicator. Low instantaneous and average receiver power consumption is, therefore, the most important way to miniaturization. Transceiver architecture and circuit design determine *instantaneous* power consumption, whereas *average* power consumption

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depends mainly on good power management and sensible communication protocols.

Paging receivers consume minute amounts of current. For instance, a state of the art receiver operating in the 930 MHz band is powered from a single AAA cell, which lasts up to many months. The receiver can detect signals as low as $1\,\mu V$. It comes as something of a surprise, then, that although in the same frequency band as what mobile telephones use today, and almost the same minimum detectable signal, the power consumption of the paging receiver is at least 10× lower than the best receivers used in cellular telephones. The question is: How? What is special about the paging receiver, or the technologies it uses, that result in order-of-magnitude greater energy efficiency compared to a voiceband wireless receiver? That is mainly the subject of this paper.

To fulfill the vision of communication "anytime, anywhere", the mobile telephone will fulfill a certain function. However, ultralow power wireless devices capable of at least receiving messages may be embedded into a mobile telephone, which may actually be used for short e-mails. This two-tier approach will likely succeed but devices small enough to be worn like a wristwatch will supplement it.

There is another class of wireless communicators, perhaps not as widely used as telephones which operate at similar radio frequencies, but whose power consumption must be 10–50 × lower. These communicators often work at a low duty cycle, but they must be dependably available over many months without battery replacement or recharge. The radio-paging receiver is one example. A 900 MHz FLEX paging receiver operates for periods as long as six months from a single AAA-size cell. Like any wearable electronic device such as a wristwatch, the user need not be concerned with the state of the battery for long periods of time. Wireless communicators built into implantable biomedical devices, or in miniature remote sensors, must also be very low power. This class of wireless device must also often operate at low voltages such as 0.9V, which is the lower limit of useful life for certain common batteries.

This paper describes circuit techniques and radio architectures that have been discovered in the course of recent research which enable the power consumption of RF, IF, and baseband building blocks to be lowered by orders of magnitude in integrated wireless communicators. It does not cover other important ways to lower power consumption, such as signaling schemes, protocols and power management. A total low power design must intelligently use all these techniques.

An understanding of the principles and practice of low power techniques is expected to not only benefit the circuits in existing mobile wireless devices such as cellular telephones, it holds the potential to practically realize an altogether new class of wearable communicator which makes wireless ubiquitous in ways that have so far only been imagined.

23.2. Lowering Power across the Hierarchy

A low power *system* is the result of comprehensive power awareness cutting across the entire hierarchy of a system. In a communication device, this hierarchy descends from the system definition, signaling protocols and choice of modulation, through architecture of the receiver and transmitter, to the transistor-level circuits comprising the RF and IF analog circuits and baseband DSP. It is easy to speak of these concepts in the abstract, but difficult to illustrate them with a specific example of an operational system. Fortunately, there exists a good example in the world of wireless paging: the evolution of the POCSAG paging system into today's FLEX [1].

The POCSAG paging protocols was introduced in the UK in the 1970s, and served for many years as the paging standard there, in the US, and in many other countries of the world. It transmits data at 100b/s using binary frequency-shift keying of the carrier. Most POCSAG transmissions are broadcast from strong transmitters in the 200 or 400 MHz bands. As paging use grew, there arose the need for bandwidth-efficient modulation and higher data rate to enable a greater number of users to receive messages more frequently. This has led to the development of the FLEX paging protocol.

For higher throughput, FLEX uses 4-FSK modulation enabling the data rate to step up from 100 b/s to 1.1 kb/s. The most significant advances over POCSAG are at the system level [2,3]. Data frames rely on time-synchronized reception. Internal clocks synchronize the operation of all receivers within range of a particular transmitter to 5 μs or better. This means that compared to asynchronous reception in POCSAG, where data frames must contain preambles long enough for any given receiver to wake up randomly and then synchronize, the preamble in FLEX may be much shorter. Synchronization also means that receivers may be powered down for multiple frames at a time. The radio section contains enough logic to decode the address field, and a FLEX receiver only powers up the microcontroller when it has recognized its own address.

Together, these techniques lower a FLEX receiver's power 10 × over a POCSAG receiver, while using the *same* RF circuits. This proves that good system planning can extend battery life by an order-of-magnitude without evolution in RF circuits.

The right modulation scheme, too, helps to lower power dissipation. For instance, on–off keying (OOK) or amplitude-shift keying (ASK) need only a threshold detector, which is simple to construct and consumes low power. Low-end applications such as wireless remote keyless entry use these modulations in simple, ultralow power transceivers [4]. However, the transmitted signals are susceptible to additive noise or interference. Wideband frequency-shift keying (FSK) is less susceptible, but requires a frequency discriminator for demodulation. As the peak energy in its frequency spectrum lies on either side

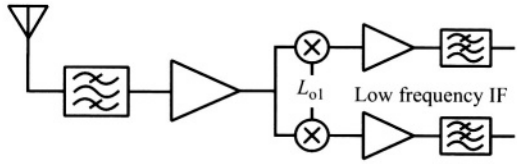


Figure 23.1. Direct conversion receiver.

of the carrier frequency away from the center, it is well suited to a zero-IF direct-conversion receiver [5]. Flicker noise and DC offset in baseband circuits may be suppressed by AC coupling without removing valuable signal spectrum.

The direct conversion receiver (Figure 23.1) is most amenable to full integration on a single chip. It requires no image-reject filter, and only a minimum RF section comprising a low-noise amplifier (LNA) and two mixers. All subsequent amplification and filtering takes place at low frequencies, close to DC, at the price of duplicating circuits in quadrature branches. The power consumption of an active channel-select filter is least when the channel of interest lies at a low frequency [6]. As the active filter is often one of the largest consumers of power [7], zero IF is the clear choice in this respect.

23.3. Power Conscious RF and Baseband Circuits

This section explores the fundamental limits on power dissipation in many of the building blocks in a wireless receiver. The receiver must usually be more power conscious than the transmitter, which in the messaging-type communications is seldom invoked.

23.3.1. Dynamic Range and Power Consumption

The fundamental lower limit to a circuit's power consumption is tied to its performance. For circuits in the signal chain of a wireless receiver, the main specification is on spurious-free *dynamic range.* In decibels, this is proportional to the difference between the 3rd-order intercept point and the noise floor as measured at the receiver output, then referred to the receiver input to normalize for gain. Take, for example, the simple circuit consisting of two common-source MOSFETs driven with balanced input signal voltages, and producing output currents that are differentially sensed (Figure 23.2(a)). The dynamic range is limited at the lower end by the voltage noise spectral density integrated across the channel bandwidth, and at the upper end by the large signal swing that distorts gain and defines the intercept point. The equivalent input noise voltage density is $\hat{v}_n^2 = 4kT\,\gamma/g_m$ where kT is a physical constant and γ is a noise factor associated with the FET channel length and bias [8].

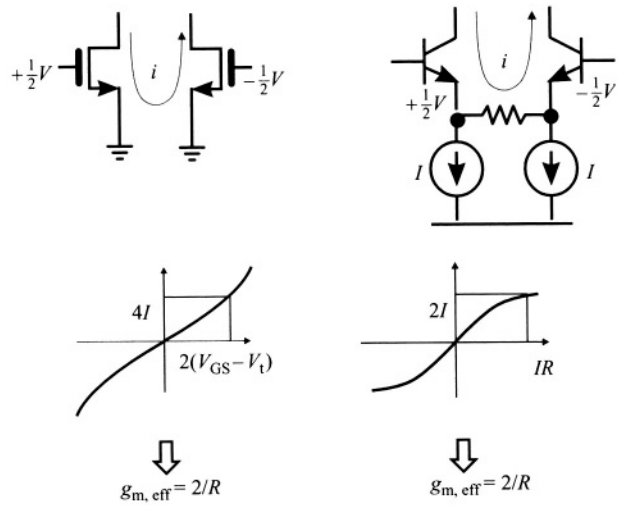


Figure 23.2. Comparsion of degenerated bipolar and MOS large-signal transconductors, designed for the same gain compression point.

If the FETs obey the pure square law characteristics, this circuit is a perfectly linear large signal differential transconductor. Its input–output characteristic distorts significantly when the signal swing shuts off one of the FETs. If this were the only distortion, however, the circuit would show infinite 3rd-order intercept at small signal well below the shut-off condition. In fact, this is not so. Gate electric field dependence of inversion layer mobility introduces a small 3rd-order nonlinearity that defines a finite intercept point even at small test signals [9]. The governing equation is:

$$I_D = \frac{W}{2L}\frac{\mu_0}{(1+\theta V_{eff})}C'_{ox}V_{eff}^2 \tag{23.1}$$

where $V_{eff} = V_{GS} - V_t$. The 3rd-order intercept for a single 0.5-μm NMOSFET simulated using the Philips MOS 9 model fits well with the intercept point this equation predicts with $\theta = 0.1\ V^{-1}$ (Figure 23.3). Roughly speaking, a higher intercept point in dBm calls for an almost proportionally larger bias V_{eff} in volts. Therefore, in an *open-loop* circuit as used in the RF and IF sections, a given dynamic range fixes the FET's g_m and V_{eff}. Now, assuming that the *I–V* characteristics roughly conforms to the classic square law, the bias drain current in saturation is

$$I_D = \frac{1}{2}\mu C'_{ox}\frac{W}{L}V_{eff}^2 = \frac{1}{2}g_m V_{eff} \tag{23.2}$$

This leads to the very important conclusion that in open-loop small-signal circuits such as amplifiers, mixers and active filters, the specification on *dynamic*

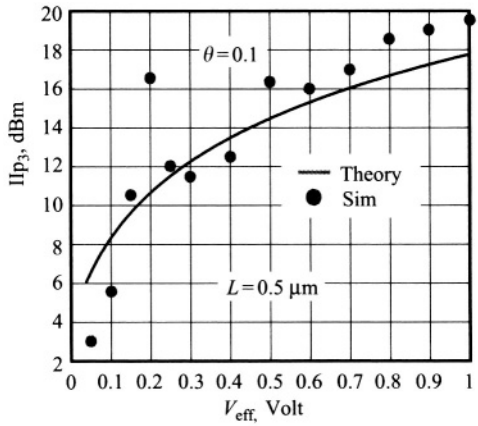


Figure 23.3. Simulated IIP3 of a MOSFET compared with analytical expression, as a function of effective gate voltage, $V_{\text{eff}} = V_{\text{GS}} - V_{\text{t}}$.

range determines current drain, independently of the FET channel length and technology scaling! With good design, the actual current consumption of an amplifier can approach this limit. Therefore, on fundamental grounds a system employing very low power receivers must relax requirements on dynamic range. Alternatively, when the noise spectral density is large because of low bias current, the system may improve sensitivity by using narrowband channels, that is, low data rates.

This relationship also holds true for bipolar transistor (BJT) circuits. The intrinsic input-referred IP3 of an ideal BJT is –12.7 dBm at any bias voltage. Just as greater V_{eff} at bias extends a FET's capability to amplify large signals with low distortion, so resistor degeneration linearizes the BJT (Figure 23.2(b)) and raises its intrinsic IP3. The degeneration voltage, $I \times R$, determines the maximum input voltage at the onset of gain compression, while the input-referred voltage noise is $4kT\Gamma R$, where Γ is some noise factor. As R sets the lower end of dynamic range and IR the upper end, the current drain is once again fixed.

In fact, a degenerated bipolar differential pair gives the same transconductance per unit bias current as the MOSFET transconductor, when both are designed for equal linear full-scale (Figure 23.2(b)).

23.3.2. Lowering Power in Tuned Circuits

Strictly speaking, the link between current consumption and dynamic range described above applies to baseband or wideband circuits.

Now consider an inductor degenerated differential pair, where the resistor in Figure 23.2(b) is replaced by an inductor. As the feedback inductor is

noiseless, the input-referred noise voltage is the same as the original differential pair but the degeneration extends the linear range. Reactive degeneration thus decouples dynamic range from power consumption. This benefit from the inductor is, however, frequency dependent. Degenerating reactance is lower with frequency, and at high frequencies is limited by the onset of resonance with whatever device and parasitic capacitance appears across it. This technique has been used in some RF circuits, such as transformer-coupled stages [10].

23.3.3. Importance of Passives Quality in Resonant Circuits

The quality factor of passive tuned circuits can profoundly influence the circuit power dissipation. As a starting point, consider a low-noise amplifier whose input port impedance is *not* to be impedance matched.

First, the amplifier must provide sufficient gain in the frequency band to which it is tuned. Suppose the input capacitance C of the next stage is known and fixed. Then the load inductor (L) is chosen to resonate with C in the narrow frequency band of interest. The resulting peak voltage gain is $g_m Z_0$, where Z_0 is the tuned circuit's impedance at resonance. This impedance is usually limited by the inductor quality factor, Q, and given by $Z_0 = Q(\omega_0 L) = Q/(\omega_0 C)$. The voltage gain is thus $Qg_m/(\omega_0 C) = 2QI/(\omega_0 C V_{eff})$. To lower power dissipation, if the amplifier FET is scaled down in width, then g_m and the voltage gain will also scale down, unless Q of the inductor is raised to compensate. Figure 23.4 illustrates a specific case of a 22 nH inductor tuning a common-source amplifier to 930 MHz while driving a capacitor load. For various inductor Qs, the width of the FET (length fixed at $0.25\ \mu m$) is scaled to obtain 20 dB voltage gain. Bias V_{eff} is fixed at 200 mV to define a constant large-signal V_{GS} handling capability at the FET input port.

If the 22 nH inductor is fabricated on-chip with a Q of, say 3, the FET must be biased at 3.3 mA. On the other hand if the Q were 20, the required bias current at that gain falls to 0.5 mA, resulting in a 6.6× reduction in power. Therefore, use of high quality inductors lowers the power dissipated in tuned RF circuits, a fact that has also been noted elsewhere [11]. Although an inductor with this large a Q cannot be integrated today as a spiral in a standard IC process, it may be an off-chip discrete component, or it may be fabricated in some specialized technology [12,13].

Discrete wire-wound chip inductors are most commonly used at RF and microwave frequencies [14,15]. The inductor consists of a solenoid of high conductivity metal wire wound on a ceramic header, or lately with an air core. Inductance as large as 100 nH may be fit into a "chip" about 1 mm on a side

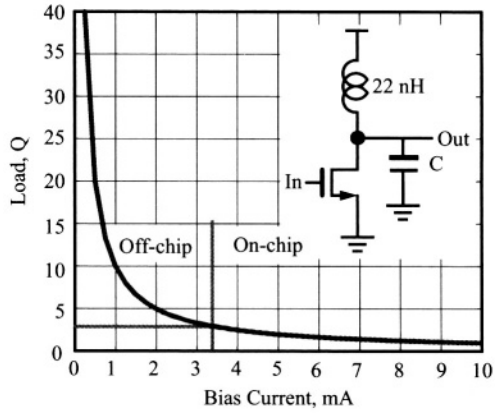


Figure 23.4. Bias current versus inductor Q for a simple amplifier at constant gain.

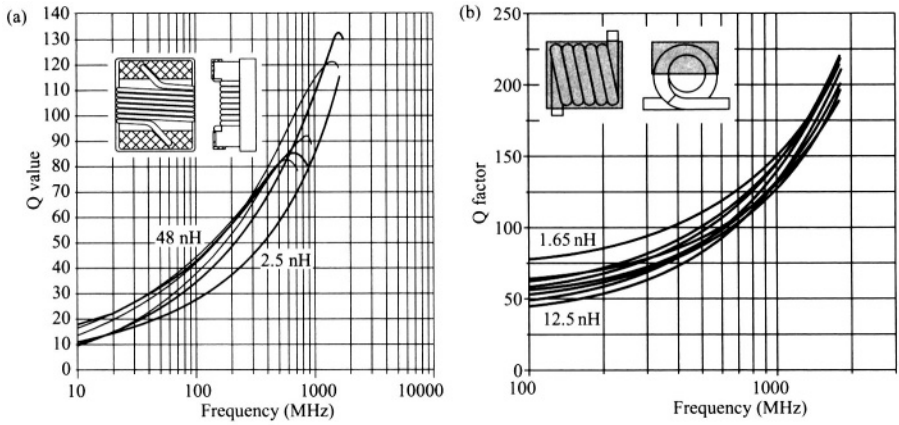


Figure 23.5. Discrete surface-mount chip inductors, (a) ceramic core, (b) air core: physical structure, and typical Q vs frequency. (Courtesy Coilcraft Corporation.)

(Figure 23.5). The small size lowers the parasitic capacitance across the inductor, extending its self-resonant frequency and the highest attainable Q. For example, a representative 68 nH chip inductor gives a Q of 60 at 1 GHz.

Every signal line on an integrated circuit connecting to an off-chip component suffers loading by parasitic capacitance and loss due to the bond pads, bondwire inductance, and the inductance and capacitance of package leads and PC board traces. The parasitics are usually large compared to the on-chip reactances, and they do not shrink with transistor scaling. Mounting bare die with solder balls on to ceramic substrates (the flip-chip technique) cuts down on many of these parasitic reactances. It is also possible to fabricate planar spiral

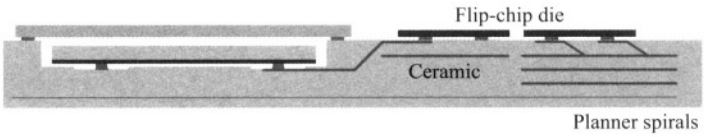


Figure 23.6. Ceramic substrate with embedded printed spiral inductors, and flip-chip die attach.

inductors using thick, low-loss metal traces on, or within, the ceramic substrates (Figure 23.6); the latter multi-layer technology is called low-temperature co-fired ceramic (LTCC) [16]. This approach has been successfully used in ultralow power wireless transceivers associated with wireless sensors [11].

On-chip, a grounded shield under the bond pad substantially eliminates substrate loss [17]. For effective shielding, the grounded layer under the pad may have to be connected to off-chip ground with multiple bond wires. Now the pad appears almost purely capacitive, and the remaining parasitics are mainly reactive and lossless.

There are repercussions to using off-chip tuning elements. With inaccurate estimates of the parasitics or because of spreads in their values, a circuit node with a high loaded Q is susceptible to frequency detuning. If the resulting variation in gain due to spreads is to be kept below, say, 1 dB, then the loaded Q at that node must not be too large. Using the classic 2nd-order frequency response of an LCR circuit, this upper limit on loaded Q is

$$Q < \frac{1}{4(\Delta\omega/\omega_0)} = \frac{1}{2\sqrt{(\Delta L/L)^2 + (\Delta C/C)^2}} \tag{23.3}$$

The active device attached to this resonator must consume a minimum current to provide the required gain. One way to circumvent this limitation is to allow a higher Q, but compensate for spreads with some form of active tuning. For example, following auto-calibration a digital word can switch an array of small binary-weighted capacitors to re-tune a resonant circuit to the desired frequency.

23.3.4. Low Noise Amplifiers

A low noise amplifier must be matched at the input port to some characteristic impedance such as $50\,\Omega$. The first candidate for the LNA is the common-gate amplifier circuit degenerated by an inductor, L_S (Figure 23.7). Its input impedance is matched by resonating the net capacitive reactance of C_{GS} and L_S in series with a gate inductor, L_G [18]. The Q of the matching network amplifies the input voltage, and in the absence of any other losses this produces the LNA

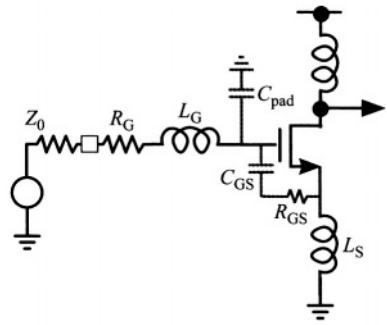


Figure 23.7. Narrowband common-source amplifier with inductor degeneration. Various parasitics are also shown.

noise factor [19]:

$$F = 1 + \gamma g_m Z_0 \left(\frac{\omega_0}{\omega_T}\right)^2 \tag{23.4}$$

At first sight this suggests that if FET g_m, and therefore its size and bias current are shrunk, and at the same time the matching network is adjusted to maintain impedance match, then this will result in the lowest noise *and* a bias current approaching zero. Potentially, this is of great value in a low power receiver.

However, by neglecting other forms of loss this limiting case is seriously in error. Series resistor R_G representing loss in the gate inductor L_G, and the inversion layer resistance R_{GS} of the MOSFET, which is a fundamental loss, both scale *up* as the LNA MOSFET shrinks in size. When they are equal to the source impedance Z_0, the LNA noise figure is 3 dB. As the FET is scaled down further, the noise figure worsens. This implies an optimum FET size for least noise figure. Taking into account these losses, the noise factor is

$$F = 1 + \frac{R_{GS} + R_G}{Z_0} + \frac{\gamma}{g_m Z_0 Q^2} \tag{23.5}$$

Q is the quality factor of the input-matching network. The main advantage of the inductively degenerated LNA is that it can achieve a low noise figure limited by the ratio of the unity current gain frequency (ω_T) to the band of operation (ω_0). There is no guarantee, though, that this optimum lies at a low bias current.

Suppose a receiver needs an LNA with 3-dB noise figure, but with lowest possible power consumption. To simplify the analysis, assume L_g is a very low loss external inductor so that the loss at the input port is mainly due to the inversion layer resistance, R_{GS} in series with C_{GS}. It has been shown that $R_{GS} \approx 1/(5g_m)$ [19,20]. It is a reasonable assumption when the FET size is

aggressively scaled down for low power that R_{GS} is the main contributor to noise figure. To justify this, the expression for noise factor is re-cast as follows, where $\omega_0 < \omega_T$ always.

$$F = 1 + \frac{R_{GS}}{Z_0} + 4\gamma g_m Z_0 \left(\frac{\omega_0}{\omega_T}\right)^2 \simeq 1 + \frac{R_{GS}}{Z_0} \tag{23.6}$$

For LNA noise figure of 3dB, that is $F = 2$, choose $R_{GS} \simeq Z_0$. Then the relation between R_{GS} and g_m specifies the current consumption:

$$I_D = \frac{g_m V_{eff}}{2} \approx \frac{V_{eff}}{10R_{GS}} \simeq \frac{V_{eff}}{10Z_0} \tag{23.7}$$

This estimate of current consumption is based only on consideration of noise figure. However, a practical receiver also specifies a minimum LNA dynamic range. Of concern here is the Q of the matching network, which amplifies the incident voltage. This lowers the input-referred 3rd-order intercept point of the LNA ($\mathrm{IIP3_{LNA}}$) relative to the 3rd-order intercept point of the FET ($\mathrm{IIP3_{FET}}$), as follows:

$$\mathrm{IIP3_{LNA}} = \mathrm{IIP3_{FET}}/(V_{gs}/V_{in})^2 = \mathrm{IIP3_{FET}} \times (g_m Z_0)^2 \left(\frac{\omega_0}{\omega_T}\right)^2 \tag{23.8}$$

Third-order nonlinearity in a FET arises from field-dependent mobility, and $\mathrm{IIP3_{FET}}$ in dBm is roughly proportional to V_{eff}. Therefore, LNA dynamic range ($\mathrm{DR_{LNA}}$) is given by the following expression, which shows that at constant impedance match, the dynamic range is proportional to the bias current of this amplifier.

$$\mathrm{DR_{LNA}} \propto \mathrm{IIP3_{LNA}}/(F-1) = \frac{g_m Z_0}{\gamma}\mathrm{IIP3_{FET}} \propto \frac{g_m Z_0}{\gamma} V_{eff} = \frac{2IZ_0}{\gamma} \tag{23.9}$$

Thus, stronger reactive feedback merely *slides* the dynamic range by lowering noise figure and intercept point together. The only remaining possibility to lower current at a given dynamic range is by raising the LNA input impedance.

A common-gate amplifier with transformer feedback may be similarly configured for impedance match and low noise [21] (Figure 23.8). Assuming $g_m Z_0 \gg 1$, the feedback circuit sets the insertion voltage gain (s_{21}) and input impedance:

$$\begin{aligned} s_{21} &= M \\ Z_{in} &= Z_0 \text{ if } N = M^2 - M - 1 \end{aligned} \tag{23.10}$$

At impedance match, the noise factor of the amplifier is:

$$F = 1 + \frac{\gamma}{g_m Z_0} \tag{23.11}$$

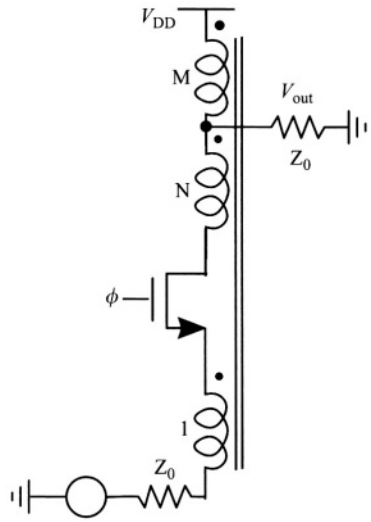


Figure 23.8. Wideband common-gate amplifier with transformer feedback.

The noise figure may be lowered towards 0 dB by raising $g_m Z_0$, until, like the inductively degenerated amplifier, it is limited by parasitic losses which scale adversely. However, large g_m is usually not consistent with low current consumption. Also, the termination resistor Z_0 itself must be low noise, for instance implemented at the input terminals of a transimpedance amplifier. Because it is difficult to realize transformers on-chip, this circuit topology is rarely used in integrated LNA's. Transformer coupling remains interesting because the zero DC voltage drop across inductors enables operation at low supply voltage. This is evident in the few integrated LNA's with transformer-coupling reported to date [10,22].

Next consider a simple common-gate amplifier (Figure 23.9(a)), whose noise factor is $(1 + \gamma)$ at impedance match [17]. FET g_m sets the input resistance, large signal handling determines the gate overdrive V_{eff}, and together these two factors specify the bias current. To circumvent this constraint the LNA may be designed with a higher than wanted input impedance $(Z_1 > Z_0)$, which implies a lower bias current, and then it may be scaled to the required value (Z_0) at the amplifier input with a reactive impedance transformer (Figure 23.9(b)). The transformer may be a simple LC narrowband circuit [23] which needs neither coupled magnetic elements nor bias current. The relations governing this approach are as follows, where I_D, g_m, V_{eff} refer to an LNA matched to Z_0 with no transformer, and the same quantities with the prime symbol refer to an LNA whose input impedance is Z_1 instead of Z_0. FET V_{eff} is adjusted to

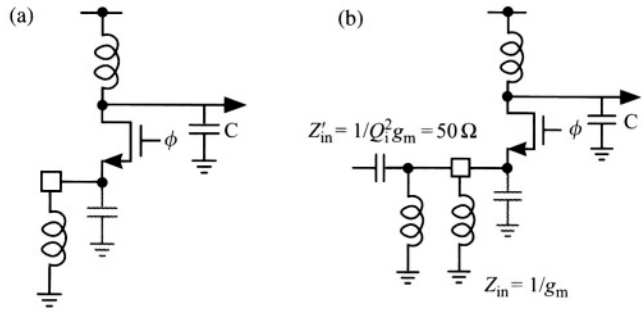


Figure 23.9. (a) Simple common-gate LNA; (b) Low current common-gate LNA with impedance transformer at input port.

V'_{eff} to maintain constant LNA IIP3.

$$
\begin{aligned}
&I_D = \frac{1}{2} g_m V_{eff} = \frac{1}{2}\frac{V_{eff}}{Z_0} \\
&\text{Choose } V'_{eff} = V_{eff}\sqrt{\frac{Z_1}{Z_0}} \text{ for constant IIP3}_{LNA} \\
&I'_D = \frac{1}{2} g'_m V'_{eff} = \frac{1}{2}\frac{V_{eff}}{Z_1}\sqrt{\frac{Z_1}{Z_0}} = \frac{1}{2}\frac{V_{eff}}{\sqrt{Z_0 Z_1}} \\
&\Rightarrow I'_D = I_D\sqrt{\frac{Z_0}{Z_1}}
\end{aligned}
\tag{23.12}
$$

Impedance transformation with modest scale factors is quite feasible in practice. However, when scaling impedance by a large factor, the required quality factor of the matching circuit grows quadratically and is sensitive to parasitics. Including the voltage gain in the matching network, the total LNA insertion gain to the output is:

$$
\text{Gain} = \frac{Q_i g_m Q_0}{\omega_0 C} = \frac{Q_0}{50 Q_i \omega_0 C} \tag{23.13}
$$

where Q_i is the quality factor of the LC matching network at the input port, and Q_0 of the resonant load. Compared to the case of no matching network at the input, a load with higher Q_0 is required to obtain a specified voltage gain. As the input port of the common-gate amplifier is equivalent to a two-terminal resistor of value $1/g_m$ terminating the reciprocal matching network, the LNA noise factor at impedance match remains $(1 + \gamma)$ independent of the voltage gain in the matching network. γ is 0.67 for long-channel FETs,

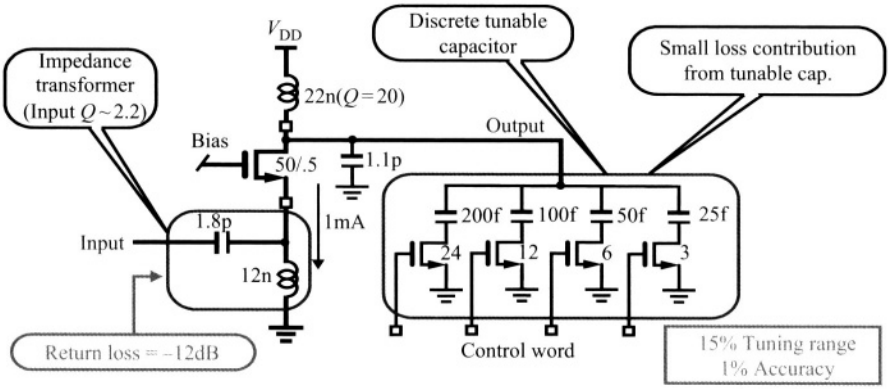


Figure 23.10. Actual implementation of common-gate LNA, including tuning of high-Q load.

which implies an LNA NF of 2.2 dB. γ is higher at short channels [8], and in practice, a typical NF for this LNA is 3 dB. For this LNA to bias at the same current as the inductively degenerated common-source amplifier with 3 dB NF, $Z_1 : Z_0 = 25 : 1$. It may be difficult in practice to realize the required impedance transformer to present Z_0 at the LNA input. Figure 23.10 shows a practical realization of a low current LNA tuned to 900 MHz.

So far, the LNA scaling has been considered with the intent of maintaining a constant dynamic range. However, often two different circuit blocks in a complete receiver chain may determine the upper and lower limits to dynamic range. For example, the LNA may principally determine the cascade noise figure, and the following mixer or some other downstream circuit the intercept point [7,24]. Now it is appropriate to lower LNA noise figure alone, without the consequently lower intercept point becoming a major concern. The common-source LNA with inductor degeneration offers a lower noise figure than the simple common-gate LNA, however accompanied by some practical limitations. A high Q matching network must precede the LNA FET, whose width is small to lower the bias current. The capacitance to ground due to the bond pad and package lead (Figure 23.7), which is much larger than the small FET C_{GS}, significantly alters the real part of the LNA input impedance and disturbs the intended impedance match. This may be corrected by re-tuning the matching network, but in practice the additional branch to ground due to the relatively large parasitic tends to degrade the lowest achievable noise figure.

23.3.5. Oscillators

It is well known that for lower phase noise, oscillators benefit from high Q inductors. In fact, this forms an important part of conventional methodology of

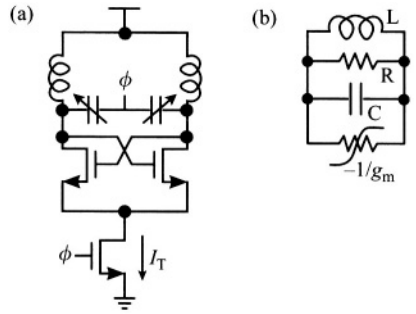


Figure 23.11. (a) Differential LC Oscillator; (b) equivalent circuit.

oscillator design [25]. However, what is not as well understood is the impact of inductor Q on current consumption, when the oscillator delivers a certain phase noise at a given frequency. A complete analysis of oscillator phase noise in some recent work [26] sheds light on this question.

Consider the differential switched current oscillator (Figure 23.11), which is popular in RF-ICs. There are three sources of noise in this circuit: loss in the LC resonator, noise in the switching differential pair, and noise in the tail current source. The ratio of oscillation amplitude to noise determines the oscillator phase noise sidebands. Once oscillation starts, the differential pair switches the tail current, I, into the resonator. The resultant differential amplitude is $(4/\pi)IR$, where R is the parallel loss resistance of the differential inductor. The power supply limits the largest achievable amplitude to $2V_{DD}$ differential, when the tail current source FET shuts off at each negative peak of the oscillation. Least phase noise is obtained when the current is just large enough to reach this amplitude [26,27]. This optimum current is:

$$I_{opt} = \frac{\pi V_{DD}}{2R} = \frac{\pi V_{DD}\omega_0 C}{Q} \tag{23.14}$$

Q is the loaded quality factor of the resonator, usually determined by the inductor. C is the net capacitance in parallel with each inductor. On an integrated oscillator the loading of the following stage often determines C. Clearly, therefore, the larger the inductor Q, the lower the optimum tail current.

However, the question remains how an oscillator with a lower optimum current compares with another oscillator with a higher optimum current, as measured by some meaningful figure-of-merit? One such figure-of-merit is the phase noise $\mathcal{L}(f_m)$ at offset frequency f_m normalized to oscillation frequency

f_0 and to power consumption [28].

$$\text{FoM} = \left(\frac{f_0}{f_m}\right)^2 \frac{1}{\mathcal{L}(f_m) V_{DD} I} \tag{23.15}$$

Analysis of the differential oscillator [26] shows that

$$\mathcal{L}(f_m) = \frac{2FkT}{\left(\frac{1}{2}V_0^2/R\right)} \left(\frac{f_0}{2Qf_m}\right)^2 \tag{23.16}$$

V_0 is the amplitude and F is the noise factor representing, respectively, the contributions of resonator loss, differential pair switches and current source to phase noise, as follows:

$$F = 2 + \frac{8\gamma RI}{\pi V_0} + \gamma \frac{8}{9} R g_{mbias} \tag{23.17}$$

At the optimum bias current, I_{opt}, the figure of merit is then:

$$\text{FoM} = \frac{4}{\pi} \frac{Q^2}{kT} \frac{1}{2 + 4\gamma + \frac{32}{9}\gamma\pi V_{DD}/V_{eff,bias}} \tag{23.18}$$

The FoM improves as Q^2, but depends on little else that is circuit-specific other than V_{eff} in the third term in the denominator. This means that for high-Q resonators, both the optimum current and the normalized phase noise go down together. This is a doubly favorable outcome. In practice, the resonator Q must include varactor loss, and the tuning range should encompass both the frequency band of interest and spreads in parasitics.

If thermal noise in the differential pair and in the current source dominates F, and the tail current drives the differential oscillation amplitude to its largest possible value, $2V_{DD}$, limited by the power supply, then:

$$\mathcal{L}(f_m) = kT \frac{\gamma I}{\pi V_{DD}^2} (\omega_0 L)^2 \left(\frac{1}{V_{DD}} + \frac{2}{V_{eff}}\right) \left(\frac{f_0}{f_m}\right)^2 \tag{23.19}$$

V_{eff} is the effective gate voltage biasing the current source FET. As $V_{eff} \ll 2V_{DD}$, noise in the current source dominates phase noise. Raising V_{eff} lowers current source compliance, causing the highest oscillation amplitude to limit at some value lower than $2V_{DD}$. This worsens phase noise. The equation also shows that at a fixed tail current, I, forces the oscillation amplitude into the V_{DD}-limited regime, the phase noise is independent of inductor Q.

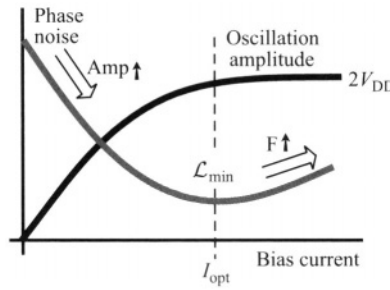


Figure 23.12. Amplitude and phase noise dependence on bias current.

In fact in this regime as the tail current is made larger the phase noise worsens (Figure 23.12). The lowest current to produce the V_{DD}-limited amplitude, $I_{opt} = \pi V_{DD}/2R = \pi V_{DD}/(2Q\omega_0 L)$, produces the least phase noise $\mathcal{L}_{min}$:

$$\mathcal{L}_{min}(f_m) = kT\frac{\gamma}{V_{DD}}\frac{\omega_0 L}{2Q}\left(\frac{1}{V_{DD}} + \frac{2}{V_{eff}}\right)\left(\frac{f_0}{f_m}\right)^2 \tag{23.20}$$

Furthermore, at a given oscillation frequency, the *lower* the (L/Q) ratio of the resonator's inductor, the lower the $\mathcal{L}_{min}$. On the other hand, to lower power with smaller I_{opt} the $(L \times Q)$ product should be *greatest.* In discrete inductors Q is almost independent of L at frequencies in the range of 1 GHz (Figure 23.5). Thus, L should be low for better phase noise $\mathcal{L}_{min}$ but high for low current I_{crit}. For a given Q, phase noise scales down with resonator inductance, that is, inversely with resonator capacitance, but at the optimum bias current is higher.

Two practical realizations of low current oscillators at 800 MHz and 1 GHz are shown, respectively, in Figures 23.13(a) (b). The switched capacitor tuning method [29] in Figure 23.13(b) is a means to cover process variations and resonator spreads with digital control, without using a high swing varactor, which degrades phase noise.

23.3.6. Mixers

The passive commutating switch mixer, consisting of four FETs used as analog switches (Figure 23.14), needs no bias current, which makes it the ultimate low power circuit. However, this mixer is non-unilateral, that is, signals flow bi-directionally from input to output. This poses several practical problems. For example, if this mixer is directly connected to the inductor output node of an LNA, the subsequent amplifier stage may substantially load the inductor. Similarly, two mixers downconverting a common input by quadrature LO phases would tend to load each other's outputs during the overlap period of LO-I and

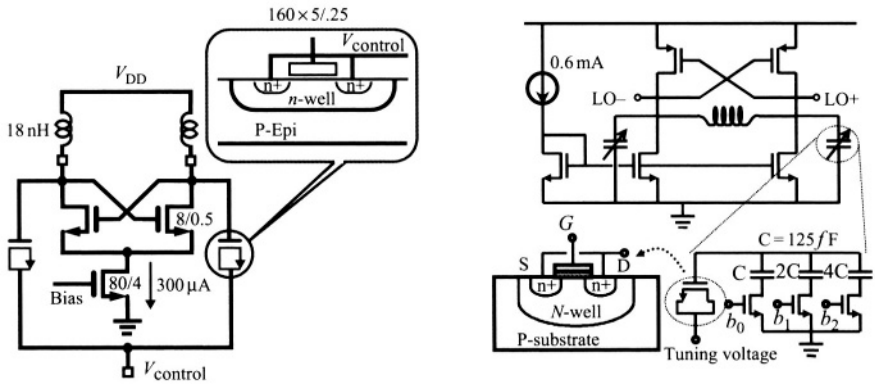


Figure 23.13. Actual low power oscillator circuits. (a) NMOS differential pair switches with MOS varactor for continuous tuning; (b) PMOS differential pair switches with continuous and discrete tuning.

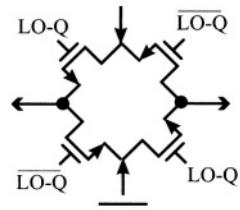


Figure 23.14. Passive FET mixer.

LO-Q when switches turn ON in both mixers. For these reasons unilateral active mixers are preferred in a receiver.

The most straightforward way to lower power dissipation of an active mixer (Figure 23.15) is to scale down FET size. The large signal handling remains unchanged if V_{eff} is held constant for the input transconductor stage, but the mixer noise goes up inversely with bias current. The following expressions gives the total input-referred DSB white noise spectral density of a double-balanced MOS active mixer [30], and compares it with the input IP3 of the mixer:

$$\hat{v}_{\text{on}}^2 = 8kTR\left(1 + \frac{2\gamma IR}{\pi A_{\text{LO}}} + \gamma g_{\text{m}} R\right)$$

$$\text{SSB}\hat{v}_{\text{in}}^2 = \frac{\hat{v}_{\text{on}}^2}{\left(\frac{2}{\pi} g_{\text{m}} R\right)^2} \simeq 2\pi^2 kT \frac{\gamma}{g_{\text{m}}} = \pi^2 kT\gamma \frac{V_{\text{eff}}}{I} \tag{23.21}$$

$$\text{IIP3} \sim V_{\text{eff}}$$

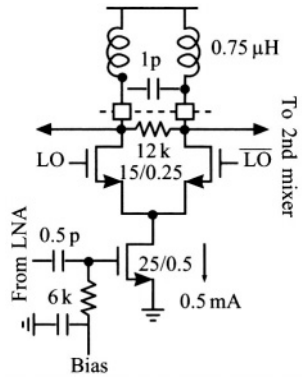


Figure 23.15. Active CMOS mixer example: single balanced.

γ is the FET noise factor and the amplitude of a sinewave LO, A_{LO}, is assumed large enough to completely commutate the mixer switches. The three terms in the expressions for $\hat{v}_{on}^2$ give the output noise voltage due to the load resistors, the mixer differential switches, and the input transconductor stage. As the noise due to the input transconductor stage dominates in most cases, the expression for input-referred noise may be simplified. When compared to the expression for IIP3, this shows that increasing V_{eff} merely slides the mixer dynamic range, that is noise and IP3 go up together. A larger dynamic range requires more bias current. In low-power receivers, the mixer is often the bottleneck to overall IPS.

The LNA insertion gain must be raised to overcome large mixer noise, which once again argues for the use of high impedance, that is, high *Q,* inductors in the LNA load. A differential LNA followed by a doubly balanced mixer rejects common-mode pickup of stray signals and disturbances. On the other hand, a single-ended LNA takes half the power of a differential LNA and it is simple to connect to the antenna. A single-ended LNA output readily drives a single-balanced active mixer, which then produces a differential downconverted output. The subsequent baseband stages may be fully differential.

The main problem in using a single-balanced mixer is that the large LO feedthrough at its output may saturate the following stage. Here, too, an inductor load tuned to the intermediate frequency at the mixer output can attenuate the LO frequency. However, the higher the IF, the sharper the required transition band of the LC filter load to attenuate the LO feedthrough.

It has been said before that the direct conversion architecture is of great interest in low power implementations. However, flicker noise in active CMOS mixers poses a threat to the achievable sensitivity in this receiver, particularly for narrowband channels. This is because the switch FETs (Figure 23.16)

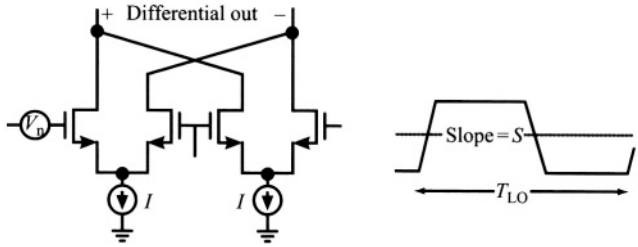


Figure 23.16. Flicker noise equivalent source at mixer switches, and assumed LO voltage waveform.

contribute flicker noise to the mixer output without frequency translation [30]:

$$v_{n,o} = \frac{4IR}{ST_{LO}} v_{n,sw} \tag{23.22}$$

where $\hat{v}^2_{n,sw} \propto 1/(WL)$, $v_{n,sw}$ is the input-referred flicker noise voltage of the switch FETs, IR is the maximum voltage across the mixer's load resistor, S is the slope of the LO voltage at differential zero crossing, and T_{LO} is the LO period. So as not to load the LO buffers and yet to switch quickly, the switch FETs must be of small width and of minimum channel length. As a result, $v_{n,sw}$ is large, and this produces high flicker noise $v_{n,o}$ at the mixer output. If the LNA amplifies the RF signal of interest by only a modest gain and the mixer downconverts it to zero IF, flicker noise may easily overwhelm the signal at the mixer output. Clearly, the narrower the signal bandwidth, the closer the valuable signal energy lies to DC, and the worse the SNR.

A straightforward way to lower noise is by quadratic scaling up of the switch FET area. This, however, translates into a quadratic increase in power consumption in the LO buffer driving the switches. A more power-efficient way is to replace "direct" by "indirect" conversion to zero IF (Figure 23.17). The RF input is first converted by a high frequency LO (small T_{LO}) to some IF, and then by a lower frequency 2nd LO (large T_{LO}) to zero IF. Suppose CMOS inverters buffer the LO buffers to drive the mixers. The inverter outputs will slew with a maximum slope S, which is the same in the expression above for both 1st and 2nd mixers. With all else the same, flicker noise at the output of the 2nd mixer is then lower in proportion to its LO frequency. After the first downconversion, the signal lies at some IF which is easily chosen far away from the frequency band where the flicker noise is large at the first mixer output. Compared to direct conversion, this scheme requires one additional mixer and an LO buffer. Both LO frequencies can be derived from a single VCO by tapping off the prescaler in the PLL. The choice of frequencies is flexible, as no fixed filters are involved. The first IF must be high enough so that the RF

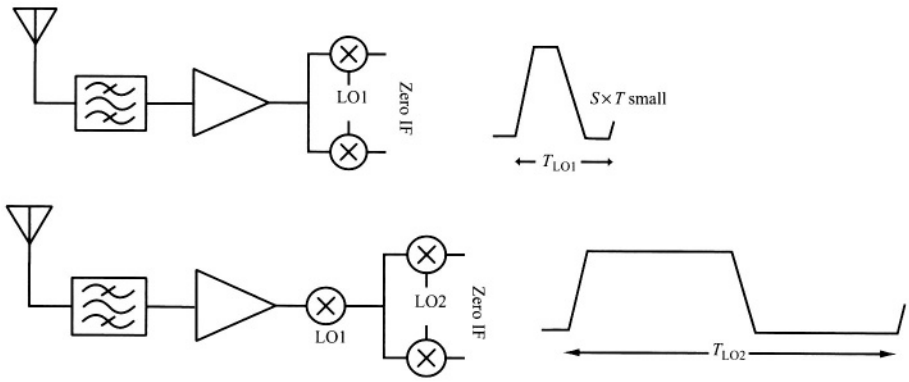


Figure 23.17. (a) Signal at zero IF in direct conversion receiver competes with large flicker noise at mixer output; (b) indirect conversion overcomes this.

preselect filter and the tuned LNA load satisfactorily suppress the image signal. However, it must not be too high, otherwise the LO frequency in the 2nd mixer must be higher, which would lead to more flicker noise at its output.

23.3.7. Frequency Dividers

The frequency divider can easily be the most power-hungry digital circuit in the radio portion of the receiver. It tunes the LO frequency to a particular channel. In the worst case, it comprises a variable modulus digital divider clocked at the LO frequency. However, usually the LO frequency is first divided by a fixed small integer (often 2 or 4) and then by the variable modulus. At high frequencies, or when low power dissipation is important, the prescaler is implemented as a bipolar ECL circuit. A high frequency, low power CMOS prescaler is of great interest.

High frequency, low power GaAs FET prescalers are designed with Source Coupled FET Logic (SCFL), a current-steering circuit modeled on an ECL divider (Figure 23.18). The SCFL is extendable to CMOS. The internal logic voltage swings must be large enough to switch a CMOS differential pair. A 1 V single-ended voltage swing is very typical. If the swing is smaller, the size of the differential pair FETs must be scaled up to rapidly switch the tail current, but this increases the input capacitance. On the other hand, too large a swing only lengthens the rise and falltime.

Technology scaling directly improves the performance of logic circuits in general, specifically of frequency dividers. As linewidth scales down, so does parasitic capacitance of source and drain junctions and wiring which usually dominate the load on the divider stages.

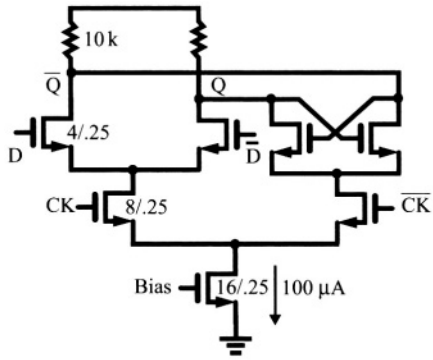


Figure 23.18. Low power CMOS divide-by-2, which toggles at 1.5 GHz.

In a 0.25-μm CMOS implementation, the 1 V swing can be set by, say, a $100\,\mu$A current switching into a $10\,\text{k}\Omega$ load. The load capacitance limits the lowest current. With only a 1.5-V supply, this swing drives the conducting device in the differential pair deep into the triode region. Unlike a bipolar transistor that should not be driven into saturation, it is acceptable to force a CMOS switch into the triode region. The bias current may be scaled down in subsequent stages of the frequency divider, which toggle at lower frequencies.

23.3.8. Baseband Circuits

Variable gain amplifiers and active filters are the important baseband blocks in a direct conversion or low-IF receiver. As the input signal and accompanying interferers in the circuits up to and including channel-select filter have been previously amplified, large signal handling in these circuits is of greater concern than noise. The dynamic range should slide up relative to the front-end. To illustrate this point, an active low-pass filter for channel selection in a zero-IF receiver is considered.

Past experience [7] shows that in well-designed integrated receivers, noise in the active filter dominates the receive signal chain. The input noise level of a multi-stage filter v_{in} can only be lowered at the expense of a quadratic increase in current consumption and capacitor area. This is because the noise spectral density in the passband of, say, a g_{m}-C filter depends on the g_{m}, and to implement a fixed pole frequency, the filter capacitance is proportional to g_{m}. As a result, the input-referred noise in the passband and the filter capacitors are related as follows [6]:

$$\begin{aligned} \hat{v}_{\text{in}}^2 &= 4\text{kT}\Gamma Q^2/g_{\text{m}} \propto Q^2 V_{\text{eff}}/2I \\ C &= g_{\text{m}}/\omega_p \propto Q^2/(\omega_p \hat{v}_{\text{in}}^2) \end{aligned} \tag{23.23}$$

Γ is some noise factor associated with the transconductor circuit, and Q is the pole quality factor. A power-efficient receiver will use an active channel-select filter with the lowest Q poles, that is, whose passband is centered at the lowest frequency. The filter should therefore select the desired channel at zero or low IF. Rather than to lower noise by scaling the filter, it is usually more power-efficient to amplify the input signal before it arrives at the filter. However, now the filter must handle amplified large interferers at its input, which although they lie in the stopband and are eventually suppressed at the filter output, may induce intermodulation distortion that falls in the filter passband. Filter linearity is, therefore, paramount.

Op-amp-based active filters are usually more linear than open-loop transconductor-based active filters. An op-amp-based filter is as linear as the passive feedback components such as resistors and capacitors, and in a well-designed op-amp the gain compresses at a maximum output voltage swing almost equal to the power supply. There are two well-known types of op-amp-based filter: switched capacitor, or active *RC*. The switched capacitor circuit is ruled out because the filter in a wireless receiver must handle out-of-band signals lying far away from the narrow passband needed for a single channel. Therefore to simplify the anti-alias filter, the switched capacitor circuit must be clocked at a large oversampling factor, otherwise sampling at the filter input may alias the out-of-band signals into the filter passband. The high clock rate proportionally raises the current consumption.

The continuous-time active RC filter (Figure 23.19) is interesting because with op-amps biased at low currents in weak inversion, it is possible to accurately produce the desired passband, transition band, and close-in stopband

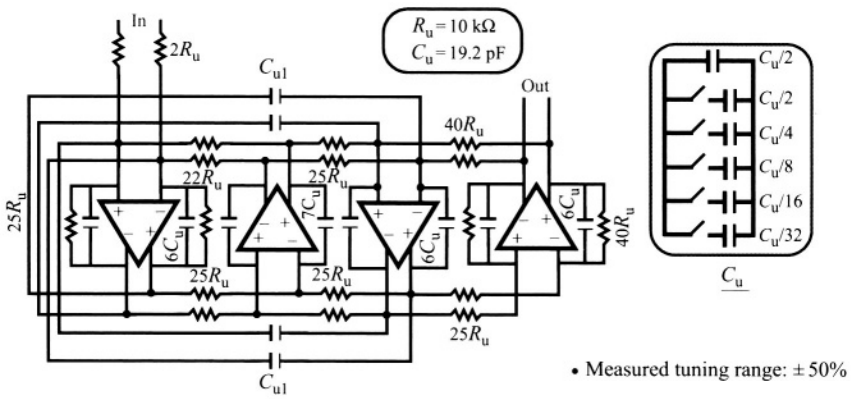


Figure 23.19. Active RC filter offers best linearity of all time-continuous active filters. Discrete tuning method shown.

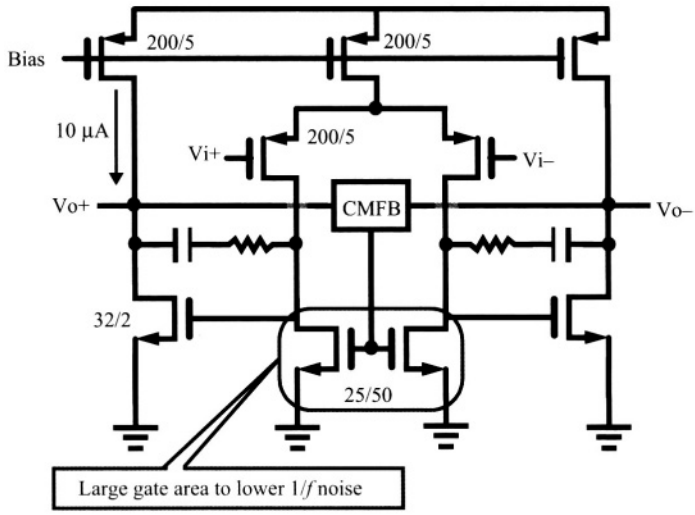


Figure 23.20. Low power two-stage op-amp used in active RC filter.

characteristics at low or zero IF. In most cases, the circuit's inability to respond at high frequencies ensures large loss in the high frequency stopband, without requiring high loop gain in the op-amp circuits. A two-stage op-amp drives the filter resistors (Figure 23.20). The output stage must be capable of rail-to-rail voltage swing. A dominant pole and a zero compensate the fully differential op-amp for stable operation in feedback. The pole and zero frequencies of the active RC filter must be tunable to overcome process spreads. The lowest power method to do so is with a binary-weighted array of switched capacitors at every filter node [31]. The number of array elements depends on the desired accuracy of filter poles. For example, a 5 b switch-selectable capacitor array in parallel with a fixed capacitor equal to the largest array capacitor encompasses variation of up to ±50% in dielectric thickness, while tuning the filter frequency response to 3% accuracy. This is good enough in most practical cases.

Low frequency flicker $(1/f)$ noise is of particular concern in a CMOS zero-IF receiver. The op-amp circuit must be designed to lower the input-referred flicker noise. The flicker noise in a PMOS input stage is usually lower than in an NMOS stage, an effect ascribed to buried-channel conduction in PMOS. Furthermore, as input-referred flicker noise voltage is inversely proportional to gate area $W \times L$, the width and length of all FETs in the op-amp is scaled up while keeping W/L constant. The increase in L lowers f_T roughly in inverse proportion. The noise corner frequency, where flicker noise density intercepts white noise, is proportional to f_T (Figure 23.21). In baseband circuits such as the filter, lower f_T is not of much concern until it approaches roughly ten times the highest signal frequency applied to the circuit.

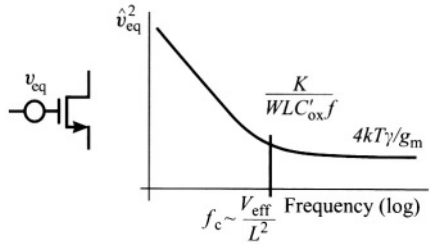


Figure 23.21. Input-referred noise of a MOSFET, and its various dependencies on device size.

The final op-amp sizes must be scaled to deliver some large DC gain when driving the filter resistors. These resistors determine the noise spectral density in the filter passband, that is, the filter's noise figure. A powerful way to improve dynamic range is by embedding gain into filter stages. The largest dynamic range is usually obtained by uniformly interleaving gain with filtering. When the bottleneck is filter noise but not intercept point, it is best to concentrate gain into the filter's input stage, which then significantly lowers the noise contributions of the subsequent filter stages, particularly of stages with high-Q poles where noise is boosted near the pole frequency.

Another important baseband circuit is the A/D converter and demodulator. Using sigma–delta techniques, it is relatively easy to implement a high-resolution A/D converter in the baseband section of a zero IF receiver. However, for wideband FSK demodulation it is simpler still, because a low-power limiting amplifier [32], which is effectively a 1 b A/D converter, may be followed by an efficient but very low power detector [33]. This approach can be extended to constant envelope modulations with lower index, such as GFSK.

23.3.9. On-Chip Inductors

The foregoing sections point out the vital role of large value and high quality inductors in lowering power dissipation. It has also been said that these inductors must usually be off-chip. However, there is increasing need to integrate all the elements in a receiver, among other reasons to obtain a physically compact form-factor. On-chip inductors that are substantially better than the ones customary today will come about from advances on two fronts: CMOS processes which address the needs for better inductors; and efficient software to design spiral inductors, which accurately captures the various losses. Recently, there has been progress on both fronts.

Some BiCMOS and also pure CMOS processes now offer lightly doped substrates. Traditionally CMOS substrates were heavily doped ($\sim 10\,\text{m}\Omega\text{-cm}$) to

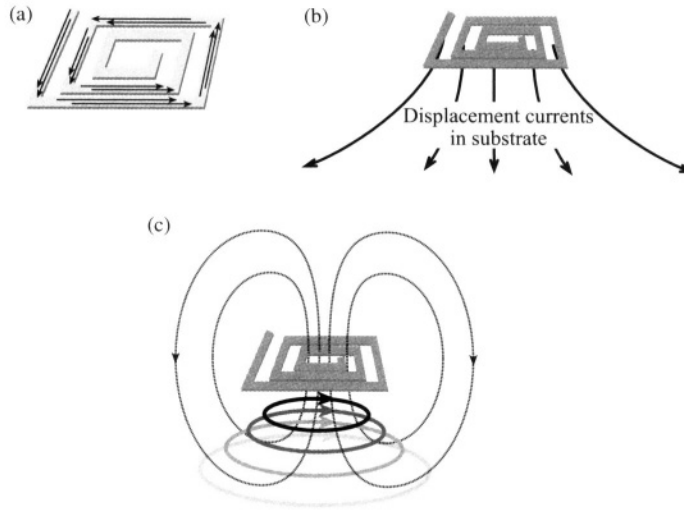


Figure 23.22. Three sources of loss in a spiral inductor on silicon: (a) ohmic, (b) displacement current, and (c) eddy current.

avoid latchup, and the active devices were fabricated in a lightly doped epitaxial layer (usually p-epi on p+ bulk). However, today the trend is to eliminate the epitaxial layer and to use a lightly doped bulk ($\sim 15\ \Omega$-cm) accompanied by dual or triple wells. Also, it is relatively straightforward to add a thicker than usual film of interconnect metal at the uppermost layer of a system of multi-level interconnect, where planarization is less of a concern. The thicker metal cuts down on the usually dominant series ohmic loss in an on-chip spiral inductor.

Spiral inductors fabricated on lossy substrates are poorly modeled. In addition to ohmic losses, they induce displacement currents in the substrate, and eddy currents too as the inductor flux substantially penetrates the substrate in planes parallel to the inductor (Figure 23.22). The latter are distributed effects, and difficult to model analytically. General-purpose software to solve Maxwell's equations is usually too slow to be useful. To this end, a simulator customized to spirals has been developed to model self-inductance, capacitance, and all losses including skin effect [34].

With the right features in the technology and the appropriate CAD tools, it becomes possible to obtain better inductors than the usual. One example is shown here, an 80 nH spiral inductor with a Q of 4.3, with a self-resonance frequency of about 1 GHz (Figure 23.23). The inductor consists of four identical spirals stacked in series to obtain a solenoid-like coupling, whose total self-inductance grows quadratically with the number of layers. The high self-resonance is due to the much smaller footprint of the structure compared to

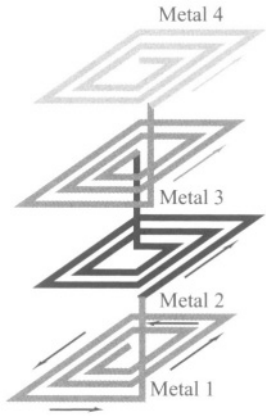


Figure 23.23. Multiple spirals in series with coupled magnetic fields realize a vertical solenoid. The self-inductance of the stack increases quadratically with the number of layers.

a single-layer spiral, and the consequently lower capacitance to substrate. This type of high value integrated inductor is frequently required in low power circuits.

23.3.10. Examples of Low Power Radio Implementations

Various CMOS building blocks and a complete receiver embodying the principles described above have been reported [24]. For instance, an indirect conversion receiver tuned to 900 MHz takes a total of 2.1 mA from 1.5 V, at least a factor of ten lower current than what is reported in other well-designed CMOS receivers. Eventually, the receiver drained 3 mA because the on-chip coupling capacitors were much smaller than expected. The details and performance summary is available in the original publication [24].

What is interesting for the purposes of this paper is that this receiver gives experimental verification of the principles outlined above. The RF front-end of this receiver was built in different CMOS technologies spanning two generations of feature size scaling: $0.6\,\mu m$, and $0.25\,\mu m$. The front-end consists of the 900 MHz LNA, a first mixer, and an 830 MHz VCO. Both implementations use the same external inductors. As Table 23.1 shows, the performance of both circuits is almost equal, and they dissipate essentially the same power. This proves our earlier assertion that once dynamic range is fixed, shrinking technology does not lower the power dissipated by the analog circuits in the RF front-end. What matters more is the quality of the passive elements.

23.3.11. Conclusions: Circuits

In the first part, this paper has surveyed some of the circuit design techniques and system methodologies underlying ultralow power wireless receivers implemented in bipolar and CMOS IC's. High quality passive components are shown to be very important in lowering power dissipation of RF ICs, a fact that was either not realized or set aside in the rush to fully integrate wireless transceivers on a single chip. Dissipation-less passive components can also transform high impedance levels associated with low power circuits to lower off-chip characteristic impedance.

To achieve a certain target for cascade noise figure, a low power receive signal chain must carefully choose between inserting gain prior to the most noisy building blocks or scaling up power consumption to lower their noise level. This trade-off is illustrated with specific examples.

Baseband and IF building blocks are often very challenging, because to realize the necessary dynamic range they may consume as much power as the RF sections. If the modulation scheme allows, a low or zero IF is most desirable from the point of view of lowering power consumption. The dynamic range of blocks up to, and including, the channel-select filter is usually comparable to the receiver front-end dynamic range, except that as the signal is amplified, the dynamic range must slide up. For narrowband channels, circuits in weak inversion are well suited to implement these blocks. If the circuits can swing rail-to-rail at the output without significant gain compression, the input signal can tolerate a higher noise level, which implies that circuit power may be scaled down. An example is given of a baseband amplifier and active RC filter.

One important finding is that technology scaling brings limited benefits in lowering the power consumption of the receiver. To the first order the required dynamic range sets the current consumption of RF and IF circuit blocks, and improving the f_T of the transistors brings no major benefit. However, technology scaling can significantly lower the power that overdriven binary circuits such as frequency dividers consume at a certain clock frequency.

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Chapter 24

PHOTORECEIVER DESIGN

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24.1. Introduction

In optical communication systems, the photoreceiver circuit, which converts the low-level photocurrent detected by a photodiode into an amplified digital logic signal, plays a critical role in determining the overall performance of the optical data link. As in most classes of circuit, the design of these circuits involves trades between conflicting requirements. In this case, the performance parameters of interest are sensitivity, channel rate, power consumption, dynamic range and layout area. This chapter explores the trade-offs between these parameters.

The relative importance of these parameters is very much application dependent. In the traditional application of long-haul telecommunications links, sensitivity is of primary importance. More recently, serial optical data links have also been used in higher volume Local Area Network applications, such as Gigabit Ethernet, in which a desire for low cost increases the importance of low power consumption and low component count. Parallel optical data links, which are being developed in research labs for high data rate interconnections in digital computer systems and telecommunications switches, inherently require the integration of many photoreceiver circuits into a single chip, and, therefore, place particularly stringent demands on power consumption and layout area of individual circuits. Near term prototypes based on fiber ribbon technology have been demonstrated with 32 channels [1] while longer-term technology demonstration systems based on free-space optics have been designed with as many as 4,000 optical channels [2,3]. In such systems, an understanding of the main trades and bounds on performance can provide useful input into system-level design decisions on variables such as, for example, the number of channels to use to implement a given total link capacity.

The primary focus of the discussion in this chapter is on photoreceivers designed for multichannel optical data links that use a simple DC coupled circuit architecture. Many of the trade-offs discussed are equally applicable to single-channel data links, although in single-channel data links there is more flexibility in the choice of circuit architecture due to the more relaxed constraints on layout area and power consumption.

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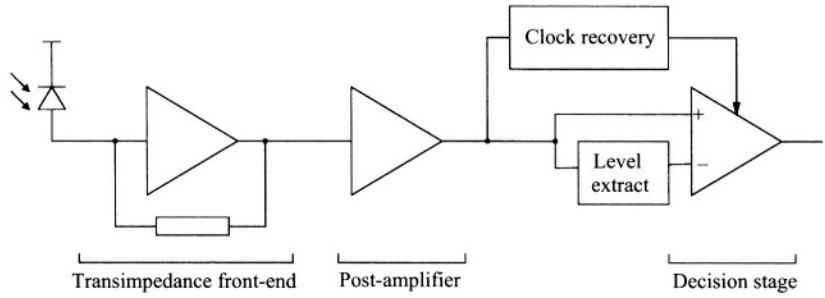


Figure 24.1. Structure of a receiver.

The structure of a conventional single-channel photoreceiver is shown in Figure 24.1. The transimpedance front-end converts the detected photocurrent into a low-level voltage. The front-end generates most of the noise in the receiver circuit; optimizing its noise performance is often an important design objective. Further amplification of the front-end output results in a signal that is sufficient for the decision stage to produce a regenerated logic signal. A low-pass filter can be used to extract an ideal decision threshold equal to the mean optical input power and to remove any inter-stage offset. The logic signal is often retimed with a clock extracted from the data signal.

A significant difference between many of the receivers designed for multichannel optical data links and those designed for the more traditional single-channel link is that the filter is omitted to eliminate the requirement for line-coding and produce a compact layout; DC coupled receivers with a built-in decision threshold are often used instead to buy simplicity of implementation at the (significant) cost of having to deal with DC offsets.

This chapter restricts its attention to the design trade-offs in the transimpedance front-end and the post-amplifier. It considers how the design variables of these blocks influence important characteristics such as front-end noise, post-amplifier gain and inter-stage offsets, and how these characteristics relate to the performance of the receiver as a whole. It builds on previous work on receiver design trade-offs in the specific area of multichannel optical channel data links [4–8] as well as the more established field of single-channel photoreceivers [9–11]. The general approach of analysing design trade-offs by identifying the main design variables and considering their effect on the performance parameters of interest is inspired by the methodology of Laker and Sansen outlined in [12].

24.2. Review of Receiver Structure

The transimpedance gain stage can be implemented using several circuit topologies. Simple gain stages based on CMOS, NMOS and PMOS inverters

are shown in Figure 24.2. Many variants are possible: multiple stages [13,14]; the use of a diode connected load to reduce and stabilize the circuit gain [6–14]; addition of a source follower to reduce the influence of capacitance on the output node [15]; common-gate amplifiers and other current-mode structures [16–18]; a bipolar gain stage with shunt-series feedback [19]. This chapter concentrates on analyzing a simple gain stage with a single-pole transfer function. It gives particular attention to the complementary gain stage that is widely used in multichannel receiver arrays because of the simplicity of a self-biasing amplifier, but most of the analysis is applicable to the other receiver types in Figure 24.2.

The complete circuit of a typical receiver in this application area is shown in Figure 24.3 [20]. Note that this receiver is designed to receive a differentially encoded optical signal and uses two photodiodes to detect the two optical beams. Historically, this arrangement was motivated by a requirement to receive signals from low-contrast multiple-quantum-well modulator devices [21] but differential encoding of the optical signal has many advantages even for high contrast optical data. In particular, the optimum decision threshold is independent of the signal input-level, which gives very good dynamic range even with a fixed decision threshold.

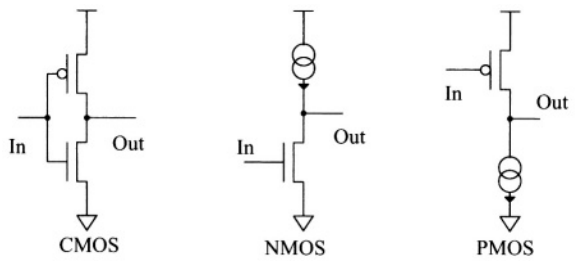


Figure 24.2. Example gain stages for use in multichannel photoreceivers.

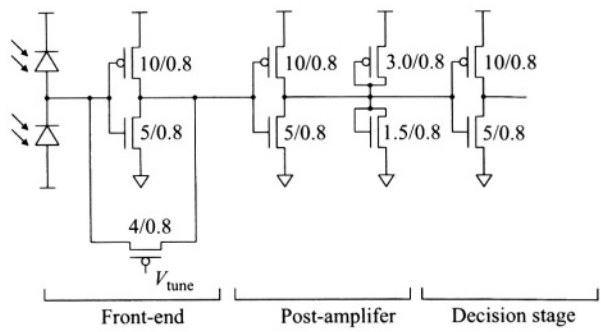


Figure 24.3. Schematic of a typical photoreceiver for multichannel arrays [20].

24.3. Front-End Small-Signal Performance

24.3.1. Small-Signal Analysis

This section begins the discussion of the receiver design trade-offs by considering a small-signal model of the front-end and examining the influence of the feedback resistor, the design variables of the front-end gain stage and the photodiode capacitance on the overall circuit performance.

Figure 24.4 shows a small-signal equivalent circuit of the transimpedance front-end.[1]

This model can be applied to gain stages containing **NMOS** and/or PMOS gain transistors; g_m is the total transconductance of the gain transistors(s) and g_{ds} is the output conductance of the gain transistors(s) and bias transistor if any. The open-loop gain of the stage is g_m/g_{ds}.

C_{IN} is the capacitance of the input node; it includes the photodiode capacitance and the gate–source capacitance of the input transistor. Typically, the photodiode capacitance is the main contributor to this capacitance, particularly in designs that are optimized for power consumption.

C_F is the feedback capacitance between input and output nodes. It includes the gate–drain capacitance of the input transistor and any parasitics.

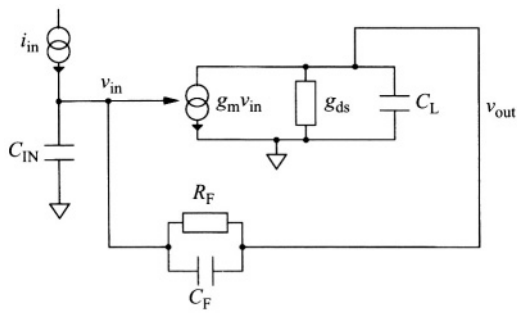


Figure 24.4. Small-signal model of a transimpedance front-end.

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[1] Note that the model of Figure 24.3 starts to break down at frequencies above about $\omega_T/8$ due to non-quasistatic behavior [22] where ω_T is the transit frequency of the gain transistor. For the example parameters, the limit of validity is about 2 GHz. The feedback transistor typically uses a channel length of several times minimum to realize a large resistance and so can have a much lower transit frequency. The equivalent circuit used for the feedback transistor is, therefore, a first-order correction to quasi-static behavior corresponding to the Ward MOSFET capacitance model [23] which can still be accommodated within the circuit model of Figure 24.3 by adding a negative component to C_F [24] and is valid within 5% upto $1.5\omega_T$.

Table 24.1. Typical parameter values for a transimpedance receiver in a multichannel optical data link.

Parameter	*Terms proportional to transistor dimensions*				
	Component multiplier	*Front-end* $W_{\text{FRONT-END}}$	*Post-amplifier* $W_{\text{POST-AMP}}$	*Feedback transistor* $W_{\text{FB}} \times L_{\text{FB}}$	*Constant terms and parasitics*
C_{IN}		2.0 fF/μm		1.4 fF/μm^2	100 fF photodiode 20 fF parasitics
C_{F}		0.7 fF/μm		−0.5 fF/μm^2	2 fF
C_{L}		0.4 fF/μm	2.0 fF/μm	1.4 fF/μm^2	9 fF
g_{m}		190 μS/μm			
A					16.0

C_{L} is the capacitance at the output node of the front-end. It includes the input capacitance of the post-amplifier, the drain junction capacitance of the front-end and the source–gate capacitance and junction capacitance of the feedback transistor. The Miller approximation is used to include the effect of the post-amplifier feedback capacitance in C_{L}.

Table 24.1 shows typical values of these parameters, and how they relate to transistor dimensions for a complementary gain stage on a specific 0.6 μ m process with a 5 V supply. Identical widths are assumed for the NMOS and PMOS transistors. $W_{\text{FRONT-END}}$ and $W_{\text{POST-AMP}}$ denote the widths of the NMOS transistors in the front-end and post-amplifier gain stages. W_{FB} and L_{FB} denote the width and length of the feedback transistor.

As the transistors used are typically quite small, routing capacitance is also significant. The table includes parasitic values extracted from an actual layout with $W_{\text{FRONT-END}} = 10\,\mu\text{m}$ and $W_{\text{POST-AMP}} = 5\,\mu\text{m}$.

Assuming that $A \gg 1$, $C_{\text{IN}} \gg C_{\text{F}}$ and $g_{\text{m}} R_{\text{F}} \gg 1$, simple nodal analysis of the circuit gives a transimpedance gain $Z_{\text{T}}(s)$ of

$$Z_{\text{T}}(s) = \frac{v_{\text{out}}}{i_{\text{in}}} = -\frac{R_{\text{F}}\,(1 - sC_{\text{F}}/g_{\text{m}})}{1 + s\tau + 1/\omega_0^2 s^2} \tag{24.1}$$

where

$$\tau = R_{\text{F}}\left(C_{\text{F}} + \frac{C_{\text{IN}}}{A+1}\right) + \frac{C_{\text{IN}}}{g_{\text{m}}} + \frac{C_L}{g_{\text{m}}}$$
$$\frac{1}{\omega_0^2} = \frac{R_{\text{F}} C_{\text{IN}}(C_L + C_F)}{g_{\text{m}}} \tag{24.2}$$

The zero at $\omega = g_m/C_F$ is usually at high frequency and does not have a big effect on performance although it may lead to increased overshoot. The circuit, therefore, has a second-order response with damping factor $\zeta = \omega_0\tau/2$. The requirement for a response in the time domain with acceptable overshoot requires that ζ is above a certain minimum. For $\zeta > 1/\sqrt{2}$, the step response of a second-order system settles to within 5% of its final value after a settling time of approximately[2]

$$T_S = 3\tau \tag{24.3}$$

T_S is used to estimate the minimum bit-period of a particular front-end. It is assumed for the moment that the post-amplifier has sufficient bandwidth that it does not degrade the rise time. The bit-rate B is then given by

$$B = \frac{1}{3\tau} \tag{24.4}$$

24.3.2. Speed/Sensitivity Trade-Off

For a fixed gain stage, the receiver bit-rate can be traded off against sensitivity by varying the feedback resistor. Large values of R_F will give high sensitivity but lower speed and vice versa. It is useful to define the *switching energy* of a receiver as a measure of the transimpedance–bandwidth product. Following the definition in [5], the switching energy of a two-beam receiver is defined to be the peak optical energy in each beam per bit:[3]

$$E_{OPT} = \frac{P_{PEAK}}{B} \tag{24.5}$$

It is assumed that there is a minimum peak-to-peak voltage V_{MIN} required at the post-amplifier input to produce a valid logic signal at the receiver output that is determined by the properties of the second-stage amplifier only. This assumption is valid for designs that are limited by the gain of the post-amplifier and is a reasonable approximation for designs that are limited by DC offset which is typically the case for receivers in multichannel arrays with no low frequency cut-off. It is not valid for designs that are limited by front-end noise; noise limits will be discussed separately in Section 24.4. In the first instance, V_{MIN} is assumed to be independent of bit-rate, although this assumption will be modified when the behavior of the post-amplifier is examined.

The peak photocurrent per photodiode for a high contrast optical signal required to produce an output swing of V_{MIN} is $I_{MIN} = R_F V_{MIN}/2$ where the

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2 This expression is accurate to about 20% for the stated range.

3 Definitions varying by a factor of 2 in either direction have also been used in the literature, depending on whether the peak or average optical energy is used and whether the energy per beam or total energy in two beams is calculated.

factor of 2 is due to the fact that there are 2 input beams. If the responsivity of the photodiode is SA/W, then the switching energy is

$$E_{OPT} = \frac{1}{2S}\frac{V_{MIN}}{R_F}T_{BIT} \tag{24.6}$$

By eliminating R_F from the expression for τ, an alternative form can be derived:

$$E_{OPT} = \frac{3}{2}\left(C_F + \frac{C_{IN}}{A+1}\right)\frac{1}{1-B/B_0}\frac{V_{MIN}}{S} \tag{24.7}$$

where

$$B_0 = \frac{g_m}{3\,(C_{IN} + C_L)} \tag{24.8}$$

This equation predicts that the switching energy is constant for large values of R_F (low bit rates) but increases asymptotically as the bit-rate B approaches B_0.

The form of this equation is plotted in Figure 24.5. Selecting the part of this curve in which a receiver is to operate by controlling the value of B_0 allows certain trade-offs to be made. B_0 can be controlled by adjusting the design variables of the front-end gain stage. Since $C_L \ll C_{IN}$, B_0 is primarily determined by the transconductance of the input stage and the photodiode capacitance. The transconductance is directly proportional to the width of the front-end transistors. The supply current is also proportional to the width; there is thus a reasonably direct trade-off between power consumption and maximum operating speed for low switching energy. A design optimized to obtain a switching energy close to the low-frequency limit would operate at the low end of the curve, with perhaps $B = 5B_0$ representing a point of diminishing returns. A design in which power consumption was more critical might operate closer to the center of the curve. Operation towards the top of the curve would only be possible if switching energy was a low priority; the slope of the curve indicates that any design in this region would be very sensitive to process variation.

The expression for switching energy (24.7) is valid provided the circuit has an acceptable damping factor ($\zeta > 1/\sqrt{2}$). This may limit the range of bit-rates at which a given gain circuit may be made to operate by adjusting R_F. To get an idea of how the design variables influence this limit, the variation in the damping factor as the feedback resistor is varied can be written in terms of B/B_0:

$$\zeta = \frac{\zeta_{MIN}}{2}\frac{1}{\sqrt{(B/B_0)(1-B/B_0)}} \tag{24.9}$$

where

$$\zeta_{MIN}^2 = \left(1 + \frac{C_L}{C_{IN}}\right)\frac{C_{IN}/(A+1) + C_F}{C_L + C_F} \approx \frac{C_{IN}/(A+1) + C_F}{C_L + C_F} \tag{24.10}$$

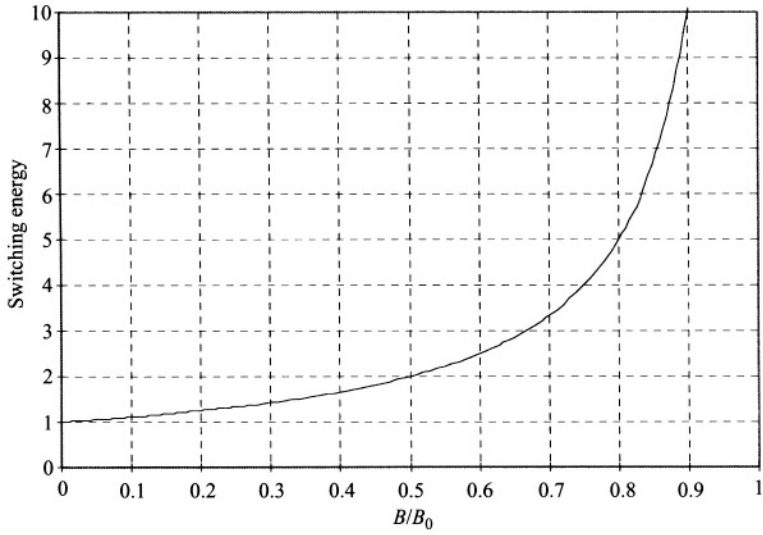


Figure 24.5. Variation in switching energy with bit-rate for a fixed front-end amplifier.

gives the minimum value of ζ. The form of this function is plotted in Figure 24.6 – it is relatively flat over the range of values of B/B_0 that ensure a good compromise between power consumption and switching energy. As one would expect, excessive capacitive loading of the front-end can degrade the damping factor. If the post-amplifier input transistor scales in proportion to the front-end, the load capacitance will scale in proportion to the bit-rate; the damping factor constraint thus limits the maximum speed of operation. This limit can be overcome by reducing the front-end gain (e.g. by using diode connected load transistors inside the feedback loop) but at the expense of switching energy. Damping also limits the extent to which the switching energy may be improved by using longer-channel transistors with higher gain in the front-end.

The choice of transistor bias point also influences the trade-off between transconductance and power consumption. Low values of $V_{GS} - V_T$ give a good g_m/I but require wider transistors for the same g_m which increases the capacitive loading on the output and tends to degrade the damping factor. For the complementary inverter gain structure, $V_{GS} - V_T$ can be controlled by the PMOS : NMOS ratio or, where it is not fixed by external constraints, by choosing the supply voltage. The ratio does not have a strong effect: Figure 24.7 plots the relative g_m and total transistor width at a fixed supply current as a function for the PMOS : NMOS ratio for the example process at a 5 V supply. In the simple receiver structure of Figure 24.3, the small improvement in g_m that

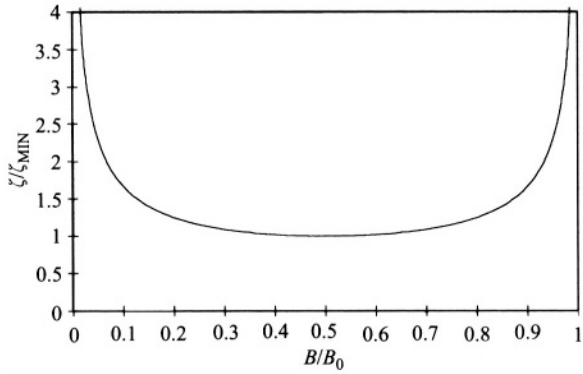


Figure 24.6. Variation in damping factor with B/B_0.

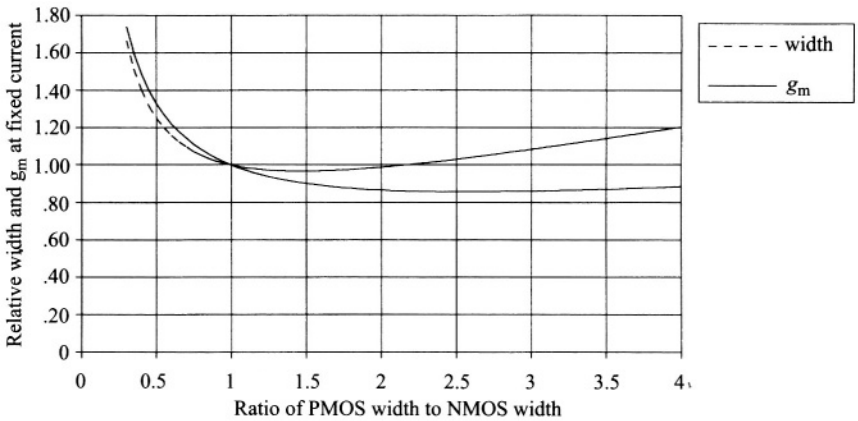


Figure 24.7. Effect of inverter ratio on g_m and total width at fixed current.

is obtained for ratios much less than 1 comes at the cost of highly asymmetric large-signal rise and fall times.

It is worth highlighting the very strong influence of the photodiode capacitance on the performance of the front-end: both directly on the switching energy through equation (24.7) and indirectly on the power consumption through the constraint on g_m implied by equation (24.8). This has important implications for other components in an optical data link system: the design of the optomechanical packaging (the performance of which determines the detector diameter required to collect the light) and the optimization of the optoelectronic devices themselves.

24.3.3. Calculations, for example, parameters

In this section, the expressions developed in the previous sections and the example parameters in Table 24.1 are used to investigate the performance trade-offs numerically.

Figure 24.8 shows the effect on the switching energy of adjusting the front-end width. In this example, $W_{\text{POST-AMP}}$ has been taken equal to $W_{\text{FRONT-END}}$ and a post-amplifier gain of 5 has been assumed in the estimation of the Miller load capacitance. A responsivity of 0.5 A/W and a V_{MIN} of 200 mV were assumed.

For simplicity, a fixed size of feedback transistor of $1.2\,\mu\text{m} \times 2.0\,\mu\text{m}$ is used, independent of the required resistor value; it is assumed that the resistance can be adjusted by varying the gate voltage.[4]

It can be seen that, for each data rate, there is a broad minimum in switching energy for front-end widths greater than a particular value. This is a sensible region in which to design the receiver: in this region, the switching energy should be insensitive to process variation. Increasing the width beyond this optimum slightly degrades the switching energy due to the increase in front-end feedback capacitance.

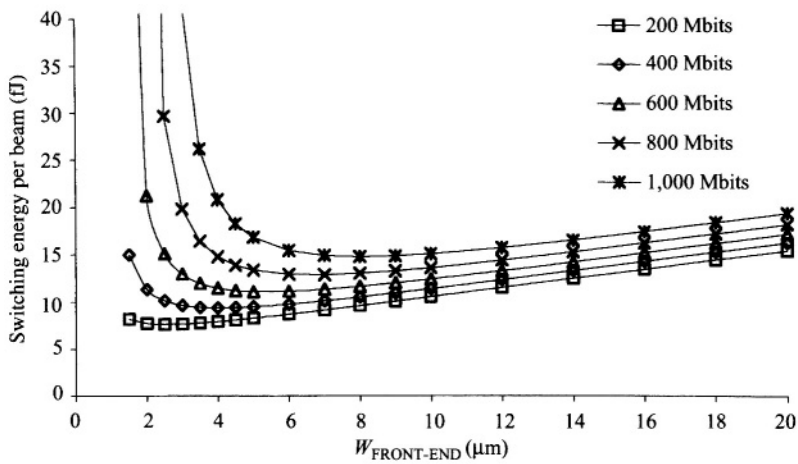


Figure 24.8. Effect of front-end width on switching energy at different bit-rates.

[4] For an NMOS transistor with the example dimensions, the resistance can be adjusted between 7 and $70\,\text{k}\Omega$ for drive voltages between 200 mV and 2 V. The resistor value required to achieve the necessary rise time varied between 12 and $120\,\text{k}\Omega$ depending on bit-rate and so, in a practical implementation, the transistor would have to be slightly longer at low speeds.

This optimal width increases with data rate. For example, at 200 Mbit/s, the model predicts a minimum switching energy of 8 fJ at $2.5\,\mu\text{m}$, whereas at 1 Gbit/s, the minimum is 15 fJ at $8\,\mu\text{m}$. The switching energy is thus relatively insensitive to bit-rate, but the power consumption of a good design varies quite strongly. For reference, the power consumption of the front-end only for $W_{\text{FRONT-END}} = 5\,\mu\text{m}$ under typical process conditions is 2.6 mW.

The damping factor calculated for these parameters was greater than 0.7 at bit-rates up to 400 Mbit/s but fell to around 0.6 at 1 Gbit/s. In the latter case, it was possible to improve the damping factor to 0.7 by sizing the post-amplifier to be half as wide as the front-end to reduce loading.

24.4. Noise Limits

The sensitivity of stand-alone receiver circuits is usually limited by noise. In this section, the fundamental noise limits of a transimpedance front-end are reviewed and a comparison made between the traditional optimization of a front-end for low noise and the somewhat different optimization of a design for multichannel receiver arrays.

The integrated output noise $\langle i_{\text{in}}^2 \rangle$ of a transimpedance front-end referred back to the input is [11]:

$$\left\langle i_{\text{in}}^2 \right\rangle = \left(2q\,(I_{\text{GATE}} + I_{\text{DARK}}) + \frac{4kT}{R_{\text{F}}}\right) \int_0^\infty \frac{|Z_{\text{T}}(f)|^2}{|Z_{\text{T}}(0)|^2}\,\mathrm{d}f + 4kT\,\Gamma \frac{(2\pi\,C_{\text{IN}})^2}{g_{\text{m}}} \int_0^\infty f^2 \frac{|Z_{\text{T}}(f)|^2}{|Z_{\text{T}}(0)|^2}\,\mathrm{d}f \tag{24.11}$$

Γ is a numerical factor describing the thermal noise which is 2/3 for long channel MOS devices but significantly higher for short-channel devices under certain bias conditions [25–27]. I_{GATE} is the transistor gate leakage current and I_{DARK} is the detector dark current; both these noise sources are usually negligible for MOS transistors. Flicker noise has also been neglected.

These integrals are evaluated in [11] for the transfer impedance $Z_{\text{T}}(f)$ from equation (24.1) to give

$$\left\langle i_{\text{in}}^2 \right\rangle = \frac{kT}{\tau}\left(\frac{1}{R_{\text{F}}} + \Gamma \frac{C_{\text{IN}}^2 \omega_0^2}{g_{\text{m}}}\right) = \frac{kT}{\tau\,R_{\text{F}}}\left(1 + \Gamma \frac{C_{\text{IN}}}{C_{\text{L}} + C_{\text{F}}}\right) \tag{24.12}$$

The first and second terms represent the thermal noise in the feedback resistor and the transistor channel respectively. The noise power can be related to a sensitivity for a particular bit error rate by treating it as a Gaussian noise source with the same power. Defining I_{MIN} as the peak photocurrent per photodiode

for a high contrast optical signal as before,

$$I_{MIN} = Q\sqrt{\langle i_{in}^2 \rangle} \tag{24.13}$$

where Q is the solution of

$$\text{BER} = \frac{1}{2}\text{erfc}\left(\frac{Q}{\sqrt{2}}\right) \tag{24.14}$$

and is 6.00 for a bit error rate of 10^{-9}.

Eliminating R_F from equations (24.2), (24.5) and (24.12) as before gives an expression for the switching energy:

$$E_{OPT} = \frac{3Q}{S}\frac{1}{\sqrt{1-B/B_0}}\left[kT\left(C_F + \frac{C_{IN}}{A+1}\right)\left(1+\Gamma\frac{C_{IN}}{C_L+C_F}\right)\right]^{1/2} \tag{24.15}$$

This expression is quite similar to (24.7). Both expressions contain the factor $1/(1-B/B_0)$ raised to a power: 1 in the minimum output signal limited case and 0.5 in the noise limited case. The optimum width from a noise perspective is, therefore, lower than in the minimum output signal case because the factor falls off more rapidly as B_0 is increased above B. Nonetheless, the general principle of sizing the gain transistor to make B_0 significantly greater than B holds. Sizing the transistor wider than this optimum will reduce the noise spectral density but move the second-order pole, which determines the effective limit of the second integral in (24.11), to a higher frequency, offsetting the reduction in spectral density. If there are higher order poles in the transfer function, or if the post-amplifier can be used to band-limit the noise (as is quite commonly the case), then the preceding analysis ceases to be valid and the noise at the input to the decision stage can be reduced by further increasing the width of the front-end gain transistor. However, the expression still gives an upper-bound on the noise.

Figure 24.9 plots the noise limited switching energy for the example parameters, assuming $Q = 6$ and, optimistically, $\Gamma = 2/3$. Notice from the graph that a front-end that has been sized to lie on the flat portion of the switching energy curve will also be near optimum from a noise point of view for a given amplifier configuration.

The importance of the thermal noise in a smart-pixel circuit can be assessed by writing an expression for the voltage signal swing at the output of the first stage and comparing it with typical values of V_{MIN} for the second stage amplifier:

$$V_{OUT} = 2Q\sqrt{1-B/B_0}\left[kT\left(1+\Gamma\frac{C_{IN}}{C_L+C_F}\right)\Big/\left(C_F+\frac{C_{IN}}{A+1}\right)\right]^{1/2} \tag{24.16}$$

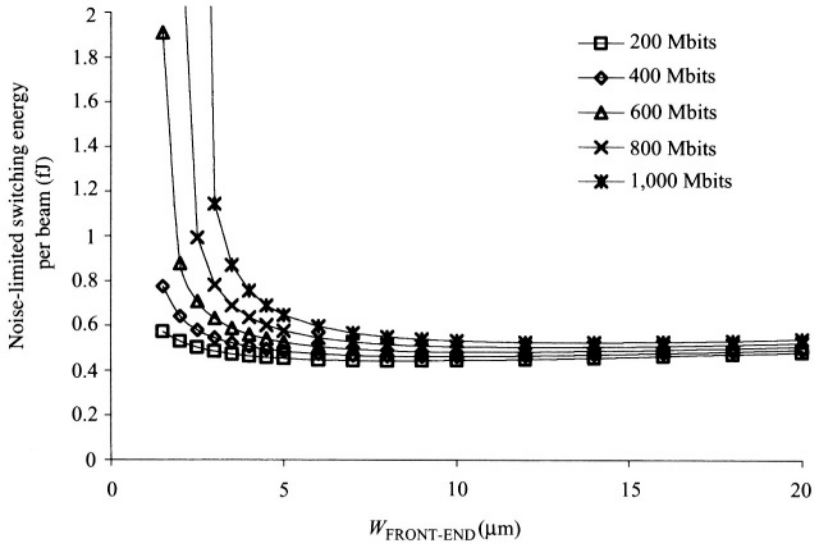


Figure 24.9. Upper bound on noise-limited switching energy as a function of front-end width.

For a design with B_0 significantly larger than B, this function is only weakly dependent on the bit-rate and the exact sizing of the front-end; C_{IN} and C_{L} are the main influences on its value. For designs satisfying this condition using the example parameters, the value was between 9 and 14 mV. Sections 24.5 and 24.6 will show that this is less than the minimum signal requirement imposed by post-amplifier gain and DC offsets.

24.5. Post-Amplifier Performance

The analysis so far has expressed the sensitivity of the receiver in terms of the minimum input signal V_{MIN} required at the output of the front-end to produce a valid logic level at the output of the decision stage. The trade-offs in the design of the front-end at constant V_{MIN} have been discussed.

However, the value of V_{MIN} is determined by the design of the post-amplifier and decision stage. In this section, the parameter V_{MIN} is related to the design variables of the post-amplifier circuit and the results used to discuss the trade-off between power consumption, switching energy and bit-rate in the photoreceiver as a whole. Discussion of the impact of DC offsets on the optimization of the post-amplifier is left to Section 24.6.

The post-amplifier circuit considered is a simple low-gain linear voltage amplifier comprising a complementary inverter Mn2/Mp2 with a diode connected load Mn3/Mp3 (Figure 24.10). The diode loads increase the bandwidth of the linear amplifier from that of an unloaded inverter, help to stabilise the

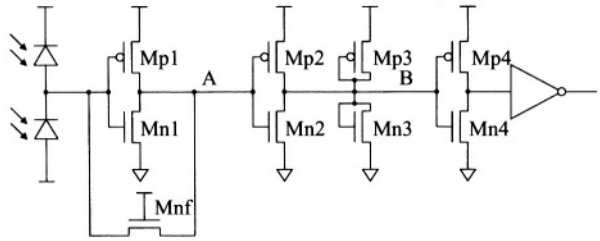


Figure 24.10. Single-stage DC-coupled post-amplifier together with front-end.

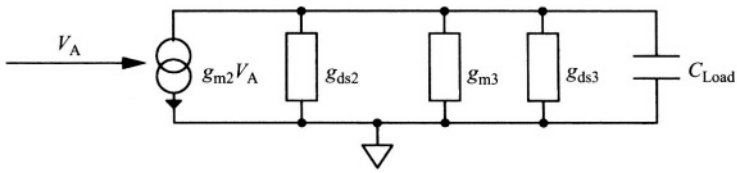


Figure 24.11. Small-signal model of the post-amplifier circuit.

gain against process variation and increase the linear input range. The decision stage, inverter Mn4/Mp4, is essentially a very simple limiting amplifier. The minimum input signal to the decision stage, $V_{DECISION}$, is assumed to be set by the requirement to create a fully restored DC output level after a single inverter stage and is thus treated as independent of bit-rate. Consequently, V_{MIN} is controlled by the gain of the second stage $A_{POST\text{-}AMP}$. For the $0.6\,\mu m$ process considered so far with a 5 V supply, $V_{DECISION}$ is about 800 mV.

The design trade-offs in this circuit are relatively straightforward. The small-signal model shown in Figure 24.11 gives rise to the expression

$$A_{POST\text{-}AMP} = \frac{g_{m2}}{g_{m3} + g_{ds2} + g_{ds3} + sC_{LOAD}} \approx \frac{g_{m2}/g_{m3}}{1 + sC_{LOAD}/g_{m3}} \quad (24.17)$$

for the post-amplifier gain where C_{LOAD} is the total load capacitance. For a fixed load and fixed dimensions of Mn2/Mp2 there is a simple gain–bandwidth trade-off that is controlled by the width of the Mn3/Mp3. The gain–bandwidth can be increased at the expense of power consumption by increasing the width of Mn2/Mp2.

These predictions were validated using HSpice simulations. Using a fixed decision stage, the maximum gain achievable by varying the width of the load transistor under constraint of a minimum 3 dB bandwidth was determined using a small-signal analysis. The channel lengths of the diode loads were assumed to match the channel lengths of Mn2/Mp2 to avoid a systematic offset between the switching point of the front-end and post-amplifier under process variation.

Figure 24.12 shows the results which confirm that the power consumption can be traded against gain up to a point, although there is a diminishing return for gains larger than about 5. The gain–bandwidth trade-off is only evident at higher bandwidths: even with minimum width transistors for the load devices, the bandwidth of the stage is still quite high.

A more effective way to trade power consumption for gain beyond this point of diminishing returns is to employ a multistage post-amplifier. A two-stage amplifier is shown in Figure 24.13. The results of similar simulations performed on this design are shown in Figure 24.14.

It can be seen that, at low bandwidths, this circuit can deliver much higher gains compared to a single-stage design of the same power consumption. However, at higher overall bandwidths closer to the gain–bandwidth product of a single stage, this technique seems to be less useful because the gain per stage must be quite low to achieve the necessary overall bandwidth. Increasing the number of stages further can help; a multistage cascade of low-gain amplifiers is a common-technique for achieving an overall improvement in gain–bandwidth product in wide-band amplifiers [28,29].

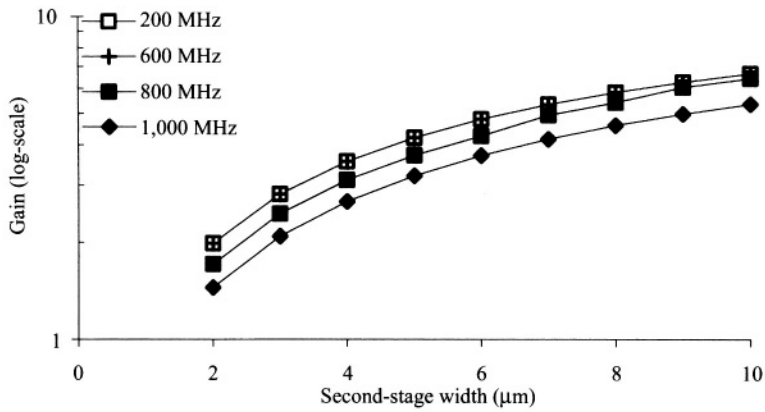


Figure 24.12. Trade-off between gain and power consumption in a single-stage post-amplifier.

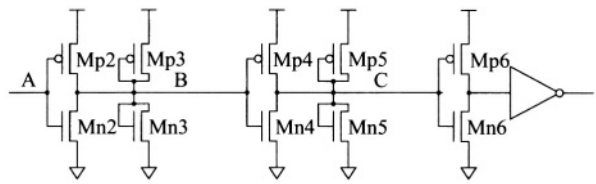


Figure 24.13. Two-stage post-amplifier design.

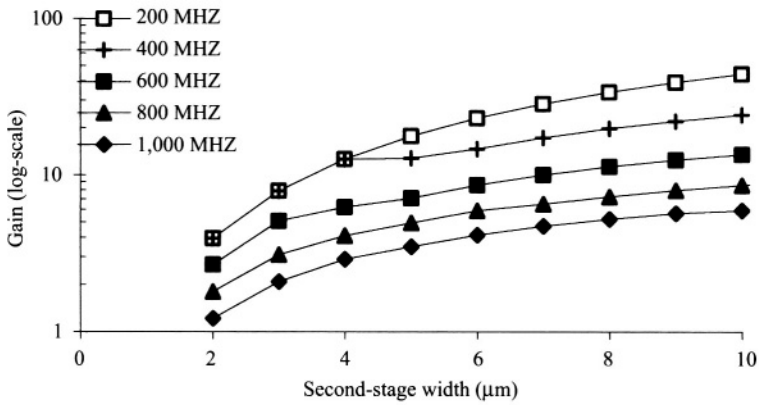


Figure 24.14. Trade-off between gain and power consumption in a two-stage post-amplifier.

Another way to defeat the gain–bandwidth "limit" using a multistage amplifier is to use a cascade of a transconductance stage and a transimpedance stage after Cherry and Hooper [30]. In this approach, the signal is represented as a current at the node between the transconductance and transimpedance stages, making the circuit less sensitive to capacitance at this point. This approach has been compared against the use of multiple voltage-gain stages in this application and has been shown to offer better overall performance at high bit rates [24,31].

24.6. Front-End and Post-Amplifier Combined Trade-Off

To establish the trade-offs in the receiver as a whole, the interactions between the design variables of the two components must be considered.

The main interaction is through the load capacitance presented by the post-amplifier. It has been seen that the load capacitance does not have a strong effect on B_0 or on the switching energy at fixed V_{MIN}. However, it does affect the damping factor ζ; this imposes an upper limit on the effective load capacitance.

The input capacitance of the post-amplifier is proportional to $W_{\mathrm{POST\text{-}AMP}}$. However, in practice, the width of the second stage is not a completely free parameter because of layout requirements for low systematic offset. It is desirable to have the ratio $W_{\mathrm{FRONT\text{-}END}} : W_{\mathrm{POST\text{-}AMP}}$ expressible as a ratio of small integers so that they may be constructed from paralleled unit transistors. Ratios of 1:1 and 2:1 have layouts that are particularly simple (and hence have low parasitic capacitance) and, for the example process parameters, have been found to ensure acceptable damping with 2 : 1 preferred at higher bit-rates.

Assuming that the ratio remains fixed, the power consumption of the post-amplifier and the front-end cease to be independent and it is possible to treat the front-end width as a direct measure of the power consumption of the photoreceiver. It is then useful to weight the switching energy graph of Figure 24.8 by $V_{\text{DECISION}}/A_{\text{POST-AMP}}$ to provide an indication of the overall trade-off between power consumption and sensitivity as a function of bit-rate in the absence of DC offset.

The overall bandwidth of the front-end/post-amplifier combination is less than that of the component stages. The frequency response of the two stages has been approximated by taking the r.m.s. sum of the rise times. Where possible, the second stage has been designed to have the same bandwidth as the front-end[5] such that the overall bandwidth in MHz is half the bit-rate in Mbit/s. In low bit-rate cases where a post-amplifier with a minimum width load has more bandwidth than is required to satisfy the equal bandwidth condition, the bandwidth of the front-end has been chosen to give the required overall bandwidth.

A one- or two-stage post-amplifier has been selected to provide the highest gain for a particular post-amplifier power consumption, comparing a one-stage design with width $W_{\text{FRONT-END}}$ with a two-stage design with width $W_{\text{FRONT-END}}/2$.

The results of this calculation are plotted in Figure 24.15. As the width is increased, there is initially a very rapid reduction in switching energy due to the front-end requirement that $B \ll B_0$. As the width increases further, the additional gain available from the post-amplifier causes the switching energy to continue to decrease; consequently, there is no optimum width as there is if a V_{MIN} independent of width is assumed.

It is also useful to estimate typical values of V_{MIN}. If an arbitrary upper limit on the post-amplifier width of $10\,\mu\text{m}$ is assumed, then gains of between 3 and 18 are possible depending on speed and power consumption requirements. This corresponds to values of V_{MIN} between 40 and 250 mV. In many cases, these figures are such that the overall performance of the photoreceiver is gain-limited [5]. More precisely, the gain–bandwidth product available from a post-amplifier stage with a given constraint on power consumption is not sufficient to implement enough gain to amplify the front-end signal to the detection threshold of the decision stage.

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[5] In general, a cascade of two stages each having a fixed gain–bandwidth product and the same basic shape of frequency response will have a maximum overall gain for a given overall bandwidth when both stages are designed to have the same bandwidth.

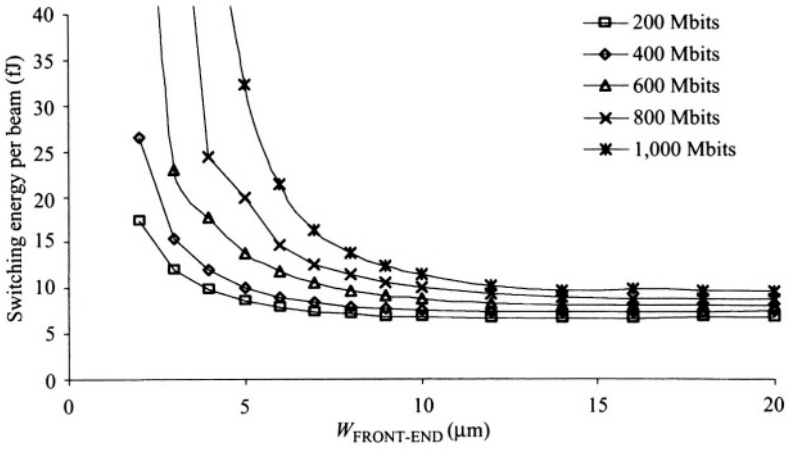


Figure 24.15. Trade-off between front-end width and switching energy including the bit-rate dependence of the second-stage gain.

24.7. Mismatch

In this section, the impact of random DC offsets arising from transistor mismatch is quantified and compared with the limits due to post-amplifier gain and thermal noise that have already been discussed.

In a receiver without a low-frequency cut-off, a DC offset sets an absolute minimum on the detectable signal, introduces pulse-width distortion into the signal (effectively increasing the minimum bit period) and makes it difficult to implement multistage high-gain post-amplifiers (because an amplified DC offset can shift later stages out of the linear region of operation).

Offsets due to random mismatch are statistical variables with a variance that depends on transistor dimensions and can consequently be controlled by design. The mismatch ΔP in a parameter P is formally defined as the difference between the value of the parameter for two identically designed devices with mean zero and variance σ_P^2, commonly with a normal distribution.

Several studies of mismatch have been reported in the literature [32–36]. Here we use the model of Bastos [35], which incorporates terms that account for short and narrow channel effects. This model describes the variance in the mismatch in the drain current at constant gate–source voltage $\sigma^2(\Delta I)$ by

$$\frac{\sigma^2(\Delta I)}{I^2} = \left(\frac{2}{V_{GS} - V_T}\right)^2 \sigma^2(\Delta V_T) + \frac{\sigma^2(\Delta\beta)}{\beta^2} \qquad (24.18)$$

where

$$\sigma^2(\Delta V_T) = \frac{A_{VT}^2}{WL}\left(1 + \frac{L_{VT}}{L} - \frac{W_{VT}}{W}\right) \tag{24.19}$$

and

$$\frac{\sigma^2(\Delta\beta)}{\beta^2} = \frac{A_\beta^2}{WL} \tag{24.20}$$

Let the mean operating point of the inverter be V_{OP} and the mean value of the current at this operating point be I. Suppose that, as a result of mismatch, the operating point varies by δV_{OP} and the current in the NMOS and PMOS transistors at the nominal operating point varies by δI_N and δI_P. Then, equating the change in current in the two transistors,

$$\delta I_N + g_{mn}\delta V_{OP} = \delta I_p - g_{mp}\delta V_{op} \tag{24.21}$$

The variance in the current of a single transistor biased about its nominal operating point σ_I^2 is given by $\sigma_I^2 = \sigma^2(\Delta I)/2$ since I for the two transistors of the pair is statistically independent.

The variance in the operating point is then

$$2\sigma_{V_{OP}}^2 = \frac{\sigma_{In}^2 + \sigma_{Ip}^2}{(g_{mn} + g_{mp})^2} \tag{24.22}$$

where the transconductance values should be calculated using a full transistor model including the effects of velocity saturation even though a reduced transistor model has been used to develop a statistical model of the mismatch.

Now consider a receiver consisting of a front-end, a single post-amplifier with a gain A and a decision stage. It is readily shown that the offset voltage, defined, as the nominal voltage required at the output of the first stage to produce zero output is

$$V_{OFFSET} = -\delta V_{FRONT\text{-}END} + \left(1 + \frac{1}{A}\right)\delta V_{POST\text{-}AMP} - \frac{\delta V_{DECISION}}{A} \tag{24.23}$$

and hence

$$\sigma_{VOFFSET}^2 = \sigma_{FRONT\text{-}END}^2 + \left(1 + \frac{1}{A}\right)^2 \sigma_{POST\text{-}AMP}^2 + \frac{\sigma_{DECISION}^2}{A^2} \tag{24.24}$$

In the simple case when the gain of the second stage is high, the mismatch in the post-amplifier load transistors is neglected, and the second stage is the same size as the front-end, this can be approximated as $\sigma_{VOFFSET}^2 = 2\sigma_{VOP}^2$. This is the expression that is used to estimate the offset voltage.

In a multichannel optical data link, the parameter of interest is the worst case offset voltage that can be expected across the array. As the offset is a statistical variable, this is related to the required yield. The probability that, in any one particular receiver, the offset is within $\pm k\sigma_{VOFFSET}$ assuming a normal distribution is

$$P_{WORKING} = \text{erf}\left(\frac{k}{\sqrt{2}}\right) \tag{24.25}$$

The probability that, in a group of N circuits, all of the circuits are within specification is $P_{WORKING}^{N}$. In a multichannel array, a larger number of standard deviations have to be considered to achieve a given yield. For example, to achieve a failure rate of 1 in 100, a 1024 channel array must be designed to accommodate an offset of $\pm 4.5\sigma_{VOFFSET}$ compared to $\pm 2.6\sigma_{VOFFSET}$ for a single channel circuit. Similar issues occur in the design of, for example, sense amplifiers in large DRAM arrays [36] and high-resolution data converters.

In order to produce a rail-to-rail swing at the output of the decision stage, the input to the decision stage must be enough to overcome the offset plus the signal level required in the absence of any offset, previously defined as V_{MIN}. The actual switching point of the receiver can be anywhere within a band of $\pm V_{OFFSET}$ centred about the nominal switching point and so the minimum input signal to produce a full swing output is, therefore,

$$V'_{MIN} = V_{MIN} + 2V_{OFFSET} \tag{24.26}$$

The offset will also lead to increased pulse width distortion; this in turn may degrade the sensitivity further.

The implications of offset voltage for the overall design trade-off can be examined by performing some calculations in an example process. For this purpose, the matching data for the $0.7\,\mu m$ process reported in [35] is used. Relevant matching data for this process is summarized in Table 24.2. A front-end with width $W_{PMOS} = W_{NMOS}$ and $L_{NMOS} = L_{PMOS} = 0.7\,\mu m$ was assumed. The offset voltage was calculated as a function of $W_{FRONT\text{-}END}$ assuming a 1024 channel array with a required yield of 0.99 for designs having a $W_{FRONT\text{-}END} : W_{POST\text{-}AMP}$ ratio of 1 : 1 and 2 : 1. Figure 24.16 shows the results of the calculation. In this technology, about 75% of the offset voltage could be attributed to the threshold voltage mismatch term.

For the device dimensions considered, the limit on minimum signal imposed by the offset voltage, which is twice the offset plotted in the graph, is quite large. In particular, it is significantly greater than the estimates of the thermal noise in Section 24.4, indicating that, in a DC coupled receiver, thermal noise does not set an important limit on receiver performance. The results also suggest that offset may be more important in determining sensitivity than the post-amplifier gain limit under many circumstances. Direct comparison with the

Table 24.2. Matching data for the 0.7 μm process reported in Bastos [35].

Parameter	*NMOS*	*PMOS*
A_{VT}	11 mV μm	22 mV μm
A_β	1.9% μm	2.8% μm
L_{VT}	0.67 μm	—
W_{VT}	0.40 μm	—

Model parameters for the PMOS devices in this process are not reported. Reasonable assumptions regarding the relative strength of the PMOS devices have been made in the calculations. The PMOS devices characterized for matching were special purpose devices with a minimum channel length of 1.2 μm. It was also assumed that the standard 0.7 μm PMOS devices would display short/narrow channel matching effects comparable to those in the NMOS devices. At the time of writing, no matching data were available for the 0.6 μm process used in the first part of the chapter. The constant A_{VT} has been found to improve linearly with oxide thickness [35] and so slightly better matching performance might be expected.

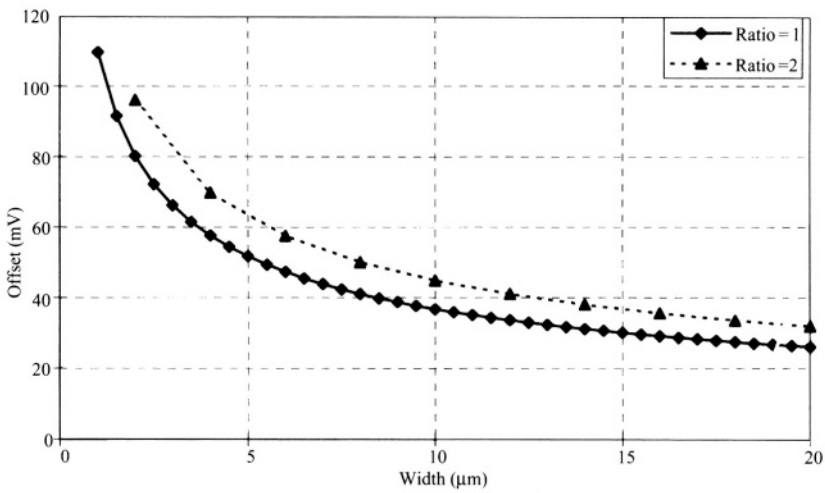


Figure 24.16. Calculation of the worst-case offset voltage as a function of transistor width in an example 0.7 μm process.

0.6 μm process post-amplifier gain limits is difficult because of the use of a different process for the analysis. However, the worst-case offset voltage varies between ±20 and ±70 mV for reasonably dimensioned transistors and it has been seen that the gain-limited V_{MIN} ranged between 40 and 250 mV depending on bit-rate and power consumption requirements. The offset limit is more important in low bit-rate circuits where it is possible to achieve high post-amplifier gain and/or sufficient bandwidth with narrow transistors.

Taking offset voltage into account in the design process leads to a slightly different design approach. Firstly, it limits the amount of gain that can be implemented in the post-amplifier to between 10 and 20. Secondly, if a design is offset limited then a higher overall sensitivity can be attained by putting more gain/less bandwidth into the front-end and less gain/more bandwidth into the post-amplifier stage. This contrasts with the post-amplifier gain–bandwidth limited case where it is better to make the bandwidths of the two stages the same as discussed in Section 24.6. Finally, it suggests that better overall performance may be obtained by using transistors with channel lengths slightly longer than minimum to increase the effective channel area for a given transconductance. The disadvantage of this approach is the rapid increase in gate capacitance as a function of channel length at constant transconductance, which will eventually result in an inadequately damped response as discussed in Section 24.3.2.

The importance of offset in overall receiver performance highlighted by this analysis indicates that it is worth investigating circuit techniques for implementing compact receivers with a low-frequency cut-off. Some possible approaches are discussed in [24].

24.8. Conclusions

This chapter has reviewed the basic structure of photoreceivers designed for multichannel optical data links and how it compares to that of a conventional telecommunications receiver. The design variables that can be used to achieve a trade-off between sensitivity, power consumption and speed have been identified and the analysis of their influence provides a starting point for a design procedure for receiver circuits in this application area.

The relative importance of thermal noise, post-amplifier gain and mismatch-related offset on sensitivity has been discussed. In marked contrast to conventional telecommunications receivers, noise is not a limiting factor: first, because the low photodiode capacitance resulting from hybrid integration provides good noise performance even at low power dissipation; secondly, because the DC coupled nature of the design imposed by layout area constraints and the limited number of post-amplifier gain stages imposed by power consumption limitations make it difficult to design a post-amplifier that can detect signals at the noise limit. It is the properties of the post-amplifier, not those of the front-end, which limit the performance of this class of photoreceiver.

Acknowledgments

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Chapter 25

ANALOG FRONT-END DESIGN CONSIDERATIONS FOR DSL

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25.1. Introduction

The digital subscriber line (DSL) techniques enable high-speed data transmission over twisted copper wires [1,2]. These wires are usually used for plain old telephone service (POTS) or integrated service digital network (ISDN). To deliver a higher data rate, DSL systems usually utilize frequencies much larger than POTS or ISDN frequencies. A typical DSL transceiver system is shown in Figure 25.1.

The data from the DSP is converted into analog signal by a digital-to-analog converter (DAC). To attenuate the images at the multiple clock frequencies, an image rejection filter is usually needed. It could be a continuous-time filter or a combination of a sampled-data filter and a continuous-time filter. For frequency-division duplexing (FDD) or frequency-division multiplexing (FDM) systems, where transmit and receive signals occupy different frequency bands, a band-splitting filter or transmit (Tx) filter can be used to filter out out-of-band noise and signals. Besides the FDD, echo-cancelation (EC) based systems exist for DSL as well where both transmit and receive signals occupy the same frequency band. In order to extract the receive (Rx) signal, adaptive digital filters or echo canceller are used to subtract the Tx signal that is coupled into the receiver. (The portion of the Tx signal that aliases into the receive path is referred to as the echo signal.) In EC-based systems, band-splitting Tx

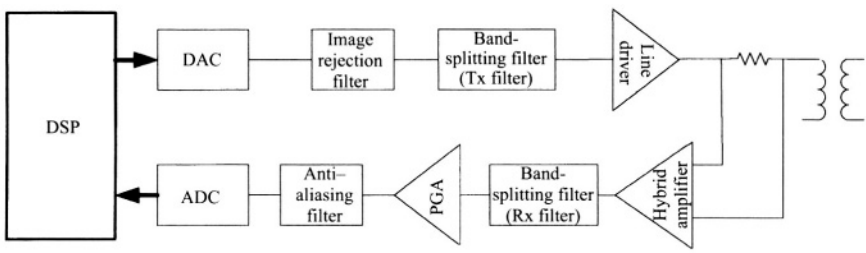


Figure 25.1. A simplifed DSL transceiver system.

C. Toumazou et al. (eds), Trade-Offs in Analog Circuit Design: The Designer's Companion, 723–746.
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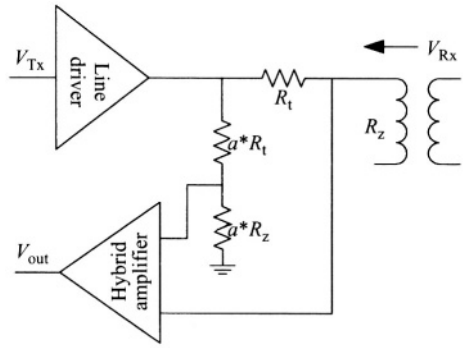


Figure 25.2. Simplified diagram of a hybrid.

filters cannot be used. In order to drive the telephone line that has a characteristic impedance of 100 ohms (usually in US) or 135 ohms (usually in Europe), a line driver is generally needed. In most systems where power cutback is required, a programmable attenuation is needed in the transmit path.

At the receive side, the first block is usually the hybrid amplifier that is essentially a difference amplifier with a programmable gain. The use of a resistor (back-matching resistor) at the line driver output is to terminate the telephone line properly and to facilitate the extraction of the received signal if the hybrid is used (see discussions in the next paragraph). Due to the frequency dependency of the line impedance, some of the Tx signal is still present at the hybrid amplifier output. For FDD systems, a band-splitting or Rx filter may be used to eliminate the echo signal. Even for EC systems, an Rx filter could be used to reduce the echo power if the Tx bandwidth is larger than the Rx bandwidth. A programmable gain amplifier (PGA) is generally needed to utilize the dynamic range of the analog-to-digital converter (ADC). To avoid spectral aliasing, an anti-aliasing filter (AAF) is usually required before the ADC. The digital outputs of the ADC are then processed by the DSP.

The use of a hybrid is critical in most DSL systems. In Figure 25.2, we show a simplified diagram of a hybrid.

Assume that the line driver has a unity gain and the transformer ratio is 1:1. Also assume that the signal transmitted is V_{Tx} and the signal received (i.e. the signal transmitted from the other end that arrives at the receiver) is V_{RX}. The signal after the hybrid amplifier (ignoring the gain in the difference amplifier) is given by

$$\begin{aligned} V_{out} &= \left\{ \frac{R_z}{R_t + R_z} \cdot (V_{Tx} - V_{Rx}) + V_{Rx} \right\} - \frac{a \cdot R_z}{a \cdot R_t + a \cdot R_z} \cdot V_{Tx} \\ &= \frac{R_t}{R_t + R_z} \cdot V_{Rx} \end{aligned} \tag{25.1}$$

where R_z is the characteristic impedance of the line and R_t is the termination resistance. The constant a is usually far larger than unity in order not to load the line driver.

It is seen that the output does not contain any Tx signal or echo signal. However, the derivation above is based on the assumption that the impedance of the hybrid perfectly matches the line impedance. Due to the vast variation in the line impedance, the Tx signal is usually present at the receiver. The ratio of the Tx signal seen by the hybrid amplifier output (echo signal) and the Tx signal is usually defined as hybrid loss or echo rejection. To make the definition meaningful, we usually refer all the signals to the line such that the transformer ratio and the gain of the hybrid amplifier will not alter the definition. In a real system, there is usually a passive matching network at the hybrid amplifier input to match the line impedance. This matching network can also be made adaptive in order to provide high hybrid loss for different lines.

It is also seen that the termination resistor R_t has a strong impact on the Rx signal. Too small R_t reduces the receive signal increasing the receiver dynamic range requirement. Too large R_t dissipates too much power from the line driver unless the termination resistance is synthesized by active termination techniques.

25.2. System Considerations

As for most applications, performance, power dissipation, flexibility and cost are the major factors in designing a DSL transceiver. Since most DSL systems rely on extensive signal processing, a dedicated DSP chip is usually needed to deliver high performance at relatively low power dissipation, though software DSL modems do exist. Besides the DSP chip, there are many analog functions in a DSL transceiver. Depending on applications and system requirements, there are several alternatives to design and integrate these analog functions [3–9]. How to design and integrate all the analog functions has tremendous impact on the system performance, system power dissipation, system flexibility and system cost.

Referring to Figure 25.1, there are many questions concerning designing and integrating the analog functions. What process is needed to design and integrate the analog functions? Should we use active or passive filters? These are among the most important questions besides the data converter requirements for a specific system.

25.2.1. Digital vs Analog Process

Integrating analog and digital circuits on the same die reduces the cost for certain applications. For high-performance communication systems, integration of analog and digital circuits may not be economically favorable or performance competitive.

To design a high-performance low-power DSP for DSL systems, low-voltage deep sub-micron CMOS process offers obvious advantages. Even though deep sub-micron process offers some analog components such as metal-to-metal capacitors at an extra cost, the lower supply voltage, larger leakage current of low threshold voltage devices, and noise coupling via the heavily doped substrate are a few of many hurdles for high-performance analog design. The statement that digital CMOS process is cheaper than analog process is only true if both processes have the same minimum transistor length. Mask tooling and wafer cost for an advanced digital CMOS process are much more expensive than a CMOS process that is tuned for analog and mixed signal circuits, at least for the time being. For instance, the same size wafer for a 0.18-μm pure digital CMOS process could cost 2 ~ 3 times more than that for a 0.35/0.5-μm mixed signal CMOS process at the moment when this chapter is being written.

For a given DSP function, using smaller geometry devices can shrink the die size and reduce the power dissipation, though in reality we seldom see the DSP die size shrink due to the fact that customers always ask for more functionalities. However, analog die size and power dissipation usually do not decrease but most likely increase in a low supply voltage deep sub-micron process if the performance is fundamentally limited by thermal noise. A large die size due to the integration of high-performance analog and DSP circuits also has a strong negative impact on the chip yield as well as testability.

Of course, integrating the DSP and analog functions on the same die could potentially reduce the number of chips on the board and reduce the board size. However, the board size may not be limited by the DSP and AFE chip. Also there exist other packaging techniques that offer board space advantage such as multi chip module (MCM) and chip-scale package, though they do come with a price. Another consideration is that instead of integrating DSP and analog on the chip die for a single channel, the DSP and AFE could have multiple channels to further reduce the board space for central office applications [9,10] where many lines are terminated.

In a nutshell, for high-performance DSL systems, integration of analog and digital circuits in a digital CMOS may not be advantageous. It could be a better choice to design the DSP in a deep sub-micron process and design analog functions in a process optimized for mixed-signal circuits.

25.2.2. Active vs Passive Filters

Analog or continuous-time filters are usually needed for most communication systems. The inevitable purpose of analog filters is to prevent spectral aliasing when the analog signal is sampled by an ADC and to reject images at the multiple clock frequencies of a DAC output. If the analog signal is oversampled,

integrated analog filters can usually fulfill anti-aliasing and image-rejection purposes. However, if the analog signal is not oversampled, the anti-aliasing filter and image-rejection filters are difficult to integrate. For FDD systems, the band-splitting filter usually calls for a sharp transition band, making it difficult to integrate, though entirely possible. For any analog filter that require a sharp transition band, passive filters become an attractive alternative.

From the system's viewpoint, using passive filters may not seem to be attractive. To have a low noise floor, LC passive filters are usually preferred. Inductors are bulky, increasing the board space. If the cut-off frequency of the passive filter is low, it is difficult to make the impedance high and thereby driving the LC passive filter may be power consuming. Generally speaking, the more external components a system has, lower is the system yield. Due to these reasons, integrated analog filters may seem attractive.

Integrated filters in CMOS are usually active. The cut-off frequency of an active filter is usually determined by capacitance and resistance (or transconductance). In order to have a low noise floor, the resistance has to be low. Driving low resistance is very power hungry. A high-order active filter usually consumes much more power than an equivalent LC filter if a low noise floor is required. For any active filter, every resistance and every active component contribute to the noise at the output, and the noise gain from some internal nodes to the output could be considerably higher than the voltage gain of the filter, making low-noise design very difficult. Depending on the filter architecture, noise peaking at the transition band may occur for filters with a sharp transition band. If the frequencies where the noise peaking occurs are used by the system, the system performance can degrade significantly.

Another problem associated with active filters is the inaccuracy and variation of the cut-off frequency. Process variation can be trimmed. Temperature trimming could be tricky. After a data link is established, the excessive shift in the cut-off frequency and the glitch when the cut-off frequency is trimmed could break the link depending on the system.

If the cut-off frequency is low, the capacitance has to be very large since small resistance has to be used to reduce the noise floor of active filters. This significantly increases the die size and the chip cost.

In general, passive LC filters have lower power dissipation and higher performance, but integrated analog filters have the advantage of higher integration level and their cut-off frequency can be controlled by the DSP thereby having the possibility of multi-mode operation without board change. As far as the cost is concerned, external components for LC filters are generally more expensive than integrated active filter. However, if the noise requirement is very stringent and the filter cut-off frequency is low, the active filter solution can be equally expensive due to the chip yield and the large die mainly occupied by linear capacitors.

25.3. Data Converter Requirements for DSL

Data converter requirements are determined by the system [11]. For DSL applications, there are usually two types of line codes, one being baseband, the other being passband. The baseband line codes do not have energy at DC, although the baseband line codes can be modulated to a carrier. The passband codes have energy at DC [2,11]. The basic data converter requirements can be derived from the system requirements such as the desired data rate or bit rate and desired error probability (which determine the carrier signal to noise ratio), the signal peak-to-average ratio (PAR), and the duplexing method [11]. In the following discussions, we generally assume (if not explicitly stated) that the SNR is mainly limited by the ADC quantization noise and that we ignore the noise margin and coding gain. All the formulas can be slightly modified to accommodate noise contribution from other sources, noise margin and coding gain.

One of the most commonly used baseband codes is pulse amplitude modulation (PAM). A b-bit RAM has $M = 2^b$ equally spaced levels symmetrically placed about zero ($b = 1,2,\ldots$). A b-bit PAM is often referred to PAM-M or M-ary PAM. The basic data converter requirement for M-ary PAM is given [11] by

$$\text{SNR} = 20 \cdot \log\left\{Q^{-1}\left(\frac{1}{2 \cdot (1 - 1/M)}\right) \cdot P_{PAM}\right\} + 20 \cdot \log(M - 1) + 20 \cdot \log(\beta) - 10 \cdot \log(\text{OSR}) - 3 \tag{25.2}$$

where $Q(x)$ is the Q function defined as the probability that a unit variance zero-mean Gaussian random variable exceeds the value in the argument x, M is the number of levels in the PAM code, P_{PAM} is the error probability, β is determined by the excess bandwidth (bandwidth relative to the symbol rate), and OSR is the oversampling ratio. The Q function is defined by

$$Q(x) = \int_x^{\infty} \frac{1}{\sqrt{2\pi}} \cdot e^{-u^2/2} \cdot du \tag{25.3}$$

The SNR is related to the number of bits in data converters by

$$N(\text{bits}) = \frac{\text{SNR} - 1.76}{6.02} \tag{25.4}$$

In Figure 25.3, we plot the data converter requirement for M-ary PAM. β is assumed to be 2 and no oversampling is used. It is seen that for every doubling in the number of levels M for PAM, the data converter requirement increases by 1 bit.

Passband codes have no energy at DC. The widely used passband code is the quadrature amplitude modulation (QAM) code. A QAM signal is constructed

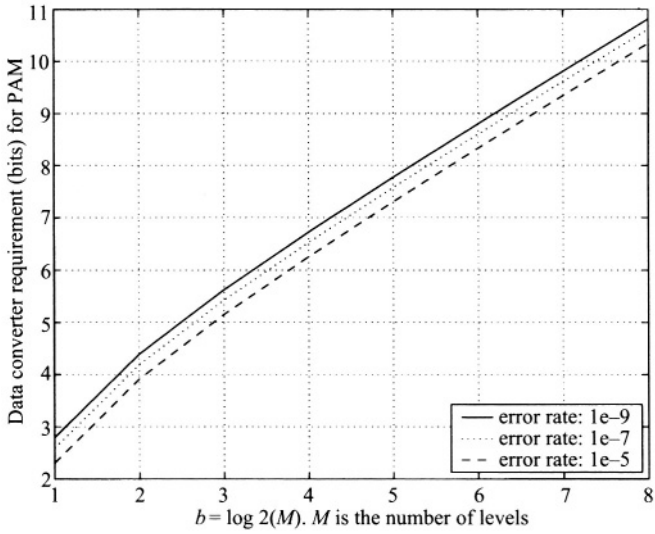


Figure 25.3. Data converter requirement for PAM.

by the summation of an in-phase signal (I) and a quadrature signal (Q), given by

$$I + Q = \varphi(t) \cdot \cos(\omega_c \cdot t) - \varphi(t) \cdot \sin(\omega_c \cdot t) \tag{25.5}$$

where ω_c is the carrier frequency and $\varphi(t)$ is a real-time pulse like a sine or a square-root raised cosine pulse that is determined by the digital data stream. The QAM, codes are two-dimensional. With a b-bit QAM, there are $M = 2^b$ symbols in the constellation (M-ary QAM).

For M-ary QAM, the data converter requirement is given [11] by

$$\begin{aligned} \text{SNR} = {} & 20 \cdot \log\left\{ Q^{-1}\left(\frac{1}{4 \cdot (1 - 1/(\sqrt{M}))} \right) \cdot P_{\text{QAM}} \right\} \\ & + 10 \cdot \log\left\{ \frac{(M-1) \cdot (\sqrt{M} - 1)}{(\sqrt{M} + 1)} \right\} \\ & + 20 \cdot \log(\beta) - 10 \cdot \log(\text{OSR}) \end{aligned} \tag{25.6}$$

where $Q(x)$ is the Q function, M is the number of levels in the QAM code, P_{QAM} is the error probability, β is determined by the excess bandwidth, and OSR is the oversampling ratio.

In Figure 25.4, we show that the data converter requirement as a function of the number of the levels M for QAM line codes, β is assumed to be 1.6 and no oversampling is used. It is seen that for every doubling in the number of levels M for QAM, the data converter requirement increases by 0.5 bit.

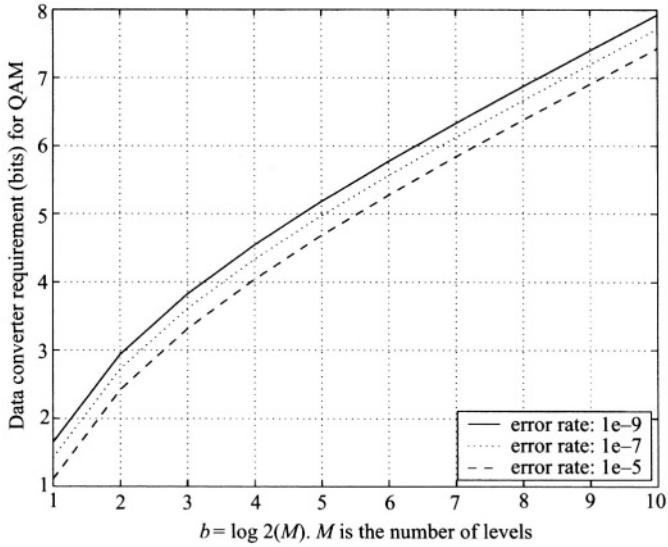


Figure 25.4. Data converter requirement of QAM.

The discrete multi-tone modulation (DMT) is the standard modulation scheme for asymmetrical DSL (ADSL). A DMT is essentially a summation of many QAM signals that have different carrier frequencies and/or phases. One of the disadvantages of DMT is the increased PAR. Suppose that there are m sub-carriers in the DMT and that every sub-carrier has the same number of levels, M. Since the PAR of the DMT increases by $\sqrt{m}$ compared to its individual sub-carrier, by using the previous equations, we have

$$\begin{aligned}\text{SNR} = {} & 20 \cdot \log\left\{ Q^{-1}\left(\frac{1}{4 \cdot (1 - 1/(\sqrt{M}))}\right) \cdot P_{\text{QAM}} \right\} \\ & + 10 \cdot \log\left\{ \frac{(M-1) \cdot ((\sqrt{M}-1)}{(\sqrt{M}+1)} \right\} \\ & + 10 \cdot \log(m) - 10 \cdot \log(\text{OSR}) \end{aligned} \tag{25.7}$$

where $Q(\text{x})$ is the Q function, P_{QAM} is the error probability, M is the number of levels in the sub-carriers, m is the total number of sub-carriers, and OSR is the oversampling ratio. The modulation and demodulation for DMT (usually using IFFT and FFT) are different from those for a single-carrier QAM. Therefore, the excess bandwidth parameter does not apply.

Theoretically, with the maximum of 255 tones in ADSL, the data converter requirement for the DMT increases by 4 bits compared to its corresponding

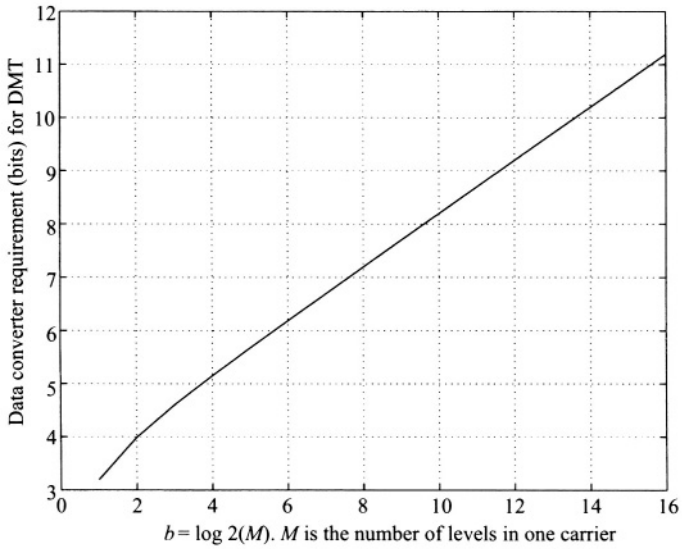


Figure 25.5. Data converter requirement for DMT.

QAM. Fortunately, when m is large, the DMT tones can be treated as additive white Gaussian noise (AWGN). With a clipping probability of 10^{-7} (this gives a PAR of 5.3), we have the approximation given [11] by

$$\begin{aligned}\text{SNR} &= 20 \cdot \log\left\{Q^{-1}\left(\frac{1}{4} \cdot 10^{-7}\right)\right\} + 10 \cdot \log\left\{\frac{(M-1)}{3}\right\} \\ &\quad + 20 \cdot \log(\text{PAR}) - 10 \cdot \log(\text{OSR}) - 3 \\ &= 10 \cdot \log(M-1) - 10 \cdot \log(\text{OSR}) + 21 \end{aligned} \tag{25.8}$$

In Figure 25.5, we show the data requirement as a function of the number of levels in one carrier.

We assumed that all the carriers have been modulated with the same number of levels. In the DMT standard, the maximum number of bits that is allowed to be modulated on a single carrier is 15, that is, 32768-QAM. This QAM has a PAR of 2.45. The DMT signal that has a PAR of 5.3 increases the data converter requirement by 1.1 bits. Due to the influence of the excess bandwidth in a real implementation, the PAR of a single carrier system, can be somewhere between 3.6 ~ 4. Therefore, the use of DMT usually increases the data requirement by ~0.5 bits. This may not seem to be significant for data converters. However, it can increase the requirements on line drivers significantly [12].

25.3.1. Optimum Data Converters for ADSL

In the above discussions, we derived the data converter requirements from the system requirements. For more advanced digital transmission systems, the modulation (including number of modulated bits), the duplexing method, and/or the signal bandwidth vary according to the environment. A typical example is the ADSL. For most modern digital transmission systems, there is also a need to minimize the number of analog components. Therefore, higher performance data converters are preferred. This is essentially the same concept as in software radio. The question is how high performance is enough to meet a specific standard for a given practical environment. The following section is devoted to answering this question.

Optimum ADCs for ADSL. Without any analog filter in front of an ADC for either an FDM or an EC-based system, the ADC is supposed to quantize both the echo signal and the received signal. We need to find out the requirement on the ADC. Since the transformer does not change the SNR, we can assume the transformer ratio to be 1:1 without losing generality. If the hybrid network and some optional gain stages before the ADC do not introduce appreciable noise, the gain before the ADC does not change the SNR. We can assume a unity gain for simplicity in the derivation.

If the ADC is sampled at f_s, the power spectral density of the background noise including interference on the loop is $\mathrm{PSD_n}$, the transmit power spectral density is $\mathrm{PSD_{Tx}}$ (bandwidth from f_{t1} to f_t2), the echo rejection is assumed to be $T_e(f)$, the power spectral density of the signal sent from the other side is $\mathrm{PSD_{Rx}}$ (bandwidth from f_{r1} to f_{r2}), and the loop attenuation of the received signal is $T_l(f)$.

The echo power at the ADC input in dBm is, therefore, given by

$$\begin{aligned} P_{\text{echo}} &= 10 \cdot \log \left\{ \int_0^{f_s/2} 10^{\mathrm{PSD_{Tx}}/10} \cdot 10^{-T_e(f)/10} \cdot \mathrm{d}f \right\} \\ &= 10 \cdot \log \left\{ \int_{f_{t_1}}^{f_{t2}} 10^{\mathrm{PSD_{Tx}}/10} \cdot 10^{-T_e(f)/10} \cdot \mathrm{d}f \right\} \\ &= \mathrm{PSD_{Tx}} - T_e + 10 \cdot \log(\mathrm{BW_{Tx}}) \end{aligned} \tag{25.9}$$

where $\mathrm{BW_{Tx}}$ is the transmit bandwidth. In the above derivation, we have used the averaged transmit PSD in dBm/Hz and the averaged echo rejection $T_{e(f)}$ in dB.

The power of the received signal excluding the echo at the ADC input in dBm is given by

$$\begin{aligned} P_{\mathrm{Rx}} &= 10 \cdot \log \left\{ \int_0^{f_s/2} 10^{\mathrm{PSD_{Rx}}/10} \cdot 10^{-T_l(f)/10} \cdot \mathrm{d}f \right\} \\ &= 10 \cdot \log \left\{ \int_{f_{r_1}}^{f_{r2}} 10^{\mathrm{PSD_{Rx}}/10} \cdot 10^{-T_l(f)/10} \cdot \mathrm{d}f \right\} \\ &= \mathrm{PSD_{Rx}} - T_l + 10 \cdot \log(\mathrm{BW_{Rx}}) \end{aligned} \tag{25.10}$$

where $\mathrm{BW_{Rx}}$ is the received signal bandwidth. In the above derivation, we have used the averaged received PSD in dBm/Hz and the averaged line attenuation $T_{l(f)}$ in dB.

The total signal power in dBm at the ADC input is, therefore, given by

$$P_{\mathrm{sig}} = 10 \cdot \log \left\{ 10^{P_{\mathrm{echo}}/10} + 10^{P_{\mathrm{Rx}}/10} \right\} \tag{25.11}$$

The total line noise power in dBm at the ADC input is given by

$$P_{\mathrm{n}} = 10 \cdot \log \left\{ \int_0^{f_s/2} 10^{\mathrm{PSD_n}/10} \cdot \mathrm{d}f \right\} = \mathrm{PSD}_{\mathrm{n}l} + 10 \cdot \log \left(\frac{f_s}{2} \right) \tag{25.12}$$

It appears that the SNR requirement for the ADC is given by the ratio of the signal power vs noise power at the ADC input. However, the PAR significantly increases the requirement due to the fact that the SNR measure of an ADC is based on a single sinusoidal input that has a PAR of 1.4. Therefore, we have [11]

$$\mathrm{SNR_{ADC}} = P_{\mathrm{sig}} - P_{\mathrm{n}} + 20 \cdot \log \left(\frac{\mathrm{PAR}}{1.4} \right) \tag{25.13}$$

(Strictly speaking, a margin should be included considering SNR degradation due to the ADC quantization noise.) Now, we need to find out the SNR requirement needed for the ADC as a function of the echo rejection T_e and the background noise power spectral density $\mathrm{PSD_n}$.

Different lengths of the loop introduce different loop attenuation of the receive signal. The smallest attenuation occurs when the loop length is zero. By assuming a zero line attenuation $T_l = 0\,\mathrm{dB}$, we can find out the maximum SNR needed for the ADC. However, the SNR or carrier-to-noise ratio (CNR) of each sub-carrier only needs to be large enough to demodulate a maximum 15-bit QAM signal with a given bit error rate for ADSL. By using equation (25.1), the SNR for the QAM is required to be larger than 55 dB for an error probability better than 10^{-7}. Considering a 3-dB coding gain and a 6-dB noise margin, the

SNR only needs to be 55 – 3 + 6 = 58 dB to guarantee an error rate less than 10^{-7}. Therefore, the received maximum signal power spectral density only needs to be $\mathrm{PSD_n} + 58\,\mathrm{dBm/Hz}$. If the loop is extremely short, we can reduce the transmit power as the standard suggests.

Therefore, we have the SNR requirement for the ADC for ADSL without any analog filter, given [11] by

$$\begin{aligned}\mathrm{SNR_{ADC}} = 10 \cdot \log \Big\{ & 10^{(\mathrm{PSD_{Tx}} - T_e + 10 \cdot \log(\mathrm{BW_{Tx}}))/10} \\ & + 10^{(\mathrm{PSD_n} + 58 + 10 \cdot \log(\mathrm{BW_{Rx}}))/10} \Big\} \\ & - \mathrm{PSD_n} - 10 \cdot \log\left(\frac{f_s}{2}\right) + 11.6 \end{aligned} \tag{25.14}$$

Notice that the quantization noise contribution is not factored into the above equations for simplicity. We use the noise margin in the following discussions to account for it as well for other influences.

In the above discussion, we have assumed that the ADC is sampled at f_s and the signal bandwidth is $f_s/2$. If the signal bandwidth is much lower than $f_s/2$, the ADC needs less dynamic range. Since the ADC noise floor is governed by the input signal, we can integrate the noise within the receive band to get the total in-band ADC noise. The peak input signal power does not vary; therefore, we have the SNR requirement on an oversampling ADC given by

$$\begin{aligned}\mathrm{SNR_{ADC}} = 10 \cdot \log \Big\{ & 10^{(\mathrm{PSD_{Tx}} - T_e + 10 \cdot \log(\mathrm{BW_{Tx}}))/10} \\ & + 10^{(\mathrm{PSD_n} + 58 + 10 \cdot \log(\mathrm{BW_{Rx}}))/10} \Big\} \\ & - \mathrm{PSD_n} - 10 \cdot \log(\mathrm{BW_{Rx}}) + 11.6 \end{aligned} \tag{25.15}$$

If the echo signal dominates, we have

$$\begin{aligned}\mathrm{SNR_{ADC}} &= \mathrm{PSD_{Tx}} - T_e + 10 \cdot \log(\mathrm{BW_{Tx}}) \\ &\quad - \mathrm{PSD_n} - 10 \cdot \log(\mathrm{BW_{Rx}}) + 11.6 \\ &= \mathrm{PSD_{Tx}} - T_e - \mathrm{PSD_n} + 10 \cdot \log\left(\frac{\mathrm{BW_{Tx}}}{\mathrm{BW_{Rx}}}\right) + 11.6 \end{aligned} \tag{25.16}$$

Optimum ADC for ADSL-CO. At the ADSL-CO, we have [13]

- $\mathrm{PSD_{Tx}} = -40\,\mathrm{dBm/Hz}$
- Maximum $\mathrm{BW_{Tx}} = 1104 - 26 = 1078\,\mathrm{kHz}$
- Maximum $\mathrm{BW_{Rx}} = 138 - 26 = 112\,\mathrm{kHz}$.

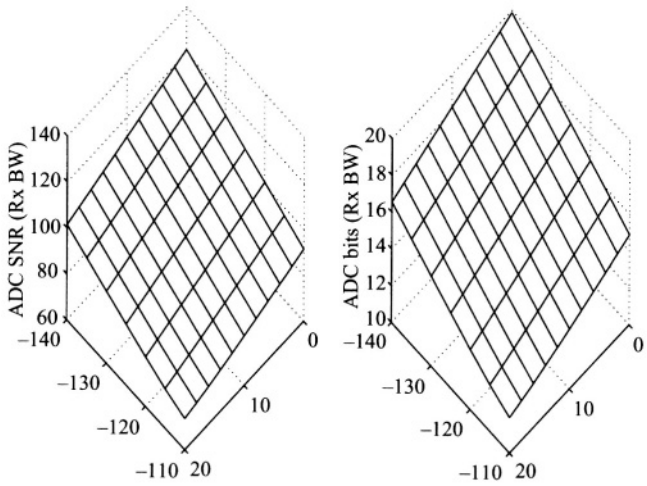


Figure 25.6. ADSL-CO ADC requirements vs echo rejection and background noise. X-axis: background noise power spectral density in dBm/Hz; Y-axis: echo rejection in dB.

We plot the SNR and number of bit requirements in Figure 25.6. It is seen that with a small background noise floor (– 140 dBm/Hz as specified as the background thermal noise floor for ADSL) and poor echo rejection, the ADC requirement is formidably high. However, with good echo rejection that is usually feasible at the central office side, and large noise floor (due to the interferences from other lines and from other services), the ADC is realizable.

Optimum ADC for ADSL-CP. At the ADSL-CP, we have [13]

- $\text{PSD}_{\text{Tx}} = -38\,\text{dBm/Hz}$
- Maximum $\text{BW}_{\text{Rx}} = 1104 - 26 = 1078\,\text{kHz}$
- Maximum $\text{BW}_{\text{Tx}} = 138 - 26 = 112\,\text{kHz}$.

We plot the SNR and number of bits requirements in Figure 25.7. It is seen that with a small loop noise floor and poor echo rejection, the ADC requirement is formidably high especially considering the bandwidth.

Optimum DACs. In the above discussions, we assumed that the echo signal would only increase the received signal power. In reality, the noise floor in the echo signal may be another limitation to achieving a high SNR. The noise at the ADC input consists of two parts, one being the contribution due to the line noise and the other being the contribution due to the DAC assuming the noise contributions from the line driver and hybrid network are negligible.

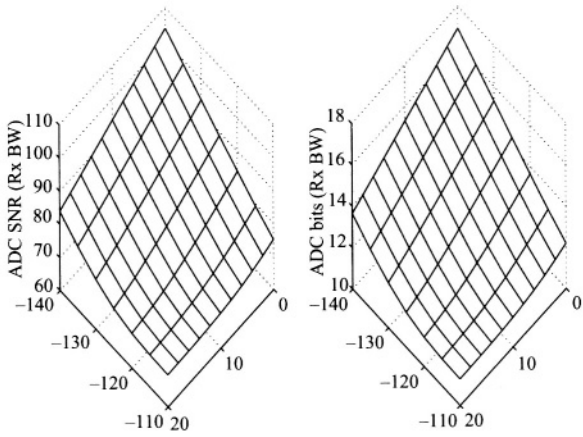


Figure 25.7. ADSL-CP ADC requirements vs echo rejection and background noise. X-axis: background noise power spectral density in dBm/Hz; Y-axis: echo rejection in dB.

To calculate the noise contribution from the DAC, we need to calculate the voltage gain from the DAC output to the ADC input. The gain consists of the gain of the line driver, echo rejection by the hybrid network and the gain stage before the ADC. In a practical design, ADCs and DACs usually have a comparable signal range and we usually set the gain such that the ADC dynamic range is fully utilized. If the echo signal dominates at the ADC input, the total voltage gain from the DAC output to the ADC input is unity. If the receive signal is not negligible compared to the echo signal, the total gain from the DAC to the ADC is less than unity. Therefore, as long as the DAC has comparable or smaller noise floor than the ADC, the noise floor in the DAC will not degrade the receiver performance significantly (< 3 dB). Since the ADC noise floor is set by the $\mathrm{PSD_n}$, the DAC noise floor should be less than $\mathrm{PSD_n}$.

If we integrate the noise within the Tx band, and compare it to the total received signal (since ADC and DAC have the same signal swing) we can derive the SNR requirement for the DAC, that is,

$$\begin{aligned}\mathrm{SNR_{DAC}} &= P_{\mathrm{sig}} - P_{\mathrm{n}} + 20 \cdot \log\left(\frac{\mathrm{PAR}}{1.4}\right) \\ &= 10 \cdot \log\left\{10^{(\mathrm{PSD_{Tx}} - T_e + 10 \cdot \log(\mathrm{BW_{Tx}}))/10} \right. \\ &\quad \left. + 10^{(\mathrm{PSD_n} - T_l + 10 \cdot \log(BW_{\mathrm{Rx}}))/10}\right\} - \mathrm{PSD_n} - 10 \cdot \log(\mathrm{BW_{Tx}}) \\ &\quad + 20 \cdot \log\left(\frac{\mathrm{PAR}}{1.4}\right) = \mathrm{PSD_{Tx}} - \mathrm{PSD_n} - T_e + 11.6 \qquad (25.17)\end{aligned}$$

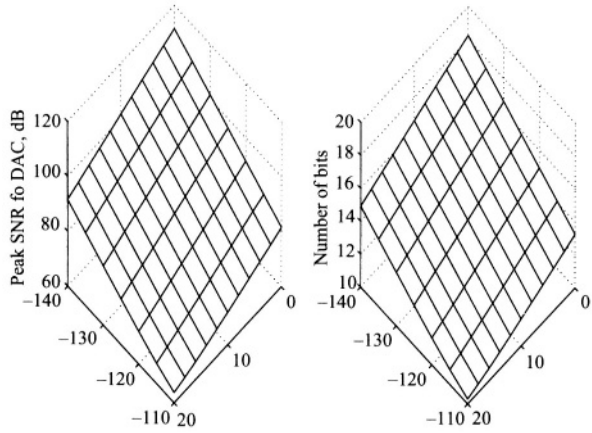


Figure 25.8. ADSL-CP DAC requirements vs echo rejection and background noise. X-axis: background noise power spectral density in dBm/Hz; Y-axis: echo rejection in dB.

In the above derivation, we have assumed that the echo dominates at the ADC input. If the echo signal does not dominate, the DAC requirement is reduced since the gain from the DAC to the ADC is less than unity assuming both ADC and DAC have the same signal swing. (The ADC input is scaled such that it can accommodate both the echo signal and the Rx signal.)

Notice that we only require that the DAC noise within the received band be governed by equation (25.17). Outside the received band, the noise floor is governed by how many bits are modulated on each sub-carrier according to the ADSL standard.

Optimum DAC for ADSL-CO. At the ADSL-CO, we have [13],

- $\text{PSD}_{\text{Tx}} = -40\,\text{dBm/Hz}$
- Maximum $\text{BW}_{\text{Tx}} = 1104 - 26 = 1078\,\text{kHz}$
- Maximum $\text{BW}_{\text{Rx}} = 138 - 26 = 112\,\text{kHz}$.

The simulated DAC requirement is shown in Figure 25.8.

Optimum DAC for ADSL-CP. At the ADSL-CP, we have [13],

- $\text{PSD}_{\text{Tx}} = -38\,\text{dBm/Hz}$
- Maximum $\text{BW}_{\text{Rx}} = 1104 - 26 = 1078\,\text{kHz}$
- Maximum $\text{BW}_{\text{Tx}} = 138 - 26 = 112\,\text{kHz}$.

The simulated DAC requirement is shown in Figure 25.9.

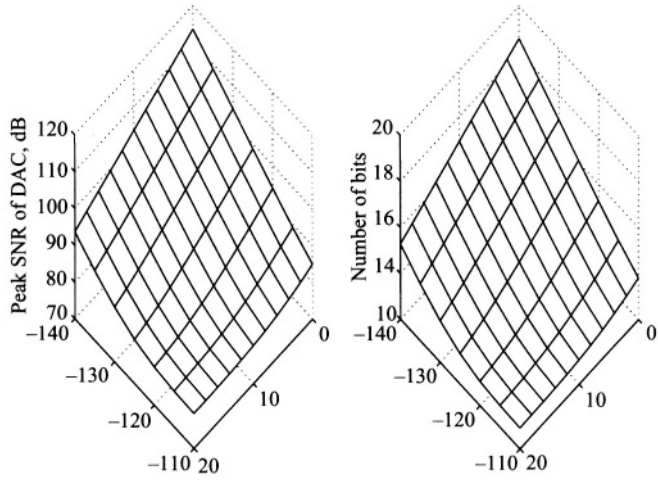


Figure 25.9. ADSL-CO DAC requirements vs echo rejection and background noise. X-axis: background noise power spectral density in dBm/Hz; Y-axis: echo rejection in dB.

25.3.2. Function of Filtering

At the receive side, the use of the filter (Rx filter) can eliminate the echo signal for FDM systems and reduce the echo signal power for EC systems if the Tx bandwidth is larger than the Rx bandwidth. The total signal seen by the ADC is reduced; therefore, the ADC requirement can be reduced significantly. If there is no echo signal at the ADC, the ADC only needs to quantize the receive signal. The minimum received SNR is determined by the system requirement such as bit rate and bit error rate as given in (2)–(8). For DSL systems, the bit rate is usually a function of the loop length. The maximum bit rate determines the ADC requirements.

Clearly, trade-offs can be made between ADC dynamic requirement and Rx filter attenuation.

For ADSL-DMT applications, assuming that the echo signal dominates at the ADC input and the Rx filter has a stopband attenuation of T_{RxF} dB, by using equations (25.9) and (25.17), we have

$$\mathrm{SNR}_{\mathrm{ADC}} = \max \left\{ \begin{array}{l} \mathrm{PSD}_{\mathrm{Tx}} - T_{\mathrm{e}} - T_{\mathrm{RxF}} - \mathrm{PSD}_{\mathrm{n}} + 10 \cdot \log \left(\dfrac{\mathrm{BW}_{\mathrm{Tx}}}{\mathrm{BW}_{\mathrm{Rx}}} \right) + 11.6 \\ 10 \cdot \log (M - 1) + 21 \end{array} \right\} \tag{25.18}$$

Notice that the above formula holds even if the Rx filter does not have a sharp transition band. In this case, the stopband attenuation T_{RxF} can be interpreted as the attenuation on the echo signal power by the Rx filter. If the

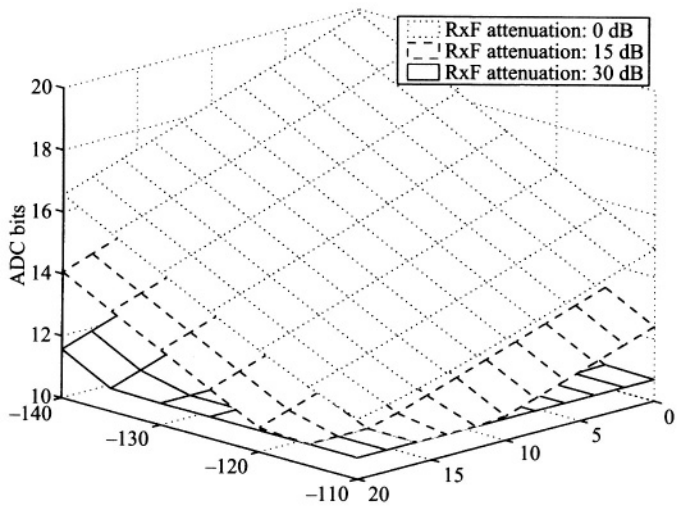


Figure 25.10. ADSL-CO ADC requirements vs echo rejection and background noise for different Rx filter attenuation. X-axis: background noise power spectral density in dBm/Hz; Y-axis: echo rejection in dB. No margin or coding gain was considered.

echo signal is completely eliminated by the Rx filter, the ADC requirement is determined by the system requirement such as bit rate and bit error rate as given in formula (25.9).

For instance, for ADSL-CO applications where the maximum number of bits per bin is 15, the use of an Rx filter can significantly reduce the ADC requirement as shown in Figure 25.10. The attenuation of the Rx filter is treated as the total signal power reduction in the stop band.

For the Tx filter in an FDM system, the purpose is to attenuate the residue signal and noise within the Rx band such that the noise contribution from the Tx path within the Rx band is smaller than the received line noise floor. Similar results can be obtained for DACs for ADSL-DMT applications by using formulas (25.9) and (25.18). It is given by

$$\mathrm{SNR_{DAC}} = \max \left\{ \begin{array}{l} \mathrm{PSD_{Tx}} - T_e - T_{\mathrm{TxF}} - \mathrm{PSD_n} + 11.6 \\ 10 \cdot \log (M-1) + 21 \end{array} \right\} \qquad (25.19)$$

where T_{TxF} is the Tx filter attenuation in the stopband.

For instance, for ADSL-CO applications where the maximum number of bits per bin is 15, the use of aTx filter can significantly reduce the DAC requirement as shown in Figure 25.11.

For applications where there is no guard band between the Tx and Rx band, the Tx filter needs to be sharp in order to maximize the usable Tx and Rx

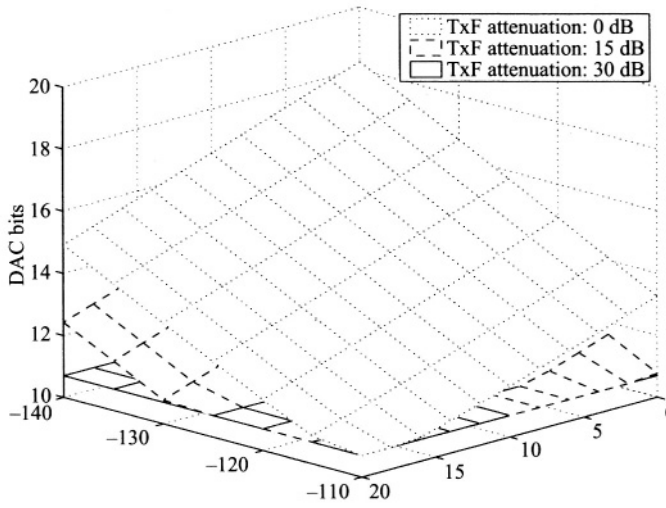


Figure 25.11. ADSL-CO DAC requirements vs echo rejection and background noise for different Tx filter attenuation. X-axis: background noise power spectral density in dBm/Hz; Y-axis: echo rejection in dB. No margin or coding gain was considered.

frequencies. Otherwise, the frequencies at or close to the transition band cannot be utilized by the system. This is the most significant difference between the functions of the Rx and Tx filter. The Rx filter is only needed to reduce the echo signal such that the dynamic range on the ADC can be reduced. There is no stringent requirement on the transition band. Therefore, the Tx filter is usually more difficult to design due to the requirement on the transition band.

25.4. Circuit Considerations

After having chosen the process and considered system partitioning and trade-offs, the rest is circuit design. There are many design considerations and trade-offs in actually designing the AFE chip.

25.4.1. Oversampling vs Nyquist Data Converters

It is known that oversampling data converters are well suited for low bandwidth applications. For ADSL applications where the maximum bandwidth can be up to 1.1 MHz, the clock frequency for an oversampled data converter can be high depending on the architecture. Both oversampling data converters and Nyquist data converters have been used in ADSL products [5–9].

With oversampling data converters, we can have higher dynamic range reducing the filtering requirement as discussed above. However, higher clock frequency could make the analog design more difficult. Even the digital decimation filter can be power hungry if it is implemented in the AFE

chip where the process is not deep sub-micron. Special techniques can be employed to reduce the power dissipation and maintain programmability [14] by combining recursive [15–17] and non-recursive architecture [18–19]. The most troublesome is the oversampling DAC for high bandwidth applications such as ADSL CO.

An oversampling DAC relies on the analog filters to remove the out-of-band noise. To avoid slewing on the analog continuous-time filters, sampled-data filters such as switched-capacitor (SC) or switched-current (SI) filters are needed. SC or SI filters operating at high clock frequency are very difficult to design. For example, the *kT/C* noise from every sampled capacitor and thermal noise of every operational amplifier (op-amp) contribute to the output noise. Due to the large oversampling ratio, the capacitance spread could be large and/or the noise gain from some internal nodes to the outputs could be far larger than the signal gain. All these make low-noise high-frequency SC or SI filters extremely difficult to design. One way to reduce the clock frequency for SC or SI filters is to use a passive SC or SI FIR decimation filter and operate the SC or SI filter at a lower clock frequency [20–21]. However, the mismatch introduces inaccuracy in the FIR coefficients. When decimated, higher frequency spurs and noise will be aliased into the baseband. To avoid this problem, the use of intelligent clocking can make the FIR coefficient insensitive to the mismatch [22].

Unlike high-order oversampling ADCs, high-order oversampling DACs suffer from limit cycle [20]. If a single tone or multi-tone is applied to an oversampling DAC, the tones due to the limit cycle appear most likely close to half of the sampling frequency. These tones are usually not harmonically related but signal dependent. Any non-ideality in the analog circuits can cause the tones to fold back into the baseband, degrading the performance. These kind of folded-back tones that are signal dependent can introduce bit error even in the data mode. Adding a dithering signal even during data mode could improve the system performance [23].

The sensitivity to clock jitter is determined by the maximum signal amplitude change between two successive samples in the interface of continuous-time and discrete-time circuits [20]. Due to the noise shaping in the oversampling DAC, the signal amplitude change is very large. This is the reason why discrete-time filters are needed to filter out the high frequency noise and reduce the signal amplitude change. This reduces the sensitivity to the clock jitter as well as the distortion due to the slewing in the continuous-time filter. At high speed, high-order discrete-time filters are noisy and power hungry. A trade-off has to be made.

In Figure 25.12, we show the performance degradation as a function of clock jitter in sampling a 150-kHz sinusoid. The OSDAC is a single-stage fourth-order noise shaper. The clock frequency is assumed to be 70 MHz and the

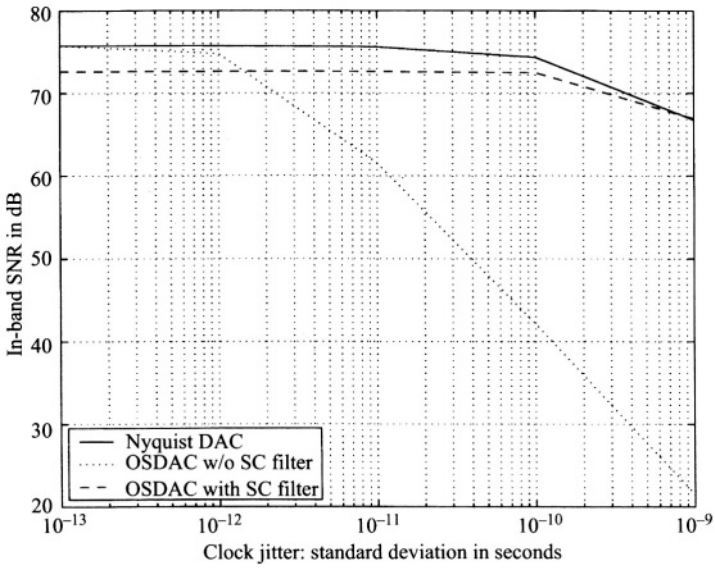


Figure 25.12. DAC performance vs clock jitter.

oversampling ratio is 32. The discrete-time filter is a combination of a passive SC FIR decimation filter and a SC filter. The Nyquist DAC has an equivalent resolution of the OSDAC. Notice that with very low clock jitter, the OSDAC with SC filter has lower performance. This is due to the non-ideal SC FIR decimation filter that introduces aliased noise. The SC filter attenuates most of the quantization noise; therefore, the oversampling DAC with the SC filter has the same sensitivity to clock jitter as the Nyquist DAC.

It is seen that without adequate discrete-time filtering, OSDACs are very sensitive to clock jitter.

Compared to Nyquist data converters, oversampling data converters are operated at a much higher clock frequency for the same applications. Higher clock frequency imposes much tougher requirement on the reference buffer as well as the buffer for the ADC. In an AFE chip, they have to be on-chip. With higher clock frequency, the SC load behaves as a low impedance, driving 'low impedance' load could cause the referenced voltage drop unless compensation techniques are used [24]. To avoid performance degradation in the signal buffer, the best approach is to have a switching network to minimize the interaction from sample to sample, that is, the charging and discharging current that the buffer needs to provide is signal independent.

In general, for ADSL applications where the maximum signal frequency is 1.1 MHz, both oversampling and Nyquist data converters can be used. The major disadvantage of the Nyquist data converter is its relatively lower dynamic

range. For higher bandwidth application such as very high data rate DSL (VDSL), Nyquist data converter (or a combination of Nyquist and oversampling data converter) is probably the better choice.

25.4.2. SI vs SC

To design sampled-data circuits such as ADCs and filters, either SI or SC techniques can be used. The summary of comparison between SI and SC technique is given in [11,25].

SI circuits

- Require no high-gain amplifiers and no linear capacitors that makes the technique suitable for implementation in a digital CMOS process.
- Due to their simplicity and the slightly smaller capacitive loads, it is easier to design high bandwidth circuits using SI techniques.
- Due to the simple structure of the basic SI circuits, it is relatively easy to design SI circuits at lower supply voltage.

SC-circuits

- Since the voltage swing in SC circuits is larger than in SI circuits, the dynamic range is better in SC circuits.
- When using the bottom-plate sampling, SC circuits are less sensitive to clock feedthrough errors, and aperture errors are almost completely removed. SC circuits usually have lower distortion.
- The matching accuracy in SC circuits is usually better than in SI circuits.

In general, SC circuits offer higher performance than SI circuits. For high-performance design, the SC technique is usually preferred. In most reported DSL papers and products, the SC technique is used.

25.4.3. Sampled-Data vs Continuous-Time Filters

Sampled-data filters usually have accurate cut-off frequency and low temperature drift since the cut-off frequency is determined by the clock frequency and the device ratios. The major drawback of sampled-data filters is the thermal noise. For instance, for SC filters, kT/C of every sampled capacitor and the thermal noise of every op-amp contribute to the total output noise. Unlike in continuous-time filters, the op-amp noise is folded due to the sampling in SC filter. The same statement holds true for SI filters [25]. For low-noise applications, continuous-time filters are preferred. Notice that the noise gain could be far larger than the signal gain from certain internal nodes to the output for both sampled-data and continuous-time active filters.

For oversampled systems where the ratio of the clock frequency and the cut-off frequency is large, the spread in capacitance for SC filters or the spread in transistor sizes for SI filters are large unless a passive FIR decimation filter is used. Large spread usually limits the highest operating frequency due to the increase in the capacitance value or transistor size. (For any given process, we cannot make the components arbitrarily small due to the processing, parasitic and matching consideration.) There are techniques to reduce the capacitance spread [26]. However, they usually either introduce settling-chain between two op-amps limiting the high-frequency performance or have large noise peaking. Also for high clock frequencies, the distortion performance is difficult to meet.

In general, sampled-data filters should be avoided except for oversampling DACs. For oversampling DACs, sampled-data filters have to be used to reduce the high-frequency noise before driving continuous-time filters. Otherwise, large distortion could occur in the continuous-time filters due to slewing caused by the large step change. The drawback of integrated continuous-time filters is the inaccuracy and temperature drift of the cut-off frequency that has to be trimmed or compensated.

25.4.4. Gm-C vs RC filters

Gm-C filters are usually attractive for high-frequency applications. The serious drawback of the Gm-C filters is the distortion. Active RC filters can usually achieve 20 ~ 30 dB lower distortion compared to Gm-C filters. For low distortion applications, RC filters are the right choice.

25.5. Conclusions

In this chapter, the author has described analog front-end design considerations for DSL. In order to have the optimum system, analog engineers need to understand the whole system and assess different options at the system level. For an actual mixed-signal chip design, analog engineers also face many options. Trade-offs between external and internal components, analog and digital, and trade-offs among different circuits and circuit techniques have to be made in order to have a competitive mixed-signal chip for a specific communication system.

There are always different approaches to solving the same problem. The discussions the author has presented and the statements that the author has made may be different from others. However, most of the results have been used in designing several AFE chips for DSL that succeeded in tough competitions and most of them are currently in high-volume mass production. This indicates that the author's approach is at least one viable approach.

Acknowledgments

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Chapter 26

LOW NOISE DESIGN

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26.1. Introduction

Noise plays an important role in analog circuit design, since it is involved in many design trade-offs. For this reason, it asks for a careful treatment by the designer; at one side, circuits have to realize the required signal processing, at the other side, the circuit components produce noise that corrupts the information.

A frequently applied approach to handle such conflicting requirements is to establish an acceptable trade-off between the various design requirements. Finding such a trade-off, however, is usually a difficult and time-consuming task that for large circuits can only be found through numerical optimization, for example, as in [1].

An often more attractive and effective approach is to eliminate the conflict between design requirements, such that each of them can be optimized separately. Such an "orthogonalization" of requirements can be achieved by assigning conflicting requirements to different parts of the circuit. These can then be separately optimized. The strength of this approach is that the design procedure becomes straightforward, without the need of complicated optimization techniques.

In this chapter, we will show how the noise performance of various types of circuits can be improved by elimination of trade-offs between noise and other requirements. Section 26.2 briefly reviews some useful tools for the analysis of the circuit noise behavior. Sections 26.3–26.5 discuss the design techniques to minimize the noise level in amplifiers, harmonic oscillators and relaxation oscillators, respectively.

26.2. Noise Analysis Tools

Noise analysis tools are indispensable in optimization of the noise behavior of circuits. They reveal the dominant causes of the circuit noise production, and also indicate possibilities to minimize it. In this section, we briefly review some noise analysis techniques that are very useful in the synthesis of low noise circuits.

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Generally, the purpose of a noise analysis is to determine the equivalent input/output Signal-to-Noise Ratio (SNR) of a circuit. To this extent, all noise produced by the various circuit components is thought to be concentrated into a single noise source, the so-called "equivalent" noise source. The power contents of this source equal the noise power produced by the entire circuit, and can be obtained through standard techniques [2,3]. The remainder of this section will concentrate on the determination of this equivalent noise source from the various circuit noise processes.

26.2.1. Equivalent Noise Source

The equivalent input noise source replaces all other noise sources in the circuit; once this source is obtained, the remainder of the circuit can be considered "noise free". Consequently, it may be viewed as the resultant of transforming all circuit noise sources to a single position, as illustrated by Figure 26.1.

The noisy circuit is represented as a noise-free multi-port, connected to independent noise sources $v_{n,2i}$ and $i_{n,2i+1}$ that represent the various circuit noise processes. The equivalent noise source $e_{n,eq}$ is connected to one of the circuit ports (usually the input or output) and equals the resulting voltage/current at this port due to the noise sources $v_{n,2i}$ and $i_{n,2i+1}$. Usually, the circuit behaves (small-signal) linear with respect to the noise, such that the (time-domain) transfer from $v_{n,2i}$ and $i_{n,2i+1}$ to $e_{n,eq}$ can be represented by an impulse response:

$$e_{n,eq}(t) = \sum_{i=1}^{n} h_{2i} * v_{n,2i}(t) + \sum_{k=0}^{m} h_{2k+1} * i_{n,2k+1}(t) \qquad (26.1)$$

where "*" denotes a convolution. Consequently, the noise transformation essentially consists of calculating the impulse responses $h_k(\tau)$, or equivalently the frequency transfers $H_k(j\omega)$. This can be done through combination of the four types of transforms discussed below.

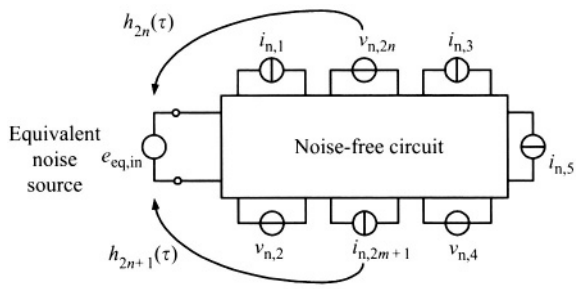


Figure 26.1. Representation of noisy circuit as a noise-free multi-port network, connected to multiple noise sources.

26.2.2. Transform-I: Voltage Source Shift

The voltage source shift (V-shift) is a transform that enables to move (noise) voltage sources through the circuit without changing the maze equations defined by the Kirchhoff Voltage Law (KVL). Its principle is visualized in Figure 26.2.

The original (noise) source v_n is shifted out of the branch between the nodes 1,4 into the two other branches connected to node 4; the ones between 2,4 and 3,4. In order to guarantee that the KVLs of the mazes I, II and III, associated to node 4 remain unchanged, the new sources $v_{n,1}$ and $v_{n,2}$ have to be exactly equal to each other, that is, fully correlated, and to the original source v_n.

26.2.3. Transform-II: Current Source Shift

The dual transform of the V-shift is the I-shift, which allows moving current (noise) sources through the circuit without changing the nodal equations defined by the Kirchhoff Current Law (KCL). The principle is depicted in Figure 26.3.

The original (noise) current source i_n is redirected from the branch between nodes 1,2 through the sources $i_{n,1}$ and $i_{n,2}$ between nodes 1,3 and 2,3. In order to keep the KCLs of the nodes 1, 2 and 3 unchanged, $i_{n,1}$ and $i_{n,2}$ have to be exactly equal to each other (fully correlated) and to i_n.

26.2.4. Transform-III: Norton–Thévenin Transform

The equivalence of the well-known theorems of Norton and Thévenin can be used to transform a (noise) current source into a (noise) voltage source and vice versa. This type of transform does essentially not move sources through

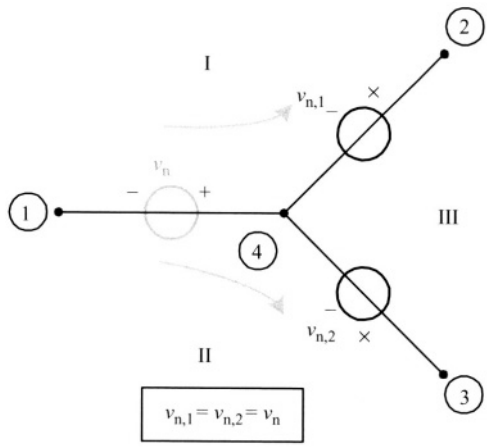


Figure 26.2. V-shift transform.

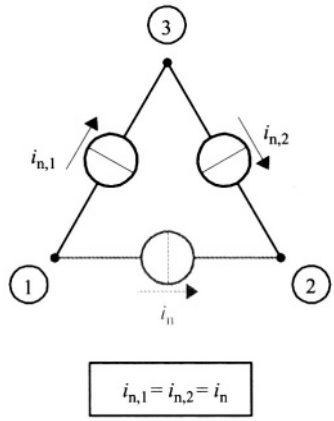


Figure 26.3. I-shift transform.

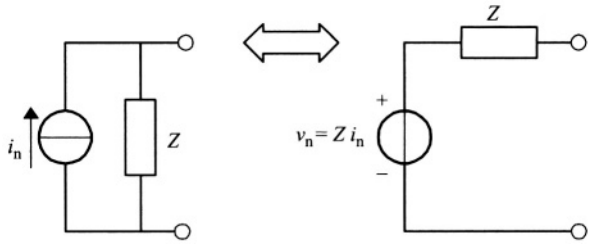


Figure 26.4. Norton–Thévenin transform.

the amplifier network, but is used to switch between the V-shift and I-shift. An example of its application is depicted in Figure 26.4.

The current source i_n and the voltage source v_n have a one-to-one correspondence through the impedance Z. They are fully correlated. Note that this transformation does change the KVLs and KCLs of the circuit; it exchanges a circuit branch for a circuit node, and vice versa. For this reason, the Norton–Thevenin transform, in combination with the V-shift and I-shift can be used to eliminate a voltage source from a maze, or a current source from a node.

26.2.5. Transform-IV: Shift through Twoports

The three transformations we have considered so far are all concerned with two-terminal elements (oneports) only. If a network consists entirely of such elements, these three transforms are all we need to determine the equivalent input noise.

Many circuits, however, also contain elementary twoports, controlled sources (included in transistor models) or a nullor, that cannot be replaced

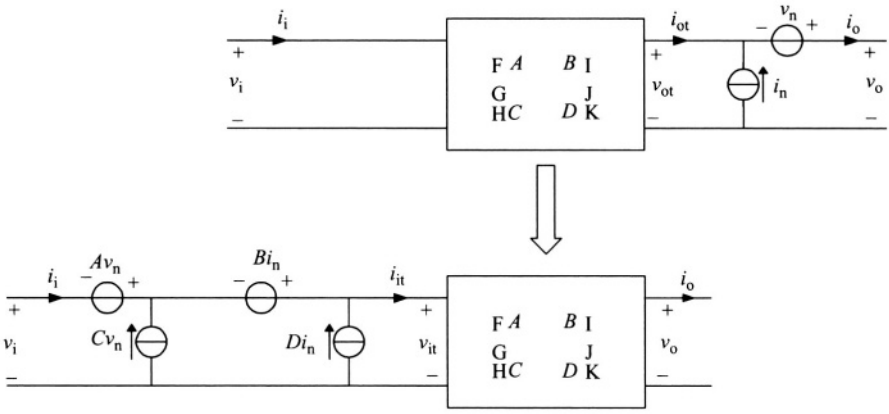


Figure 26.5. Transformation of noise sources through a twoport.

by any combination of oneports. For such networks, we need an additional transform: the twoport shift. This transformation is illustrated by Figure 26.5.

The output voltage v_o and the output current i_o of the twoport are mutilated by a noise voltage v_n and noise current i_n, respectively, as depicted in the upper part of the figure. The purpose of the twoport shift transform is to obtain the equivalent input noise source that yields this output noise. The result depicted in the lower part of the figure is easily obtained from the chain matrix equation for the twoport,

$$\begin{pmatrix} v_{it} \\ i_{it} \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \begin{pmatrix} v_{ot} \\ i_{ot} \end{pmatrix} \tag{26.2}$$

and substitution of v_i, i_i, v_o, i_o, v_n and i_n. Observe that the output noise voltage source v_n is transformed into an input noise voltage source Av_n and a noise current source Cv_n that are fully correlated. Likewise, the output noise current source i_n transforms into an input noise voltage source Bi_n and an input noise current source Di_n.

26.3. Low-Noise Amplifier Design

Amplifiers are the hearts of many electronic circuits and systems. Besides their direct use to increase the power content of small information signals, in order to make them less vulnerable to noise, they are also used as key building blocks in, for example, filters, oscillators and bandgap references.

The main trade-off to be made in amplifier designs is among the amplifier noise production, distortion generation and its bandwidth. Especially when a high-performance level is required, it is difficult (or even impossible) to satisfy all requirements simultaneously within one amplifier stage. For this reason,

we will attempt to make these requirements "orthogonal" and optimize them separately. A particularly suitable concept that enables such an "orthogonalization" is overall negative feedback; it localizes the various design requirements in different parts of the amplifier circuit. This section will, therefore, focus on the design of low-noise negative feedback amplifiers.

26.3.1. Design of the Feedback Network

Essentially, a negative feedback amplifier consists of two parts; an active part that provides the amplification, and a feedback network that accurately fixes the overall gain to a predefined value. The active part consists of a combination of transistors that approximates a "nullor"; a circuit theoretical twoport element with infinite gain (all elements of its chain matrix equal zero).

In theory, the nullor and the feedback network establish complete orthogonality between the overall amplifier gain at one side, and requirements with respect to noise, distortion and bandwidth at the other side. The feedback network only fixes the overall gain, and has no effect on the noise, distortion or bandwidth. The nullor implementation completely determines the noise, distortion and bandwidth of the amplifier and has no influence on the overall gain. Further, inside the nullor, the noise, distortion and bandwidth requirements can be made orthogonal by localizing them to different stages, as will be discussed in Subsection 26.3.2. The idealized amplifier configurations that establish such a perfect orthogonalization, consisting of a nullor and feedback networks of ideal transformers and gyrators are depicted in Figures 26.6 and 26.7.

The amplifier in Figure 26.6 comprises all four possible feedback loops. It realizes an accurate power gain and has an independently configurable input and output impedance. Figure 26.7 depicts the four types of ideal single-loop amplifiers. The ideal transformers and gyrators in these configurations only determine the amplifier gain, and have no effect on the noise, distortion or bandwidth.

Unfortunately, ideal transformers and gyrators are not available, such that, in practice, a designer has to resort to amplifiers using impedance feedback networks. Figure 26.8 depicts the impedance feedback amplifiers corresponding to the ideal types in Figure 26.7.

An important difference with the ideal transformer–gyrator configurations is that the orthogonality between the design requirements in these configurations is no longer perfect. The feedback impedances disturb the orthogonality in three different ways:

- They generally produce noise.
- They magnify the noise produced by the nullor.
- They increase the distortion and reduce the bandwidth.

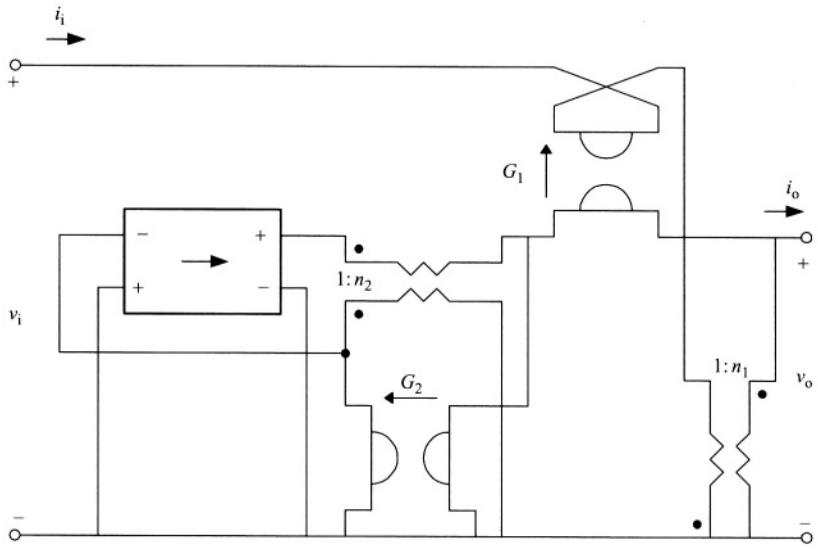


Figure 26.6. Ideal amplifier configuration comprising all possible feedback loops.

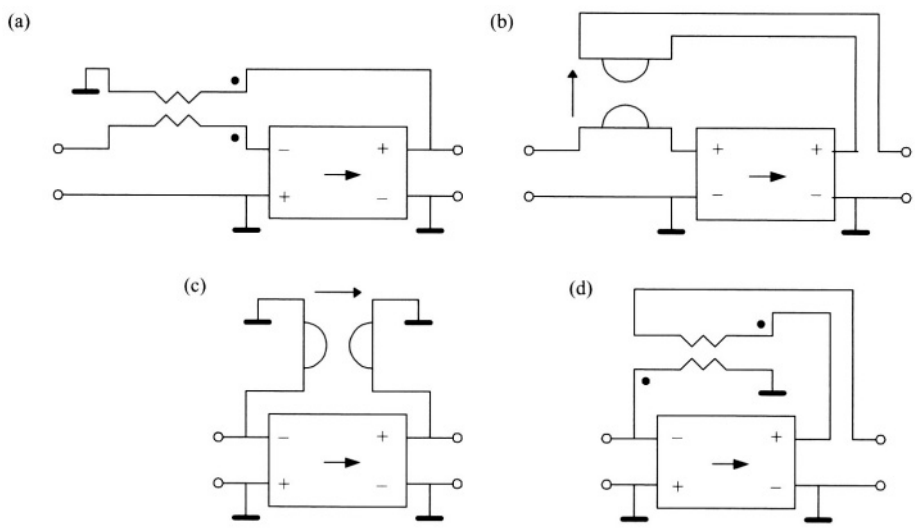


Figure 26.7. The four types of ideal single-loop amplifiers. (a) Voltage amplifier, (b) transconductance amplifier, (c) transimpedance amplifier and (d) current amplifier.

Noise production by the feedback network. This way of affection is rather obvious. If the feedback network contains resistors, it will produce noise such that the amplifier noise production is no longer completely localized inside the nullor.

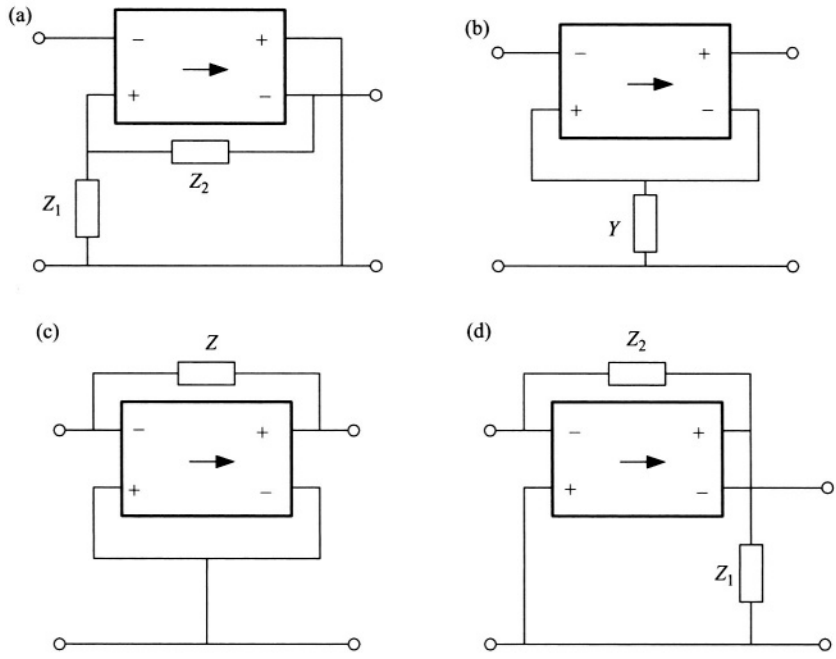


Figure 26.8. Single-loop amplifier configurations using impedance feedback (a) voltage amplifier, (b) transconductance amplifier, (c) transimpedance amplifier and (d) current amplifier.

Magnification of nullor noise. This contribution is less obvious. Even when the impedance feedback network contains no resistors (i.e. consists of capacitors and inductors), it still increases the amplifier noise by magnifying the nullor noise. The voltage amplifier in Figure 26.9 illustrates this effect.

The noise produced by the nullor is represented by the noise sources v_n and i_n. Using the analysis tools discussed in Section 26.2, the equivalent input noise source of the complete amplifier, $v_{n,eq}$ is found to equal:

$$v_{n,eq} = v_n + \left(Z_s + \frac{Z_1 Z_2}{Z_1 + Z_2} \right) i_n \tag{26.3}$$

This expression clearly shows that the feedback impedances Z_1 and Z_2 increase ("magnify") the contribution of i_n to the equivalent input noise source $v_{n,eq}$, even when they are capacitors or inductors. In an amplifier using transformer feedback, i_n would contribute to $v_{n,eq}$ through R_s only. It can be shown for the configurations in Figure 26.8 that the feedback network has the same effect on the amplifier noise as an impedance, equal to the output impedance, of the feedback network that is connected in series/parallel with the input signal

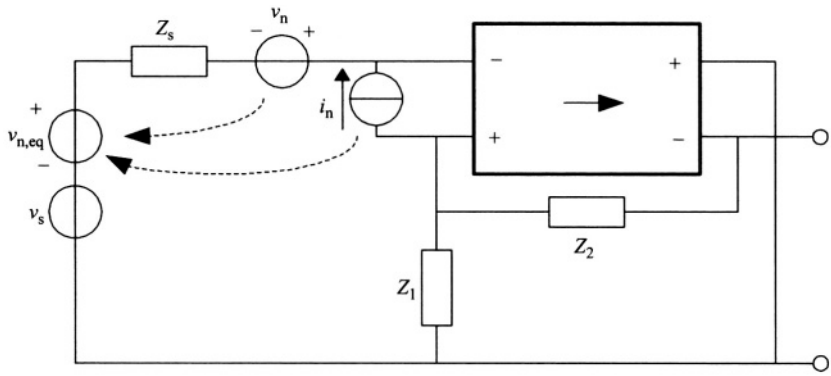


Figure 26.9. Magnification of the nullor noise by the feedback impedances.

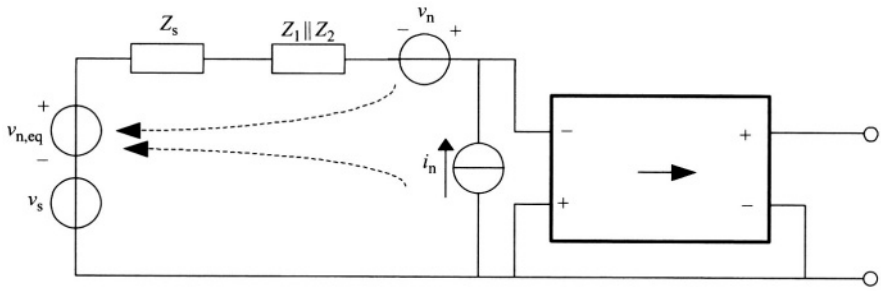


Figure 26.10. Equivalent circuit of the voltage amplifier in Figure 26.9 with respect to noise.

voltage/current source. For example, the result given by equation (26.3) could also be obtained from Figure 26.10, which is equivalent to Figure 26.9 with respect to noise.

Generally, these equivalent circuits provide a very efficient "short-cut" in the analysis of the amplifier noise behavior.

Distortion increment and bandwidth reduction. Impedance feedback networks affect the amplifier distortion and bandwidth due to the fact that they consume power. Their input impedance loads the output stage of the nullor, which increases the distortion (the nullor output stage has to deliver more power) and reduces the bandwidth (the loop-gain is reduced). As a consequence, a "residual" trade-off between noise, distortion and bandwidth remains present. For example, a low value of the feedback impedances Z_1 and Z_2 is beneficial in a voltage amplifier with respect to noise. At the same time, however, this may also cause a low value of the feedback network input impedance

$Z_1 + Z_2$, which deteriorates the distortion and bandwidth. Often, the increase of distortion and reduction of bandwidth can be repaired by increasing the bias current of the nullor output stage (increase power consumption). However, it is clear that the feedback impedances should not be chosen much smaller (larger) than is necessary to match the noise requirements.

26.3.2. Design of the Active Part for Low Noise

The nullor implementation has to comply simultaneously with the requirements with respect to noise, distortion and bandwidth. To achieve this, we "orthogonalize" the requirements by confining them to different stages inside the nullor in the following way.

Since small signals are more vulnerable to noise than large ones, it is likely that the amplifier input has a dominant influence on the noise performance; the power contents of the information signal is minimum here. Therefore, it makes sense to design the nullor input stage for minimum noise, and assure that the noise contribution of other stages is negligible. Similarly, the distortion is likely to be dominated by the output stage, since the signal levels are maximal there. By proper design, it can be assured that all distortion is confined to the nullor output stage. Similarly, the bandwidth requirements can be localized into intermediate stages [2]. In this section, we concentrate on the design of the input stage for low noise.

The input stage of the nullor in a low-noise amplifier has to comply with two requirements:

- It has to assure orthogonality between noise and the other requirements.
- Its own noise production should be minimal.

To assure orthogonality, the gain of the nullor input stage should be made as large as possible. This was noticed already by Friis in 1944 [4] in conjunction with repeaters for telegraph lines. It also directly follows from the twoport transformation discussed in Section 26.2 as illustrated by Figure 26.11.

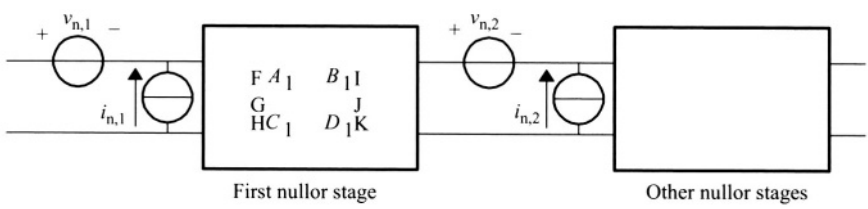


Figure 26.11. Assuring orthogonality with respect to noise by maximization of the gain of the input stage.

The twoport on the left of this figure represents the nullor input stage, while the one on the right represents the other stages. The equivalent input noise of these stages, represented by $v_{n,2}$ and $i_{n,2}$ transforms to the amplifier input through the chain parameters of the input stage, according to Figure 26.5. Their contribution to the equivalent amplifier input noise vanishes when all chain parameters of the input stage equal zero, that is, when the gain of the input stage is infinite. The transistor stage that best approximates this behavior is the common source (CS) stage for MOSFETS/JFETS, or the common emitter (CE) stage for bipolar transistors. These are the only stages that do not contain local feedback, like the emitter/source follower $(A \approx 1)$ or current follower $(D \approx 1)$.

In order to assure that the noise production of the input stage itself is minimum, it should clearly not contain local impedance feedback, such as in a shunt or series stage. The remaining options are a CE/CS stage, an emitter/source follower and a current follower. The noise production of these three stages are almost identical. Since the chain parameters of the CE/CS stage are significantly smaller than one or more chain parameters of the other ones, it is by far the preferred choice to implement the input stage. In some cases, a stage derived from the CE/CS-stage (like a differential pair) is also suitable; their chain parameters differ only slightly from that of the CE/CS stage.

26.3.3. Noise Optimizations

After selection of the feedback network and the nullor input stage, there are still some degrees of freedom left to optimize the amplifier noise performance. These optimizations will be discussed below. In general, one or more of the following three types of optimizations can be applied:

- Noise matching to the source.
- Optimization of the bias current of the first stage.
- Connecting several input stages in series/parallel.

All of them can essentially be viewed as variants of the first type, as shown below.

Noise matching to the source. The principle of noise matching to the signal source can be explained with the aid of Figure 26.12.

The sources v_n and i_n represent the equivalent amplifier input voltage and current noise, respectively. The purpose of the (ideal) transformer is to adjust the source impedance, as seen by the amplifier, in such a way that the available power of the equivalent noise source $v_{n,eq}$ becomes minimum. Since it leaves the equivalent power of the signal source v_s unchanged, this approach

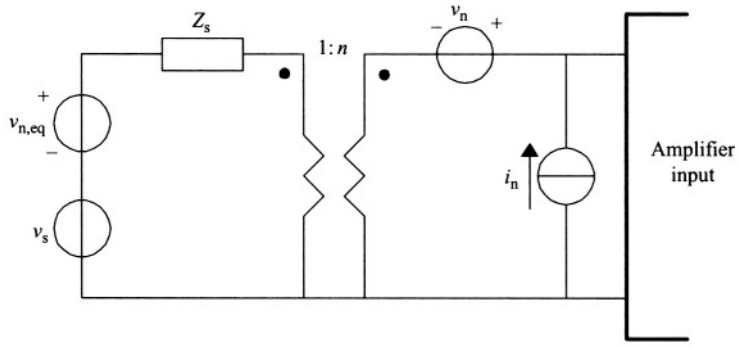


Figure 26.12. Principle of noise matching to the source.

maximizes the equivalent amplifier input SNR. The details are as follows. As known from circuit theory, the available power of v_s and $v_{n,eq}$ equals:

$$P_{av,v_s} = \frac{\bar{v}_s^2}{4\,\mathrm{Re}\{Z_s\}} \tag{26.4}$$

$$P_{av,v_{n,eq}} = \frac{\bar{v}_{n,eq}^2}{4\,\mathrm{Re}\{Z_s\}} \tag{26.5}$$

The equivalent amplifier input SNR equals the ratio of these two. The transformer has no effect on equation (26.4), but it does effect equation (26.5), through the relation between $v_{n,eq}$ and v_n, i_n:

$$v_{n,eq} = \frac{v_n}{n} + nZ_s i_n \tag{26.6}$$

Consequently, the amplifier input noise effectively "sees" a source impedance equal to $n^2 Z_s$. The transformation ratio n can now be chosen such that equation (26.5) is minimized, while equation (26.4) remains unchanged. For simplicity, assume that $Z_s = R_s$ is real, and v_n and i_n are uncorrelated (which is not always true). Then the optimal ratio n_{opt} satisfies:

$$n_{opt}^2 = \frac{1}{R_s}\sqrt{\frac{\bar{v}_n^2}{\bar{i}_n^2}} \tag{26.7}$$

A similar result is found if the signal source is a current source. For the optimal ratio, the contributions of v_n and i_n are equal. The advantage of this approach is that all noise sources in the amplifier are included in the optimization. The main disadvantage is that a transformer is not available in many cases or, as in microwave designs, realizes a match over a limited frequency range only.

Optimization of the bias current. This type of optimization [2,5] relies on the fact that the intensity of several transistor noise sources, the collector and base shot noise in a bipolar transistor and the channel noise in a MOS/JFET, depends on the transistor bias current. In addition, the chain parameters are also bias dependent.

The principle is illustrated by Figure 26.13, which depicts the nullor input stage with only the bias dependent noise sources.

The source $i_{n,1}$ represents the bias dependent output noise current source (collector shot noise/channel noise), present for both a bipolar and MOS/JFET input stage. As depicted, it transforms to the input through the chain parameters B and D. The bias dependent input noise source $i_{n,2}$ (base shot noise) is present only in case of a bipolar input stage. The power spectral density of both $i_{n,1}$ and $i_{n,2}$ is proportional to the transconductance g_m. Two different situations can be distinguished.

For a FET input stage, both B and D are proportional to $1/g_m$ and consequently, the power contents of all equivalent input noise sources due to $i_{n,1}$ is proportional to $1/g_m$. In this case, no global noise optimum exists; to minimize the noise g_m, that is, the bias current, should be chosen as large as possible.

For a bipolar input stage, a global noise optimum does exist. The chain parameter D is independent of g_m in this case, such that the power contents of the nullor input current noise is proportional to g_m. The power contents of the voltage noise are, similar to a FET input stage, proportional to $1/g_m$. The resulting possibility to optimize the noise with respect to g_m is very similar to optimization of the transformer ratio in the noise matching optimization, as illustrated by Figure 26.14.

The transistor at the right side is biased at a constant current $I_{c,o}$, resulting in a transconductance $g_{m,o}$. The total impedance seen from the transistor input,

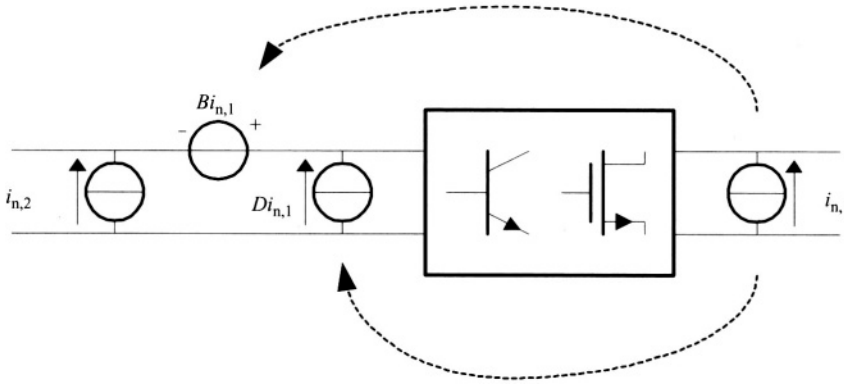


Figure 26.13. First nullor stage including bias dependent noise sources.

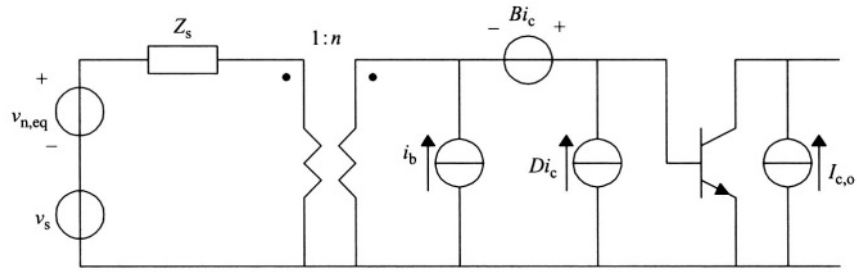


Figure 26.14. Similarity between noise matching and optimization of the bias current; the bias current changes the ratio of the (fictitious) transformer.

including the base resistance, is represented by Z_s. The fictitious transformer represents the effect of changing the bias current; the squared transformation ratio n^2 equals the factor by which this current and g_m are changed. It can be optimized in the same way as in the noise matching case. For example, when $Z_s = R_s$ is real, and $\beta_F \gg 1$ (such that Di_c is negligible compared to i_b), then it follows from equation (21.7) that:

$$n_{opt}^2 = \frac{g_m}{g_{m,o}} = \frac{1}{R_s}\sqrt{\frac{B^2\bar{i}_c^2}{\bar{i}_b^2}} = \frac{\sqrt{\beta_F}}{g_{m,o}R_s} \tag{26.8}$$

This is the familiar result for the g_m of an optimally biased bipolar input stage [3].

The strength of bias current optimization is that it is virtually always applicable; no additional circuitry is required. Its main disadvantage is the limited scope; it can only optimize the contribution of bias dependent sources such as i_c and i_b. The contribution of other sources cannot be affected by it.

Connecting stages in series/parallel. A third optimization method is connecting several input stages in series or in parallel/scaling of the input stage. Also, this approach can be explained with the aid of a fictitious transformer, as depicted in Figure 26.15.

If two identical stages are placed in parallel, their identical but uncorrelated input current sources add, resulting in a total noise current of $\sqrt{2}$ times the input current of a single stage. It can be shown that at the same time, the equivalent input noise voltage source of the two stages is *reduced* by a factor $\sqrt{2}$. In case of two series connected input stages, exactly the opposite situation occurs; the voltage noise increases by factor $\sqrt{2}$, while the current noise decreases by a factor $\sqrt{2}$. When n stages are placed in series or in parallel, the same magnification/reduction is observed, but now with a factor $\sqrt{n}$. Altogether, the effect of series/parallel connection is the same as that of a transformer with turn

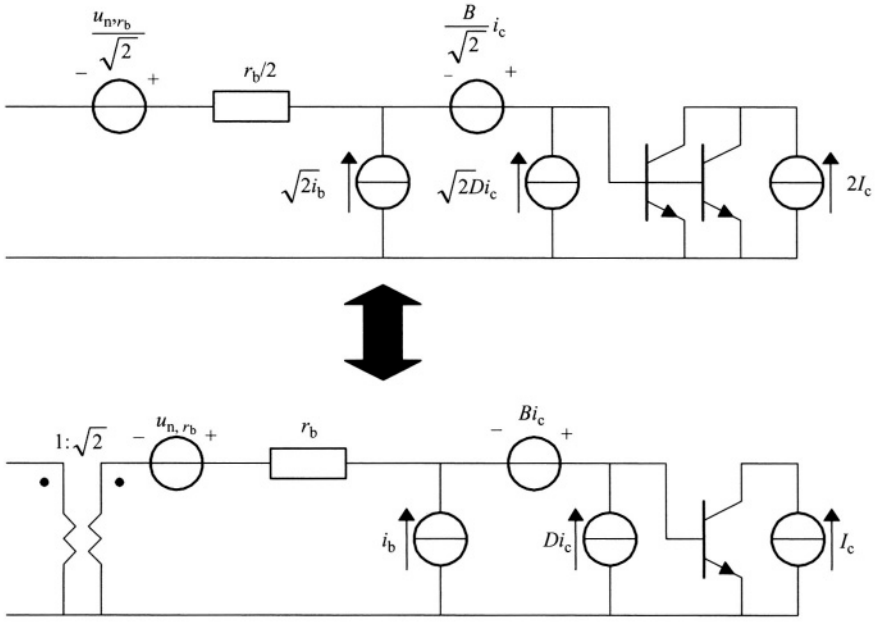


Figure 26.15. Effect of scaling or series/parallel connection of the nullor input stage. Depicted is a parallel connection of two identical CE-stages and its equivalent representation using a (fictitious) transformer.

ratio $\sqrt{n}$. Figure 26.15 shows the situation for parallel connection. For series connection, both ports of the transformer are interchanged.

The optimal scaling factor of the input stage can again be found from equation (26.7). In full-custom ICs, n can be chosen arbitrarily (within certain boundaries), but in semi-custom ICs and discrete circuits, only integer values can be realized.[1]

Summary of optimizations. Figure 26.16 shows all possible optimizations together in one amplifier. Bias current optimization has the most limited scope, since it only affects the noise sources that are dependent on the bias current (such as i_c and i_b), shown at the right of transformer 3. Placing stages in series/parallel (scaling) has a slightly wider scope; it also covers the bias independent noise sources of the input transistor, such as the noise of the base/gate resistance. It does not cover the noise produced by the feedback network. Furthermore, the turning ratio of the corresponding transformer, n_2, has to be

[1] Eventually, rational values for n can be obtained using combinations of series and parallel connection.

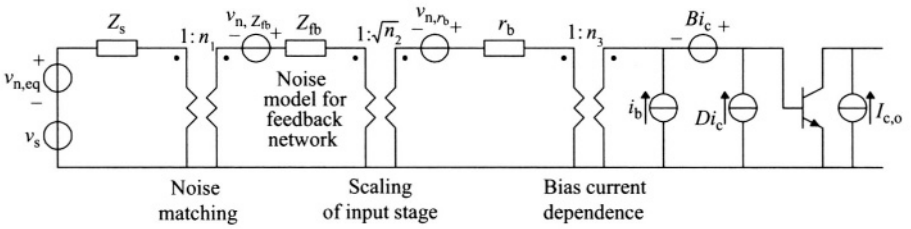


Figure 26.16. Summary of all possible amplifier noise optimizations.

integer (or rational) for discrete realizations. Noise matching to the source has the widest scope; it covers all noise produced by the amplifier, including the noise of the feedback network.

26.4. Low Noise Harmonic Resonator Oscillator Design

Another type of circuit is that which is encountered in a wide variety of electronic systems, where a frequency or timing reference is required, such as down-conversion in communication receivers, or as a clock in synchronous digital circuitry. In this section, we focus on low-noise design of an important subclass of oscillators; resonator oscillators. The characteristic property of these oscillators is that their frequency/time stability is determined by a passive, reactive component, such as an LC-tank or a crystal. As a consequence, they are intrinsically capable of attaining very low phase noise levels, and cannot be tuned over a wide range.

26.4.1. General Structure of a Resonator Oscillator

A resonator oscillator basically consists of two parts: a resonator and an undamping circuit, as depicted in Figure 26.17 [6–8].

The resonator serves as a frequency/timing reference, determining the oscillation frequency ω_o. Resonators with a high frequency stability are passive components that dissipate an extremely small, but noticeable amount of power. As a consequence, they are unable to sustain the oscillation autonomously. For this purpose, the undamping circuit is included; it supplies the energy dissipated by the resonator, such that the oscillation is maintained.

The dissipation inside the resonator, and the supply of energy by the undamping circuit are both fundamentally contaminated with noise. This noise, denoted by n_i in Figure 26.17, enters the oscillator loop and causes phase noise, that reduces the frequency stability. According to [9], the single-sideband phase noise power spectral density at a distance $\Delta\omega$ from the oscillation frequency

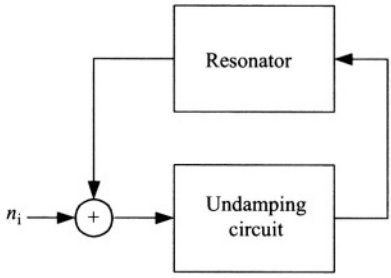


Figure 26.17. General structure of a resonator oscillator.

ω_o can be expressed as:

$$L(\Delta\omega) = \left(\frac{\omega_o}{\Delta\omega_o}\right)^2 \frac{S_{ni}(\omega_o + \Delta\omega_o)}{4Q^2A^2} \tag{26.9}$$

where A denotes the amplitude of the oscillation signal, S_{ni} the noise power density spectrum at the input of the undamping circuit and Q the quality factor of the resonator, defined as:

$$Q = \frac{\omega_o}{2}\left|\frac{d\phi(\omega)}{d\omega}\right|_{\omega=\omega_o} \tag{26.10}$$

where $\varphi(\omega)$ represents the resonator phase-frequency characteristic. Consequently, the minimum attainable phase noise level decreases proportionally to Q^2.

26.4.2. Noise Contribution of the Resonator

One of the contributions to the noise process n_i in Figure 26.17 is due to the dissipation of power in the resonator. In practice, various types of resonators are encountered in oscillators, varying from LC-tanks, to quartz crystals and even resonating sensor elements. From an electronic point of view, however, there are only two main classes: series resonators and parallel resonators, as depicted in Figure 26.18. Close to the resonance frequency, all resonators can be modeled as either a series or a parallel resonator [9,10]. In both models, the resistors represent the power loss in the resonators. As follows from thermodynamics, the noise produced by the resonators will, therefore, (at least) equal the thermal noise of these resistors.

The series resonator has a resonant voltage-to-current transfer (admittance with two complex poles). Therefore, for an oscillator constructed around such a resonator, the signal sensed at the input of the undamping circuit in Figure 26.17 is a current. The contribution of the resonator to the input noise n_i, therefore,

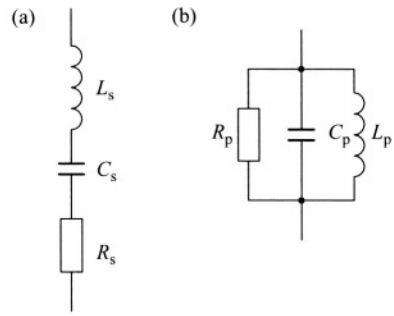


Figure 26.18. The two main resonator classes. (a) Series resonator and (b) parallel resonator.

equals the (thermal) noise current produced by R_s. Using equation (26.9) and [1., the corresponding minimum possible phase noise level is found to equal:

$$L_{s,\min}(\Delta\omega) = \frac{kTR_s}{A^2 L_s^2 (\Delta\omega)^2} \tag{26.11}$$

Thus, R_s should be as low as possible, or, equivalently, the quality factor $Q_s = \omega_o L_s / R_s$ should be as high as possible.

The parallel resonator has a resonant current-to-voltage transfer (impedance with two complex poles). Therefore, in an oscillator constructed around such a resonator, the signal sensed at the input of the undamping circuit in Figure 26.17 is a voltage. The contribution of the resonator to the noise n_i in this case equals the (thermal) voltage noise of R_p. The minimum phase noise level for this resonator equals:

$$L_{p,\min}(\Delta\omega) = \frac{kT}{A^2 R_p C_p^2 (\Delta\omega)^2} \tag{26.12}$$

Thus, in this case R_p should be as large as possible, which is also equivalent to an as large as possible quality factor $Q_p = \omega_o R_p C_p$.

Concluding, a low phase noise level can only be attained by using a resonator with a high quality factor.

26.4.3. Design of the Undamping Circuit for Low Noise

The purpose of the undamping circuit is to maintain the oscillation in the oscillator loop, by compensating for the power loss in the resonator. Since this power loss is modeled by the positive resistors R_s and R_p, the undamping circuit, exactly compensating the losses, can be represented by a negative resistance—R_s (series resonator) or —R_p (parallel resonator), as depicted for a series resonator in Figure 26.19.

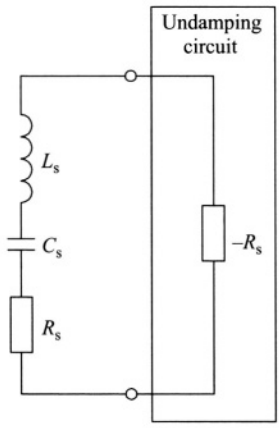


Figure 26.19. Undamping of a series resonator by a negative resistance.

In the remainder of the chapter, we concentrate on the series resonator; the results for the parallel resonator are easily derived from this by interchanging current and voltage.

Principle implementation of the undamping circuit. In principle, to sustain the oscillation, the undamping circuit in Figure 26.19 has to perform two operations:

- It has to sense the current through the resonator.
- It has to drive the voltage across the resonator.

Both functions can be performed by a transimpedance amplifier, as depicted in Figure 26.20.

To sustain the oscillation, the amplifier transfer should *exactly* equal the resonator series resistance R_s, which is impossible in practice. When the transfer is smaller than R_s, the oscillation will damp out, while it will grow unboundedly when the transfer is larger. Therefore, in order to stabilize the oscillation, an amplitude control loop is required that adjusts the amplifier gain to maintain a constant oscillation amplitude.

Amplitude control. The amplitude control can generally be realized in two different ways. The first possibility is to use a slow gain control loop that continuously adjusts the gain of the transimpedance amplifier. The second possibility is to replace the linear transimpedance amplifier by a limiting transimpedance amplifier. In that case, it has to be assured that the limiter gain exceeds the loss resistance R_s in order to maintain oscillation. Generally, the

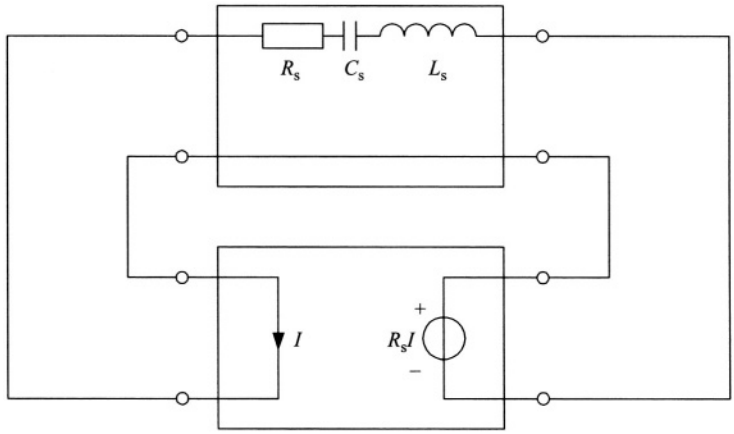


Figure 26.20. Implementation of a negative resistance by a transimpedance amplifier.

limiting amplifier solution is much simpler to implement and, as will be discussed below, only yields a slightly lower Carrier-to-Noise ratio (CNR) level than an ideal linear undamper.

Noise performance. Generally, two types of noise can be distinguished in an oscillator using a limiting amplifier as undamper:

- Noise with an intensity that is independent of time, such as the resonator noise and part of the amplifier noise.
- Noise with an intensity that switches "on" and "off".

An example of the latter type of noise is collector shot noise in a differential pair; when the differential pair saturates, the shot noise is not noticeable at the output ("off"), while it is noticeable in the linear region ("on"). The limiter gain can be used to realize a suitable trade-off between both types of noise. Aliasing due to the nonlinear transfer of the limiter increases the contribution of the first type of noise. This aliasing, and the noise, increases for increasing limiter gain values. In [10] is shown that a limiter "overdrive" of 2, that is, a gain of $2R_s$, is a suitable value that assures oscillation and degrades the CNR by only 3 dB due to aliasing. The contribution of the switching noise (second type) decreases for increasing limiter gain values; for increasing gain, the fraction of time that the limiter operates in its linear region decreases. The true optimum limiter gain value, therefore, depends on the relative magnitude of the switching noise and the continuous noise.

Driving the oscillator load. In principle, the undamping circuit can be combined with an output buffer/amplifier that drives the oscillator load. Such

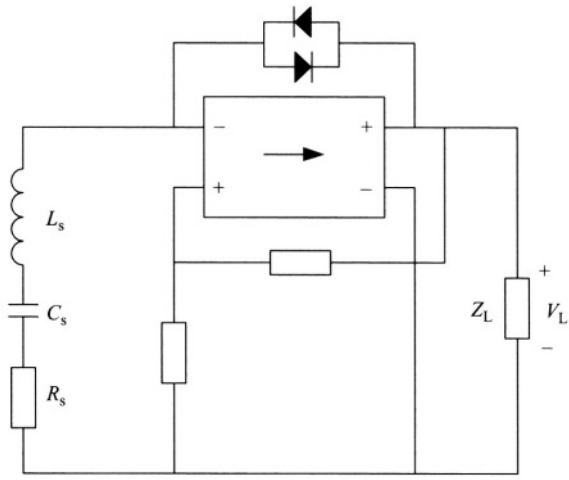


Figure 26.21. Oscillator with undamping realized by a double-loop limiting amplifier.

an amplifier is generally required to prevent so-called "loading" of the amplifier by the load, which reduces the resonator quality factor.

An elegant solution that comprises both the undamping and output buffering is provided by double-loop amplifier configurations. One negative and one positive feedback loop together realize an accurately defined, negative amplifier input impedance, and drive the load by an accurately defined voltage/current. An example of such a configuration, that establishes amplitude stabilization through limiting, is shown in Figure 26.21.

Further details on the design of double-loop undamping amplifier can be found in [10,11].

26.4.4. Noise Matching of the Resonator and Undamping Circuit: Tapping

In the same way as discussed for amplifiers, the noise behavior of the undamping circuit in resonator oscillators can be optimized using the techniques shown in Subsection 26.3.3. An especially useful optimization in oscillator design is noise matching to the source, which is the resonator in the oscillator case, as discussed below.

A simplified representation of the noise matching is depicted for a series resonator in Figure 26.22.

The voltage across the resonator is driven by the output of the amplifier (see Figure 26.20), which can be viewed as a short circuit. Close to the resonance frequency, the resonator behaves as a current source with source impedance R_S. The transformer can be used to minimize the equivalent amplifier input

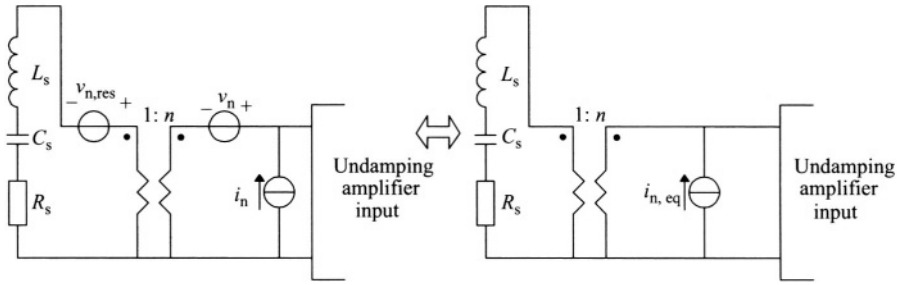


Figure 26.22. Noise matching to the resonator.

noise current $i_{n,eq}$ by matching R_s to the noise resistance R_n, the ratio of the rms value of v_n and i_n, of the amplifier. Seen from the amplifier input, the transformer enlarges the resonator series resistance to $n^2 R_s$. The equivalent amplifier input noise power can, therefore, be written as:

$$P_{n,eq} = n^2 R_s \bar{i}^2_{n,eq} = \frac{\bar{v}^2_{n,res}}{R_s} + \frac{\bar{v}^2_n}{n^2 R_s} + n^2 R_s \bar{i}^2_n \qquad (26.13)$$

The equivalent input signal power is independent of the transformer ratio n, such that the same optimum ratio as given by equation (26.7) is found again:

$$n^2_{opt} = \frac{1}{R_s}\sqrt{\frac{\bar{v}^2_n}{\bar{i}^2_n}} \qquad (26.14)$$

Obviously, for very high Q resonators, this optimum ratio can become impractically large. For medium and low Q resonators, the matching technique can provide a significant CNR improvement.

This matching technique wouldn't be interesting if there was no suitable means to approximate the ideal transformer. Fortunately, however, a suitable approximation technique does exist: capacitive (or inductive) tapping [9–12]. The principle is illustrated in Figure 26.23.

Besides the required transformer, the capacitive tap also adds an unwanted parallel capacitance. As long as the tapping capacitance C_2 is much smaller than C_1, that is, if the transformer ratio n is large, this parallel capacitance will have a negligible effect. Eventually, for relatively low transformation ratios, it will [11]:

1 add a parallel-resonance frequency above the series resonance frequency;

2 decrease the series resonance frequency;

3 degrade the Q factor.

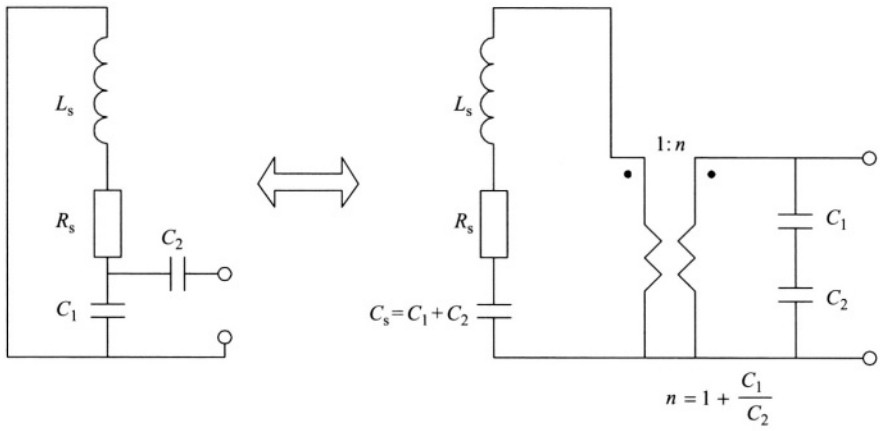


Figure 26.23. Approximation of a transformer by capacitive tapping.

When these effects occur, it is possible to cancel the parallel capacitance by means of an active negative capacitance [9,11], that in many cases can be incorporated in the design of the negative resistance/undamping amplifier. Details on the design on such negative capacitance can be found in [11].

26.4.5. Power Matching

Further optimization of the oscillator CNR, besides matching the undamping amplifier input to the source, is possible by power matching of the undamping amplifier output to its load [13]; the resonator. This power matching assures that the maximum possible power is delivered to the resonator (for a certain power consumption).

In principle, when the output impedance of the amplifier in Figure 26.20 is close to zero, it would be possible to deliver a very large amount of power to the resonator. However, for very high Q resonators, the current to be delivered by the amplifier to achieve this becomes extremely large. To reduce the required current, a transformer can be inserted, as depicted in Figure 26.24.

With this setup, the current through the resonator is n times as large as the current through the amplifier. Again, this transformer can be realized through capacitive tapping of the resonator. Consequently, if both noise matching and power matching is applied, we attain a configuration with a doubly tapped resonator, as depicted in Figure 26.25.

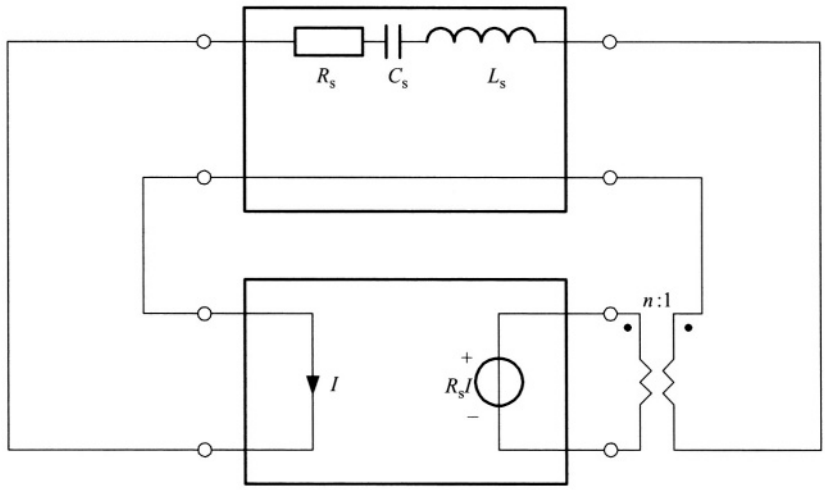


Figure 26.24. Power matching to reduce the amplifier output current.

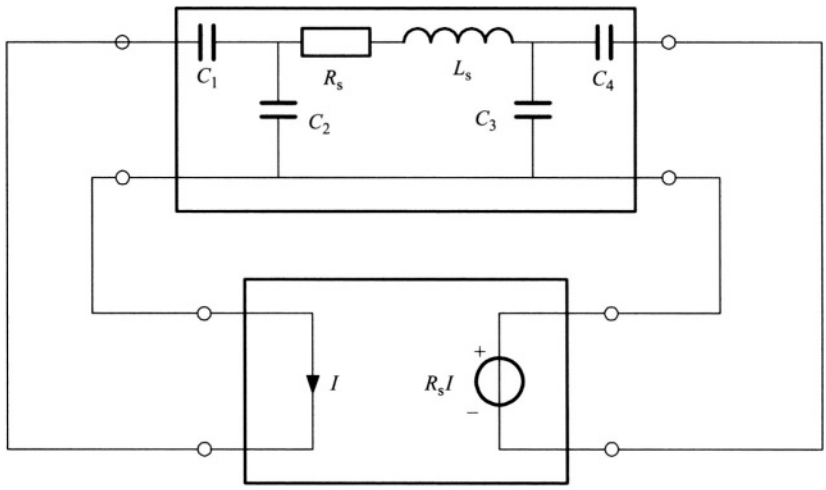


Figure 26.25. Doubly tapped resonator achieving both noise and power matching.

26.4.6. Coupled Resonator Oscillators

Besides selection of a high-Q resonator and the design of a low-noise undamping circuit, there is in principle a third possibility to minimize the phase noise; coupling several oscillators together. In literature, coupled resonator oscillators are proposed as means to achieve various objectives: a reduced phase noise level [14,15], an extended tuning range [16], and generation of

quadrature outputs [17,18]. Neither of these proposals, however, appears to be a very good solution [9]; resonator oscillators should not be coupled. In this section, we explain why coupling of resonator oscillators deteriorates the phase noise.

As expressed by equations (26.9) and (26.10), the phase noise level of a resonator oscillator is determined by the steepness (slope) of the resonator phase characteristic at the resonance frequency, that is, the frequency where the phase characteristic crosses through zero degrees. The steeper this characteristic is, the lower is the resulting phase noise level. Coupling deteriorates the phase noise level because it generally decreases the steepness of the phase characteristic, as discussed below. The ineffectiveness of coupling of resonator oscillators can be explained with the aid of the cascaded (in-phase coupled) structure of Figure 26.26.

Each resonator is accompanied by a separate undamping circuit to assure isolation of the resonators and prevent mutual loading effects (which deteriorate the resonator Q-factor). When all amplifiers and resonators are assumed to be identical, the total noise power in the loop equals N times the noise produced by a single resonator-amplifier combination (10 log(N) dB). At the same time, the steepness of the phase characteristic of the loop is N times larger than that of a single resonator. The combined effect of the noise and the slope of the phase characteristic is an improvement of the CNR by 10log(N) dB.

The conclusion that can be drawn from Figure 26.26 is that putting N identical resonators in cascade improves the phase noise by 101og(N) dB, at the cost of an N times higher power consumption. However, as shown by equation (26.9), the same improvement can be obtained by putting N times more power into a single resonator (if possible), that is, increasing the oscillation amplitude by a factor N^2. This already shows that coupling of resonator oscillators is a rather roundabout way to realize a CNR improvement of 10 1og(N) dB.

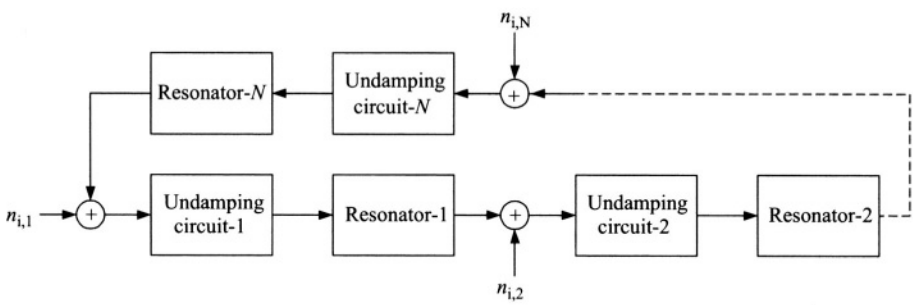


Figure 26.26. N cascade-coupled resonator oscillators.

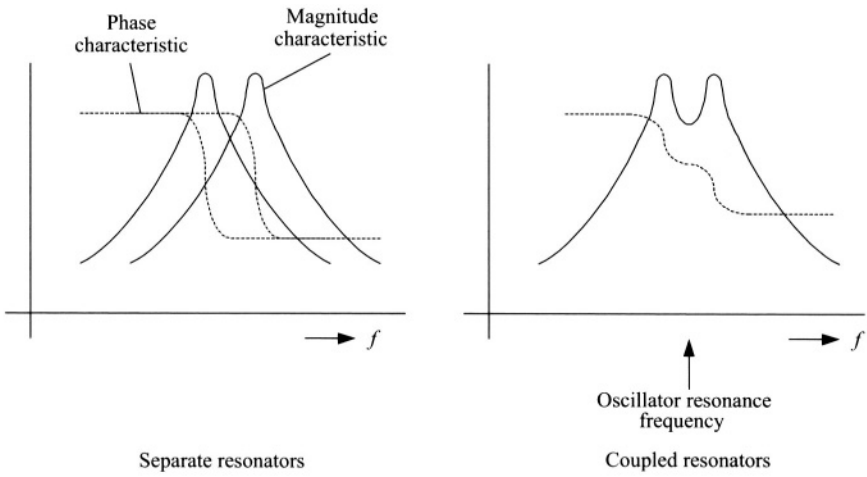


Figure 26.27. Magnitude and phase characteristics of separate resonators (left) and coupled resonators (right) with a slightly different resonance frequency.

In practice, the situation is actually far worse, because it is impossible to attain N exactly equal resonators with identical resonance frequencies. The oscillator resonance frequency will then be somewhere between the resonance frequencies of the individual resonators, where as illustrated by Figure 26.27, the slope of the loop's phase characteristic can even be much lower than that of a single resonator. Concluding, we observe that coupling of resonator oscillators is not only a roundabout way to put more power into the resonator, it is generally not a good solution.

26.5. Low-Noise Relaxation Oscillator Design

This section discusses the noise behavior of a second important class of oscillators; relaxation oscillators. These oscillators are also called "first-order" oscillators, because of the fact that, as opposed to, for example, a resonator oscillator, only one dynamic element, an integrator (usually a capacitor), determines the timing (frequency of oscillation). The differential equation describing their dynamic behavior, however, is of the second order.

Of course, a relaxation oscillator comprises more than just a single integrator. Figure 26.28 depicts a generalized block diagram, including the extra functions needed to implement a complete first-order oscillator. The capacitor integrates a constant current coming from the (binary) memory. When the detection level of one of the comparators is crossed, the memory is switched, its output changes sign and the integrator starts integrating towards the detection level of the other

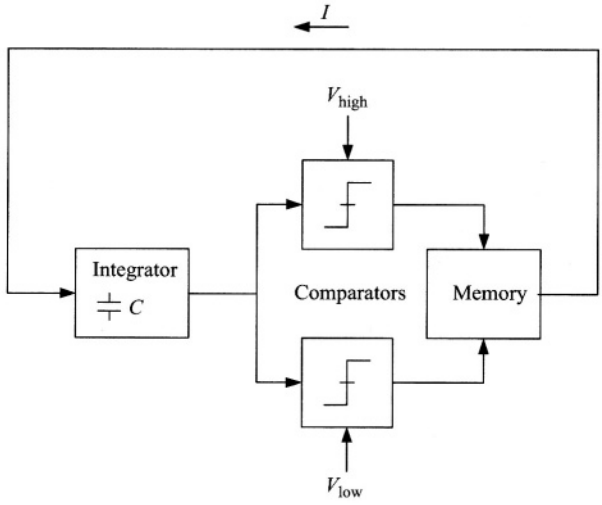


Figure 26.28. Generalized block diagram of a relaxation/first-order oscillator.

comparator. The frequency of oscillation is:

$$\omega_o = \frac{\pi}{(V_{high} - V_{low})C} \tag{26.15}$$

The operation of this class of oscillators is very basic and assumed to be known to the reader. More information on the basics can be found in [9,19].

The topology shown in Figure 26.28 is very commonly used. In this text we will take a close look at this topology to investigate its noise behavior and to consider the influence of the various components on the total noise behavior. We will see that alternative topologies, with a better noise performance do exist but are unfortunately rarely used.

26.5.1. Phase Noise in Relaxation Oscillators

When a relaxation oscillator is properly designed, which means that the right topology has been chosen and that the noise behavior has been optimized, its phase noise can be predicted via a rather simple equation. This is derived from the uncertainty involved with the point in time at which the integrator signal crosses the comparator detection levels. In this section, we discuss the modeling and causes of phase noise in relaxation oscillators. First, a simplified noise model is discussed. Subsequently, the influence of the memory and comparators on the phase noise is considered.

Simple phase noise model. In its simplest form, the noise in relaxation oscillators can be modeled by two noise sources. A noise current source (i_n) in

parallel to the output of the memory and a noise voltage source (v_n) in series with the capacitor. Depending on the frequency range occupied by the power spectral density of the noise sources, relative to the frequency of oscillation, different methods apply to calculate the resulting phase noise [9,19,20].

Noise that is (mainly) located at frequencies much smaller than the oscillation frequency ω_o causes frequency modulation of the oscillator, in the same way as a baseband message signal would do. Noise that is located at high frequencies, that is, around f_o and beyond, also noticeably influences the switching action of the comparators, which causes considerable noise aliasing. The aliased noise is located at low frequencies, and again causes frequency modulation of the oscillator.

If, for the moment, we assume that the aliasing noise is negligible, and that the power density spectra of i_n and v_n are white, the contribution of these sources to the oscillator phase noise power density spectrum equals:

$$L(\Delta\omega) = \frac{S_{i_n}}{2I^2}\left(\frac{\omega_o}{\Delta\omega}\right)^2 \tag{26.16}$$

$$L(\Delta\omega) = \frac{S_{v_n}}{(V_{high} - V_{low})^2}\left(\frac{\omega_o}{\Delta\omega}\right)^2 \tag{26.17}$$

The lower bound on the power density of v_n depends on the used technology. For a bipolar realization, this noise source is usually dominated by the thermal noise of the base resistance of the transistors.

Unfortunately, the noise aliasing effect is generally not negligible; the switching action is inherent to relaxation oscillators. High-frequency noise is folded back to low frequencies, causing low-frequency modulation of the oscillation signal. Aliased high-frequency noise components usually come from v_n, since the capacitor suppresses the high-frequency components of i_n. The effect of aliasing caused by v_n can be represented by a multiplication of its contribution to the phase noise, equation (26.17), by a factor:

$$\alpha = \frac{\pi B_{conv}}{\omega_o} \tag{26.18}$$

in which B_{conv} (in Hz) is the effective noise conversion bandwidth. In high-frequency oscillators, a dominant pole in the comparator usually determines B_{conv}.

Influence of the memory on the oscillator phase noise. The memory in a relaxation oscillator is a regenerative binary memory. It remembers the latest detection level that was crossed. This is the only task in a relaxation oscillator that cannot be done by another circuit. Another task that could be performed by the memory circuit, but also by other circuits is the comparator function. Any regenerative circuit is capable of detecting the crossing of

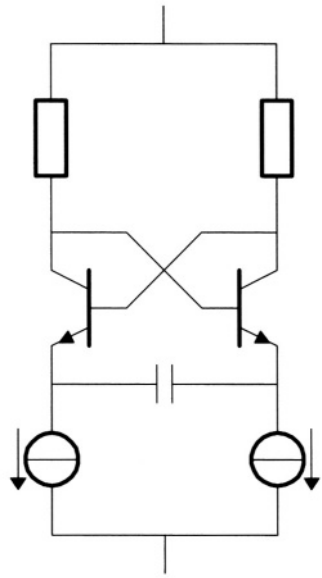


Figure 26.29. Emitter-coupled multi-vibrator; relaxation oscillator in which the memory also performs the level detection (comparator function).

a detection level by an input signal. This implies that, in principle, the comparators can be deleted from the topology depicted in Figure 26.28. The result is a very simple topology, implemented, for example, by the emitter-coupled multi-vibrator of Figure 26.29.

In order to evaluate the effect on the phase noise of omitting the comparators, the quality of the comparator function performed by the memory has to be analyzed. Figure 26.30 shows a plot of the state X of a regenerative circuit (memory) as a function of the memory input signal u_{in}. The z-shaped line connects the operating points at which the regenerative circuit is stable; it does not change state when it is on the line. When the operating point is not on the line, the memory changes state in the direction given by the block arrows in the graph. The graph shows two states: $-X_{\text{th}}$ and X_{th}. Between these states the memory has a regenerative behavior.

Outside the interval $X \in [-X_{\text{th}}, X_{\text{th}}]$ the memory is in a non-regenerative mode; the state variable X tracks the input signal u_{i} along the z-curve. The states $\pm X_{\text{th}}$ are the boundaries between the regenerative and the non-regenerative parts of the z-curve. Suppose that u_{i} increases from $-\infty$ towards positive values. The state variable X then follows the lower part of the z-curve, until it reaches $-X_{\text{th}}$ (a threshold state). If u_{i} increases any further, the memory enters its regenerative mode and X will move along transition T_1 to a point in

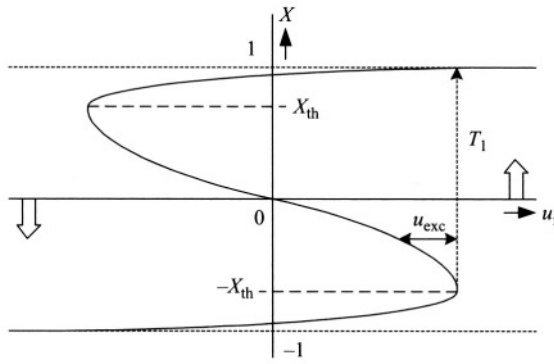


Figure 26.30. State of the regenerative (binary) memory as a function of the memory input signal u_{in}.

the other non-regenerative part of the z-curve, irrespective of the value of u_i. The stimulus that moves X to the other non-regenerative state can be quantified by the excitation (u_{exc}), the horizontal distance between the z-curve and the operating point of the memory circuit. From this it can be easily seen that when the transition starts, the excitation of the circuit is still very small, so the transition starts very slow and speeds up later. No matter what the amplitude of the input signal is, the excitation u_{exc} is only given by the distance of the operating point to the z-curve.

As a consequence, also effect of noise on the memory is determined by the (initially very low) SNR of the excitation u_{exc}, and *not* by the SNR of u_i. Therefore, a regenerative circuit can detect the crossing of a detection level, but only with extreme noise sensitivity and an initially slow reaction. The only way to improve this is to move the operating point quickly horizontally away from the z-curve (to the right), in order to stimulate the regenerative memory with an input signal that moves faster than the circuit can switch. This speeds up the start of the transition and makes it by far less noise sensitive. The topology shown in Figure 26.28, including the comparators, therefore, has a much better noise performance than the simpler topology of Figure 26.29. Further, it is not necessarily slower than the simple topology since the extra delay of the comparators can be very well compensated by acceleration of the state transition of the memory they introduce [21].

Influence of comparators on the oscillator phase noise. Above, it has been shown that the introduction of comparators in the relaxation oscillator is beneficial to the noise performance. However, there is also some risk involved in their use. How much gain should the comparators have, how fast should they be to improve the noise performance? Looking at Figure 26.28 again, it can

be seen that the comparators are embedded in a large *negative* feedback loop, that tries to keep the capacitor voltage below the detection levels. As soon as the capacitor voltage reaches detection level, the comparator starts generating a signal that "counteracts" this crossing. The comparator actually cancels its own stimulus, and the stimulus for the regenerative memory to switch state. The signal u_{in} in Figure 26.30 moves to the left again before the transition is completed. The only hope for the oscillator to function is that meanwhile, the excitation u_{exc} of the regenerative memory has gained sufficient strength to continue the state transition. Thus, although the trajectory Tl in Figure 26.30 may bend towards the z-curve, it should stay to the right of the curve. If it reaches the z-curve and crosses it due to a preliminary reduction of u_{in}, the regenerative memory returns to its original state and the oscillator stops.

Resistances in series with the integration capacitor increase the bandwidth of the negative feedback loop and, beyond certain resistance values, will also stop the oscillator. However, long before this happens, they make the oscillator even noisier than one would expect on the base of the noise contribution of the resistances themselves. Another way in which the bandwidth of the negative feedback loop is increased is by an increase of the gain of the comparators. Usually the introduction of comparators in a relaxation oscillator for level detection makes them less noisy [21]. It can, however, be easily seen that when the gain of the comparators would be infinite, the oscillator would "hang" at one of the detection levels. In practice, the combination of series resistances to the capacitor and the gain of the comparators increases the bandwidth of the negative feedback loop and thereby reduces the excitation of the regenerative memory somewhat. But as long as the increase of the excitation due to the comparators is larger than this reduction by the negative feedback loop, the introduction of the comparators is beneficial for the noise behavior. When the gain is increased further, the oscillator becomes more and more noisy and finally stops oscillating.

To prevent this effect from happening, the gain of the comparators should be kept low enough. The negative feedback loop, however, remains present, even in the absence of comparators, and always reduces the performance of the relaxation oscillator to some extent; it reduces the excitation of the regenerative memory. This loop, therefore, requires special attention in the design of relaxation oscillators.

26.5.2. Improvement of the Noise Behavior by Alternative Topologies

The main challenge for further improvement of the relaxation oscillator performance is to reduce the influence of the negative feedback loop or even remove it completely. In this section, two topologies will be shown that can be

used to achieve this. In the first topology, the regenerative memory is identified as the main "victim" of the feedback loop, and therefore the contribution of the memory to the overall timing of the oscillator is removed via a "memory bypass". In the second topology, which is a system of coupled relaxation oscillators, the loop is broken and its negative influence on the timing is thereby removed. Both topologies have shown to be very good candidates for low-noise relaxation oscillator designs [9,19,22].

Relaxation oscillators with memory bypass. When we look in detail at the various functions in relaxation oscillators, and evaluate the precise purpose of each of the components, it is observed that the only task for which the regenerative memory cannot be avoided is to remember which detection level was crossed last. In principle, it does not set the output frequency of the oscillator. The capacitor, the current that is integrated by the capacitor and the comparators that define the detection levels set the output frequency. This means that noise produced by the regenerative memory should not have influence on the oscillator output frequency.

Therefore, we can conclude that the topology shown in Figure 26.28, in which the memory actually is involved in the determination of the output frequency, is apparently not optimal. The regenerative memory cascades the comparators, such that its timing adds to the timing of the comparators. Its noise contribution is, therefore, also found in the output frequency. This effect is avoided in the topology depicted in Figure 26.31.

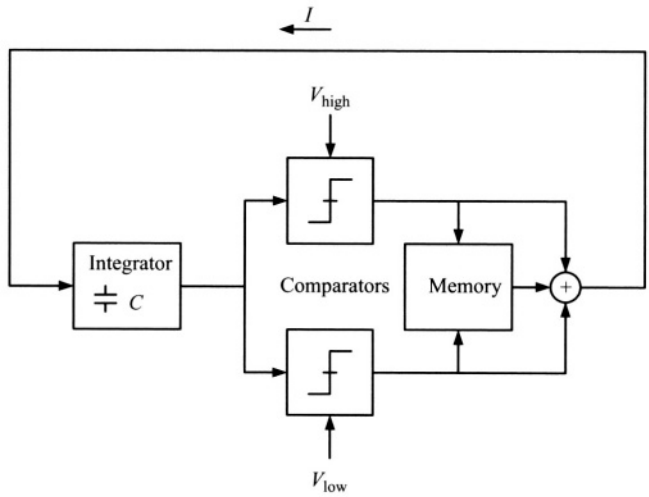


Figure 26.31. Relaxation oscillator with memory bypass [20].

There, regenerative memory does not cascade the comparators, but is put in parallel with them. The result of this is that around the state transitions, the comparators directly switch the integrator input current. At the same time the comparators stimulate the regenerative memory. The integration constant is thus already switching with a timing accuracy that is independent of the regenerative memory, the memory itself has the time to switch (in a noisy way) without injecting noise into the oscillator timing loop. The only restriction on the timing of the memory is that it should have reached its final state before the comparator stimulus disappears, due to the integrator signal that drops below the detection level again.

Figure 26.32 shows the various signals that appear in this topology. During the time that the integrator signal is above the detection level, the comparator output signal is high. The output signal of the memory, which is triggered by the comparators, follows later in time. Also shown by the combined signal is how the memory takes over from the comparator and keeps the signal level high after the comparator signal disappears again. The timing of the memory has little influence on the combined signal and thus the timing jitter of the memory is hardly contributing to the combined signal and with that to the output frequency of the oscillator.

Figure 26.33 shows a transistor circuit in which this topology has been implemented. Details on this circuit can be found in [9,20]. The center of the circuit diagram shows a flip-flop that fulfills the memory function. The differential pair above it is used as a current switch. The differential pairs at both sides of the flip-flop implement the comparator function. The differential pair

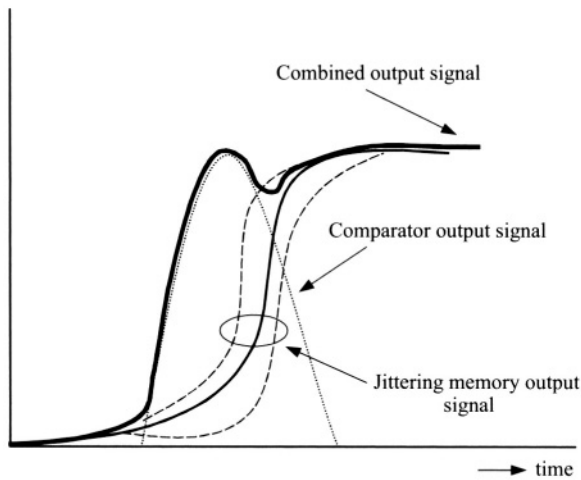


Figure 26.32. Signals in the "bypass" oscillator during a state transistion.

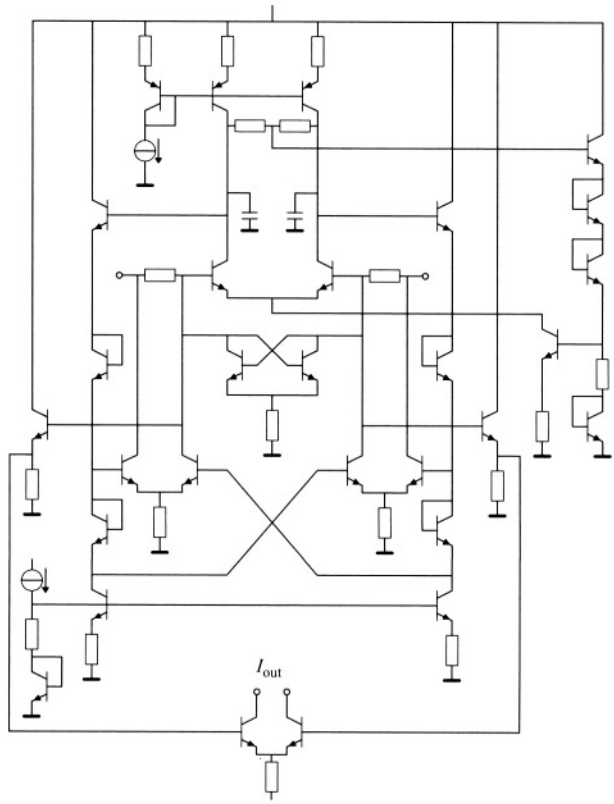


Figure 26.33. Relaxation oscillator with memory bypass [20].

at the bottom acts as an output buffer. All other transistors are used for biasing and level shift purposes. Two grounded capacitors have been used instead of one floating because the circuit has been integrated in a rather old IC-process in which capacitors have a large parasitic capacitor to the substrate at one plate. These plates are, therefore, chosen to coincide with the oscillator ground node, to make the parasites ineffective. The consequence of this is that the rest of the oscillator has to be floating, which explains the rather complicated biasing structure around the oscillator core. Clearly visible is that the comparators directly control the current switch. The flip-flop that is connected to the same node follows the signals and switches in parallel with the current switch without infecting the timing of the oscillator with its noise. When the comparator signal disappears again, the flip-flop keeps the current switch in the same state.

Coupled relaxation oscillators. *Quadrature coupling.* It has been previously discussed that the negative feedback loop in the oscillator reduces the

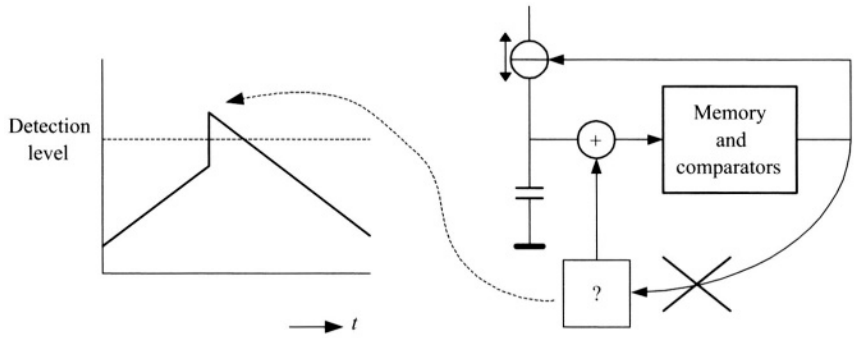


Figure 26.34. Configuration required to break the negative feedback loop around the detection level.

excitation of the regenerative memory. An improvement of the noise behavior of a relaxation oscillator can be expected when this loop is broken. The question, however is how to achieve this. Figure 26.34 illustrates the problem. To break the feedback loop when the capacitor (integrator) voltage in a relaxation oscillator approaches the detection level, the comparators should somehow quickly cross the detection level, as shown in Figure 26.34. In this way, there would be no chance for the feedback loop to counteract the comparator and memory input signals during the level crossing.

Unfortunately, such a situation cannot be realized through the comparators in the relaxation oscillator itself. Since they are also part of the negative feedback loop, increasing their gain to high values is detrimental to the noise behavior, as discussed before. Actually, it is difficult to derive the required "transition" signal directly from the oscillator itself. In fact, the only way to break the loop is to introduce a delay between the generation of such a signal and its actual addition to the capacitor voltage. However, since this delay will dominate the timing (and noise) behavior of the oscillator, it has to be very accurate and stable. It is unlikely that such a delay can be constructed with the same components available to implement the relaxation oscillator. If it were, possible, an oscillator would probably have been built around these components. Therefore, the only way to generate a delay that properly fits the requirements is to use a second relaxation oscillator. Figure 26.35 depicts the principle.

Figure 26.36 shows an implementation containing simple versions of relaxation oscillators; two emitter-coupled multi-vibrators. The quadrature coupling is realized by two differential pairs operating as limiters, depicted below the capacitors, that detect the zero crossings of the capacitor voltage and injected their output signal into the other oscillator. The mutual injection of zero crossings ensures that the two oscillators run in quadrature. The injected signals have

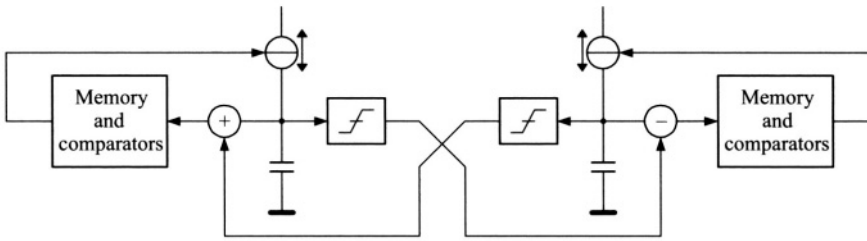


Figure 26.35. Breaking the negative feedback loop through quadrature coupling of two relaxation oscillators [9,19,23].

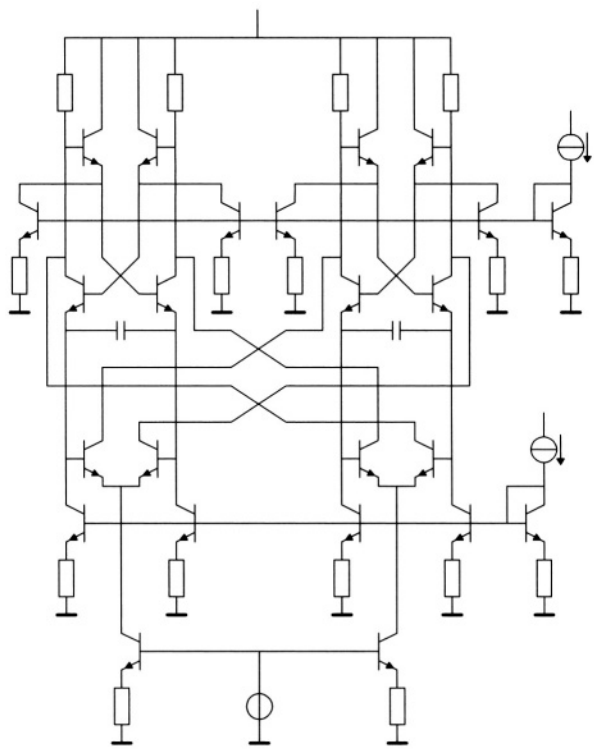


Figure 26.36. Implementation of a quadrature relaxation oscillator according to Figure 26.35.

no immediate timing relation to the switching of the oscillator; the negative feedback loop is broken. Due to this, the noise behavior of this topology is very good.

The extra feature of the topology, the fact that it produces nearly perfect quadrature signals, makes it extra attractive. The stability of the phase relation between the quadrature signals is far better than the absolute phase stability

of the system. It can be shown that the first-order sensitivity of the quadrature relation for noise equals zero [9]. To date, this topology seems to be the most accurate way to generate quadrature signals at the highest possible frequency, typically one-fifth of the f_T of the transistors; since no double frequency is needed to drive any dividers. Further, the quadrature relation is frequency independent since (frequency dependent) phase shifters are not used. Unlike the other methods to create quadrature signals, here is an active feedback mechanism that keeps the oscillators in quadrature, which is responsible for the extreme stability of the quadrature relation, without a compromise to the maximum operating frequency.

In-phase coupling. Another way to couple relaxation oscillators is *in-phase* coupling. Whereas quadrature coupling can only be applied to two oscillators, in-phase coupling can be applied to an arbitrarily large number of oscillators in parallel. The improvement of the noise behavior achieved in this way is not based on improvement of the excitation of the regenerative part, or by breaking the negative feedback loop, but on averaging. In a system of in-phase coupled relaxation oscillators, the oscillator that switches first initializes the switching of all other oscillators in the system. The average switching instant of the system is advanced and, more important, the variance of the switching instant is reduced.

Figure 26.37 shows how the noise behavior improves when the number of oscillators in the system is increased. For an increasing number of oscillators, the average of the state transition time reduces, while the distribution narrows. A system like this is very robust. A faulty oscillator would not hamper proper operation of the system. Large numbers of oscillators are needed to obtain a significant improvement. However, gradually, technology begins to offer the

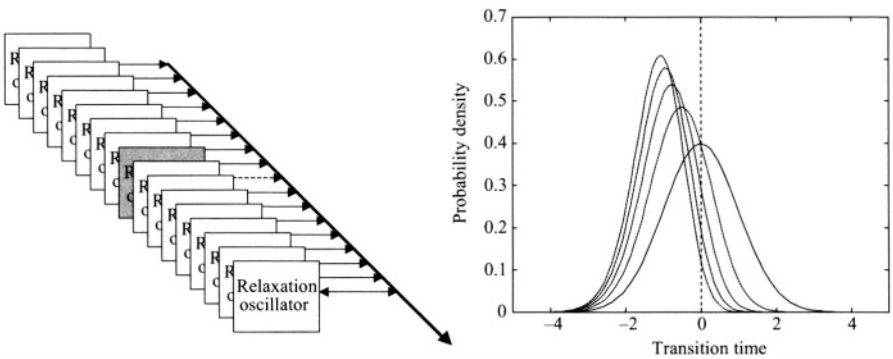


Figure 26.37. In-phase coupling of relaxation oscillators and probability density of the state transitions.

possibility to actually build systems like this. This type of oscillator systems can eventually attain the stability of a crystal oscillator, combined with the tuning range of a relaxation oscillator. There is no other oscillator topology to obtain this feature. Complex synthesizer systems also approach these characteristics, but they are more complicated to design, and much less robust. Nature shows many examples of in-phase coupled systems of relaxation oscillators, the hart muscle being one of the best known. Failure of one cell (relaxation oscillator) generally does not stop the hart. One could imagine what the changes of survival of a human being would be when the hart muscle had to rely on the pulses of one single clock-cell.

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Chapter 27

TRADE-OFFS IN CMOS MIXER DESIGN

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27.1. Introduction

Mixers are a very important block in the RF front-end, as they perform the crucial task of frequency conversion. When used in a transmitter, mixers convert baseband signals to a higher frequency for transmission. This process is called upconversion. When used in receivers, mixers convert a received signal from a high frequency to lower frequencies. This process is called downconversion. Most modern communication systems operate in the 1–2 GHz range [1]. The most widely used communication systems in Europe are GSM, which operates in the 900 MHz band, and DCS 1800, which operates at 1.8 GHz. Bluetooth devices, that are just starting to appear in the market, operate at around 2.5 GHz. The RF front-end receiver has to convert the signals it receives from 1–2 GHz down to baseband for demodulation and further processing. The exact frequencies which the downconversion mixer operates at, and the performance required of it, are strongly dictated by the receiver architecture employed. Most wireless transceivers use the heterodyne or the dual IF superheterodyne receiver architecture.

The design of a mixer depends strongly on the receiver in which it is going to be used. Although upconversion and downconversion mixers are conceptually similar, their design involves various different trade-offs that are unique to either upconversion or downconversion mixers, helping to optimize the mixer for its intended role. This chapter deals with particularly the case of downconversion mixers, primarily because a downconversion mixer, being used in the RF receive path, has to deal with a wider dynamic range of signals, which in turn places many constraints on its design. The design of downconversion (and upconversion) mixers has been dealt with exhaustively in the literature [1–4]. The aim of this chapter is not to replace these excellent texts, but rather to supplement them by highlighting various trade-offs that are often encountered in mixer design. To this end a more intuitive and less mathematical approach is employed, which should facilitate the understanding of the important underlying trade-offs in mixer design.

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As stated previously, the design of, and performance required from, a mixer strongly depends on the transceiver architecture in which it is used. This means that the trade-offs involved in mixer design are present at two levels – the system level and the circuit level. Various system level trade-offs in the design of RF front-end circuits have been dealt with in Chapter 23. This chapter concentrates on the circuit level trade-offs within the mixer itself. Nonetheless, it is useful to start off a treatment of the topic of mixers by examining the system level circuit in which a mixer will be used. Thus this introduction ends by presenting a basic heterodyne receiver architecture, and highlights the role played by the mixer in this receiver. In the rest of this chapter, after a brief explanation of mixer basics, a description of the various figures of merit used to describe mixers is given. This leads to a presentation of various mixer architectures, and a discussion of the trade-offs they represent.

27.1.1. The RF Receiver Re-Visited

In many wireless applications the received signal is typically in the order of 1–2 GHz, and has to be downconverted to baseband. In the heterodyne receiver [1,2], the RF band is first downconverted to an Intermediate Frequency (IF), before being further downconverted to baseband. It is possible to downconvert the received signal to baseband in one step, as in direct conversion or homodyne receivers [5–7]. These receivers however are very susceptible to DC offsets,[1] even-order distortion, LO leakage, etc [1]. Since the heterodyne receiver first converts the RF signal to an intermediate frequency, it avoids such problems. A block diagram of the heterodyne receiver is shown in Figure 27.1.

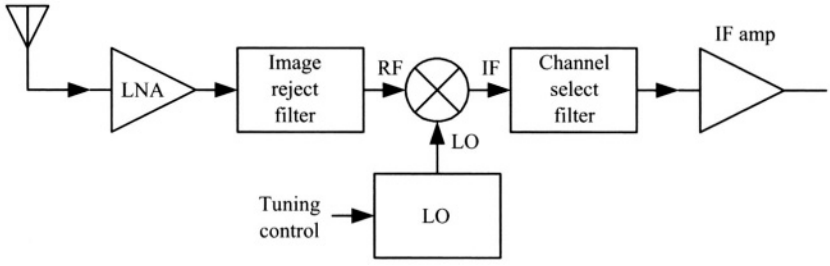


Figure 27.1. The heterodyne receiver.

[1] Even considering the drawbacks stated here, direct conversion receivers have the major advantage of reduced power consumption (since they lend themselves well to full integration, without the need for buffers to drive off-chip components). With recent advances in the technology and design of direct conversion receivers, they are becoming a serious contender.

Received signals can be quite weak, and hence they are first amplified by a Low Noise Amplifier (LNA). The gain of the LNA also helps reduce the noise contribution from the image reject filter, mixer and following circuits. For the moment the mixer can be viewed as a simple analog multiplier. Therefore if both the RF and the LO signals are simple sinusoids, the operation of the mixer can be described as:

$$\begin{aligned}\text{IF} &= V_{\text{RF}} \cos(\omega_{\text{RF}} t + \phi_{\text{RF}}) \times V_{\text{LO}} \cos(\omega_{\text{LO}} t) \\ &= \frac{V_{\text{RF}} V_{\text{LO}}}{2} \cos[(\omega_{\text{LO}} - \omega_{\text{RF}})\, t - \phi_{\text{RF}}] \\ &\quad + \frac{V_{\text{RF}} V_{\text{LO}}}{2} \cos[(\omega_{\text{LO}} + \omega_{\text{RF}})\, t + \phi_{\text{RF}}] \\ &= \frac{V_{\text{RF}} V_{\text{LO}}}{2} \cos[\omega_{\text{IF}} t - \phi_{\text{RF}}] + \frac{V_{\text{RF}} V_{\text{LO}}}{2} \cos[(\omega_{\text{LO}} + \omega_{\text{RF}})\, t + \phi_{\text{RF}}]\end{aligned} \tag{27.1}$$

The multiplication of the RF and the LO sinusoids generates sum and difference frequencies, the difference frequency being the IF. The IF channel can now be filtered using a channel select bandpass filter. Thus the basic job of a mixer is one of frequency translation, or more specifically to translate the received RF frequency to a lower one. In the above example, frequency translation is shown being achieved with the multiplication of two sinusoids.

27.2. Some Mixer Basics

27.2.1. Mixers vs Multipliers

The job of a mixer is to translate an input signal to a different frequency while maintaining amplitude and/or phase information. This is shown as being achieved using multiplication in equation (27.1). However, mixers are *not* simple multipliers [4]. In equation (27.1), the IF output amplitude of a multiplier depends (ideally linearly) on both the RF and the LO input amplitudes. This implies that the LO amplitude has to be precisely controlled, or it might possibly distort the IF output. IF distortion is obviously detrimental in an AM system, where information is encoded in the amplitude of the transmitted signal. IF distortion can also be detrimental in an FM system since it changes the positions of zero crossings of the IF signal.

In a typical application, the LO will be generated in one part of the chip, and will control a mixer in another part of the same chip. It might often prove quite difficult to control the LO amplitude precisely. Moreover using a multiplier to perform the required frequency translation in the RF front-end has serious implication on the noise figure of the circuit, which will be dealt with in further detail later in the chapter.

In the RF front-end, we would like the IF signal to be an amplified, frequency translated version of the RF signal. This means that ideally we want the IF amplitude to depend only on the RF amplitude and not be controlled by the LO signal amplitude. This suggests that it is not wise to use a multiplier to perform the job of frequency translation, but rather a mixer. The mixing operation is described by equation (27.2) below:

$$\text{IF} = V_{\text{RF}} \cos(\omega_{\text{RF}} t) \times \text{sgn}(\text{LO}) \tag{27.2}$$

Since the RF input is only being multiplied by the *sign* of the LO input, it can be conceptually thought of as being multiplied by a square wave alternating between ±1 at the frequency of the LO. This is depicted in Figure 27.2.

The conceptual representation of Figure 27.2 lends itself easily to describe the operation of a mixer mathematically:

$$V_{\text{IF}} = V_{\text{RF}} \cos(\omega_{\text{RF}} t) \times \text{square}(\omega_{\text{LO}} t) \tag{27.3}$$

Substituting for the Fourier series expansion of a square wave gives

$$\begin{aligned} V_{\text{IF}} &= V_{\text{RF}} \cos(\omega_{\text{RF}} t) \times \frac{4}{\pi}\left[\cos(\omega_{\text{LO}} t) + \frac{1}{3}\cos(3\omega_{\text{LO}} t) + \cdots\right] \\ &= \frac{2V_{\text{RF}}}{\pi} \cos(\omega_{\text{IF}} t) + \cdots \end{aligned} \tag{27.4}$$

where higher order multiplication terms will be filtered out at the output of the mixer. It should be obvious from the multiplication in equation (27.4) that mixing provides many complex harmonics in the output spectrum. Of these, only the first IF harmonic is desired.

Therefore, employing a mixer which multiplies the input RF signal by a square wave at the frequency of the LO, results in an IF whose amplitude is only dependant on that of the RF input. Multiplication provides amplitude

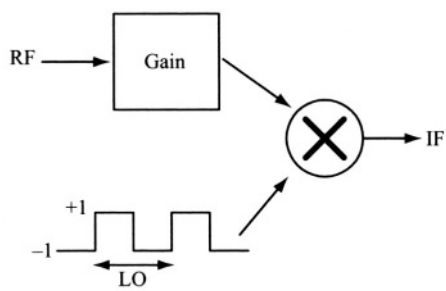


Figure 27.2. Conceptual representation of a mixer.

linearity with respect to the LO input as well, but this is not really required in an RF front-end.

Multiplication is easy to obtain in circuits – all that is required is a nonlinear device. To this end even a simple diode or MOSFET will do, since any nonlinear device will provide multiplication between signals applied at its input.[2]

Mixing on the other hand will require more complex circuits. Nonetheless mixing is more desirable over multiplication in the RF front-end since the amplitude of the IF output is only dependant on the amplitude of the RF input. Furthermore mixing traditionally yields lower noise figures [4] since only some of the transistors in the circuit are switched on at any time. This is described in greater detail in Subsection 27.4.6.

27.2.2. Mixers: Nonlinear or Linear-Time-Variant?

A nonlinear system is one which does not obey the principle of superposition. Nonlinear systems are capable of producing frequency components at the output that were not present at the input, while linear systems are not. It was stated above that frequency translation (via multiplication) can be easily be obtained from a simple nonlinear device. Since the operation of mixing also provides frequency translation between its input and output, it stands to reason that a mixer is a nonlinear device.

However, one of the important figures of merit of a mixer is its linearity. Being interested in the linearity of a nonlinear circuit (where this nonlinearity is essential in providing frequency translation) seems to be a contradiction in terms! This contradiction can be avoided by thinking of a mixer as a linear-time-variant circuit with respect to its RF input [1].

A circuit is said to be time-invariant if a time shift in its input results in the same output time shift, that is, for a system described by the equation below:

$$y(t) = F[x(t)] \tag{27.5}$$

A time shift in its input should produce

$$y(t - \tau) = F[x(t - \tau)] \tag{27.6}$$

Time-variant systems do not obey equation (27.6). To see how a mixer can be thought of as a linear-time-variant circuit, consider the conceptual representation of a switching mixer from Figure 27.2 reproduced below.

---

[2] Nonlinearity by definition provides intermodulation between its various inputs and produces extra frequency components in the output spectrum. A desired IF output can be obtained from solely a simple nonlinear device by the intermodulation between its RF and LO inputs, although this might not necessarily provide a multiplier with sufficiently good performance.

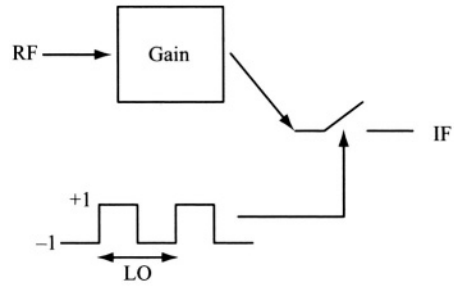


Figure 27.3. The mixer as a linear-time-variant circuit.

In Figure 27.3, the multiplier block has been replaced by a simple switch controlled by the LO signal. This is still conceptually correct with basic mixer operation as described in equations (27.3) and (27.4). When considering the IF output with respect to the LO input, the system is nonlinear, because the IF output only depends on the polarity of the LO input. However, when considering the IF output with respect to the RF input, the system is actually linear (the IF amplitude is linearly proportional to the RF input when the switch is closed) but also time-variant, since the switch is being controlled by the polarity of the LO input. Since in an RF front-end receiver, the signal flow path of interest is from the RF through to the IF, then the mixer can be thought of as a linear-time-variant circuit.

It is not only nonlinear circuits, but also linear-time-variant circuits that can produce frequency translated outputs. Thinking of the mixer as a linear-time-variant circuit helps clear up any confusion that might arise when talking about the linearity of a mixer, and aids analysis of the circuit. Although it does not explicitly express it, the linearity of a mixer concerns the linearity from the RF input to the IF output. The discussion here of linear-time-variance, only applies to mixers (i.e. switching circuits as opposed to non-switching multipliers), and even then only when considering the circuit from the RF input terminal. This does not apply to simple multipliers, which are indeed nonlinear circuits, and whose output exhibits (possibly) linear behavior with respect to both inputs.

27.3. Mixer Figures of Merit

Before examining mixer architectures it is useful to first understand the performance parameters of mixers, so that comparisons can be made between the various mixer topologies. This section presents the main figures of merit that characterize a mixer.

Simulating mixers to determine these figures of merit can prove rather difficult, due to the time-variant nature of mixers. This renders conventional ac

analyses useless since an ac analysis would linearize the mixer, and not simulate its switching behavior. Traditionally, transient analysis has been the only method to simulate mixers. This can often be time-consuming, and provide huge amounts of output data. Time steps of transient simulations have to be selected carefully, bearing in mind that the selected time step would have to be sufficiently small to cover all the multiple frequencies of interest in the circuit. New simulation methods have been introduced recently, which greatly simplify the simulation of multiple input switching circuits such as mixers. Notably, the Periodic Steady State (PSS) series of analyses found in Spectre simplifies the task of simulating mixers while providing good agreement with traditional transient techniques.

27.3.1. Conversion Gain and Bandwidth

The concepts of gain and bandwidth when applied to mixers are similar in definition to all other amplifiers, with one crucial difference – the input and output signals of a mixer are at different frequencies. Since the output of the mixer is centered around a different frequency to the input of the mixer, the gain of the mixer is referred to as the *conversion* gain. Similarly, since a mixer has different input and output frequencies, there are *two* bandwidths associated with a mixer.

The voltage conversion gain of a mixer is defined as the ratio of the output voltage (at the IF) to the input voltage (at the RF). Similarly the power conversion gain is defined as the ratio of the output power (at the IF) to the input power (at RF). Downconversion mixers should provide sufficient gain to compensate for the loss of the IF channel select filter, as well as reduce the noise contribution from the components following it. However, if the conversion gain of the mixer is too high, a large output might saturate the following stages. The conversion gain of the mixer has to be specified carefully, after considering various system level trade-offs in an RF front-end (refer to Chapter 23).

The power conversion gain will be equal to the voltage conversion gain (when expressed in decibels) if the load (at the IF port) and source (at the RF port) impedances of the mixer are equal. This is not always the case [1], especially in an integrated implementation of an RF front-end. If the mixer is to be connected to off-chip inputs and outputs, efficient impedance matching at both the RF and the IF ports can be essential to obtaining a good conversion gain from the mixer. The choice of mixer topology can have implications on the ease of impedance matching the mixer, a topic covered later in this chapter. Due to the lack of high quality inductors within an integrated circuit [9], impedance matching is not always easy, especially in a fully integrated RF front-end.

As in all practical systems, the conversion gain of a mixer drops as the operating frequency is increased, which gives rise to a certain “bandwidth”.

Since a mixer has two operating frequencies (the RF and the IF), two bandwidths can be defined:

1 The input bandwidth is the bandwidth seen by the input signals at the RF port.

2 The output bandwidth is the bandwidth seen by the output signals at the IF port.

The input bandwidth should be sufficiently high, usually in the region of a few gigahertz, to accommodate RF signals, while the output bandwidth can be lower, since the IF is at a lower frequency. A drop in conversion gain as the RF frequency is increased can be due to either one or both of the poles at the input and output. Care should be taken when deciding on what bandwidth is required at the input and output that these values not be made unduly larger than required. An excessively high input and output bandwidth can result in a higher noise figure [2,8].

27.3.2. 1 dB Compression Point

The 1 dB compression point is a performance parameter that measures the linearity of a mixer. The mixer has previously been described as a linear-time-variant circuit. However a mixer, as with any other circuit, is not ideally linear,[3] and so it suffers from gain compression from the RF input to the IF output. A strong input signal can saturate the mixer, causing a reduction in the mixer's conversion gain. The origin of gain compression is described mathematically below [10].

The output of any nonlinear system can be expressed as a power series in terms of its input:

$$y = a_0 + a_1 x + a_2 x^2 + a_3 x^3 + \cdots \tag{27.7}$$

Here a_1 is the linear or small-signal gain of the system. In differential circuits, the output will not contain any even order terms, which will cancel out due to the differential nature of the circuit. In this case equation (27.7) becomes

$$y = a_1 x + a_3 x^3 + a_5 x^5 + \cdots \tag{27.8}$$

If the input to the system is a simple sinusoid, $\rho \cos(\omega t)$, equation (27.8) can be expanded [10] to give

$$y = \left(a_1 + \tfrac{3}{4} a_3 \rho^2 + \cdots\right) \rho \cos(\omega t) + \left(\tfrac{1}{4} a_3 + \cdots\right) \rho^3 \cos(3\omega t) + \cdots \tag{27.9}$$

---

[3] Perhaps a better way of describing a mixer is as a weakly nonlinear time variant circuit. No circuit built can be described as totally linear, although with the current trend in MOSFET technologies, the MOSFET is certainly becoming more linear – at the expense of transconductance.

It is clear from equation (27.9) that the output of the system contains multiple harmonics of the input-frequencies that are not present in the input spectrum. The large-signal gain is the coefficient of the fundamental frequency at the output:

$$\left(a_1 + \tfrac{3}{4}a_3\rho^2 + \cdots\right) \tag{27.10}$$

In most systems, the coefficient a_3 is negative, and hence as the magnitude of the input, ρ, is increased, the gain of the system is reduced. The 1 dB compression point is defined as the input power when the fundamental frequency at the output falls 1 dB below its small-signal (or low-power) value. This is described graphically in Figure 27.4.

The above mathematical description of the 1 dB compression point is a rather simplistic view. The coefficients a_0, a_1, etc. have been assumed to be frequency independent constants. In reality this is obviously not the case, where these coefficients will be frequency dependent, due to the frequency dependent behavior of the components present (intentionally or due to parasitics) in the circuit. The frequency dependence of the coefficients vastly complicates matters when estimating 1 dB compression points using the equations above. This renders the above equations useful only in providing an intuitive understanding of the origins of a 1 dB compression point in practical circuits. Any proper estimation of high frequency 1 dB compression points would require the use of more advanced techniques (such as a Volterra series) or a numerical circuit simulator.

In addition to the odd-order nonlinearities described above, limiting [3] (current limiting and/or voltage limiting) can also give rise to gain compression. If limiting is the main source of gain compression, the output power of

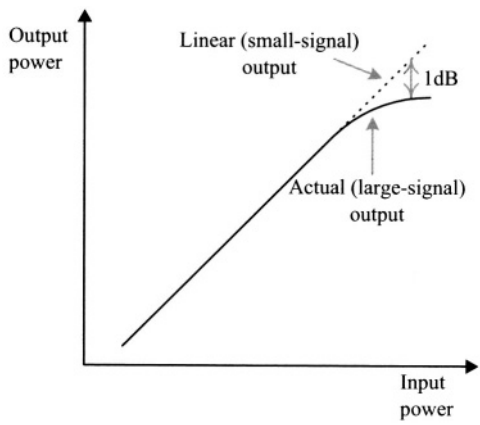


Figure 27.4. The 1 dB compression point.

the fundamental harmonic drops abruptly rather than gradually as depicted in Figure 27.4. Input power levels above the 1 dB compression point can cause quite high distortion in the amplitude of the desired output signal. This is obviously detrimental to AM systems, where the transmitted information is carried in the amplitude of the signal. However even FM systems can be affected, since the zero crossings of the desired signal will be shifted [1]. As a rule of thumb, the 1 dB compression point is an estimate of the largest signal that can be processed by the receiver, and hence sets the upper bound on the dynamic range of the mixer, the lower bound being determined by the noise figure.

27.3.3. Third-Order Intercept Point

Due to the nonlinear behavior of mixers, two adjacent channels (or interferers) will generate intermodulation products at the output. The origin of these intermodulation products can be described using similar power series analysis techniques used above. Please refer to [10] for a full derivation. Figure 27.5 describes how an RF channel and an interferer generate intermodulation products after downconversion.

The 3rd order intermodulation products generated due to adjacent RF channels or interferers can corrupt a desired output signal if they fall within the desired channel. The magnitude of the 3rd order intermodulation products depends on the linearity of the mixer. The more linear the mixer, the better it is at suppressing the 3rd order intermodulation products. A mixer's ability to suppress 3rd order intermodulation products is measured by its 3rd order intercept point, which is defined as the input power when the 3rd order intermodulation products are equal to the linear products (the IF channel and the downconverted interferer). This is depicted graphically in Figure 27.6.

The 3rd order intercept point, or IP3 for short, refers to the point where magnitude of the intermodulation product is equal to the desired IF downconverted product. This point can either be quoted in terms of the input power or

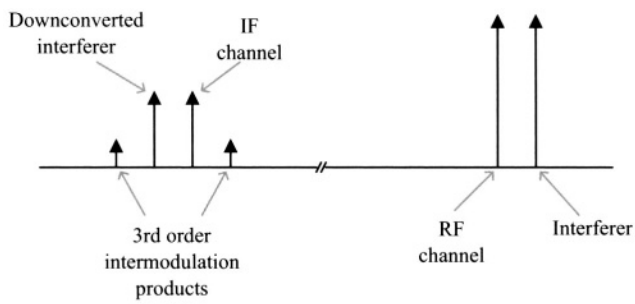


Figure 27.5. Intermodulation distortion.

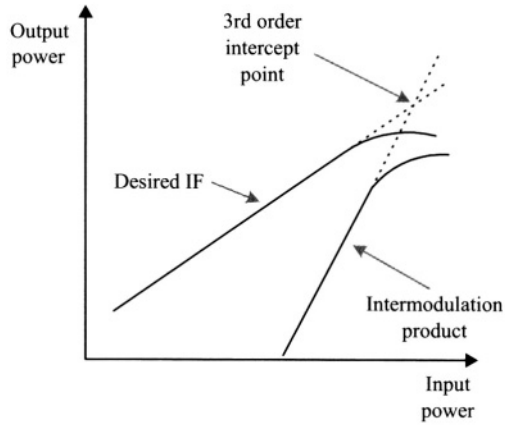


Figure 27.6. The 3rd order intercept point.

the output power in the graph in Figure 27.6. To avoid any ambiguity, when quoted as the input power it is called the input 3rd order intercept point, or IIP3 for short, and when quoted as the output power it is called the output 3rd order intercept point, or OIP3. From Figure 27.6 it will be apparent that the OIP3 and the IIP3 are related by the conversion gain of the mixer. Note that the IP3 is a purely fictitious point and cannot be directly measured in practice. This is because in a practical circuit the 1st and 3rd order products do not actually intersect, but rather gradually tail off as indicated in Figure 27.6. When performing a measurement, the IP3 can be determined graphically, by plotting the measured 1st and 3rd order products for low input powers (before nonlinear behavior sets in) and extrapolating to find the intersection point.

27.3.4. Noise Figure

The noise figure of a mixer [8,13] measures the signal-to-noise ratio degradation caused by the mixer. The total input referred noise of the RF receiver determines the smallest signal that can be processed by the receiver, and hence sets a lower bound on the dynamic range of the receiver. Since RF receivers often have to process very weak received signals, it is important that the noise figure of all the building blocks of the RF front-end are minimized. Mixers generally tend to be more noisy than the other building blocks in the RF front-end, hence the LNA must have sufficient gain to help reduce the overall noise contribution of the mixer.

Two types of noise figures have been defined for mixers [3]

1 Single-sideband (SSB)

2 Double-sideband (DSB)

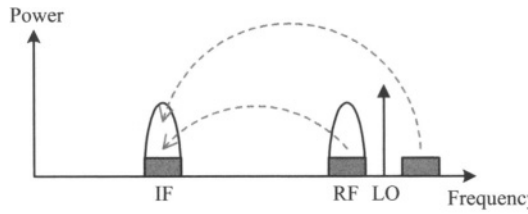


Figure 27.7. SSB noise.

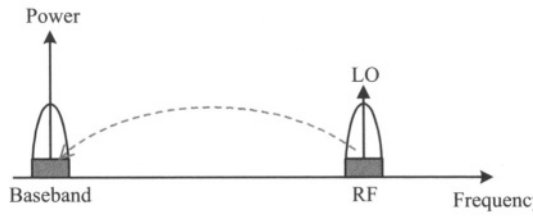


Figure 27.8. DSB noise.

Single-sideband noise figures are applicable to heterodyne receivers, where the LO is offset from the RF. As illustrated in Figure 27.7, noise from both the sidebands of the LO will be downconverted to the IF, while useful information is contained in only one sideband (hence the name single-sideband) of the LO.[4]

In direct conversion receivers on the other hand, the LO is at the same frequency as the RF, since the RF channel has to be downconverted directly to baseband (Figure 27.8). In this case useful information is contained in both sidebands.

From Figures 27.7 and 27.8, it is obvious that heterodyne receivers will downconvert twice the amount of noise compared to homodyne receivers. Hence the SSB noise figure is typically[5] 3 dB more than the DSB noise figure [2]. It is also important to note that, although it has not been depicted in Figures 27.7 and 27.8, multiple harmonics of the LO are present in switching mixers.[6] Each of these harmonics will also downconvert noise to the IF output,

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4 It has been assumed here that the image frequency has been rejected by use of an image reject filter before the mixer. In any case, the image frequency doesn't contain "useful" information.

5 The exact difference between the SSB and DSB noise figure depends on multiple factors, such as the bandwidth and relative noise contribution of the higher order LO harmonics.

6 The switching function can be regarded as a multiplication by a square wave at the frequency of the LO. It has already been illustrated in equation (27.5) that a square wave will have multiple harmonics.

and cannot be ignored in noise calculations. Careful selection of the output bandwidth of the mixer at the IF port can help reduce the total noise of the mixer.

27.3.5. Port-to-Port Isolation

The isolation between the three ports of the mixer is important, especially at the high operating frequencies of the mixer. The LO to RF isolation measures how much of the local oscillator signal appears at the RF port. Any LO leakage to the RF port can cause DC offsets in the output due to self-mixing, which can corrupt the output of a direct conversion receiver. Moreover, this LO leakage can travel through the LNA to the antenna and cause interference to other users of the same RF band. The LO to RF isolation can be maximized by designing the mixer to be as symmetrical as possible, thus hoping for two paths where any LO to RF leakage cancel each other out (refer to Subsection 27.4.5). In practice however, asymmetries in the layout and parasitics due to the packaging will limit the LO to RF isolation. LNAs are also required to have good reverse isolation to prevent any LO leakage to the RF port of the mixer from being radiated at the antenna.

The LO to IF and the RF to IF feedthrough is not as big a problem as the LO to RF feedthrough. This is because the RF and the LO are located at much higher frequencies than the IF, and hence any part of the RF or the LO that appears at the IF output can be easily removed by filtering. However, the LO to IF and the RF to IF feedthrough must not be too large, as they may saturate the output of the mixer (or the IF filter following the mixer), and hence reduce its linearity.

27.3.6. Common Mode Rejection, Power Supply, etc.

Although not specifically a figure of merit of just mixers alone, figures of merit that apply to other standard analog circuits such as amplifiers, etc. are equally applicable and important with mixers. The current trend towards systems-on-a-chip means there is increased integration of analog and digital circuits on a common substrate. Digital circuits can introduce noise on the power supply and ground lines, as well as noise in the substrate. This noise can be detrimental to the operation of analog circuits, and thus it is important to design all analog circuits in fully differential mode, so that any noise picked up from the substrate or power supply lines appears as common mode signals within the analog signal path. Therefore, in a differential mixer, the common mode rejection ratio is an important consideration.

Moreover, if the mixer is to be used in a portable application, battery life is of paramount importance. Power dissipation and power supply requirements are important figures of merit for a mixer. Note the distinction between power

dissipation and power supply requirement. This is because in a battery powered application, portable batteries can often supply only a few volts. Thus it is not sufficient that the mixer have a low power dissipation. It is also important to be able to work within the confines of the supply voltage provided by the portable battery.

27.4. Mixer Architectures and Trade-Offs

This section brings together the various figures of merit for a mixer, described in Section 27.3 above, into the trade-offs that are present in the design of mixers. Many trade-offs in mixers tend to be rather architecture dependant, and so various mixer architectures other than the standard Gilbert Cell will be presented in this section. The trade-offs that each of these architectures represents is explained. Some trade-offs in mixer design appear time and again in analog design in general, such as the sizing of transistors to trade-off gain against bandwidth, etc. This section does not deal with such trade-offs in great depth, but rather concentrates on those more specific to mixers.

A single balanced mixer is rarely used in practice, but it is the best way to illustrate the concepts presented in Sections 27.2 and 27.3. Therefore this section first presents the single-balanced mixer, then goes on to show how the double-balanced mixer is a logical step forward from the single-balanced mixer. The standard Gilbert double-balanced mixer is the mixer of choice in today's RF front-ends, and so the rest of the section presents how the various figures of merit from Section 27.3 can be traded off again each other for this mixer. This also leads to the variant architectures of the standard double-balanced mixer.

27.4.1. Single Balanced Differential Pair Mixer

A single-balanced mixer is basically a differential pair whose bias current is modulated by the RF input. It is illustrated by the circuit in Figure 27.9, which is derived directly from its bipolar counterpart. Due to LO to IF feedthrough, the single-balanced mixer is only used in communications circuits when extremely low noise figures or power consumption requirements have to be met. The more popular mixer choice is its double-balanced equivalent. However it is the easiest topology to illustrate the main stages of a mixer, and how switching provides frequency translation.

For the single-balanced mixer of Figure 27.9, the transistor Ml acts as a transconductor which converts the input RF voltage into a current, I_{RF}, that is passed to M2 and M3 (the switching pair). The IF output is obtained differentially at the drain of M2 and M3. If transistors M2 and M3 are driven with a small signal LO, the circuit forms an analog multiplier, where the nonlinearity

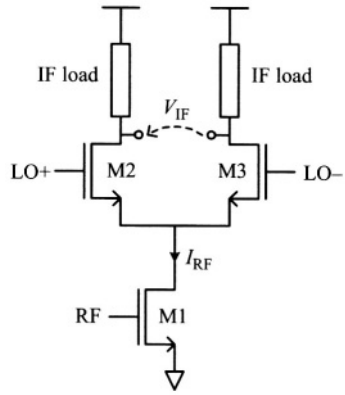


Figure 27.9. The single-balanced mixer.

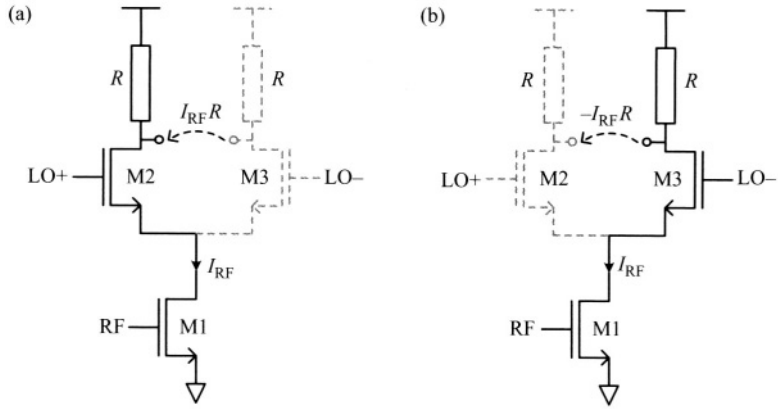


Figure 27.10. Mixer in (a) LO+ phase: 32 ON, M3 OFF, (b) LO− phase: M2 OFF, M3 ON.

of the differential pair will provide frequency translation. However for mixing purposes it is more desirable for transistors M2 and M3 to act as switches controlled by the local oscillator signals [4]. LO+ and LO– are two antiphase large signals that act as the clock for the switching pair of transistors formed by M2 and M3. Figure 27.10(a) and (b) below depict the single-balanced mixer in the LO+ and LO– phases.

In Figure 27.10, the current I_{RF} represents the ac drain current of transistor M1. As can be seen from the figure, in the LO+ phase the ac output voltage is given by $I_{RF}R$, while it is $-I_{RF}R$ in the LO– phase. Therefore the effect of the switching is to multiply I_{RF} with a square wave alternating between +1 and –1 at the frequency of the local oscillator. This can be described

mathematically [14]:

$$V_{IF} = V_{RF} \cos(\omega_{RF} t) \times g_{m1} \times R \times \text{square}(\omega_{LO} t) \tag{27.11}$$

where g_{m1} is the transconductance of M1.

Substituting for the Fourier series expansion of the square wave gives

$$\begin{aligned} V_{IF} &= V_{RF} g_{m1} R \cos(\omega_{RF} t) \times \frac{4}{\pi}\left[\cos(\omega_{LO} t) + \frac{1}{3}\cos(3\omega_{LO} t) + \cdots\right] \\ &= \frac{2 V_{RF} g_{m1} R}{\pi} \cos(\omega_{IF} t) + \cdots \end{aligned} \tag{27.12}$$

In equation (27.12) above, multiplication of the ω_{LO} and the ω_{RF} harmonics gives rise to the frequency downconversion. Equations (27.11) and (27.12) above demonstrate how the commutating action of M2 and M3 downconverts the RF signal. The preceding analysis suggests that mixers have two main stages (refer to Figure 27.3):

- a transconductance or gain stage; and
- a switching stage.

The transconductance stage converts the RF input to a current and provides the mixer's conversion gain together with the IF load. If the switching stage can be assumed to have more or less ideal switching, then the transconductance stage sets the limit on the mixer's linearity, and hence it is important to design an input transconductance that is as linear as possible. The switching stage provides the frequency translation via its commuting action, and also provides a loss of $2/\pi$. The idea of having two distinct stages in a mixer is also explained pictorially by Figure 27.3, where the transconductance stage is the RF gain block.

The single-balanced mixer is rarely used in communications circuits since there is direct feedthrough of LO and RF frequencies. This is because it suffers from the clock feedthrough (via the gate-drain capacitance of the switch transistors M2 and M3) problem experienced by many clocked circuits [15]. As described previously, any LO signals that appear at the output are at a much higher frequency than the IF and hence can be easily filtered out. However they are large signals and can saturate stages that follow the mixer, as well as reduce the mixer's own linearity. Furthermore, the mixer is only differential at its output, but not at the RF input. This means that many unwanted signals in an integrated circuit, such as noise on the ground line, coupling from nearby circuits and interconnects, etc. can all corrupt the RF input, and subsequently the IF output.

27.4.2. Double-Balanced Mixer and Its Conversion Gain

A double-balanced mixer is an extension of the single-balanced mixer using a Gilbert Cell [16] as the mixer core. It is illustrated in Figure 27.11 below.

The double-balanced mixer depicted above is derived directly from its bipolar counterpart, and is one of the most popular mixer architectures [3,14,17]. Transistors M1–M3 form a differential pair transconductance that converts the RF input to a current. This current is then commutated by the switching action of the mixer core formed by transistors M4–M7. If all the transistors are well matched, then LO feedthrough from M4 will be canceled by that from M6, and any feedthrough from M7 will be canceled by that from M5. Of course this requires carefully balanced LO switching and a well constructed layout.

In the process of overcoming LO feedthrough with the doubly balanced Gilbert Cell, we have now increased the noise figure of the circuit. With the single-balanced mixer of Figure 27.10, only two transistors were ON at any one time. However, with the double-balanced mixer depicted below, there are five transistors that are ON at any one time. For a constant gate overdrive bias for Ml in Figure 27.10 and M2–M3 in Figure 27.11, it can be shown that the double-balanced mixer will have a noise figure 3 dB higher than the single-balanced mixer [13].

The derivation of the gain for a double-balanced mixer is similar to that for the single-balanced mixer:

$$V_{IF} = V_{RF} G_m R \cos(\omega_{RF} t) \times \frac{4}{\pi}\left[\cos(\omega_{LO} t) + \frac{1}{3}\cos(3\omega_{LO} t) + \cdots\right]$$
$$= \frac{2 V_{RF} G_m R}{\pi} \cos(\omega_{IF} t) + \cdots \tag{27.13}$$

where the IF load is a resistor of value R, V_{RF} is the differential input voltage $(V_{RF+} - V_{RF-})$ and G_m is the transconductance of the RF input differential pair [23]:

$$G_m = \frac{1}{2} K \frac{4 I_{D1}/K - 2V_{RF}^2}{\sqrt{4 I_{D1}/K - V_{RF}^2}} \tag{27.14}$$

In equation (27.14), $K = \mu_0 C_{ox} W_2/L_2$ and is it assumed that M2 and M3 are well matched so that $W_2 = W_3$ and $L_2 = L_3$. It is obvious that the transconductance of the input differential pair varies with input voltage, giving rise to a certain linearity of the differential pair. The transconductance is maximum for small input voltages, where $V_{RF+} = V_{RF-}$ and $V_{RF} = 0$. This maximum transconductance is

$$G_{mmax} = \sqrt{\mu_0 \cdot C_{ox} \cdot W_2/L_2 \cdot I_{D1}} \tag{27.15}$$

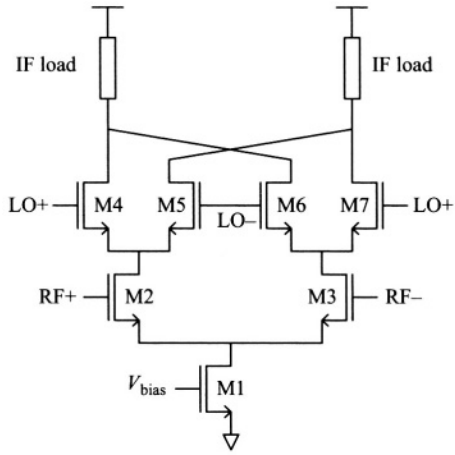


Figure 27.11. The double-balanced mixer.

Since the input stage of the mixer is basically formed by a differential pair, equation (27.15) brings to light trade-offs in the design of mixers that are common to all differential pair circuits. In order to increase the conversion gain of the mixer one has to increase G_m. This may be achieved by either increasing the tail bias current of Ml (I_{D1}), or the dimensions of M2 and M3. This, of course, trades off with higher power consumption or lower RF bandwidth respectively. Increasing the bias current of the RF differential pair can also be used to increase its linearity.[7]

However, increasing the bias current of the differential pair will also have implications for the switches M4–M7, which will now take longer to switch ON and OFF. Improper switching can be modeled by a Fourier series expansion that has many more terms than that of the ideal square wave in equation (27.13). Furthermore, the coefficient of the fundamental will be lower than $4/\pi$ in equation (27.13). Thus improper switching may lead to lower than expected linearity and conversion gain.

Changing the conversion gain of the mixer will also have an effect on the noise figure of the mixer. These effects are considered in more detail on the section on trade-offs in mixer noise figure. This illustrates that no one figure of merit can be considered in isolation. Rather, upon a design change to one of these figures of merit, its implication on all the rest has to be considered and the design altered again as required. This represents an iterative process.

The double-balanced mixer of Figure 27.11 is fully differential with respect to both its RF input and IF output. This is advantageous for reasons already

[7] The standard double-balanced mixer depicted in Figure 27.11 is a simple Class A circuit. The linearity of this circuit can be increased by increasing its gate overdrive.

presented in Subsection 27.4.1. However, in making the mixer fully differential, there are now three MOSFETs and one IF load stacked on top of each other. This rather tall stack of MOSFETs means that a higher supply voltage will be required to power the mixer. The following section examines the trade-offs that can be made to help reduce the supply voltage and power requirements for a low power environment.

27.4.3. Supply Voltage

An easy way to reduce power consumption in the standard double-balanced mixer is to directly reduce the differential pair bias current. This should be achieved by scaling down the area of M1–M3 (refer to Figure 27.11), rather than reducing the gate overdrive of M1–M3. This is because reducing the gate overdrive of M2–M3 will also reduce the linearity of the mixer.

Another technique to reduce power consumption is to directly reduce the power supply of the circuit. This is rather important in portable applications, where both the total power consumption as well as the required supply voltage is of importance (due to limitations on the supply voltages of portable batteries). A traditional technique employed in operational amplifier design is to use folded cascodes. Although the double-balanced mixer of Figure 27.11 lends itself rather well to folded cascode architectures, this is not necessarily the best solution. Although using a folded cascode architecture will reduce the supply voltage requirement of the mixer, it will increase the current requirements. Therefore, an overall saving on power consumption is not obtained.

Active loads. A first step to reducing the power supply requirements of the double-balanced mixer is to replace resistors in the signal path with active devices. In the case of the mixer of Figure 27.11 this is possible with the IF loads. However, using active devices of the IF loads as opposed to resistors will increase the flicker noise content in the output. This could be extremely detrimental if the mixer is intended for a low IF or direct conversion receiver. Using a PMOS active load as opposed to an NMOS one will help reduce the flicker noise, since PMOS devices suffer from lower flicker noise due to buried channel behavior [2,8].

Inductive current source. An alternate method of reducing the required supply voltage is to attack the 3-level stack of MOSFETs, and try reduce the number of devices stacked on top of each other. Replacing the tail current source with an inductor as depicted in Figure 27.12 helps reduce the stack of transistors: At DC, the inductor L_{tail} is a short and hence requires no supply voltage drop across it. At the high RF frequencies of operation, the inductor will appear as a rather large impedance resembling a crude current source. The

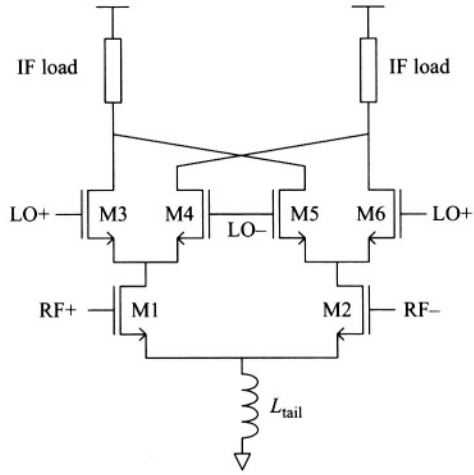


Figure 27.12. Double-balanced mixer with tail current source as an inductor.

value of inductor used has to be sufficiently high to ensure that its impedance is sufficiently high at the RF frequency of interest. Of course, this technique will work better with mixers that are to be used at high RF frequencies, to maximize the impedance of L_{tail}. However, large inductors are quite difficult to implement on an integrated circuit, and often need special processing steps to ensure a high quality factor. Further, an integrated spiral inductor is liable to pick up many interfering signals due to substrate coupling. These signals will pass right through to the output, corrupting the IF.

Two stack source coupled mixer. Since we are dealing with MOSFET mixers in this chapter, it is possible to completely omit the tail current source all together [14,19]. The input stage is now no longer a differential pair, but rather a source coupled pair. The circuit is still balanced, but will only operate in a differential manner if it is driven differentially at the RF input.

The input stage of the circuit in Figure 27.13 exploits the fact that the dominant second order nonlinearity of square law MOSFETs cancel if the circuit has balanced differential inputs and outputs [18]. If the input to Ml is $V_{\text{RF}}/2$ and the input to M2 is $-V_{\text{RF}}/2$, the differential drain current of Ml and M2 $(I_{\text{DM1}}-I_{\text{DM2}})$ is given by:

$$\begin{aligned} I_{\text{diff}} &= \beta\left(V_{\text{GS}}+\frac{V_{\text{RF}}}{2}-V_{\text{th}}\right)^2-\beta\left(V_{\text{GS}}-\frac{V_{\text{RF}}}{2}-V_{\text{th}}\right)^2 \\ &= 2\beta\left(V_{\text{GS}}-V_{\text{th}}\right)V_{\text{RF}} \end{aligned} \tag{27.16}$$

where V_{GS} is the bias gate-source voltage at the gates of Ml and M2.

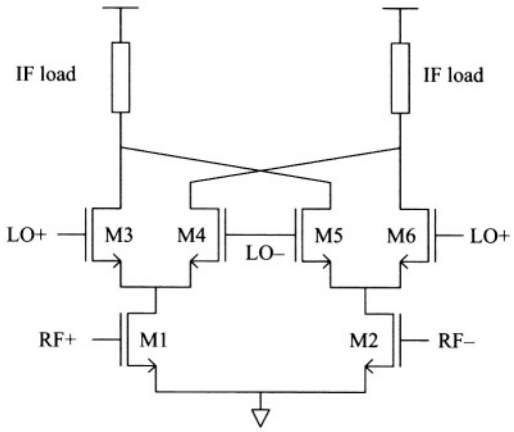


Figure 27.13. Two stack source coupled mixer.

Note that no such equivalent equation exists for bipolar mixers, since bipolar devices are governed by an exponential law rather than a square law. Equation (27.16) suggests that the linearity of the input stage depends only on V_{RF}, while the gate-source overdrive $(V_{GS} - V_{th})$ sets the transconductance. Provided there is a fairly good switching stage (transistors M3–6) the overall linearity of the mixer should be an improvement over the standard double balanced Gilbert Cell mixer of Figure 27.11. This circuit also only has two transistors stacked on top of each other, and hence can operate at a lower supply voltage.

Equation (27.16) assumes the MOSFETs are governed by a square law. This is not true in practical, short channel MOSFET circuits where once velocity saturation sets in, the MOSFET becomes incrementally linear [2]. Hence there will be some third order nonlinearity that will produce some distortion in the input stage.

This circuit has also completely traded off common mode rejection. Although the circuit has a differential input and output, it has no common mode node in it, and hence no common mode rejection. It, therefore, relies solely on the LNA that precedes it and the IF filter that follows it to provide common mode rejection. Common mode feedback can be used at the output of the mixer, but nonetheless, the common mode rejection ratio of this circuit will not be as good as the traditional double-balanced Gilbert Cell mixer of Figure 27.11.

Bulk driven topologies. A rather radical approach to reducing the supply voltage requirements of the double balanced Gilbert Cell mixer takes the idea of reducing the number of stacked transistors one step further. The concept is to use the MOSFET as a true four terminal device (gate, drain, source

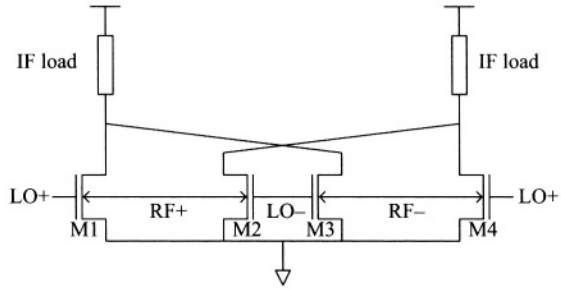


Figure 27.14. A bulk driven mixer.

and bulk), where both the transconductance and switching functions are performed by the same MOSFET. A possible bulk driven mixer configuration [20] is depicted in Figure 27.14 below.

In the configuration illustrated in Figure 27.14, LO signals are applied to the gate of the MOSFETs to switch them ON and OFF, while RF signals are applied to the back gate to modulate the output via the back gate transconductance, g_{mb}. The gain of this mixer is typically lower since the back gate transconductance is considerably lower than that of the top gate. Further, due to the lower back gate transconductance, the mixer also suffers from a lower of noise figure. However, the mixer's main advantage is its supply voltage, which only has to satisfy one IF load and the drain–source saturation condition of one MOSFET. Supply voltages for this mixer can be as low as 1V.

Implementing the mixer using NMOS transistors requires special twin-well technologies where isolated NMOS transistors are available. Alternately they can be implemented using PMOS devices in a standard technology.

The mixer core of an alternate implementation of the bulk driven mixer [21] is shown in Figure 27.15. In this implementation, the RF input drives the top gate, while the LO input drives the back gate. This will provide better noise figures and gain, since the RF input (where the noise is referred to) has the larger top gate transconductance. However, it might prove difficult to switch the transistor properly from its back gate. If the transistors are not switched properly, the circuit will operate as a multiplier rather than a mixer.

Another important system level consideration when using this mixer is that the MOSFETs at the RF input are switching ON and OFF. This means that the input impedance of the mixer can change periodically during operation. This condition is eased a bit since, for each RF input, while one MOSFET is switching ON, another is switching OFF and careful design and layout can ensure that there is reasonable cancelation of the switching effects at the RF input. Nonetheless, cancelation of the switching effects will not be exact, and so it is important to design the LNA that precedes the mixer to be capable of

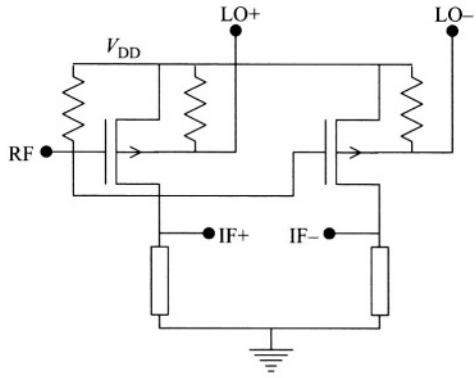


Figure 27.15. A PMOS mixer utilizing the bulk terminal.

handling the range of impedances that the mixer can present it without any potential instability problems (the LNA's operating point must not be near any stability circles[8]). The LNA must also have good reverse isolation to ensure that any harmonics at the switching frequencies of the LO do not get to the antenna.

27.4.4. Linearity

The linearity of mixers is measured by the 1 dB compression point and the 3rd order intercept point (refer to Subsection 27.3.2). The linearity of the whole mixer is usually limited by the linearity of the input transconductance stage since switching stages generally do not contribute significantly to the nonlinearity of the circuit.[9] Therefore, attempts to improve the linearity of the mixer generally focus on improving the linearity of the input transconductance stage. Indeed, the two stack source coupled mixer of Figure 27.13 was not only useful in reducing the supply voltage requirements of the mixer, but in also increasing its linearity.

Source degeneration. Standard analog electronics practice to improve the linearity of a differential pair is by source (or emitter) degeneration. When applied to the double-balanced Gilbert Cell mixer of Figure 27.11, it is depicted in Figure 27.16.

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8 Since the load impedance presented to the LNA is varying as the mixer switches, the LNA will see multiple stability circles.

9 Overlapped switching (where both LO+ and LO– transistors are on simultaneously) can affect the linearity of the mixer. This is discussed in Subsection 27.4.5.

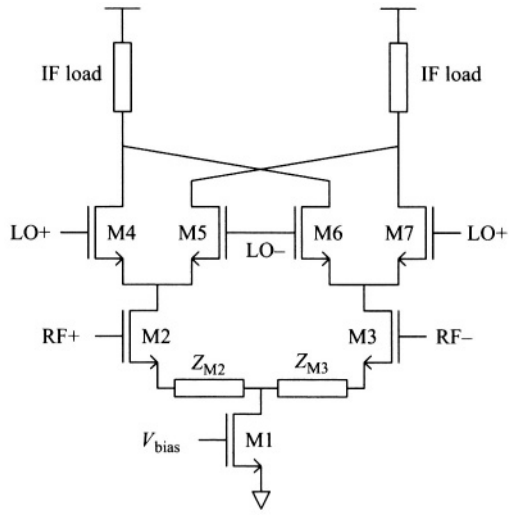


Figure 27.16. Source degenerated double-balanced Gilbert Cell mixer.

The source degeneration impedances Z_{M1} and Z_{M2} help linearize the input stage at the expense of gain. Z_{M1} and Z_{M2} can either be implemented as resistors, or more preferably as inductors since they do not require a DC supply voltage drop and do not contribute as much noise to the circuit. Inductive source degeneration has the further advantage that it can aid in source impedance matching by providing a $50\,\Omega$ input impedance (important only if the mixer is to be driven from an off-chip source) looking into the gates of transistors M2 and M3. Provided the drain of Ml is at a reasonable ac ground, the input impedance of M2 [2] can be shown to be

$$Z_{in2} = \frac{g_{m2}L_{m2}}{C_{gs2}} + j\left(\omega L_{m2} - \frac{1}{\omega C_{gs2}}\right) \tag{27.17}$$

where the degeneration impedance (Z_{m2}) used is an inductor of value L_{m2}. The equation neglects the contributions of the gate–drain capacitance (C_{gd}), which would serve to reduce the input impedance below that predicted by the equation.

The input impedance of M3 can of course be derived by an equation similar to (27.17). The input impedance of the mixer can be set to $50\,\Omega$ by designing the degeneration inductors L_{m2} and L_{m3} for a given transconductance and gate–source capacitance. The imaginary part of the input impedance can be tuned off using a series inductor (or indeed any other matching technique) at the gates of M2 and M3. Using inductive degeneration is one of the few ways to achieve a real $50\,\Omega$ input impedance at the gate of a MOSFET.

However, it is not necessary that the value of degeneration inductance required for a $50\ \Omega$ input impedance match coincides with that which is required to sufficiently linearise the mixer. As always, using inductors suffers from the drawbacks mentioned previously, that is, they are difficult to implement on an integrated circuit and are notorious for picking up substrate noise. Since Z_{M1} and Z_{M2} appear on opposite sides of a differential circuit, careful design and layout of Z_{M1} and Z_{M2} can help ensure that any substrate coupled noise appears as a common mode signal in the mixer.

Switched MOSFET degeneration. A novel technique that combines degeneration with switching is proposed in [22], and is illustrated in Figure 27.17.

In the circuit of Figure 27.17, transistors M5–M8 act as transconductors for the RF input, while M1–M4 are switched by the local oscillator. The commutating action of these switches on the RF transconductance stage helps provide frequency translation. When M1 and M4 are ON (LO+ phase), they are held in the triode region and hence act as resistors which provide degeneration to M5 and M8. Similarly, M2 and M3 act as switches and triode region degeneration resistors for M6 and M7. This helps to improve the linearity of the mixer. Since M1–M4 act as both the switching stage and the degeneration stage, there is no penalty in the minimum supply voltage of the circuit which would otherwise be increased due to the added voltage lost across the degeneration resistors.

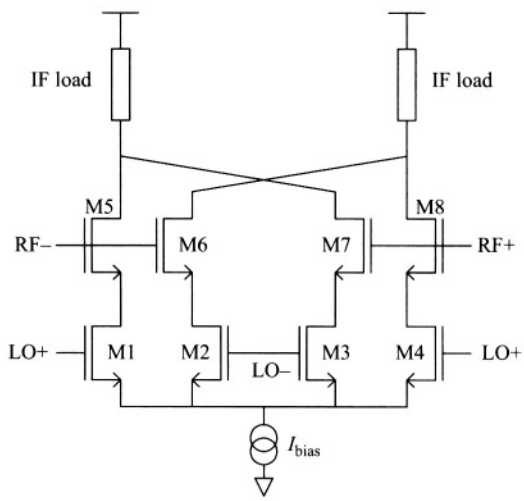


Figure 27.17. Double-balanced mixer with switched FET degeneration.

This mixer with switched FET degeneration suffers from the same varying input impedance problem as the bulk driven topologies presented in Subsection 27.4.3. The authors in [22] have used a diode connected device at the input of the mixer to help reduce the effects of this varying input impedance as the mixer switches.

27.4.5. LO Feedthrough

In a switching mixer, LO signals are reasonably large to ensure that the mixer switches properly. It is important that this large LO signals do not feedthrough to the IF output, or back to the RF input. Feedthrough to the IF output can saturate the stages following the mixer, while feedthrough to the RF input can facilitate self-mixing of the LO (and hence DC offsets), or radiation of the LO at the antenna (via the LNA). The problem of LO to IF feedthrough has already been mitigated by the double-balanced Gilbert Cell structure. Employing a tuned IF load can help further suppress LO signals at the IF port.

LO feedthrough to the RF port depends on capacitive coupling between the LO and the RF ports which is illustrated by the bold lines in Figure 27.18 below. Balanced non-overlapping switching will help greatly cancel out any LO feedthrough from the LO+ and LO– inputs. Capacitive coupling between the LO and RF ports have to be kept to a minimum, and this is strongly layout dependent.

To promote good switching within the mixer core, it might prove helpful to have a local LO buffer that drives the LO transistors in the mixer. In typical integrated circuits, the LO generator is often quite a distance away from the mixer that it is intended to drive. LO signals that travel from this LO generator could have faced significant capacitive effects before they arrive at the mixer. A local buffer can vastly help shape and boost the LO before it drives the mixer, improving switching performance. This buffer need not be more than just a few inverters. Care must be taken, however, in the layout of these inverters next to the mixer of interest. Any coupling between these inverters and the mixer core should affect both paths of the differential mixer equally.

Although a large LO drive is necessary to promote good switching, an excessively large LO drive should be avoided. In the presence of an excessively large LO drive, the gates of M4–M7 are driven well beyond the levels required for switching. The LO+ and LO– signals can couple through the gate–source capacitance of the LO transistors to nodes X and Y in Figure 27.18. If LO+ and LO– are not exactly in antiphase, there will be imperfect cancelation between the coupled LO signals. This will give rise to spikes at the nodes X and Y at twice the LO frequency, as well as spikes in the drain current of M2 and M3. These spikes are generally at much higher frequencies than the IF of interest, and hence can be filtered at the output. However, large spikes at X

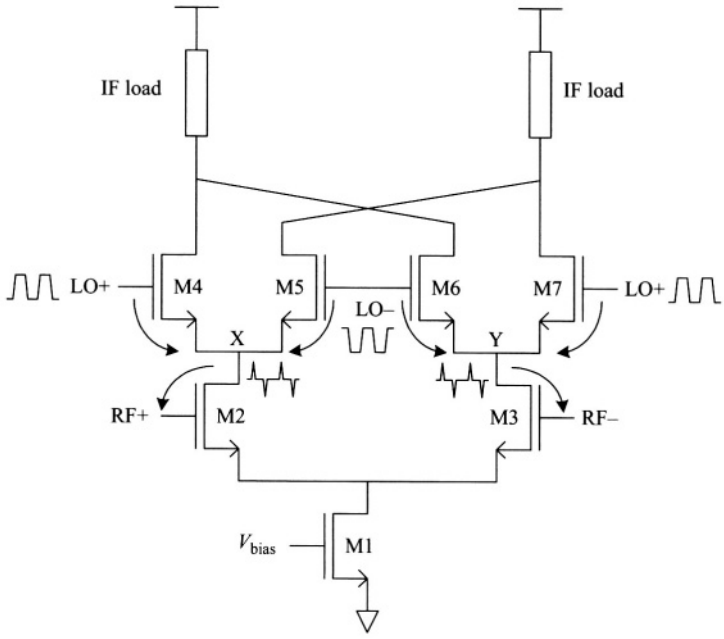


Figure 27.18. LO feedthrough paths.

and Y will noticeably affect the bias conditions of M2 and M3, resulting in 3rd order distortion. In the worst case, large spikes at X and Y can even push M2 and M3 out of the saturation region.

27.4.6. Mixer Noise

Noise in a mixer is often determined by the RF transconductance stage, which draws parallels with standard differential pair noise theory. However, the switching action of mixers provide frequency translation for not only the signal of interest, but the noise as well – a phenomenon called noise folding. As a result, one might encounter higher spectral noise density in parts of the spectrum where it is not intuitively expected. The switching action of mixers has rendered straightforward AC noise analysis tools useless in simulating the noise properties of a mixer. In recent times, SpectreRF and the Periodic Steady State (PSS) suite of tools has analyses suitable for mixer noise simulation. This section hopes to present some of the main causes of noise in a mixer, and aid the designer with a more intuitive grasp of the subject. Noise can arise due to any of the three constituent parts of a mixer: the load, the input transconductance and the switches. The rest of this section refers to noise in the

standard single-balanced mixer (Figure 27.9) and the double-balanced mixer (Figure 27.11).

Noise due to the load. The noise contributions of the mixer load are, of course, dependent on the type on load employed. If a resistive load of value R is used, then its white noise spectral density at the output is given by the well-known formula:

$$v_n^2 = 4kTR \tag{27.18}$$

To find the input referred noise due to this resistor, we have to divide by the conversion gain of the mixer given by $2G_m R/\pi$ where G_m was defined in equation (27.14).

It is extremely important to consider flicker noise at the output of a mixer, especially in a direct conversion of low IF receiver. Any flicker noise in such topologies could seriously deteriorate the desired signal. If the load resistors are made of polysilicon, then they should generally be free of flicker noise. However, if active loads are used, then flicker noise could become a serious problem. Generally, any mixer active loads should be designed using PMOS devices, since they suffer from lower flicker noise than their NMOS counterparts.

Noise due to the input transconductor. Noise in the input RF transconductor is indistinguishable from the signal of interest. Therefore it will be translated in frequency by the LO in exactly the same way as the RF signal. The input transconductor can give rise to both white and flicker noise. However, in the case of the input transconductor, white noise is more important. Flicker noise, being at low frequencies near DC, will be translated up to ω_{LO}, $3\omega_{LO}$, etc. upon multiplication with the Fourier series expansion that models the switching action of the mixer (refer to Subsection 27.4.1). This does assume ideal balanced switching in the mixer. Under realistic conditions any offset voltage in the LO stages that drive the mixer can cause non-ideal switching, where some transistors turn ON earlier, or later, than they should. This results in overlaps when all switching transistors might be ON simultaneously, which in turn can cause some of the flicker noise from the input transconductor to leak through to the IF output without frequency translation [13]. This should generally be less of a problem in a well designed mixer. Large LO amplitudes as well as careful layout can help to suppress these effects to a minimum by ensuring fast, efficient switching.

When considering the thermal noise contribution of the input transconductor, in the interests of simplicity let us first take the case of a single balanced mixer depicted in Figure 27.9. The input referred drain current thermal noise of the

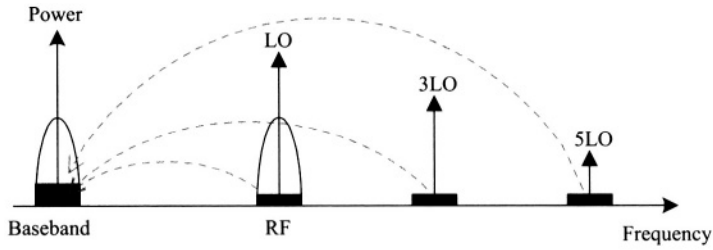


Figure 27.19. Downconversion of noise from multiple harmonics of the LO.

input transconductor (M1) is

$$v_n^2 = \frac{4kT\gamma}{g_{m1}} \tag{27.19}$$

The output thermal noise contribution of Ml is not simply found by multiplying equation (27.19) with the conversion gain. Rather, the effects of the multiple harmonics of the LO must be taken into account. Thus, the output thermal noise contribution of Ml is:

$$v_n^2 = \frac{4kT\gamma}{g_{m1}} \left(\frac{2}{\pi} g_{m1} R\right)^2 \left(1 + \frac{1}{3^2} + \frac{1}{5^2} + \cdots\right) \tag{27.20}$$

The switching action of the mixer multiplies signals (desired or otherwise) at the RF input by a square wave. The Fourier series expansion of a square wave contains harmonics at ω_{LO}, $3\omega_{LO}$, $5\omega_{LO}$, etc. The last term in equation (27.20) above models the fact that thermal noise centered around these higher-order harmonics of the LO will all be downconverted to the same IF. This be better illustrated in the Figure 27.19.

Omitting the contributions of the higher-order LO harmonics is a common mistake in calculations of thermal noise due to the input transconductance, which could result in an underestimation of noise figure by a few decibels. The exact number of LO harmonics that have to be taken into account in equation (27.20) is determined by the bandwidth of the RF stage of the mixer. The higher the bandwidth, the higher the frequency at which noticeable thermal noise exists, and hence more LO harmonics have to be taken into account. Thankfully, since the amplitude of the LO harmonics decreases with increasing frequency, their noise contribution diminishes as well.

Noise due to the switches. Again, when looking at the noise contribution of the switches within a mixer, in the interests of simplicity, lets first consider the single-balanced mixer of Figure 27.9. A potentially serious problem from the switches is their flicker noise contribution. Flicker noise in the

switches is at a much lower frequency that the LO that drives their gates. It can be modeled as a slowly varying offset voltage at the gate of either M2 or M3 that either advances or delays the instant at which the transistor switches. It can be shown [13] that the output current noise contribution from this flicker noise is:

$$i_n = \frac{4I_{D1}}{S_{LO}T_{LO}} v_{nLO} \tag{27.21}$$

where I_{D1} is the drain current of M1, S_{LO} is the slope of the LO waveform at a zero crossing, T_{LO} is the period of the LO and v_{nLO} is the flicker noise of the switches M2 and M3 referred to the gate of M2.

To find the overall input referred noise due to equation (27.21) at the gate of M1, we have to divide equation (27.21) by the conversion transconductance[10]:

$$v_{ni} = \frac{2I_{D1}}{g_{m1}S_{LO}T_{LO}} v_{nLO} \tag{27.22}$$

For a classical square law MOSFET

$$\frac{g_m}{I_D} = \frac{2}{V_{GS} - V_T}$$

while for a short channel device, this becomes [2]

$$\frac{g_m}{I_D} = \frac{1}{V_{GS} - V_T}$$

Substituting for a short channel MOSFET's g_m into equation (27.22) gives a final expression for the input referred flicker noise contribution of the switches:

$$v_{ni} = \frac{2(V_{GS} - V_T)}{S_{LO}T_{LO}} v_{nLO} \tag{27.23}$$

Equation (27.23) suggests several ways to reduce the flicker noise contribution of the switches. Increasing the LO amplitude promotes faster switching (larger S_{LO}) and hence reduces the effects that the flicker noise of M2 and M3 has in advancing or delaying their switching. However, a larger LO drive runs the risk generating spikes at the drain of M1, which can considerably change the bias conditions of M1, or couple through to the RF input. Faster switching can also be achieved by scaling up the area of the switches. However, this increases the total capacitance that is presented to the LO buffer driving

[10] The conversion transconductance is similar to the conversion gain. It is simply the differential output current divided by the input voltage, and is given by $(2g_{m1})/\pi$ for the single-balanced mixer of Figure 27.9.

the switches, which results in increased power consumption in the LO buffer. Equation (27.23) also suggests that reducing the LO frequency (larger T_{LO}) will reduce the flicker noise contribution of the switches. This represents more of a system level trade-off, since reducing the LO frequency will increase the IF frequency and the receiver architecture has to be able to cope with a higher IF.

Alternately the gate overdrive of the input transconductor M1 can be reduced. This directly trades off against the linearity of the mixer. The mixers presented in this chapter are all Class A circuits, and hence reducing the gate overdrive of the input transconductance will directly reduce their linearity.

All the arguments presented for single-balanced mixers in this section, can equally be applied to double-balanced mixers as well. However, comparing a double-balanced mixer and a single-balanced mixer with the same power consumption (same overall bias current), the double-balanced mixer will have a noise figure 3 dB larger than its single-balanced counterpart. This is because the double-balanced mixer has half the current in each branch (same total bias current) and hence half the gain. In order to achieve the same noise figure, the double-balanced mixer requires a larger power consumption. This is the price for the LO feedthrough reduction that the double-balanced mixer provides.

27.5. Conclusion

This chapter has presented a brief look at CMOS downconversion mixers. The authors have endeavoured to present a more intuitive look at the design of CMOS mixers. Before one can appreciate trade-offs between the various figures of merit of CMOS mixers, a good understanding of these figures of merit is necessary. Thus explanations of the various figures of merit for CMOS down-conversion mixers was presented in Section 27.3, and the trade-offs between these figures of merit was highlighted in Section 27.4. In the design of CMOS mixers, it is often the case that various figures of merit can be traded-off against each other by using different mixer architectures. Therefore, this chapter has also presented various CMOS mixer architectures. Each architecture provides certain advantages at the expense of other figures of merit, and hence the suitability of each architecture to an application has to be carefully evaluated.

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Chapter 28

A HIGH-PERFORMANCE DYNAMIC-LOGIC PHASE-FREQUENCY DETECTOR

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28.1. Introduction

Phase-locked loops are widely used as frequency synthesizers and data recovery circuits. The design of integrated phase-locked loops still remains one of the most challenging tasks in communication systems. In order to meet the stringent requirements of communication systems, low phase-noise, fast settling and low power consumption are some of the most critical aspects in PLL design, which in practice involves a lot of design trade-offs [1].

The block diagram in Figure 28.1 shows the general form of a PLL, which consists of a phase detector (PD), a low-pass filter (LPF), a voltage-controlled oscillator (VCO) and a frequency divider.

PD design issues and trade-offs are the topics of this chapter. A number of different circuits can be used as PDs. In earlier days, people used multiplier, exclusive-OR gate and JK-flipflop for phase detection. Auxiliary circuits were often needed to assist the acquisition of frequency locking. A second class of PD, the tri-state PD or phase-frequency detector (PFD), provides both phase and frequency-detection capability, which is favorably (if not exclusively) used in most phase-locked loops.

The characteristics of a PD have great impact on the performance of PLLs. This chapter will go over the features of different PDs, and focus on high-frequency PFD design. Several dynamic-logic PFDs are analyzed that more or less demonstrate certain drawbacks such as large dead-zone or blind-zone.

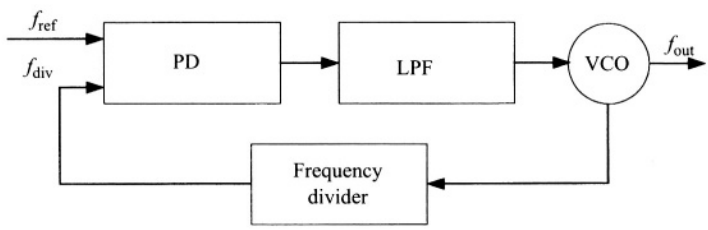


Figure 28.1. Block diagram of a phase-locked loop.

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Dead-zone and blind-zone are detrimental to the performance of PLLs, and in particular, the decrease of one of them may cause the increase of the other. To overcome these problems, we presented a new dynamic-logic PFD which presents no visible dead-zone and reduced blind-zone.

28.2. Phase Detectors Review

The operation and characteristics of different PDs are examined in this section. Two features that critically influence the loop dynamics of PLLs are under close inspection: the monotonic detection range and the frequency-detection capability.

28.2.1. Multiplier

An analog multiplier (Figure 28.2(a)) can be used for phase detection. A possible implementation of a multiplier is the Gilbert cell (Figure 28.2(b)). For proper operation, the reference input signal needs to be a sine wave:

$$V_{\text{ref}} = A_1 \sin(\omega_1 t + \theta_1) \tag{28.1}$$

The other signal is generally a square wave, which can be described by a Fourier series:

$$V_{\text{div}} = \frac{4A_2}{\pi}\left[\cos(\omega_2 t + \theta_2) + \frac{1}{3}\cos(3\omega_2 t + \theta_2) + \cdots\right] \tag{28.2}$$

Multiplying V_{ref} and V_{div}, we get:

$$V_{\text{out}} = \frac{4A_1A_2}{\pi}\sin(\omega_1 t + \theta_1)\left[\cos(\omega_2 t + \theta_2) + \frac{1}{3}\cos(3\omega_2 t + \theta_2) + \cdots\right] \tag{28.3}$$

With $\omega_1 = \omega_2$, V_{out} will be given by

$$V_{\text{out}} = \frac{2A_1A_2}{\pi}[\sin\theta_e + \cdots] \tag{28.4}$$

where $\theta_e = \theta_1 - \theta_2$ is the phase error.

After low-pass filtering, all the other higher frequency AC components will be removed, and the remaining DC term

$$\bar{V}_{\text{out}} = K_{\text{PD}} \sin\theta_e \tag{28.5}$$

reflects the phase error. Here $K_{\text{PD}} = 2A_1A_2/\pi$ is the detection gain. Note that the detection gain is dependent on the amplitude of the two inputs. The

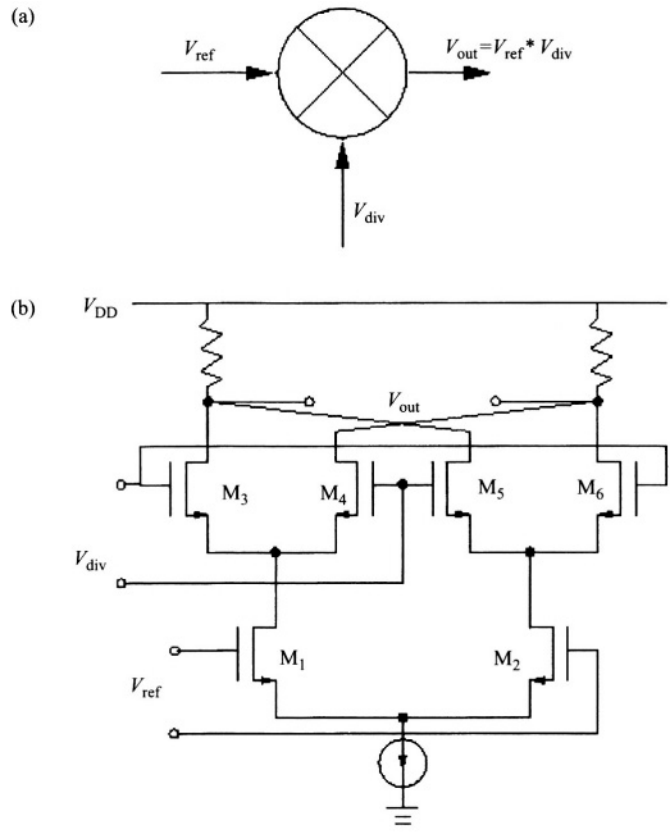


Figure 28.2. Multiplier used as PD; (a) multiplier and (b) Gilbert cell.

transfer characteristics of the analog PD is shown in Figure 28.3; we see that the analog multiplier operates nonlinearly, and the monotonic detection range is $(-\pi/2, \pi/2)$.

It is obvious that when the two inputs have different frequencies $(\omega_1 \neq \omega_2)$, $\bar{V}_{out}$ will be zero, so the analog PD is not frequency sensitive.

28.2.2. Exclusive-OR Gate

The operation of an exclusive-OR gate used as a PD is shown in Figure 28.4. When the two input square-wave signals are 90° out of phase, the output will have a 50% duty cycle, giving an average value of zero. When the phase difference deviates from 90°, the output duty cycle is no longer 50%, and the average value of the output is proportional to the phase difference. The monotonic detection range in this case is $(0, \pi)$. If the waveforms of the input signals are not symmetrical, the detection range may be significantly reduced.

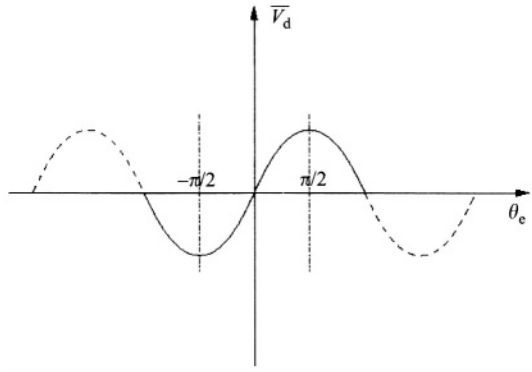


Figure 28.3. Phase characteristics of the multiplier.

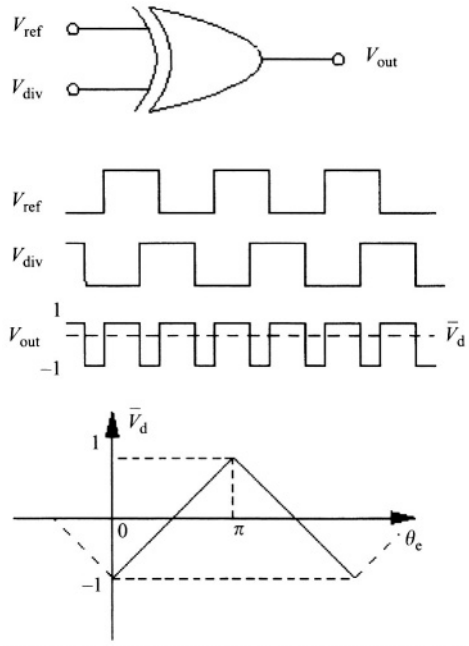


Figure 28.4. An exclusive-OR PD and its phase characteristics.

This can be illustrated by considering an extreme situation when both the inputs have a small duty cycle, for example, 1%. In this case, the average output is clipped to a value close to zero and the whole detection range is only $2\pi/100$.

Obviously, this PD is not frequency sensitive.

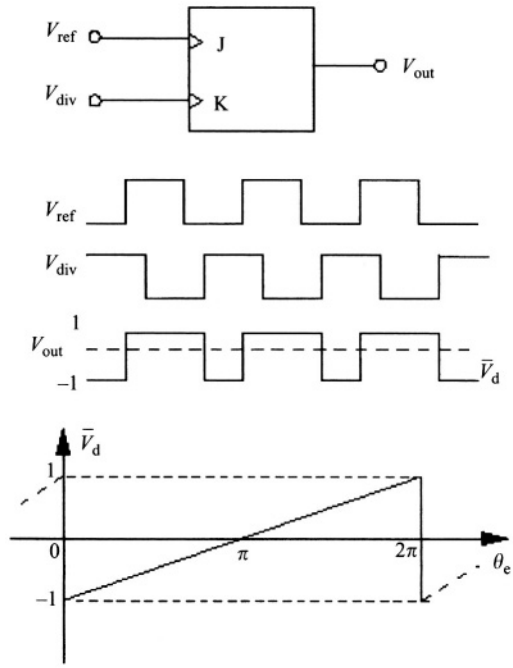


Figure 28.5. A JK-flipflop PD and its phase characteristics.

28.2.3. JK-Flipflop

An edge-triggered JK-flipflop can be used as a PD, as shown in Figure 28.5. In this device, a positive edge at the J input triggers the output to "high" and a positive edge at the K input triggers the output to "low". Note that the average of the output $\bar{V}_d$ reaches zero when the two input signals are at opposite phase. The average output reaches maximum when there is a 360° phase difference, and reaches minimum when the two signals are in phase. So the phase-detection range of this PD is twice that of the previous two PDs. In addition, because this PD is edge triggered, the waveforms of the inputs do not need to be symmetrical.

Similar to the exclusive-OR gate PD, the JK-flipflop is not capable of frequency detection.

28.2.4. Tri-State Phase Detector

A tri-state PD, or PFD, is shown in Figure 28.6. It is composed of two D-flipflops and an AND-gate, and has two output terminals UP and DN.

At any time, the two outputs of the PFD, UP and DN, will be at one of four states: 00, 01, 10, 11, with UP = high, DN = low represented by state 10, etc. The fourth state is an unstable state (at state 11, the AND-gate will reset the

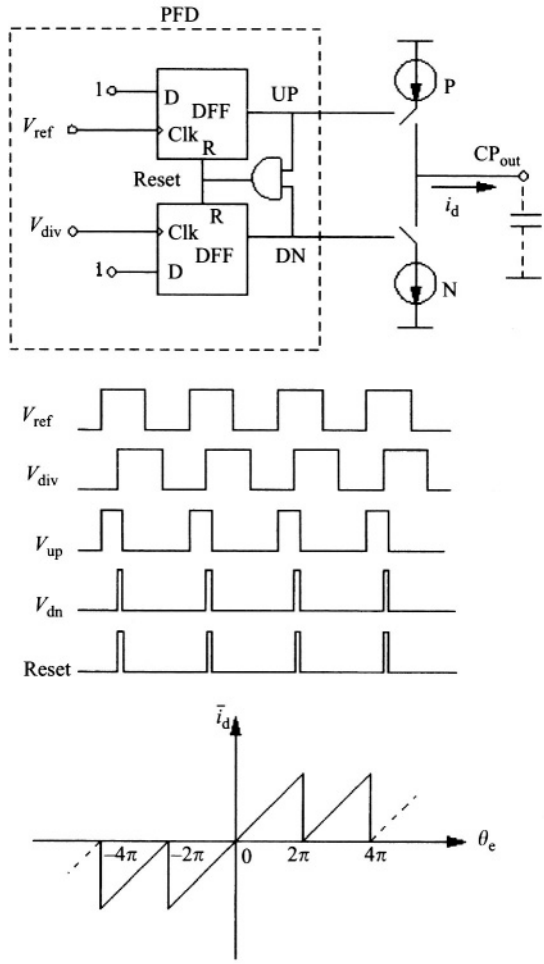


Figure 28.6. A tri-state PFD with charge pump and its ideal phase characteristics.

D-flipflops). In general, the tri-state PFD is implemented together with a charge pump, as illustrated in the dashed-line box in Figure 28.6. In this simple illustration, the charge pump is composed of a P current source and an N current source. The two current sources are controlled by the two outputs of the PFD. An active signal at UP (UP = 1) will turn on the P current source, allowing a positive current to flow into the output node (node CP_{out}) and make the output voltage to rise. Similarly, an active signal at DN (DN = 1) will turn on the N current source, which pulls current from the output node, causing the voltage at the output node to reduce. When both UP and DN are not active (UP = 0, DN = 0), both current sources are turned off from the output node, then the voltage at node CP_{out} will remain unchanged.

The operation of the PFD is illustrated in Figure 28.6 as well. A positive transition in the REF signal causes the UP terminal to transit to "high". Similarly, a positive transition in the DIV signal causes the DN terminal to transit to "high". When both UP and DN are "high", the PFD is reset, which brings UP and DN to "low". The average output of the PFD is given in Figure 28.6. This time, the output is expressed in current instead of voltage, since our interest is the average current flowing in and out of node $\mathbf{CP_{out}}$.

It turns out that the ideal linear phase-detection range of this PFD is $(-2\pi, 2\pi)$, which is twice that of the JK-flipflop PD's detection range. Beyond this range, the phase characteristic curve is periodic with a period of 2π. To look at the extra frequency-detection feature provided by this device, we assume that the REF frequency is higher than the DIV frequency. Notice that now the REF signal will have more positive transitions than the DIV signal, as such the UP terminal will have more chances to stay at "high" than the DN terminal. This means more current will flow into node $\mathbf{CP_{out}}$, causing the voltage to increase.

We conclude that the tri-state PD has superior performance than other PD in terms of phase-detection range and frequency sensitivity.

Up to now, our focus is on the ideal behavior of PDs. We will continue to investigate the non-ideal characteristics of PFD.

28.3. Design Issues in Phase-Frequency Detectors

28.3.1. Dead-Zone

Instead of using complex reset D-flipflops, a tri-state PFD is often implemented in the form of Figure 28.7 [2]. Note that the reset signal is generated from intermediate signals instead of from the UP and DN outputs directly. If the phase difference of the input signals is small, a positive transition at UP or DN will be closely followed by a reset operation. If the propagation delay at UP and DN is large enough, it is possible that UP or DN may be pulled to low by the reset operation before it completes a positive transition. Consequently, the charge pump output voltage will keep intact at a small phase difference. This phenomenon is called "dead-zone", and is shown in Figure 28.8, with the dead-zone exaggerated. In a PLL, if the input phase error is within the dead-zone, it will have little influence on the VCO control voltage. Consequently, the PLL operates as if the loop is open, and the oscillator noise will appear at the PLL output without being suppressed.

A delay cell is usually inserted in the reset path such that the reset pulse is wide enough to allow the PFD outputs become effective before they are reset (Figure 28.7). By doing so, the UP and DN outputs are given enough time to make a positive transition, and thus dead-zone can be reduced. Nevertheless, the maximum operating frequency of the device will be limited by the total delay of the reset path. Since the maximum operating frequency happens when

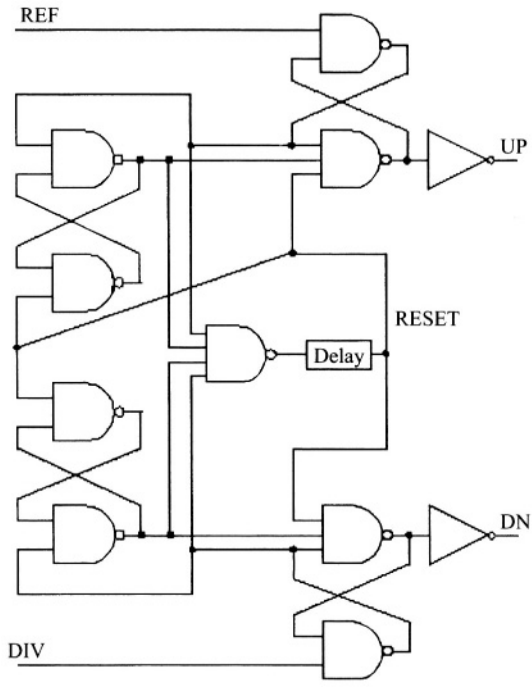


Figure 28.7. A conventional PFD.

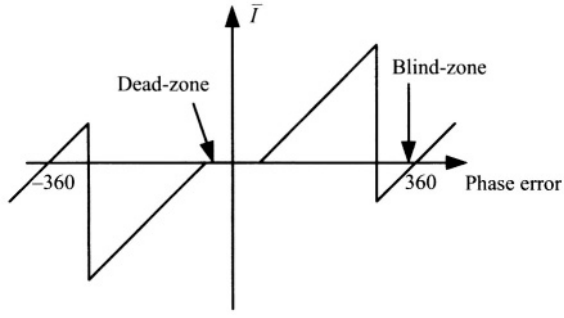


Figure 28.8. Dead-zone and blind-zone.

REF and DIV are in opposite phase [3], an approximate estimation of the operating frequency is given as follows.

Assume equal gate delay t_g for the internal gates and t_G for the driving gates of UP/DN nodes in Figure 28.7. Also, denote the delay time of the delay element as t_d. It follows that the minimum RESET pulse width is $3t_g + t_d$, and the delay time from the input (REF or DIV) to RESET is $2t_g + t_d$. Any transition edge in

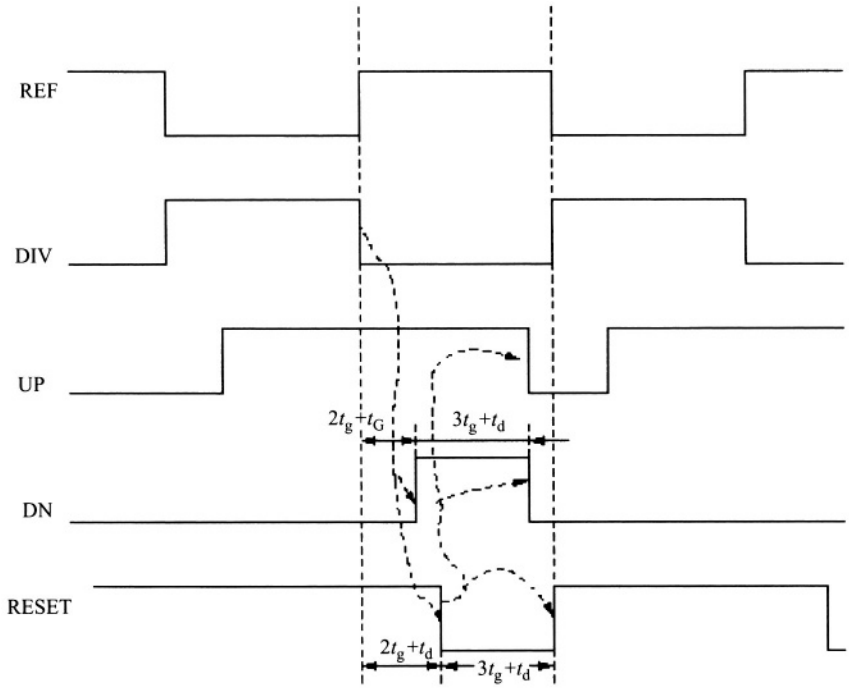


Figure 28.9. Maximum frequency estimation.

REF and DIV will be ignored during the reset operation (RESET = 1), and this is considered abnormal. To avoid such a situation, a transition in REF or DIV should happen after the reset operation. The maximum operating frequency is therefore given by

$$f_{max} = \frac{1}{2(5t_g + 2t_d)} \tag{28.6}$$

which is illustrated graphically in Figure 28.9.

28.3.2. Blind-Zone

The PFD output characteristic curve in Figure 28.8 rises monotonically with phase error. When the phase error approaches $\pm 2\pi$, the curve changes to the opposite sign abruptly. The cause of the abrupt polarity change can be explained through timing analysis. In Figure 28.10, the occurrence of a REF rising edge coincides with a reset operation (RESET = 1) and, therefore, does not have any impact on the PFD output. This situation is depicted in Figure 28.10 by the dotted area. Consequently, the leading REF signal is incorrectly indicated by the PFD as lagged (DN is wider than UP) in a subsequent cycle. As long as

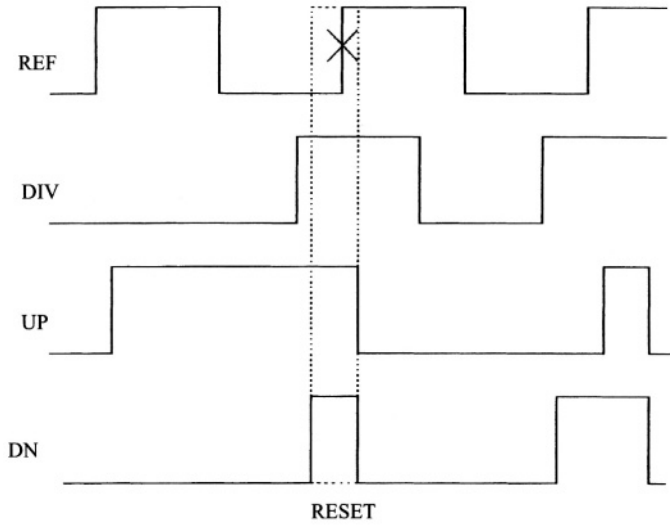


Figure 28.10. Timing analysis of blind-zone.

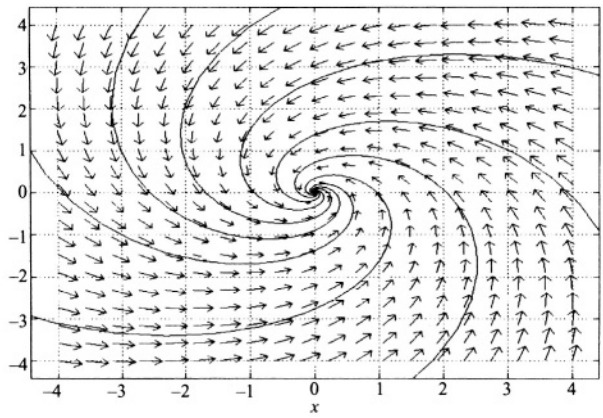


Figure 28.11. The convergence of a dynamic system.

a PFD is in reset mode, it will be blind, that is, any input transition will not be seen by the PFD.

It becomes obvious that the blind-zone of a PFD is detrimental to the PLL settling behavior, and will slow down the lock time. This can be further perceived in a Cartesian plane in which the X-axis represents phase-error $(\Delta\phi)$ and the Y-axis represents frequency error (Δf) of a PLL (see Figure 28.11): during the settling process, $(\Delta\phi, \Delta f)$ will follow a trace moving toward the

origin. If an input transition of the PFD happens to occur in the blind-zone, the trace will bounce further away from the origin, and therefore it will take a longer time for the trace to converge to the origin.

The situation that an input transition falls in the blind-zone is nevertheless a random event. In the phase plane of Figure 28.11, from different initial conditions, a PLL may follow a trace that may or may not experience a blind-zone event. If it does, the PLL is driven to follow a new trace. A blind-zone event is hard to capture during a PLL settling process. Since the reset time cannot be infinitely small, it also becomes obvious that one cannot completely eliminate blind-zone through circuit design. In practice, the only effective way to reduce the probability of having a "blind-zone event" is to reduce the blind-zone.

Having a blind-zone is equivalent to having a reduced phase-detection range. It turns out that the lock range of a PLL is proportional to the phase-detection range of the PD in use [4]. Based on the previous discussion, one can easily estimate the phase-detection range $(-\phi_{\max}, \phi_{\max})$ from the reset time of the PFD:

$$\phi_{\max} = 360^\circ(1 - t_{\text{reset}} f_{\text{in}}) \tag{28.7}$$

where f_{in} is the frequency of input signals, with $f_{\text{in,max}}$ constrained by $f_{\text{in,max}} \leqslant (1/2t_{\text{reset}})$. It follows that the phase-detection range is inversely proportional to the input frequency. Therefore, at high-operating frequency, a PFD will experience a blind-zone event more frequently. This implies that a PFD functional at low frequencies may give poor performance if the input reference frequency in a PLL is very high.

28.4. Dynamic Logic Phase-Frequency Detectors

Dynamic CMOS logic circuits and especially domino-logic have been used in high-performance designs due to their faster operating speed and potential saving in power. Several dynamic-logic PFDs were introduced in the last five years [5–8].

A pioneer dynamic-logic (domino-logic) PFD is shown in Figure 28.12 [5]. In this circuit, the outputs are reset almost immediately following a positive transition at one of the inputs if initially a positive transition has occurred at the other input. As a result, the circuit experiences dead-zone problem. In this design, dead-zone cannot be effectively reduced by adding an extra delay in the reset path as given in Figure 28.7. Furthermore, the detection range of this circuit is only $(-\pi, \pi)$. To see this problem, consider a situation that a positive transition in REF occurs when DIV = 1: in a normal tri-state PFD, following the rising edge of REF, UP should be pulled to "high". In this circuit, UP will stay at "low" instead. This is because node U1 is discharged and node U2 is charged immediately after the rising edge of REF. UP gets no time to transit to high.

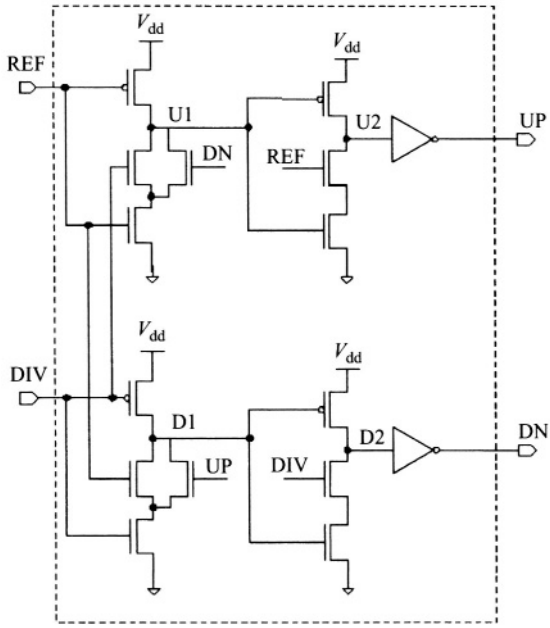


Figure 28.12. A pioneer dynamic-logic PFD.

The dead-zone problem in the above design was partially improved in [6] (Figure 28.13). This is accomplished by the three inverters and two NMOS transistors at the REF (or DIV) input, which basically form a pulse generator to create a delay for the discharge of node U1 (and U2) such that UP and DN can become effective for a certain amount of time. A defect in this circuit is that a DC path might be formed from the power supply to the ground through node U1 or U2. For instance, if DIV is transiting from 0 to 1 while REF = 0, a DC path is formed through node U1. Depending on whether the voltage at node U1 is low enough to be below the threshold of the following PMOS transistor, the UP signal may or may not be reset. Because of this, this circuit also has a limited linear detection range of $(-\pi, \pi)$.

Shown in Figure 28.14 is another dynamic PFD circuit [7]. Unlike the two dynamic PFDs discussed above, in this design, the reset action is initiated solely by the PFD outputs. This means that a reset process will not happen until UP and DN become effective. For this reason, dead-zone is not visible in this design. There also exists a defect in this circuit: assume a rising edge of REF has caused a positive transition at UP, and soon after REF returns to 0. Subsequently, if a rising edge of DIV causes a positive transition at DN, a DC path will be formed between the power supply and the ground via node U1

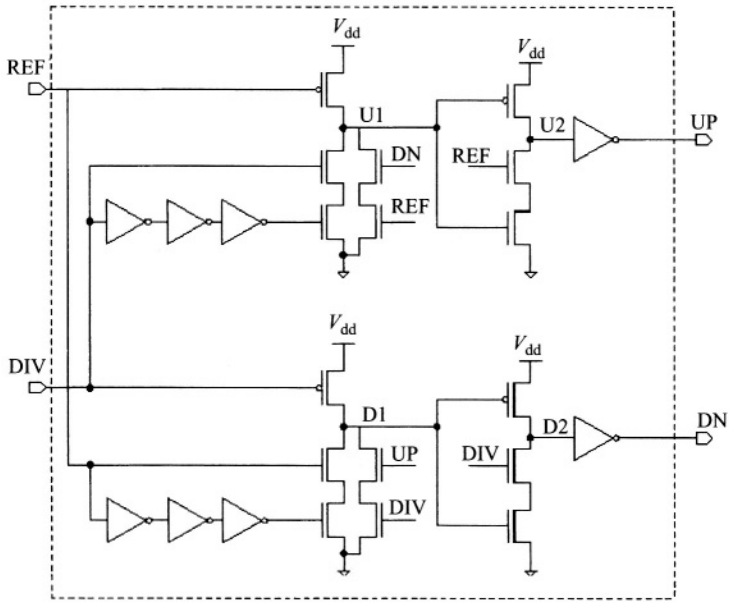


Figure 28.13. A dynamic PFD with reduced dead-zone.

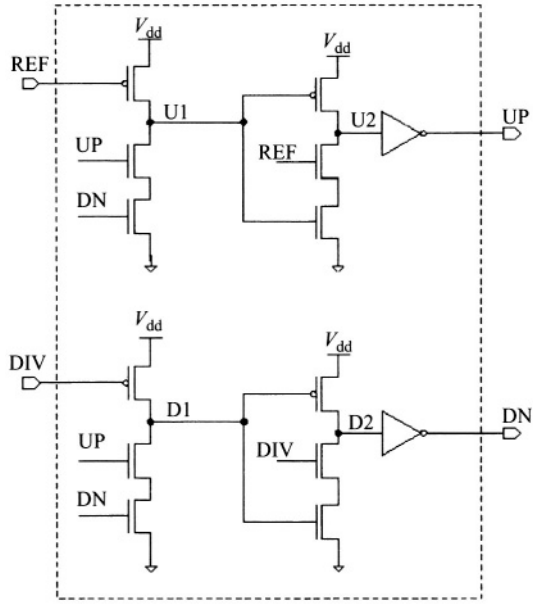


Figure 28.14. A dynamic PFD without dead-zone.

since REF = 0, UP = 1, and DN = 1. This situation is very similar to the short-circuit problem found in Figure 28.13. The linear detection range of this circuit is only $(-\pi, \pi)$ as well.

A common problem in the above three dynamic PFDs is that they are not purely edge sensitive, and especially, the two circuits in Figures 28.13 and 28.14 violate the operation integrity of domino circuits, although they seem to perform better in terms of dead-zone. By using two pulse generators (similar to that used in Figure 28.13), a dynamic-logic PFD disclosed in [8] (Figure 28.15) is made to be purely edge sensitive. The device then functions in the same way as demonstrated by the original tri-state PFD (Figure 28.6). Ideally, the phase-detection range will approach $(-2\pi, 2\pi)$. Yet, according to our analysis on blind-zone, a blind-zone of approximately three gate-delays exists in this circuit. This circuit is relatively very simple, but requires a careful control of

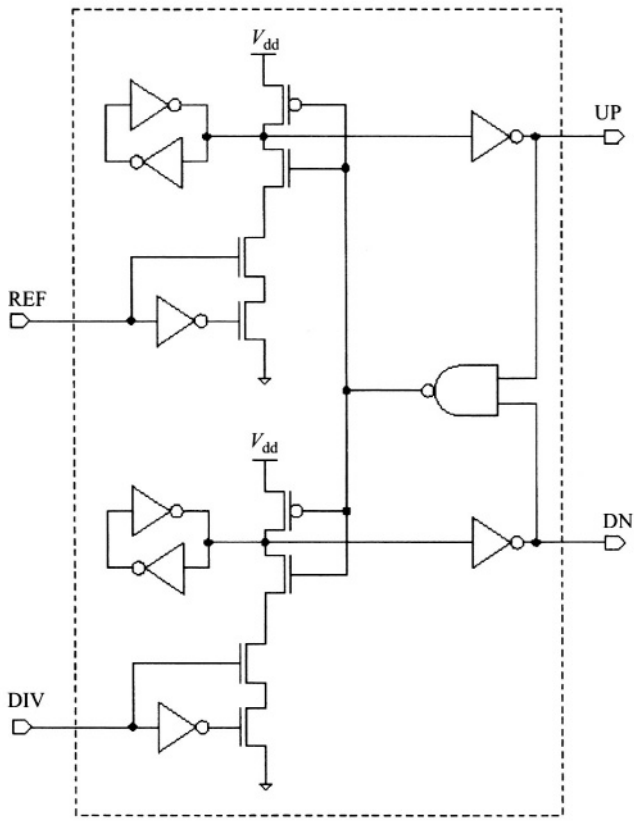


Figure 28.15. A dynamic PFD with reduced blind-zone.

the delay of the pulse generators in order to reduce dead-zone. Extra latches are used (the cross-connected inverters) in this circuit to ensure proper operation, which also slows down its operating speed.

28.5. A Novel Dynamic-Logic Phase-Frequency Detector

In an effort to design a PFD capable of working at gigahertz frequency with minimum dead-zone, minimum phase offset and reduced blind-zone, we have proposed a new domino-logic PFD. Our design goals are accomplished by overcoming the drawbacks existing in previous dynamic PFDs. Circuit integrity is maintained in this design.

The new PFD is shown in Figure 28.16. MU2-3 and MD2-3 form two inverter structures in the precharge stage that basically prevent the device from

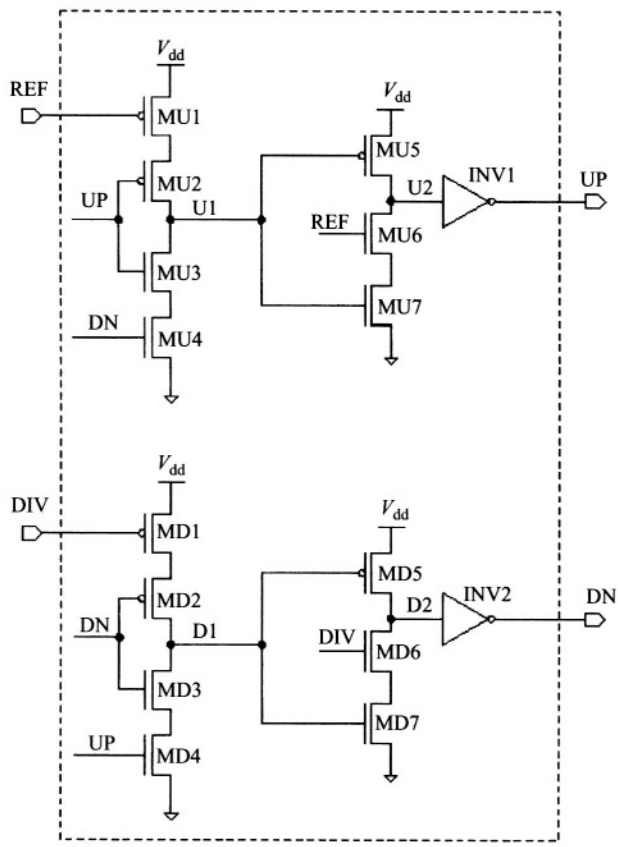


Figure 28.16. The proposed dynamic PFD.

being short-circuited as happened in Figures 28.13 and 28.14. It should become obvious that the circuit will be fully operational with a permutation of MU1 and MU2, MU3 and MU4 (also MD1 and MD2, MD3 and MD4).

The operation and the merits of this new PFD are further analyzed in the following discussion.

28.5.1. Circuit Operation

To inspect the behavior of this PFD more closely, we have shown a finite-state diagram of the PFD with all its four possible states included (Figure 28.17). In the diagram, each state transition is accompanied by its corresponding transition condition, which is basically the positive transition of REF or DIV, denoted by *REF*↑ and *DIV*↑ respectively. Two simultaneously occurring positive transitions are simply denoted by (*REF*↑ *DIV*↑).

The operation of the circuit can be explained according to the charging and discharging behavior of typical dynamic circuits. Assuming initially UP and DN are both low (state = 00) and REF and DIV are low, nodes U1 and D1 are precharged to high through transistor MU1–2 and MD1–2 respectively. At the rising edge of REF, MU6-7 are turned on, node U2 is pulled to low, which drives UP too high. Similarly, a rising edge of DIV will drive DN to high. If the rising edge of REF comes first, the state will transit from 00 to 10, and then transit from 10 to 11 upon the arrival of a rising edge of DIV. If the rising edge of DIV comes first, the state transition will be from 00 to 01 and then to 11. In the case that the rising edges of REF and DIV come simultaneously, the state will transit from 00 to 11 directly. State 11 is an unstable state, as identified by the dashed circle. At state 11, UP and DN will turn on MU3–4 and MD3–4, nodes U1 and D1 are discharged accordingly, and nodes U2 and D2 will be charged to high through MU5 and MD5, respectively. This returns the circuit to state 00.

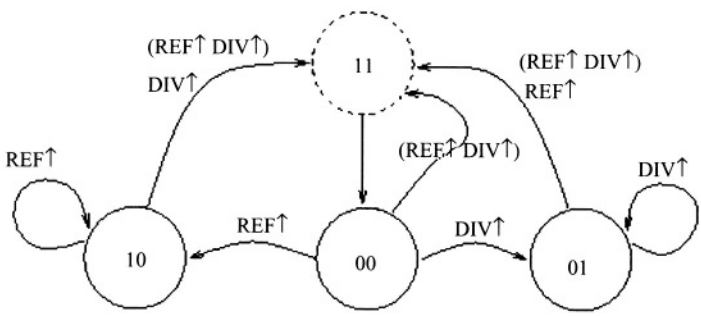


Figure 28.17. Finite-state diagram of PFD operation.

Indeed, all the tri-state PFDs operate in the above manner, that is, a rising edge of REF drives UP to high, and a rising edge of DIV drives DN to high. When both UP and DN are high, the circuit is reset, returning UP and DN to low. This general statement may disguise the truth. As we have carefully inspected all the previously mentioned dynamic PFDs, when the phase error is beyond $(-\pi, \pi)$, some of the dynamic PFDs behave differently from expected. For this reason, we examine the operation of our PFD cautiously as below.

Assume REF is leading DIV by more than 180°: initially, a leading rising edge of REF drives the device to state 10 as before. Now, upon a DIV rising edge, DN will be pulled to "low". At this moment, REF is "low", but UP is driven "high". So, the path formed by MU1-2 is shut off and no charge is injected from V_{dd} to node U1 during the time when U1 is being pulled to "low" through path MU3–4. UP is therefore reset to low normally. This clarifies that the detector indeed operates correctly when phase error lies between $(\pi, 2\pi)$.

28.5.2. Performance Evaluation

High-speed operation is one of our design concerns, so let's examine the maximum operating frequency of the circuit. As before, we assume DIV lags REF by 180°. Also we assume that the circuit is initially at state 00 and it transits to state 10 upon the arrival of the rising edge of REF. Refer to Figure 28.16, at state 10, an incoming rising edge of DIV causes node D2 to discharge. After $t_1 = t_{D2,f} + t_{DN,r}$, DN reaches high and the circuit transits to state 11. This triggers the reset mode, and after $t_2 = t_{D1,f} + t_{D2,r} + t_{DN,f}$, UP/DN are pulled down to low. Note that REF cannot rise immediately after the falling edge of UP/DN, instead, it has to wait for an additional time $t_3 = t_{U1,r}$ for node U1 to be precharged to high so as to prepare for the next cycle's operation (see Figure 28.18). The maximum operating frequency is estimated to be:

$$f_{max} = \frac{1}{2(t_1 + t_2 + t_3)} = \frac{1}{2(t_{D1,r} + t_{D1,f} + t_{D2,r} + t_{D2,f} + t_{DN,r} + t_{DN,f})} \tag{28.8}$$

In the above representations such as $t_{DN,f}$, the first subscript refers to the corresponding node in charging or discharging, the second subscript refers to a rising or falling transition.

For simplicity, let $t_g = t_{D1,r} = t_{D1,f} = t_{D2,r} = t_{D2,f}$ and $t_G = t_{DN,r} = t_{DN,f}$, the maximum operating frequency is then given by

$$f_{max} = \frac{1}{4(2t_g + t_G)} \tag{28.9}$$

where t_G depends on external loads at nodes UP and DN.

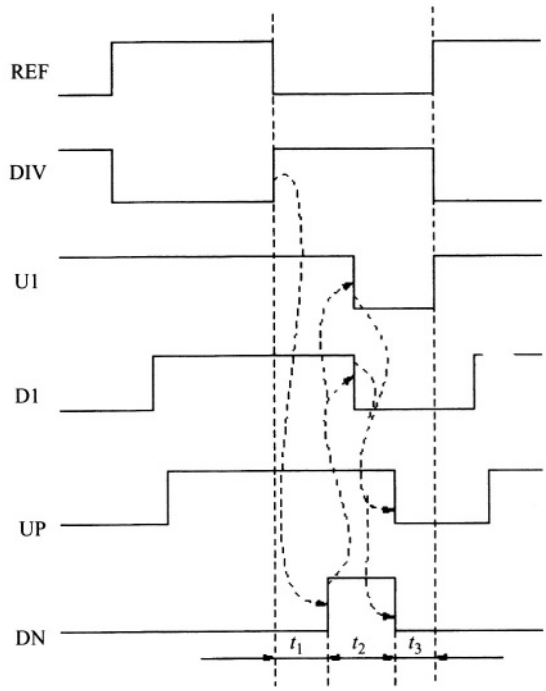


Figure 28.18. PFD Timing analysis.

Note that $t_2 = 2t_g + t_G$ corresponds to the minimum pulse width of UP and DN, and t_2 is one-fourth of $1/f_{max}$. From this observation, one can estimate the maximum operating frequency of the circuit based on its minimum UP/DN pulse. Figure 28.19 demonstrates the waveform when the two inputs are at maximum operating frequency. Indeed, in our implementation the minimum pulse width of UP and DN is around 100ps, one-fourth of the period of the maximum operating frequency.

The phase characteristic of the PFD is obtained as shown by the solid line in Figure 28.20. This clarifies our previous analysis that the circuit is able to operate up to 2π phase difference. Near the 2π phase difference, the phase curve falls down, presenting a blind-zone. Notice that the blind-zone is considerably smaller than that of the conventional PFD (dashed line). This is attributed to the smaller reset time (or small minimum pulse width). In Figure 28.20, the operating frequency applied is 500 MHz, and the blind-zone is less than 10% of a clock cycle.

The phase curve near small phase error is examined in Figure 28.21, no obvious gain degradation is found even though the phase difference is as small as 1.0ps. Also, because the PFD is symmetrical in structure, no phase offset is incurred.

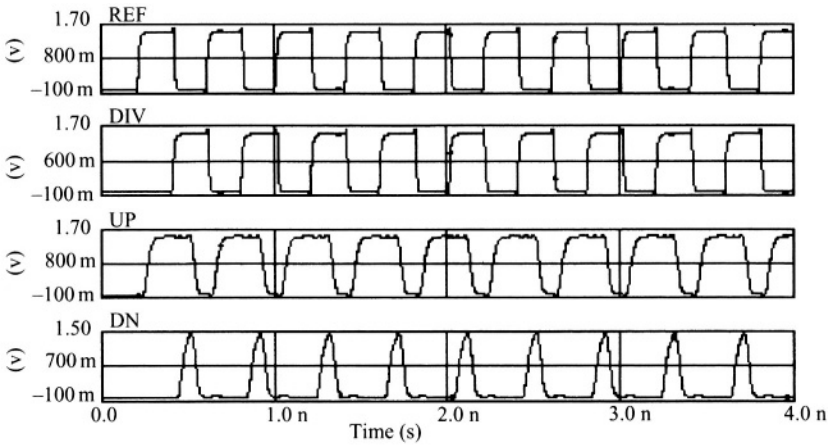


Figure 28.19. Maximum frequency test.

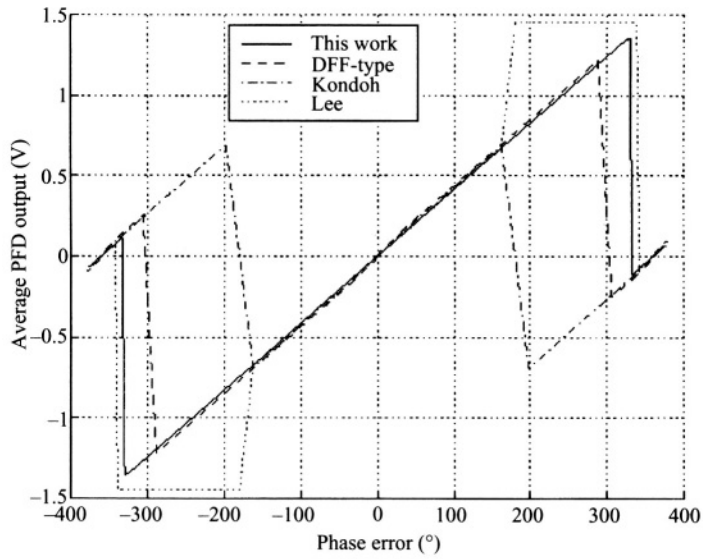


Figure 28.20. Phase characteristics of the proposed PFD (versus prior arts).

The frequency sensitivity of the proposed PFD is illustrated in the waveform of Figure 28.22. The two input signals are at different frequencies.

Charge sharing issue does not seem to impact the normal operation of the PFD although charge transfer through transistors MU2, MU3 (MD2, MD3) changes the voltage level at node U1 (D1). This can be attributed to the larger noise threshold provided by the double-buffer structure formed by MU5–7 and INV1 (as well as MD5–7 and INV2).

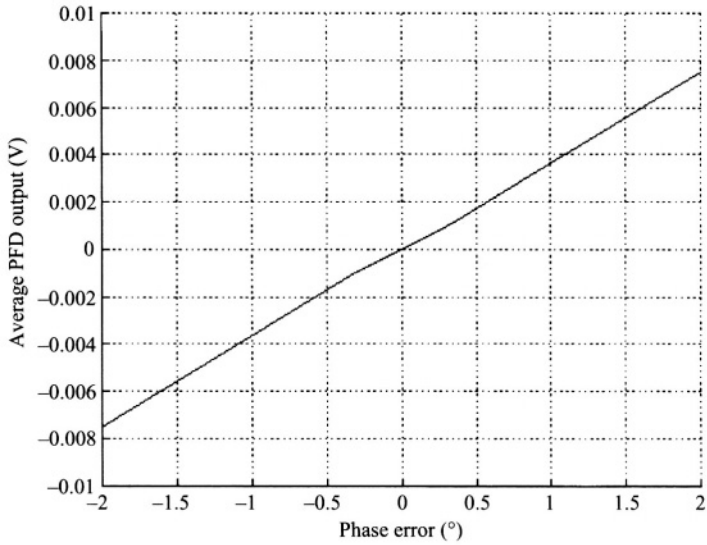


Figure 28.21. Magnified view near zero phase error.

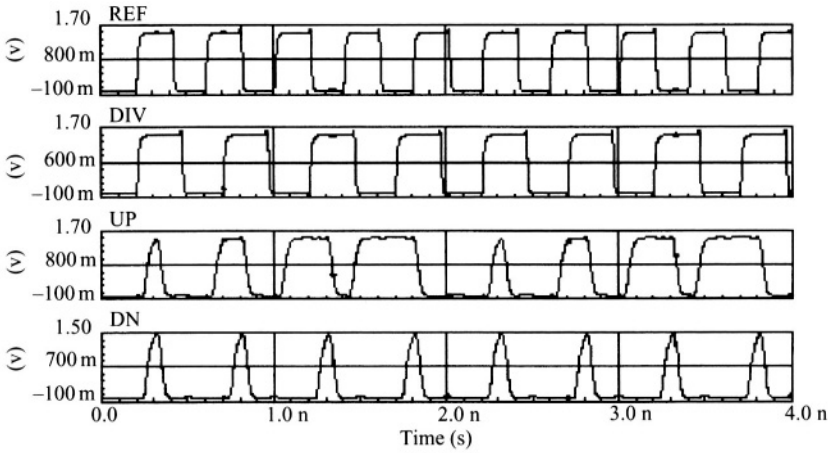


Figure 28.22. Frequency sensitivity.

It turns out that the cascaded PMOS transistors (MU1–2, MD1–2) are the limiting factor for the PFD to run at higher speed. Nevertheless, compared with other PFDs requiring more complexity to achieve similar performance, speed is not sacrificed in this design. Benefiting from the very simple structure, no particular design efforts and trade-off are required in designing this PFD.

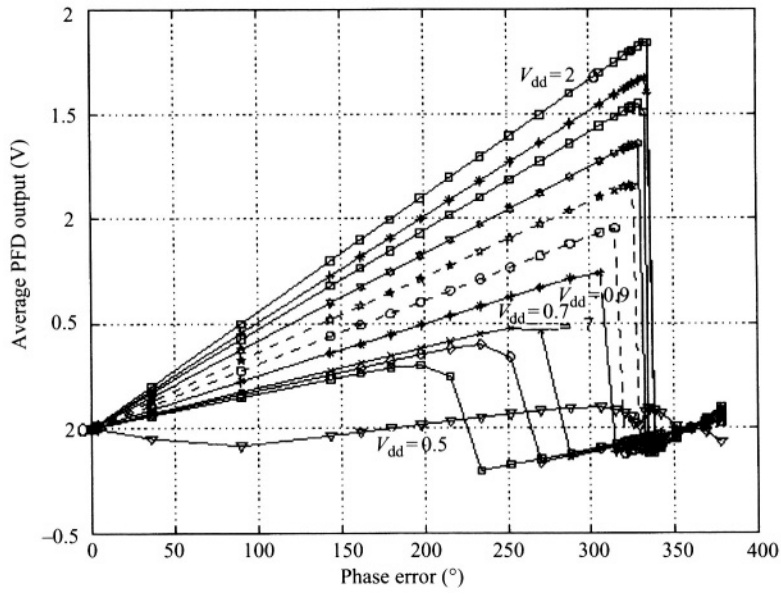


Figure 28.23. Phase characteristics under various power supplies.

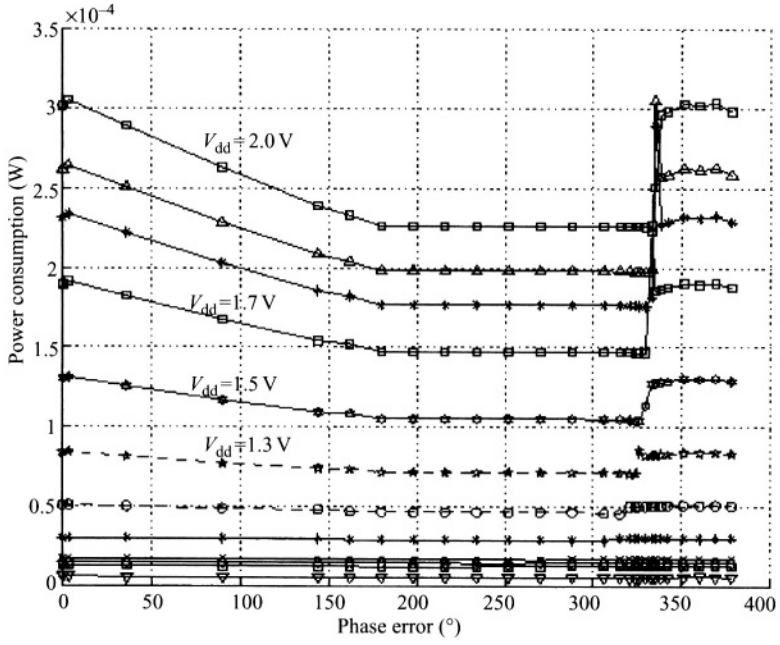


Figure 28.24. Power consumption under various power supplies.

Under different corner and temperature tests, the device appears to be very robust, and still presents a linear detection range greater than π even when the power supply is as small as 0.7 V. This is illustrated in Figure 28.23.

At 500 MHz, the power consumption of this device is less than $400\,\mu W$ for 1.5 V power supply, which is trivial compared with other blocks in a PLL (Figure 28.24).

28.6. Conclusion

A new domino-logic PFD with extended phase-detection range and no visible dead-zone is designed to operate at high frequency and low power consumption. The new PFD has the simplest form and uses only 18 MOS transistors. The design is achieved through the analysis of the shortcomings in previous PFD circuits. In particular, we have maintained the operation integrity of domino-logic circuit, which is the key to obtaining the improved performance for the new PFD.

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Chapter 29

TRADE-OFFS IN POWER AMPLIFIERS

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29.1. Introduction

The most power-consuming part in a mobile phone is the power amplifier, which amplifies the modulated RF signal and delivers it to the antenna. A highly efficient power amplifier reduces the power consumption of the phone and the heat generated. The reduction in the power consumption increases the "talktime" and reduces the size and the weight of the battery. The reduction in the heat generated reduces the risk of local overheating and relaxes the heat dissipation requirement of the package. With these benefits, a highly efficient power amplifier enhances the competitiveness of a product in a keen mobile communication market.

In order to reduce power loss, the number of transistors is minimized. Usually, only one transistor is required for a single-ended power amplifier and the use of resistors is avoided. Therefore, many circuit techniques, such as cascode output and output source follower, are not generally applicable to power amplifier circuits. Instead, impedance matching and the harmonic elimination are achieved by passive components, such as inductors, capacitors, transmission lines [1] and coaxial lines [2]. A general model for power amplifiers is shown in Figure 29.1.

The transistor is connected in a common-source configuration. The load resistor at the drain of the transistor in ordinary common-source amplifiers is replaced by a large inductor, L_1 which is called the Radio Frequency Choke (RFC) or "Big Fat" inductor (BFL). The inductance of L_1 should be large enough to maintain an almost constant current following through it. In other words, the impedance of the inductor should be substantially high for AC signals and is negligible for DC signals so that it provides DC bias with very high AC impedance. A filtering and matching network is required to reduce harmonics due to large-signal operation of the transistor and deliver sufficient power to the load. Depending on the conduction angles and the load networks, power amplifiers can be categorized under many classes: Class A, Class B, Class AB, Class C, Class D, Class E and Class F [3,4]. In Section 29.2, different classes of power amplifiers are briefly described and compared in terms of normalized power capability and efficiency. Among different classes of power amplifiers,

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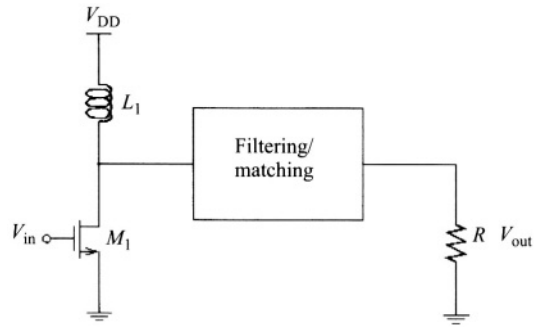


Figure 29.1. General power amplifier model.

Class E power amplifiers provide 100% ideal efficiency with minimization of transitions power loss and are suitable for linearization with envelope elimination and restoration (EER) techniques [5]. Therefore, special emphasis is paid on the Class E power amplifier in the later part of this chapter.

Since the Class E tuned power amplifier was introduced by Sokals [6], many papers on highly efficient Class E power amplifiers have been published [7–14]. Analyses have focused on variations of circuit components [8], operating duty cycle [9] as well as power efficiency [10, 11]. The power efficiency of this switch-mode power amplifier is theoretically 100%. Thus, if one assumes that the switching device is ideal [7] then the losses in the amplifier are theoretically zero. Kazimierczuk discussed the effects of the collector current fall time on power efficiency assuming the current is linear and decays after the transistor is switched off [10]. Blanchard and Yuan extend the analysis by assuming the current is an exponential decay during the fall time [11]. All of these papers are based on the assumption ‘ Q-factor of the output resonant tank is infinite. However, the Q-factor of the passive inductors becomes more critical for the circuits operating at giga-hertz frequencies. This is not only true for the large size passive inductors but also for inductors implemented on silicon substrates where large resistive and capacitive parasitics reduce the inductor Q-factor. In Section 29.3, the trade-off between harmonic distortion introduced by the loaded quality factor and the power efficiency of the amplifiers is presented. The power efficiency of Class E power amplifiers are given. Comparisons are made between the drain current exponential decay model employed in the analysis and circuit simulation using HSPICE.

Also, in the literature, most of the papers are based on the assumption that the shunt capacitance is linear. The shunt capacitor C_1 in a Class E power amplifier is the capacitor connected across the drain and the source of the switching transistor. From classical Class E theory, the required shunt capacitance is

inversely proportional to the operating frequency [7]. At radio frequency in the giga-hertz band, the required value may be comparable to the nonlinear parasitic capacitance of the switching transistor M_1 at the drain terminal. The effect of this nonlinear drain capacitance cannot be neglected. Analysis of the Class E amplifier with nonlinear shunt capacitance was presented by Chudobiak [15]. Recently, a theory based on numerical methods for hyper-abrupt junctions with a grading coefficient $M_j = 0.5$, 0.67 and 0.75 was presented by Alinikula [16]. In Section 29.4, a new approach for finding the optimal zero-bias capacitance of the nonlinear drain-bulk capacitor with a hyper-abrupt junction with a grading coefficient $M_j = n/(n + 1)$ where $n = 1, 2, \ldots, 8, 9$ for a tuned operation of Class E amplifiers is presented. The approach is also generalized for any nonlinear drain-bulk capacitor. It is interesting that the nonlinearity of the shunt capacitance indeed enhances the Class E characteristics at the expense of higher device stress. The use of a small auxiliary linear shunt capacitor to compensate the nonlinearity of the output drain capacitance is suggested. The AM-to-PM distortion during the linearization of a Class E power amplifier with the EER technique can be minimized by this small auxiliary linear shunt capacitor. In addition, the trade-off between operating frequency and device stress with compensation of the nonlinear shunt capacitance by means of an auxiliary shunt capacitor is discussed.

29.2. Classification of Power Amplifiers

In this section, different classes of power amplifiers are briefly described. The performance of those classes of power amplifiers is compared in terms of normalized power capability and efficiency. There are two mains groups of power amplifiers: (1) current-source amplifiers with the transistor acting as a current source, and (2) switch-mode amplifiers with the transistor acting as a switch [6].

29.2.1. Current-Source Power Amplifiers

In Class A, Class AB, Class B and Class C power amplifiers, the input transistor, M_1 acts as a current source. The operation of these power amplifiers is similar to the conventional common-emitter/common-source amplifiers. The classification of these power amplifiers depends on the conduction angle Φ, which represents the duration of conduction of the transistor per one period. For example, conduction angle = 360° means the transistor conducts all the time and conduction angle = 180° means the transistor conducts for half of the period. Table 29.1 shows a classification of these amplifiers.

The transistor operates in its active region of operation when it conducts current. That is, the drain/collector voltage of the transistor has to be higher than a certain value in order for the device to operate in its active region. Power

Table 29.1. Classification of current-source power amplifiers.

Class	*Conduction angle*
A	360°
AB	Between 180° and 360°
B	180°
C	Between 0° and 180°

loss in the transistor is inevitable when the transistor conducts current. Thus, very high power efficiency with a reasonable amount of output power cannot be obtained with these amplifiers [4].

To compare different power amplifier designs in terms of device stress and output power, the normalized power capability is defined as the ratio of the maximum output power to the product of the maximum transistor voltage and the maximum transistor current:

$$P_N = \frac{P_{o,max}}{v_{D,max} i_{D,max}} \tag{29.1}$$

where $P_{o,max}$ is the maximum output power, $v_{D,max}$ is the maximum drain voltage and $i_{D,max}$ is the drain current.

The higher the normalized power capability is, the smaller the stress is on the device for the same maximum output power. $P_N = 0$ means either the transistor voltage or the current is infinite for nonzero output power.

For a current-source power amplifier, the maximum amplitude of the signal across the load is the supply voltage and therefore the maximum output power is equal to [4]:

$$P_{o,max} = \frac{V_{DD}^2}{2R} \tag{29.2}$$

The DC voltage across the RF choke is zero. Therefore, the average drain voltage of the transistor must be equal to the supply voltage. Corresponding to the maximum output amplitude, the maximum drain-source voltage is equal to:

$$v_{D,max} = 2V_{DD} \tag{29.3}$$

The maximum drain current is given by [4]:

$$i_{D,max} = \frac{2\pi V_{DD}}{R(\Phi - \sin\Phi)} \left[1 + \frac{\sin(\Phi/2) - (\Phi/2)\cos(\Phi/2)}{\pi}\right] \tag{29.4}$$

Substitute equations (29.2), (29.3) and (29.4) into equation (29.1):

$$P_N(\Phi) = \frac{\Phi - \sin\Phi}{8\,(\pi + \sin(\Phi/2) - (\Phi/2)\cos(\Phi/2))} \tag{29.5}$$

The ideal efficiency of a current-source power amplifier is [17]:

$$\eta(\Phi) = \frac{1}{4}\frac{\Phi - \sin\Phi}{\sin(\Phi/2) - (\Phi/2)\cos(\Phi/2)} \tag{29.6}$$

Figures 29.2 and 29.3 show the trade-off between the normalized power capability and the ideal efficiency. The Class C amplifier, $0° \leq \Phi < 180°$,

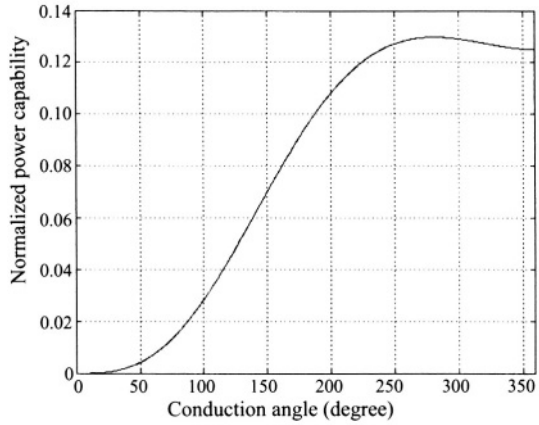


Figure 29.2. Variation of normalized power capability with conduction angle.

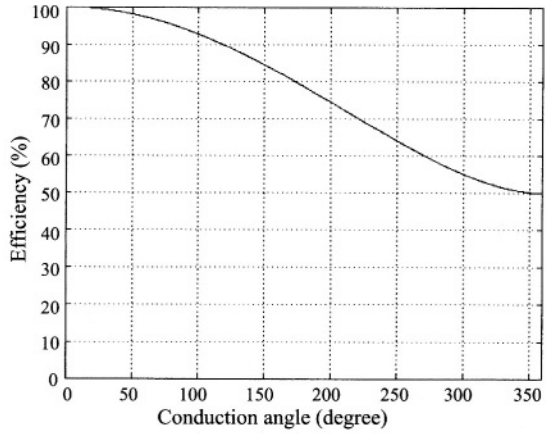


Figure 29.3. Ideal efficiency vs conduction angle.

has the highest ideal efficiency among other classes of current-source power amplifier. The high ideal efficiency of the Class C power amplifier comes at the expense of low normalized power capability. In the extreme case, 100% ideal efficiency can be achieved by the Class C power amplifier with zero normalized power capability at $\Phi = 0$. The Class AB amplifier, $180° < \Phi < 360°$, also has the maximum normalized power capability of 0.1298 at $\Phi = 281.12°$ with 58.18% ideal efficiency. Note that the ideal efficiency is the maximum achievable efficiency. Practically, power losses in the non-ideal components have to be accounted for. Therefore, different topologies of power amplifiers with high ideal efficiency and acceptable normalized power capability are preferable.

29.2.2. Switch-Mode Power Amplifiers

In Class D, Class E and Class F amplifiers, the transistor acts as a switch. When an ideal switch is ON, the voltage across the switch is zero. On the other hand, when the switch is OFF, the current through the switch is zero. Therefore, there is no simultaneous nonzero voltage and nonzero current at any time. Therefore, there is no power loss in the ideal switching transistor. Theoretically, 100% power efficiency with a reasonable amount of output power can be obtained with these amplifiers.

The switch current and voltage are independent of the input drive. Instead, the switch current and voltage are controlled by the response of the load network. Therefore, the output does not depend on the envelope variation of the input drive provided that the input drive is high enough for the switch-mode operation of the transistor. Therefore, the switch-mode amplifiers are called constant-envelope amplifiers.

Class D power amplifier. A Class D power amplifier circuit is shown in Figure 29.4. The circuit is similar to a push-pull Class B amplifier. The transistors, M_1 and M_2 conduct alternatively for 180°.

The difference between this Class D amplifier and a push-pull Class B is that the transistors act as switches. The switches short alternatively the input terminals transformer T1 to the ground. Theoretically, the drain voltage of the transistors is a square-wave with amplitude of V_{DD} and DC component of V_{DD}. The resonator, which is formed by C_2 and L_2, is tuned to the fundamental frequency of the square-wave. Only a sinusoidal current at the fundamental frequency will thus flow through the load and the secondary coil. The primary current is a sinusoidal current at the fundamental frequency of the square-wave. Therefore, the drain current of each transistor contains half of the sinusoidal primary current when they are turned on.

Theoretically, a push–pull Class D power amplifier can achieve 100% ideal efficiency with very high normalized power capability of 0.318 [7]. Note that the normalized power capability of a single-transistor Class D power amplifier is only 0.159. As with CMOS logic gates, there is substantial power loss during on/off transitions of the transistors. In addition, the transformers dissipate a substantial amount of power and usually have to be implemented as discrete components. Therefore, Class D power amplifiers are generally not suitable for radio frequency mobile applications.

Class E power amplifier. The main shortcoming of the Class D power amplifier is the power loss during on/off transitions. The drain voltage and the drain current of the transistor in switch-mode amplifiers are determined by the transient response of the load output network. It is possible to assemble a load output network such that the power loss during on/off transitions is minimized.

A Class E power amplifier is shown in Figure 29.5. L_1 is a radio frequency choke, which provides a DC path to the supply voltage. When the switch is on,

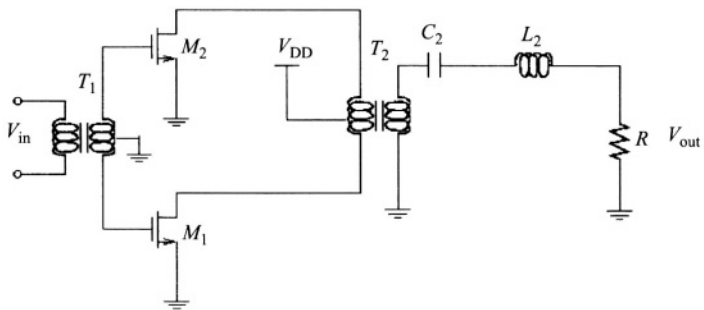


Figure 29.4. Class D power amplifier model.

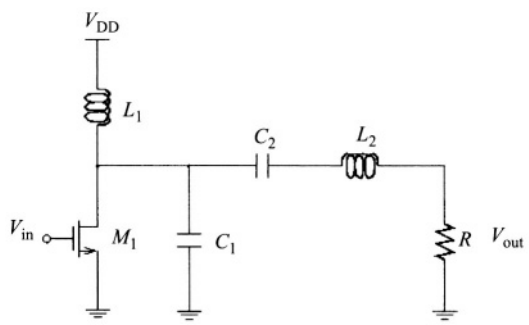


Figure 29.5. Class E power amplifier model.

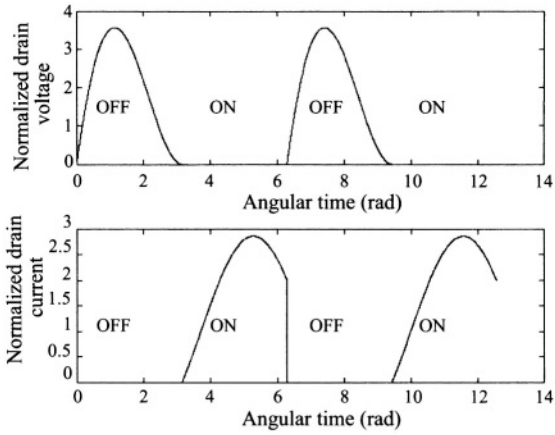


Figure 29.6. Typical waveforms of a Class E power amplifier.

the voltage across the shunt capacitor, C_1, is small. At switch turnoff, time is required to charge up this capacitor. Therefore, C_1 delays the increase of the drain voltage at switch turnoff. C_2 and L_2 form a resonator nearly tuned to the operating frequency with a residual reactance. When the switch is off, the DC current from L_1 and the sinusoid output current from the LC resonator charge up and then discharge the shunt capacitor, C_1. With appropriate component values, the drain voltage rises to a maximum and then decreases to zero with a zero slope.

The waveforms of the normalized drain voltage v_D/V_{DD} and the normalized drain-to-source current i_D/I_{DD} of an ideal Class E power amplifier are shown in Figure 29.6. The power loss during on/off transitions is minimized by shaping the drain voltage such that its value is small just after turn-off and before turn-on. The minimization of transitions power loss comes at the expense of large drain voltage in the middle of the turn-off interval. Thus, the transistor suffers higher stress than that in a Class D power amplifier. The normalized power capability of a Class E power amplifier is 0.0981 [7].

Class F power amplifier. The power loss at on/off transitions can also be minimized when the transitions are sharp enough. The closer the drain voltage waveform to a square wave, the sharper the transitions are. A square wave with 50% duty cycle contains only odd harmonics. Therefore, the drain voltage waveform can be shaped close to a square wave by eliminating even harmonics and enhancing odd harmonics.

By creating an open circuit for all odd harmonics and a short circuit for all even harmonics at the drain of the transistor, 100% ideal efficiency can be

obtained by a Class F power. The required frequency characteristics can be obtained by using a quarter-wavelength transmission line in the output load network. The main drawback with this implementation is that the required transmission line occupies substantial space. Alternatively, a lump circuit element implementation of a Class F power amplifier can be used to provide the desired frequency characteristics at finite number of harmonics.

A typical Class F power amplifier with lump circuit elements is shown in Figure 29.7. L_1 is a radio frequency choke, which provides a DC path to the supply. C_1 prevents DC dissipation in the load. All even harmonics are shorted to ground by the resonators. The load networks provide very high impedance for the third and fifth harmonics. Only the signal with fundamental frequency reaches the load. Since the circuit does not provides an open circuit for all odd harmonic, the voltage waveform at the output of the transistor is not perfectly square-wave. Therefore, the ideal efficiency for a Class F power amplifier with lump circuit elements is lower than 100%. The performance of Class F power amplifiers with different output networks is shown in Table 29.2.

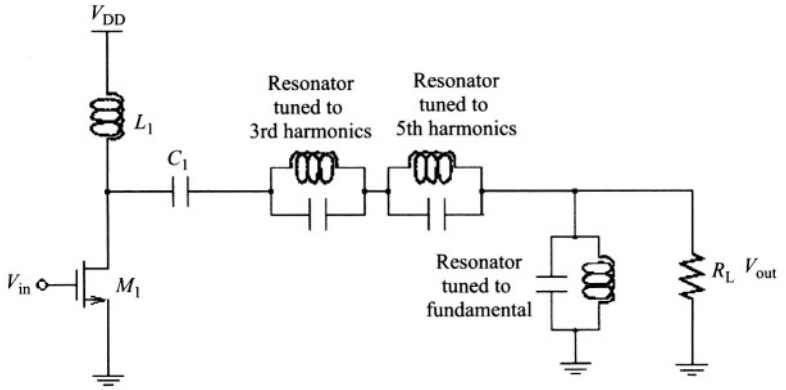


Figure 29.7. Class F power amplifier model [4].

Table 29.2. Performance of Class F PA's for various combinations of harmonics [18].

	Fundamental (Class B)	*Fundamental and 3rd harmonic*	*Fundamental 3rd and 5th harmonics*	*All odd harmonics (Class D)*
Ideal efficiency (%)	78.5	88.4	92	100
Normalized power capability	0.125	0.141	0.146	0.159

The ideal efficiency and normalized power capability of Class F power amplifiers improve with increasing number of odd harmonics included. In contrast to current-source power amplifiers, there is no trade-off between the ideal efficiency and the normalized power capability for Class F power amplifiers. For Class F power amplifiers with lump circuit elements, more passive components are required to provide high impedance at more number of odd harmonics. Therefore, the increase in ideal performance comes at the expense of higher power loss from the passive components and larger space occupied.

29.2.3. Bandwidth Efficiency, Power Efficiency and Linearity

Although switch-mode power amplifiers have superior power efficiency performance over current-source amplifiers, they are nonlinear amplifiers. With a sufficient input drive, the transistor acts as a switch. The voltage across and the current through a switch are not controlled by the input drive but controlled by the transient response of the load network. The amplitude of the output of switch-mode power amplifier is not controlled by the input drive. Therefore, switch-mode power amplifiers are also called constant-envelope amplifiers. Linear amplification of signal cannot normally be obtained with these amplifiers. A RF signal with a constant envelope and smooth phase transitions can be amplified with these highly efficient nonlinear power amplifiers. Switch-mode power amplifiers are used in GSM (Global System for Mobile communication) and DECT (Digital European Cordless Telephone) systems in which constant-envelope modulation schemes with smooth phase transitions such as GMSK (Gaussian Minimum Shift Keying) and GFSK (Gaussian Frequency Shift Keying) are employed [3].

Typically, constant-envelope modulation schemes with smooth phase transitions need wider bandwidth than those with abrupt phase transitions. Bandwidth efficient modulation schemes such as $(\pi/4)$-DQPSK (Differential Quadrature Phase Shift Keying) and OQPSK (Offset Quadrature Phase Shift Keying) in NADS (North American Digital Standard) and Qualcomm CDMA (Code-Division Multiple Access) systems requires linear power amplifiers to avoid spectral regrowth [3].

To achieve both high power efficiency and high bandwidth efficiency, linearization techniques are used to linearize power amplifiers with high power efficiency. Linearization techniques for current-source power amplifiers include feedforward [19], Cartesian feedback [20], digital pre-distortion [21], pre-distortion with cubic spline interpolation [22] and Bi-directional Control feedback [23]. Basically, these linearization techniques adjust the input drive to obtain a linear output, and therefore, they are not suitable for switch-mode power amplifiers when the output amplitude is independent of the input drive.

EER [5] techniques can be applied to linearize constant-envelope amplifiers. In an EER system, a RF signal is divided into phase and envelope components with an amplitude limiter and an envelope detector respectively. The envelope component is used to modulate the supply voltage of the power amplifier while the phase component is used to drive the switch-mode transistor at the input.

EER technique was employed to linearize Class C amplifiers [24]. Since the output of Class C and Class F amplifiers is not directly proportional to the supply voltage [25], a feedback network from the output to the supply is required. The application of EER on Class E amplifiers does not require such feedback loop [26] because the output voltage of a tuned Class E power amplifier varies linearly with the supply voltage [7,27]. However, in Class E amplifiers the large variation in the supply voltage changes the phase of the output. This AM-to-PM distortion can be minimized with a phase correcting feedback network [28]. A simple alternative to minimize the AM-to-PM distortion is presented in Section 29.4.2.

29.3. Effect of Loaded *Q*-Factor on Class E Power Amplifiers

In this section, the trade-off between harmonic distortion introduced by the loaded quality factor and the power efficiency of the amplifiers is presented. The power efficiency of Class E power amplifiers are given. Comparisons are made between the drain current exponential decay model employed in the analysis and circuit simulation using HSPICE.

29.3.1. Circuit Analysis

The basic circuit of the Class E power amplifier is shown in Figure 29.8. For simplification, we assume that

(a) The inductance of RF choke is high enough that the current that flows through it can be regarded as dc current.

(b) The output capacitance of the active device is independent of the switching voltage.

(c) The active device is an ideal switch with zero on resistance and zero switching time.

(d) The active device is closed for $0 < \theta \leq \pi$, and open for $\pi < \theta \leq 2\pi$.

The loaded Q-factor at the operating frequency f can be defined as [6]

$$Q_L = \frac{\omega L_2}{R} \tag{29.7}$$

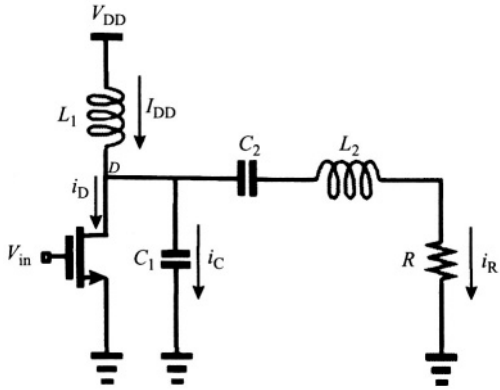


Figure 29.8. Basic circuit of Class E power amplifier.

For a series resonant circuit, the load current $i_R(\theta)$ including harmonic components can be represented as [29]

$$i_R(\theta) = \sum_{n=1}^{\infty} C_n I_{R1} \sin(n\theta + \phi_n) \tag{29.8}$$

where

$$C_n = \frac{1}{\left[1 + Q_L^2(n - 1/n)^2\right]^{1/2}}, \quad \phi_n = \phi_1 - \tan^{-1}\left[Q_L(n - 1/n)\right]$$

I_{R1} and ϕ_1 are the amplitude and the initial phase of $i_R(\theta)$ in the operating frequency, respectively. The subscript n refers to the nth harmonic component. Notice that the input voltage signal of the load network can be any waveform whereas our assumption in the analysis is the case of equal-magnitude signal for each harmonic.

By applying Kirchhoff's current law to the circuit in Figure 29.8, the ac current equation at node D can be written as

$$I_{DD} - i_R(\theta) = i_D(\theta) + i_C(\theta) \tag{29.9}$$

Since the MOSFET is conducting in the time period $0 < \theta \leq \pi$, the drain–source voltage is zero in this period

$$v_D(\theta) = 0 \quad \text{for } 0 < \theta \leq \pi \tag{29.10}$$

The ac current $i_C(\theta)$ is

$$i_C(\theta) = 0 \quad \text{for } 0 < \theta \leq \pi \tag{29.11}$$

From equations (29.8), (29.9) and (29.11) the drain current in the period is given as

$$i_D(\theta) = I_{DD} - \sum_{n=1}^{\infty} C_n I_{R1} \sin(n\theta + \phi_n) \quad \text{for } 0 < \theta \leq \pi \tag{29.12}$$

For the time period $\pi < \theta \leq \pi + \theta_f$, the drain current can be described as

$$i_D(\theta) = i_D(\pi) \exp\left[-\frac{\theta - \pi}{\tau}\right] \quad \text{for } \pi < \theta \leq \pi + \theta_f \tag{29.13}$$

where θ_f is the fall time of drain current [11] and

$$i_D(\pi) = I_{DD} - \sum_{n=1}^{\infty} C_n I_{R1} \sin(n\pi + \phi_n) \tag{29.14}$$

where τ is the decay lifetime.

Substituting equations (29.8), (29.13) and (29.14) into (29.9), the current $i_C(\theta)$ during the fall time is

$$\begin{aligned} i_C(\theta) = {} & I_{DD} - \sum_{n=1}^{\infty} C_n I_{R1} \sin(n\theta + \phi_n) \\ & - \left[I_{DD} - \sum_{n=1}^{\infty} C_n I_{R1} \sin(n\pi + \phi_n) \right] \exp\left[-\frac{\theta - \pi}{\tau}\right] \end{aligned} \tag{29.15}$$

for $\pi < \theta \leq \pi + \theta_f$. Thus the drain–source voltage during this period is

$$\begin{aligned} v_D(\theta) &= \frac{1}{\omega C_1} \int_{\pi}^{\theta} i_C(\theta)\, d\theta \\ &= \frac{1}{\omega C_1} \left\{ I_{DD} \left[\theta - \pi + \tau \left(\exp\left(-\frac{\theta - \pi}{\tau} \right) - 1 \right) \right] \right. \\ &\quad + \sum_{n=1}^{\infty} C_n I_{R1} \left[\frac{1}{n} \left(\cos(n\theta + \phi_n) - \cos(n\pi + \phi_n) \right) \right. \\ &\quad \left. \left. - \tau \sin(n\pi + \phi_n) \left(\exp\left(-\frac{\theta - \pi}{\tau} \right) - 1 \right) \right] \right\} \end{aligned} \tag{29.16}$$

for $\pi < \theta \leq \pi + \theta_f$.

For the time period $\pi + \theta_f < \theta \leq 2\pi$, the MOSFET turns off and the drain current approaches zero, thus the capacitive current is

$$i_C(\theta) = I_{DD} - \sum_{n=1}^{\infty} C_n I_{R1} \sin(n\theta + \phi_n) \quad \text{for } \pi + \theta_f < \theta \leq 2\pi \tag{29.17}$$

and the drain–source voltage is

$$\begin{aligned} v_D(\theta) &= \frac{1}{\omega C_1} \int_{\pi+\theta_f}^{\theta} i_C(\theta')\, d\theta' + v_{DS}(\pi + \theta_f) \\ &= \frac{1}{\omega C_1} \left\{ I_{DD} \left[\theta - \pi + \tau \left(\exp\left(-\frac{\theta_f}{\tau} \right) - 1 \right) \right] \right. \\ &\quad + \sum_{n=1}^{\infty} C_n I_{R1} \left[\frac{1}{n} \left(\cos(n\theta + \phi_n) - \cos(n\pi + \phi_n) \right) \right. \\ &\quad \left. \left. - \tau \sin(n\pi + \phi_n) \left(\exp\left(-\frac{\theta_f}{\tau} \right) - 1 \right) \right] \right\} \end{aligned} \tag{29.18}$$

for $\pi + \theta_f < \theta \leq 2\pi$.

It is well known that for Class E switching conditions the drain voltage as well as its derivative should be zero when the MOSFET turns on [6]. Thus, the boundary conditions are

$$v_D(2\pi) = 0 \tag{29.19}$$

$$\left. \frac{dv_D}{d\theta} \right|_{\theta=2\pi} = 0 \tag{29.20}$$

From equations (29.19) and (29.20), we obtain equations (29.21) and (29.22) respectively.

$$\begin{aligned} I_{DD} \left\{ \pi + \tau \left[\exp\left(-\frac{\theta_f}{\tau} \right) - 1 \right] \right\} &= \sum_{n=1}^{\infty} C_n I_{R1} \left\{ \frac{\cos(n\pi + \phi_n) - \cos\phi_n}{n} \right. \\ &\quad \left. + \tau \left[\exp\left(-\frac{\theta_f}{\tau} \right) - 1 \right] \sin(n\pi + \phi_n) \right\} \end{aligned} \tag{29.21}$$

$$I_{DD} = I_{R1} \sum_{n=1}^{\infty} C_n \sin\phi_n \tag{29.22}$$

thus,

$$\sum_{n=1}^{\infty} C_n \left\{ \left[\pi + \tau \left(\exp\left(-\frac{\theta_f}{\tau} \right) - 1 \right) \right] \sin \phi_n - \left[\frac{\cos(n\pi + \phi_n) - \cos \phi_n}{n} + \tau \left(\exp\left(-\frac{\theta_f}{\tau} \right) - 1 \right) \sin(n\pi + \phi_n) \right] \right\} = 0 \tag{29.23}$$

In equation (29.23), if Q_L, τ, θ_f are known, we can solve ϕ, the output current, drain current, and the current flowing through the shunt capacitor.

29.3.2. Power Efficiency

Typically, power efficiency has two definitions; the power added efficiency (PAE) which defined as

$$\text{PAE} \equiv \frac{\text{output power} - \text{input power}}{\text{supply power}}$$

and the power efficiency is simply defined as

$$\text{PE} \equiv \frac{\text{output power}}{\text{supply power}}$$

In this chapter, the power efficiency is referred to the latter definition. From the previous derivation, we can calculate the power efficiency. The supply dc power is

$$P_{dc} = I_{DD} V_{DD} \tag{29.24}$$

and the power consumption for a full cycle of the MOSFET is

$$P_{tf} = \frac{1}{2\pi} \int_0^{2\pi} i_D(\theta) v_D(\theta) \, d\theta \tag{29.25}$$

thus, the power efficiency η is given by

$$\eta = 1 - \frac{P_{tf}}{P_{dc}} = 1 - \frac{1}{2\pi} \int_0^{2\pi} \frac{i_D(\theta)}{I_{DD}} \frac{v_D(\theta)}{V_{DD}} \, d\theta \tag{29.26}$$

Substituting equations (29.13), (29.14) and (29.16) into equation (29.26) yields

$$\eta = 1 - \frac{1}{2\pi}\int_{\pi}^{\pi+\theta_f}\left[1 - \frac{I_{R1}}{I_{DD}}\sum_{n=1}^{\infty} C_n \cos n\pi \sin\phi_n \exp\left(-\frac{\theta-\pi}{\tau}\right)\right] \times \left\{\frac{1}{\Delta}\left[I_{DD}\left(\theta - \pi + \tau\left(\exp\left(-\frac{\theta-\pi}{\tau}\right) - 1\right)\right) + \sum_{n=1}^{\infty} C_n I_{R1}\left[\frac{\cos(n\theta+\phi_n)}{n} - \tau\left(\exp\left(-\frac{\theta-\pi}{\tau}\right) - 1\right) \times \sin(n\pi+\phi_n) - \frac{\cos(n\pi+\phi_n)}{n}\right]\right]\right\} \tag{29.27}$$

where

$$\Delta = \frac{1}{2\pi}\left\{I_{DD}\left[\frac{\pi^2}{2} - \tau\left[\theta_f + (\tau - \pi + \theta_f)\left(\exp\left(-\frac{\theta_f}{\tau}\right) - 1\right)\right]\right] + \sum_{n=1}^{\infty} C_n I_{R1}\left[\frac{\sin\phi_n - \sin(n\pi+\phi_n)}{n^2} - \frac{\pi\cos(n\pi+\phi_n)}{n} + \tau\sin(n\pi+\phi_n)\left[\theta_f + (\tau - \pi + \theta_f)\left(\exp\left(-\frac{\theta_f}{\tau}\right) - 1\right)\right]\right]\right\} \tag{29.28}$$

29.3.3. Circuit Simulation and Discussion

With the assumption of harmonic distortion in the output signal at the operating frequency, we can derive equation (29.23), which can be solved numerically. Furthermore, we can also solve for the power efficiency. Figure 29.9 shows the drain–source voltage waveform normalized to V_{DD} vs time for different loaded Q-factor (Q_L) at $\theta_f = \pi/6$. For a higher Q_L, the voltage is shifted to higher degrees. It is seen that the normalized voltage decreases with Q_L. The drain-source voltage waveform at $\theta_f = \pi/2$ is shown in Figure 29.10. For $Q_L = 5$ or 6, the normalized voltages are much lower than the case at $\theta_f = \pi/2$. Figure 29.11 shows the drain current waveform at $\theta_f = \pi/6$. For a higher Q_L, the normalized current is shifted to higher degrees. For the case $Q_L = 2$, the waveform has the shortest decay angle which means the cross-section part of drain current and drain–source voltage is smaller than for higher Q_L.

Figure 29.12 shows the normalized drain current at $\theta_f = \pi/2$. Compared to the case at $\theta_f = \pi/6$, the drain current has a longer decay. To validate the

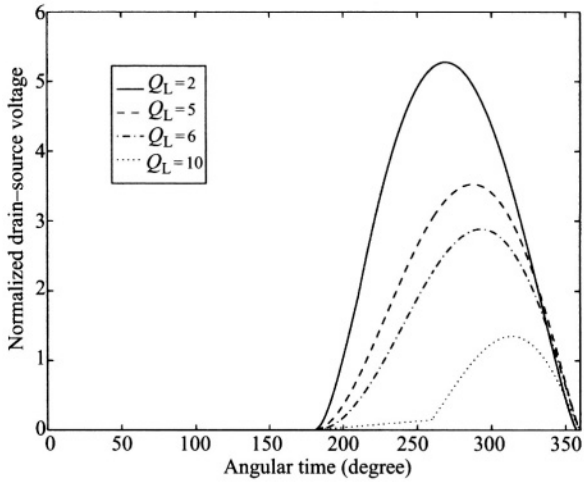


Figure 29.9. Normalized drain–source voltage waveform vs time (fall time angle = $\pi/6$).

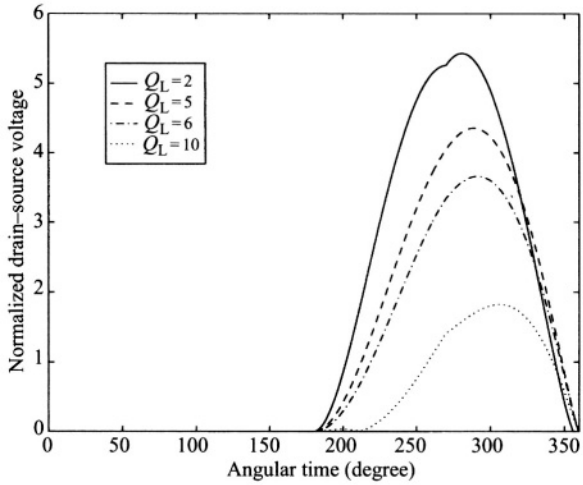


Figure 29.10. Normalized drain–source voltage waveform vs time (fall time angle = $\pi/2$).

analysis, HSPICE circuit simulation for 1.8 GHz operation has been performed. The circuit configuration for simulation is shown in Figure 29.13.

Notice that since the RF choke current, $i_L(\theta)$ is independent of the loaded quality factor, here we can use lower inductance for the RF choke and the current flowing through it at the beginning of the drain current decay is $i_L(\theta)|_{\theta=\pi} = V_{DD}/L_1(\pi/\omega)$ + Const instead of I_{DD}. Moreover, in order to compare the performance influenced by the decay angle of the transistor, we

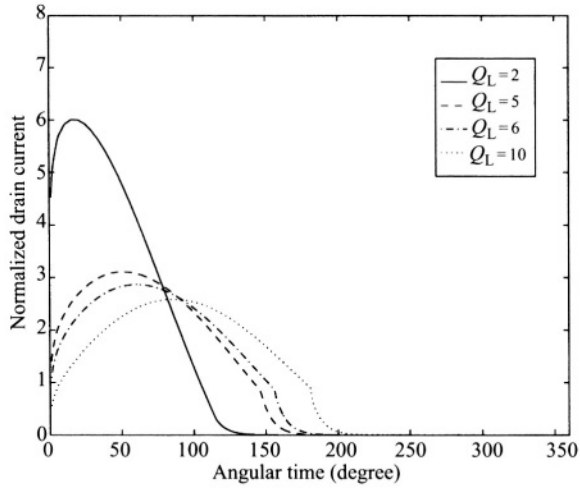


Figure 29.11. Normalized drain current waveform vs time (fall time angle $= \pi/6$).

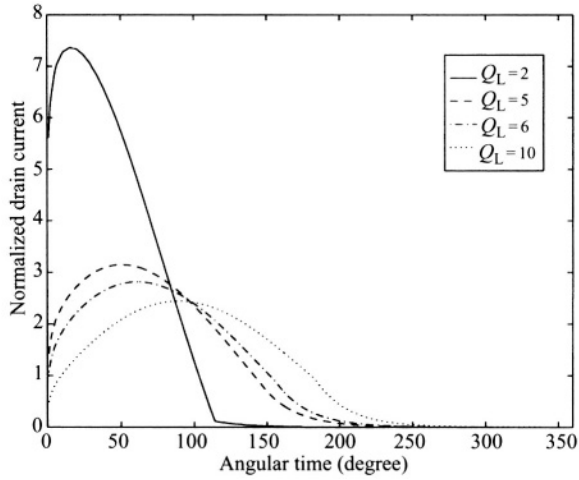


Figure 29.12. Normalized drain current waveform vs time (fall time angle $= \pi/2$).

use two models, one is a commercial 0.8-μm CMOS technology, the other is a commercial 0.6-μm CMOS technology and the simulation results are shown in Figure 29.14. The power efficiency decreases with an increase of Q_L. For the 0.6-μm model, since it has lower decay angle, higher power efficiency can be expected. Comparing the results to the 0.8-μm model, it shows much slower decrease with an increase of Q_L. Figure 29.15 shows a comparison

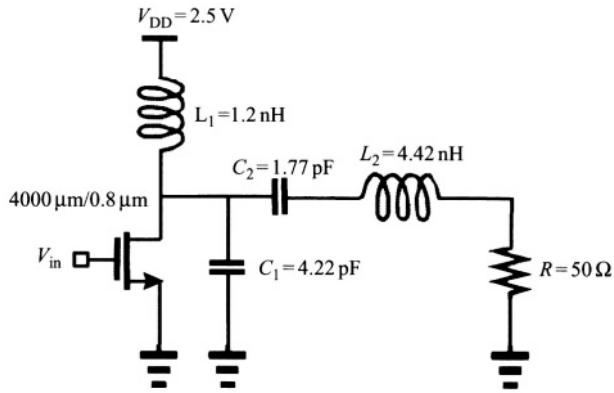


Figure 29.13. Schematic of Class E power amplifier for circuit simulation.

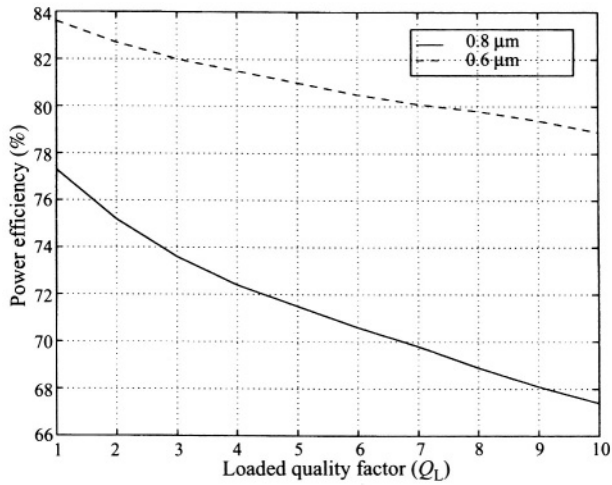


Figure 29.14. Power efficiency vs Q_L for two different feature size models.

between the theoretical results and HSPICE circuit simulation results, close agreement has been obtained. The total harmonic distortion analysis is also given in Figure 29.16, serious distortion can be seen for low Q_L as predicted.

29.4. Class E Power Amplifiers with Nonlinear Shunt Capacitance

In this section, a new approach for finding the optimal zero-bias capacitance of the nonlinear drain-bulk capacitor with a hyper-abrupt junction for any

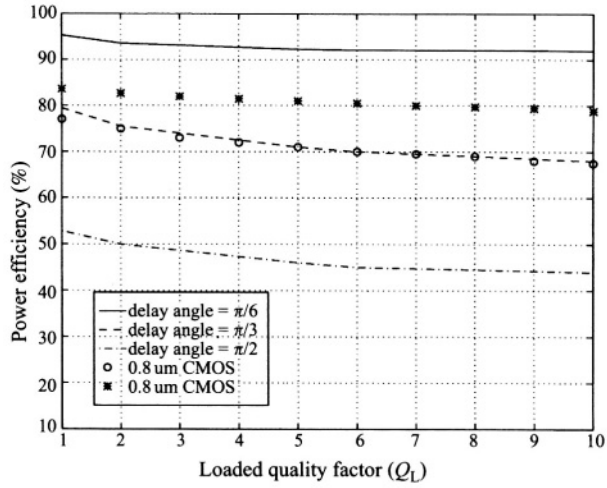


Figure 29.15. Power efficiency vs Q_L for the comparison between the theoretical and HSPICE model.

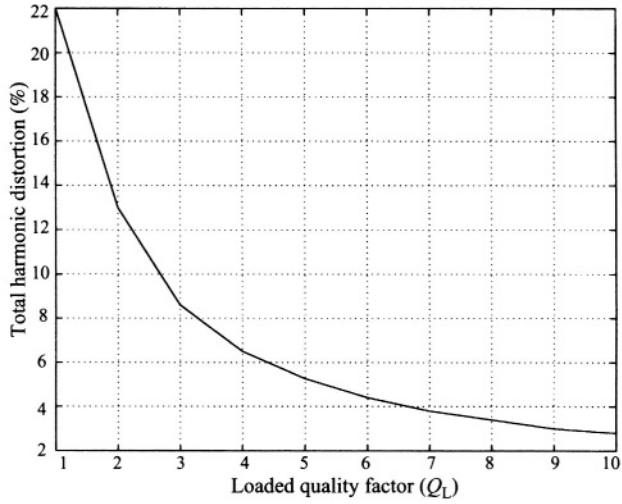


Figure 29.16. Total harmonic distortion vs loaded quality factor.

nonlinear drain-bulk capacitor is presented. The use of a small auxiliary linear shunt capacitor to compensate the nonlinearity of the output drain capacitance is suggested. The AM-to-PM distortion during the linearization of Class E power amplifier with the EER technique can be minimized by this small auxiliary linear shunt capacitor. In addition, the trade-off between operating frequency and device stress is also discussed.

29.4.1. Numerical Computation of Optimum Component Values

The ideal Class E power amplifier circuit is shown in Figure 29.17. The assumptions made in this analysis are

1 The transistor acts as an ideal switch.

2 The inductance of the radio frequency choke, L_1, is infinite.

3 The quality factor, Q_L, of the resonant tank formed by C_2' and L_2' is infinite.

4 All passive components except C_1 are linear.

5 The shunt capacitor C_1 is a hyper-abrupt junction capacitor.

6 The switching duty cycle is 50%.

Basic equations. The expressions for the output voltage v_R, the output current i_R, the fundamental voltage v_1 and the charging current i_C are the same as those for the case of a linear shunt capacitor [7]. Since only pure sinusoid current at operating frequency, ω, can pass through the resonant tank with infinite Q_L, the output voltage and current are sinusoidal:

$$v_R(\theta) = c \sin(\theta + \phi) \tag{29.29}$$

$$i_R(\theta) = \frac{c}{R} \sin(\theta + \phi) \tag{29.30}$$

where $\theta = \omega t$ is the angular time; ϕ is the phase shift with respect to the input and c is the amplitude of the output voltage.

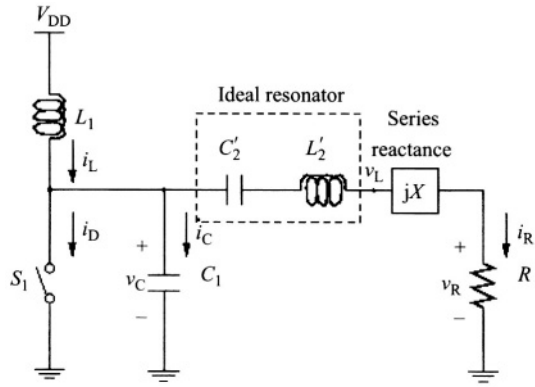


Figure 29.17. Ideal Class E power amplifier model.

The series reactance, jX, introduces a phase difference between the output voltage and the fundamental component of the drain voltage. The voltage at the output of the ideal resonator is given by:

$$v_1(\theta) = c_1 \sin(\theta + \phi_1) \tag{29.31}$$

$$c_1 = c\sqrt{1 + \frac{X^2}{R^2}} = \rho c \tag{29.32}$$

$$\phi_1 = \phi + \tan^{-1}\left(\frac{X}{R}\right) = \phi + \psi \tag{29.33}$$

If the inductance of L_1 is infinite, only constant DC current can flow through it. Therefore, i_L in Figure 29.17 can be denoted by I_{DD}. Applying KCL at the drain of the transistor,

$$i_C + i_D = i_L - i_R \tag{29.34}$$

$$i_C(\theta) + i_D(\theta) = I_{DD} - \frac{c}{R}\sin(\theta + \phi) \tag{29.35}$$

When the switch is open, $0 < \theta < \pi$

$$i_D(\theta) = 0 \tag{29.36}$$

$$i_C(\theta) = I_{DD} - \frac{c}{R}\sin(\theta + \phi) \tag{29.37}$$

The drain-to-bulk capacitor can be modeled as a reverse-biased hyper-abrupt PN junction capacitor:

$$C_{db}(v_C) = C_{j0}\left(1 + \frac{v_C}{V_{bi}}\right)^{-n/(n+1)} \tag{29.38}$$

$$C_{db}(v_C) = C_{j0}\left(1 + \frac{v_C}{V_{bi}}\right)^{-M_j} \tag{29.39}$$

where v_C is the voltage across the capacitor; $M_j = n/(n+1)$ is the grading coefficient; C_{j0} is the zero-bias capacitance; n is an integer and V_{bi} is the junction built-in voltage. M_j, C_{j0}, n and V_{bi} are process dependent.

The charging current i_C is given by

$$i_C = \omega C_1(v_C)\frac{dv_C}{d\theta} \tag{29.40}$$

Let the shunt capacitance $C_1(v_C)$ be equal to the drain-to-bulk capacitor $C_{db}(v_C)$. Substitute equations (29.37) and (29.39) into equation (29.40) and

integrate both sides,

$$\frac{1}{\omega}\int_0^{\theta}\left[I_{DD}-\frac{c}{R}\sin(\varphi+\phi)\right]d\varphi=\int_0^{v_C}\left[C_{j0}\left(1+\frac{v}{V_{bi}}\right)^{-n/(n+1)}\right]dv \tag{29.41}$$

$$\frac{I_{DD}\theta+c/R\left[\cos(\theta+\phi)-\cos(\phi)\right]}{\omega}=V_{bi}C_{j0}(n+1)\left[\left(1+\frac{v_C}{V_{bi}}\right)^{1/(n+1)}-1\right] \tag{29.42}$$

Optimum operation (*Alinikula's method [16]*). Equation (29.42) is used to solve for the capacitor voltage v_C:

$$v_C(\theta)=V_{bi}\left\{\left[\frac{I_{DD}\theta+c/R\left[\cos(\theta+\phi)-\cos(\phi)\right]}{\omega C_{j0}V_{bi}(n+1)}+1\right]^{n+1}-1\right\} \tag{29.43}$$

By applying the Class E conditions $i_C(\pi)=0$ and $v_C(\pi)=0$,

$$\sin(\phi)=-\frac{I_{DD}R}{c} \tag{29.44}$$

$$\cos(\phi)=\frac{\pi I_{DD}R}{2c} \tag{29.45}$$

$$\tan(\phi)=-\frac{2}{\pi} \tag{29.46}$$

$$\sin(\phi)=-\frac{1}{\sqrt{1+\pi^2/4}} \tag{29.47}$$

$$\frac{c}{I_{DD}R}=\sqrt{1+\frac{\pi^2}{4}} \tag{29.48}$$

For 100% efficiency, the output power is equal to the input power.

$$P_o=P_i \tag{29.49}$$

$$\frac{c^2}{2R}=V_{DD}I_{DD} \tag{29.50}$$

$$\frac{1}{2}\left(\frac{c}{I_{DD}R}\right)^2RI_{DD}=V_{DD} \tag{29.51}$$

Substitute equation (29.48) and solve for I_{DD},

$$I_{DD} = \frac{2V_{DD}}{\left(1 + \pi^2/4\right) R} \tag{29.52}$$

The value of R is determined by the output power and the supply voltage. For 100% efficiency,

$$P_o = I_{DD} V_{DD} \tag{29.53}$$

$$P_o = \frac{2V_{DD}^2}{\left(1 + \pi^2/4\right) R} \tag{29.54}$$

$$R = \frac{2V_{DD}^2}{\left(1 + \pi^2/4\right) P_o} \tag{29.55}$$

Equation (29.46) shows that the phase shift ϕ is unaffected by the nonlinearity of the parasitic shunt capacitance as long as the Class E operation is maintained. Substitute equations (29.44), (29.45) and (29.52) into equation (29.43),

$$v_C(\theta) = V_{bi} \left\{ \left[\frac{2V_{DD}\left(\theta + \pi/2 \cos(\theta) + \sin(\theta) - \pi/2\right)}{\left(1 + \pi^2/4\right) \omega R C_{j0} V_{bi} (n+1)} + 1 \right]^{n+1} - 1 \right\} \tag{29.56}$$

The DC voltage across an infinite inductor L_1 must be zero. Therefore,

$$V_{DD} = \frac{1}{2\pi} \int_0^{\pi} v_C(\theta)\, d\theta \tag{29.57}$$

The result of the integration is a $(n + 1)$th order nonlinear equation for unknown C_{j0}.Numerical methods are applied to integrate equation (29.57) and solve the resulting $(n + 1)$th order equation for unknown C_{j0} [16]. Solutions for $n = 1, 2, 3$ can be obtained by this method. The higher value *of n,* the higher the order of the equation. The resulting equation becomes too complicated to be calculated by numerical means for $n > 3$.

Physical property approach. In this section, the derivation of a solution is based on observation of the physical property of capacitors. Equation (29.42) can be written as:

$$Q_i(\theta) = Q_v(v_C) \tag{29.58}$$

$$Q_i(\theta) = \frac{I_{DD}\theta + c/R\left[\cos(\theta + \phi) - \cos(\phi)\right]}{\omega} \tag{29.59}$$

$$Q_v(v_C) = V_{bi} C_{j0} (n+1) \left[\left(1 + \frac{v_C}{V_{bi}}\right)^{1/(n+1)} - 1 \right] \tag{29.60}$$

where $Q_i(\theta)$ and $Q_v(v_C)$ are the charges in the capacitor in terms of angular time θ and the capacitor voltage v_C respectively. According to the property of capacitors, $Q_v(v_C) = 0$ if and only if $v_C = 0$. So, the condition, $v_C = 0$ at $\theta = \pi$ can be written as:

$$Q_i(\pi) = Q_v(0) \tag{29.61}$$

$$Q_i(\pi) = 0 \tag{29.62}$$

$$I_{DD}\pi - \frac{2c}{R}\cos(\phi) = 0 \tag{29.63}$$

According to the property of capacitors, the rate of change of the voltage across a capacitor is zero if and only if the charging current is zero. So, the condition $dv_C/d\omega = 0$ at $\theta = \pi$ can be written as:

$$i_C(\pi) = 0 \tag{29.64}$$

$$I_{DD} + \frac{c}{R}\sin(\phi) = 0 \tag{29.65}$$

It is interesting to find that the equations (29.63) and (29.65) for Class E conditions are unaffected by the nonlinearity of the capacitor. Therefore, the phase shift ϕ is unchanged and thus the DC current I_{DD}, the required load R and the output voltage amplitude c are unaffected by the nonlinearity of the capacitor.

$$\phi = \tan^{-1}\left(-\frac{2}{\pi}\right) \tag{29.66}$$

$$I_{DD} = \frac{P_o}{V_{DD}} \tag{29.67}$$

$$R = \frac{2V_{DD}^2}{\left(1 + \pi^2/4\right) P_o} \tag{29.68}$$

$$c = I_{DD}R\sqrt{1 + \frac{\pi^2}{4}} = \frac{2V_{DD}}{\sqrt{1 + \pi^2/4}} \tag{29.69}$$

From equations (29.66)-(29.68) and (29.89), the charges in the drain capacitor

$$Q_i(\theta) = \frac{I_{DD}\theta + c/R[\cos(\theta + \phi) - \cos(\phi)]}{\omega}$$

is also unaffected by the nonlinearity of the drain capacitance and can be computed given P_o, V_{DD}, ω. The stored charge $Q_v(v_C)$ is a monotonically

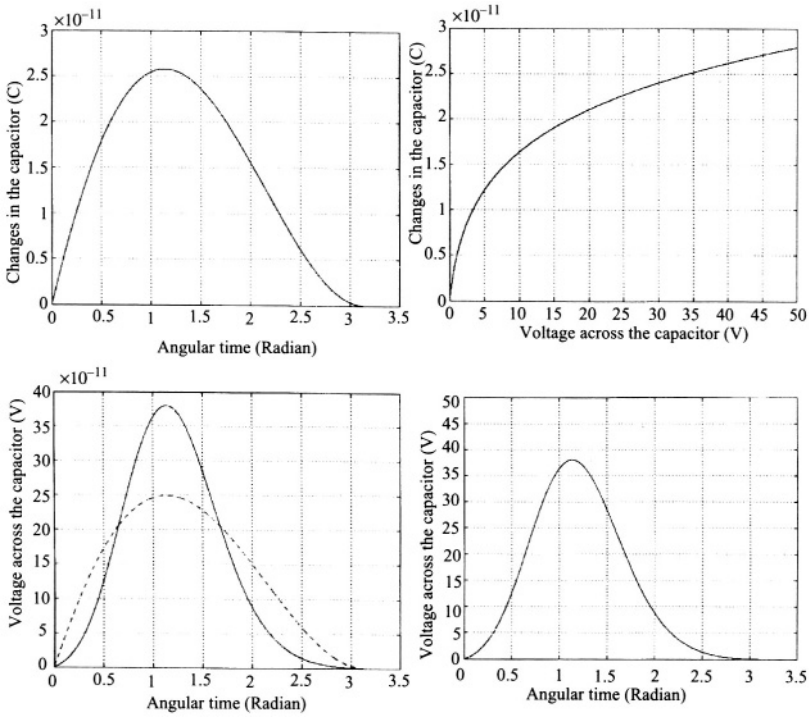


Figure 29.18. Graphical illustration of calculation of drain voltage.

increasing function of voltage. Therefore, for a given value of θ, the root of the following function can be found by a bisection method.

$$G(v_C) = Q_v(v_C) - Q_i(\theta) \tag{29.70}$$

The calculation of drain voltage $v_C(\theta)$ is illustrated graphically in Figure 29.18. The parameters in this example are $P_o = 1\,\text{W}$, $V_{DD} = 7\,\text{V}$, $f = 1$ GHz, $V_{bi} = 0.7\,\text{V}$ and $n = 9$. The top-left sub-graph shows the waveform of $Q_i(\theta)$ and the top-right sub-graph shows the waveform of $Q_v(v_C)$. The value of v_C at a certain value θ can be obtained by equating the corresponding charges. Therefore, the two sub-graphs can be combined to form the bottom-right sub-graph which is the relationship between v_c and θ. In the bottom-left sub-graph, the solid line is the drain voltage waveform when a nonlinear shunt capacitor $n = 9$ is used and the dotted line is the drain voltage waveform when a linear shunt capacitor is used. The average voltage across the shunt capacitor is given by,

$$\bar{v}_C(C_{j0}) = \frac{1}{2\pi}\int_0^{\pi} v_C(\theta)\,\mathrm{d}\theta \tag{29.71}$$

For the same amount of stored charges, the higher the zero-bias capacitance, the lower the voltage across the capacitor is. Therefore, an increase in the zero-bias capacitance reduces the average voltage across the capacitor. That is, $\bar{v}_C(C_{j0})$ is a monotonically decreasing function of C_{j0}. The root of the following function can be found by using a bisection method.

$$F(C_{j0}) = \overline{v_C}(C_{j0}) - V_{DD} \tag{29.72}$$

The method requires two bisection procedure loops. The outer loop is used to find the root of $F(C_{j0})$ in equation (29.72) and the inner loop is used to find the root of $G(v_C)$ in equation (29.70) for each value of θ.

Fourier analysis. Similar to the linear case, the series reactance jX can be found with Fourier analysis:

$$v_1(\theta) = c_1 \sin(\theta + \phi + \psi) \tag{29.73}$$

$$v_1(\theta) = c_1[\cos(\psi)\sin(\theta + \phi) + \sin(\psi)\cos(\theta + \phi)] \tag{29.74}$$

Therefore, by finding the $\sin(\theta + \phi)$ and $\cos(\theta + \phi)$ components of $v_C(\theta)$, X can be found.

$$\frac{X}{R} = \tan(\psi) = \frac{\int_0^{\pi} v_C(\theta)\cos(\theta + \phi)\,d\theta}{\int_0^{\pi} v_C(\theta)\sin(\theta + \phi)\,d\theta} \tag{29.75}$$

Normalized power capability. The maximum drain voltage can be obtained by finding the angular time at which maximum drain voltage occurs [7].

$$I_{DD} - \frac{c}{R}\sin(\theta_{v,\max} + \phi) = 0 \tag{29.76}$$

$$\theta_{v,\max} = \sin^{-1}\left(\frac{I_{DD}R}{c}\right) - \phi \tag{29.77}$$

$$\theta_{v,\max} = 2\tan^{-1}\left(\frac{2}{\pi}\right) \tag{29.78}$$

$$v_{C,\max} = v_C\left(2\tan^{-1}\left(\frac{2}{\pi}\right)\right) \tag{29.79}$$

When the switch is closed, $\pi < \theta < 2\pi$

$$i_C(\theta) = 0 \tag{29.80}$$

From equation (29.35),

$$i_D(\theta) = I_{DD} - \frac{c}{R}\sin(\theta + \phi) \tag{29.81}$$

The maximum drain current is given by [7]:

$$i_{D,max} = I_{DD} + \frac{c}{R} = \left(1 + \sqrt{1 + \frac{\pi^2}{4}}\right) I_{DD} \tag{29.82}$$

Using equations (29.79) and (29.82), the normalized power capability can be calculated. The normalized component values and characteristics of a Class E power amplifier with nonlinear drain capacitance are shown Figure 29.19.

The drain voltage waveform for a Class E power amplifier with a nonlinear shunt capacitance $n = 9$ is shown in the bottom-left sub-graph of Figure 29.18. In the short time intervals after turn-off and before turn-on, the drain voltage with a nonlinear shunt capacitance is smaller than that with a linear shunt capacitance. A Class E power amplifier with a nonlinear shunt capacitance has better performance in terms of on/off transition power loss due to a small variation in frequency or duty cycle. However, the maximum drain voltage for a Class E power amplifier with a nonlinear shunt capacitance is higher than that with a linear shunt capacitance. Therefore, there is a trade-off between on/off transition power loss suppression and normalized power capability.

In Figure 29.19, the bottom-right sub-graph shows the trade-off between the normalized supply voltage and the normalized power capability. Note that the output power is proportional to the square of the supply voltage. Therefore, it is also a trade-off between the normalized power capability and the output power. The normalized power capability drops sharply with increasing supply voltage when the supply voltage is small and decreases slowly when the supply voltage is large. It is also observed that the more nonlinear the shunt capacitance is, the smaller the normalized power capability becomes.

29.4.2. Generalized Numerical Method

The method is generalized for any nonlinear shunt capacitance. The charges in the capacitors can be represented in two forms:

$$Q_i(\theta) = \frac{I_{DD}\theta + c/R\,[\cos(\theta + \phi) - \cos(\phi)]}{\omega} \tag{29.83}$$

$$Q_v(v_C) = \int_0^{v_C} C_1(v)\,dv \tag{29.84}$$

Following the same arguments in the previous section, the charge $Q_i(\theta)$ is independent of the nonlinearity of the drain capacitance for a tuned Class E power amplifier. Given the expression for nonlinear capacitance $C_1(v)$, the charge $Q_v(v_C)$ can be obtained by equation (29.84). According to the physical property of capacitors, the amount of stored charges is a monotonically

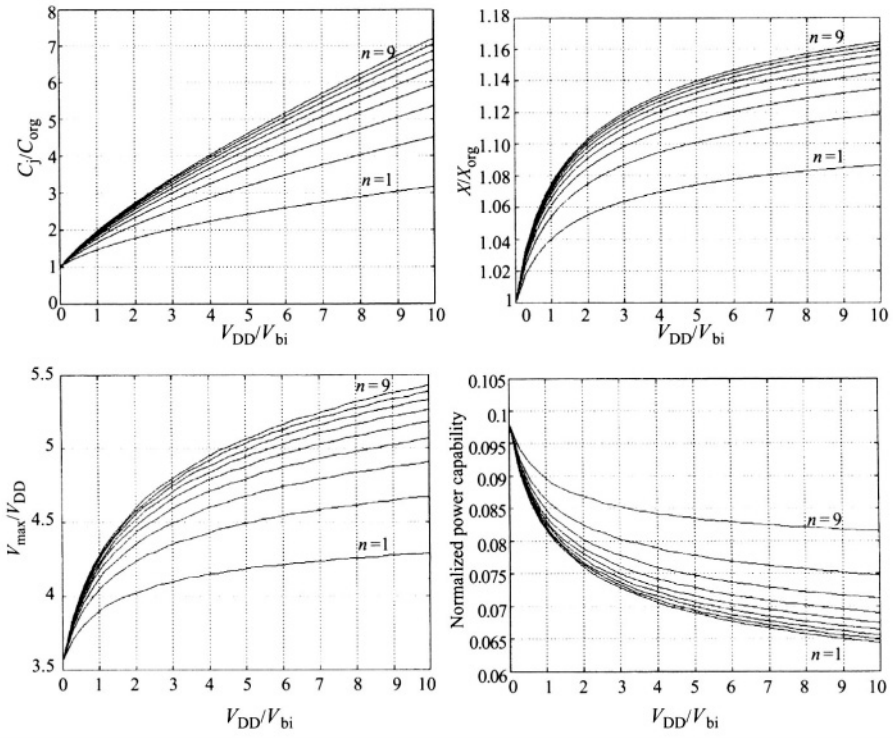


Figure 29.19. Normalized component values and characteristics of Class E power amplifier with nonlinear drain capacitance.

increasing function of voltage. Given any $C_1(v)$, the drain voltage $v_C(\theta)$ can be obtained by finding the root of equation (29.70) with the bisection method for each value of angular time θ.

Consider a nonlinear capacitance $C_1(v, \alpha)$ with parameter α such that

$$C_1(v, \alpha_1) < C_1(v, \alpha_2) \quad \forall v \quad \text{if } \alpha_1 < \alpha_2 \tag{29.85}$$

$$\int_0^{v_C} C_1(v, \alpha_1)\, dv < \int_0^{v_C} C_1(v, \alpha_2)\, dv \tag{29.86}$$

$$Q_v(v_C, \alpha_1) < Q_v(v_C, \alpha_2) \tag{29.87}$$

Since $Q_v(v_C, \alpha)$ is a monotonically increasing function of voltage, the voltage across $C_1(v, \alpha_1)$ has to be higher than that across $C_1(v, \alpha_2)$ for the same amount of stored charges, that is, for the same amount of $Q_i(\theta)$,

$$v_C(\theta, \alpha_1) > v_C(\theta, \alpha_2) \quad \forall \theta \quad \text{if } \alpha_1 < \alpha_2 \tag{29.88}$$

Therefore, the average drain voltage $\bar{v}_C(\alpha)$ is a monotonically decreasing function of α. The root of the following function can be found by using a bisection method.

$$F(\alpha) = \bar{v}_C(\alpha) - V_{DD} \tag{29.89}$$

Similar to the method described previously, the generalized method requires two bisection procedure loops. The outer loop is used to find the root of $F(\alpha)$ in equation (29.89) and the inner loop is used to find the root of $G(v_C)$ in equation (29.70).

Design example. A 1 GHz 0.4 W Class E power amplifier with supply voltage 1.4V was designed with the generalized numerical method. The AMS $0.6\,\mu\text{m}$ CMOS process BSIM3v3 model was used in the simulation. The drain parasitic capacitance was modeled as:

$$C_1(v, w) = w\left[\text{cgd0} + \text{ld} \times \text{cj}\left(1 + \frac{v}{\text{pb}}\right)^{-\text{mj}} + \text{cjsw}\left(1 + \frac{v}{\text{pbsw}}\right)^{-\text{mjsw}}\right] + 2\text{ld} \times \text{cjsw}\left(1 + \frac{v}{\text{pbsw}}\right)^{-\text{mjsw}} - 2\text{dwc} \times \text{cgd0} \tag{29.90}$$

where cgd0, cj, pb, mj, cjsw, pbsw, mjsw and dwc are technology dependent parameters; w is the channel width and $\text{ld} = 1.1\,\mu\text{m}$ is the length of the drain. This model of the shunt capacitance satisfies the condition set by equation (29.85) with w as the parameter α. Please refer to Figure 29.17 for the ideal circuit of a Class E power amplifier. From equation (29.68), $R = 2.83\,\Omega$. Let the quality factor $Q_L = 10$. Thus, $C_2' = 5.63\,\text{pF}$ and $L_2' = 4.50\,\text{nH}$. Minimum channel length of $0.6\,\mu\text{m}$ was used to maximize the drain current driving capability of the transistor. The optimum width of the transistor and the required excess reactance were calculated using the generalized numerical method: $w = 9950\,\mu\text{m}$ and $jX = 3.33\,j\Omega$ which corresponds to an inductance of 0.530 nH. A very large DC-Feed inductor $L_1 = 1\,\mu\text{H}$ was used in order to satisfy the assumption of an infinite DC-Feed inductor.

The transient analysis simulations were performed by the Cadence Spectres simulator. The simulation time was set to be long enough for the circuit to reach steady-state. A square wave at 1 GHz was applied to the gate of the transistor. The waveforms for the drain voltage and the drain-source current at input power of 17.2 dBm are shown in Figure 29.20. The drain efficiency η and power added efficiency PAE were 95.8% and 80.2% respectively.

Small linear shunt capacitor. In the literature, the use of a shunt linear capacitor in parallel with the parasitic drain capacitor was mentioned [30,31].

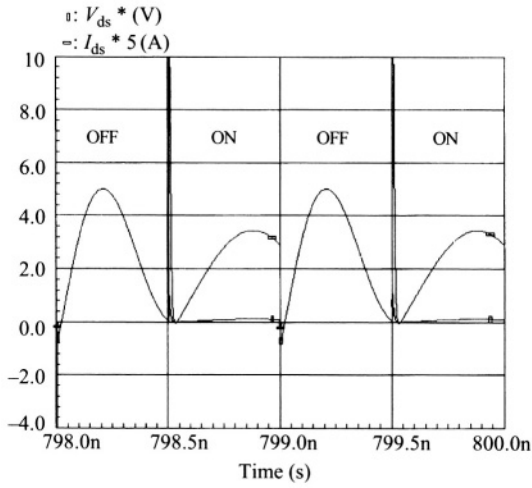


Figure 29.20. Waveforms of the simulated Class E power amplifier.

In order to make the effect of the nonlinearity of the parasitic drain capacitance negligible, the linear shunt capacitor has to be much larger than that of parasitic. However, the required shunt capacitance for the tuned operation of Class E amplifiers at high frequency is small and comparable to the parasitic capacitor. Therefore, using a large shunt capacitor to minimize the effect of the nonlinearity of parasitic drain capacitance is not possible. In fact, the nonlinear drain capacitance together with a small linear auxiliary capacitor is proposed to provide the required shunt capacitance.

Elimination of AM-to-PM distortion. From Subsection 29.2.3, by applying EER linearization technique on Class E power amplifiers, both high power efficiency and bandwidth efficiency can be achieved. However, due to the AM-to-PM distortion, there is a trade-off between the maximum supply voltage and the phase accuracy. To minimize the AM-to-PM distortion a phase-correcting feedback network, which consists of a limiting amplifier, a phase detector and a phase shifter, was suggested. In this section, a simple idea to minimize the AM-to-PM distortion is described.

From equation (29.66), the phase shift ϕ is theoretically independent of the nonlinearity of the shunt capacitance and the supply voltage V_{DD} if the power amplifier is tuned. Component values for optimal Class E operation at different supply voltage can be found. From Figure 29.19, the variation of the series reactance jX is small compared to the variation of the optimal zero-bias shunt capacitance C_{j0}. Therefore, variation of the optimal zero-bias shunt capacitance C_{j0} could be sufficient to minimize the AM-to-PM distortion. However, once the transistor is fabricated, the zero-bias capacitance cannot be

adjusted with respect to the variation of the supply voltage. A variable auxiliary shunt capacitor is added in parallel with the drain capacitance. If the capacitance of the auxiliary capacitor can be adjusted according to the modulation of the supply voltage, the AM-to-PM distortion due to the nonlinearity of the shunt capacitor can be minimized. The proposed circuit is shown in Figure 29.21. C_p is the output parasitic capacitance and C_l is the variable auxiliary capacitor.

The variable auxiliary capacitor may be realized by using a network of capacitor with controlling transistors [32], The model of the shunt capacitor is given by

$$C_l(v_C, C_l) = C_{j0}\left(1 + \frac{v_C}{V_{bi}}\right)^{-n/(n+1)} + C_l \tag{29.91}$$

where C_{j0} is the zero-bias capacitance of the drain–bulk junction and C_l is the capacitance of the linear auxiliary capacitor. This model of the shunt capacitance satisfies the condition set by equation (29.85) with C_l as the parameter α. The optimum values for the linear auxiliary capacitor can be calculated with the generalized method. In this analysis, C_{j0} is fixed and equal to $C_{org} = 1/5.4466\omega R$ which is the shunt capacitance in the linear case.

Figure 29.22 shows the results of the analysis. In equation (29.91), the first term represents the nonlinear capacitance due to the drain parasitic capacitance. The value of this nonlinear term decreases with increasing supply voltage. At a small supply voltage, the nonlinear term is relatively large and the required linear auxiliary capacitance is small. The characteristic for the nonlinear capacitance is dominant. Therefore, the normalized maximum drain voltage increases with the supply voltage and the normalized power capability decreases. At a large supply voltage, the nonlinear term is small and the required linear

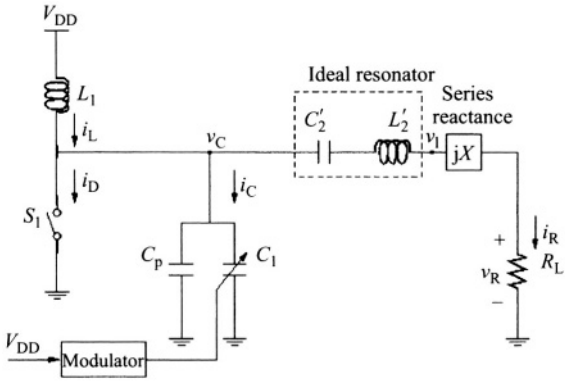


Figure 29.21. Class E power amplifier model with a variable auxiliary capacitor.

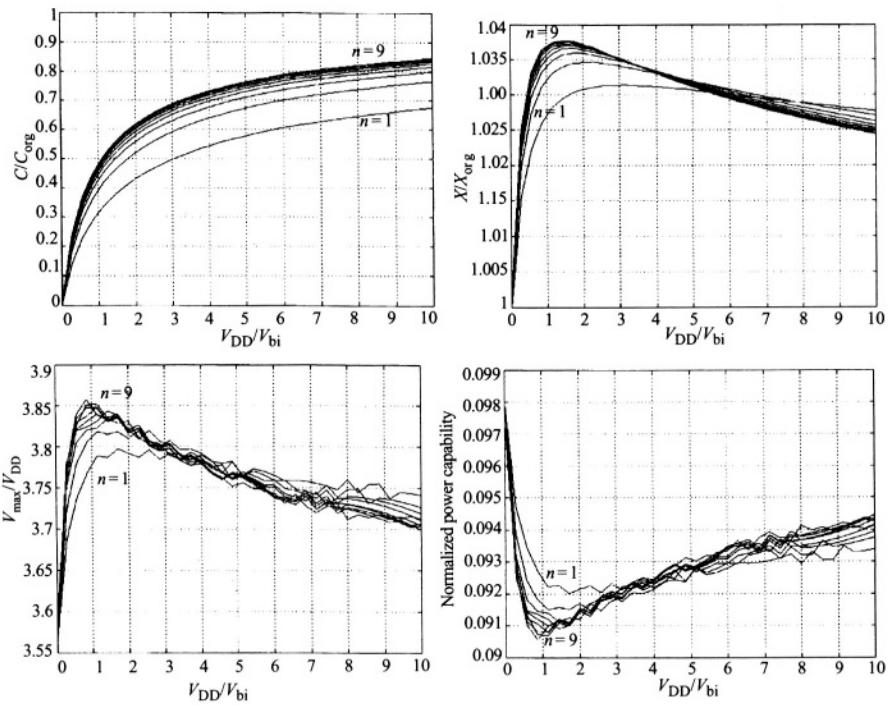


Figure 29.22. Normalized component values and characteristics of Class E power amplifier with a nonlinear drain capacitance and variable shunt capacitor.

capacitance is large. The characteristic for the linear capacitance is dominant. Therefore, the normalized maximum drain voltage tends to reduce to the value for the linear case. Thus, the normalized power capability increases with the supply voltage.

To illustrate the AM-to-PM distortion on Class E power amplifiers, a 1 GHz Class E power amplifier with an abrupt junction drain capacitance was simulated. The power amplifier was designed to output 1 W power at 3.3V supply voltage. The component values are $L_1 = 100\,\text{nH}$, $C_{j0} = 4.65\,\text{pF}$, $n = 1$, $V_{bi} = 0.7\,\text{V}$, $C_1 = 2.65\,\text{pF}$, $L_2 = 11.18\,\text{nH}$, $C_2 = 2.53\,\text{pF}$ and $R = 6.28\,\Omega$. The supply voltage was varied linearly from 0.1 to 3.3V. As shown in Figure 29.23(a), the output voltage varies very linearly with the supply voltage. Figure 29.23(b) shows a magnified view of the boxed area in Figure 29.23(a). It is noticed that the phase of the output voltage also changes with the supply voltage. This is called the AM-to-PM distortion. In this example, the output phase variation can be as large as 14.76°.

Figure 29.24 shows the output voltage of the same Class E power amplifier with an ideal variable auxiliary shunt capacitor. Figure 29.24(a) shows that the

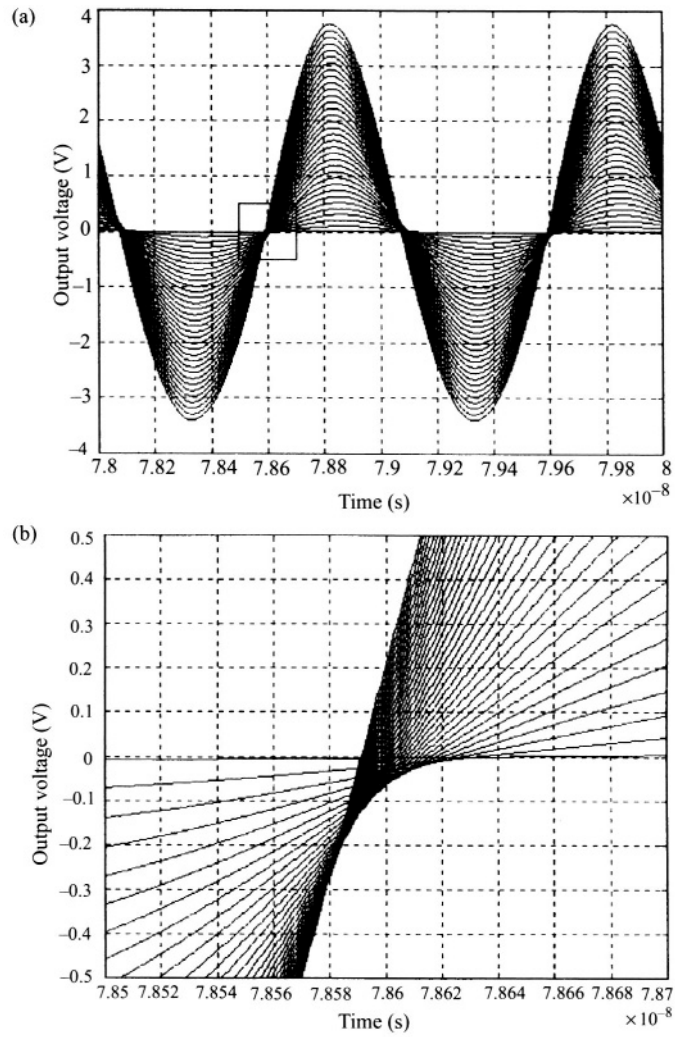


Figure 29.23. The AM-to-PM distortion on Class E power amplifier.

output voltage varies linearly with the supply voltage. Figure 29.24(b) shows a magnified view of the boxed area in Figure 29.24(b). It is noticed that the phase does not change significantly with the supply voltage. The phase change between 0.1 and 3.3V supply is limited to 2.16° in this example.

Compensation for MHz Operation. At low frequency 1 MHz, the required linear shunt capacitance is usually much larger than the nonlinear drain capacitance. The drain capacitance is negligible and the required linear shunt capacitance can be obtained by conventional Class E theory. At high frequency 1 GHz, the required linear shunt capacitance is very small and comparable to

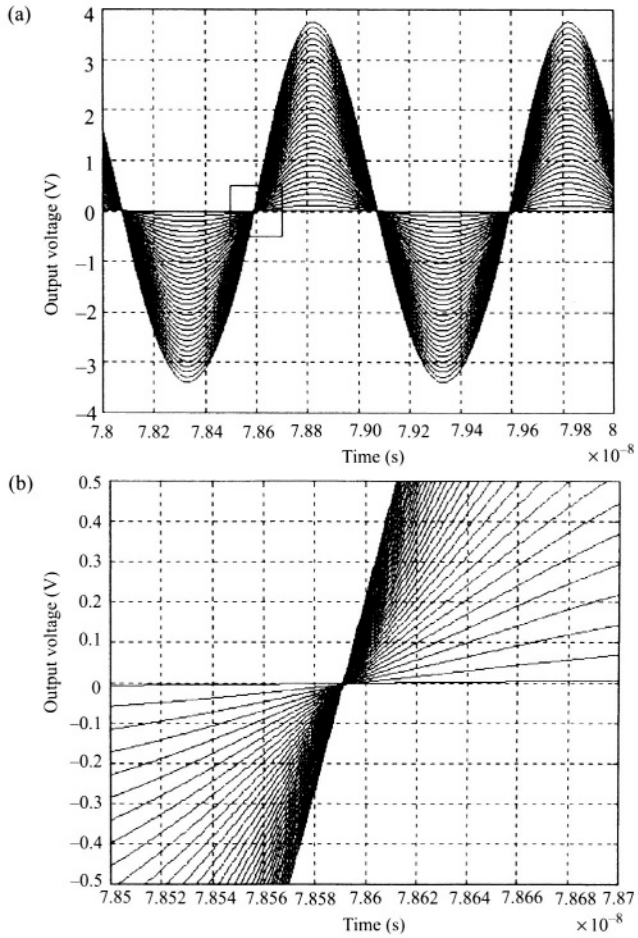


Figure 29.24. **Minimization of the AM-to-PM distortion with a variable auxiliary shunt capacitor.**

the drain capacitance. It is sensible to use the nonlinear drain capacitance to replace the linear shunt capacitance. At frequency between 1 MHz and 1 GHz, the required linear shunt capacitance is small and thus the drain capacitance is not negligible. The required shunt capacitance can be provided partially by a small linear auxiliary capacitor and partially by the drain capacitor. The model for the shunt capacitance is given by

$$C_1(v_C, C_l) = C_p(v_C) + C_l \tag{29.92}$$

where $C_p(v_C)$ is the nonlinear drain capacitance and C_l is the linear auxiliary capacitance. This model of the shunt capacitance satisfies the condition set by

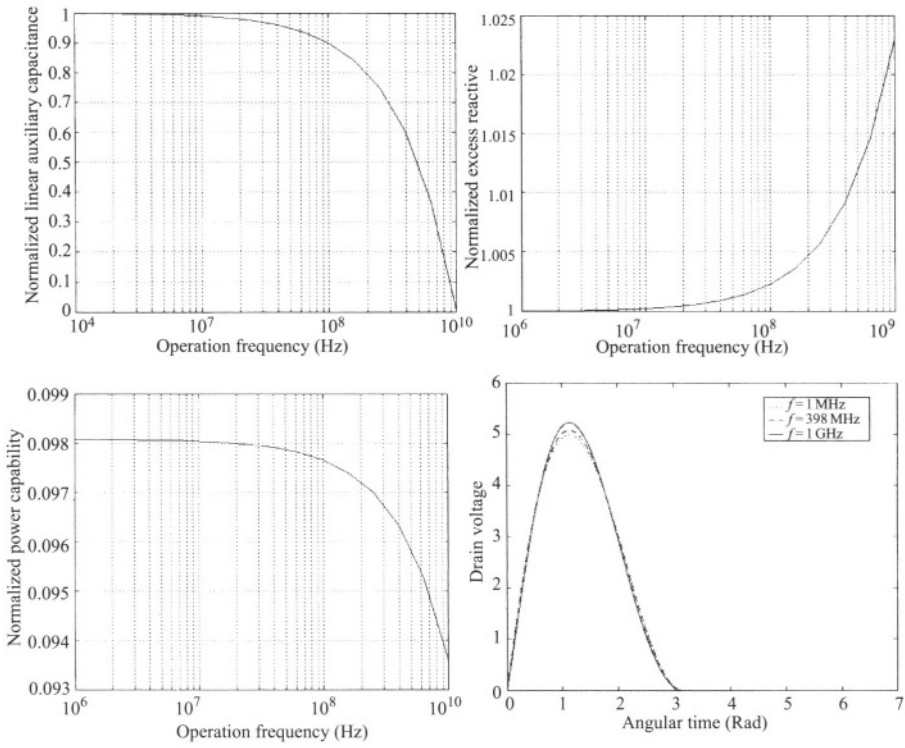


Figure 29.25. Effect of frequency on Class E power amplifier design with auxiliary capacitor.

equation (29.85) with C_1 as the parameter α. The optimum values for the linear auxiliary capacitor can be calculated with the generalized method. Analysis results on a 1.4 V 0.4 W Class E power amplifier at frequency ranging from 1 MHz to 1 GHz are shown in Figure 29.25. In this analysis, the nonlinear transistor output capacitance is given by equation (29.90) with $w = 9950\,\mu\text{m}$.

As shown in the top-left sub-graph of Figure 29.25, the normalized linear auxiliary capacitor changes from 1 to 0 as frequency increases from 1 MHz to 1 GHz. In the bottom-left sub-graph, the normalized power capability decreases accordingly as the nonlinear transistor output capacitance becomes dominant. Clearly, there is a trade-off between the operating frequency and the normalized power capability. The bottom-right sub-graph shows the drain voltage waveforms at different frequencies.

29.5. Conclusion

In this chapter, different classes of power amplifiers are compared in terms of ideal efficiency, power capability and bandwidth efficiency. Among

current-source power amplifiers, Class C power amplifiers have highest ideal efficiency with low normalized power capability whilst Class AB power amplifiers have high normalized power capability with low ideal efficiency. Theoretically, all switch-mode power amplifiers can achieve 100% ideal efficiency. Class D and Class F power amplifiers have the highest possible power capability of 0.159. Depending on the number of odd harmonics present in the drain voltage waveform of Class F power amplifiers, the ideal efficiency varies from 78.5% to 100% with normalized power capability from 0.125 to 0.159. The improvement of ideal efficiency of Class F power amplifiers does not come at the expense of normalized power capability but at the expense of higher complexity of the circuit. Class E power amplifiers also have 100% ideal efficiency with acceptable normalized power capability of 0.0981. The advantages of Class E power amplifiers over other classes of switch-mode power amplifiers are the minimization of power losses during transistor on/off transitions and suitability for linearization with EER technique to improve bandwidth efficiency. The latter part of this chapter focuses on Class E power amplifiers.

An analytical method is derived to describe the power efficiency of a Class E power amplifier taking into account the loaded Q-factor. With the mechanism of the power losses associated with the drain current fall time, we derive the equations governing the operation of Class E power amplifier and these equations make the performance more predictable. Circuit simulations using CMOS SPICE models are performed to confirm the validity of our models. Characteristics of this circuit as a function of Q_L and θ_f have been shown. In terms of power efficiency and linearity, the plausible Q_L is in the range of 5–10. For small feature size MOS devices, lower fall time angle can be expected and loaded Q-factor becomes less important for power efficiency. On the other hand, given the continued advances in scaling of silicon MOS technologies, it is evident that high power efficiency CMOS power amplifier is possible in the near future as deep-submicron technologies become commercially available.

A theory based on physical properties of capacitor for Class E power amplifiers with nonlinear transistor output capacitance is presented. A generalized numerical method to obtain optimal component values for any nonlinear transistor output capacitance is described. A design example of a realistic Class E power amplifier with a BSIM3v3 drain capacitance model is used to validate the method. From simulation results, it is found that the nonlinearity of the shunt capacitance reduces the drain-to-source voltage near on/off transitions but increases the maximum drain-to-source voltage. Hence, there is a trade-off between reduction of power loss during on/off transitions and the device stress. An alternative way to minimize AM-to-PM distortion in EER linearization method for Class E power amplifiers is also proposed. A small linear auxiliary shunt capacitor is proposed to provide the required shunt capacitance together

with the nonlinear transistor output capacitance. A linearized Class E power amplifier can be used in a system with a more bandwidth efficient modulation scheme and thus the trade-off between power efficiency and bandwidth efficiency can be relaxed.

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Chapter 30

TRADE-OFFS IN STANDARD AND UNIVERSAL CNN CELLS

Martin Hänggi, Radu Dogaru and Leon O. Chua

30.1. Introduction

In 1988, Chua and Yang proposed the cellular neural network (CNN) [1,2] which differs from the analog Hopfield network in its *local connectivity* property, where each neuron has a *separate input* from its neighbor cells, in addition to its own *input* and *initial state,* its space-invariant weight patterns, and the piece-wise linear output function of its neurons or *cells* which are arranged in a regular grid of dimension one or two. These properties allow its realization in VLSI technology, resulting in CNN chips that are tailor-made for real time signal processing. In fact, many complex scientific problems can be formulated with regular grids, where direct interaction between the signals on various grid points is limited within a finite local neighborhood, which is also called the *sphere of influence.* Hence, the most fundamental ingredients of the CNN paradigm are: the use of analog processing cells with continuous signal values, and local interaction within a finite radius. Applications of the CNN include image and video signal processing, nonlinear signal processing in general, modeling of biological systems and higher brain functions, pattern recognition and generation, and the solving of partial differential equations. The CNN has turned out to be a very general paradigm for complexity, based on nonlinear dynamics.

In this chapter we will restrict our study to the case of binary information processing. The ideal CNN cell is supposed to be compact, robust to deviations of the circuit parameters, universal (i.e. capable of implementing arbitrary Boolean functions) and capable of fast learning and adaptation. In a practical realization, however, these requirements are often contradictory, and therefore, leading to different engineering solutions characterized by certain trade-offs. This chapter presents state-of-the-art models of CNN cells and the trade-offs between the properties mentioned above one has to cope with. For example, a first trade-off to be considered is between universal and standard CNN cells. In standard CNN cells, universality is sacrificed to get very compact implementations but limited functional capabilities.

As shown in Section 30.2, some additional trade-offs should be considered within the standard CNN cell since not all local functions are leading to equally

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robust representations and since there is an interdependence between processing speed and reliability. Even if the universality is sacrificed at the hardware level (i.e. the cell implementation), certain decomposition schemes can be defined so that a more complex local function is represented by sequentially computed simpler local functions using standard CNN cells and combining the partial results.

Section 30.3 introduces three models of universal CNN cells where arbitrary local functions can be represented directly in hardware. The trade-offs between robustness, compactness and complexity of the learning algorithm are discussed comparatively for those models.

30.2. The Standard CNN

A CNN or, more generally, a cellular nonlinear network is an ensemble of spatially arranged cells, where each cell is itself a dynamical system that is locally coupled to its neighboring cells within some prescribed sphere of influence [1,3,4].

A CNN is characterized by its *topology* and its *dynamics.* The topology determines the arrangement of cells (e.g. a square or a hexagonal grid) and the dimensionality, whereas the dynamics describes the temporal evolution of each *cell* which is assumed to be governed by an ordinary differential equation.

In the first part of this chapter, we will focus on standard CNNs with $n = MN$ identical cells on a two-dimensional rectangular grid and spatially invariant coupling laws, using the same notation and terminology as in [4]. The topology of such a CNN is shown in Figure 30.1. $x_{ij}(t)$ is the *state,* $y_{ij}(t)$ the *output,* u_{ij} the (time-invariant) *input,* and z_{ij} the *threshold* of the cell C_{ij} at position (i, j). Assuming that the coupling is linear, the dynamics of the network is governed by a system of n differential equations,

$$\frac{\mathrm{d}x_{ij}(t)}{\mathrm{d}t} = -x_{ij}(t) + \sum_{k,l \in \mathcal{N}_{ij}} \left(a_{k-i,l-j}\, y_{ij}(t) + b_{k-i,l-j}\, u_{kl}\right) + z_{ij} + \partial_{ij} \quad (30.1)$$

$(i, j) \in \{1, \ldots, M\} \times \{1, \ldots, N\}$, where $\mathcal{N}_{ij}$ denotes the neighborhood of the cell C_{ij}, and a_{kl} and b_{kl} are the *feedback* and *control* template parameters, respectively. Since the cells on the margins of the CNN do not have a complete set of regular neighbors, the CNN is assumed to be surrounded by a virtual ring of cells whose input and output is constant (Dirichlet boundary condition) or determined by regular cells (zero flux or periodic boundary condition); their contribution is given by the quantities ∂_{ij}. The *output function* $f(\cdot) : \mathbb{R} \to \mathbb{R}$ is a monotonically increasing function, and $y_{ij}(t) = f(x_{ij}(t))$ is the *output equation* of the standard CNN. The nonlinearity $f(\cdot)$ is the following piece-wise

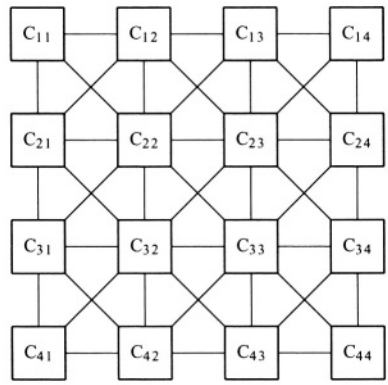


Figure 30.1. Topology of a planar CNN.

linear function (Figure 30.2):

$$f(x) = \tfrac{1}{2}(|x+1| - |x-1|) \tag{30.2}$$

We will also denote it by $\mathbf{sat}(\cdot)$, the *saturation* function.

If we restrict the neighborhood radius of every cell to 1 (nearest neighbors) and assume that z_{ij} is constant over the whole network, the *cloning template* $\{\mathbf{A}, \mathbf{B}, z\}$ is fully specified by 19 parameters, namely the two 3×3 matrices $\mathbf{A} = \{a_{kl}\}$ and $\mathbf{B} = \{b_{kl}\}$ and the value of z. For notational convenience, these 19 parameters are often rearranged into a single one-dimensional vector $\mathcal{T} \in \mathbb{R}^{19}$, henceforth called a template vector or, biologically inspired, a *CNN gene*.

Denoting the nine entries in A and B by

$$\mathbf{A} = \begin{bmatrix} a_1 & a_2 & a_3 \\ a_4 & a_5 & a_6 \\ a_7 & a_8 & a_9 \end{bmatrix} \quad \mathbf{B} = \begin{bmatrix} b_1 & b_2 & b_3 \\ b_4 & b_5 & b_6 \\ b_7 & b_8 & b_9 \end{bmatrix}$$

the corresponding CNN gene is

$$\mathcal{T} = [z, b_1, b_2, b_3, b_4, b_5, b_6, b_7, b_8, b_9, a_1, a_2, a_3, a_4, a_5, a_6, a_7, a_8, a_9]$$

We speak of a *linear* cell if the state of the cell is in the linear region of $\mathbf{sat}(\cdot)$, that is, $|y(t)| = |x(t)| < 1$, and otherwise of a *saturated* cell. A saturated cell can take on only the values ± 1, that is, it is *bipolar* valued. If all elements in the **A**-template are zero except possibly the center element, a_c, the CNN is said to be *uncoupled* since there is no feedback from the outputs of the neighbors. If at least one of the off-center entries in **A** is non-zero, the CNN is *coupled*. The *steady-state output* is denoted by y^*, provided the CNN is stable. In many

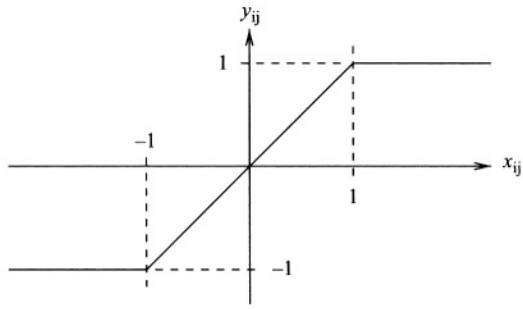


Figure 30.2. The saturation output function.

applications we are interested in bipolar (±1) outputs y_{ij}^*. If the input is also bipolar, we speak of a bipolar CNN.

Definition 30.1 (Bipolar CNN). *A CNN is* bipolar, *if* $\mathbf{u}$, $\boldsymbol{y}^* \in \mathbb{B}^{MN}$ *and* $\boldsymbol{x}(0) \in \mathbb{B}_0^{MN}$ *for* $\mathbb{B} = \{-1, 1\}$ *and* $\mathbb{B}_0 = \{-1, 0, 1\}$.

A simple theorem provides a sufficient condition for bipolar outputs at equilibrium.

Theorem 30.1 (Condition for bipolar output). *Assuming that the system (30.1) always tends to a dc equilibrium point and that the self-coupling term* a_c *satisfies* $a_c > 1$, *then the outputs of the system (30.1) at equilibrium are bipolar.*

For a proof we refer to [5]. The basic idea is to show that for $a_c > 1$ any equilibrium in the linear region becomes unstable, that is, there is at least one eigenvalue λ with $\mathrm{Re}(\lambda) > 0$.

30.2.1. Circuit Implementation of CNNs

Applications of CNNs in image and signal processing become efficient only if the network equation can be implemented in analog hardware. A variety of approaches have been proposed and successfully implemented [6–12]. Consider the circuit depicted in Figure 30.3. The differential equation describing this circuit corresponds to (30.1) and can be written as

$$C\frac{\mathrm{d}\tilde{x}_{ij}(\tau)}{\mathrm{d}\tau} = -\frac{1}{R}\tilde{x}_{ij}(\tau) + \sum_{mn\in\mathcal{N}_{ij}^r} \tilde{a}_{mn} f(\tilde{x}_{mn}(\tau)) + \sum_{mn\in\mathcal{N}_{ij}^r} \tilde{b}_{mn}\tilde{u}_{mn} + \tilde{I} \quad (30.3)$$

where the tilde signifies non-normalized parameters. The state of a cell is the voltage across the capacitor. The weights are realized as voltage controlled current sources.

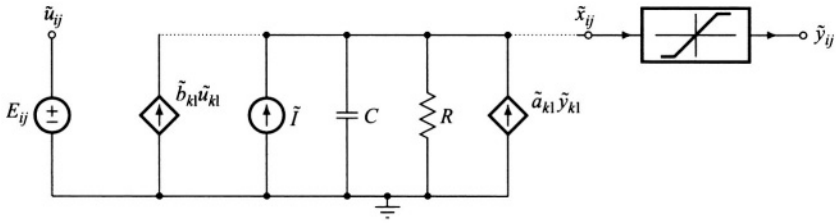


Figure 30.3. Circuit of a cell.

In this chapter, we will be mainly concerned with the *normalized* equation (30.1), where all quantities are dimensionless. Its relation to (30.3) is established by the following transformations:

$$\begin{aligned} t &\longrightarrow \frac{\tau}{RC} \\ x_{mn} &\longrightarrow \tilde{x}_{mn} \\ u_{mn} &\longrightarrow \tilde{u}_{mn} \\ a_{mn} &\longrightarrow R\tilde{a}_{mn} \\ b_{mn} &\longrightarrow R\tilde{b}_{mn} \\ I &\longrightarrow R\tilde{I} \end{aligned}$$

30.3. Standard CNN Cells: Robustness vs Processing Speed

The reliability and the speed of an analog circuit are among its most important quality attributes. However, for most circuits, including the cellular neural network, these are conflicting issues. In this section, we will provide an in-depth analysis of the reliability–speed trade-off for standard CNN cells.

30.3.1. Reliability of a Standard CNN

Introduction. Analog VLSI implementations of the network equation (30.1) have a number of limitations that need to be taken into account in the theory of CNNs in order to guarantee correct and efficient operation of analog VLSI hardware. Template parameters can only be realized with a precision of typically 5–10% of the nominal values [6,11,13,14], and usually only a discrete set of possible values is available [15,16]. Further sources of error are

- perturbations of the input and the initial state.
- the output nonlinearity. Both the slope in the linear region and the clipping level may deviate from (30.2).

- the mismatch of the cell's time constant (product of the resistor's and the capacitor's values in each cell). Large differences in the time constants of interacting cells may result in unexpected network behavior.
- the limited state swing. The cell's states saturate at some level $x_{\max}$, determined by the bias voltage of transistors or operational amplifiers, leading to non-exponential transients. (The solutions of the ideal network equation (30.1) are piece-wise exponential functions.)

The requirement that a template set fulfills a given task reliably under these circumstances poses additional obstacles to template design or template learning. A CNN operation that is carried out reliably despite all these imperfections, is a so-called *robust* operation. For our analysis, we consider only perturbations of the template parameters, assuming that inaccuracies in input, initial state and clipping level can be accounted for by large enough errors for templates. Accordingly, the *robustness* issue reduces to the problem of finding template parameters that can tolerate deviations from their nominal values while still executing the correct operation.

Absolute and relative robustness. For a general system (or circuit) $\mathcal{M}$ with given input and initial state, whose output y depends on a parameter vector $\boldsymbol{p} \in \mathbb{R}^m$, we may quantify the degree of *robustness* with respect to its parameters by the following definition:

Definition 30.2 (Robustness). *M is* ϵ*-robust at* $\boldsymbol{p} \in \mathbb{R}^m$ *if*

$$\|\boldsymbol{p} - \boldsymbol{p}'\|_\infty \leq \epsilon \quad \Leftrightarrow \quad y(\boldsymbol{p}') = y(\boldsymbol{p}) \tag{30.4}$$

If this condition holds, we also say that for M, the parameter vector p has an absolute robustness *of* ϵ *and a* relative robustness *of* $m \cdot \epsilon / \|\boldsymbol{p}\|_1$.

This definition is based on strict *output-invariance*; hence, sensitivity theory is not applicable, since the partial derivatives $\partial y / \partial \boldsymbol{p}$ are zero or not defined for bipolar CNNs.

The Robustness of a CNN template set. In the case of a CNN, programed by a template set $\boldsymbol{p}$, the *robustness* is a measure which quantifies the degree by which a template set can be altered while still producing the desired output (at equilibrium) $y^*(\boldsymbol{p})$.

We include only the non-zero parameters in the vector $\boldsymbol{p} \in \mathbb{R}^m$, since a zero template entry is assumed to be realized by omitting some circuitry, or by switching or disabling some controlled source, not by nulling; zero template entries are therefore "precise". For later convenience, let the first element in $\boldsymbol{p}$ be the center element of the A template ($p_1 := a_c$).

Definition 30.3 (Robustness of a template set). *The* absolute *robustness* ϵ *of a template set is*

$$\epsilon(\boldsymbol{p}) = \max_{\alpha} \{\alpha \,|\, y^*(\boldsymbol{p}) = y^*(\boldsymbol{p} + \alpha \boldsymbol{I}^{\pm}) \quad \forall \boldsymbol{I}^{\pm} \in \mathbb{B}^m\}$$

Hardware tolerance effects due to physical and manufacturing imperfections give rise to parameter errors roughly proportional to the absolute value of the respective parameter [13]. We, therefore, also consider the relative *robustness criterion: The* relative *robustness D of a template set is*

$$D(\boldsymbol{p}) = \max_{\alpha} \left\{ \alpha \mid y^* \left(\boldsymbol{p} \odot (\boldsymbol{1} + \alpha \boldsymbol{I}^{\pm}) \right) = y^*(\boldsymbol{p}) \quad \forall \boldsymbol{I}^{\pm} \in \mathbb{B}^m \right\} \tag{30.5}$$

$\odot$ *denotes componentwise vector multiplication.*

For the sake of clarity and mathematical tractability, we define a slightly modified template vector $\tilde{\boldsymbol{p}}$ to be

$$\tilde{p}_1 := p_1 - 1 = a_c - 1 \quad \tilde{p}_i := p_i \quad 2 \le i \le m$$

or, alternatively, $\tilde{\boldsymbol{p}} := \boldsymbol{p} - \boldsymbol{e}_1$, where $\boldsymbol{e}_1$ is the unit vector in direction of increasing a_c.

For the further analysis, we restrict ourselves to the class of *locally regular* CNN operations [17,18], which includes almost all bipolar operations that can possibly be executed reliably on an analog CNN chip. Locally regular CNN tasks are fully characterized by a set of $\hat{m}$ inequalities for $\dot{\boldsymbol{x}}(t)$. Utilizing the modified template vector $\tilde{\boldsymbol{p}}$ and matrix-vector notation, the region $\mathcal{R} \subset \mathbb{R}^m$ where a template set operates correctly is then defined to be

$$\mathcal{R} = \{\tilde{\boldsymbol{p}} \in \mathbb{R}^m \,|\, (\mathbf{K} \cdot \tilde{\boldsymbol{p}})_i > 0 \quad \forall 1 \le i \le \hat{m}\} \tag{30.6}$$

for a coefficient matrix $\mathbf{K} \in \mathbb{B}^{\hat{m} \times m}$ representing the different constellations of u and x(t). (If a negative derivative is prescribed, the sign of the corresponding row in K is adapted.)

The term *safety margin* of an operation is denoted by $\gamma(\mathcal{T})$ and formally defined to be

$$\gamma(\mathcal{T}) = \gamma(\tilde{\boldsymbol{p}}) = \min_{1 \le i \le \hat{m}} \{(\mathbf{K} \cdot \tilde{\boldsymbol{p}})_i\} \quad \tilde{\boldsymbol{p}} \in \mathcal{R} \tag{30.7}$$

The *absolute* and the *relative robustness* may now be expressed as

$$\epsilon(\mathcal{T}) = \frac{\gamma(\mathcal{T})}{m} \quad \text{and} \quad D(\mathcal{T}) = \frac{\gamma(\mathcal{T})}{\|\mathcal{T}\|_1} \tag{30.8}$$

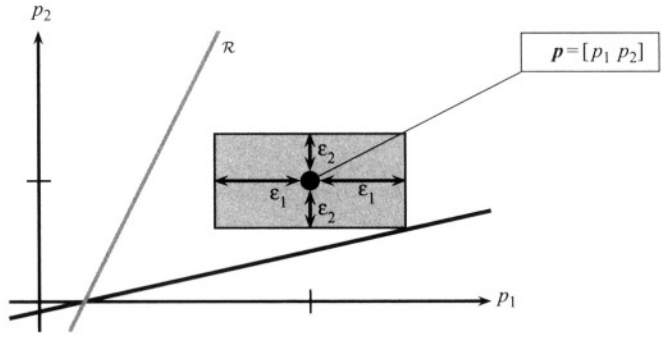


Figure 30.4. Determination of the relative robustness in a two-dimensional case.

respectively. $\|\mathcal{T}\|_1$ is the L_1-norm of the template vector,

$$\|\mathcal{T}\|_1 = |I| + \sum_{i=1}^{9} |a_i| + |b_i| \tag{30.9}$$

Note that these definitions of robustness are completely deterministic – they are not based on any assumptions on the probability density of the perturbation of the template vector.

In Figure 30.4, the determination of the relative robustness D in a two-dimensional case is illustrated. The gray-shaded box is the largest box with $\epsilon_1/p_1 = \epsilon_2/p_2 =: D$.

Template scaling. From (30.7) and (30.8), it follows that $\epsilon(q\,\tilde{\boldsymbol{p}}) = q\epsilon(\tilde{\boldsymbol{p}})$, that is, by scaling the template vector $\tilde{\boldsymbol{p}}$ by a factor of q, we achieve proportionally higher *absolute robustness.*

For the *relative robustness,* we obtain

$$D(\tilde{\boldsymbol{p}}) = \frac{\gamma(\tilde{\boldsymbol{p}})}{\|\tilde{\boldsymbol{p}}\|_1 + 1} \quad \Rightarrow \quad D(q\,\tilde{\boldsymbol{p}}) = \frac{q\,\gamma(\tilde{\boldsymbol{p}})}{q\,\|\tilde{\boldsymbol{p}}\|_1 + 1} = \frac{\gamma(\tilde{\boldsymbol{p}})}{\|\tilde{\boldsymbol{p}}\|_1 + 1/q} \tag{30.10}$$

where we have made use of the fact that $\|\mathcal{T}\|_1 = \|\tilde{\boldsymbol{p}}\|_1 + 1$. Hence, the *relative robustness* is strictly monotonically increasing with increasing q, but it is upperbounded by $\gamma(\tilde{\boldsymbol{p}})/\|\tilde{\boldsymbol{p}}\|_1$.

Template design. It is now easily seen that optimization with respect to *relative robustness* implies increasing $\gamma(\tilde{\boldsymbol{p}})$, while keeping $\|\tilde{\boldsymbol{p}}\|_1$ small. Template scaling by large factors does not improve the robustness significantly, and has the disadvantage of resulting in larger template values which may not be realizable on the CNN chip.

Given the set of inequalities (30.6) which define the desired CNN operation, the design of a template with maximum robustness turns out to be a *design centering* problem, since $\tilde{\boldsymbol{p}}_{\text{opt}}$ is, in some sense, "centered" in $\mathcal{R}_*$. Formulated more precisely, the problem is to find a template set $\mathcal{T}_{\text{opt}}$ (or $\tilde{\boldsymbol{p}}_{\text{opt}}$) having the same *safety margin* in all its inequalites,

$$(\mathbf{K} \cdot \tilde{\boldsymbol{p}}_{\text{opt}}(\gamma))_i = \gamma \quad 1 \leq i \leq \hat{m} \tag{30.11}$$

Under mild conditions on the rank of **K**, the optimally robust template set can be calculated analytically in an elegant manner. For a proof, we refer to [17].

Theorem 30.2 (Optimally robust template design). Assuming that

$$(\mathbf{K} \cdot \tilde{\boldsymbol{p}})_i > 0 \quad 1 \leq i \leq m \quad \mathbf{K} \in \mathbb{B}_0^{\hat{m} \times m}, \quad \tilde{\boldsymbol{p}} \in \mathbb{R}^m \tag{30.12}$$

is a set of inequalities characterizing a CNN task, the optimally robust template vector $\tilde{\boldsymbol{p}}_{\text{opt}}$ *as a function of a scaling parameter q is*

$$\tilde{\boldsymbol{p}}_{\text{opt}}(q) = q(\mathbf{K}^t\mathbf{K})^{-1}\mathbf{K}^t\boldsymbol{I}^{\hat{m}} \tag{30.13}$$

($\boldsymbol{I}^{\hat{m}}$ *denotes the vector in* $\mathbb{R}^{\hat{m}}$ *with all its components* +1*)*

As an example, we design an uncoupled template that operates as a *horizontal line detector.* The functionality of the templates proposed in this section may be verified using the simulator available on World Wide Web under http://www.isi.ee.ethz.ch/haenggi/CNNsim_adv.html [19].

Example 30.1 (Uncoupled horizontal line detection). We consider the "actual" image to be in black (+1) on a white (−1) "background". The horizontal line detector (HLD) then removes horizontally isolated black pixels. The boundary condition for both state and input is assumed to be – 1 throughout this section.

Since this is a symmetrical and row-wise operation without global propagation of information, the template prototype

$$\mathbf{A} = [\tilde{p} + 1] \quad \mathbf{B} = [s \;\; b_c \;\; s] \quad \mathbf{I} = z \quad \boldsymbol{x}(0) = \boldsymbol{u}$$

where we have abbreviated the A-template $[0 \quad \tilde{p} + 1 \quad 0]$ by $[\tilde{p} + 1]$ for simplicity, is appropriate. The task is defined by a set of *local rules,* which specify whether a cell has to change from black to white, from white to black, or not to switch at all. For HLD, three local rules are sufficient:

	$u = y(0) \rightarrow y^*$	$\dot{x}(0)$
(1)	○●○ → ○○○	$c - 2s + z < 0$
(2)	○●● → ○●●	$c + z \geq 0$
(3)	●○● → ●○●	$-c + 2s + z \leq 0$

The underlined (center) cell is the cell under consideration. The first rule states that an isolated black cell has to turn white, which implies that $\dot{x}(0)$ has to be negative. If we insert this configuration of neighbors into the CNN dynamical equation (30.1), we find one of the inequalities that have to be satisfied for a correctly operating HLD template. For the other two, we proceed similarly.

Since the initial state $x(0)$ is equal to the input $\boldsymbol{u}$, the parameter c was introduced as the sum of $\tilde{p}$ and b_c.

Subsuming the three inequalities into a single matrix-vector equation yields

$$\begin{bmatrix} -1 & 2 & -1 \\ 1 & 0 & 1 \\ 1 & -2 & -1 \end{bmatrix} \cdot \begin{bmatrix} c \\ s \\ z \end{bmatrix} = \gamma \boldsymbol{I}^3$$

where we postulate that all inequalities are to be satisfied by γ. Applying Theorem 30.2 (in this case, $\mathbf{K}$ is invertible), we get

$$\tilde{\boldsymbol{p}}_{\text{opt}} = \gamma \mathbf{K}^{-1} \mathbf{1}^3 \quad \Longrightarrow \quad c = 2\gamma, s = \gamma, z = -\gamma$$

and, finally,

$$\mathbf{A} = [2\gamma + 1]; \quad \mathbf{B} = [\gamma\, 0\, \gamma]; \quad \mathbf{I} = -\gamma \qquad \text{or}$$
$$\mathbf{A} = [1 + \gamma]; \quad \mathbf{B} = [\gamma\, \gamma\, \gamma]; \quad \mathbf{I} = -\gamma$$

which are equivalent solutions, as both of them satisfy the condition $c = \tilde{p} + b_c = 2\gamma$. They have a safety margin of γ, and a relative robustness of $1/(5\gamma + 1)$. The maximum achievable robustness for $\gamma \to \infty$ is 1/5 = 20%.

30.3.2. The Settling Time of a Standard CNN

Introduction. In the case of a nonlinear dynamical system, the processing speed is defined by its *settling time,* that is, the time it takes the system to reach its equilibrium state.

Definition 30.4 (Settling time). For stable planar CNNs with bipolar output, we define the settling time T_S *to be the time it takes all cells to reach their final output value:*

$$T_S = \min_{t \geq 0}(t | \boldsymbol{y}(t) = \boldsymbol{y}^*)$$

This is the normalized settling time, which has to be multiplied by the RC constant of the analog cell to determine the actual processing speed of a specific CNN hardware implementation.

The exact approach for uncoupled CNNS. In this sub-section, for the sake of simplicity, input, state and output of a particular cell are represented by one index, that is, all cells are considered to form a vector.

Uncoupled templates have only one non-zero entry in the **A**-template, namely the center element a_c.

The settling time for uncoupled CNNs turns out to be of the form

$$T_S^* = \frac{1}{\tilde{a}_c} \log \frac{[1, \mathbf{1}^{\pm}] \cdot \tilde{\boldsymbol{p}}}{[-1, \boldsymbol{I}^{\pm}] \cdot \tilde{\boldsymbol{p}}}, \tag{30.14}$$

where $\boldsymbol{I}^{\pm}$ is a row vector of dimension $m - 1$, that is, $\boldsymbol{I}^{\pm} \in \mathbb{B}^{1\times(m-1)}$, representing the bipolar configurations of the neighboring cells [20].

From this result, it is seen that template scaling results in proportionally faster processing; the logarithmic part is not affected, whereas $\tilde{a}_c$ scales.

$$T_S(q \cdot \tilde{\boldsymbol{p}}) = \frac{1}{q} \cdot T_S(\tilde{\boldsymbol{p}}). \tag{30.15}$$

We have shown that by scaling $\tilde{\boldsymbol{p}}$ by a factor $q > 1$, proportionally higher absolute robustness and a slightly higher relative robustness is achieved. Hence, for uncoupled templates, *optimization for robustness and optimization for speed go hand in hand;* it is not a trade-off.

However, respecting implementation issues of the VLSI CNN chip, the *realizable* parameter space is bounded. Accordingly, the issue of speeding up the CNN processing has to be regarded under the additional condition $\|\boldsymbol{\mathcal{T}}\|_1 \leq \beta$. As an example, we consider again the HLD.

Example 30.2 (Uncoupled horizontal line detection). From Example *30.1, we know that the template set*

$$\mathbf{A} = [1 + q] \quad \mathbf{B} = [q \;\; q \;\; q] \quad \mathbf{I} = -q \tag{30.16}$$

is optimally robust. Its settling time is

$$T_S = \frac{1}{q} \log 3 \approx \frac{1.10}{q}. \tag{30.17}$$

30.3.3. Analysis of Propagation-Type Templates

Introduction. For this class of templates, no exact analytical expression can be given for the settling time. However, tight upper bounds $\hat{T}_S \gtrapprox T_S$ can be derived [20].

We start by investigating several examples.

Examples of propagation-type templates.

Example 30.3 (Shadowing). The shadowing operation (SH) is defined by the template set

$$\mathbf{A} = \begin{bmatrix} 0 & p & s \end{bmatrix} \quad \mathbf{B} = \begin{bmatrix} 0 & 0 & 0 \end{bmatrix} \quad \mathbf{I} = s \quad \text{with } 1 < p < 2s + 1$$

with a boundary of – 1. It projects the shadow of objects in the input image to the left, as if illuminated from the right side:



A tight upper bound for the settling time of this operation is [20]

$$\hat{T}_S = N \frac{p}{p-1} \log\left(\frac{2s}{2s-p+1}\right) \tag{30.18}$$

Example 30.4 (Horizontal hole detection). The horizontal hole detection template [4], also known as the connected component detector (CCD), reduces contiguous blocks of black cells along the horizontal direction to a single pixel and shifts them to the right with a one-pixel separation. It can be interpreted as a counter which counts the number of connected components in the horizontal direction.

We analyze the CCD template

$$\mathbf{A} = \begin{bmatrix} s & p & -s \end{bmatrix} \quad \mathbf{B} = [0] \quad \mathbf{I} = 0 \quad \partial_x = -1 \quad \text{with } 1 < p < 2s + 1$$

If $p \leq 2s - 1$, which is the interesting case, since other CCD templates are much slower, the settling time is

$$\hat{T}_S = -N \log\left(1 - \frac{p}{2s}\right) \tag{30.19}$$

These examples demonstrate that for this template class, the settling time is very robust with regard to template scaling, since it depends primarily on the *ratio* of the parameters, not on their absolute values. If the *ratio* determines the settling time, we immediately conjecture that the fastest templates lie on the boundary of R and thus have zero robustness.

Figure 30.5 depicts robustness and speed contour plots for three typical tasks (shadowing, horizontal line detection, connected component detection), reduced to two dimensions, and Table 30.1 presents optimally robust and optimally fast templates. It is easily seen that a joint optimization is difficult, since robustness has to be balanced against speed. However, if a CNN chip permits a reproduction of the parameters with a relative accuracy of, say, 8%, rather than creating a (slow) template with 20% robustness, we should focus on maximizing the processing speed to find the fastest template with 8% robustness. Thus,

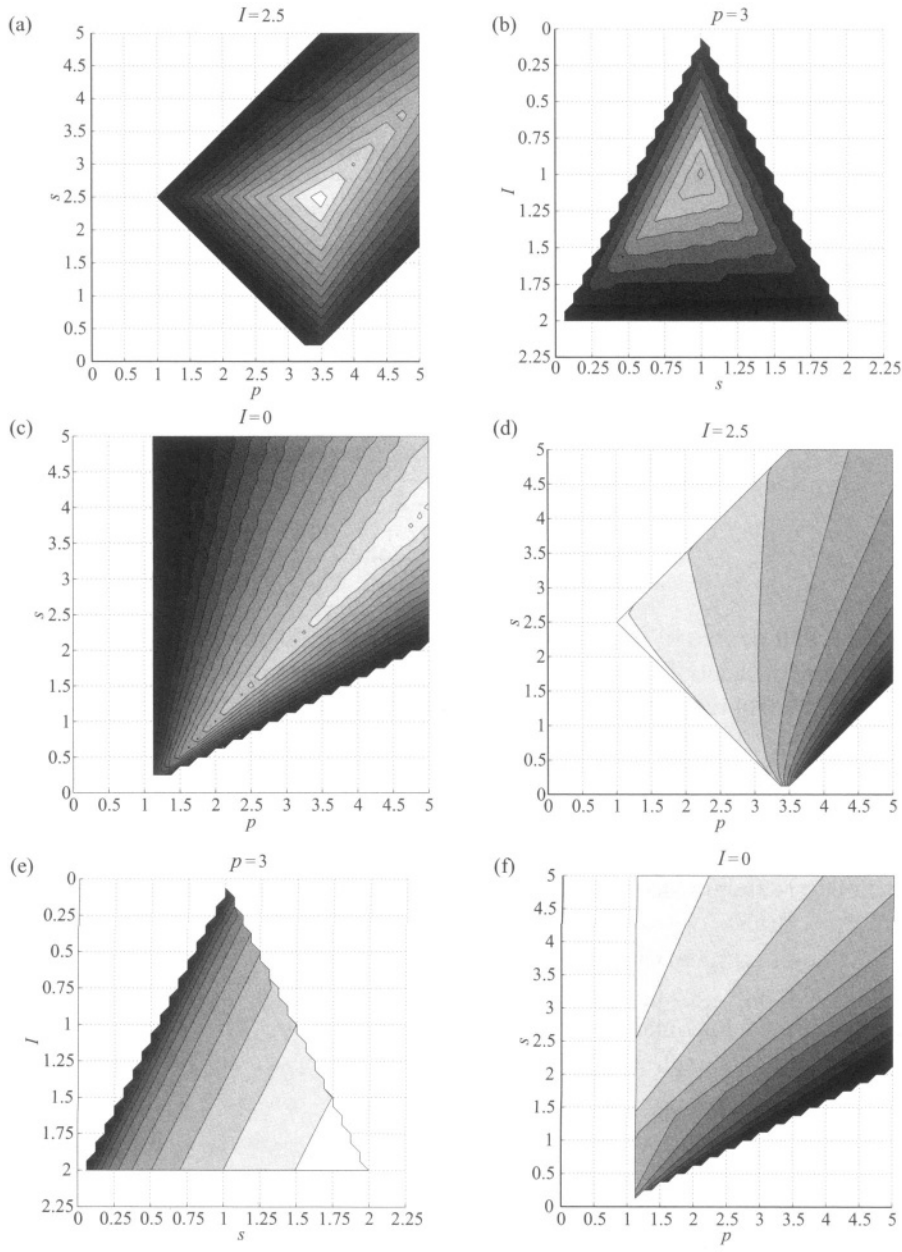


Figure 30.5. Robustness and speed contour plots. The robustness (gray scale) resolution is 2%, and brighter colors depict higher robustness. In the speed plots, brighter colors indicate higher processing speed. (a) SH, robustness. (b) HLD, robustness. (c) CCD, robustness. (d) SH, speed. (e) HLD, speed. (f) CCD, speed.

Table 30.1. Optimum points in Figure 30.5. The optimization for speed yields templates with robustness zero. The optimally robust templates are between 2.3 and 8.3 times slower than the optimally fast ones.

Optimization for Robustness

Task	*Best template*	D_{best}	Δt
SH	$A = [0\ 3.5\ 2.5],\ I = 2.5$	29.0%	0.92
HLD	$A = [1\ 3\ 1],\ I = -1$	16.5%	0.8
CCD	$A = [3.75\ \ 4.75\ \ -3.75]$	30.0%	1.0

Optimization for Speed

Task	*Best template*	Δt_{best}	Δt_{worst}
SH	$A = [0\ 1\ 2.5],\ I = 2.5$	0.16	3.96
HLD	$A = [2\ 3\ 2],\ I = -2$	0.35	2.09
CCD	$A = [1.125\ 5\ \ -1.125]$	0.12	4.16

a sufficient degree of robustness has to be considered as a *constraint* which a template must satisfy, not as a quantity to be optimized.

This new optimization problem may now be formulated as follows:

$$\textit{Find the fastest template with robustness } \mathbf{D} \textit{ and } \|\mathcal{T}\|_1 = \beta$$

where β is a chip-specific upper bound for the template norm. (A larger robustness than $\mathbf{D}$ and/or a smaller L_1-norm than β would be tolerable, but such a template is always slower than the fastest template with a robustness of $\mathbf{D}$ and $\|\mathcal{T}\|_1 = \beta$.)

An approximate solution may be found graphically by investigating the robustness and speed plots as depicted in Figure 30.5, but this is possible only in two dimensions and does not yield accurate results. To solve the problem analytically, we exploit the results from the robustness analysis. From

$$\mathbf{D} = \frac{\gamma}{\|\tilde{\boldsymbol{p}}\|_1 + 1} = \frac{\gamma}{\beta}$$

it follows that $\gamma = \mathbf{D} \cdot \beta$, that is, the safety margin of the template is given by the product of both constraints, namely the robustness and the L_1-norm. It remains to maximize the ratio of some template parameters (depending on the task) under the constraints

$$\min_i (\mathbf{K} \cdot \tilde{\boldsymbol{p}})_i = \mathbf{D} \cdot \beta \tag{30.20}$$

$$\|\tilde{\boldsymbol{p}}\|_1 = \beta - 1. \tag{30.21}$$

Example 30.5 (Connected component detection). Once again, we consider the CCD template prototype

$$\mathbf{A} = \begin{bmatrix} s & \tilde{p}+1 & -s \end{bmatrix}; \quad \mathbf{B} = [0]; \quad \mathbf{I} = 0 \qquad \text{with } 0 < \tilde{p} < 2s$$

In (30.19), we found that the settling time for CCD decreases monotonically with increasing $s/\tilde{p}$. With the coefficient matrix $\mathbf{K}$, $\mathbf{K}\tilde{\boldsymbol{p}}$ evaluates to

$$\mathbf{K}\cdot\begin{bmatrix} s, & \tilde{p}, & -s \end{bmatrix}^t = \begin{bmatrix} -1 & 1 & -1 \\ 1 & -1 & -1 \\ 1 & 1 & 1 \end{bmatrix}\cdot\begin{bmatrix} s, & \tilde{p}, & -s \end{bmatrix}^t = \begin{bmatrix} \tilde{p}, & 2s-\tilde{p}, & \tilde{p} \end{bmatrix}^t$$

Expecting that our template will turn out to be rather fast, that is, $s > \tilde{p}$, the minimization yields $\gamma = \tilde{p}$. Hence, $\tilde{p} = \gamma = \mathbf{D}\cdot\beta$ is already determined. By inserting $\|\tilde{\boldsymbol{p}}\|_1 = 2s + \tilde{p}$ into (30.21), we obtain $s = \frac{1}{2}(\beta - 1 - \tilde{p}) = \frac{1}{2}(\beta(1-\mathbf{D}) - 1)$.

If, for example, a CNN chip has parameter perturbations of up to 10% and an L_1-norm of 10 ($\mathbf{D} = 0.1$ and $\beta = 10$), the fastest template meeting these requirements is

$$\mathbf{A} = \begin{bmatrix} 4 & 2 & -4 \end{bmatrix} \quad \mathbf{B} = [0] \quad \mathbf{I} = 0$$

with a settling time of $T_S = N \log \frac{4}{3}$. The commonly used CCD template A = [1 2 — 1], by comparison, settles at $T_S = N \log 4$, which is almost 5 times slower. On the other hand, its robustness is 25%, but such a high degree of robustness is rarely demanded.

30.3.4. Robust CNN Algorithms for High-Connectivity Tasks

The degree of connectivity of a standard CNN template and its degree of robustness are related. The higher the connectivity of a template, the more sensitive it is to parameter variations. For some types of tasks, which require a high degree of connectivity, for example, corner and edge detection, the achievable robustness is not sufficient for correct operation on an analog chip. Nevertheless, they can be realized in a highly robust manner by using an *algorithmic approach,* rather than a single template; the technique presented here was proposed by Mirzai and Lím [21]. Such algorithms comprise several CNN templates with a low degree of connectivity, combined with logical operations. The resulting approach can be viewed as another class of a speed–sensitivity trade-off.

We assume that the accuracy and programing range of the CNN hardware is limited so as to make it impractical to use templates which consider five

or more input cells. Hence, only templates with connectivity lower than five are used. Moreover, we prefer CNN transients over logical operations. The main reason for doing so is the assumption that a CNN processor is probably not designed to rapidly perform many logical operations. A CNN processor is primarily an *analog array,* rather than an array of gates, logic circuits, DSPs or a cellular automaton, so it is reasonable to assume that the digital logic in each cell and its control circuits are optimized for small circuit size, which implies a speed penalty [22].

Any given task of the type considered here can be decomposed in numerous ways; the decompositions suggested here are not optimal in the sense of switching algebra, nor do they minimize the number of CNN transients of logical operations – rather they make reasonable use of the capabilities of a standard CNN. Note that the procedures herein are not applicable to propagation-type tasks, they are restricted to uncoupled or *Boolean* CNN operations. Templates suggested for performing edge or corner detection in one CNN run, for example, in [23,24], have, by nature of the task, a high degree of connectivity, which limits the degree of attainable robustenss severely. The algorithms presented here inherit the robustness of the individual component CNN operations, allowing the entire processing task to be performed in a robust manner, albeit at the cost of speed.

Template classes. For the decomposition, a suitable set of *basis templates* has to be defined. Similarly to linear algebra, where a set of vectors may be a *basis* for a vector space, a set of *basis templates* is required to be universal in the sense that all Boolean functions can be constructed by subsequent application of basis templates and logic functions.

A straightforward choice are the *atomic* or *primitive* templates, which have only one single non-zero entry in the **B** template. These template are arbitrarily robust, but they reduce the CNN to a logic gate, acting essentially as a one-of-nine selector. A more reasonable choice is the set of Class **I**, **II** and **III** templates. Each class provides an elementary operation, which can be "rotated" as required to operate in all relevant directions. In conjunction with logical operations, these templates will allow us to develop algorithms for CNN applications. The class is identified by an upper case Roman number, and the rotation is specified by a geographic subscript, for example, NN, NW, etc.

Class I $\mathbf{I}_{WW}$ is defined by the following mapping of the initial cell configurations onto the corresponding desired outputs:

Input	● ● ○	○ ● ●	● ● ●	○ ● ○	* ○ *
Output	○ ● ○	○ ○ ●	○ ○ ●	○ ○ ○	* ○ *

where $*$ is a "don't care" symbol. An optimally robust template for this operation is

$$A = [2] \quad B = [1 \;\; 0 \;\; -1] \quad I = -2$$

Similarly, we define and find the two template classes:

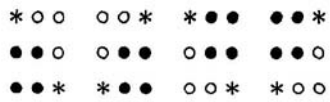
Class II: $\mathbf{II}_{WW}$: $A = [2]$ $B = [-1 \;\; 0 \;\; -1]$ $I = -2$

Class III: $\mathbf{III}_{WW}$: $A = [2]$ $B = [1 \;\; 0 \;\; 1]$ $I = -2$

The robustness for all three template classes is $1/6 \approx 16.7\%$. The settling time is $\log 3 \approx 1.1$. Note that these templates may be scaled. A scaling factor of 2 would result in a robustness of $2/11 \approx 18.2\%$ and a settling time of only $\frac{1}{2} \log 3$.

As an example, let us study the convex corner detector.

Example 30.6 (Convex corner detection). The identification of "convex" corners is a task that involves the cell's entire neighborhood. The nearest neighborhood of a *convex comer* can be characterized as one of the following configurations:



where, in each case, the corner itself is the center cell, and $*$ denotes a "don't care" cell. With this definition, the convex corner detection problem cannot be solved by a single CNN operation, since it belongs to the linearly non-separable class. For such tasks, there is no choice but to resort to a decomposition algorithm.

If, however, we define a convex corner more "generously" to be a black cell with 5 or more white neighbors, there is a single-template solution:

$$\mathbf{A} = [1] \quad \mathbf{B} = \begin{bmatrix} -1 & -1 & -1 \\ -1 & 4 & -1 \\ -1 & -1 & -1 \end{bmatrix}, \quad \mathbf{I} = -5 \tag{30.22}$$

It requires a bias value as high as 5, which may not be available on all chips. More disadvantageous is, however, its low robustness of merely $1/(1+4+8 \cdot 1+5) = 1/18 \approx 5.6\%$. The settling time is 2.

Using the basis templates, we can derive a CNN algorithm to achieve higher robustness.

To extract the convex corner, for example, in the case of



we apply the templates $\mathbf{I}_{WW}$, $\mathbf{I}_{SS}$ and $\mathbf{I}_{SW}$, in turn, to the input image. Denote the respective outputs as $\mathbf{O}(\cdot)$. Next we perform the following logical[1] operation:

$$\mathbf{O}(\mathbf{I}_{WW}) \text{ AND } \mathbf{O}(\mathbf{I}_{SS}) \text{ AND } \mathbf{O}(\mathbf{I}_{SW}).$$

The only pixels that remain black are convex corners of the type depicted above. To obtain the other convex corner configurations we repeat the procedure with appropriately rotated templates, and OR the results:

$$\mathbf{O}(\mathbf{I}_{WW}) \text{ AND } \mathbf{O}(\mathbf{I}_{SS}) \text{ AND } \mathbf{O}(\mathbf{I}_{SW})$$
$$\text{OR}$$
$$\mathbf{O}(\mathbf{I}_{NW}) \text{ AND } \mathbf{O}(\mathbf{I}_{NN}) \text{ AND } \mathbf{O}(\mathbf{I}_{WW})$$
$$\text{OR}$$
$$\mathbf{O}(\mathbf{I}_{EE}) \text{ AND } \mathbf{O}(\mathbf{I}_{SS}) \text{ AND } \mathbf{O}(\mathbf{I}_{SE})$$
$$\text{OR}$$
$$\mathbf{O}(\mathbf{I}_{NN}) \text{ AND } \mathbf{O}(\mathbf{I}_{EE}) \text{ AND } \mathbf{O}(\mathbf{I}_{NE})$$

Figure 30.6 shows the complete convex corner CNN algorithm.

Every Boolean function can be decomposed in a similar way. The decomposition algorithm is described in [21].

One-step vs algorithmic processing. The two alternative processing methods – a non-robust single CNN template with high connectivity, or an algorithm based on elementary operations with low connectivity – can be viewed as a complexity sensitivity speed trade-off. The algorithms require some number of intermediate storage registers, whereas a single-step template requires none. The registers, however, store only bipolar data, that is, essentially digital storage, so that they present a minimal increase in complexity. Depending on how intermediate results are stored, the convex corner algorithm requires about eight CNN transients, four 3-input ANDS and one 4-input OR. The convex corner algorithm would be substantially slower than a single step template, *provided that the CNN processor has the accuracy to perform the respective operation with a single template.* However, the circuit complexity required to achieve high accuracy may be prohibitive, so it may, in fact, be impossible to run the single step template on analog CNN hardware.

If it were possible to run a fully connected template, the speed penalty is not as severe as one might assume at first sight. By scaling the class templates by a

[1] Black (+1) corresponds to the boolean value "TRUE", for example, (+1) AND (+1) = (+1); all other AND combinations yield — 1. The operations are carried out pixel-wise.

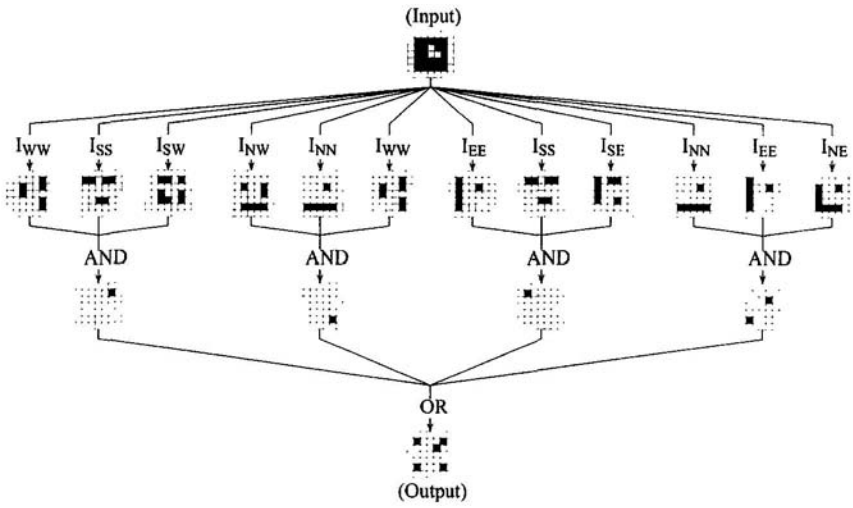


Figure 30.6. Convex corner detection example.

factor of 3, the parameters are still in a reasonable range and the settling time drops to $\frac{1}{3}\log 3 \approx 0.37$, which implies that one run requires less than one-fifth of the time of a single fully connected corner detection template. Hence, the speed penalty for the algorithmic approach is not more than a factor of 2.

An intermediate point in the trade-off exists. For example, the first part of algorithmic convex corner detection (three CNN transients, and one 3-input AND), can be replaced by a single CNN transient involving a template with a connectivity of 9:

$$\mathbf{A} = [a] \quad \mathbf{B} = \begin{bmatrix} 0 & -c & -c \\ c & b & -c \\ c & c & 0 \end{bmatrix} \quad \mathbf{I} = z \tag{30.23}$$

Convex corner detection can then be performed using, in total, four CNN transients and one 4-input OR. The intermediate algorithm may or may not be sufficiently robust for a given implementation. A suitable template for this case would be $a = 2$, $c = 1$, $b = 0$, and $\mathbf{I} = -6$. Its robustness is $1/(2+6\cdot 1+6) \approx 7\%$, which is 60% less than the class templates.

30.3.5. Concluding Remarks

In this section, we have analyzed the robustness and the settling time of standard cellular neural networks. Different approaches were used for the two main classes of CNNs, the uncoupled and the propagation-type class. Furthermore, the mutual influence of processing speed and template robustness has been studied.

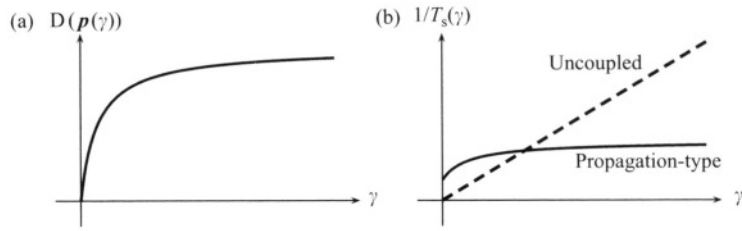


Figure 30.7. Robustness and processing speed as a function of a scaling parameter γ. (a) Robustness (uncoupled and propagation-type-templates), and (b) processing speed.

Clearly, a joint optimization for both speed and robustness is desirable. This is possible for uncoupled templates, where template scaling results in both proportionally higher speed *and* monotonically increased relative robustness (Figure 30.7(a)).

For propagation-type templates, the fastest templates turn out to have zero robustness – hence, there is a trade-off between speed and robustness. Noting that it is not sensible to design a template with a robustness which is higher than the relative inaccuracy of a CNN chip, it is advisable to concentrate on the processing speed (instead of balancing speed versus robustness), and to regard a *sufficient* degree of robustness as a *constraint* in the optimization process. The problem is now *to find the fastest template with a robustness of D (at least) and a (maximum)* L_1*-norm of* β. By means of the analysis of the robustness and the settling time, it is shown that this general class of problems can be solved in a straightforward manner.

The same idea of considering a sufficient robustness as a constraint applies to the decomposition of high-connectivity templates into simpler basis templates. In this speed–robustness trade-off, several solutions of different complexity are possible and may be selected according to the accuracy of the CNN hardware.

One of the major advantages of the standard CNN cell compared to more universal and more complex cells is the fact that there exists a direct and analytical template design method. Hence, no learning or training process is involved.

30.4. Universal CNN Cells and their Trade-Offs

30.4.1. Preliminaries

An ultimate goal in analog design is to pack as much functionality as possible into a circuit, given the constraints of a technology. In this section, the problem of designing nonlinear circuits (cells) that are capable of implementing *arbitrary* Boolean functions with n inputs is considered, with an emphasis on

the trade-offs between different conflicting features of such cells. The application of such a circuit (herein referred to as a *universal CNN cell* [25]) is to expand the functionality of the standard CNN cells to arbitrary (including linearly not separable) Boolean functions while solving the trade-offs between certain quality attributes.

Ideally, the resulting cell design should be fast in terms *of processing speed* and, at the same time, it should be *compact* and *robust.* It is also desirable to use a simple and efficient *design or learning algorithm* to determine the cells' parameters when a specific Boolean function is given. In practice, however, it is not possible to optimize simultaneously all the attributes mentioned above. Therefore it is important to consider trade-offs between *quality attributes* such as:

- *Universality or functional versatility*
- *Compactness* or number of cells per area
- *Robustness* with respect to changes in the parameter space
- *The complexity of the learning/design algorithms*
- *Processing speed*

In a digital technology, the most compact realization of the *universal CNN cell* requires a digital multiplexor, where its 2^n data inputs are used to specify the *arbitrary* Boolean function, and its n selection inputs are used as the cell inputs [26]. Such an arrangement, the most compact in digital technology, leads to a circuit complexity of the order $O(2^n)$, which corresponds to relatively *low cell density* in a cellular neural network. In this case the *compactness* was traded off against a good *robustness,* which is characteristic for digital systems.

This section introduces several *analog* universal CNN cells and their trade-offs. A general mathematical formula for such cells is $y = \text{sgn}(w(\boldsymbol{u}, \boldsymbol{G}))$, where w is a nonlinear function called a *discriminant,* $\boldsymbol{u}$ is the (binary) input vector (for usual standard CNNs its size is 9), and $\boldsymbol{G}$ is a vector of parameters (biologically inspired, called a *gene* [4]) determining the specific Boolean function realization. In the case of uncoupled standard CNNs, the gene $\boldsymbol{G}$ is represented by the B template. For a *universal CNN cell,* each Boolean function corresponds to an analog *gene,* which is almost never a unique point in the parameter space. In fact, the parameter space is partitioned into sub-domains separated by *failure boundaries* [4] and each sub-domain corresponds to a Boolean function realization. However, some points lead to less robust realizations, namely the points situated in the neighborhood of the failure boundaries (several examples are given in Section 13.4.4).

Different analog technologies can be used to implement the nonlinear discriminant function w; an interesting and convenient technique, presented in

Section 30.4.5, exploits the non-monotone characteristic of the resonant tunneling diodes (RTDs). The discriminant function w replaces the linear term corresponding to the **B** template in the standard CNN cell. For an uncoupled **A** template with the central element $a_{00} = 1$, the ordinary differential equation corresponding to the circuit implementation of the CNN cell C_{ij} is:

$$\dot{x}_{ij} = -x_{ij} + f\left(x_{ij}\right) + w\left(\boldsymbol{u}_{ij}, \boldsymbol{G}\right) \tag{30.24}$$

$$y_{ij} = f(x_{ij}) = \frac{1}{2}\left(\left|x_{ij}+1\right| - \left|x_{ij}-1\right|\right) \tag{30.25}$$

where x is the state variable and y is the output. As shown in [20], this equation converges to an equilibrium point after a certain settling time, which depends on the implementation technology, and the output of the cell at equilibrium is $y_{ij} = \mathrm{sgn}(w(\boldsymbol{u}_{ij}, \boldsymbol{G}))$. In the current 0.5 micron CMOS technologies the settling time is of the order of tens of nanoseconds.

For a theoretical investigation, it is convenient to express w as a composition of *piecewise-linear* functions. The design problem is to find a tractable expression of w so that various trade-offs between the quality attributes mentioned above can be dealt with depending on the specific application of the cell.

Several universal CNN cell architectures have been proposed, each having its own trade-offs profile. In what follows three *universal CNN cells* architectures and their major trade-offs will be presented in Section 30.4.2, Section 30.4.3. and Section 30.4.4. A circuit for implementing the most compact of the architectures using a technology based on vertical integration of resonant tunneling diodes and FETs [27] is presented in Section 30.4.5, and, in the same section, some technological trade-offs related to such implementations are discussed.

30.4.2. Pyramidal CNN cells

Architecture. The *pyramidal CNN cell* architecture (Figure 30.8), is one alternative to provide universality. For a complete description the reader is referred to [28]. In this case, the discriminant function w is given by a weighted combination of the outputs of $m = 2^n$ pyramidal basis functions,

$$b_j = r\left(1 - \frac{\lambda}{2}\sum_{i=1}^{n}\left|u_i - a_{ji}\right|\right),$$

each being centered on one of the m possible Boolean input vectors, herein represented by the coefficients $a_{ji} \in \{-1, 1\}$. The parameter λ controls the radius of each basis function, and is set to 1 for binary processing. The function $r(x) = 0.5\,(x + |x|)$ is the standard "half-wave" rectification function. The discriminant function is given by $w = \sum_{j=1}^{m} b_j g_j$, where each element of the

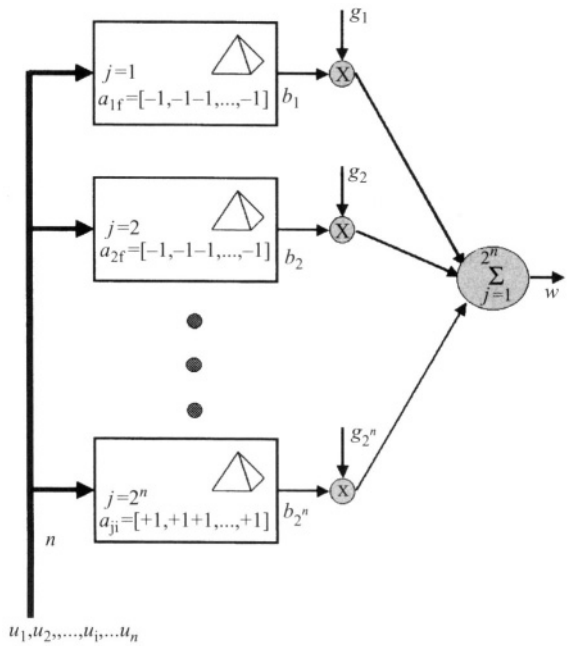


Figure 30.8. The architecture of the pyramidal CNN cell.

gene vector $\boldsymbol{G} = \{g_j\}_{j=1,\ldots,m}$ corresponds to the desired output of the Boolean cell when the binary input applied is the vector $\{a_{ji}\}_{i=1,\ldots,n}$. In other words, g_j is identical to the bit j (– 1 or 1) of the Boolean function to be represented.

Trade-offs. The cells' *compactness* (which is proportional to the number of absolute value function devices) is traded off against high *robustness, functionality,* and *simplicity in training or design.* In fact, this architecture requires no effort in designing its parameters, they are simply copied from the truth table of a given Boolean function. It is interesting to note that the gene parameters are *not* restricted to the binary values $\{-1, 1\}$ but can also have continuous values. For binary information processing, only their sign is determining the Boolean function realization, thereby introducing a high degree of robustness. The circuit complexity of this cell is of the order $O(2^n)$, like in the digital case. In contrast to a digital universal CNN cell, however, the pyramidal CNN cell is capable of processing continuous signals; for example, several applications in adaptive gray scale image filtering have been demonstrated for $\lambda = 2/n$. In this case, the gene parameters g_j can be determined by simple perceptron learning, provided that a representative set of input–output samples of the signal processing problem is available. The simulations done for several image

processing problems confirm that the gene parameters are indeed robust, no major change in the quality of the processed images is observed even if the tolerance of the g_j parameters is in the range of 25%. A trade-off between the *processing speed* and the *compactness* was also considered in [28] by calculating the weighted sum $w = \sum_{j=1}^{m} b_j g_j$ sequentially, in m time steps. This solution is particularly useful for those particular problems where a large number of the gene parameters is almost 0. In this case, the number of devices per cell reduces to $O(n)$, but the processing time increases proportionally with the number of non-zero g_j coefficients and, in general, is in the order of $O(2^n)$.

30.4.3. Canonical Piecewise-linear CNN cells

Characterization and architecture. The *canonical piecewise-linear CNN cell* (Figure 30.9) was introduced to improve the *compactness* while maintaining the universality. A complete description and characterization of this cell is given in [25]. In this case, the gene vector is not formed of independent parameters, each being associated with one bit of the Boolean function. Instead, one bit change in the desired Boolean function will imply a change in all parameters defining the gene, similar to the case of the standard CNN cell. In fact, compared to the *pyramidal universal CNN cell,* the number of absolute value functions per cell is reduced. However, for this cell, the trade-off between *compactness* and *the complexity of the learning/design algorithm*

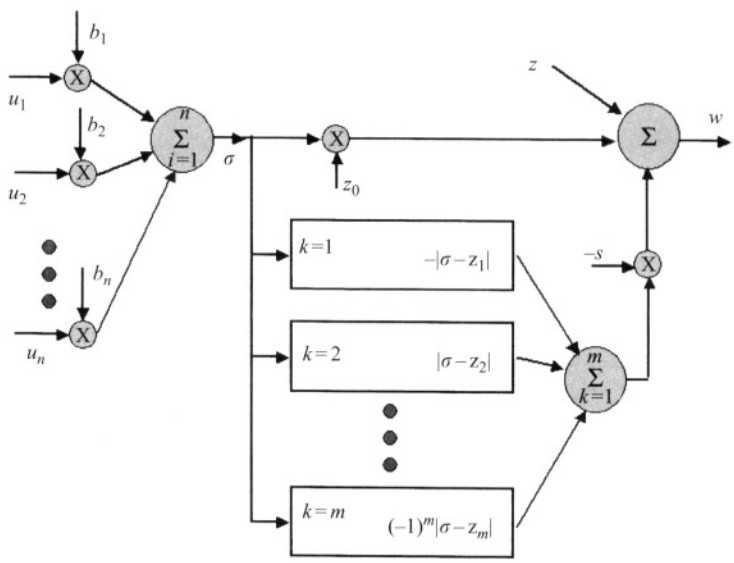


Figure 30.9. The piecewise-linear CNN cell.

has to be considered. While a straightforward design solution always exists, this solution is not necessarily optimal and, therefore, may lead to less compact implementations. If an effective optimization algorithm is used, compactness can be dramatically improved, but often at the expense of a more complex learning/design algorithm.

The central idea of this architecture is to replace the linear discriminant used in the standard CNN cell with a *canonical piecewise-linear* function $w(\sigma)$, where $\sigma = \sum_{i=1}^{n} b_i u_i$ is a scalar variable called an excitation. Here, b_i are gene parameters corresponding to the B template of the standard CNN cell. The above formula can be regarded as a *projection* of the 2^n vertices of the hypercube representing the Boolean input space onto a *scalar projection tape* represented by the excitation variable σ. Depending on the specific Boolean function, when the projection tape is scanned from $-\infty$ to $+\infty$, a number m of transitions are found on the tape between those values of σ corresponding to $y = +1$ and those values of σ corresponding to -1. The exact number of transitions depends on two factors: the specific Boolean function to be represented by the cell, and the values of the b_i parameters forming an *orientation vector.* While a *linear* discriminant $w(\sigma) = v$ can solve only one transition, a canonical piecewise-linear discriminant $\sigma w = z + z_0\sigma - s\sum_{k=1}^{m}(-1)^k|\sigma - z_k|$ can solve any number $\mathrm{tr} = m - 1$ transitions generated by an arbitrary Boolean function and an arbitrary orientation vector. By "solve" here we mean that the sign of w follows the desired output of the cell for each possible input vector. In this case, the *gene* is formed by the set of parameters $\{s, z, z_k, b_i\}_{\substack{k=1,\ldots,m \\ i=1,\ldots,n}}$.

Trade-offs. An interesting trade-off between the complexity of the design procedure and compactness has to be considered. In [25], it was shown that the simplest design procedure is to choose a *default orientation vector* $\boldsymbol{b} = [b_1, \ldots, b_n] = [2^{n-1}, \ldots, 2^0]$. Then, depending on the specific Boolean function, the transition points t_k on the projection tape can be easily determined by analytical formulae and, similarly, the remaining set of parameters $\{s, z, z_k\}_{k=1,\ldots,m}$. This convenient design procedure, which can be applied for any Boolean function, has the disadvantage of leading to a non-optimal solution in terms of the number of absolute value functions. In order to optimize the solution one should choose a powerful optimization algorithm, capable of determining the optimal *orientation vector* b^*. This is defined as the set of parameters b_i leading to a minimum number of transitions on the projection tape and to the best possible robustness (measured here as the minimal distance between a transition point and a projection of a vertex). Only for the special class of totalistic Boolean functions (where the inputs can be interchanged arbitrarily), this optimization task can be implemented in a straightforward manner by choosing all $b_i = 1$. In general, it requires a complex and time-consuming

algorithm. Because the error surface induced by the objective function is usually highly rugged, with many local extrema, gradient-based algorithms are not efficient. Instead, Simulated Annealing or Genetic Algorithms are a better alternative. The time needed to run such algorithms successfully increases dramatically with the number n of parameters, therefore, in practice, they can run efficiently on general-purpose computers for a relatively small number of inputs (e.g. maximally 5) only.

Example. For the Boolean function Parity4[2], two realizations of the *canonical piecewise-linear cell* are presented in Figure 30.10. The first one is straightforward, using the default orientation vector $\boldsymbol{b} = [8, 4, 2, 1]$ while the other is optimized for the orientation vector $\boldsymbol{b} = [1, 1, 1, 1]$. In the second case, the number of transitions is minimal, and only 3 absolute value functions are needed. Compared to the 9 absolute value functions used in the default solution, the optimal solution significantly increases the compactness.

For an arbitrary, random Boolean function, the *default orientation vector* was found experimentally to lead to a number m of transitions (and implicitly the same number of absolute value functions) bounded by a limit of the order $O(2^n)$. Additional optimization of the *orientation vector* may improve

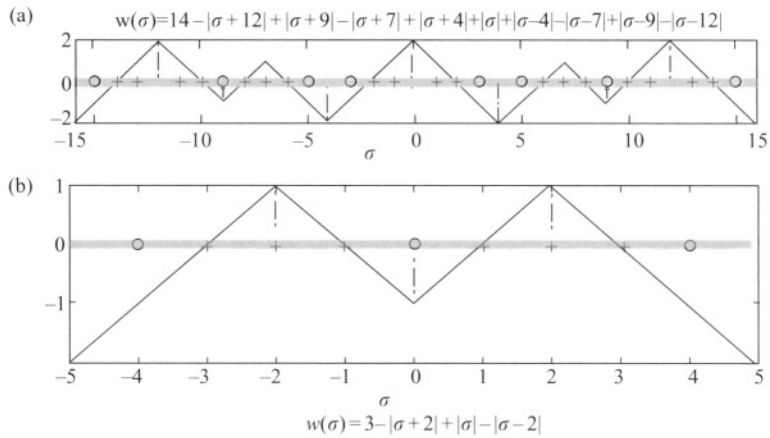


Figure 30.10. Two canonical piecewise-linear universal CNN cell realizations for the Boolean function Parity 4; (a) The *default orientation* $b = [8, 4, 2, 1]$ leads to a non-optimal projection tape with 10 transitions; (b) The optimal orientation $b^* = [1, 1, 1, 1]$ leads to only 4 transitions. The circles shown on the projection tape correspond to an output $y = -1$ of the cell.

[2] The "Parity 4" cell returns +1 if and only if there is an odd number of inputs (coming from north, south, east and west neighboring cells) in the +1 state. Otherwise, the cell returns –1.

this bound, so that for a randomly selected Boolean function the *canonical piecewise-linear CNN cell* has less devices than the *pyramidal universal CNN cell.* As mentioned above, more compact solutions can be obtained by optimizing the orientation vector $\boldsymbol{b}$. It is also interesting to note that m = 0 corresponds to the standard CNN cell.

30.4.4. The Multi-Nested Universal CNN Cell

Architecture and characterization. The *multi-nested universal CNN cell* (Figure 30.11) maintains universality while optimizing *compactness* with a dramatic reduction in the number of devices per cell to the order of $O(n)$, instead of $O(2^n)$ for the digital realizations and for the *universal CNN cells* described above. It relies on a novel discriminant function $w(\sigma)$. The *multi-nested* discriminant is a piecewise linear function where the number m of absolute value functions and the additional parameters increase only with $\log_2$ (tr), where tr represents, as in the case of the *canonical piecewise linear* cell, the number of transitions on the *projection tape.* A detailed theoretical description of the multi-nested CNN cell is given in [25]. It is conjectured that any Boolean function can be realized using a multi-nested discriminant with only $m = n - 1$ absolute value functions and $m + 1 = n$ additional z_k parameters. The expression of the *multi-nested* discriminant function is given by:

$$w(\sigma) = s\,(z_m + |z_{m-1} + |\ldots + z_1 + |z_0 + \sigma|||) \tag{30.26}$$

where σ is defined as in the case of the *canonical piecewise-linear universal CNN cell;* namely, $\sigma = \sum_{i=1}^{n} b_i u_i$, and $s \in \{-1, 1\}$. The main idea behind choosing this discriminant function is that by having a properly chosen set of parameters z_k, $k = 0, \ldots, m$, the number of roots (i.e. transitions on the

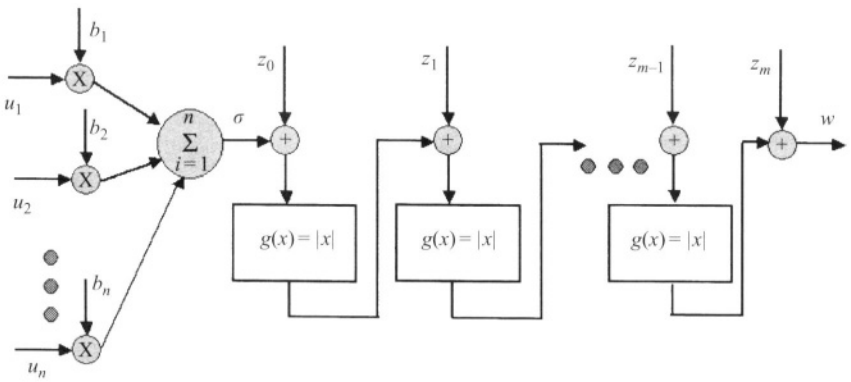


Figure 30.11. The architecture of the multi-nested universal CNN cell.

projection tape) of the equation $w(\sigma) = 0$ doubles with each additional level of "nesting". In contrast, the *canonical piecewise-linear CNN cell* requires an additional absolute value function and z parameter for each additional root. In a practical realization, any device which has a non-monotonic input–output characteristic (represented by the function $g(\cdot)$) can replace the absolute value function in the above formula with the same effect. For example, the non-monotone characteristic of the resonant tunneling diode can be used to build a compact universal CNN circuit, as shown in Section 15.3.5.

Trade-offs. Having a very compact architecture, the *multi-nested universal CNN cell* bears its own trade-offs. First, *compactness* is traded off against a *complex design/learning algorithm.* Except for a very limited class of Boolean functions (the Parity functions with n inputs), there is no direct analytical solution for finding the gene $G = \{s, z_k, b_i\}_{\substack{i=1,\ldots,n \\ k=1,\ldots,m}}$ of an arbitrary Boolean function. Therefore, the use of an efficient optimization algorithm is mandatory; the unavoidable optimization problem is usually hard, and time-consuming. It turns out that a combination between an exhaustive random search through the parameter space and a directed random search gives the best results for small number of inputs. Note that for $n = 4$, there are $2^{2^n} = 65,536$ possible Boolean functions. It takes about 2 min to find the gene for a specified Boolean function using a stochastic optimization algorithm. If the goal is to establish a gene for each of these functions, in this way, it will take a very long time. Instead, by searching randomly through the parameter space one can rapidly identify the genes for a large part of the functions and then apply the optimization algorithm only to the remaining ones.

Another trade-off of the *universal CNN cell* is the one between *compactness* and *robustness,* particularly for a large numbers of inputs. *Compactness* is a feature conflicting with *robustness.* The more compact a cell is, the less robust it will be. The reason is that any Boolean function with n inputs requires $N = 2^n$ bits to be precisely specified. A compact universal cell has to preserve this amount of information in its definition and, therefore, must distribute it among the cell parameters. For example, an arbitrary Boolean function with 9 inputs (e.g. the standard local logic for two-dimensional CNNs) requires 512 bits to be defined. For the case of the *multi-nested universal CNN cell* where universality is achieved with only $2n + l$ parameters, each parameter requires at least $\frac{512}{19} \approx 27$ bits! It is impossible to achieve such a resolution in analog technology. However, if the number of inputs is smaller, e.g., $n = 6$, the same calculation will lead to an average of $\frac{64}{13} \approx 5$ bits per parameter, which is acceptable. At the opposite extreme, the pyramidal universal cell requires 2^n parameters: In this case, since each parameter is associated with only 1 bit of information, the realization is maximally robust but clearly not compact at all.

Let us now consider the *robustness* versus *versatility* trade-off. The multi-nested architecture allow us to control the parameter m (the number of "nests") which, in turn, controls the number of Boolean functions that can be realized with a given architecture. The choice of a small m (at the limit, m — 0 corresponds to the standard CNN cell) leads to a better robustness, but in this case versatility is sacrificed, since only a limited set of the Boolean functions with n inputs can be realized.

Example. Let us consider two *multi-nested CNN cells* with 9 inputs. Both of them are not universal since in their definition $m < 8$ nests and only two parameters λ_1, λ_2 were selected to visualize the failure boundaries in a two-dimensional plane. The remaining set of parameters is kept constant, $a = b =$ 1.5, and c — 0.75. For both examples the goal is to visualize the parameter space profile, the parameter space being restricted to the square $(\lambda_1, \lambda_2) \in [-1.5, 1.5] \times [-1.5, 1.5]$. Let us consider a single nested $(m = 1)$ cell C1 having the following discriminant function:

$$w = a - \left| b + (1 + \lambda_1) u_1 + (1 + \lambda_2) u_2 + cu_3 + \sum_{i=4}^{9} u_i \right| \qquad (30.27)$$

Its corresponding partitioning of the parameter space is depicted in Figure 30.12(b), where each segment represents *a failure boundary* separating different domains, each one associated with a specific Boolean function. In this case, there are 85 distinct Boolean functions corresponding to the same number of sub-domains within the parameter space.

The zero-nests cell (CO) is obtained by removing the absolute value function $(m = 0)$ in C1 and keeping the rest unchanged. Its discriminant function is:

$$w = a - b - (1 + \lambda_1)u_1 - (1 + \lambda_2) u_2 - cu_3 - \sum_{i=4}^{9} u_i \qquad (30.28)$$

Figure 30.12(a) displays the partitioning where each segment represents a *failure boundary* separating different domains, each one associated with a specific Boolean function. In this case, there are 29 distinct Boolean functions corresponding to the same number of sub-domains within the parameter space.

Let us observe first that there is a trade-off between versatility and the number of absolute value function devices. While C1 (with $m = 1$) generates a partition of the parameter space in 85 sub-domains, there are only 29 distinct sub-domains in the case of cell C0 (where $m = 0$). C1 is more versatile than CO but requires an additional absolute value function device. As a rule, the more "nests" it has, the more versatile the cell is. At the limit, when the number of nests is large enough, the entire set of Boolean functions can be realized. For example, in the case of $n = 4$ inputs, it was found [25] that 3% of the entire set

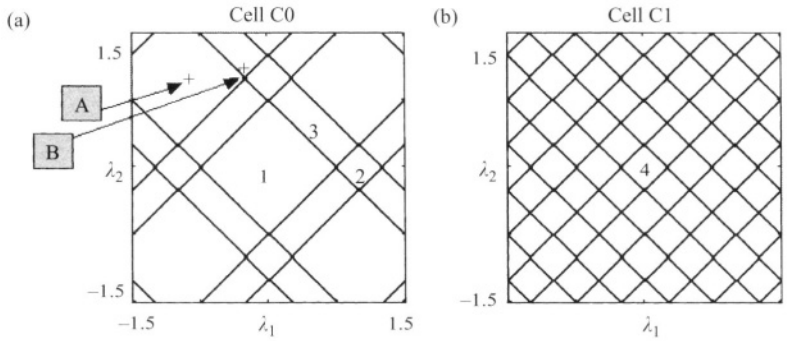


Figure 30.12. The influence of the number of nests m in a muti-nested cell on the number of Boolean function realizations and their robustness: (a) Partitions of the cell parameter space for $m = 0$, cell C0; (b) Partition of the cell parameter space for $m = 1$, cell C1.

of 65,536 Boolean functions can be realized with $m = 0$ nests, 21% of them require $m = 1$ nests, a large majority of 61% require $m = 2$ nests and only 15% of the Boolean functions require the maximum number $m = 3$ of nests.

Let us now consider the *robustness* versus *versatility* trade-off. The robustness associated with a Boolean function realization can be estimated from the area and the shape of its corresponding sub-domain. First, let us observe that in general, different Boolean functions have realizations with different degrees of robustness, This situation is illustrated in Figure 30.12(a) representing the partition generated by the cell CO. The sub-domain labeled "1" in this figure, allows more robust realizations than the sub-domain labeled "2". Moreover, if only one parameter changes, the sub-domain labeled "3" has the same robustness as the sub-domain "2", although its area is larger. On average, the cell realizations of the more versatile cell C1 are less robust than the realizations of cell CO since all 85 Boolean functions associated with Cl cover the same small square area in the parameter space. In the case of CO, however, 5 Boolean functions correspond to largest squares and therefore have larger robustness. More sophisticated shapes of the sub-domains corresponding to different Boolean function realizations are obtained in higher dimensional parameter spaces, however, the same rules apply for the above-mentioned trade-offs.

A practical estimate for the robustness of a cell realization is given by $\rho = \min(|w(\boldsymbol{u}_j)|)$, where $\boldsymbol{u}_j$ is the set of all binary input vectors. The smaller ρ, the less robust is the cell. This definition should be interpreted in the following sense: If, for a given gene (or parameter point) one input vector produces a discriminant function $w \approx 0$, a minor perturbation in its parameters is likely to cause a sign change (which is equivalent to crossing one failure boundary) and therefore the cell will fail to represent the original Boolean function. On

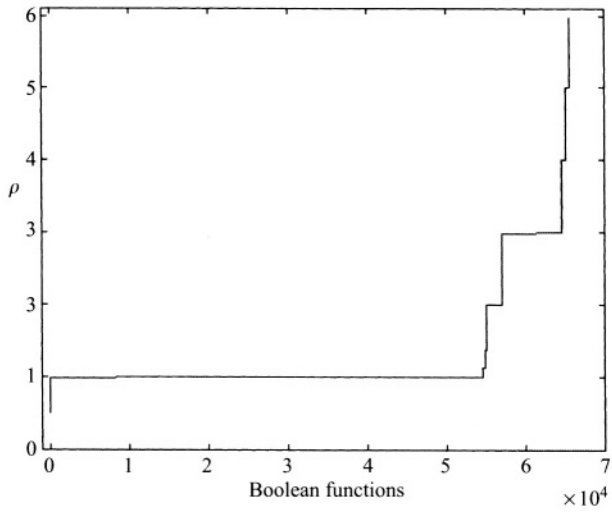


Figure 30.13. Robustness distribution among the 65,536 multi-nested universal CNN cell realizaions of the Boolean functions with $n = 4$ inputs. In all cases the number nests is $m = 3$.

the contrary, if for any input, the absolute value of the discriminant function is relatively far from 0 (e.g. the parameter point is far from the failure boundary) it is unlikely that a change in cell parameters will lead to a crossing of the failure boundary. For example, both parameter points "A" and "B" in Figure 30.12(a) lead to the realization of the same Boolean function. However, the robustness of the parameter point "A" with $\rho = 0.75$ is optimal, while the robustness of the parameter point "B" is close to 0.

The robust realizations for all 65,536 Boolean functions with $n = 4$ inputs were determined [25] using several optimization techniques. Figure 30.13 displays the distribution of the robustness estimator ρ for all realizations. Each b and z parameter of the cell varies within the range $[-61, 50]$.

Observe that not all realizations are equally robust (most of them have $\rho \simeq 1$), and the distribution has a staircase shape with a few number of steps, corresponding to a finite set of distinct polyhedrons induced by the discriminant function in the cell parameter space. When the cells are not optimized for robustness or when the absolute value function non-linearity is implemented with a realistic device (e.g. using a resonant tunneling diode), the robustness distribution exhibits a much larger number of levels.

The addition of one or more nests has an influence on the processing speed, therefore trade-offs between processing speed and versatility should also be studied. A higher versatility necessitates a large enough number of nests, but, on the other hand, each addition of a nesting device (a practical circuit example

is given in the next sub-section) decreases the processing speed. A practical application of the nesting principle is given in the next sub-section.

30.4.5. An RTD-Based Multi-Nested Universal CNN Cell Circuit

The idea of nesting non-monotone functions to obtain a compact and versatile CNN cell is more general and is applicable not only to absolute value functions but to any non-monotone function. For example, the current–voltage characteristic of the resonant tuneling diode [29], which can be approximated with a three segment piecewise-linear function (Figure 30.14) is an excellent candidate for such a function.

The *I–V* characteristic of the RTD can be modeled by the following piecewise linear function (where x plays the role of the voltage):

$$g_{\mathrm{RTD}}(x) = \alpha x + \beta + \gamma(|x - V_p| - |x - V_v|) \qquad (30.29)$$

where $\alpha, \beta, \gamma, V_p, V_v$ are the parameters of the RTD.

A circuit was proposed in [30] to exploit the nesting principle in a relatively new technology; namely the vertical integration of resonant tunnelling diodes

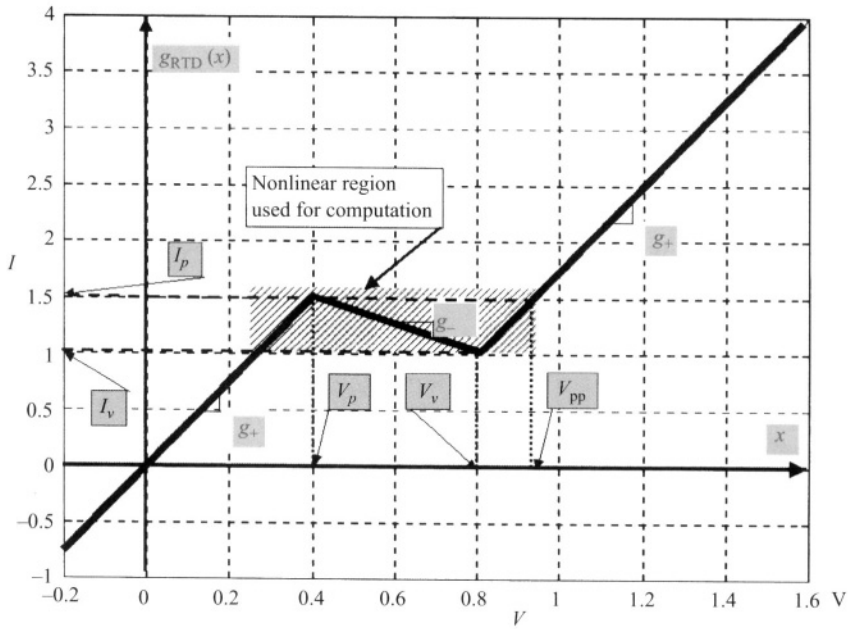


Figure 30.14. The current–voltage characteristic of the RTD (a canonical piecewise linear model).

(RTD) with FETs in high speed III-V semiconductors [27]. This technology provides high speeds and potentially high densities while operating at room temperature. The goal is to use the "nesting" idea to build a new generation of cellular neural networks with increased functional capability, a processing speed in the order of picoseconds, and a high density of cells. The schematic of the proposed circuit, using an RTD-FET GaAs technology that has been reported in [27], is presented in Figure 30.15. A detailed description of the design principles is given in [30]. Here, we will briefly present the role of each sub-circuit. The cascade of "nesting" units in our cell circuit is implementing the non-monotone discriminant function with multiple roots. The number of roots in this case is at most 3^m for "nests" where 3 stands for the number of segments in the piecewise linear characteristic of the RTD model. It was shown in [30] that $m = 3$ suffices to represent all Boolean functions with 3 inputs and most of the Boolean functions with 4 inputs. The biases z_k in the definition of the universal CNN cell are here implemented by the saturated resistors $R_{s0}, \ldots, R_{sm}$ [31]. In this circuit realization, their values are optimized so that the overall characteristic of the resulting discriminant function has its roots as homogeneously distributed as possible. The discriminant function w in the

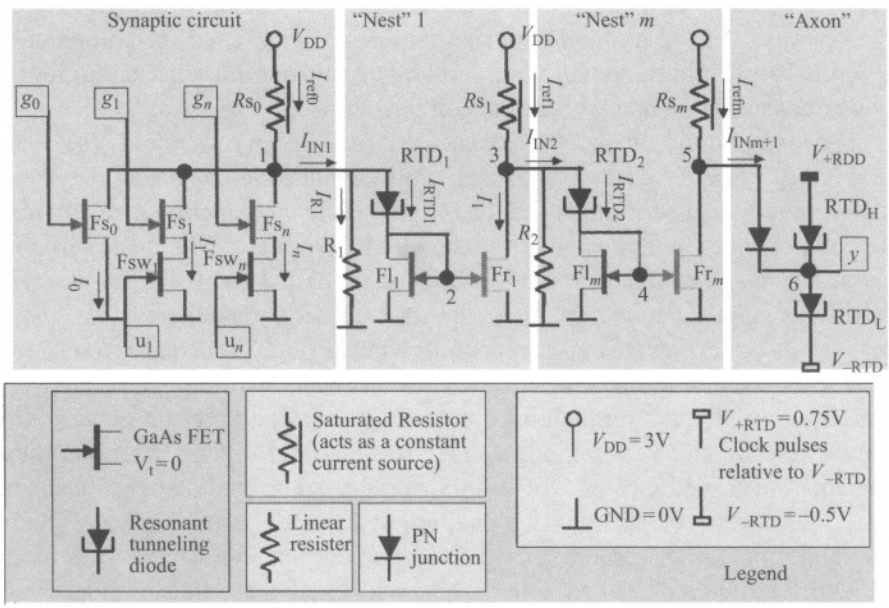


Figure 30.15. Schematic diagram of the generic RTD-based CNN cell. All symbols are standard except the "saturated resistor", which is defined as an active load acting as a current stabilizer or constant current source [31] ($n = 2$ inputs, $m = 2$ nests).

definition of the universal CNN cell here corresponds to the current $I_{\mathrm{IN}m+1}$, and the argument σ of the discriminant function is the input current $I_{\mathrm{IN}1}$. The resistors $R_1, R_2, \ldots, R_m$ play an important role and they are subject to a design trade-off. A larger value of the resistance leads to lower power consumption but, on the other hand, it increases the risk of unstable behavior due to the negative differential resistance of the RTD. If the value is too small, all other components should drive larger currents, and therefore, the *compactness* of the cell depreciates.

The functional role of these resistors is to convert the input current flowing within a nesting unit into a voltage, so that the voltage–current characteristic of the RTDs can be exploited. The current through the RTD is then read and mirrored (with a certain amplification factor k) using the current mirror formed by the two FET transistors in each "nesting" unit. The input–output current characteristic of each "nesting" unit is similar to the voltage–current characteristic but now, since both the input and the output signals are of the same type, the nesting operation can be effectively implemented.

The trade-off between *processing speed* and *versatility* is more obvious here. Each additional "nesting" unit adds more versatility but it also adds an additional delay. Another technological trade-off is given by the choice of the mirror gain k. A small mirror gain leads to less area occupied by the two FET transistors, but then the output current swing is not large enough to allow the operation of the next RTD in the nonlinear region used for computation (Figure 30.14). On the other hand, too large a mirror gain will lead to higher power consumption and worsen the compactness.

The synaptic circuit has the advantage of being very simple in the sense that it requires only positive synapses. This advantage comes from the use of a non-monotone discriminant and leads to a significant reduction in the number of components, compared with the standard CNN cells where the circuitry should be designed to accommodate both negative and positive synapses. The positive synaptic parameters b_i in the mathematical model $\sigma = z - b_0 - \sum_{i=1}^{n} b_i u_i$ correspond to the currents I_i flowing through the synaptic transistors $F_{\mathrm{S}i}$. The magnitude of these currents is controlled by the gate voltages g_i, which are implementing the concept of a "gene". They are the only control inputs that allow us to "program" the realization of a Boolean function. These currents are turned ON or OFF by the serially connected switch transistors $F_{\mathrm{SW}i}$, depending on the binary signal applied to their control gates. Finally, the output or "axon" circuit is used to implement the sign function, as in the MOBILE circuit reported elsewhere [32]. While piecewise-linear models were used in a first qualitative design, it turned out that no major changes and only slight tuning of the values for some circuit parameters was needed to achieve the same functionality in a circuit where all devices were modeled using more realistic physical models [33].

Table 30.2. Quality attributes satisfied by different CNN cell architectures (the degree of satisfaction is indicated by the number of ✓ symbols).

	Standard CNN cell	*Pyramidal CNN cell*	*Canonical piecewise-linear cell*	*Multi-nested universal CNN cell*
Universatility	✓	✓✓✓✓	✓✓✓✓	✓✓✓✓
Compactness	✓✓✓✓	✓	✓✓	✓✓✓
Robustness	✓✓✓	✓✓✓✓	✓✓	✓
Simplicity of the learning or design algorithm	✓✓✓	✓✓✓✓	✓✓	✓

30.4.6. Concluding Remarks

This section introduced several analog architectures called universal CNN cells, each being endowed with the functional capability of representing arbitrary Boolean functions by simply changing a number of control parameters. The trade-offs between several quality attributes were emphasized, suggesting solutions for dealing with trade-offs in an optimum manner. The following table summarizes the degree in which each type of cell satisfies the quality attributes discussed within this section. For comparison, the standard CNN cell is also included.

In the case of the Cellular Neural Networks, the trade-off between *compactness* and *robustness* is particularly important. Very compact cells are desirable, yet they should be robust enough to allow analog implementation. Among several theoretical solutions presented in this chapter, the multi-nested universal CNN cell is particularly promising because it allows one to manage these trade-offs easily. First of all, it is the most compact universal CNN cell architecture. For this cell, the number of "nests" m and the number n of inputs can be flexibly tuned to optimize the trade-off between *versatility* and *robustness* while keeping the cell very compact. Although it is known that any arbitrary Boolean function can be represented for $m = n - 1$, in practice, one may use a smaller m to realize certain useful local Boolean functions (having an equivalent realization in different image processing functions at the CNN level). For example, the realization of any "Parity n" Boolean function requires $m = \lceil \log_2 n \rceil$. Like in the case of standard CNN cells, there is a trade-off between the number of inputs and the robustness of the cell. A robust cell has a smaller number of inputs. On the other hand, the CNN topology imposes the number of inputs to be $n = 9$. The *multi-nested CNN cell* can be regarded as being robust enough for any of its Boolean function realizations, when $n \leq 4$. It is interesting to note that the same number of inputs $n = 4$ was found as a good compromise for

the trade-off between *versatility* and the *complexity of the learning algorithm.* In a reasonable amount of time, the whole set of realizations with $n = 4$ can be listed using state-of-the-art optimization algorithms. For larger values of *n,* this task becomes highly time-consuming. Decomposition schemes such as those presented in [21] can be used to realize compact yet robust CNN cells based on *universal CNN cells* with up to 4 inputs as the basis functions. They will lead to much more compact realizations than in the case of standard CNN cells. Multi-nested CNN cells with $n = 9$ inputs can be also considered to be practically realizable, but only for those particular Boolean functions that will be robust enough. Technological trade-offs must be also dealt with when the above-mentioned principles are implemented in analog VLSI technology. A circuit example was given where the non-monotone characteristic of vertically integrated RTDs is fully exploited, providing a highly compact circuit (in terms of the number of devices per cell).

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Chapter 31

TOP–DOWN DESIGN METHODOLOGY FOR ANALOG CIRCUITS USING MATLAB AND SIMULINK

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31.1. Introduction

This chapter presents a new design methodology for the creation of analog or mixed signal integrated circuit components. Through the use of top–down design techniques in conjunction with an optimization process, circuit design can take place at the highest level of abstraction. As a result, the requirements of the building blocks will be specified prior to the undertaking of transistor level simulations, thereby saving much valued design time. This method has the added advantage that designs can be implemented with currently used, and widely available tools. For illustration, a design example featuring a third-order, switched capacitor (SC) delta–sigma $(\Delta\Sigma)$ modulator will be presented.

A top–down design methodology consists of the division of labor in a progressive manner, among several levels of abstraction. On the conception of an *idea* and the setting of performance goals, design at the *system* level can commence. It is at this stage that the functionality of the proposed system is tested, the design or selection of a high-level architecture is made, and the analog building blocks necessary for implementation are determined. Following this, the implementation of the building blocks at the *circuit* transistor level is performed, followed by the *layout* implementation of the transistors and other components, and this is then completed by *fabricating* the design in silicon. A top–down design cycle is illustrated in Figure 31.1.

In particular, the design of analog systems primarily consists of three obstacles:

1 The selection of an architecture

2 The determination of the specifications for the analog building blocks necessary to implement the chosen architecture

3 The minimization of the effects due to circuit non-idealities.

These are usually dealt with separately, and more often than not, most of the building block specifications and non-idealities are explored through

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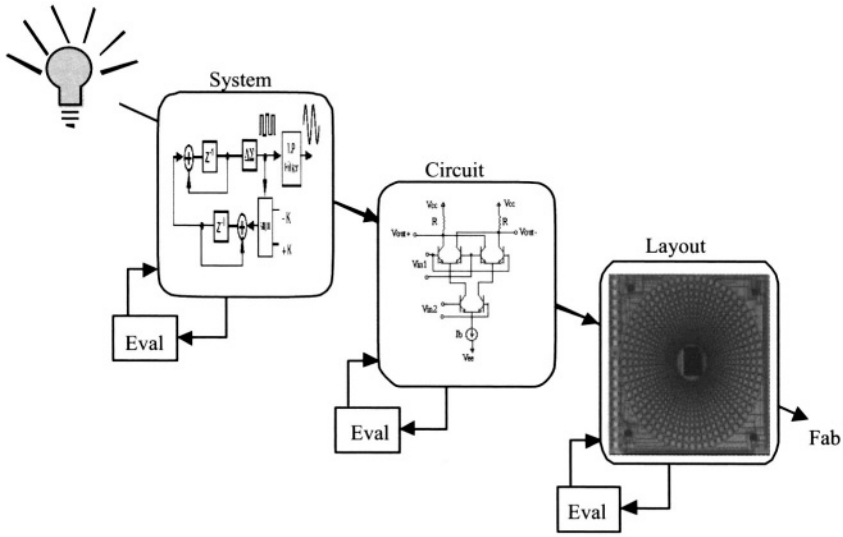


Figure 31.1. Top–down design flow.

simulation at the transistor level using circuit simulation programs such as SPICE. To verify the circuit with respect to changes in passive component (resistor, capacitor, etc.) and transistor characteristics requires simulation over the full range of these variations. Obtaining performance curves, when considering a single architecture, let alone multiple architectures, also requires multiple simulations. Attempting to perform this type of analysis at a low level can be problematic due to long simulation times [1]. Most system simulations require days to run for each case given the fastest workstations. As a result, the design cycle will take too long to practically meet the market demands for the technology, especially given the rapid progression seen today. Table 31.1 shows the Semiconductor Industry Association (SIA) predictions made in 1999. As is evident, Very Large Scale Integrated (VLSI) circuit technology feature sizes are expected to shrink, reenforcing the need for shorter design cycles.

On top of this problem, the results obtained from SPICE may be limited by rounding and truncation errors that accumulate over the large number of time steps needed for accurate simulation. Furthermore, it is often difficult to focus on key design parameters when working with many integrated devices at the transistor level. In addition to this, the entire procedure must be carried out for each architecture selected, necessitating even further simulation. Therefore, the designer has to be very careful when choosing an architecture for fear of losing much time in the initial design stages.

Table 31.1. Long-term technology roadmap [2].

Feature	*1999*	*2002*	*2005*	*2008*	*2011*	*2014*
Line width (μm)	0.18	0.13	0.10	0.07	0.05	0.035
Transistors/chip (millions)	23.8	47.6	190	539	1523	4308
Frequency (MHz)	1200	1600	2000	2500	3000	3600
Metal layers (max)	7	8	9	9	10	10
Supply voltage (volts)	1.5–1.8	1.2–1.5	0.9–1.2	0.6–0.9	0.5–0.6	0.3–0.6

In order to reduce the number of design iterations and to better explore the design options, it is beneficial to perform the analysis at the system architectural level before starting transistor level design. This allows for a feasibility analysis in which all the design considerations are treated at the highest level of abstraction. The ultimate goal of this procedure is to have the low level circuit parameters be dictated by the selected architecture and desired performance. Therefore, a top–down design procedure using optimization will be presented which makes use of Simulink modeling and Matlab optimization [3]. More specifically, in Section 31.2, the motivation for the design methodology is presented and discussed. The work is further explained in Sections 31.3 and 31.4 with a design procedure featuring a $\Delta\Sigma$ modulator involving Simulink modeling. This is followed by a discussion on the Matlab optimization setup in Section 31.5, and supported by simulation results in Section 31.6. A simple, fully detailed example is presented in Section 31.7, with some concluding remarks being made in Section 31.8.

31.2. Design Methodology Motivation

Choosing the specifications for an analog circuit, given a set of design objectives such as minimal area and power, is potentially a very complicated and time-consuming process. This task is further complicated by the fact that the number of specifications to deal with is usually very large, and varies from one application to another.

There exist tools that are aimed at fully automating the design process, however, they are limited to a small number of fixed schematics [4–7]. These tools, which are not designed to be reproduced, remove the designer from the process, and does nothing to increase the designer's knowledge. Furthermore, the techniques used in these programs are hidden and cannot be applied to other designs.

One of the main drawbacks to analog design is the uncertainty that arises due to a change in technology. As a result, it is more amenable to consider a design process that can begin without a dependence on a specific technology. This

would allow for a large portion of the design to be carried out independently of the technology, and could lead to a high degree of reusability. High-level optimization geared design avoids the reliance on a specific technology the longest, and in this case provides the designers with values for familiar parameters (e.g. g_m and r_{out} in the case of an operational transconductance amplifier or OTA). These are quantities that are very familiar and understood by designers and provide excellent guidelines for the construction of a device. Furthermore, symbolic analysis is a method by which designers can obtain an understanding of a circuit's behavior. Therefore, relating the behavior of the circuit to several descriptive equations or expressible rules of thumb, and moreover to a few key parameters, can reduce the complexity of a problem and lends itself to a solution through optimization.

The main focus of this chapter is to provide designers with a means of tackling the design problem by presenting a simple to implement design methodology that involves widely used and available tools. As a result, the procedures can be implemented and reused with little difficulty or expense. In order to make use of widely available tools which are already known to many designers [8,9], Simulink is used to implement the system architecture and model non-idealities, while the Matlab optimization toolbox [10] is used to create routines to optimize the circuit parameters.

31.2.1. Optimization Procedure

Optimization in general concerns the minimization or maximization of a function. In the case of analog systems, the objective is to maximize or minimize a given set of performance criterion, such as the Signal to Noise and Distortion Ratio (SNDR), power, area or settling time. To do so, one must establish a trackable set of variables (g_m, r_o, I_{bias} or C_{load}) that can be used to model the system while simultaneously providing a link to the performance criterion. An illustrative flow of this procedure can be seen in Figure 31.2. It consists of four main components: a property measurement block, a summing block with the desired property as one input, an optimization procedure and finally the circuit that is under development. The property measurement block detects particular attributes of the output signal from the circuit and compares it with the desired behavior. The error signal is then used to adjust the key parameters of the circuit such that the error is minimized. It is using this very simple principle that the proposed top–down methodology is executed.

Due to its ability to model nonlinear devices, there already exists much work in a variety of fields that use Simulink modeling, and as such it is not difficult to find pre-existing models, or to create new models specific to a design [11–15]. In order to best explain the procedure, the proposed methodology will be illustrated using a $\Delta\Sigma$ analog-to-digital converter (ADC). It is important

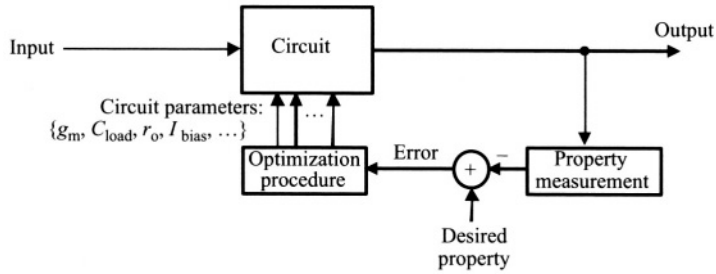


Figure 31.2. Optimization procedure.

to realize that this methodology is not limited to $\Delta\Sigma$ modulators. It may be used to help design any device or system, in which key parameters, formulas or rules of thumb can be identified.

31.3. Switched Capacitor Delta–Sigma Design Procedure

$\Delta\Sigma$ ADCs are widely used and well suited for high-resolution conversion. One dominant factor in their popularity stems from their high tolerance to component mismatch and circuit non-idealities. Despite its high tolerance to non-idealities, the $\Delta\Sigma$ modulator is still governed by the limitations of its analog building blocks. In particular, SC $\Delta\Sigma$ modulators are sensitive to circuit non-idealities at the input stage where no noise shaping has yet taken place [16]. Specifically, sampled capacitor (kT/C) noise and OTA characteristics (noise, clipping, finite gain, finite bandwidth and slew rate (SR)) at the front-end limits the achievable dynamic range and therefore performance. A high-level diagram of a Simulink realization of a third-order $\Delta\Sigma$ single-loop modulator can be seen in Figure 31.3. It is important to realize that upon implementation, each component block has to be translated into its circuit equivalent (analog building blocks) and then implemented.

In order to use an optimization procedure, it is first necessary to isolate the key parameters that influence the system's performance. In the design of high-resolution SC $\Delta\Sigma$ modulators, it can appear that there is a large set of parameters to optimize. However, if one examines the building blocks of the system, it can be seen that most of the factors that affect the system's performance (kT/C noise, OTA noise, voltage clipping due to a finite output range, finite gain, finite bandwidth and SR) can be related to a small set of parameters. These parameters will now be explored, and since $\Delta\Sigma$ modulators are sensitive to circuit non-idealities at the input stage (the first integrator seen in Figure 31.3) where no noise shaping has yet taken place, this section of the modulator will be the focus of the analysis.

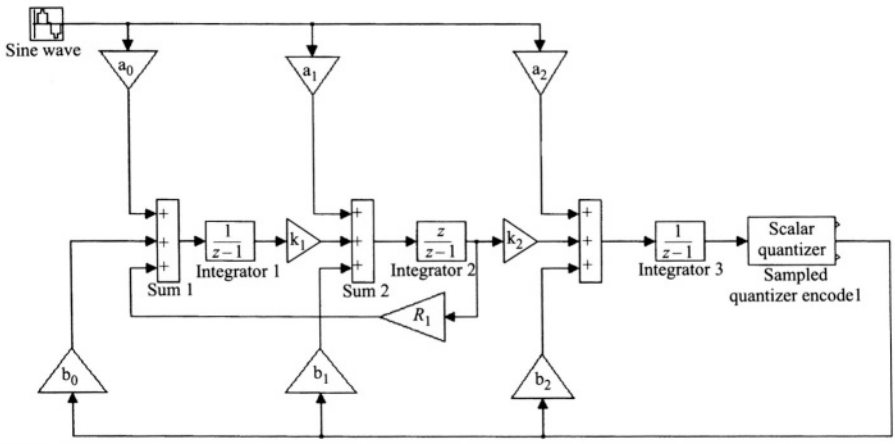


Figure 31.3. High-level diagram of the modulator.

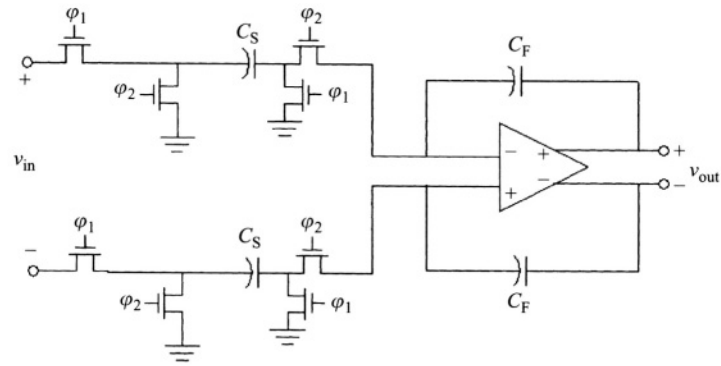


Figure 31.4. SC implementation of the first integrator.

31.3.1. Switched Sampled Capacitor (kT/C) Noise

A critical source of noise is the kT/C noise injected into the first integrator of the modulator because it directly increases the noise level at the output. The kT/C noise component results from the sampled noise stored on the capacitor due to switch resistances. As a result, the input capacitors must be large enough to counter this effect. Therefore, the first key parameter, which can be seen in Figure 31.4, is the input sampling capacitor C_S.

Table 31.2. OTA non-idealities.

Non-ideality	*Result*
Finite DC gain	Rise in quantization noise
Saturation	Possible harmonic distortion
Bandwidth limiting	Noise due to incomplete settling
SR limiting	Noise due to incomplete settling and harmonic distortion
Thermal noise	Added white noise

31.3.2. OTA Parameters

The OTA within the modulator is the most critical component, as the non-idealities that it exhibits causes an incomplete transfer of charge leading to nonlinearities. By briefly examining this device, key parameters that govern its non-ideal behavior can be isolated and examined. Shown in Table 31.2 are the corresponding non-idealities that must be considered in an OTA.

There are three OTA topologies commonly used in the design of $\Delta\Sigma$ modulators [17], the folded cascode amplifier (Figure 31.5(a)), the two-stage class A amplifier (Figure 31.5(b)), and the two-stage class AB amplifier (Figure 31.5(c)). Table 31.3 highlights the key properties that govern the operational performance of these OTAs. These properties allow for behavioral modeling of the device and, more importantly, can be dissected to obtain the key parameters of the device. It is important to note that r_{o1} refers to the output resistance of the first stage. We can see from this table, that the main sources for non-idealities in the modulator can be related to a few key OTA parameters (g_m, r_o, C and I_{bias}). As a result, the key parameters for each of the OTA topologies that can be used in the modeling of each structure are listed in Table 31.4.

31.4. Modeling of $\Delta\Sigma$ Modulators in Simulink

In order to perform behavioral simulations of $\Delta\Sigma$ modulators while taking into account most of the non-idealities, it is necessary to create models for them. A set of models has been proposed that attempt to simulate the non-idealities in Simulink [15]. The following work is intended as modifications and extensions to those models for the purpose of providing reference to the key parameters highlighted in Table 31.4, and to make them more suitable for an optimization environment.

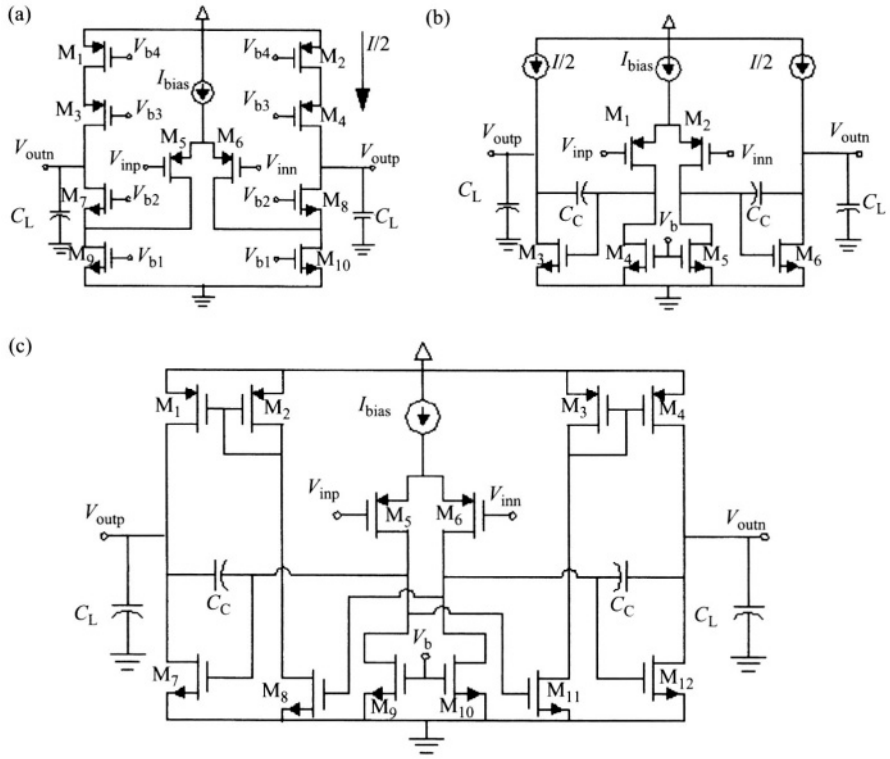


Figure 31.5. OTA topologies: (a) folded cascode, (b) two-stage class A, (c) two-stage class AB.

Table 31.3. Key properties in OTAs.

Property	*Folded cascode*	*Two-stage class A*	*Two-stage class AB*
DC gain	$g_{m5} * r_o$	$g_{m1} * ro1$	$g_{m5} * r_{o1}$
Unity gain Frequency	g_{m5}/C_L	g_{m1}/C_C	g_{m5}/C_C
SR	I/C_L	$\min\{I_{bias}/C_C, I/(C_L + C_C)\}$	I_{bias}/C_C

31.4.1. Sampled Capacitor (kT/C) Noise

The thermal noise associated with the switching due to input sampling onto the first integrator can be modeled as follows:

$$y(t) = k_{int} \cdot [x(t) + n_{switch}(t)] \tag{31.1}$$

Table 31.4. Key parameters for modeling.

Folded cascode	*Two-stage class A*	*Two-stage class AB*
$g_{m5}, r_o, C_L, I_{bias}, C_S$	$g_{m1}, r_{o1}, C_L, C_C, I_{bias}, I, C_S$	$g_{m5}, r_{o1}, C_C, I_{bias}, C_S$

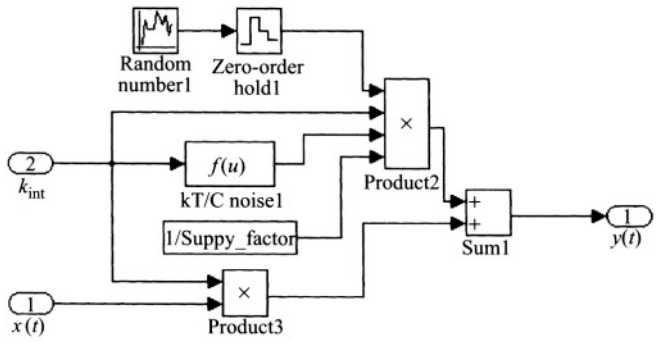


Figure 31.6. kT/C noise model in simulink.

where

$$n_{switch}(t) = \sqrt{\frac{k \cdot T}{C_S}} \cdot \mathrm{RN}(t), \tag{31.2}$$

where k_{int} is the integrator gain, C_S is the input sampling capacitor, k is Boltzman's constant, T is temperature and RN(t) is a Gaussian random number with zero mean and unity standard deviation. This has been implemented in the Simulink block diagram shown in Figure 31.6. It is important to note that the formula used in the $f(u)$ block with its input k_{int}, implements the $n_{switch}(t)$ formula given in equation (31.2). A Supply_factor block can also be seen in the diagram. This is present for simulations in which it is desired to normalize the supply voltage. If no such normalization is required, then Supply_factor should be set to 1.

31.4.2. OTA Noise

The input referred noise of an OTA can be modeled as follows:

$$y(t) = k_{int} \cdot [x(t) + n_{OTA}(t)] \tag{31.3}$$

where

$$n_{OTA}(t) = V_n \cdot \mathrm{RN}(t) \tag{31.4}$$

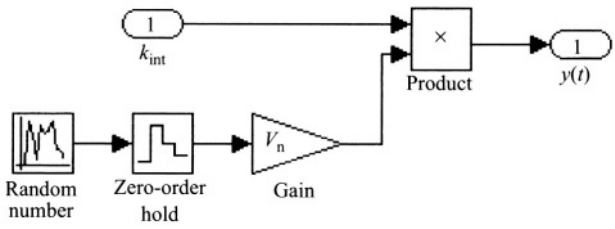


Figure 31.7. OTA noise model in simulink [15].

where k_{int} is the integrator gain, V_n is the OTA RMS noise voltage, and RN(t) is a Gaussian random number with zero mean and unity standard deviation. The model can be seen in Figure 31.7.

31.4.3. Switched Capacitor Integrator Non-Idealities

SC integrators are composed of non-ideal analog building blocks, the foremost of which is an OTA. As a result, a model needs to be created to take into account the noise and/or distortion generated by these components.

One of the main non-idealities is caused by having finite gain in the OTA. As a result, the transfer function of the integrator changes depending on the amount of DC gain provided by the amplifier. The ideal transfer function is given by

$$H(z) = \frac{k_{int}}{z-1} \tag{31.5}$$

In reality, this model is not sufficient for the complete description of the integrator's characteristics. Examining Figure 31.8 reveals that the transfer function of the integrator changes depending on the amount of DC gain provided by the amplifier.

As a result, the transfer function takes on a gain dependency given by:

$$H(z) = \frac{k_{int}}{z-\alpha} \tag{31.6}$$

where k_{int} is the integrator gain,

$$\alpha = \frac{g_m \cdot r_o - 1}{g_m \cdot r_o}$$

and g_m as well as r_o are the parameters in the amplifier that define its gain. The deviation caused by finite gain, and represented by α, must be accounted for in any modeling.

Another source of non-ideality comes about because an OTA is subject to clipping. Clipping occurs when the OTA is asked to produce an output voltage

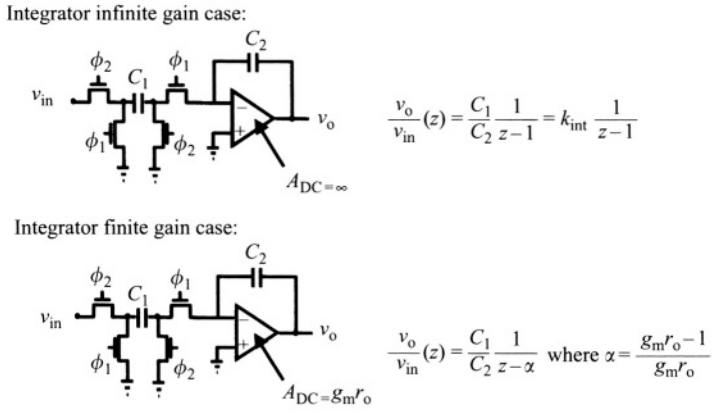


Figure 31.8. Transfer function of integrator with finite gain.

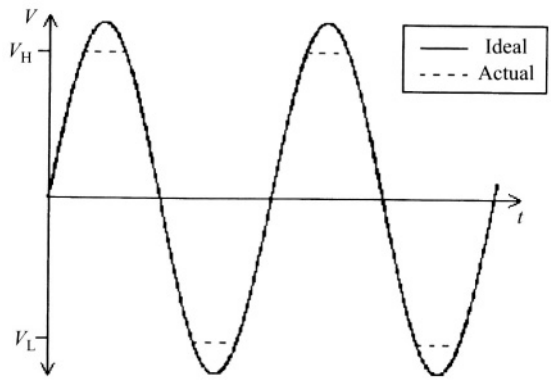


Figure 31.9. Distortion effect of clipping.

higher than the voltage supply rails. Should this occur in the system, the output would cease to follow the ideal output voltage waveform, and instead a distorted waveform would be produced. This is illustrated in Figure 31.9, where V_H and V_L are the upper and lower power supply rails. This effect must be integrated into the model as well, and is accomplished through the use of a saturation block in Simulink.

A final source of non-ideality that will be dealt with is slew and bandwidth limiting. The slew and bandwidth behavior of an OTA was modeled based on an analysis in which their effects in a SC integrator are interpreted as a nonlinear gain [18]. There are three basic mutually exclusive conditional states that can

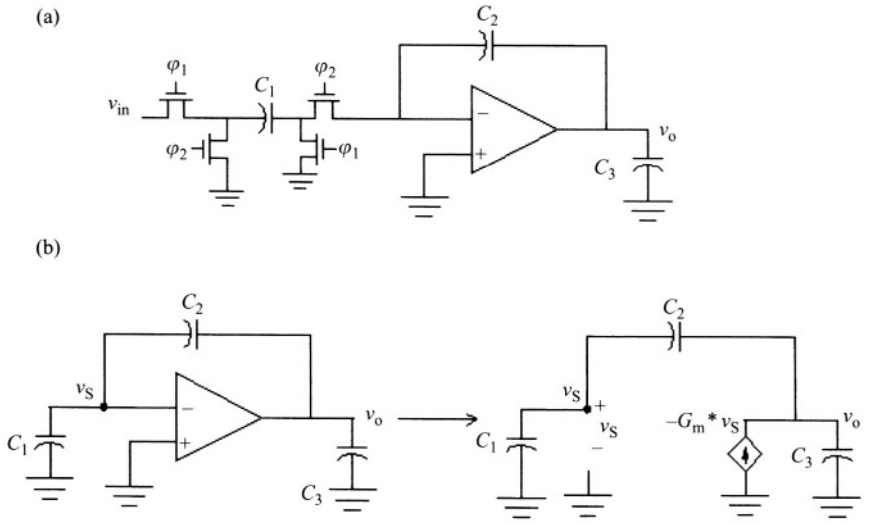


Figure 31.10. Analysis of transient integrator behavior.

occur, based on the present input voltage and the previous output voltage:

1 complete bandwidth limiting,

2 complete SR limiting, and

3 first SR followed by bandwidth limiting.

In order to understand and model this effect properly, it will now be explored in some detail. The primary goal is to capture the input–output transient behavior of the circuit in mathematical form. Figure 31.10(a) shows the single-ended SC integrator, while Figure 31.10(b) reveals the circuit representation of the integrator on the driving phase ϕ_2. It is important to recall that in a sampled-data system such as this, there is a finite amount of time given for all the phases to execute. In a two-phase system, that time corresponds to $T/2$ (where T corresponds to the clock period). For the purpose of this analysis, assume that capacitor C_3 is a lumped capacitor containing the output parasitics and the loading of the next stage. It is also important to realize that the analysis was done on a single-ended amplifier to simplify the understanding of the procedure. If one takes advantage of the symmetry present in a differential circuit, the same analysis is valid [19].

The transient associated with the output voltage of the SC integrator can be represented in the following form:

$$v_o(t) = v_o(0^-) - G \cdot v_S(0) \cdot (1 - e^{-t/\beta \cdot w_t}) \tag{31.7}$$

where $\beta = C_2/(C_1 + C_2)$, $w_t = G_m/C_L$, $C_L = C_3 + C_1 \cdot C_2/(C_1 + C_2)$, $G = C_1/C_2$, $v_S(0)$ is the input OTA node voltage at the beginning of this cycle, and $v_o(0^-)$ refers to the output voltage present at the end of the previous cycle. This means that effectively, the charging/discharging time constant τ of the circuit can be defined as:

$$\tau = \frac{1}{\beta \cdot w_t} = \frac{C_1 \cdot C_2 + C_2 \cdot C_3 + C_1 \cdot C_3}{G_m \cdot C_2} \tag{31.8}$$

It is important to note that $v_S(0) = -v_{in}(0)$, and as a result, equation (31.7) can be written as

$$v_o(t) = v_o(0^-) + G \cdot v_{in}(0) \cdot \left(1 - e^{-t/\beta \cdot w_t}\right) \tag{31.9}$$

The system behaves as described by equation (31.9) when limited purely by the charging/discharging time constant, and is commonly referred to as being bandwidth limited.

The system may also suffer from SR limitations, which is illustrated in Figure 31.11. Since the amplifier can only supply a maximum finite current (I_{bias}) to the capacitive load (C_L), an inherent limit to the instantaneous change in output voltage is present. Therefore, if the change in voltage is too large, this limit is exceeded, and the output will be subject to a linear charging (with slope SR) described by

$$\mathrm{SR} = \frac{\mathrm{d}}{\mathrm{d}t} v_o(t)\Big|_{max} = \frac{I_{bias}}{C_L} \tag{31.10}$$

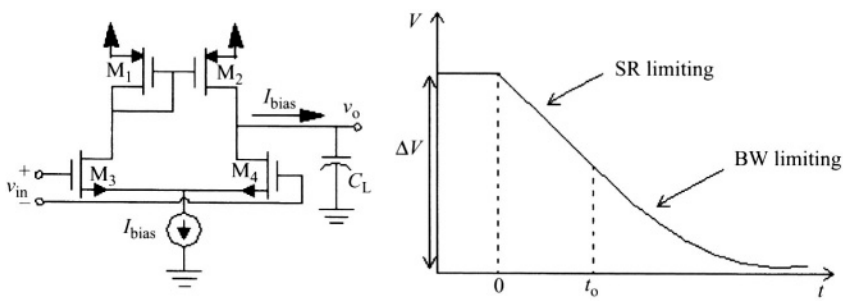


Figure 31.11. The presence and effect of SR limiting.

If it is assumed that the system is SR limited for a portion of the time t_o, the output voltage can be written as

$$v_o(t) = \begin{cases} v_o(0^-) + \mathrm{SR} \cdot t & \text{if } t \le t_o \\ v_o(0^-) + \mathrm{SR} \cdot t_o + (G \cdot v_{in}(0) - \mathrm{SR} \cdot t_o) \cdot (1 - e^{(t_o - t)/\tau}) & \text{if } t_o < t \end{cases} \tag{31.11}$$

At time t_o, the system ceases to be SR limited and returns to its "natural" charging/discharging state and becomes bandwidth limited. It follows that at only the point corresponding to t_o, the bandwidth and SR limiting will be identical. This arises because bandwidth limiting produces a monotonically increasing/decreasing exponential voltage function. Such a response has a different slope at every point, and thereby will be equal to SR only once (i.e. at $t = t_o$, $dv_o(t)/dt = \mathrm{SR}$). As a result, one can solve for the time the system remains SR limited by evaluating the slope of the bandwidth-limited response at time t_o and equating it with the slope of a SR limited system, that is,

$$\mathrm{SR} = \frac{d}{dt} v_o(t)\bigg|_{t_o} = \left(\frac{-\mathrm{SR} \cdot t_o}{\tau} + \frac{G \cdot v_{in}(0)}{\tau} \right) \cdot e^{(t_o - t)/\tau} \tag{31.12}$$

After evaluating the function at time t_o, one is left with the following equation:

$$\mathrm{SR} = \frac{-\mathrm{SR} \cdot t_o}{\tau} + \frac{G \cdot v_{in}(0)}{\tau} \tag{31.13}$$

This can be easily rearranged to provide,

$$t_o = \frac{G \cdot v_{in}(0)}{\mathrm{SR}} - \tau \tag{31.14}$$

Therefore, SR limiting will occur if $dv_o(t)/dt > \mathrm{SR}$ and last for a length of time given by t_o.

When creating a model involving SR and bandwidth limiting, the actual transient behavior of the integrator is not crucial since SC circuits depend only on the output at the end of each cycle. Therefore, it is important to obtain an expression for the output voltage of the integrator at time $T/2$. The appropriate behavior at this time can be summarized as follows:

$$v_o\left(\frac{T}{2}\right) = \begin{cases} v_o(0^-) + G \cdot v_{in}(0) \cdot (1 - e^{-T/2\tau}) & \text{if } t_o \le 0 \\ v_o(0^-) + \mathrm{SR} \cdot t_o + (G \cdot v_{in}(0) - \mathrm{SR} \cdot t_o) \cdot \left(1 - e^{(t_o - T/2)}\right) & \text{if } 0 < t_o \le T_2 \\ v_o(0^-) + \mathrm{SR} \cdot T/2 & \text{if } \frac{T}{2} < t_o \end{cases} \tag{31.15}$$

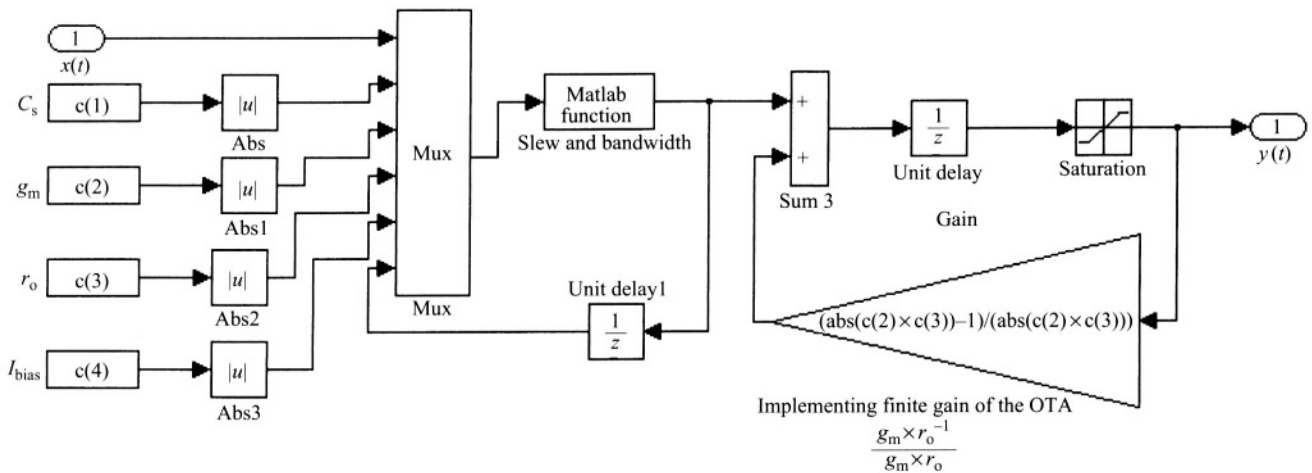


Figure 31.12. Non-ideal integrator model in simulink.

The finite gain, the clipping levels, the finite bandwidth and the SR limiting of the OTA are incorporated into a Simulink model of the SC integrator as shown in Figure 31.12. The formulas used in this block depend on the type of OTA implemented. In this case, the formulas for the folded cascode amplifier were used, hence parameters C_S, g_m, r_o and I_{bias} are required (Table 31.4). From the diagram, it can be seen that a Slew and Bandwidth Matlab function block exists that interfaces with a multiplexer. Due to its conditional nature, the modeling was much easier accomplished through the use of a Matlab function, which implemented the previously described equations. Furthermore, it was necessary due to the nature of SR limiting, to create a block that is capable of retaining "memory" of its previous state. This is accomplished by feedback through the multiplexer, which also takes in the key parameter values (C_S, g_m, r_o, I_{bias}) fed to it by the optimization routine.

31.5. Optimization Setup

In this section, a set of guidelines that clarify the Matlab design space will be presented to help explain and carry out the design methodology. Some familiarity with the Matlab optimization toolbox will be assumed.

The optimizer is essentially split up into three parts and is illustrated in Figure 31.13. Each block is described below:

1 The Matlab optimizer block receives an error value and accordingly adjusts the key parameters given to it in order to minimize any further

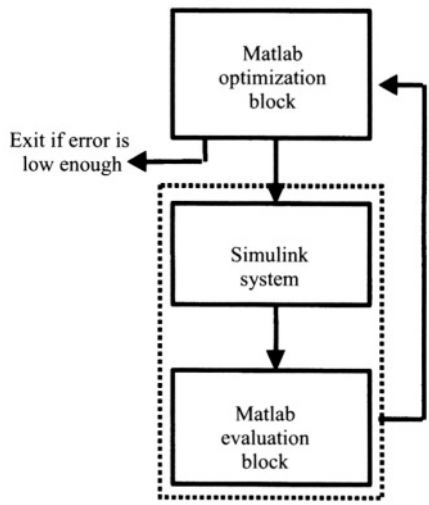


Figure 31.13. Optimization setup.

error. On the first run, the optimizer begins by using the initial conditions supplied to it for the key parameters.

2 The Simulink system, with its built in non-idealities, is called by the optimizer so that data for property measurements can be obtained (i.e. getting the required data to produce SNDR calculations).

3 The Matlab evaluation block receives data from the Simulink System, evaluates the results based on constraints (bounds) on the key parameters, and produces a value for the error based on the designer's criteria. When the error is low enough, the process will stop and deliver its results.

For the specific case of the $\Delta\Sigma$ modulator, the folded cascode OTA was chosen, and as a result, the key parameters that necessitated optimization were C_S, g_m, r_o and I_{bias}. The next step is to define both the error measurement criteria and the constraints. It is important to note that these criteria can be as simple or as complicated as the designer wishes. The more criteria that are given translate into a longer optimization routine, but a final result that is closer to the overall goal. In the case given here, the following three criteria were used:

1 *Minimization of area.* This was formulated on the basis of capacitance. Since the capacitance required in single-loop modulators usually accounts for at least half of its area, the area constraint placed an emphasis on minimizing this capacitance.

2 *Minimization of power.* The main power consumption in the modulator comes from the op-amp used in the first-stage integrator. As a result, constraints were placed on the bias current in order to place an upper bound on power consumption, and to minimize the current used.

3 *Maximization of SNDR.* Since SNDR is a dominant measure of a modulator's performance, lower limits were placed on its value, with an emphasis placed on its maximization.

The Simulink system was used in order to get the data for the SNDR measurements. All these measurements were affected by the key parameters, as the modeling for the system was based around them. An example of a $\Delta\Sigma$ Simulink system, with all of the non-ideality modeling present, can be seen in Figure 31.14. This is the same system that was presented in Figure 31.3, except that in this diagram, the Simulink models have been added to account for kT/C and OTA noise, and to account for the use of a non-ideal integrator in the first stage of the modulator.

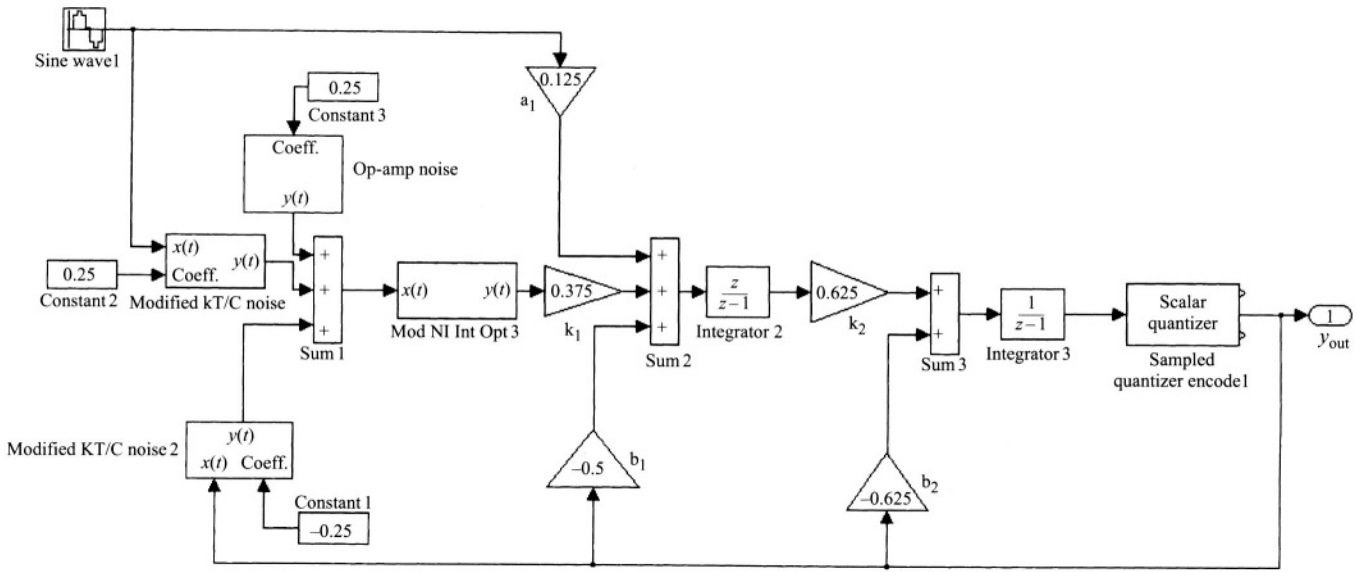


Figure 31.14. Non-ideal system in simulink.

31.5.1. Implementation in Matlab

Example code for the third-order $\Delta\Sigma$ modulator is presented in Figures 31.15 and 31.16. The first function called "optim.m" (Figure 31.15), basically implements the Matlab optimizer block seen in Figure 31.13. This function takes in performance specifications from the user (such as the sampling frequency (f_S), and the desired SNDR (SNDR_goal)) and is also used to set up the optimization options such as the step size and tolerance of the program. This program strives to minimize the coefficients that are specified, in this case C_S, g_m, r_o and I_{bias}. By minimizing these parameters, the minimal requirements for the OTA will result, and power should also be minimized.

```
% File: optim.m

function [c]  =  optim(Npoints,M,Supply_factor,fs,bw,simtime1,SNDR_goal);

% Calculation of Constants

SNDR_weight = 10^(SNDR_goal/10);
number_of_tau = -log(10^(-1*(SNDR_goal/20)));
maxtime = 1e9*(1/fs)*(1/2)/number_of_tau;
window1 = kaiser(Npoints,30);
band_edge = floor((bw/fs) * Npoints)+1;

% Starting values of Coefficients
% Cs    1e-12 (pF)
% gm    1e-4  (100's uV/Amp)
% ro    1e6   (Mohm)
% Ibias 1e-4  (100's uAmps)
coef(1) = 4.5;
coef(2) = 33;
coef(3) = 1;
coef(4) = 5;

% The optimizer will try to minimize Cs, gm ro, and Ibias

% Lower and Upper Bounds on the Coefficients
VLB  = [3.5 10 .2 .5];
VUB  = [5 34 1 10];

% Set up Optimization Options: Used to Define Tolerances and Step Sizes
options = foptions;
options(1) = 1;
options(2) = .1;
options(3) = .01;
options(4) = .1;
options(14) = 1000;
options(16) = .1;
options(17) = 1;

[C,dummy]= constr('param',coef,options,VLB,VUB,[],Npoints,M,Supply_factor, ...
                  simtime1,SNDR_weight,maxtime,SNDR_goal,window1,band_edge);
```

Figure 31.15. Matlab optimization block: *optim.m.*

```
% File: param.m

function [L2,g] = param3o(coeff,Npoints,M,Supply_factor,simtime1,SNDR_weight, ...
                          maxtime,SNDR_goal,window1,band_edge);

% Running Simulink to get the stream
  disp('Simulating...');

inputs = simset('SrcWorkspace','current','DstWorkspace','base');

%Creating the Variables for Interface with Simulink

c = [(coeff(1)*1e-12) (coeff(2)*1e-4) (coeff(3)*1e6) (coeff(4)*0.5e-4)];
Cs = c(1)
gm = c(2)
ro = c(3)
Ibias = c(14)

[tsim,xsystem,yout]=sim('Non_ideal_modulator',simtime1,inputs);

simtime = length(yout);
hy = (2*(abs(fft(yout(simtime-Npoints+1:simtime).*window1,Npoints))).^2)/((Npoints)*(Npoints-1));

% Additional Factors for use in Time Constant Calculation

Cp1 = 1e-12;
Ck1 = .75e-12;
Clp1 = 2.346e-12;

% Time Constant on Each Phase

tau11 = ((4*c(1)*Cp1) + Clp1*(4*c(1) + Cp1))/(c(2)*4*c(1));
tau12 = (Clp1 + Ck1 + 4*c(1)*(2*c(1) + Cp1)/(6*c(1) + Cp1))/((c(2)*4*c(1))/(6*c(1) + Cp1));

tau = 1e9*max(tau11,tau12);

% Calculate SNDR with Kaiser Window

noise1 = sum(hy(1:(M+1-floor(19/2)-1)));
noise2 = sum(hy((M+1+floor(19/2)+1):band_edge));
noise = noise1 + noise2;
noise = noise./(((.402)\^2);
peak = (hy(M+1))/.2276^2);
sndr = 10*log10(peak/noise);
mag = peak/noise;

L2 = (abs(1/mag))*SNDR_weight

disp('Done.');

% ******* set up constraints ************
% constr <= 0

constr1 = tau - maxtime        % Tau is less than the maximum allowable time
constr2 = -tau                 % Tau is greater than zero
constr3 = -sndr + SNDR_goal    % SNDR is greater than the SNDR goal

g = [constr1 constr2 constr3];
```

Figure 31.16. Matlab evaluation block: *param.m.*

It is in this function where the initial conditions along with the bounds on the variables are set, which will be discussed in Subsections 31.5.2 and 31.5.3. It is also in this function where all preliminary calculations are done. For example, the windowing function for the Fast-Fourier Transform (FFT) used to calculate the SNDR is created here. This is created only once and the vector is passed to the Matlab evaluation block each time an SNDR is calculated. By creating the

window in this function rather than repeatedly recalculating it in the evaluation block, valuable CPU time is saved.

The function "param.m" (Figure 31.16) basically implements the Matlab evaluation block and the Simulink system block. In fact, the Simulink System Block is implemented through a function call to the Simulink file "Non_ideal_modulator" seen in Figure 31.14. The Matlab evaluation block, which is the remainder of the file, receives the information gathered from the Simulink simulation, and calculates an error based on how far this is from the desired result. Furthermore, several constraints can be placed on any of the variables or values derived from them. For example, the settling time of the integrator is calculated in this function. A constraint is placed on it, forcing the optimization to continue until the settling time is less than the maximum settling time allowable to still achieve the desired performance. Further, constraints in this function force the settling time to be greater than zero (a condition that prevents the use of negative numbers), and force the optimizer to continue until the desired SNDR performance is achieved.

The final function "slew.m" (Figure 31.17), represents the code that was used to implement the Matlab function which accounts for bandwidth and SR limiting. This code is specifically tailored to the third-order $\Delta\Sigma$ modulator seen in Figure 31.14, however, it can be easily adapted for other designs. This function takes in the inputs C_s, g_m, r_o, I_{bias}, u and v (as seen in Figure 31.12), where u is the current input to the integrator, and v is the previous output of the integrator. This function is basically used to properly implement equation (31.15) in its entirety. It is important to note that the input u is already scaled by a factor of 1/4 (as seen in Figure 31.14), and therefore the quantity G in equation (31.15) is set to one.

31.5.2. Initial Conditions

A good set of initial conditions, or an adequate bounding of the optimized variables is needed, for improved optimization efficiency, and to increase the chances of obtaining a convergent solution.

The best set of initial conditions and bounds will usually come from the designer, as a designer usually has a better intuitive understanding and more knowledge concerning the feasibility of certain values. For example, a simulator may solve for a capacitance of 1 nF, but a designer knows that such a value is infeasible or undesired. The task then shifts to the designer for obtaining a good set of initial conditions and bounds.

In addition, the knowledge of transistor parameters such as r_o and g_m can help to obtain all of the required information necessary for setting bounds on variables. Preliminary simulations in SPICE can solve this problem quickly and efficiently. For example, the measurement of r_o for a single transistor

```
function [out]= slew(u,Cs,gm,ro,Ibias,v)

% u is current input
% v is previous output

% Sampling Frequency
Fs = 6.144e6;
Ts = (1/Fs);
Tsn = 1;              % All Equations are Normalized to Ts

% Capacitors Used in the Integrator
% Note: Gain of integrator is 1/4

Clp = 2.4e-12;        % OTA Output Capacitance
Cp  = 1e-12;          % UTA Input Capacitance
Ck1 = .75e-12;        % Capacitance of Next Stage

% Effective Load
CL = Clp + Ck1 + (4*Cs*(2*Cs + Cp))/(6*Cs + Cp);

% Slew Rate of the OTA (V/sec)
Sr = Ibias/CL;
SR = (Sr/Fs);

% Unity Gain Bandwidth of the OTA
ugbw = gm/(2*pi*CL);
UGBW = (ugbw/Fs);

% Scale Input to Integrator
d = u - v;

% Time Constant
tau = 1/((2*pi*UGBW*4*Cs)/(6*Cs + Cp));

% Slew Time: Implement Slewing Equations Here
to = ((abs(d))/SR) - tau;

f = abs((d/tau));
if abs((d/tau)) < = SR

    outpt = v + d + (1 - exp(-Tsn/(2*tau)));
else

  if to < (Tsn/2)

      output = v + d + (SR*to - d)*exp((to-(Tsn/2))/tau);

  else
      if d > 0
         outpt = v + (Tsn/2)*SR;
      else
         outpt = v - (Tns/2)*SR;
      end
  end
end

out = output;
```

Figure 31.17. Matlab function: *slew.m*.

is a trivial matter, and based on this value, a range of values for the output resistance of an OTA can be constructed. Furthermore, feasible bounds for g_m can be found by simulating a differential pair, and sweeping the bias current. This process is very simple and quick, and only needs to be done once for each new technology. Bounds can also be created based on the designer's preference. For example, if a capacitance is desired, then upper and lower bounds can be set so that no solution will contain too low (put the lower bound equal to that of the minimum sized matchable capacitor allowable in the technology) or too high a capacitance for the designer's liking. Once bounds have been chosen for each of the key parameters, choosing the initial conditions is not so arduous a task, as any values within those bounds can be taken as a starting point.

31.5.3. Additional Factors

There are additional factors that can alter the behavior of the system. As examples, the input and output capacitances of the amplifier along with the loading capacitance of the common-mode feedback circuit (CMFB) can affect the settling times of the integrators. These parameters can be accounted for by lumping them in with other key parameters. For example, C_L can be altered to reflect all the additional loading mentioned. The inclusion of these additional factors can be left to the discretion of the designer, or can be part of a larger iterative design procedure.

31.6. Summary of Simulation Results

This optimization procedure was applied to the design of a 16-bit (SNDR = 98 dB), third-order $\Delta\Sigma$ ADC, in which the primary objective was to design a lowpass, audio-band (bandwidth of 24 kHz), single bit, modulator, with an oversampling ratio of 128. The choice of coefficients used in the Simulink diagrams is purely an architectural design consideration and will not be discussed here. The focus remains on the performance of the system with the modeled non-idealities.

An ideal Simulink simulation of this modulator was run in order to determine the maximum achievable performance of such a system. The simulation yielded a peak SNDR of 105.72 dB, and a dynamic range of 112 dB, which can be seen in Figure 31.18(a). After the addition of the models that were presented in Section 31.4, the Simulink diagram was constructed (Figure 31.14), and the optimization routine was run. The process resulted in feasible design values ($g_m = 3.3\,\text{mA/V}$, $r_o = 963\,\text{kW}$, $I_{bias} = 458\,\text{mA}$ and $C_S = 4.5\,\text{pF}$, for an effective load of 8.2pF). An SNDR curve, which reflected the modeled non-idealities was produced, and can be seen in Figure 31.18(b). The simulation of the non-ideal modulator yielded a peak SNDR of 99.45 dB, and a dynamic range of 102 dB. This system was verified in SPICE through a series of simulations.

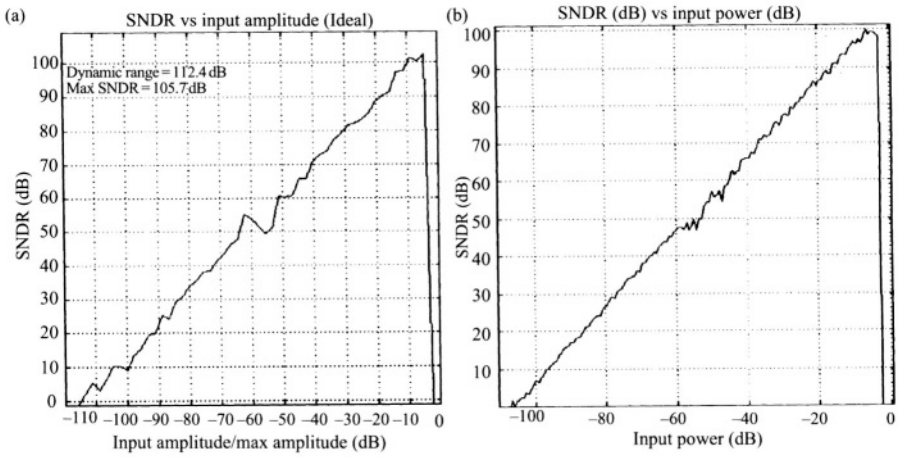


Figure 31.18. SNDR plots for third-order modulator in simulink. (a) Ideal and (b) non-ideal.

31.7. A Fully Coded ΔΣ Modulator Design Example

A brief example will be presented to further clarify the design process. This example is fully reproducible in Matlab and Simulink, and can be used to get an understanding of the methods needed for the design. The same third-order $\Delta\Sigma$ modulator will be used to design for kT/C noise requirements. The modulator will operate at 6.144 MHz, with a bandwidth of 24 kHz, have 16-bit performance, with a power supply of 2.5 V.

In order to begin, one can break the process down into several simple steps to be followed:

1 Identify/select the parameters to be optimized.

2 Create/use Simulink models to implement the non-idealities causes by the chosen parameters.

3 Select the performance criteria, and formulate relevant constraints. Choose the initial conditions, upper and lower bounds, and integrate any relevant additional factors.

For this design, the effect that will be examined is kT/C noise. This noise relates to the input capacitors C_S (as explained in Subsection 31.4.1), and as such is the parameter that will be optimized.

The step that follows involves designing the kT/C noise block for the integrator. The model used is based on the one seen in Figure 31.6, but requires some customization for this design. The first issue to deal with concerns the $f(u)$ block, and its variables (see Subsection 31.4.1). For this example, only one temperature point will be examined, so a fixed value of 300 degrees Kelvin

can be used for *T*. On top of this, C_S is needed in the formula. For the purpose of this optimization routine, C_S will be defined as *c*(1). Therefore, *c*(1) must appear in the equation. This allows for the optimization routine to directly interface with Simulink. Furthermore, since a normalized system was constructed in Simulink (i.e. the power supply is normalized to +1 V and –1 V), a value for *Supply_factor* should be chosen. Assuming that the power supply is 2.5 V, leads to a selection of 1.25 for *Supply_factor*. Upon the customization of the Simulink model, a full system diagram should be built. For this example, the diagram can be seen in Figure 31.19, and includes the Simulink kT/C modeling.

The next step that must be taken into account involves deciding what performance criteria will be used to determine a successful completion of the optimization routine. For simplicity, SNDR will be used as the sole performance indicator. In order to calculate this value, a Simulink system must be run, its output data points collected, and an FFT taken. For this modulator, 16 bits of performance is required (98 dB), and as a result, a constraint is placed on SNDR forcing it to be above 98 dB.

Finally, it is necessary to determine the initial conditions and bounds on the parameter C_S. Depending on the technology used, there is a minimum value of capacitance that can be manufactured with a certain pre-known degree of accuracy (usually 20%). Therefore, this value should be used for the lower bound on the capacitance. In this case 250 fF was chosen. The upper bound is usually limited by area constraints. In order to minimize area, one wants to use the smallest capacitance possible. In this case, the upper bound on capacitance was limited to 5 pF. A final decision remains concerning the selection of an initial condition. Basically, one can choose any value within the previously determined bounds.

At this point, there is enough information to create the optimization files. In the first file, seen in Figure 31.20, the system specifications are listed, the Kaiser window for the FFT is calculated, the initial conditions and finally the upper and lower bounds are set. The values listed correspond to numbers that are needed to make various calculations. For example, *Supply_factor* is needed for the kT/C noise block. *Npoints* refers to the number of points to be used in the FFT, while *fs* and *bw* correspond to the sampling frequency and bandwidth of the modulator. The value *band_edge* is a constant used to determine the last in-band point to be considered when calculating the FFT. The value *M*, determined by coherency, represents the bin in which the input signal lies. In this case, a frequency of 4312.5 Hz corresponds to an *M* of 23. Also defined in this file are the optimization options. The *options* vector contains the parameters used in defining the display format, coefficient accuracy, termination accuracy, constraint accuracy, the maximum number of iterations and the maximum step-size. Definitions and guidelines for choosing these values can be found in [10].

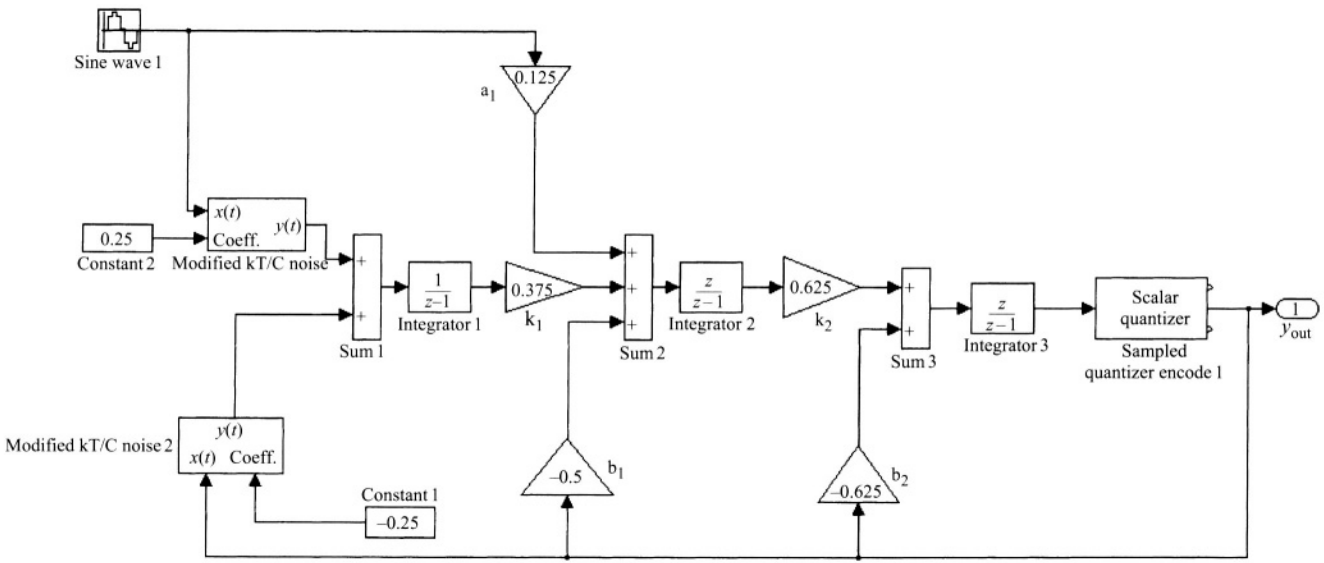


Figure 31.19. **Simulink system diagram with kT/C noise models ("*KTC_optim*").**

```
% File: optim_kTC.m

function [c] = optim_kTC();

warning off;

% Calculation of Constants

M = 23;              % Frequency of 4312.5 Hz
Npoints= 2^15;
Supply_factor = 1.25;
fs = 6.144e6;
bw = 24e3;
window1 = kaiser(Npoints,30);
band_edge = floor((bw/fs)*Npoints)+ 1;

% Starting values of Coefficient
% Cs    1e-12 (pF)
coef(1)= 3.0;

% Lower and Upper Bounds on the Coefficients
VLB = [0.25];
VUB = [5.0];

% Set up Optimization Options: Used to Define Tolernaces and Step Sizes
options = foptions;
options(1) = 1;
options(2) = .1;
options(3) = .01;
options(4) = .1;
options(14) = 1000;
options(16) = .1;
options(17) = 1;

[C,dummy]=constr('param_KTC',coef,options,VLB,VUB,[],Npoints,M,Supply_factor,window1,band_edge);
```

Figure 31.20. File "optim_kTC".

The second file, which is called in the last line of the previous one, can be seen in Figure 31.21. This file contains the call to Simulink model "KTC_optim", which was seen in Figure 31.19, the error calculation, and the constraints. The error condition is chosen to get the SNDR as close to 98 dB as possible. Dividing the V/V representation of 98 dB by the current SNDR in V/V does this. Ideally, this will give a value of one. As a result, one is subtracted to indicate that there is no error when this is achieved. This formulation penalizes SNDRs greater than 98 dB, but this is necessary to ensure that the smallest C_S possible is used. The constraint forcing the SNDR to be greater than 98 dB, can also be seen in this file.

By creating these two files along with the simulink diagram, this system can be simulated in Matlab. Once run, the optimization routine should quickly find a value for the minimum capacitance needed at the input stage. In this case, the result should be approximately 3.25 pF, and should take approximately 130 seconds of CPU time.

Based on this example involving kT/C noise along with the information gathered from the discussions in earlier sections, one has the necessary tools and background to easily expand upon these principles. Further, parameters that influence the non-idealities of the system, along with additional constraints to

```
% File: param_kTC.m

function [L2,g] = param_kTC(coeff,Npoints,M,Supply_factor,window1,band_edge);

% Running Simulink to get the stream
  disp('Simulation...');

inputs = simset('SrcWorkspace','current','DstWorkspace','base');

%Creating the Variables for Interface with Simulink

c(1) = [(coeff(1)*1e-12)];
Cs = c(1)

[tsim,xsystem,yout]=sim('KTC_optim',45700,inputs);

simtime = length(yout);
hy=(2*(abs(fft(yout(simtime-Npoints+1:simtime).*window1,Npoints))).^2)/((Npoints)*(Npoints-1));


%Calculate SNDR with Kaiser Window

noise1 = sum(hy(1:(M+1-floor(19/2)-1)));
noise2 = sum(hy((M+1+floor(19/2)+1):band_edge));
noise = noise1 + noise2;
noise = noise./((.402)^2);
peak = (hy(M+1))/(.2276^2);
sndr = 10*log10(peak/noise)
mag = peak/noise;

L2 = abs(((10{\^}(98/10))/mag) - 1)

disp('Done.');

% ******* set up constraints ***********
% constr <= 0

constr1 = -sndr + 98    % SNDR is greater than the SNDR goal

g = [constr1];
```

Figure 31.21. File "param_kTC".

more thoroughly define performance, can easily be added to develop a more accurate and comprehensive design.

31.8. Conclusion

A new design methodology for analog or mixed-signal integrated circuit components was presented, along with the benefits of a top–down optimization procedure. Foremost among these benefits was a shorter design cycle, along with ease of implementation and reproducibility. A major advantage of having adopted such a design strategy was its universal applicability to any design problem, provided that one has the ability to obtain formulas or rules of thumb to help guide the process. Once these formulas and rules of thumb have been obtained or decided upon, Matlab and Simulink could be used to model them, and an optimization procedure could be conceived, as per the guidelines presented in this chapter. In order to more easily understand and apply this procedure, Simulink modeling along with several design procedures and considerations were presented. Furthermore, the design of a $\Delta\Sigma$ modulator using

this methodology was carried out to more concretely illustrate the benefits of a top–down design methodology using Matlab and Simulink.

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Chapter 32

TECHNIQUES AND APPLICATIONS OF SYMBOLIC ANALYSIS FOR ANALOG INTEGRATED CIRCUITS

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32.1. Introduction

Symbolic analysis of electronic circuits received much attention during the late 1960s and the 1970s, where a lot of computer-oriented analysis techniques were proposed. Since the late 1980s, symbolic analysis of electronic circuits has gained a renewed and growing interest in the electronic design community [1,2]. This is illustrated by the success of modern symbolic analyzers for analog integrated circuits such as ISAAC [3,4], ASAP [5,6], SYNAP [7,8], SAPEC [9], SSPICE [10], SCYMBAL [11], SCAPP [12], Analog Insydes [13], CASCA [14], SIFTER [15] and RAINIER [16].

In Section 32.2, the technique of symbolic circuit analysis is first defined and illustrated for some practical examples. The basic methodology of how symbolic analysis works is explained. Section 32.3 then presents the different applications of symbolic analysis in the analog design world, and indicates the advantages and disadvantages of symbolic analysis compared to other techniques, especially numerical simulation. Section 32.4 then describes the present capabilities and limitations in symbolic analysis, and details recent algorithmic advances, especially for the analysis of large circuits. Finally, an overview of existing tools is presented in Section 32.5, and conclusions are provided in Section 32.6.

32.2. What is Symbolic Analysis?

32.2.1. Definition of Symbolic Analysis

Symbolic analysis of an analog circuit is a formal technique to calculate the behavior or a characteristic of a circuit with the independent variable (time or frequency), the dependent variables (voltages and currents) and (some or all of) the circuit elements represented by symbols. The technique is complementary to numerical analysis (where the variables and the circuit elements are represented by numbers) and qualitative analysis (where only qualitative

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values are used for voltages and currents, such as increase, decrease or no change). A symbolic simulator is then a computer program that receives the circuit description as input and can automatically carry out the symbolic analysis and thus generate the symbolic expression for the desired circuit characteristic.

Almost all of the symbolic analysis research carried out in the past concerned the analysis of linear circuits in the frequency domain. For lumped, linear, time-invariant circuits, the symbolic network functions obtained are rational functions in the complex frequency variable x (s for continuous-time and z for discrete-time circuits) and the circuit elements p_i that are represented by a symbol (instead of a numerical value):

$$H(x) = \frac{\sum_i x^i a_i(p_1, \ldots, p_m)}{\sum_j x^j b_j(p_1, \ldots, p_m)} \tag{32.1}$$

where $a_i(..)$ and $b_i(..)$ are symbolic polynomial functions in the circuit elements p_i. In general, these symbolic equations can be expanded in sums-of-products form or can be in nested form.

In a fully symbolic analysis all circuit elements are represented by symbols. But a mixed symbolic–numerical analysis is also possible where only part of the elements are represented by symbols and the others by their numerical values. In the extreme case with no symbolic circuit elements, a rational function with numerical coefficients is obtained with the frequency variable (s or z) as only symbol.

Note that the symbols in these expressions represent the elements that are present in the linear circuit. In case of semiconductor circuits, the devices are typically linearized around their operating point and the symbols therefore represent the elements in the small-signal expansion (e.g. g_m, g_o, etc.) of these devices. As long as the topology of the small-signal device expansion remains the same, the resulting expressions (in terms of g_m, g_o, etc.) remain valid, independent of the particular device model used (e.g. SPICE level 2, BSIM, etc.) and to some extent also independent of the operating region of the device (although the results of course depend on the operating point when symbolic simplification techniques are used). Only when the equations are numerically evaluated or when the small-signal elements are further symbolically substituted by their describing equations, then a particular set of device model equations has to be used to relate the small-signal elements to the device sizes and biasing. For complicated models, the symbolic equations might soon become too cumbersome though to be interpretable by designers.

The technique of symbolic analysis is now illustrated for two practical examples, a continuous-time and a discrete-time filter.

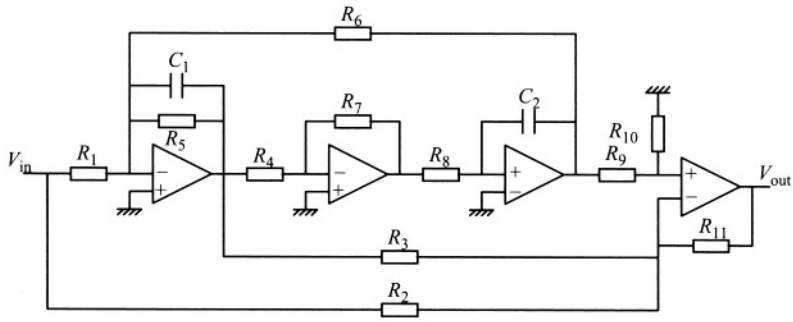


Figure 32.1. Active RC filter.

Example 32.1. Consider the active RC filter of Figure 32.1. Starting from the circuit description of this filter, a symbolic analysis program will return the following symbolic expression for the transfer function of this filter:

$$\begin{aligned}&\{-G_4G_8(G_1G_2G_9 + G_1G_3G_9 + G_1G_9G_{11} + G_2G_6G_9 + G_2G_6G_{10})\\&\quad + sG_7C_2(G_1G_3G_9 + G_1G_3G_{10} - G_2G_5G_9 - G_2G_5G_{10})\\&\quad - s^2G_2G_7C_1C_2(G_9 + G_{10})\}/\\&\quad \{G_{11}(G_9 + G_{10})(G_4G_6G_8 + sG_5G_7C_2 + s^2G_7C_1C_2)\}\end{aligned} \tag{32.2}$$

where G_x is the conductance corresponding to resistor R_x in the schematic of Figure 32.1. The operational amplifiers have been considered ideal in this case, but other, more realistic op-amp models are possible as well.

Example 32.2. As a second example, consider the switched-capacitor biquad of Fleischer and Laker of Figure 32.2. Starting from the circuit description of this filter and the timing information of the clock phases, a symbolic simulator automatically generates the following symbolic expression for the z-domain transfer function of this filter (with op-amps considered as ideal) from the input (sampled at phase 1 and held constant during phase 2) to the output (at phase 1):

$$\begin{aligned}&\{DK + DJ - AL - AH\\&\quad + z(-2DK + AL + AG - DJ - DI) + z^2D(K + I)\}/\\&\quad \{AE - DB + z(-AE + 2DB - AC + DF) - z^2D(F + B)\}\end{aligned} \tag{32.3}$$

where the symbols A–L represent the capacitors in the schematic of Figure 32.2. When the input and output are considered during other phases, other transfer

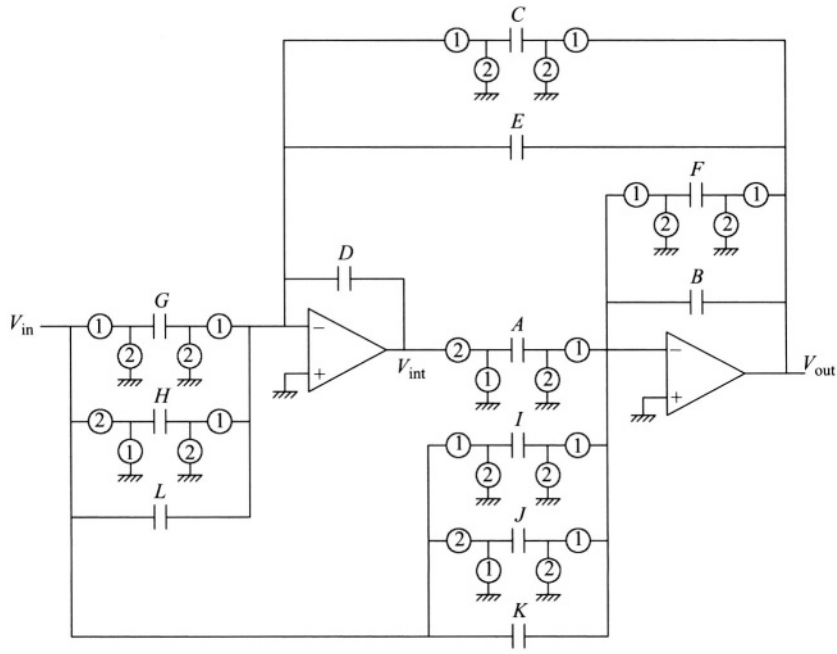


Figure 32.2. Switched-capacitor biquad.

functions are obtained. Note that only a limited number of symbolic analysis tools can handle time-discrete circuits, for instance, the tools described in [4,11,17,18].

32.2.2. Basic Methodology of Symbolic Analysis

The principle operation of symbolic analysis programs can now be explained. The basic flow is illustrated in Figure 32.3 with the example of a bipolar single-transistor amplifier. The input is a netlist description of the circuit to be analyzed (for example in the well known SPICE syntax). Since symbolic analysis is primarily restricted to linear circuits, the first step for nonlinear analog circuits (such as the amplifier in Figure 32.3) is to generate a linearized small-signal equivalent of the circuit. In the example of Figure 32.3, only the dc model is shown in order not to overload the drawing. In general, circuits consisting of resistors, capacitors, inductors, independent and controlled sources can be handled by most symbolic analyzers.

After the user has indicated the network function (i.e. the input and output) that he wants, the analysis can start. For this, two basic classes of methods exist

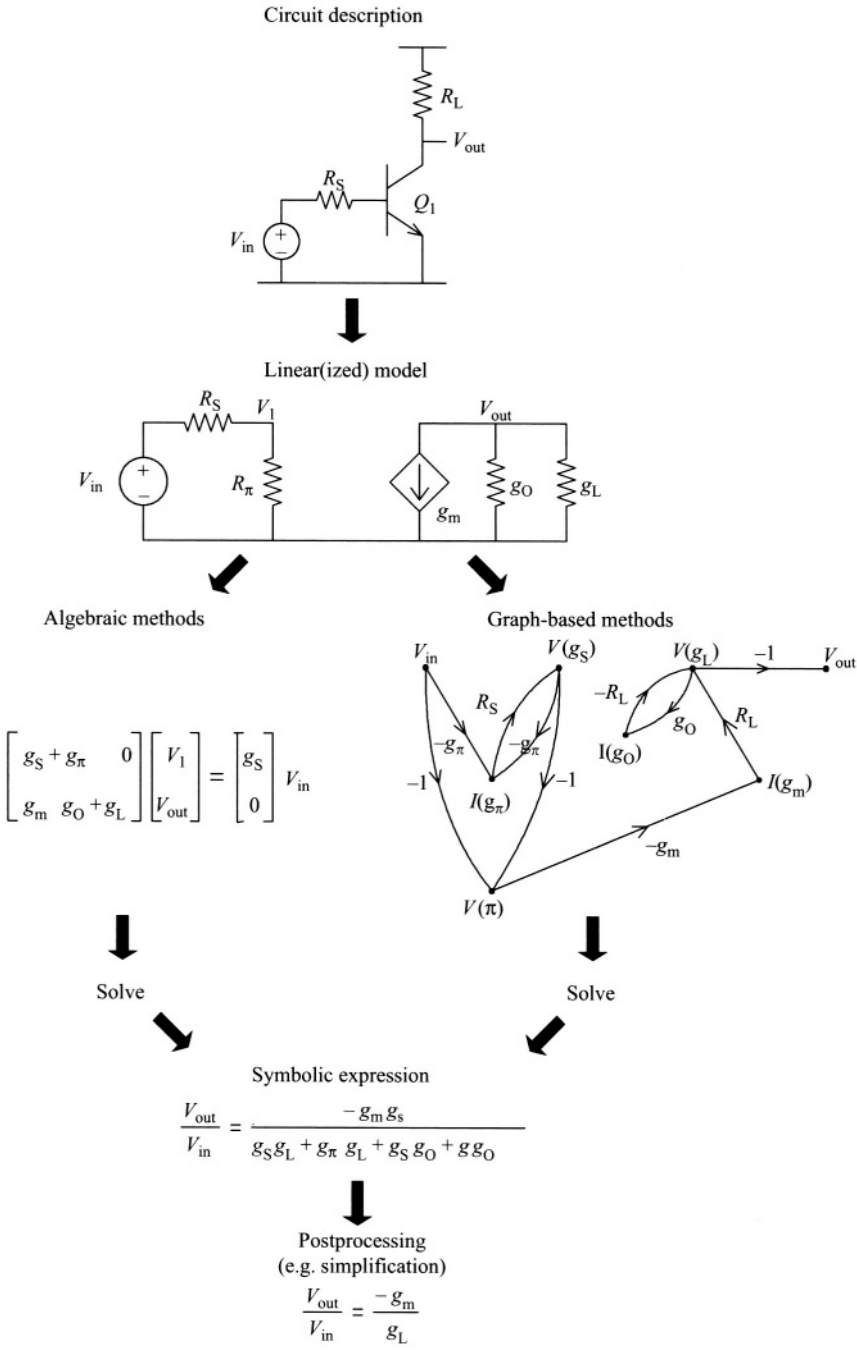


Figure 32.3. Basic flow of symbolic analysis.

(as shown by the two paths in Figure 32.3) [19,20]:

1 In the class of *algebraic (matrix- or determinant-based) methods,* the behavior of the linear(ized) circuit is described by a set of equations with symbolic coefficients. The required symbolic network function is obtained by algebraic operations on this set of equations (such as, for instance, a symbolic expansion of the determinant).

2 In the class of *graph-based (or topological) methods,* the behavior of the linear(ized) circuit is represented by one or two graphs with symbolic branch weights. The required symbolic network function is obtained by operations on these graphs (such as for instance the enumeration of loops or spanning trees).

Whatever the symbolic analysis method followed, the expression generated can then further be postprocessed in symbolic format. For example, and especially in the case of the small-signal analysis of semiconductor circuits, the network function can further be simplified or approximated. This means that information of the relative magnitudes of the circuit elements (of course depending on the operating point) is used to discard, up to a maximum user-defined error, smaller terms with respect to larger terms in order to obtain a less complicated symbolic expression with only the dominant contributions (see Section 32.4 for details). Other symbolic postprocessing operations could be factorization of results, or symbolic substitutions of certain symbols by their expressions, etc. The result after postprocessing is then returned to the user or can be used in other design applications or for numerical postprocessing (e.g. evaluations).

32.3. Applications of Symbolic Analysis

This section now summarizes the major applications of symbolic analysis in the design of analog circuits [1,2,20].

32.3.1. Insight into Circuit Behavior

Symbolic analysis provides closed-form symbolic expressions for the characteristics of a circuit. It is an essential complement to numerical simulation, where a series of numbers is returned (in tabulated or plotted form). Although these numbers can accurately simulate the circuit behavior, they are specific for a particular set of parameter values. With numerical simulation, the functional behavior of the circuit can be verified in a very short time for the given parameter set. But no indication is given of which circuit elements determine the observed performance. No solutions are suggested when the circuit does

not meet the specifications. A multitude of simulations is required to scan performance trade-offs and to check the influence of changes in the parameter values.

A symbolic simulator on the other hand returns first-time correct analytic expressions in a much shorter time and for more complex characteristics and circuits than would be possible by hand. The resulting symbolic expressions remain valid even when the numerical parameter values change (as long as all models remain valid). As such, symbolic analysis gives a different perspective on a circuit than that provided by numerical simulators, which is most appropriate for students and practising designers to obtain real insight into the behavior of a circuit [20,21]. This is especially true if the generated expressions are simplified to retain the dominant contributions only, as already discussed before. With symbolic simulation, circuits can be explored without any hand calculation in a fast and interactive way. This is illustrated in the following example.

Example 32.3. Consider the CMOS three-stage amplifier of Figure 32.4 with nested Miller compensation. (The stages are represented by equivalent circuits because we are interested in the stability properties of the overall amplifier in this example). In the presence of the two compensation capacitors, the 25% maximum-error simplified transfer function with the dominant contributions is given by:

$$\frac{-g_{m1}(g_{m2}g_{m3} + sg_{m2}C_{C1} + s^2C_{C1}C_{C2})}{g_{o1}g_{o2}g_L + sg_{m2}g_{m3}C_{C2} + s^2(g_{m3} + g_L - g_{m2})C_{C1}C_{C2} + s^3C_{C1}C_{C2}C_L} \tag{32.4}$$

This expression clearly provides insight into the stability properties of this amplifier. The two compensation capacitors C_{C1} and C_{C2} can stabilize the circuit, provided that $g_{m3} + g_L$ is larger than g_{m2}. Also, C_{C1} and C_{C2} cause one left-half-plane zero and one right-half-plane zero, which influence the phase margin.

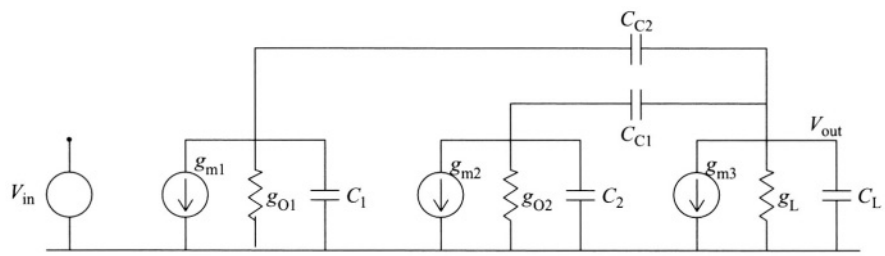


Figure 32.4. Principle schematic of a three-stage amplifier with nested Miller compensation.

In addition to improving the insight of students and novice designers, a symbolic simulator is also a valuable design aid for experienced designers, to check their own intuitive knowledge, and to obtain analytic expressions for second-order characteristics such as the power-supply rejection ratio or the harmonic distortion, which are almost impossible to calculate by hand, especially at higher frequencies and in the presence of device mismatches. On the downside, symbolic analysis is limited to much smaller circuit sizes and fewer analysis types (e.g. no transient simulation yet) than numerical simulation and inevitably takes much longer CPU times for the same circuit and type of analysis.

32.3.2. Analytic Model Generation for Automated Analog Circuit Sizing

A symbolic simulator can automatically generate all ac characteristics in the analytic model of a circuit. Such a model, that approximates the behavior of a circuit with analytic formulas, can then be used to efficiently size the circuit in an optimization program. An alternative is to use a numerical simulator to evaluate the circuit performance. Optimization time, however, is strongly reduced by replacing the full numerical simulation at each iteration with an evaluation of the analytic model equations. This approach is explicitly adopted in the OPTIMAN [22] and OPASYN [23] programs. The use of an equation manipulation program such as DONALD [24] even allows to automatically construct a design plan by ordering the equations of the analytic model such as to optimize the efficiency of each evaluation of this analytic model. To this end, DONALD constructs a computational path: it determines for the given set of independent variables the sequence in which the equations have to be solved, grouped into minimum subsets of simultaneous equations [24].

Other analog synthesis programs of course also rely on analytic information mixed with heuristics and design strategies. In IDAC [25] and OASYS [26], for example, all this knowledge has to be converted manually into schematic-specific design plans. Tools like CATALYST [27] and SD-OPT [28] use analytic equations from the tool's library to perform the architectural-level design of specific classes of analog-to-digital converters in terms of their subblocks. The manual derivation of the analytic equations, however, is a time-consuming and error-prone process that has to be carried out for each circuit schematic. The use of a symbolic simulator largely reduces the effort required to develop the analytic model for a new circuit schematic. In this way, an open, non-fixed-topology analog CAD system can be created, in which the designer himself can easily include new circuit topologies. This approach is adopted in the AMGIE [20,29] and ADAM [30] analog design systems.

It can be objected that the exponential growth of the number of terms with the circuit size in expanded symbolic expressions makes the evaluation of such expressions for automatic circuit sizing less efficient than a simple numerical simulation. Therefore, for applications requiring the repetitive evaluation of symbolic expressions, one solution is to use expressions that have been simplified for typical ranges of the design parameters. If in addition to evaluation efficiency full accuracy is also required, then the non-simplified symbolic expressions have to be generated in the most compact form, demanding for nested formats. On the other hand, for interactive use and to obtain insight into the circuit behavior, the symbolic expressions are better expanded and simplified.

32.3.3. Interactive Circuit Exploration

Symbolic simulation can be used to interactively explore and improve new circuit topologies. The influence of topology changes (e.g. adding an extra component) can immediately be seen from the new, resulting expressions. A powerful environment for the design and exploration of analog circuits then consists of a schematic editor, both a symbolic and a numerical simulator in combination with numerical and graphical postprocessing routines and possibly optimization tools. In this way, the interactive synthesis of new, high-performance circuits becomes feasible.

Moreover, in [31] a method is presented to automatically generate new circuit schematics with the combined aid of a symbolic simulator and the PROLOG language. A PROLOG program exhaustively generates all possible topologies with a predefined set of elements (e.g. one op-amp and three capacitors). The switched-capacitor-circuit symbolic simulator SCYMBAL then derives a symbolic transfer function for each structure. A PROLOG routine finally evaluates this function to check whether it fulfills all requirements (e.g. a stray-insensitive switched-capacitor integrator function with low op-amp-gain sensitivity).

32.3.4. Repetitive Formula Evaluation

The use of symbolic formulas is also an efficient alternative if a network function has to be evaluated repeatedly for multiple values of the circuit components and/or the frequency. For such applications, the technique of compiled-code simulation can be used. The symbolic expressions for the required network functions are generated once and then compiled. This same compiled code can then be evaluated many times for particular values of the circuit and input parameters. This technique can be more efficient than performing a full numerical simulation for each set of circuit and input parameters. The efficiency of this technique has been shown in [11] for the analysis of switched-capacitor circuits.

Another obvious application is in statistical analysis (e.g. Monte Carlo simulations where the same characteristics have to be evaluated many times in order to assess the influence of statistical device mismatches and process tolerances on the circuit performance), large-signal sensitivity analysis, yield estimation and design centering. An application reported in [32] is the characterization of a semiconductor device as a function of technological and geometrical parameters.

If the values of all components of a circuit are known, then symbolic analysis can also be an efficient alternative to obtain frequency spectra of the characteristics of that circuit. In that case, the symbolic analysis has to be carried out with only the frequency variable represented by a symbol and the circuit parameters by their numerical value. This results in an exact, non-simplified rational function in s or z, which can be evaluated for many different frequency points. This technique can be more efficient than repeated numerical simulations in for example sensitivity analysis or distortion analysis. If in addition to the frequency variable also one or two circuit elements are retained as a symbol, the frequency spectra can be parameterized with respect to these symbolic elements. The same expressions in s or z can also be used to numerically derive poles and zeros, and generate pole–zero position diagrams as a function of one of the symbolic parameters. (These can then be compared to the results of any symbolic expressions derived for poles and zeros, if available). It has been shown in [33] that the CPU time needed to numerically evaluate such parametrized symbolic-numerical characteristics is much lower than that of a full numerical simulation, up to five orders of magnitude in one example, which is essential in highly iterative applications.

Example 32.4. Figure 32.5 shows the position on the frequency axis of the gain–bandwidth (*), poles (solid lines) and zeros (dotted lines) for the three-stage amplifier of Figure 32.4 as a function of the value of the compensation capacitor C_{C1} for a constant C_{C2} value. The expression for the transfer function was first derived semi-symbolically as a function of C_{C1} and s, and the roots were then solved numerically for different values of C_{C1}. The information of Figure 32.5 can be used to select the optimum design values to stabilize this amplifier.

32.3.5. Analog Fault Diagnosis

The application of the symbolic technique in fault diagnosis of linear and nonlinear analog circuits is also interesting [34]. Using the symbolic network function, the circuit response is evaluated many times so as to determine those numerical values of the components that best fit the simulated response with the measured one. Based on the resulting component values, it can be decided

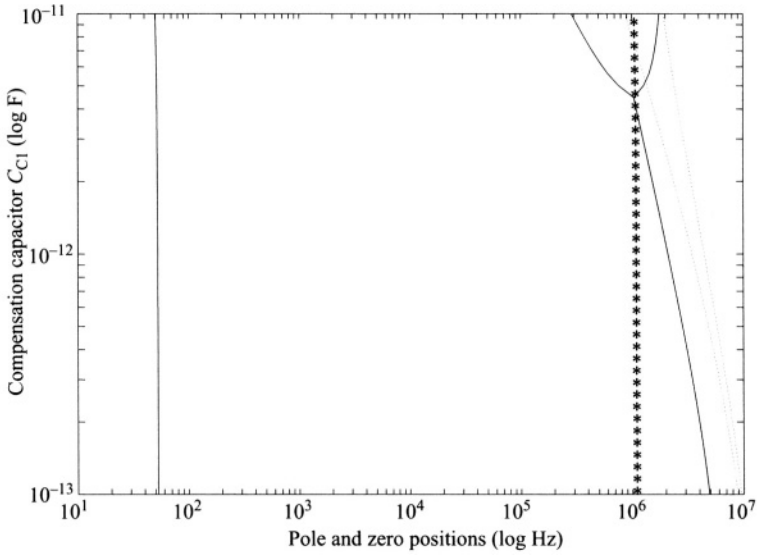


Figure 32.5. Diagram of the frequency positions of the poles (solid lines) and zeros (dotted lines) for the three-stage amplifier as a function of C_{C1}.

which component is faulty. For nonlinear devices a piecewise-linear approximation is used. Reactive elements are replaced by their backward-difference models. The time-domain simulations are then carried out by means of a Katznelson-type algorithm.

As shown in Figure 32.6, an interesting aspect of the approach is that the symbolic expression is generated only once for the circuit and then together with the code of the simulation algorithm compiled into a dedicated simulator, specific for that circuit. During the fitting of the output response, this dedicated simulator is called many times for the given input signal with different numerical values for the components. Symbolic expressions have also been used in testability analysis to determine the observability of a circuit for a given number of observation nodes [35].

32.3.6. Behavioral Model Generation

Symbolic simulation can also easily be used to automatically generate behavioral models for certain analog blocks such as op-amps and filters, which are most naturally described by transfer functions in s or z. Such behavioral models are required to simulate higher-level systems in acceptable CPU times, or in top-down design.

A big problem for general nonlinear circuits and general transient characteristics, however, is the generation of an accurate behavioral model. Therefore, in

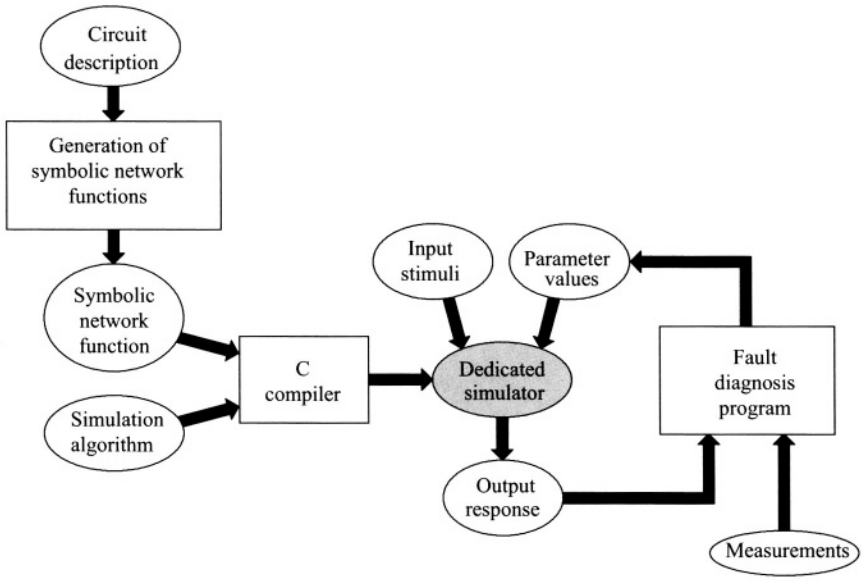


Figure 32.6. Principle of analog fault diagnosis using dedicated compiled code simulators.

[36], an approach based on symbolic simplification techniques was explored. First, the general nonlinear differential-algebraic symbolic equations of the circuit are set up. These are then simplified using both global (e.g. complete elimination of a variable) and local (e.g. pruning of a term or expansion of a nonlinear function in a truncated series) approximations. The resulting simplified expressions form the behavioral model and are converted into the desired hardware description language. In this way simulation speed-ups between 4 × and 10 × have been reported [36]. The critical part of the method is the estimation of the approximation error. Since the circuit is nonlinear, this can only be done for a specific circuit response (e.g. dc transfer characteristic). For other responses, other models have to be generated or the error is not guaranteed.

32.3.7. Formal Verification

Another recent application is analog formal verification [37]. The goal is to prove that a given circuit implementation implements a given specification. For linear(ized) circuits both the circuit implementation and the specification can be described with symbolic transfer functions. Algorithms have then been developed to numerically calculate an outer bound for the characteristic of the circuit implementation, taking into account the variations of process parameters and operating conditions, and an inner bound for the characteristic of the specification. If the former is enclosed by the latter, then it is formally proven

that the circuit is a valid implementation of the specification. The algorithms are however very time consuming and the extension to nonlinear circuits or characteristics is not at all obvious.

32.3.8. Summary of Applications

We can now summarize the major applications of symbolic analysis in analog design as follows:

- knowledge acquisition and educational/training purposes (insight)
- analytic model generation for automated circuit sizing in an open, flexible-topology analog design system
- design space exploration and topology generation
- repetitive formula evaluation, for example, statistical analysis
- analog fault diagnosis and testability analysis
- analog behavioral model generation
- analog formal verification
- etc.

It can be concluded that symbolic analysis has a large potential for analog circuit analysis and design. It will now be described in the next section what the present capabilities and limitations of the symbolic analysis algorithms are. This will allow the reader to assess whether the above promising potential can be exploited by designers in real life or not.

32.4. Present Capabilities and Limitations of Symbolic Analysis

The different types of circuits that can be analyzed symbolically nowadays and the different types of symbolic analyses which are presently feasible on these circuits are shown in highlighted form in Figure 32.7. For many years, symbolic simulation has only been feasible for the analysis of lumped, linear, time-continuous and time-discrete (switched-capacitor) analog circuits in the frequency domain (s or z). Nonlinear circuits, including both MOS and bipolar devices, are then linearized around the dc operating point, yielding the small-signal equivalent circuit. In this way, analytic expressions can be derived for the ac characteristics of a circuit, such as transfer functions, common-mode rejection ratio, power-supply rejection ratio, impedances, noise.

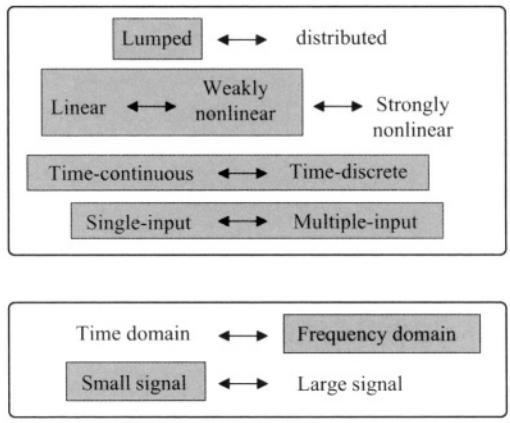


Figure 32.7. Overview of present capabilities of symbolic analysis.

Originally, the size of the circuits that could be analyzed in a symbolic way was rather restricted (a few transistors) [38], partially because of the poor algorithms used and partially because of the complexity (large number of terms for even a small circuit) that make the resulting expressions intractable for designers. The introduction of symbolic simplification or approximation techniques in the late 1980s [4,7], therefore, was a first step to improve both the interpretability and extend the maximum analyzable circuit size. In recent years, other techniques have been developed to extend the capabilities of symbolic analysis both in terms of the functionality offered to the user and in terms of the computational efficiency for larger circuits. These improvements will now be described in detail.

32.4.1. Symbolic Approximation

ISAAC [3,4] and SYNAP [7,8], later on followed by other tools like ASAP [5,6] and SSPICE [10], have introduced the idea of approximation (or simplification or truncation or pruning) of the symbolic expressions. Due to the exponential growth of the number of terms with the circuit size (e.g. more than 4.5×10^{17} terms in the system denominator of the well known μA741 op-amp), the symbolic expressions for analog integrated circuits rapidly become too lengthy and complicated to use or interpret, rendering them virtually useless. Fortunately, in semiconductor circuits, some elements are much larger in magnitude than others. For example, the transconductance of a transistor is usually much larger than its output conductance. This means that the majority of the terms in the full symbolic expression are relatively unimportant, and that only

a small number of dominant terms are important to really determine the circuit behavior and, therefore, also to gain insight into this behavior.

This observation has led to the technique of symbolic expression approximation where the symbolic expressions are simplified based on the relative magnitudes of the different elements and the frequency, defined in some nominal design point or over some range [3,7]. Conceptually, this means that the smaller-size terms are discarded with respect to the larger-size terms, so that the resulting simplified expression only contains a small and interpretable number of dominant contributions, that still describes the circuit behavior accurately enough. Of course, this introduces some error ε equal to the contribution of the discarded terms, but the maximum error allowed $\varepsilon_{\max}$, and hence also the number of terms in the final expression, is in most programs controllable by the user. The goal of simplification, therefore, is to find, based on the (order of) magnitude of the circuit elements (or their ranges) and the frequency variable (or its range), an approximating symbolic expression $h(\underline{\mathbf{p}})$ for the original symbolic circuit characteristic $g(\underline{\mathbf{p}})$ such that [20]:

$$\left\| \frac{g(\underline{\mathbf{p}}) - h(\underline{\mathbf{p}})}{g(\underline{\mathbf{p}})} \right\| \leq \varepsilon_{\max} \tag{32.5}$$

where the circuit parameters $\underline{\mathbf{p}}$ (and the frequency) are evaluated over a certain range or in a nominal design point $\underline{\mathbf{p}}_0$, and the error is measured according to some suitable norm. Symbolic expression approximation is thus a trade-off between expression accuracy (error) and expression simplicity (complexity). Note that in many tools the error $\varepsilon_{\max}$ is applied to each frequency coefficient separately, although in reality the changes in the magnitude and phase as well as in the poles and zeros of the overall network function should be controlled to within $\varepsilon_{\max}$ by the simplification algorithm [39]. Originally, the error was only evaluated in one nominal design point (which could also be a typical set of default values), but then the error could be much larger outside this single design point. Therefore, in [39] the error criterion was extended to consider ranges for all circuit elements, turning all calculations into interval arithmetic operations.

Example 32.5. Consider the low-frequency value of the power-supply rejection ratio for the positive supply voltage of the CMOS two-stage Miller-compensated op-amp of Figure 32.8. For a 25% maximum approximation error, the denominator is reduced from 56 terms to 6 dominant terms. The simplified symbolic expression with the dominant contributions is given by:

$$\frac{2g_{m1}g_{m1}g_{m2}g_{m3}}{g_{m1}(g_{o1}+g_{o2})(2g_{m2}g_{o4}-g_{m3}g_{o5})+(\Delta g_{m2BA}g_{m1}-\Delta g_{m1BA}g_{m2})g_{m3}g_{o5}} \tag{32.6}$$

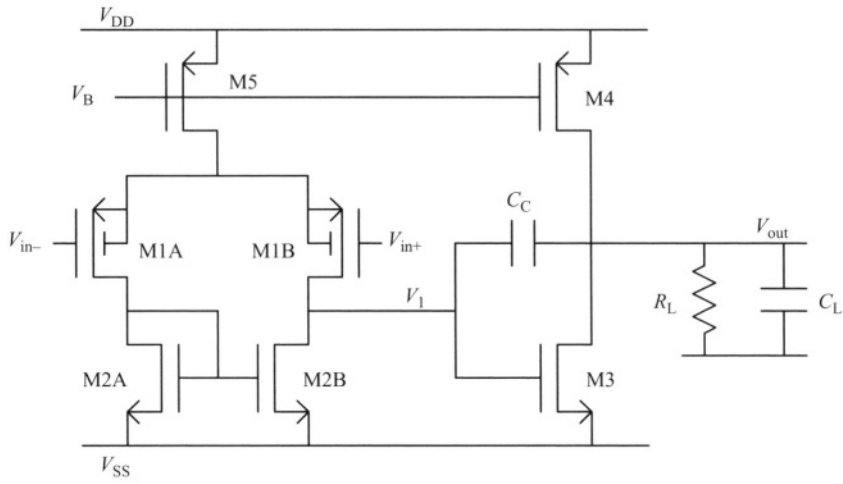


Figure 32.8. CMOS two-stage Miller-compensated op-amp.

where the Δ-symbols are the explicit symbolic representation of the statistical mismatch in transconductance between the matching transistors M1A–M1B and M2A–M2B, respectively. Approximated results like (32.6) show the dominant contributions only, and are thus convenient for obtaining insight into the behavior of a circuit. In this example, the power-supply rejection ratio is analyzed, which is a complicated characteristic even for experienced designers. The partial cancelation between the nominal contributions of the first and the second stage, and the influence of mismatches can easily be understood from expression (32.6).

32.4.2. Improving Computational Efficiency

The main limitation inherent to symbolic analysis and hence to all symbolic analysis techniques, is the large computing time and/or memory storage, which increase very rapidly with the size of the network, especially for expanded expressions. This is mainly due to the exponential rise of the number of terms with the complexity of the circuit. As a result, this limits the maximum size of circuit that can be analyzed in a symbolic way [20]. In recent years, however, a real breakthrough was achieved with new algorithmic developments that have largely reduced the CPU time and memory consumption required for large circuits, and that have made possible the symbolic analysis of analog circuits of practical size (up to 40 transistors). These developments of course avoid the complete expansion of the exact expression.

Figure 32.9 situates the different simplification techniques, depending on the place in the symbolic analysis process flow where the simplifications are

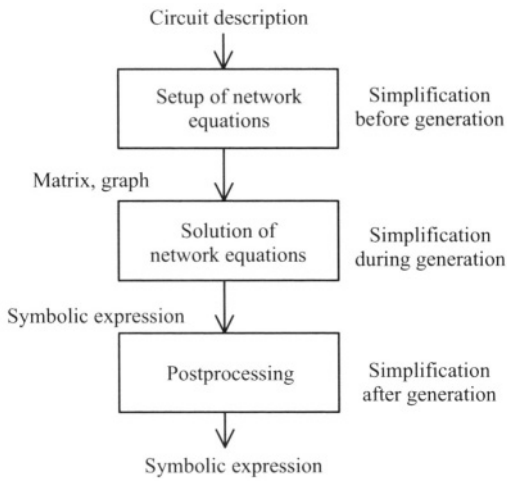


Figure 32.9. **Different simplification techniques in symbolic analysis.**

introduced. The original simplification techniques first generated the complete exact expression in fully expanded format (in order to elaborate any term cancelations), after which the smallest terms were pruned repeatedly as long as the allowed error was not exceeded. This technique can be called *simplification after generation (SAG).* Tools based on this technique like the original ISAAC [3,4], SYNAP [7] or ASAP [5,6] were restricted to circuits with a maximum of 10 to 15 transistors (depending on the actual topology configuration).

32.4.3. Simplification During Generation

An improvement to save CPU time and memory was to generate the exact expression in nested format and to carry out a lazy expansion [8], where the initially nested expression is expanded term by term with the largest terms first until the error is below the required limit. With this technique, simplified results have been generated for circuits with up to 25 transistors. When using nested formulas, however, extensive care must be paid to term cancelations. Therefore, more viable and inherently cancelation-free alternative are the recent *simplification during generation (SDG)* techniques [16,40,41] (see Figure 32.9) that don't generate the exact expression but directly build the wanted simplified expression by generating the terms one by one in decreasing order of magnitude, until the approximation error is below the maximum user-supplied value. This problem can be formulated as finding the bases of the intersection of three matroids in decreasing order of magnitude, which, however, in general, is an NP-complete problem. Applied to the two-graph method the three matroids involved are the graphic matroids corresponding to the voltage and current

graph of the circuit and the partition matroid corresponding to the correct number of reactive elements needed to have a valid term of the frequency coefficient under generation. Fortunately, polynomial-time algorithms have been developed to generate bases of the intersection of two matroids in descending order. For each base generated in this way it then has to be checked whether it is also a base in the third matroid. Such techniques have been implemented in SYMBA [41] and in RAINIER [16], and other developments are still going on. With these techniques large analog circuits can be analyzed with sizes corresponding to the current industrial practice (25 to 30 transistors). A benchmark example is the well known μA741 op-amp.

Example 32.6. Another example, a fully differential BiCMOS op-amp, is shown in Figure 32.10. The simplified expression of the gain of this op-amp can (after factorization of the results) be obtained as:

$$A_{V0} = \frac{g_{m,M2}}{g_{m,M1}} \frac{g_{m,M4}}{(g_{o,M4}g_{o,M5}/(g_{m,M5} + g_{mb,M5}) + (G_a + g_{o,M9} + g_{o,Q2})/\beta_{Q2})} \tag{32.7}$$

A more coarse approach in the same SDG line but that does not allow the user to accurately control the error was presented in [42]. The circuit elements are grouped in equivalence classes of the same order of magnitude, and the determinant is calculated by trying different combinations of equivalence classes in descending order of magnitude until the simplified symbolic expression is obtained as the first nonzero group of terms resulting from such a combination.

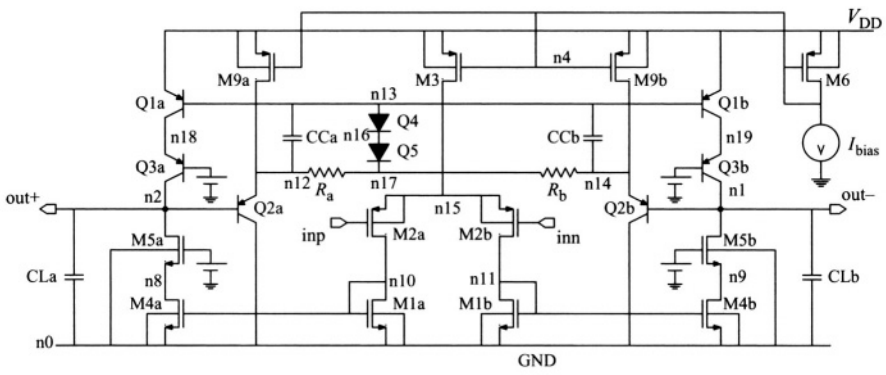


Figure 32.10. BiCMOS fully differential op-amp.

AWE symbolic [43], on the other hand, uses Asymptotic Waveform Evaluation (AWE) to produce a low-order symbolic approximation of the circuit response, both in time and frequency domain. Significant elements that have to be represented by a symbol are identified by means of numerical pole–zero sensitivity analysis in AWE. Numerical and symbolic computations are substantially decoupled by the use of moment-level partitioning. The method is most successful when only a small number of elements are represented by symbols.

32.4.4. Simplification Before Generation

In order to extend the capabilities of symbolic analysis to even larger circuits (40–50 transistors) that are still handled as one big, flat circuit, the only possibility today is to introduce simplification on the circuit schematic, on the circuit matrix or the circuit graph(s) before the symbolic analysis starts. This technique is therefore called *simplification before generation (SBG)* (see Figure 32.9) and corresponds to operations like *a priori* throwing away unimportant elements or shorting nodes, but also partial removals of elements become possible, for instance, by removing only one or two of the entries out of the complete stamp of an element in an MNA-type matrix. Note that the principle of SBG is exactly the same as designers use during hand calculations, as the calculations become intractable otherwise anyway. The same also applies to a symbolic analysis tool. The golden rule to get interpretable results from a symbolic analysis run is to simplify the circuit as much as possible in advance. A typical example is the replacement of biasing circuitry by a single voltage or current source with source impedance. Normally the devices in this biasing circuitry do not show up in the final simplified expressions, but they do complicate the symbolic calculations unnecessarily. The added value of SBG is that it quantifies the impact of every simplification. Yet, controlling the overall error is still the most difficult part of these methods.

In Analog Insydes [13], the simplifications are performed on the system matrix and the Sherman–Morrisson theorem is used to calculate the influence of the simplifications. In SIFTER [15], a combination of SBG, SDG and SAG is used. First, circuit parameters are eliminated from the cofactor during determinant calculation provided that the removal causes an error smaller than the allowed margin. Next, dimension reduction is tried and heuristic row and column operations are applied to increase the sparseness of the matrix, after which the determinant is expanded and possibly factorized.

32.4.5. Hierarchical Decomposition

If one wants to extend the capabilities of symbolic simulation to even larger circuits, it is clear that the generation of expanded expressions is no longer

feasible or results in uninterpretable expressions, and that the only solution is to generate and keep the expressions in nested format. Due to the problem of term cancelations this approach is most useful only for circuits that consist of loosely coupled subcircuits, like for instance active filter structures.

An interesting method in this respect is the use of *hierarchical decomposition* [12,44–46]. The circuit is recursively decomposed into more or less loosely connected subcircuits. The lowest-level subcircuits are analyzed separately and the resulting symbolic expressions are combined bottom-up (in nested format, without expansion) according to the previously determined decomposition hierarchy, resulting in the global nested expression for the complete circuit. This is now illustrated in the following example.

Example 32.7. Consider the theoretical example of Figure 32.11(a). The circuit (node 1 in the decomposition tree of Figure 32.11(b)) is decomposed into two parts (corresponding to nodes 2 and 3), which are each decomposed again into the leaf subcircuits A and B (for node 2) and C, D and E (for node 3). The leaf subcircuits are then analyzed by the symbolic simulator resulting in the following sets of symbolic transfer functions $\boldsymbol{H}_i$:

$$\boldsymbol{H}_{\mathrm{A}} = f_{\mathrm{A}}(s, \boldsymbol{p}_{\mathrm{A}}) \tag{32.8}$$

$$\boldsymbol{H}_{\mathrm{B}} = f_{\mathrm{B}}(s, \boldsymbol{p}_{\mathrm{B}}) \tag{32.9}$$

$$\boldsymbol{H}_{\mathrm{C}} = f_{\mathrm{C}}(s, \boldsymbol{p}_{\mathrm{C}}) \tag{32.10}$$

$$\boldsymbol{H}_{\mathrm{D}} = f_{\mathrm{D}}(s, \boldsymbol{p}_{\mathrm{D}}) \tag{32.11}$$

$$\boldsymbol{H}_{\mathrm{E}} = f_{\mathrm{E}}(s, \boldsymbol{p}_{\mathrm{E}}) \tag{32.12}$$

where $\boldsymbol{p}_{\mathrm{Y}}$ are the symbolic circuit parameters for leaf subcircuit Y. The transfer functions for the non-leaf subcircuits up the decomposition hierarchy can then

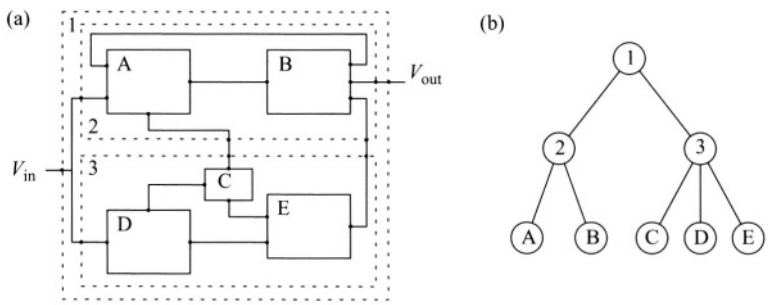


Figure 32.11. (a) Hierarchical decomposition of a circuit, and (b) corresponding decomposition tree.

be obtained without expansion in terms of the transfer functions of the composing subcircuits. For subcircuits 2 and 3, this is in terms of the above leaf transfer functions:

$$\boldsymbol{H}_2 = f_2(\boldsymbol{H}_\mathrm{A}, \boldsymbol{H}_\mathrm{B}) \tag{32.13}$$

$$\boldsymbol{H}_3 = f_3(\boldsymbol{H}_\mathrm{C}, \boldsymbol{H}_\mathrm{D}, \boldsymbol{H}_\mathrm{E}) \tag{32.14}$$

The top-level transfer function of the complete circuit is then derived in terms of the transfer functions of the subcircuits 2 and 3:

$$\boldsymbol{H}_1 = f_1(\boldsymbol{H}_2, \boldsymbol{H}_3) \tag{32.15}$$

and is, therefore, given as a sequence of small expressions having a hierarchical dependence on each other.

It is clear that the technique of hierarchical decomposition results in symbolic expressions in nested format, which are much more compact than expanded expressions. This results in a CPU time, which increases about linearly with the circuit size [45], allowing the analysis of really large circuits, provided that the coupling between the different subcircuits is not too strong. Also the number of operations needed to numerically evaluate the symbolic expression is reduced because of the nested format. Hierarchical decomposition has been used in combination with a signal-flow-graph method in [45] and [46], and in combination with a matrix-based method in [12]. The calculation of sensitivity functions in nested format has been presented in [47].

Following the use of binary decision diagrams in logic synthesis, determinant decision diagrams (DDD) have recently been proposed as a technique to canonically represent determinants in a compact nested format [48]. (Note that this has nothing to do with hierarchical decomposition as such, but merely with a compact representation format for the symbolic expressions.) The advantage is that all operations on these DDDs are linear with the size of the DDD, but the DDD itself is not always linear with the size of the circuit. This technique needs some further investigation before conclusions can be drawn about its usefulness.

None of the above mentioned programs, however, provides any approximation, which is essential to obtain insight into the behavior of semiconductor circuits. The human interpretation of nested expressions is also more difficult, especially if the nested expression is not fully factorized, which often is the case. In addition, the results of hierarchical decomposition are in general not cancelation-free, which further complicates the interpretation. A key issue here is to find efficient and reliable algorithms for carrying out the approximation of the nested expression, but without complete expansion, also in the presence of term cancelations. Some attempts in this direction have already been

presented. In [49], the symbolic expressions are generated in nested format whereby the terms are grouped and ordered in a way that eases the interpretation of the results. The decomposition of the circuit into preferably cascaded blocks becomes possible after a preceding rule-based simplification of the circuit structure (such as the lumping of like elements in series or parallel, or the application of the Norton–Thévenin transformation). Although the influence of neglected elements can be examined by means of the extra-element(s) theorem, this method does not offer a global view on the overall approximation error. Similarly, the lazy expansion technique [8] expands the nested expression term by term with the largest terms first until the error is below the required limit. Extensive care must be paid, however, to term cancelations. Another technique was presented in [50]. The numerically calculated contribution factors of each leaf-node expression to all frequency coefficients in the numerator and denominator of the total nested expression are used to determine with which individual error percentage each leaf node can be simplified on its own. The above approximation techniques are of course not needed for applications requiring only the numerical evaluation of expressions, such as behavioral modeling or statistical analysis, where compactness of the expression is necessary to gain CPU time.

32.4.6. Symbolic Pole–Zero Analysis

Algorithmic techniques to derive symbolic expressions for poles and zeros have recently been included in some symbolic analyzers, such as ASAP [5] or SANTAFE [51]. As closed-form solutions for poles and zeros can only be found for lower-order systems, the most straightforward approach is to make use of the pole-splitting hypothesis to come up with approximate symbolic expressions for the poles and zeros [5]. The use of such a capability together with advanced parametric graphical representations, however, is of significant help for interactive circuit improvement and design space exploration [6]. In SANTAFE symbolic Newton iterations are performed to calculate higher-order transfer functions in factorized pole–zero form [51].

32.4.7. Symbolic Distortion Analysis

Besides techniques for the symbolic analysis of linear(ized) circuits, a technique has also been developed, and included in the ISAAC program [4] for the symbolic analysis of nonlinear circuits with multiple inputs but without hard nonlinearity (such as mixers and multipliers) [52], as well as for the symbolic analysis of harmonic distortion in weakly nonlinear circuits [53]. The method is based on the technique of Volterra series, where each higher-order response is calculated as a correction on the lower-order responses [53]. The function $i = f(v)$ that describes a nonlinear element is expanded into a power series

around the operating point according to:

$$i = K_{1,f}v + K_{2,f}v^2 + K_{3,f}v^3 + \cdots \tag{32.16}$$

where $K_{i,f}$ is the ith-order nonlinearity coefficient of f. This power series is truncated after the first three terms. The *probing method* [53] then allows to calculate the responses at the fundamental frequency, at the second harmonic and at the third harmonic by solving the same linear(ized) circuit but for different inputs. For the analysis of the second and third harmonic, the inputs are the nonlinearity-correction current sources associated with each nonlinear element. These current sources are placed in parallel with the linearized equivalent of the element and their value depends on the type of the nonlinearity, the order, the element's nonlinearity coefficients, the input frequencies and the lower-order solutions for the controlling voltage nodes. For example, the second-order correction current INL_2 for a capacitor C_x between nodes p and q is given by the following expression:

$$\mathrm{INL}_{2,C_x} = 2\mathrm{j}\omega K_{2,C_x}[H_{1,\mathrm{p}}(\mathrm{j}\omega) - H_{1,\mathrm{q}}(\mathrm{j}\omega)]^2 \tag{32.17}$$

where K_{2,C_x} is the second-order nonlinearity coefficient for the capacitor and $H_{1,\mathrm{k}}(\mathrm{j}\omega)$ the first-order Volterra kernel for the voltage at node k (with respect to ground). This method has been extended towards the symbolic analysis of gain, noise and distortion of weakly nonlinear circuits with multiple inputs such as mixers and multipliers [52]. The expressions for the correction current sources are of course different and the solutions are a function of the frequencies ω_1 and ω_2 of the two input signals. The symbolic distortion analysis technique is now illustrated for a practical example.

Example 32.8. The second harmonic distortion at the output of the CMOS two-stage Miller-compensated op-amp of Figure 32.8 in open loop has been calculated by ISAAC [4] and is given by:

$$\frac{-A^2 K_{2,g_{\mathrm{m,M3}}} g_{\mathrm{m,M1}}^2 (g_{\mathrm{out}} + sC_{\mathrm{L}})^2 (g_{\mathrm{o,M1}} + g_{\mathrm{o,M2}} + sC_{\mathrm{C}})}{(g_{\mathrm{out}}(g_{\mathrm{o,M1}} + g_{\mathrm{o,M2}}) + 2sC_{\mathrm{C}}g_{\mathrm{m,M3}})(g_{\mathrm{out}}(g_{\mathrm{o,M1}} + g_{\mathrm{o,M2}}) + sC_{\mathrm{C}}g_{\mathrm{m,M3}})^2} \tag{32.18}$$

where A is the amplitude of the input signal. These analytic distortion expressions are almost impossible to obtain by hand, and provide invaluable information and insight to the designer. For a certain design point, the results are also graphically plotted in Figure 32.12 as a function of the frequency of the input signal. Figure 32.12 shows the total harmonic distortion ratio (solid line), as well as the major contributions: $K_{2,\mathrm{gm3}}$ (*), $K_{2,\mathrm{gm1}}$ (+) and $K_{2,\mathrm{gm2}}$ (o). All contributions are scaled to an input voltage amplitude of 1 V (i.e. $A = 1$).

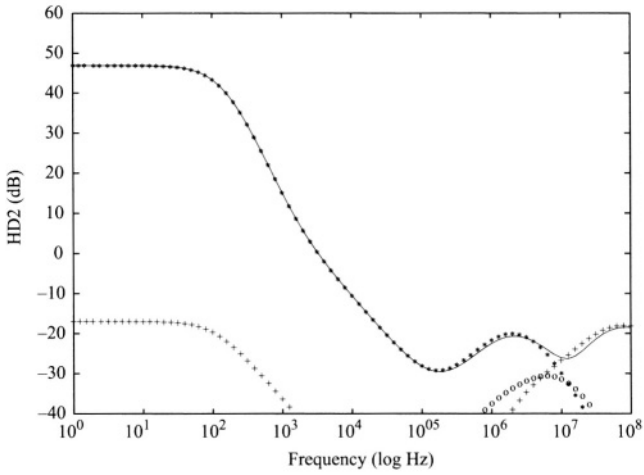


Figure 32.12. Second harmonic distortion ratio at the output of the CMOS two-stage op-amp in open loop versus the frequency of the input signal. The total harmonic distortion ratio is shown (solid line) as well as the major individual contributions.

32.4.8. Open Research Topics

At present and as far as functionality is concerned, the following topics are still open research areas in symbolic analysis of analog circuits (see Figure 32.6). The analysis of switched-capacitor circuits has upto now only been carried out in the z-domain (such as for example in ISAAC [3,4], SCYMBAL [11], SSCNAP [17] or in [18]), excluding s-domain effects such as the finite op-amp gain–bandwidth. Recently, a first step towards the combined symbolic analysis of s and z effects for a restricted class of circuits has been presented in [54].

Other unsolved topics at this moment are the symbolic analysis of large-signal behavior (e.g. slew rate), time-domain behavior, and the symbolic analysis of strongly nonlinear circuits (if this will ever be feasible). A first approach towards symbolic time-domain simulation based on inverse Laplace transformation has been presented in [55]. But techniques for nonlinear analysis especially need to be developed in the near future.

Despite these, as yet, unsolved topics, it can be concluded that the above reported algorithmic developments in symbolic analysis have recently created the breakthrough that was needed to make symbolic analysis feasible for circuits of practical size, at least for the linear(ized) behavior.

32.5. Comparison of Symbolic Simulators

The most prominent symbolic simulators for analog circuits existing nowadays are ISAAC [3,4], ASAP [5,6], SYNAP [7,8], SAPEC [9], SSPICE [10],

SCYMBAL [11], SCAPP [12], Analog Insydes [13], CASCA [14] and GASCAP [21]. Although other tools have been published as well, the above programs are all available as stand-alone symbolic simulators. A comparison of the functionality offered by most of these programs and some implementation details are given in Table 32.1. ISAAC, ASAP, SYNAP and to some extent also SSPICE are targeted towards the symbolic analysis of analog integrated circuits, with a built-in small-signal linearization and symbolic approximation of the expressions. ISAAC and SCYMBAL offer the symbolic analysis of switched-capacitor circuits. SYNAP is the only program that offers an approximate dc analysis. SAPEC and GASCAP are targeted more towards the symbolic analysis of analog filters, whereas SCAPP is the only program that offers hierarchical analysis for large circuits. ISAAC is the only program that offers a symbolic distortion analysis for weakly nonlinear circuits, and ASAP and SSPICE offer an approximate symbolic pole–zero extraction.

Tools that include the most recent algorithmic developments such as simplification before and during generation offer similar functionality but can handle larger circuits. They include SIFTER [15], RAINIER [16] and SYMBA [56]. The SYMBA tool is currently reaching the commercial prototype stage and will offer a fully integrated environment for the symbolic analysis and modeling of analog circuits. It will also be linked to a numerical simulator to extract the dc operating point information needed for the simplifications [56].

Besides functionality, a second criterion to compare symbolic analysis programs is their computational efficiency. A direct comparison, however, is extremely difficult here, because most CPU time values in the literature are published for different computing platforms (processor and memory configuration) and for different circuit examples. Therefore, a standard set of benchmark circuits should be agreed upon and used worldwide for all future comparisons. A second problem is that the different tools use different simplification techniques and expression formats (expanded versus nested), which require that reported CPU figures must be handled with care. Therefore, no CPU times are reported in this tutorial, but the reader is advised to compare the efficiency of the different tools in the light of the accuracy and reliability of their symbolic results and in the light of his targeted application.

32.6. Conclusions

In this chapter an overview has been presented of the state of the art in symbolic analysis of analog integrated circuits. The use for symbolic analysis as a complementary technique to numerical simulation has been shown. In the analog design world, the major applications of symbolic analysis are to obtain insight into the circuit's behavior, to generate analytic models for automated circuit sizing, in applications requiring the repetitive evaluation of

Table 32.1. Functional comparison between existing symbolic simulators for analog circuits.

	ISAAC	*ASAP*	*SYNAP*	*SAPEC*	*SSPICE*	*SCYMBAL*	*SCAPP*	*GASCAP*
Analysis domains	s- & z-domain	s-domain	dc & s-domain	s-domain	s-domain	z-domain	s-domain	s-domain
Primitive elements	complete	complete	complete	complete	limited	?	?	limited
Small-signal linearization	yes	yes	yes	no	yes	no	no	no
Mismatching	yes	yes	yes	no	no	no	no	no
Approximation	yes	yes	yes	no	yes	no	no	no
Weakly nonlinear analysis	yes	no	no	no	no	no	no	no
Hierarchical analysis	no	no	no	no	limited	no	yes	no
Symbolic pole/zero extraction	no	limited	no	no	limited	no	no	no
Graphical interface	no	yes	no	yes	no	no	no	yes
Formulation	CMNA	SFG	MNA	MNA	admittance matrix	SFG	RMNA & SFG	?
Language	LISP	C	C++	LISP	C	FORTRAN	C	C

characteristics (such as fault diagnosis) and in analog behavioral model generation and formal verification. For these applications, symbolic analysis is a basic technique that can be combined with powerful numerical algorithms to provide efficient solutions.

The basic methodology of symbolic circuit analysis has been described. The present capabilities and limitations of symbolic analysis, both in functionality and efficiency, have been discussed. The algorithmic improvements realized over the past years (with the techniques of simplification before and during generation as well as the development of the DDD technique) have, especially, rendered symbolic analysis possible for circuits of practical size. Also, the analysis of weakly nonlinear circuits has been developed.

Important future research topics in the field of symbolic analysis are the improvement of the postprocessing capabilities to enhance the interpretability of the generated expressions. Also, the potential of symbolic analysis in analog design automation, such as in analog design optimization, or in statistical and yield analysis, etc., has to be explored in much more detail. At the algorithmic level, analysis of nonlinear and time-domain characteristics are the key issues to be solved. If these issues can be solved, then commercial symbolic analysis tools might show up in the EDA marketplace in the near future.

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Chapter 33

TOPICS IN IC LAYOUT FOR MANUFACTURE

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33.1. Layout: The Crucial Next Step

By the end of the circuit-design phase of an IC product of even modest complexity, many hundreds, and often thousands, of decisions will have been considered and weighed, and the basic "electrical" compromises and trade-offs will have been settled. However, the product development still has a long way to go. The next step – the preparation of a set of layout drawings – is always crucial to a successful implementation, but particularly so where there is a substantial amount of analog circuitry. This distinction arises partly from the fact that analog cells and architectures are sensitive to numerous tiny details, which makes the transition from schematic to an intelligent layout a far more demanding exercise.

Cell reuse is an appealing idea, both at the circuit development stage and particularly in layout, where verbatim copying, using "cut-and-paste", can save a great deal of time. In practice, however, it is hard to implement this approach in the analog domain, where each system poses subtle differences in the signal environment and performance objectives. Analog layout for new products is invariably forced to be "hand-crafted". This is true even when using some sort of auto-routing software, which is not yet smart enough to do a satisfactory job.

By contrast, digital systems-on-a-chip (SoCs) must – and routinely do – take advantage of reuse, whether of proven transistor-level cells, logical processing algorithms, functional blocks, or even of large areas of the layout, with relatively minor modifications. But here too, this general rule takes on a different aspect when the leap is made to a much denser process, requiring the generation of a new family of logic cells, or when data and clock rates are increased by large factors, requiring a more thorough "physics-based" consideration of signal propagation along the interconnects, which must now be viewed as transmission lines and analyzed using electromagnetic theory. Current predictions about CPU clock rates reaching 20 GHz by 2009 using 30-nm gate-length transistors raise an entirely new set of questions in this regard. Analog design skills and layout expertise will be much in demand for the all-digital SoC's of the future.

Nevertheless, the fact remains that the function of even large clusters of binary cells is basically simple and their response to a set of input states is

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virtually certain. Circuit inertia is largely viewed as a barrier to higher data rates, and detailed component values influence design only to the extent that adequate margins are needed to ensure extremely high yields. There rarely are "weak signals" competing with "strong signals"; logical signals are of essentially the same amplitude, and even the density of the signal transitions is roughly the same, all over the die. So, while substrate coupling effects are far from a trivial concern, some relief is obtained from this uniformity of signal injection into the substrate, and because of the uniform and low susceptibility to noise (actually, switching hash) of the majority of cells.

The top-level *function* of the signal path in a digital processor depends very little on the parametric variances, whose potentially damaging effects are limited to their impact on the *assured robustness* of basic binary functions in high-volume production, rather than bearing on *detailed performance* of any one of numerous analog-circuit functions, which can become complex even at the few-transistor cell level. The trade-offs that arise during the layout of digital products will be largely concerned with packing the major system blocks in the most efficient way, especially where wide data paths are used to communicate between these blocks, while paying close attention to the effects of location on time delays, and to issues of clock- and power-supply distribution (Figure 33.1 (a)). It is likely that the layout of the transistor-level logic cells, the higher-order functional macros, and the top-level architecture will be handled by different people or teams, and at different times.

In sharp contrast, the layout of analog-intensive products is an amalgam of "transistor-level", "functional-level" and "architectural-level" considerations, which merge seamlessly into a single, holistic, concurrent challenge. Analog layout design involves a kaleidoscopic confluence of numerous elements, each fundamentally different in structure and behavior (Figure 33.1(b)) and each raising idiosyncratic trade-offs. Almost every transistor in an analog circuit contributes to the detailed performance, in one way or another. The device

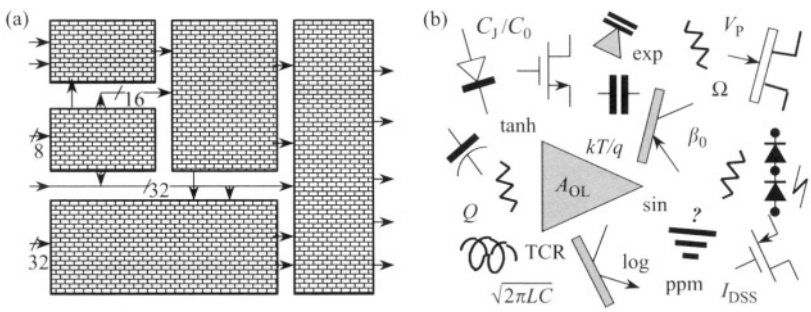


Figure 33.1. (a) Analog and (b) digital layout: worlds apart.

modeling equations, the detailed *physics,* that are at the heart of circuit design, are carried over into the layout domain, where they continue to assert their influence.

Many of these devices are so intimately involved in the preservation of signal quality, or the accuracy of a control or measurement function, that it is impossible to regard the mapping from circuit schematic to IC layout in purely algorithmic terms. The bilateral nature of analog interfaces, high linear-mode gain together with wide bandwidth, the probability of damaging effects of strong signals on sensitive cells, and the coupling of signals through subtle sneak paths all demand constant attention to the potentially dire consequences of seemingly minor layout indiscretions. Interactions through electrostatic and magnetic cross-coupling in high-frequency circuits often first appear, uninvited and unwelcome, at the layout stage.

In this domain, skill and finesse is as much a part of the product design as that required in all the steps leading to the generation of the final circuit schematics. The particular way in which this crucial transformation is implemented, and the trade-offs that are made, can have far-reaching effects, from first-order performance (a poorly conceived layout may prevent certain aspects of the desired electrical behavior from being realized *at all),* to detailed performance (the circuit generally works as planned, but fails to meet some of its critical objectives), and on to robustness and die yield during the coming years of high-volume production. These trade-offs involve a huge number of parameters, whose supposedly Gaussian distributions are often skewed by process bias and extremes during fabrication, and which are invariably influenced by temperature and supply voltage to a greater or lesser degree.

In analog circuits, the *absolute value* of numerous device parameters (often amounting to thousands) contribute to *performance uncertainties.* Consequently, the layout of a cutting-edge analog circuit demands a keen appreciation of the underlying *physical principles* of these devices, to the extent that their electrical properties will most certainly be a function of the way they are constructed; their orientation on the die; their mutual proximity when this is essential, or their adequate separation in other cases; their absolute location on the die (in prime territory close to the center and on the thermal axis in some cases, or permissibly near the edge of the die in others); the minimization of boundary artifacts and influences; and so on. Further considerations arise regarding the effects of improper intra-cell and inter-cell wiring; the impact of mechanical strain effects in precision analog circuits; and yet other layout-critical effects in microwave circuits, where the detailed topological disposition of reactive elements has a direct and major influence on performance, and the layout is usually more meaningful than the schematic-level representation.

It should not be surprising, then, that the layout of each new analog circuit function presents many, never-before-encountered trade-offs, each needing to

be resolved individually by the layout designer acting from experience, aided by accurate and unambiguous schematic documentation, and in close consultation with the circuit designer. The very nature of a trade-off requires that some benefit has to be sacrificed in the pursuit of a more pressing objective, and this dilemma is very evident in the layout process.

In this chapter, no attempt is made to catalog all the rules of layout, or present a large number of case histories. Such an undertaking can easily run to full-book length, and the knowledge it captures may take years of experience to master. Rather, it emphasizes the *cooperative nature* of the circuit/layout interface, calling for a strong codependence and mutual trust tempered with a constant concern for oversights and misjudgments on either side of this partition. Indeed, in a well-oiled team, the ebb and flow of ideas and the underlying sense of synergy will be instinctive, and not driven by rules and policies.

33.1.1. An Architectural Analogy

The relationship between an IC product concept, its elaboration, the development of circuit schematics, the layout and silicon processing is comparable to that between these six phases in architecture: Starting with (1) an artist's vision of an office building, to show the customer and confirm the key objectives, there follows (2) the basic engineering of the structure, which needs to be strong, durable and cost-effective while making no concessions to utility, efficiency or visual appeal. During the next phase (3), the articulation and consolidation of numerous design details proceeds toward a standardized format, from which (4) the blueprints – the working drawings describing the materials and methods – can be generated, for use on-site, during (5) the construction of the core building, followed by (6) the interior finishing. Careful phasing of many different kinds of resources is needed at every step.

Similarly, for the IC development, there are at the outset only some general design objectives, framed in basic terms that a specific customer, or some segment of the market, can readily understand. These address the standard and obvious demands – for more features, higher performance, lower power and lower cost – as well as new and unfamiliar capabilities. Their presentation may lead immediately to a favorable reception, but often with demand for consolidating information. Completion of Phase (1) usually means only that the new concept – described in broad strokes and invariably emphasizing the more progressive aspects of the product proposal – has been validated, ratified or modified by consideration of the several and various responses from the user community. During a Concept Review, some initial trade-offs in the objectives will be addressed and resolved.

The ensuing circuit-design phase corresponds to Phase (2) in the architectural analogy, that is, the engineering of a robust structure, using proven

materials and methods where possible, but often requiring the invention on the spot of some genuinely new cells and structures. This is the period during which many, but by no means all, of the judgments, compromises and trade-offs must be made in the long journey to manufacturing release.

This leads to Phase (3), a complete set of "building specifications", that is, the schematics and their associated documentation, from which, (4), the "blueprints", the working drawings that follow standardized layout practices, can be prepared, and subsequently verified against layout design rules and checked for full agreement with the interconnections and component values in the schematics. Tape-out – the handing over of these drawings as a data file for the generation of masks for wafer fabrication – corresponds to Phase (5): it is analogous to entrusting of a set of blueprints to a cadre of "contractors and sub-contractors" who will bring the concept a step closer to reality. The arrival of the first wafers then heralds the final Phase (6), the navigation of the product through a series of critical gates – including its initial evaluation, the characterization of a large sample, the refinement and finalization of testing methodologies and their software – prior to release for volume production. These process steps are not undertaken in a simple time-sequence, but develop in parallel with many other aspects of the overall project, which is always more than a merely technical endeavor.

An architect must rely heavily on the experience of the drafting team to provide the first glimmerings of the practical form of the concepts. It is not too difficult to implement the general vision, so that the final building will *look* very much like the original sketches. But it matters more that all of its *inner structures* are thoroughly worked out: practical, ergonomic, using the optimal materials, and observing a plethora of building codes, some of which have dubious justification. This step again involves compromise – more trade-offs – and perhaps a further dimming of the designer's original vision. Even when all these plans have been created, nothing physical exists. Much can go wrong in the subsequent construction of the building. However, the likelihood of unforeseen disappointments can be greatly lowered by having the services of *a reliable and experienced drafting team.*

33.1.2. IC Layout: A Matter of "Drafting"?

The term drafting, often diminutively called "polygon pushing", doesn't begin to describe what really happens in preparing architectural drawings. A great deal of communication is needed between the architect – perhaps several such – and the drafting team in preparing these crucial drawings. At the same time, the team members are expected to have a broad appreciation of all the numerous and detailed rules, codes and laws about building, and about the properties of construction materials, both basic and subtle. They are relied

on to apply their own special experience in making the many decisions and trade-offs that are necessary to convert a "high-level" (more abstract) vision into a detailed set of plans that fully and unequivocally define the eventual tangible reality. This crucial step of drafting, whether for a building, a bridge, an automobile or a toaster, can make or mar the quality of the product.

In no less a way, the experience and judgment that is brought to bear in transforming a circuit schematic (or, more commonly, a rather extensive set of such schematics) into the drawings for the many lithographic layers that define the placement of diffusions, contacts, thin-film layers and metalization, will have a strong impact on the performance of an integrated circuit. This is the unique contribution of the layout designer.

For this chapter, we have coined the somewhat awkward terms *"layouteer"* to refer to this person (which may be a small team for a mixed-signal project) and *"circuiteer"* to refer to the circuit designer, both of these by adaptation of the more generic *"engineer"*. Each of these jobs require considerable expertise – requiring the use of on-the-spot *creative approaches* to problem solving combined with a *strong knowledge* of the underlying physical principles – and the circuiteer and the layouteer will make equally valuable contributions and refinements to the development of the successful product.

Significantly, not only is the overall *product* design work unfinished until these drawings exist: neither is the *circuit* design. Only after the initial IC layout has been completed can the extraction of the parasitic capacitances (and in many cases, the resistances of metal traces) be undertaken. This is called *back-annotation.* Experience has proved that when this step is implemented, the new simulation results can be drastically – and disappointingly! – different. These sobering insights usually call for at least some minor changes in the layout. In severe (but not rare) cases, they require a major rethinking of the design, whether in the pad/pin sequence or in cell placement and routing (and thus still in the layout arena) or in the practical implementation of the cells and/or the overall architecture.

Such delays and setbacks are especially common in RF design, which is not surprising in view of the highly Newtonian nature of high-frequency circuits. It may be less obvious that the common use of modern, ultra-fast IC processes may lead one to forget at times that some mediocre low-frequency cell, say, an audio output buffer in a cellular handset, might manifest enigmatic and peculiarly aberrant behavior, such as instability or high distortion, when tested at the product level. Upsets of this sort can happen because the designer has a very different worldview to that of the circuit! The former thinks in terms of some desired objective, while the circuit can do no more or less than rigorously obey the laws of physics. Given half a chance, a single transistor may earnestly believe it's supposed to be a microwave oscillator, rather than a headphone driver, and wreck the whole show. In this case, an inappropriate layout

might have encouraged the mutiny, by ignoring the need to minimize parasitic capacitances in some area of the die, perhaps, where a too-casual trade-off had favored an inadvisable choice of widening the metal traces, and this capacitance in conjunction with a bond-wire inductance formed a very willing resonator. Often, in a careless design, the package model may be omitted entirely, on the argument that "it's only a low-frequency amplifier". The circuit invariably will have other ideas.

Connection capacitances are troublesome in most circuits fabricated on fast contemporary processes for a variety of similar reasons. For example, the behavior of a cell optimized for wide bandwidth and low power operation may appear to be superb in simulation, until one adds the few femtofarads of capacitance that accumulate in just connecting up the devices within cells (intraconnect), and perhaps as high as picofarads in long journeys between cells (interconnect). Disappointments of this sort are less likely if supermodels are routinely used for all the elements, although these cannot exactly anticipate all the extra capacitances that will arise in the physical reality, until at least some layout sketches are undertaken. In some cases, it may be the *coupling* between adjacent metal traces that precipitates disaster; in others, the precise *balance* in metalization capacitances and bonding pads can be critical, as for example, when attempting to maintain a precise quadrature-phase relationship, or minimize local-oscillator feedthrough, in a direct-conversion I/Q modulator.

Back-annotation is thus an essential step in the final stages of a product design, to discover, and then remedy, the effects of parasitics on performance. This can be very time consuming, which is why *design compression* is so important (see Chapter 2). All the principle elements of the design should be in place shortly after the start of a project, leaving ample time to address contingencies that invariably will emerge from robustness studies, packaging parasitics, the remediation of effects revealed through parasitic back-annotation, the deliberation of testing methodologies, and much else. It is impractical to stack all of these sub-tasks into a serial sequence. In analog IC developments, a close, ongoing dialogue between circuiteer and layouteer is essential, no matter how well-documented the schematics.

Often, the layout may begin before every detail of the circuit design is complete. This could be called a risky practice. In fact, the danger is minimal, and mostly amounts to the possibility of wasted effort if major sections of the layout need to be reworked. Overall, this may not equate to an increase in the total elapsed time to-tape-out. In some cases, a realistic outline layout – a floor plan – will be generated even before the detailed circuit design is begun. This could be the case when the need to minimize die size is crucial, and one sets an upper limit and "designs into it". The pads, electrostatic discharge (ESD) protection and their connection ring, and the primary power distribution lines

will eat up a considerable fraction of a small chip, and it is better to know in advance the nature of the "remaining" circuit design challenge.

33.1.3. A Shared Undertaking

An experienced and skillful layouteer understands the equivalence between the symbols on the schematic page and the polygons on the layout page. While the circuiteer "thinks like a transistor" when viewing the symbol for such, a good layouteer will be thinking about the impact of the surrounding environment on the performance of this device, now represented as a series of nested colored boxes. We should not view a layouteer as a "polygon pusher" any more than we would think of a circuiteer as a "transistor pusher". Our unique symbols are different representations of the same ultimate reality, and both convey a wealth of attributes.

Circuit design is often called an "art", and books about the subject have appeared bearing such titles *as "The Art of Electronics"*. Monolithic layout is even more understandably viewed as an "art", rather than a sub-domain of engineering, and this is particularly apparent for analog layout. Recently, an excellent, objective survey of this topic appeared in a full-length book entitled *"The Art of Analog Layout"*. This welcome work fills a long-standing gap in teaching layout practices. In either domain, design often involves making *non-algorithmic* and *arbitrary* decisions, based more on judgments and insights – sometimes no more than *feelings* – rather than on hard facts, but nonetheless tempered by a shared understanding of each medium.[1]

Much of what happens during the layout phase of an integrated circuit, and particularly an analog product, has this quality of arbitrariness about it. For example, if the layouteer is given no clue as to where all the cells should go, or in more extreme cases, no directive as to the pin/pad sequence, it is inevitable that some independent decisions are likely to be made. Clearly, this could be risky. In the mildest case, it could lead to a loss of initial momentum; more seriously, it may require the reworking of large sections of the layout; in the worst case, if left unchecked, it could result in sub-optimal performance, the consumption of excessive die area and low production yields, or howls of regret at lost opportunities for improvement.

The skilled layouteer will have learned from shared disappointments and will not need be reminded at length by the circuiteer about the need to give thoughtful attention to numerous fussy details of implementation. On the other hand, the

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[1] Edward de Bono holds that "in the end, all decisions are emotional", meaning that, if the data allow for no other interpretation, we do not need to *make* any decision, since the facts themselves totally dictate the outcome. While this may seem like an alien idea to a practicing professional, engineering is never algorithmic, and idiosyncratic choices are frequently made when there are no obvious constraints.

latter cannot complain if the result falls short of some internal expectations, if these have not been painstakingly articulated.

The experienced circuiteer will be constantly aware of the fact that those fine simulation results are never a satisfactory surrogate for the behavior of a silicon die, whose identity is much more closely bound to the physical world, and thus the construction of the layout, than to the schematic. Both are little more than a net-list given an *appearance of existence* through elaborate symbolic representations. However, while one can change the geography of a schematic in endless ways, with no effect, the same cannot be said of a layout, where positional information is as important as topological fidelity is to the schematic.

33.1.4. What Inputs should the Layouteer Expect?

Before entering into a discussion (by no means an exhaustive survey) of a few of the typical trade-offs that will arise and demand resolution in an IC layout, we should review a minimal list of necessary inputs that the layouteer must be given, to be effective as a team member. One of the more apparent differences in the work habits of most circuiteers and most layouteers is that the latter invariably *provide a service* to a team or group, and are expected to be *available on demand.* Accordingly, at the very outset of a new development, the project leader must provide an estimated date by which the circuit will be essentially ready for layout work to begin, to allow the layouteer to maintain an advanced schedule that can meet the intertwined demands on this resource, as they wax and wane.

This date may be close on the heels of the Design Review (see Chapter 2) but is usually pitched somewhat later, on the assumption that the critique received during that review will entail further circuit work before the design is frozen.[2] On the other hand, for a team of closely integrated coworkers, it may be possible to provide many – or even the majority of – the constituent cells *ahead* of this date, to allow layout work to begin, with a view to maintaining momentum. This is especially important in the contemporary domain of commercial and competitive product development, where the minimization of time-to-market must be given extraordinary emphasis. In practice, predicting a precise date for layout start is rarely possible, and one needs to fall back on estimates. However, a *team-spirited circuiteer* will be particularly sensitive to the fact that any slippage in the delivery of the schematics will almost certainly upset the overall project schedule, not only with regard to layout, but in the workload for downstream product- and test-development engineers, and may undermine the best-laid plans of the anxious marketeers.

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[2] The seasoned layouteer will tell you that this only happens at tape-out, and then by only a narrow margin!

Well-prepared schematics will transfer of a great deal of information. In an earlier time, when these may have been handdrawn, it was necessary to provide the layouteer with an extensive set of "Layout Notes", describing in agonizing detail all the components and how they should be constructed. With the advent of electronic schematic capture, the need for this discipline has lessened, since most of this description is now embedded in the schematic file and can be attached in a variety of ways. Nevertheless, a large amount of additional information is needed for layout purposes that will not automatically appear on any of the schematic layers.

To begin with, of course, the IC process must be clearly indicated; where there are variations between one version of the process and another, the circuiteer must be quite explicit about which version is to be used. The IC package that is to be used will have an important bearing on the way in which the layout will proceed. It will strongly influence the permissible range of pad placements and dictates the maximum size of a chip, in order to fit on the paddle. Functional considerations will determine its overall aspect ratio. Frequently, there will be special devices, or ensembles of devices, whose physical construction cannot be fully explained on the schematic, calling for a few sketches to be provided by the circuiteer. There will also be a strong importance in the way the cells are placed on the layout, and this may require some additional information.

On the other hand, the need for additional documentation of this sort can be largely avoided, when the "top schematic" in the set is carefully drawn to closely resemble the desired floor plan for the IC – a *pseudo-layout* – an example of which was provided in Chapter 2. For present purposes, examine Figure 33.2. This drawing,[3] whose representation of *physical structure,* and stronger sense of the final objective, is of immense value to both the circuiteer and layouteer, is also a "fully-working" die-level schematic. It is also a *scaled drawing,* and shows the precise pad positions, all of the ESD devices, the general size and arrangement of the major cells, and the major metalization paths. The latter are widened to show the high-current routes, or those branches where very low resistance is essential, and crosshatched to make viewing easier. Connections to the substrate (or, in a silicon-on-insulator (SOI) product, the unworked silicon regions outside the trenches) all along the common lines are shown as small squares. The careful circuiteer will also take steps to ensure that any "starred" common nodes, or "Kelvin sensing" wiring arrangements, are clearly identified on the pseudo-layout schematic.

A useful practice in the representation of a hierarchy of cells is that of identifying the most basic (lowest-level) cells using a simple rectangle, having node

[3] While this is an actual product, the names of the blocks, and of some pads, have been changed.

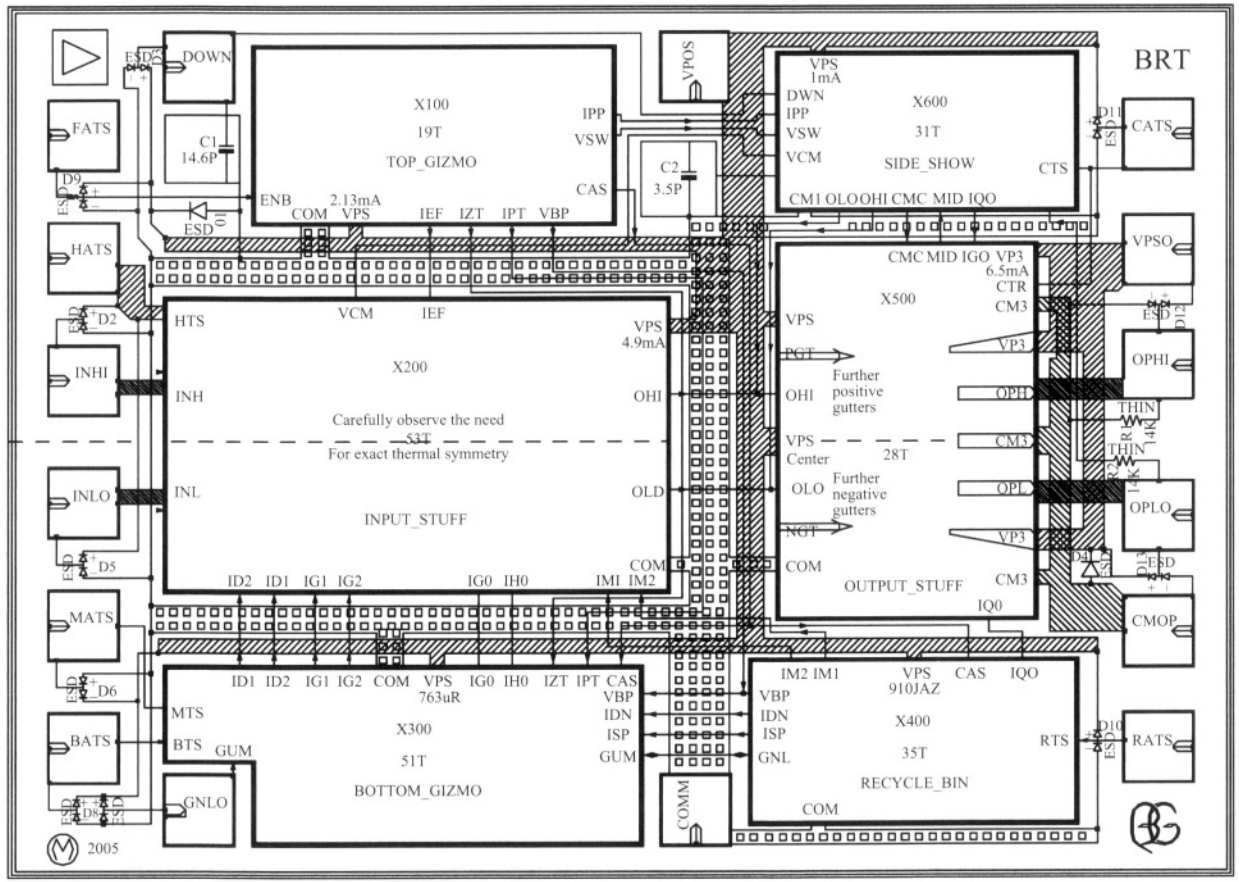


Figure 33.2. A well-annotated pseudo-layout schematic.

names around the boundary of this symbol, and within the cell, that are as brief as possible. This generally means using a two-character name, such as CM, VP, IP, OP. For the next level up – the cells comprising the second layer, their intraconnects and perhaps a few individual components – the symbol boundary is two closely nested rectangles, and its node names use three characters (thus, COM, VPS, INP, OUT). For the third layer cells, three closely nested rectangles are used, and the node names use four characters (COMM, VPOS, RFIN, IFOP). Uniform cell boundaries and node-naming conventions provide a useful navigational tool in the presentation, communication and interpretation of one's ideas and intentions. It is usually possible to organize even quite complex analog circuits into such a basic three-layer hierarchy, and remain within the bounds of four-character names for the pads and pins.

It is also useful to agree on a general set of *pin*-naming conventions, not only to simplify the interpretation of schematics by all members of the team as they review each others' work, but more importantly, to provide a consistent resemblance between products in a given family for the benefit of the user community. Who has not been baffled by arcane pin-names? One wishes that better cooperation in this regard could be achieved throughout the company; but conventions of this sort are bound to be idiosyncratic and somewhat arbitrary. The important point here is that by adopting them for a given product line, the circuit/layout interface is less prone to ambiguity and misinterpretation, and the final product easier to comprehend and apply. Rather than proposing a new set of symbols and naming conventions for each new product, by each individual designer, the use of a uniform nomenclature will contribute to the team's unity of purpose, and minimizes customer confusion.

33.2. Interconnects

Some of the most challenging trade-offs arise in connection with design of the metalization paths in a layout. The circuiteer may at times give insufficient thought to interconnections. In most schematic capture environments, a "wire" of any extent is just a *node,* a singularity without any physical properties, having no resistance, no capacitance, no current-carrying limitations. In view of the critical role of interconnects, it is surprising that schematic capture programs do not generally allow one to include a wire as an object with properties, without case-by-case intervention. This capability will be commonplace in the future, and the series resistance of a trace, its total capacitance, C_T, to the substrate (partially distributed as $C_T/4$, $C_T/2$ and $C_T/4$), and its safe current-bearing limit will be automatically captured. Alerts of over-current can also be implemented. More ambitious plans include the routine algorithmic extraction of inductance, the capacitance(s) to one or more adjacent traces and full transmission-line modeling. Until then, the circuiteer must be especially

attentive to the effects of metalization parasitics, and to making his or her requirements clear.

The sheet resistance of a conductive layer depends, of course, on the material, the grain structure and the thickness of the film. For thin-film aluminum, the resistivity is $2.7\,\mu\Omega$-cm; thus, a typical 0.6-μm layer has a resistance of $45\,m\Omega$/square. For silicon-doped aluminum, more commonly used for interconnects in ICs, the sheet resistance is about 40% greater than pure aluminum, thus as high as $63\,m\Omega$/square for a 0.6-μm film. Further, these films have a very high temperature coefficient of resistance (TCR). For bulk aluminum, it is +0.38%/°C at $T = 27$°C, and the grain structure of deposited films with included elements (silicon or copper) causes this to be even higher.[4]

Multi-level metal is common in modern ICs and the layers closest to the transistors may be thinner than this; top-level aluminum may be as thick as $4\,\mu$m, thus under $10\,m\Omega$/square. These thick layers are needed for a variety of reasons, including the bussing of power at high currents, to provide a very low connection resistance between elements, and to improve the Q of inductors used in many RF circuits. Although these sheet resistances are seemingly small, inappropriate interconnection techniques can cause them to introduce many artifacts into analog circuit behavior.

A common oversight is illustrated in Figure 33.3. Following a poorly drawn schematic, the layouteer may have interpreted the schematic literally, and constructed the arrangement shown. From this drawing, the resistance of the metal connection between the two emitters, R, might amount to $0.5\,\Omega$, and if the transistors were operating at a low enough current level, this resistance would be unimportant. But now assume that a second indiscretion crept in, and the section of metal between these emitters was also carrying a steady current, $I = 2$ mA, as part of some other circuit branch. This induces a voltage drop of 1 mV, which will tilt the ratio of currents in these two BJTs by a factor of 4%. In this scenario, the effects may be no worse than causing a tolerable amount of DC offset. However, if we consider a scenario in which the "cross-wire" is carrying a significant amount of fluctuating signal current, and where these transistors are associated with a high-gain area of the circuit, the effect could be catastrophic, and include any of the following (initially mysterious) consequences: gain error; distortion; signal-dependent offsets; and in the worst case, outright oscillation or even latch-up. These risks are entirely avoidable, by using good schematic disciplines which force unambiguous interpretation at the layout stage, as depicted in Figure 33.4.

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[4] It is possible to put this TCR to advantage, since it is only slightly more than proportional to absolute temperature (PTAT, which is +0.33%/°C at 27°C) and this may be used to generate PTAT voltages that are also proportional to a current, for special purposes.

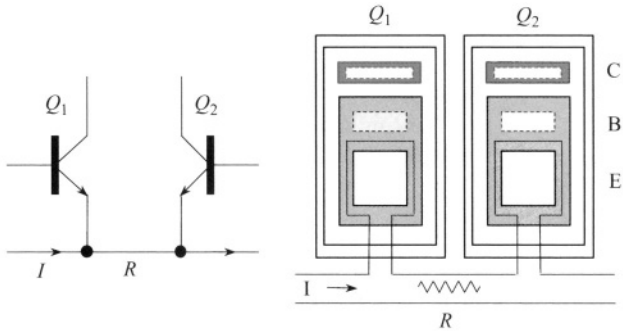


Figure 33.3. A badly constructed bipolar-transistor cell.

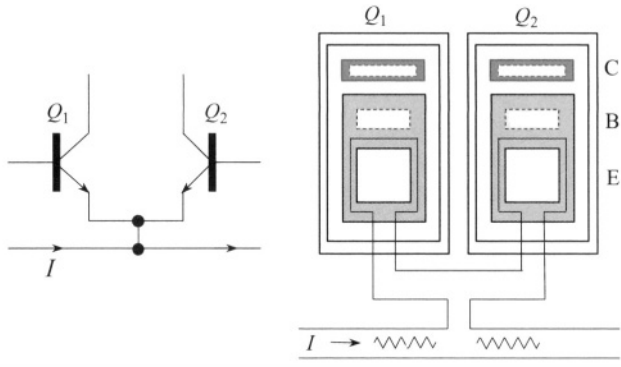


Figure 33.4. A disciplined schematic and the resulting layout.

It should be noted that the silicon-doped aluminum more commonly used for interconnects in ICs has a sheet resistance that is about 40% greater than pure aluminum, thus as high as 63 mΩ/square for a 0.6-μm film. Further, these films have a very high TCR. For bulk aluminum, it is +0.38%/°C at T = 27°C, and the grain structure of deposited films with included elements (silicon or copper) causes this to be even higher. It is possible to put this TCR to advantage, since it is only slightly more than proportional to absolute temperature (PTAT, which is +0.33%°C at 27°C) and this may be used to generate PTAT voltages that are also proportional to a current, for special purposes.

33.2.1. Metal Limitations

The current-carrying capacity of interconnects is ultimately limited by its fusing current. But at much lower currents than this, there is another consideration to robustness, namely, the phenomenon of electromigration. This refers

to the gradual alteration of the metal layer, by lateral growths ("whiskers") that are created when very high densities of energetic electrons collide with the metal atoms, and actually displace the material over significant distances. The process is slow, and its effects may only show up after years of service, when these whiskers become large enough to reach adjacent metal traces and thereby cause short-circuits.[5]

A common guideline for the peak sustained (long-term RMS) current-density in aluminum is $500\,\mathrm{kA/cm^2}$. For example, consider a $2\text{-}\mu\mathrm{m}$ wide trace of $0.6\text{-}\mu\mathrm{m}$ thick metal, that is, having a cross-sectional area of $12 \times 10^{-9}\,\mathrm{cm^2}$; the recommended maximum current for this trace is thus 6 mA. In practice, this will rarely give rise to the need for any trade-offs in interconnects, but may be a cause for concern at the *intraconnect* level. The electromigration guideline may also be too optimistic where metal negotiates steps in the surface dielectrics. On the other hand, occasional high peaks of current, with a low long-term mean value, will not pose a serious migration risk.

At the connections to the ends of an emitter finger, the contacting metal will often be less than $1\text{-}\mu\mathrm{m}$ wide, thus limiting the maximum sustained emitter current to 3 mA. Here, the proximity of the flanking base contacts (Figure 33.5(a)) poses a serious threat of emitter–base shorts in the event of whisker development. Where greater current-carrying capacity is needed, as in power stages, the transistor must be re-designed accordingly. A common solution is to use larger number of shorter emitters (Figure 33.5(b)). Here, the current density in the small collector contact, and the equivalent collector resistance, will also be high. A broadside connection to a single emitter and the collector provides maximum current handling capacity (Figure 33.5(c)).

In each case, there is a slightly different set of consequences – not only in the matter of electromigration. For example, the base resistance in the last case will be appreciably higher, but the collector–substrate capacitance is the lowest of all three examples. It is in such situations that an alert layouteer may catch an incipient problem, in the event of a sub-optimal choice of geometry by a less-experienced circuiteer, since some of these structural changes will have little immediate impact on circuit behavior, and may go unnoticed in simulation, which will not accurately model every conduction mechanism, in modern fully scalable bipolar transistor. Similar considerations apply, of course, to MOS devices.

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[5] A less common concern arises where there is no nearby metal to short to. In this scenario, the wear mechanism amounts to a progressive increase in the electron density as the material migrates away from the central conduction path, and into the whiskers, where the main-axis current flow is essentially zero.

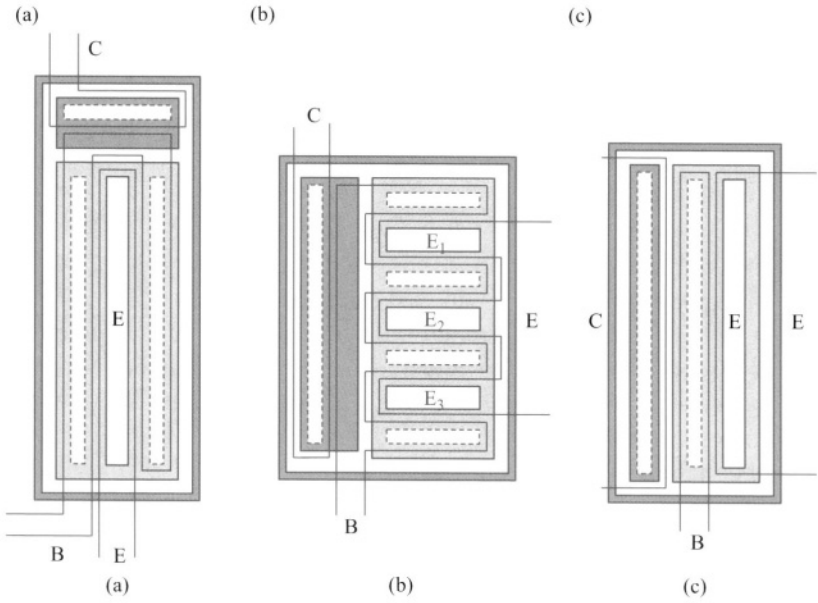


Figure 33.5. Current-density management at emitter contacts.

33.2.2. Other Metalization Trade-Offs

All branches that are expected to carry large currents should be annotated to indicate the estimated average (or maximum fault-condition) current. This allows the layouteer to choose an appropriate metal layer, or sometimes combined layers, and its width to cope with these currents. This also has a bearing on the number of vias that should be used between metal layers. Rules about the minimum number of required vias should not be interpreted as the "correct" number. They should be used generously between metal layers: vias are absolutely free, and present one of the rare occasions when no trade-off is involved! If an IC pin current is likely to be high, two or more pads and multiple bond-wires may sometimes be needed. This should be anticipated by the circuiteer, and explicitly indicated on the pseudo-layout schematic. The layouteer will need to maintain a close watch on these, however, since a less-experienced designer may not provide all the needed practical guidance.

Wide metal may be required at times for a different reason, namely, to provide especially low connection resistances. Such needs often arise in the intraconnects (and to a lesser extent in the interconnects) in translinear cells and band-gap references, where the delta-V_{BE}s are of crucial importance. For example, even a few microvolts of resistance-generated voltage arising in an analog multiplier or variable-gain cell can introduce significant amounts of

harmonic distortion. In such cases, the use of metal-level changes through vias would be ill-advised (their resistance is somewhat ambiguous) and the circuiteer must anticipate this danger, and mark such conductors as needing to be realized on a single continuous layer. Here again, some team conventions are useful. Special "resistance-free" or "resistance-equalized" connections can, for example, be indicated on the schematic by adding widened cosmetic lines along their length.

Frequently in monolithic analog design, signals are transported in the form of *differential pairs,* and the relevant conductors are almost always kept adjacent across the layout. One can assume that a skilled layouteer will observe this rigor instinctively, but it is nonetheless good practice on the part of the circuiteer – and very easy – to make this clear on the schematics, rather than *assuming* anything. In special cases, such as two pairs of differential signals in quadrature from a local oscillator, it may be important to keep all four traces close together. Certainly, the *total length* of these traces should be as nearly identical as possible, and changes from one layer to another (when such is unavoidable) must be made at the same general breakpoints, with a view to matching delay/phase. Occasionally, dummy lengths of metal may need to be added to balance parasitics, either resistance or capacitance or both.

The requirement for very narrow interconnections should also be marked on the schematic. Usually, these are used with a view to minimizing the parasitic *loading capacitance* on these traces. It is of equal importance to minimize *coupling into the substrate,* when the signals on this trace could endanger other cells in the complete system, or *the fringing capacitance between adjacent traces.* These various objectives should not be confused. On the other hand, long narrow traces may generate excessive resistance, which is equally capable of slowing a circuit. Some simple modeling of these interconnections will point to a broad optimum and resolve this trade-off.

It is important to keep in mind that the software algorithms used to extract metalization capacitances are often rather simplistic. They may do an adequate job of modeling metal-to-metal capacitances (between adjacent traces and at crossovers between different layers) and in capturing the effects of fringing fields. However, they probably won't correctly model the capacitances where a metal trace passes over some other element, such as a transistor, a block of resistors, or the non-metallic top plate of certain capacitors. This can lead to errors of two sorts. First, the net *loading* impedance may be pessimistically modeled. For example, when a trace is allowed to cross a block of resistors, of moderate to high value, the net impedance of the loading will be reduced, and thus the asymptotic impedance at high frequencies may in fact be lower than indicated by the back-annotation. Second, signal coupling *both out of and into* such elements will not be modeled, and a potentially serious source of signal disturbance or performance skew may be obscured.

The most certain way of avoiding such problems would be to forbid signal-bearing conductors to cross circuit components over a significant total area. Even ground and supply metals will exert a small loading effect on such areas, and may lead to effects that are never captured in any simulation studies, while in fact having a strong bearing on circuit behavior. But the avoidance of such metal routes may present a trade-off, if it is cast in the form of an option. As a compromise, the team could agree that, even though *permitted* by the layout rules, metal traces will not be routed over certain elements (notably resistors) under *any* conditions, thus eliminating altogether the risk of this type of signal coupling. The trade-off now is a *forced,* rather than an *elective,* one. The downside of this choice is that metal traces may be longer than otherwise possible, and the layout less compact.

In other circumstances, the circuiteer will again need to account for the effect on circuit performance arising from the *resistance* of long interconnects. This is often negligible (say, in conveying a current from a biasing cell to its destination), but on other occasions it may be extremely important. For example, suppose a signal is to be conveyed from a source cell having some low output resistance to a destination cell that likewise presents a small load impedance. To address worries about coupling of this signal to the substrate, which is not, of course, a zero-impedance node (see Section 3.3) the circuiteer may propose a minimum-width metal trace. If this is $2\,\mu\text{m}$ and the sheet resistance is assumed to be $50\,\text{m}\Omega$ per square, and the total length of this trace were 1 mm (roughly, ten pad pitches) the resulting resistance would be $(1000/2)^{*}0.05 = 25\,\Omega$. This could be serious in many cases. Often, the loss of signal may not be troublesome, but other currents, possibly of high amplitude, may couple into this line and disturb operation in some critical way. Since the TCR of copper-doped aluminum is about 3, 800 ppm/°C, voltage drops will vary with temperature in a roughly "PTAT" fashion, when these interconnects carry a temperature-stable current.

The loading effects of the capacitance of long metal traces can sometimes be addressed by simple changes to the circuit. For example, consider the circuit shown in Figure 33.6. Here, the overall plan for the layout requires that the current-mode signal output of Cell A has necessarily to be conveyed over a relatively long distance before being utilized in its target, Cell B, where it is converted to a voltage by R_1 and then level-shifted by emitter-follower Q_1 before the next step in the chain. Clearly, it was likely that the circuiteer was thinking in a particular way that led to this division in the cell functions; it *may* have not been appreciated that this connection would traverse such a great distance. (It should be added that the use of the pseudo-layout top schematic would almost certainly have caught this routing issue.)

The alert layouteer, however, will notice that the capacitance of this long wire will severely load the source, when operating at the impedance level set by

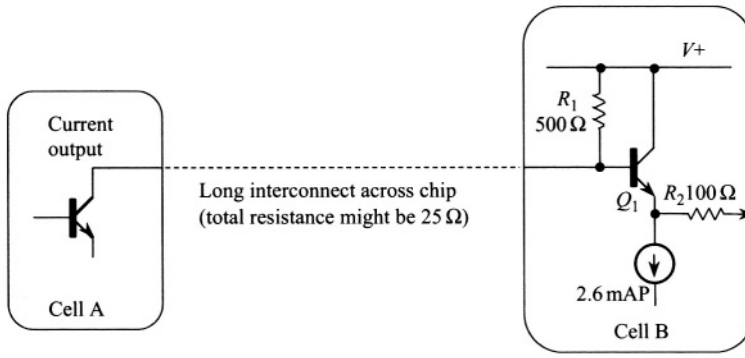


Figure 33.6. A signal-intraconnect scenario.

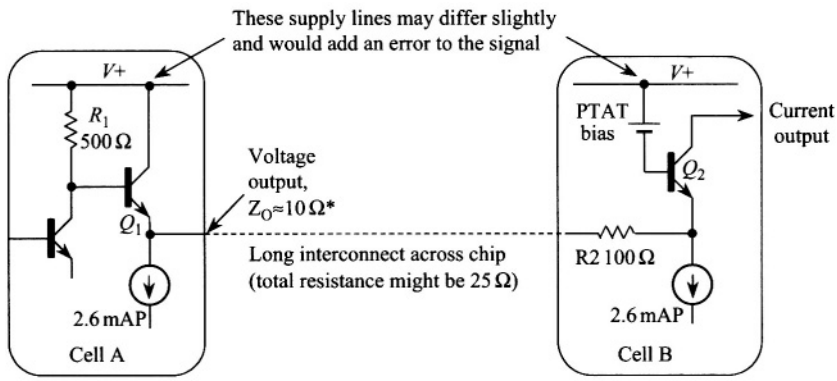


Figure 33.7. A revision to the signal-intraconnect plan.

R_1, and realize that this might have been a design oversight. By simply repositioning the emitter follower on the layout, to inside Cell A, the driving point impedance can be reduced by a factor often (Figure 33.7). This is because R_1 is shown as being $500\,\Omega$, while the emitter-follower is operating at 2.6 mAP (the circuiteer showed this much on the schematic, and was careful enough to also note the current as being PTAT) and thus its output resistance has a temperature-independent value of $10\,\Omega$ (kT/qI). The lower driving point impedance could significantly improve the bandwidth of this interconnection, and the possibility of a revision should be brought to the attention of the circuiteer.

However, confirmation is crucial, since there may actually have been a good reason for breaking the cells in the way shown on the schematic. For example, the output impedance of the emitter follower is inductive and may conspire with the lead capacitance to form a high-Q resonant response, or be severe enough to cause sustained oscillations. It is not at all unlikely that the

changing output impedance of the emitter follower over a large signal range will cause subtle and hard-to-locate conditional oscillations, at a very high and perhaps undetected frequency. In working silicon, a strange kind of signal distortion caused by these "squegging" oscillations may be apparent. Equally troublesome, the metal resistance is now in series with R_2, increasing its value by an uncertain amount of about 25%.

For this kind of teamwork to happen, the circuiteer and the layouteer must understand each other's task. The circuiteer, thinking in layout terms, should have been aware that the chosen cell boundaries and the long route would conspire to generate a "nuisance pole"; on the other hand, a layouteer unaware of circuit behavior, or unable to judge the beneficial effect of the emitter follower, through long familiarity with such circuit methods, would have not caught this indiscretion, or have been able to offer a better arrangement. But supposing that the emitter follower was indeed deliberately removed to Cell B, in another area of the layout, because it must be in exactly the same *thermal environment* as Q_2, a requirement that relates to some other (unspecified) circuit function, and to which the V_{BE} of Q_1 must closely match?

We're here faced with apparently conflicting needs: a classical trade-off! Here, mastery of one's medium may be exerted by either the experienced layouteer (who has an extensive bag of tricks up his sleeve) or by the circuiteer (who is thinking about all the many ways her circuit might be prone to layout indiscretions). The interconnection cannot be long, yet must be associated with the base of the emitter-follower, Q_1, because that transistor cannot be moved into Cell A. The solution in this case may be to pull out of the bag the common trick of *bootstrapping*. For this to work, at least two layers of metalization are needed, and in practice more may be required to cope with crossovers. Figure 33.8 shows the idea. The high-impedance node is run along the top of an underlying metal trace connected to the emitter of Q_1. Since the voltage at this emitter is almost exactly equal to that on the base, the effect of the capacitance between the upper and lower traces can be reduced. Meanwhile, the capacitance on the lower metal is driven by a much lower impedance, which essentially eliminates the nuisance pole in the transmission function. This kind of measure is quite general, and often possible (not only where emitter- or source-followers are used). The circuit will be correctly modeled when the layout is back-annotated.

In a variation of this theme, the effective capacitance of a bonding pad can likewise be reduced by bootstrapping an underlying plate (perhaps now a buried-payer diffusion) from a low-impedance driving point. At very high frequencies, however, this ruse may backfire, due to the complex circuit impedances that prevail, although here again, the back-annotation will reliably point out such problems. In other cases, bootstrapping may be useful to eliminate the effects of DC leakage paths at sensitive nodes (e.g. the inputs of

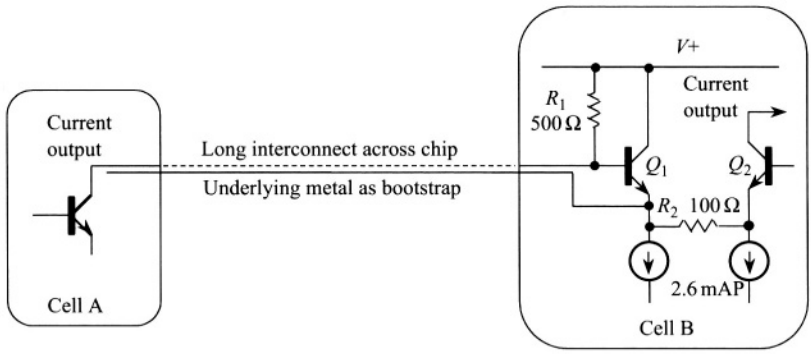


Figure 33.8. An alternative plan using bootstrapping.

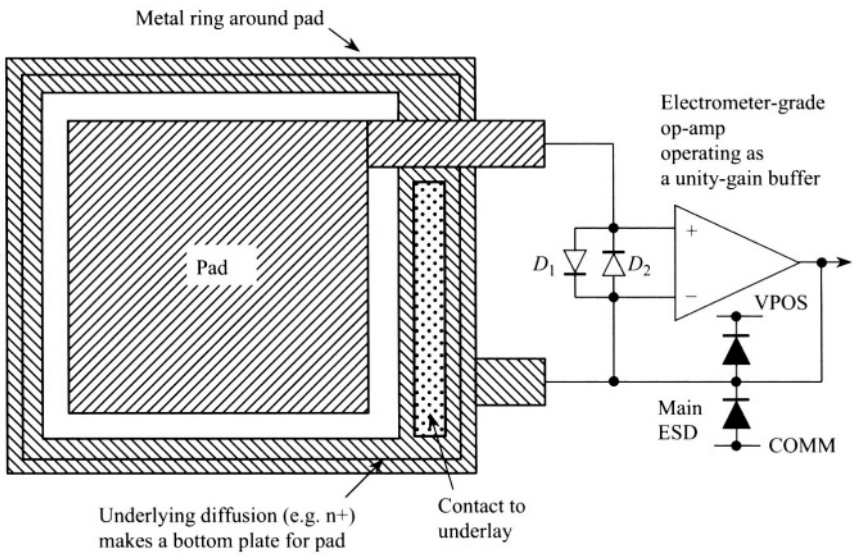


Figure 33.9. A bootstrapped guard-ring.

an electrometer-grade preamplifier), where a guard-ring around the input pads should be used, as shown in Figure 33.9. If possible, two adjacent pads and pins should also be used to guard this pin at the board level. Another detail shown in this circuit is also commonly found in this type of product. This is the elimination of conventional ESD protection, and the alternative use of a "box" of low-voltage diodes, D_1/D_2, with the ESD diodes on the remote side, at the amplifier's output. The trade-off here is that chip area and extra package pins are being used for a fairly small, although possibly invaluable, payback. On the other hand, the die cost for many analog circuits is already very low,

and the value added comes in the form of advances in performance and overall engineering finesse at every stage of the product development.

Whether layout trade-offs of this nature are made by the circuiteer or layouteer is not critical. Knowing what one can reliably expect from all team members is more important. A good team supports its colleagues in avoiding a bad outcome. But even the most expert layouteers are not mind readers. Unless kept well informed, they may have no way of knowing what bizarre acts are scheduled to appear in the circus ring devised by the circuiteer, apart from guessing, based on similar projects and the experience gained through these. Even then, no two products are alike, and the possibilities for missteps are endless.

While it is unlikely that every eventuality can ever be anticipated, it is incumbent on the circuiteer to make every intention crystal clear, using a liberally annotated top schematic to "tell the story". A high proportion of disappointments in IC performance can be traced to some sort of interconnect-related phenomenon, whether it be signal loading, signal coupling, unaccounted for resistances, or indiscretions in choosing the precise location of connection points.

33.3. Substrates and the Myth of "Ground"

It is well known that monolithic circuits are built on a silicon platform, the upper side of which contains all the interesting stuff, while the lower side is pretty dull, being little more than the mechanical handle, which, by the way, is uniformly connected to "ground" in some way or another. The truth is more complex, and can only begin to be fully appreciated as each circuit takes on more realism in a set of layout drawings.

Most conventional junction-isolated IC processes start with a rather pure silicon wafer of a certain polarity type, doped to a certain level and thus somewhat conductive. For example, in a conventional NPN bipolar process, this material is boron doped (P-type) and has a typical resistivity of 5 Ω-cm. In order for the collector–substrate junction to remain reverse-biased, it is customary to bias the substrate at the most negative potential for the circuit. For earlier analog ICs, this used to be the negative supply rail of – 15V, later – 15V; for the majority of modern ICs, operating on a single positive supply of +5 V, +3 V or less, it will be ground. This is convenient, since the metal paddle on which the chip will be mounted, and electrically connected across the entire lower surface, can then easily and directly be connected to the "ground plane" of the printed circuit board on which the IC is mounted. In chip-scale packages (CSP) and other types, this paddle is exposed, affording both a low electrical resistance in the path to system ground, and a low thermal resistance, which is becoming an increasingly critical concern in many classes of communications products.

The direct connections between the IC circuit-level ground and the paddle still have to be made. This is often implemented by the use of one or more "down-bonds" (Figure 33.10). These serve to lower the impedance by shortening the length of the bond-wires. Using the corner pins of a package for the ground connections also minimizes the vulnerability to ESD events on the often more sensitive signal pins, which are less exposed to contact with charge sources when placed at an inner position along the package edges. The extravagant use of four pins for the one "Common" node, as shown in the figure, will often be contraindicated by the need to minimize the overall pin count, or the need to separate analog/digital or input/output grounds, or simply because a more attractive pin-out can be devised for the function, bearing in mind the intended applications and board layouts. These are common trade-offs, if one may be excused the *double entendre.*

While the emphasis in high-frequency practice is to make very liberal use of multiple ground pins, similar considerations apply to the supply pins, particularly those associated with output stages that drive considerable current into a load. Obviously, this current does not flow just in the output pin(s): the circuit is completed through both the common node, which often will be one or more dedicated pins for exclusive use by such an output stage, and the supply node, which likewise may need just as many low-impedance connections. Considerations of such a basic kind need to be made right at the start of the development, using the preliminary floor-plan, and be carried through a continuous chain of

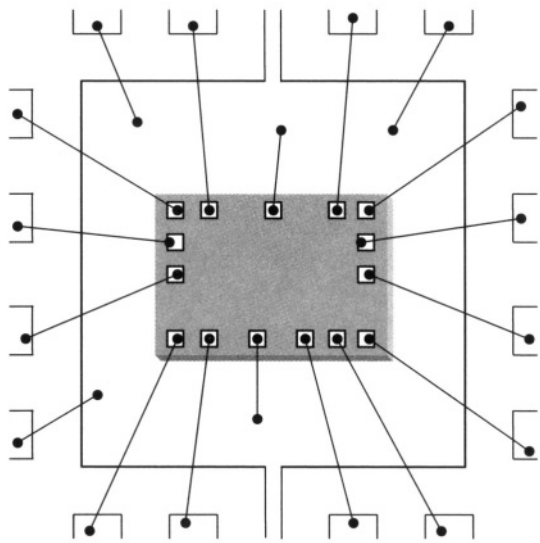


Figure 33.10. Use of down-bonds.

design steps, right up to the fully annotated pseudo-layout schematic. It has often been said that "the Devil's in the details": in analog design, it's nothing but details.

The traditional pressure to minimize pin count is gradually giving way to the view that the manufacturing cost difference between, say, a 16- or 28-pin package is in many cases quite negligible, and it is senseless to jeopardize the performance advantages obtained by providing low-impedance connections between the chip ground and supply nodes and the corresponding board-level nodes. The more important difference may be in board area. Some applications (cellular handsets being a prime example) size is everything, and many of the RF support functions (such as antenna power measurement) are expected to be realized in tiny packages, such as the minuscule 6-pin $1 \times 2\,\text{mm}^2$ SC-70 package. On the other hand, some functions, such as a baseband-to-RF modulator, may demand the use of these multiple ground and supply pins, simply to achieve the required high level of performance.

In contemporary practice, it is increasingly the case that one or more pins formed by the etched or stamped metal header are extended to be electrically contiguous with the paddle. These are called "fused lead-frames". To minimize the number of different header styles needed, some agreement has to be reached as to which pins are to be fused. In optimizing a header for a 16-pin CSP for RF applications, all four corner pins might be fused, although even a single fused lead is valuable. Fused leads may eliminate the need for down-bonds, which are difficult to include when the chip size is almost equal to the maximum that may be accommodated on the paddle area, and which will also slightly reduce yield due to the occasional faulty stitch-bond. They also improve the quality of the ground connection to the die underside, by lowering both the resistive and inductive magnitude of the impedance. As previously noted, many modern packages allow the underside of the paddle to be exposed (not covered by the plastic molding), and soldered over its full area to the PC board. This not only makes the ultimate ground connection, but also greatly lowers the thermal resistance from IC chip to board ambient.

Even when using the best of these techniques, it would be a mistake to assume that a node labeled "COMM" will conveniently correspond to perfect "ground connection" anywhere across the full extent of the circuit (at the simulation level) or the chip (at the layout level). The idea of a chip-level ground plane is seductive, but in practice it is an elusive myth. Even at moderate frequencies, on-chip grounds will be very lively, because of the consequences of the interconnection resistances from inside a cell to the point at which a ground connection is made to the outside world. At frequencies of the sort commonly used in communications ICs (in the range 200 MHz to 2.5 GHz, and higher in more recent systems) the notion

of a "mecca" called ground, at which there is no potential variation, is laughable.[6]

33.3.1. Device-Level Substrate Nodes

Prior to the layout of any circuit, the circuiteer must define the node to which the device's local "substrate node" is connected, for each of the components, in order that the parasitic effects related to the device/substrate interface can be modeled. For an NPN transistor, these relate to the collector–substrate junction and include its leakage current, its capacitance (C_{JS}) and the variation of C_{JS} with voltage. However, this modeling is incomplete, for at least two reasons.

First, there is also an important resistive component associated with C_{JS} that is not included in basic SPICE models. This can have a marked bearing on the noise performance of an RF LNA, for example, due to the injection of the Johnson noise of this resistance directly to the output node, through one or more C_{JS}. Second, and more worrisome, in the layout version of the circuit (and in reality) this junction is not directly connected to the node named in the circuit schematic (say COMM, which would enjoy a short circuit to "Ø", the ultimate zero-potential reference node in SPICE, should the package and interconnection modeling be unwisely excluded). Rather, it is driven by *the substrate potentials that appear in the vicinity of each component.*

As noted, these AC voltages may be quite large, unless special precautions are taken to reduce the impedance between the local substrate connection on the top surface and the best possible choice of "ground" at the chip level. If general rules are of any value, the substrate nodes for all elements within a small cell (which includes the relevant node for supermodels of all passive components) should be connected to a single node which is given a special name and which must be viewed as a true signal node. The way this node finds a path to others external to the cell, all seeking a path to the header "ground", is a matter of considerable complexity. The trade-off in this case involves making pragmatic decisions about what can safely be omitted and what prudence dictates must be included.

The substrate may not be regarded as a true ground in another scenario, which arises when a junction-isolated NPN transistor goes into deep saturation, that is, its collector junction is strongly forward-biased. This floods the P-material

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6 Should there be any doubt about this, try probing chip-level "ground" nodes during high-frequency AC simulations, using comprehensive package and interconnection modeling. It is not unusual to find these nodes at 20 dB or more *above* the signal input level over certain bands of frequencies, until remedial steps are taken to tighten up the grounding disciplines. Even then, these so-called ground nodes will rarely show signal levels much below a few dBc. Exercises of this sort can be very sobering, and serve to remind us of the need for even greater care in translating the schematic to the layout.

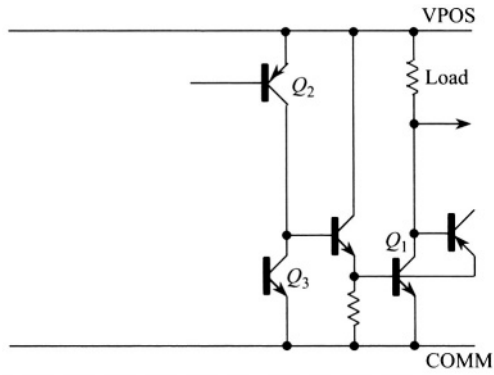


Figure 33.11. An example of the effects of proximity.

in the surrounding material with spurious carriers which can often find their way to other surrounding elements and thereby form sneak signal paths, and in severe cases, latch-up.[7]

Figure 33.11 shows a layout involving a *potentially* saturating transistor, Q_1, placed too close to a lateral **PNP,** Q_2, which supplies what is supposed to be a moderate bias current for Q_3. Under most circumstances, this layout will work fine, but if for some reason Q_1 should saturate, the "loose electrons" that manage to find their way to the base of Q_2 (which in fact is the N-epi layer immediately adjacent to the collector of Q_1) can sustain a high-current latch-up condition that cannot be released until the supply is removed. The most obvious solution is to move Q_2 far enough away from Q_1 (or any other transistor likely to saturate). In some cases, even the use of a well-grounded isolation ring all around Q_2 may not prevent the influx of carriers into its effective base region.

At one time, it was common to exploit many such merged structures to reduce the die area, when the base-to-isolation distance was large, usually with complete success. Nowadays, the benefits of merging are less apparent, and the risks are generally regarded as too high. This aversion can also be attributed to the difficulty of being sure about device modeling for simulation studies. Later, it will be argued that this is a layout/design method to reconsider.

33.4. Starting an Analog Layout

The IC designer probably feels that most of the needed trade-offs will have been addressed by the time the layout starts. This could be true, if this circuiteer

[7] This used to happen frequently in earlier analog layouts, but it is less likely to occur using today's practices.

is thinking like a layouteer and is worrying about all the same issues, which tend to be of a somewhat more practical kind. More likely, however, the benefit of the team endeavor will become fully evident only subsequent to the transference of a "final design" to layout. This chapter has stressed the importance of the *shared responsibility* of the electrical and layout design of a product, and while the precise division of labor will vary from team to team, and from time to time, this principle will continue being emphasized as we continue.

The chief objective of the layouteer will be to accurately implement the *intent* of the circuiteer. But this is different *from faithfully following* the circuiteer's instructions. A good layouteer will also play the role of advocate and watchdog, suggesting in many small but important ways how each step toward reality should be taken. After this overarching responsibility, the next will be to ensure that the layout is compact and realizes a minimal die area. This can only happen when sufficient forethought is applied, before even a single polygon is drawn on the general floor plan. Here again, a well-oiled team will know how to best ensure this outcome The circuiteer's use of the pseudo-layout method for the top schematic is a good starting point. As noted, this can be a powerful tool for minimizing the routing complexity, when employed carefully and creatively. Meanwhile, the layouteer can start to focus on the interior of the key cells – those that are novel in this product, or crucial to its success, or which consume the greatest area or define basic dimensions – and decide how to achieve a reasonable compliance to the suggested aspect ratio and preserve the pad locations recommended in the pseudo-layout schematic.

The question of how to take the first step in developing a layout will always be a matter of circumstance, personal style and experience. However, some approaches are more effective than others, and, just as in planning a building, the first step is to define the boundaries within which the entire structure is to be built. This is fairly straightforward, since the maximum die outline will invariably be predetermined by (1) cost considerations, (2) the number of pads and (3) the available mounting area for a given package. This approach is analogous to that advocated in Chapter 2, for planning the product design, by *visualizing the finale,* and then working to ensure that the layout converges on this outcome, and all the development goals are met. The alternative, of starting with cells and only later thinking about the overall chip plan, will surely lead to poorly chosen sizes for these cells and an insolvable jigsaw puzzle.

In good layout practice, one starts by drawing a preliminary chip boundary, based on the facts currently at hand, locating the pads based on bond-wire considerations, adding the main power buses and even a few of the major metal routes, and including the ESD protection devices. This provides the minimal, necessary framework for the layout development. If boundary adjustments are later needed, they can be done fairly quickly in a modern software context. This drawing will also be used to check the angles and clearances of the

bond-wires. Even at this early stage, some trade-off may be needed. For example, in connecting to a high-power output driver, multiple bond-wires will often be needed. But when these are sketched in place, it may be found that pins that were planned to be along the same side of the chip may need to be moved, and this could influence the floor plan and even the pin sequence.

In planning the placement of the major blocks, both designers will be equally concerned about such details as the use of a thermal axis of symmetry, the avoidance of high-stress areas, common-centroid techniques to reject all manner of chip gradients, the fine-tuning of transistor geometries and above all, relentless, unflagging attention to device matching.

33.5. Device Matching

No other aspect of monolithic design is more important than *matching,* and the allied use of *ratios.* A consummate reliance on *like-against-like* is the cornerstone of analog circuit design and of more than passing interest in many digital cells. Such a reliance is practicable, since it is grounded in fundamental ideas about materials, and has proved to be dependable in case after case. Matching (aided and abetted by its close cousin, isothermal device operation), is nowadays regarded as a kind of birthright for the circuit designer and layout designer alike. However, while a *dependable principle,* the attainment of close matching is not automatic. There are many rules, most quite obvious, others more subtle, for ensuring that the needed closeness in parameter values can be guaranteed in high-volume production. In the course of pursuing tight matching, frustrating trade-offs are encountered. We cannot be overly concerned about whether these should properly be made by the circuiteer or the layouteer. Nevertheless, whoever is the one to resolve them, they are manifestly *trade-offs in layout.*

The detailed behavior of all components on a chip is a function of their physical dimensions, and many of these are extremely small. Production variances in the thickness, width and length of layers cause large variations in parameters. Standard deviations of 10% in the *absolute* value are common, meaning that variations of up to ±30% will regularly occur in the for an isolated element in a production sample size. Aspects of circuit performance that are forced to be *Dependent on Absolute Parameters* were identified as DAPs in Chapter 2. The circuit designer can do much to mitigate the effect of such variations, but they rarely can be eliminated. In such cases, we do our best to provide a margin of safety, so that elements at the "extreme end" of some possible range of values (not a statistically precise statement) will still result in "acceptable" performance (likewise imprecise). The use of physically large elements will reduce the spread of parameter values, to the extent that these are caused

by *delineation* errors, which are generally a consequence of imperfections in photolithography.

In many other cases, however, considerable variation in absolute values is permissible. Those aspects of performance that are *Tolerant of Absolute Parameters* were identified as TAPs. Device matching[8] is with a view to implementing circuit cells based on this particular kind of robustness. Even in the first-generation IC processes of the mid-1960s, matching as close as 0.1 % could often be achieved between a pair of diffused resistors, with care in layout. This was partly a consequence of their size, perhaps as large as $25 \times 125\ \mu m^2$. Modern ICs use far smaller components, and mismatches are consequently much worse, commonly in the range 0.3–3% unless special precautions are taken. It is always unwise to *presume* tight matching, and safer to explore the effects of a worst-case scenario.

It is not possible to depend on the precision in any element ratio that is implemented through the use of *differing* dimensions. Thus, in the case of two resistors, each of $5\ k\Omega$, we clearly will make these as identical geometries, and can speak correctly of their matching properties. However, it is dangerous to presume an accurate ratio will be exhibited between a $5\ k\Omega$ and a $1\ k\Omega$ resistor in which the length of the former is simply five times that of the latter. It is more dangerous (and somewhat pointless) to use resistors of differing widths in those cases where their ratio is of even moderate importance. Not only are these at the mercy of *random* width variations which do not equally affect them, but more troublesome is the impact of *process biases,* that is, the fixed difference between the *drawn widths* on the layout and the final *effective width* after masking anomalies, including diffraction and shadowing effects, etching, non-uniform doping or deposition, and other processing steps.

The detailed specification of how all elements are to be implemented at the layout level is an *integral part of circuit design:* it must be captured at the schematic level, with the greatest possible rigor and concern for detail. Even the most carefully wrought analog circuit design is likely to perform badly if dimensioning – whether of active or passive devices – is treated in a casual manner. By far, the safest practice is the use of *unit elements* to ensure precise matching, where this is critical, and even when it is thought to be unimportant. (It is distressing to only later discover that it really was, after all.) The extensive utilization of unit elements, arranged in simple matching pairs, or grouped as matching quads, or combined in suitable ways to realize integer or low-fractional ratios, is very common in analog design. More detailed examples will be discussed for specific component types.

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[8] The term "matching" is loosely employed to refer to the exactness in a nominal *ratio* between any two like components, but a more precise use of the term is in connection with the deviation of a particular device parameter between two *nominally identical* devices.

However, even this discipline does not automatically guarantee close matching, since *short-range variations* in material properties is an all-pervasive aspect of real elements. If there were some way to measure in elaborate detail the specific electrical parameter that is subject to variation – say, the incremental sheet resistance of a layer – over fractional micron ranges, and plotted this versus large-range distances, it would almost certainly take the form of a noisy waveform (Figure 33.12(a)). The shorter-range variations will be due to grain sizes (much more pronounced in polycrystalline layers than in diffused layers), while the longer-range variations can be attributed to non-uniform deposition (as in thin-film resistors).

Whatever the physical details, such variations can be represented in the spatial frequency domain, through their Fourier transforms, as white or pink noise (Figure 33.12(b)). In the first case, there is an equal probability of an "undulation" in the parameter having a certain magnitude for periods of any length. The statistical implication of this physical fact, which is not a manifestation of *process control,* but fundamental to the *constituent materials,* is that the uncertainty in the ratio between any two unit devices, in the absence of any gradients or topological influences, reduces as the square root of the area. This $1/\sqrt{A}$ prediction has been verified by numerous experiments. The noise in the spatial domain will be pink for materials having a granular structure over somewhat longer distances (such as poly resistors). The probability of large-magnitude

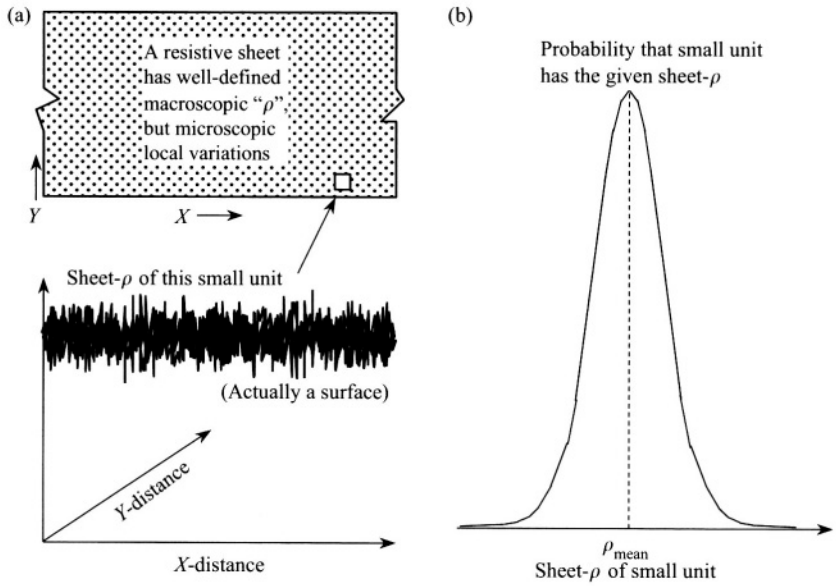


Figure 33.12. Short-range variations in sheet resistance.

variations is elevated at dimensions corresponding to the grain boundaries. However, the $1/\sqrt{A}$ rule is generally a good guide.

This leads to the troubling realization that *mismatches may NOT be predominantly caused by poor control of lithography,* although numerous detailed effects undoubtedly do conspire to introduce both random and systematic errors in delineation. The sobering fact is that, even if the lithography were perfect, the granularity statistics ultimately determine the precision of resistor values. By the same reasoning, it will be apparent that, to the degree that mismatches are influenced by delineation errors, it is incorrect to suppose that doubling the width of a resistor will halve the random mismatch. Even where the delineation errors dominate, as for narrow resistors, or where the granularity is of very small amplitude, as for thin-film and diffused resistors, this will be only approximately true.

33.5.1. The "Biggest-of-All" Layout Trade-Off

We are here facing the *biggest-of-all trade-offs in analog layout*: to achieve good matching, elements must be physically large. Unfortunately, large components consume proportionally more chip area; furthermore, the parasitic capacitance of large-area components may quickly become prohibitive. This is very bad news in analog circuits, and is frequently the primary limiting factor to achieving high accuracy, of many kinds (e.g. the gain of high-frequency amplifiers, the calibration of voltage references, the scaling of nonlinear circuits) and low offsets (at the input of sensitive amplifiers). Matching also limits other aspects of signal processing, such as feedthrough effects, channel matching and intermodulation.

In spite of their tiny dimensions, satisfactory matching can usually be achieved between most components without using excessive die area, or incurring too much inertia. Decisions about the physical size of all components will generally be made by the circuiteer, working at the schematic capture level, as each new element is added to the design. It is unwise to leave the dimensions unspecified until the last moment, with the argument that they are not an essential part of the electrical design challenge. This is occasionally true, where, say, a single resistor or capacitor stands apart from its surroundings. But more often than not, the matching of components, whether pairwise, or in local groups, or from one cell to another, will have profound implications. When matching requirements are lumped into groups, each of these must be identified and the element dimensions quantified with meticulous care.

Aside from these matching considerations, the physical dimensions determine the parasitic capacitances of circuit elements, which must also be fully accounted for, particularly in high-frequency simulations, by the use of supermodels. Be aware at all times that your objectives for the IC may not directly

require certain HF properties, but *the circuit does not know your intentions,* and constant vigilance is needed in ensuring that it is not prone to microwave oscillations behind your back. Where speed is of less concern, some freedom may be given to the layouteer to choose dimensions later, particularly in the case of resistors. Of course, the physical sizing and layout style of transistors controls their circuit behavior very strongly.

33.5.2. Matching Rules for Specific Components

The methods by which close matching of IC components can be achieved differ only slightly from one element type to another. The general rules are as follows; additional rules are needed for specific components.

1 Identical "unit" geometries of the same materials should be used to realize the highest accuracy, and other ratios developed by combining unit elements.

2 The use of large dimensions for these elements generally favors matching, at least up to the point beyond which long-range effects (die gradients) play a role; in any event, avoid very short or narrow dimensions, even when invoking geometric similarity.

3 Elements that are required to match should be as close to each other as possible.

4 The elements should be in the same orientation relative to the chip boundary.

5 Interdigitation and common-centroid methods should be applied to minimize gradient effects.

6 Dummy elements should be added at the boundary of a set of matching components.

7 Thermally sensitive elements should straddle the major thermal axis of the die, if such can be identified or created by suitable adjustments to the overall layout; in any event, these elements should be placed as far as possible from significant power-dissipating devices.

8 The elements having the most critical matching requirements should be placed close to the center of the die.

In dicussing some general aspects of the matching challenge, some important aspects of resistor layout were touched on. These will now be further elaborated.

Each end of a resistor entails a contact, the interface between the resistive material and the metal interconnect. In some cases, an actual third interface layer will be added. For example, a lightly doped silicon P-layer would form a

Schottky barrier with aluminum, rather than an ohmic contact. In such resistors (which might be formed using the intrinsic base layer of an NPN transistor), a contact diffusion of more highly doped P-silicon must be used. A different rationale applies to the otherwise similar use of an interface layer to contact a thin-film layer such as SiCr or NiCr resistor. The active thickness of a $1\,k\Omega/square$ SiCr film is commonly as little as 25 Å – only a few atomic layers – while the contacting metal layer will be several hundred times thicker. Due to the processing sequence, the surface of the SiCr film will not readily make a low-resistance (and low-noise) contact to the metal, so a barrier layer of a more highly conductive material is added to the film for contacting purposes.

In all cases, the contact region of a nominal resistor of well-controlled length and width will introduce a further component of resistance, and it will be prone to some variation from one element to a similar one. Where the length/width ratio is small, and the highest possible accuracy of match is needed, the contact area may need to be enlarged beyond that generated by the standard parameterized cell (P-cell) provided by the layout database. Increases in the transverse width of the contact have a large effect on lowering contact resistance; extensions along the length axis have rapidly diminishing value, since the current density in the contact falls dramatically away from the inner-facing edge.

In high-precision DC applications it may be necessary to address the fact that a contact may also introduce a small thermo-electric potential, which varies with temperature, although usually by only a small factor, of the order of microvolts/degree. Where this matters, the contacts should be placed in close proximity. Thus, one might use a pair of parallel resistors, shorted by a metal bar at the remote end and contacted at the side-by-side proximal ends. But there is a trade-off here, too: by contacting at the same ends, any misalignment between the metal and/or additional contacting material and the body of the resistor will cause a change in the absolute value of that composite resistor. This will generally be of low importance when the unit element is moderately long, relative to the shift, and changes to the absolute value from this effect are only one of several factors affecting the net resistance, the largest being sheet resistance and width.

When forming arrays of unit elements to implement either larger resistors or sets of resistors that define important ratios, these should each be spaced by the same amount. The dummies at each end of an array need not have the full width of the unit elements, for thin-film and poly resistors, although there may be benefits to maintaining this width for diffused resistors. It is good practice to connect at least one end, and preferably both, to an appropriate circuit node. This may be a "quiet" node, such as ground (keeping in mind that no nodes on the die are absolutely silent), or one chosen to provide some useful bootstrapping effect for the outer element in the active array.

33.5.3. Capacitor Matching

As is true for resistors, some capacitors in an analog IC don't have to match at all; in many cases, even the exact value isn't critical. For example, it is generally not a serious matter if supply and bias-line decoupling capacitors are a little larger than originally planned. Frequently, "white spaces" that may arise in a layout can be advantageously used to increase some of these capacitances. Where this is done, it is important to back-annotate these changes into the schematic and rerun a selection of focused simulations to determine whether the increases did not introduce any surprises.

In other cases, the absolute value of the capacitor may determine important aspects of behavior. Thus, the "HF compensation" capacitor, C_C, in a basic g_m-integrator operational amplifier sets the unity-gain frequency rather directly. Discounting the effects of parasitics, and assuming a first-stage transconductance of g_m, the angular frequency at which the open-loop gain is unity is simply g_m/C_C. No amount of cleverness will circumvent this basic dilemma, which is a classic example of a "DAP". This does not mean that there are no ways to extend the bandwidth and slew-rate using more elaborate schemes; but even then, the absolute magnitude of this capacitor, and other capacitors which may be implicated in a more complex stabilization method, will largely determine the unity-gain frequency, unless very aggressive bandwidth pushing is employed. In that case, the dependence is merely transferred to transistor parameters, which are no more reliable.

Fortunately, the area of a moderate-sized IC capacitor is well above the point at which delineation of its critical boundary (the top plate) is a critical issue, and the oxide thickness is usually very well controlled. Furthermore, unlike a diffused resistor, there are no modulation effects arising from the bottom plate biasing in either a metal-oxide-metal capacitor (MOMCAP) or poly–poly capacitors, negligible voltage-nonlinearity (a few ppm/V at most), and very low stress and temperature dependencies. For these reasons, the absolute accuracy of such capacitors is higher than that of resistors. However, junction and MOS capacitors do exhibit bias dependence, and even double-poly capacitors are slightly nonlinear, due to the finite doping level of the two layers, which introduce depletion layers whose thicknesses are voltage dependent to varying degrees.

For many of the same reasons, the matching of capacitors is less prone to effects such as gradients in doping level and temperature than are resistors. Good layout practice demands that sets of unit capacitances are used wherever a precise ratio of other than unity is required. This discipline is often augmented by surrounding the active top plates by dummies of the same geometry, in a similar way to close-matched resistors, when these units are small in value (say, < 1 pF). For larger plates, perimeter effects are of little importance. Where

non-integer ratios are required, one can use a square plate for the smaller capacitor, C_S, and a rectangular plate for the larger capacitance, C_L, to address delineation uncertainties (often called "process biases", and applicable to all IC elements) in the side-lengths of the smaller plate. It is readily shown that when the second capacitor is constructed using a relative length and width of $(C_L/C_S)\{1 \pm \sqrt{(1-C_S/C_L)}\}$, both the area and perimeter components of the capacitances will be ratioed correctly, assuming a uniform delta in the dimensions for all sides. For example, if the ratio is to be 3.162, then C_L would be given a relative width of 0.5474 and a length of 5.777. These two approaches are compared in Figures 3.13(a) and (b).

However, a little thought shows that this would be an inefficient way to realize such a ratio requirement. First, it is unlikely to work out well in a real layout, particularly if many such ratioed pairs are needed. Second, the assumption of a delta that is independent of side length is unreliable in practice. Third, to ensure the perimeter components of capacitance are in the correct ratio, one might include a perimeter ring around the top plate, tied to the bottom plate; but that will only work well when the bottom plates are nominally grounded, and only transfers the problem to a more outward perimeter when both plates are active.

It is apparent that the correct way to approach this particular requirement would be to use one unit plate and three paralleled plates each having a relative

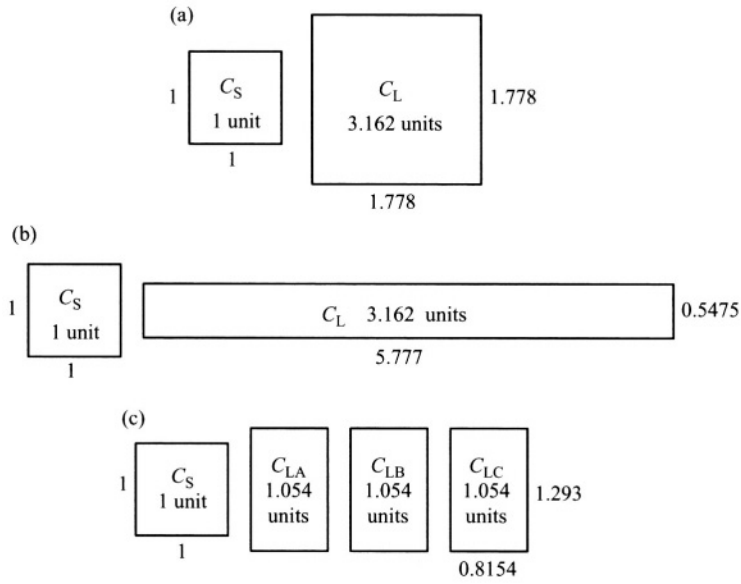


Figure 33.13. Various ways to realize an irrational capacitor ratio.

value of 3.162/3 = 1.054. Applying the same calculation, the relative widths of these three plates would be 0.8154 and their lengths 1.293 (Figure 33.13(c)). Of course, this leaves the problem of how these irrational dimensions are to be approximated when they must be subjected to the mask-making resolution, which may be as coarse as $0.1\,\mu\text{m}$. For example, a unit side of $10\,\mu\text{m}$ would put each of the second plates at $8.2 \times 12.9\,\mu\text{m}^2$, leading to a final ratio of 3.173, which is almost 0.4% in error. The trade-off here comes back to the same basic fact: any better matching will require the use of larger elements, although here it's because of mechanical limitation in defining rectangles to high enough resolution in the relevant masks, rather than fundamental physical effects, such as grain boundary fluctuations.

33.5.4. Circuit/Layout Synergy

This sort of situation arises often in practical IC design. Invariably, the optimal solution is not for the layouteer to go to extreme lengths to meet the circuiteer's specification, but rather for the latter to think in layout terms from the outset. One must ask: How important are these ratios? What is the precise effect on performance if they aren't perfectly correct? And, even after due attention to the plate sizes for these capacitors, will the wiring capacitance parasitics have a significant impact? There are trade-offs lurking here, in the constant tension between maintaining performance goals (depending on precise component values) and robustness (jeopardized by process biases and random delineation errors).

Surprisingly, perhaps, the genuine need for non-integer ratios arises relatively infrequently. Such are certainly indefensible when they are the consequence of a "cookbook" approach to design, and these hard-to-realize component values are nothing more than the output of some blind algorithm. Examples of this sort may arise in filter design, where the application of formal synthesis for a standard filter form (Butterworth, Bessel, Chebyshev and the like) of a certain order generate an arcane set of resistor and capacitor values. The use of exact values definitely becomes more important when very large numbers of poles and zeros are involved, and conformance to a very tight response mask is essential. But many less demanding filters do not need such rigor, or the use of a standard form, to perform quite adequately.

These forms, it should be remembered, allow the *systematic synthesis* of filters of increasing order, in a canonic fashion, and are indispensable for high-order filters where the number of combinations of possible component values is huge, and the correct solution is unlikely to be found by trial and error. However, the equations and design algorithms make no concessions to realization; they generate the "right" numbers within the rigid bounds of the theory, but not necessarily the right values for a practical circuit. It should also be remembered

that the bulk of classical analog filter design was developed before the availability of numerical simulation methods, and the implementation had to be "right by design" without much hope of exploring the consequences of being a little bit wrong, other than through the application of tedious sensitivity equations.

So here again, probing questions are needed: What key performance details must this filter really provide? Is the requirement to meet a certain AC magnitude response, in which case, is phase a critical factor? Or is the time-domain response, and the permissible amount of pulse overshoot, delay or settling time, more important? Is there a way of modifying the component values to use integer, near-integer or low fractional ratios? What is lost if these concessions to manufacturability are made? The need for pragmatic questions of this general sort is demanded in all aspects of IC design, not only in the realization of filter functions. Note that while the possible combination of values is immense when they may have any value in a continuum, and optimization outside of the formal theory is like hunting for the needle in the haystack, the solution becomes tractable when the components are forced to assume a finite number of discrete values. In such cases, many candidate solutions can be explored using simulation and a few nested DO-loops.

Figure 33.14 shows an "exact" solution for a fifth-order 0.1/40 dB elliptic high-pass filter, which has been partially rationalized to permit certain components to have simple values and/or integer ratios. However, the five capacitors

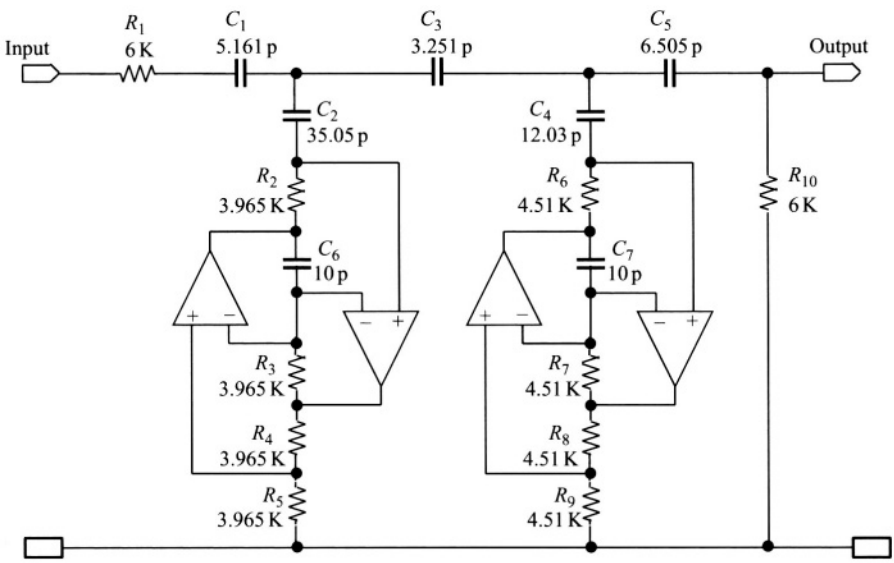


Figure 33.14. An exact realization for a 5th-order filter.

C_1 through C_5 still have irrational values, and would be difficult to manufacture with a high degree of robustness. It is an easy matter to predict the effect of bulk changes in the absolute value of the capacitors and resistors, since the corner frequency must be of the basic form *K/CR,* and there is no escape from the large variations in frequency that will occur from lot to lot, in a fixed-function filter of this sort.

On the other hand, the geometry of the pole-zero locus will be fixed by the ratios, which depend only on matching and ratioing. The sensitivity of this filter to random distributions of component values (both absolute values and mismatches) is easily explored in simulation by the use of Monte-Carlo methods. Figure 33.15 shows the AC magnitude response for thirty trials[9] in which all components were subjected to variation with a standard deviation of 1%. The lateral shifts in frequency – a "DAP" – are unavoidable, as previously noted. However, the 40 dB stop band response, and the 0.1 dB ripple width, are consistently attained.

While one could lay out the components of this filter with the precise values generated by the theory, the question arises: What is so special about the adherence to the elliptic formulation of this filter? Would a set of integer or

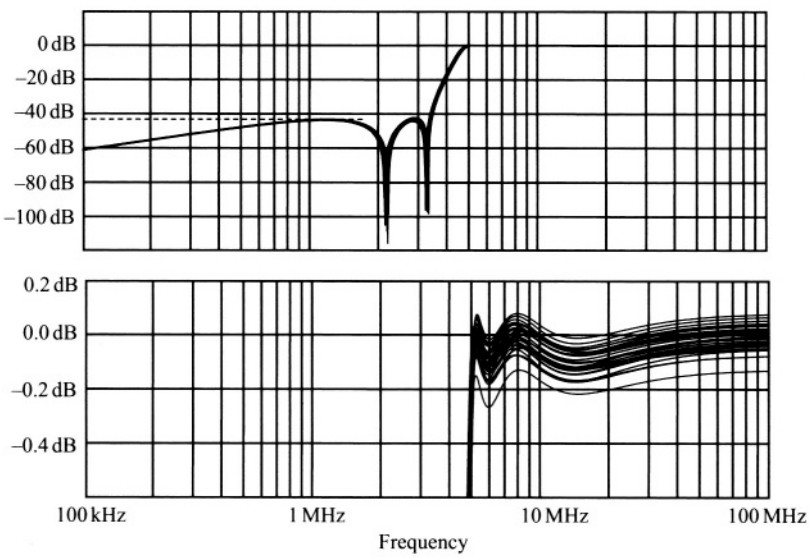


Figure 33.15. Monte-Carlo results for the 5th-order filter.

[9] Many more would be used in practice, but the resulting graphs would be harder to read for present purposes. Furthermore, a complete study would include the concurrent variations in the AC behavior of the op-amps.

low-order fractional ratios for the component values work as well? This is an interesting question, and deserving of a thorough discussion. But the basic points to be made here are, first: the formal solution found by applying one of the standard forms are only special in as much as they are analytic, which allows one to systematically synthesize high-order filters, and realize strict adherence to other performance aspects such as phase response, and thus rise-time, delay, overshoot, droop and other artifacts in the time-domain response. Second, non-formal filters, based on the use of more dependable component ratios, can often serve just as well, and, as we shall show here, may even have better properties.

Figure 33.16 shows a *partial rationalization,* in which only the capacitors have been given exact integer-ratioed values. The resistor ratios can be quite robust when all are made of the same generous width (and obviously, of the same material), since the length of the resistor for the particular values in this ohmic range and for these ratios will be sufficiently large that it will not introduce serious errors. In general, however, it is usually possible to take the next step and rationalize these resistors, also. For example, in g_m/C filters using a state-variable design technique, it is desirable to use uniform g_m values, all of which can then be varied to tune the filter to a precise frequency. Filters fabricated in this way will exhibit very exact response functions even in the presence of very large tolerances in absolute value.

For the present purposes, Figure 33.17 shows that the use of exact-integer capacitor ratios, in which all components were supposed to vary randomly

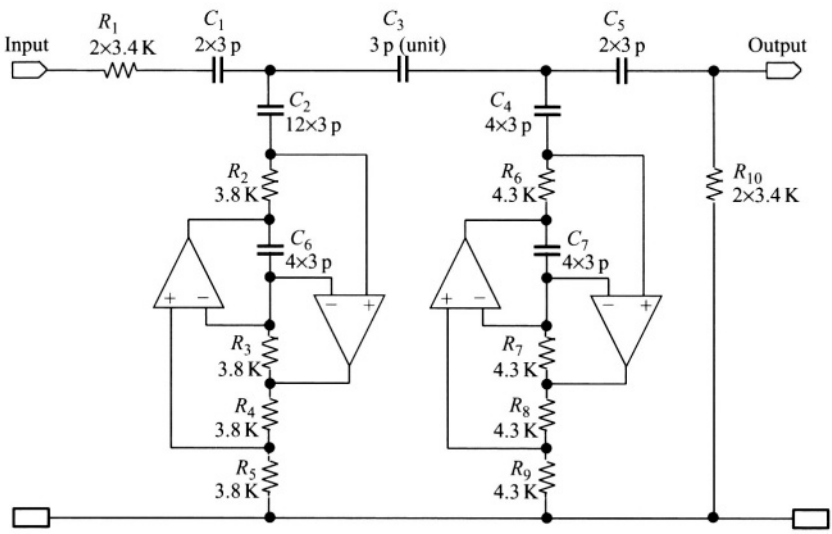


Figure 33.16. A rationalized implementation of the same filter.

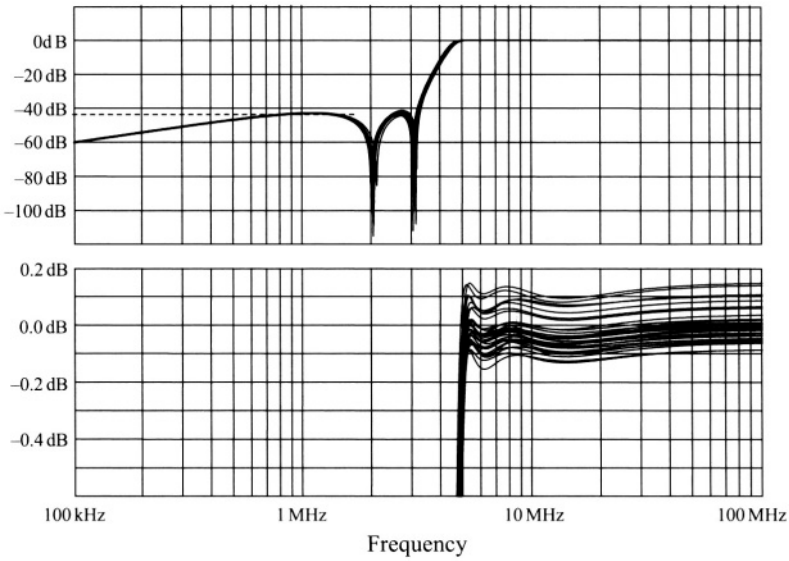


Figure 33.17. Monte-Carlo results for the rationalized filter.

without the benefit of correlation that would in fact be the case, results in very little difference in the response. The important 40 dB stop band is still guaranteed, and there is an interesting bonus: the ripple in the pass band is now halved, being about 0.05 dB. The apparent increase in vertical spread in the pass band gain is an artifact of the small sample size.

This simple example serves to demonstrate the more general point that one can safely depart from rigid synthesis procedures in pursuing the design of a layout that is more robust in manufacture. The practice of *bending the circuit in favor of the layout* is an extremely common one, and frequently entails few, if any, trade-offs. On the contrary, such synergistic give-and-take between circuiteer and layouteer is at the heart of the most successful cooperative developments. Invariably, the circuit design will benefit from numerous subtle refinements, and is only finished when the layout is signed off and taped out.

33.6. Layout of Silicon-on-Insulator Processes

Modern analog bipolar processes make use of SOI technologies, the most common of which employ *bonded wafer* techniques. When two wafers are brought into contact over their entire surfaces, which are always coated with a thin layer of oxide, the two surfaces will form a strong molecular bond, with very little help, usually involving a steam environment. At this point, one has a sandwich comprising two thick slices of pure crystal silicon, between which is

a thin layer of amorphous silicon dioxide. However, unlike earlier techniques for dielectric isolation, these wafers are mechanically robust and easy to handle.

One of the silicon wafers (in some cases, it may be doped to a different resistivity) is then mechanically ground and polished to a uniform thickness of only a few microns. This becomes the crystalline surface on which further layers may be grown by epitaxy, and subsequently doped using all of the standard production methods. Both NPN and PNP transistors can be made in this way, and the techniques are generally compatible with other IC processes such as CMOS, SiGe and BiCMOS technologies. The isolation between devices is now achieved by etching trenches through this relatively thin *primary oxide* and then backfilling to provide the required planarity for subsequent metalization of the devices. This fabrication technique has many outstanding advantages over junction isolation, and some minor disadvantages. The layout methods differ in certain crucial ways.

Here, the concept of a "substrate" involves essentially the notion of a *mechanical handle,* during wafer processing, that will later provide the physical attachment to the paddle in the package. There is no longer a galvanic connection between this layer and the devices on the upper layer. All the transistors are now true *three-terminal* devices, the only caveat being that there remains a small C_{JS} from the collectors to the handle.[10] But unlike a junction-isolated transistor, where the C_{JS} varies with the collector–substrate bias (in other words, it is an unwelcome *varactor* diode) the C_{JS} of a bonded wafer transistor is constant, thus eliminating an important source of HF nonlinearity. It is also smaller than for a junction-isolated transistor having similar internal geometry, for two reasons. First, the use of trench isolation greatly reduces the *total area* of the collector region, compared to that of a junction-isolated transistor, where a large spacing is required around the base to accommodate the collector–substrate depletion layer. Second, the *specific capacitance* of the sub-collector oxide (i.e. the primary oxide of the bonded wafer structure) is much smaller than for a junction.

In a three-terminal SOI transistor, there is no leakage current to the substrate. This is valuable in micropower circuit design, particularly at high temperatures. There is also no possibility of latch-up at the *device* and *layout* level. (A poorly designed *circuit* may still exhibit latch-up for quite different reasons; this can be completely captured in simulation studies, unlike the layout-level latch-up described earlier.) For similar reasons, the possibility of the transport of "stray carriers" across the isolation boundaries is eliminated. Finally, SOI allows

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[10] Due to the construction of the *vertical PNP* transistors, this is also a true for them. This differs from the *lateral PNP* in a standard BJT process, where its *base,* the N-epi layer, has a capacitance to substrate.

bipolar transistors to be used as series-pass switches in certain situations: the base must be driven by sufficient current to support the emitter–collector current, but the sum of all the currents is now fully defined, since there is no current to the substrate.

While the lower side of the die is electrically connected to the paddle, and thus to a defined potential, this connection only plays a role in HF operation, since it is the "sink" into which all the C_{JS} currents flow. Accordingly, it is still very important that the impedance from the paddle to the external ground (the elusive "Ø" node) be minimized. However, on the upper side of the die there will be regions where the thin, starting layer of silicon is unused. This is called the "Region Outside the Trenches" (ROTT). It is highly desirable, although not inherently essential, that these regions also be connected to a known potential. Since there is no junction associated with them (they are sandwiched between the primary oxide and the field oxide) it generally does not matter what this potential is, although certain preferences will be applied within a particular company. Figure 33.18 shows in simplified form the cross-section of an NPN transistor on SOI. There is no intention here to represent a real structure, but only to illustrate its key ideas.

There are two disadvantages to SOI processes. The first is the obvious one of wafer cost: the starting material is greater than that of a simple wafer, and the full production cost is higher because these processes are also quite sophisticated in other ways, and involve numerous advanced fabrication steps to support thin-film laser-trimmable silicon–chromium resistors (of either 100 Ω/square

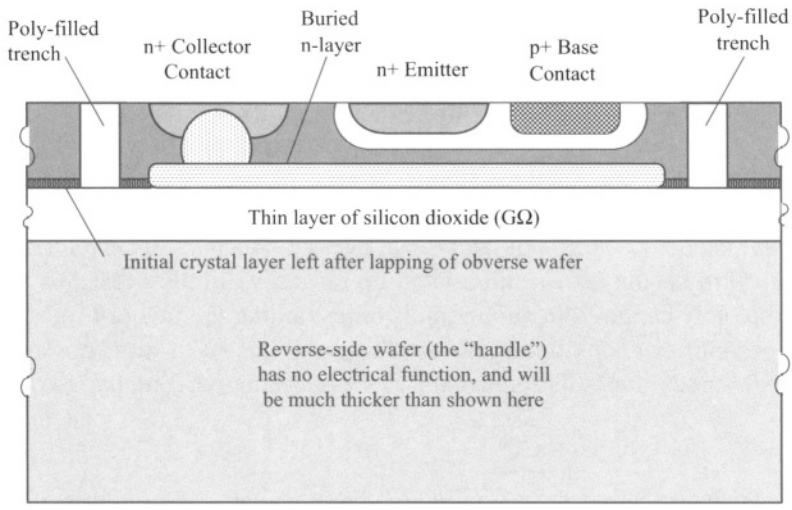


Figure 33.18. Cross-section of a generic SOI BJT.

or 1 kΩ/square), MOMCAPs, Schottky diodes and other special elements such as junction-FETs and buried zener diodes for high-accuracy voltage references. However, although expensive, these processes are immensely versatile. The second disadvantage of SOI touches more directly on layout methodologies, and this is the matter of thermal resistance. Silicon is a pretty good heat conductor; in fact, it has the highest thermal conductivity of all common semiconductors (145 μW/μm-°C at 27°C, which is about 60% that of aluminum), while silicon oxide is a much poorer conductor, by a factor of a hundred (1.4 μW/μm-°C). There are several consequences of this.

The first is that power dissipated in a transistor (or other oxide-isolated device, such as thin-film or poly resistors) encounters a higher thermal resistance, and this results in a higher operating temperature. Alternatively stated, the power that may be dissipated in a given sized SOI transistor is lower, compared to a junction-isolated device. This factor is not quite as large as the Si/SiO_2 ratio of thermal conductivities, because the sub-collector oxide is relatively thin and comprises only a part of the total thermal path. Nevertheless, it is not uncommon to encounter values of thermal resistance for a minimum-geometry device as high as 10,000°C/W or even more.

The second disadvantage is related: any change in power/temperature will dynamically affect several BJT parameters, most importantly, its $I_S(T)$ and V_{BE}. This change will occur over a period of time dictated by the thermal resistance and thermal mass of the intrinsic transistor. The effects on circuit behavior can be readily predicted, and a fully simulated SOI circuit will include the appropriate thermal modeling provided in both the model equations and the parameters database.

Figure 33.19 shows a simple way to model a "Hot BJT" in SPICE. The total device voltage is V_{CE}, measured between the collector and emitter nodes, and the total current is taken as that in the emitter I_E. These two quantities are multiplied using the nonlinear poly(2) element, which is scaled to generate an output current scaled 1 A/W of transistor power $P_O = I_E V_{CE}$ at the (dynamically varying) operating point. This current is then applied to a resistor R_{TH} representing the thermal resistance of the transistor in parallel with a capacitor C_{TH} representing the thermal mass. The resulting voltage can be then used to modulate device parameters. In the primitive model shown in the figure, only the base–emitter voltage is altered. The thermal time-constant $R_{TH}C_{TH}$ is essentially independent of device area, and is about 2.5 ms for a typical high-speed complementary-bipolar process, which corresponds to a corner frequency of 60 kHz.

The thermal resistance, on the other hand, scales in roughly inverse proportion to device area. In a fully embedded thermal modeling algorithm, this is determined automatically from the transistor size attributes and the same database as used to model the electrical parameters. Furthermore, all these

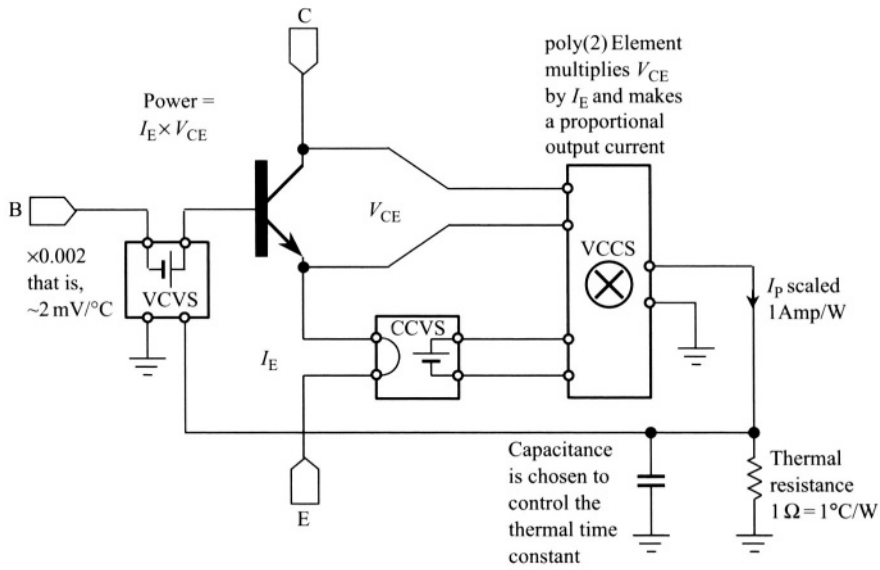


Figure 33.19. The "Hot BJT".

parameters are modulated, using the individual device operating temperature $T_O = T_A + P_O R_{TH}$. This can be also written as $T_O = T_A(1 + P_O/P_A?)$, where PA is the ratio T_A/R_{TH}, and can be viewed as the "reference power" for a given device. A typical value for P_A is 250 mW, using a measured thermal resistance of 1,200 K/W for a transistor having a single $20 \times 0.8\,\mu m^2$ emitter. A minimum geometry transistor in the same IC process has a thermal resistance of about 13,600 K/W and thus $P_A \approx 22\,mW$.

33.6.1. Consequences of High Thermal Resistance

The "Hot BJT" quickly reveals the dramatic and far-reaching consequences of a high thermal resistance. Both the magnitude and the duration of these effects will be very much greater than for a junction-isolated process, which raises a basic trade-off, namely, the need to use generously proportioned devices. The thermal coupling between one SOI device and another will sometimes be weakened by the presence of an oxide-filled trench, compared to that between transistors separated by a doped-silicon isolation barrier between the devices.[11] This can occasionally be good news where one wishes to isolate

[11] But this is not always true: the larger spacings needed in a junction-isolated process may raise the device-to-device thermal resistance to values higher than encountered between oxide-walled transistors. All modern IC processes suffer from the same basic problems caused by the extremely high power densities.

certain cells from other heat-generating ones, but it is more often bad news when attempting to preserve isothermal operation. Considerations of this sort impact many of the special layout trade-offs for SOI.

For example, when a transistor is driven with *a fixed* base–emitter voltage V_{BE} and fixed collector–emitter voltage V_{CE}, the V_{BE} required to support a nominal collector current of I_C declines as the device heats, which raises I_C further. This is the well-known condition of thermal runaway, a phenomenon once of interest only in high-power amplifiers. However, with the extraordinarily large values of thermal resistance encountered in contemporary SOI processes, there is a clear risk that this may occur at very much smaller power levels. It is easily shown that runaway will occur when a critical value of collector current is reached, at about $I_{CRIT} = V_{T0}P_A/\{V_{CE}(E_{GE} - V_{BE0})\}$. Thus, with $V_{T0} = 26\,\text{mV}$, $P_A = 0.25\,\text{W}$, $V_C = 3\,\text{V}$, $E_{GE} = 1.2\,\text{V}$ and $V_{BE0} = 0.73\,\text{V}$, I_{CRIT} is about 5 mA. Stated differently, the transconductance would tend to infinity at this current. In view of the fact that many analog circuits depend on transconductances that are not only well behaved, but very precise, there is ample reason to wonder whether these cells are even viable when implemented in SOI processes.

33.7. Reflections on Superintegrated Layout

It has been noted in that traditional analog monolithic design is based on three rock-solid assumptions: (1) Like devices match very closely; (2) All devices are at the same temperature; (3) The BJT is translinear, that is, its transconductance is a linear function of its collector current, and is reliably equal to qI_C/kT. Alas, modern emitters with areas that are often less than $1\,\mu\text{m}^2$ match poorly; even adjacent transistors on an SOI process are not at the same temperature; and the poly contacts used to access the active emitter generate such high resistance that accurate translinear operation is seriously jeopardized.

Thus, we have arrived at a new juncture, where none of the old rules can be relied on. There are ways of addressing these problems, but they unquestionably pose frustrating trade-offs. Thus, the matching imperative can be addressed by using larger emitters than "intended" by the process developers (and who may balk at the use of wider-than-minimum emitters), as well as by special attention to device structure and orientation. The larger emitters also bring down the emitter resistance. But the price one pays for these measures is a considerable increase in inertia and, of course, less efficient use of die area.

Isothermal operation, or a close approximation, can be restored in a number of ways. Clearly, operating at lower currents and voltages is one possibility; but that is not always permissible. Low currents raise the voltage shot-noise density at the emitter–base port, while low voltages further impact high-frequency

performance. A second approach comes at the circuit level, where judicious choices of cell topology can significantly reduce thermal distortion effects, even when temperature fluctuations of several tens of degrees may occur with signal swings. A third possibility is to look for circuit forms in which transistors share common collector regions. While obviously not a general solution, there is room for innovation in this regard. Indeed, superintegrated circuits of several kinds have been described in which dozens of circuit elements (NPN and lateral PNP transistors, and resistors) share a single pocket. An example is shown in Figures 33.20 and 33.21.

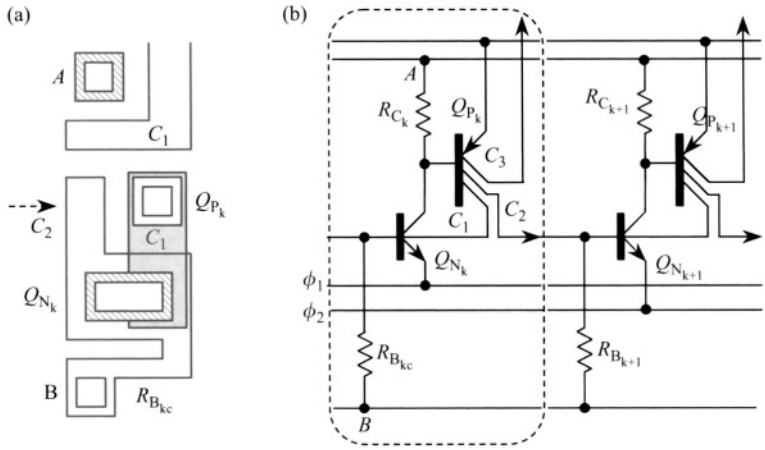


Figure 33.20. A superintegrated counter cell, *c.* 1969.

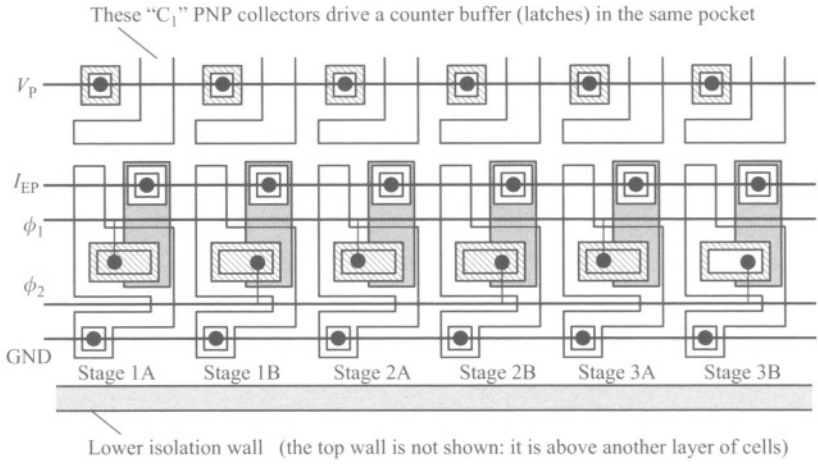


Figure 33.21. Six half-stages of the superintegrated counter.

Here, a decade ring counter is being realized using twenty of the cells shown in the first of these figures. Each cell consists of an NPN transistor, Q_N, whose base region also forms the base resistor R_B, and further acts as the collector C_1 for the lateral PNP, Q_P, as well as collector C_2 for the corresponding PNP in the preceding cell to the left. A third collector region C_3 is placed along the top edge of the PNP emitter, which drives a count buffer (ten latch cells, not shown in these figures). The second figure shows how these are combined. The counter state is advanced a half-step by alternating the NPN emitter currents, ϕ_1 and ϕ_2; at each transition the state is forced to move one step to the right (the ring is completed by a metal feedback path). The count value is latched into the buffer when its NPN emitter is turned on, and thereafter holds at the corresponding stage as the lower counter "circuit" (shown) continues to operate normally.

What is especially noteworthy about this structure is that not only are all elements of each cell merged into a common N-type collector pocket, but all twenty counter stages and the ten buffer latches *are merged into one and the same pocket.* In this example, sixty bipolar transistors and sixty diffused resistors are realized in a single common collector region. Operation is extremely robust and these cells are highly manufacturable.[12]

Subsequent to the development of these merged-logic cells, integrated-injection logic (I^2L) was invented. The ultimate failure of this technology, which pre-dated CMOS logic by many years, was not a reflection of the inadequacies of superintegration as much as of the limitations of I^2L as a sufficiently versatile logic medium for VLSI. However, the problems introduced in recent years by the high thermal resistance of SOI processes and the escalating power densities have generated new interest in what such common-collector layout techniques might offer. There is clearly much room for innovation in this respect, and already some leading-edge products are beginning to draw again on the concept of merged analog cells. Even though the use of superintegration techniques make simulation studies harder (it requires the use of large numbers of discretized sub-cells), and hopelessly confuses layout verification programs – two obvious trade-offs – it may be time to reconsider their benefits.

If that should happen to any significant extent, we would truly be able to assert that there is no line to be drawn in the sand between circuit design and layout design. On the other hand, it is already safe to say that about the current status of analog integrated circuit development.

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[12] Such superintegrated ring (STRING) counters were used in the 7000-Series of Tektronix lab scopes for about twenty years, and large ensembles of them consistently produced high manufacturing yields.

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