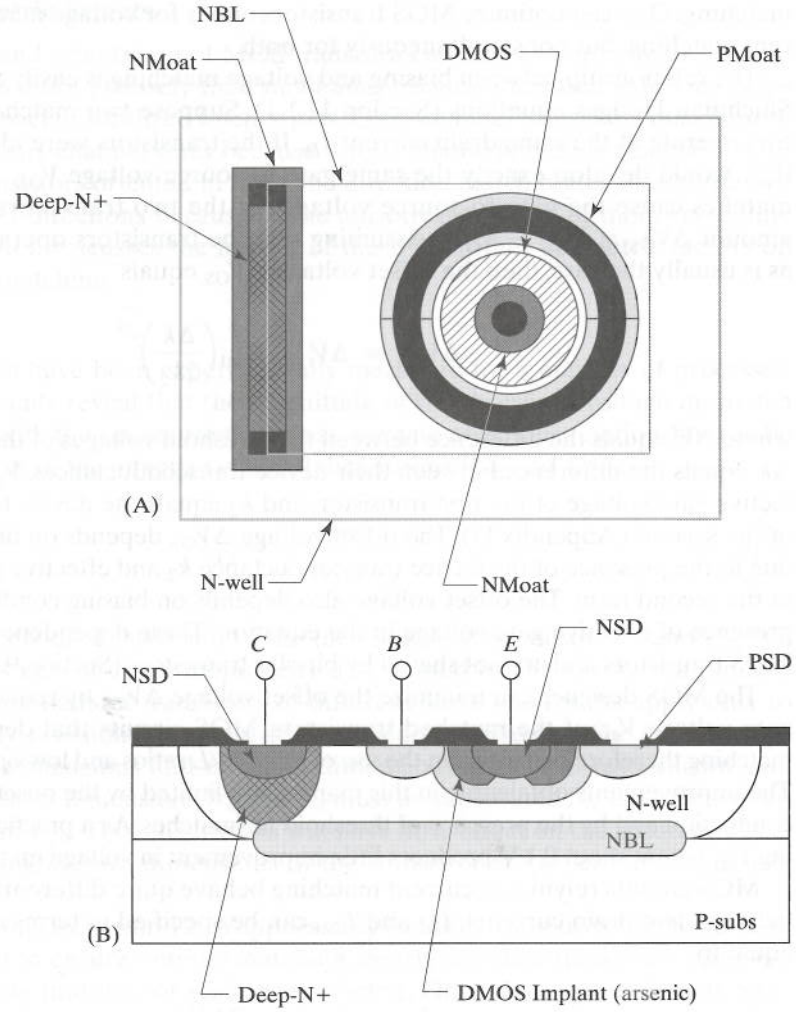

FIGURE 12.27 Layout and cross section of a DMOS NPN (omitting poly field plate).

The structure in Figure 12.27 omits the moat geometry normally covering the DMOS implant, and allows thick-field oxide to grow over it. Dopant segregation and oxidation-enhanced diffusion drive the arsenic emitter deeper into the boron base, reducing the base width of the transistor. Conducting a field oxidation over the DMOS implant thus increases the beta of the DMOS NPN.

All DMOS NPN transistors contain a parasitic DMOS transistor connected between collector and emitter. The structure in Figure 12.27 does not show the poly gate electrode required to suppress this parasitic device. The poly electrode, or *field plate,* must cover the exposed boron DMOS implant with sufficient overlap to allow for misalignment. This field plate is usually connected to the emitter, since this connection shorts the gate and source of the parasitic DMOS.

12.3 MOS TRANSISTOR MATCHING

A wide variety of analog circuits use matched MOS transistors. Some circuits, such as differential pairs, rely on matching of gate-to-source voltages, while others, such as current mirrors, rely on matching of drain currents. The biasing conditions required to optimize voltage matching differ from those required to optimize current

matching. One can optimize MOS transistors either for voltage matching or for current matching, but not simultaneously for both.

The relationship between biasing and voltage matching is easily derived from the Shichman-Hodges equations (Section 11.1.1). Suppose two matched MOS transistors operate at the same drain current I_D. If the transistors were ideal devices, then they would develop exactly the same gate-to-source voltage V_{GS}. In practice, mismatches cause the gate-to-source voltages of the two transistors to differ by an amount $\Delta V_{GS} = V_{GS1} - V_{GS2}$. Assuming that the transistors operate in saturation, as is usually the case, then the offset voltage ΔV_{GS} equals

$$\Delta V_{GS} \cong \Delta V_t - V_{gst1}\left(\frac{\Delta k}{2k_2}\right) \qquad [12.14]$$

where ΔV_t equals the difference between the threshold voltages of the two transistors, Δk equals the difference between their device transconductances, V_{gst1} equals the effective gate voltage of the first transistor, and k_2 equals the device transconductance of the second (Appendix D). The offset voltage ΔV_{GS} depends on device dimensions due to the presence of the device transconductance k_2 and effective gate voltage V_{gst1} in the second term. The offset voltage also depends on biasing conditions because of presence of effective gate voltage in the equation. These dependencies are unique to MOS transistors and are not shared by bipolar transistors (Section 9.2).

The MOS designer can minimize the offset voltage ΔV_{GS} by reducing the effective gate voltage V_{gst} of the matched transistors. MOS circuits that depend on voltage matching therefore benefit from the use of large W/L ratios and low operating currents. The improvements obtainable in this manner are limited by the onset of subthreshold conduction and by the presence of threshold mismatches. As a practical matter, reducing V_{gst} below about 0.1 V produces little improvement in voltage matching.

MOS circuits relying on current matching behave quite differently. The mismatch between two drain currents, I_{D1} and I_{D2}, can be specified in terms of a ratio I_{D2}/I_{D1} equal to

$$\frac{I_{D2}}{I_{D1}} \cong \frac{k_2}{k_1}\left(1 + \frac{2\Delta V_t}{V_{gst1}}\right) \qquad [12.15]$$

The mismatch in drain currents actually increases at low effective gate voltages due to a larger contribution from the threshold mismatch ΔV_t (Appendix D). MOS circuits relying on current matching should operate at reasonably large effective gate voltages to avoid exacerbating threshold voltage variations. The optimal value of V_{gst} depends on many factors and is difficult to quantify. As a practical matter, one should endeavor to maintain a nominal V_{gst} of at least 0.3 V (and preferably 0.5 V) in MOS transistors generating matched currents. Larger effective gate voltages may provide some additional benefit, but most applications cannot spare the headroom to support a higher V_{gst}.

In summary, MOS circuits that generate matched voltages should operate at low effective gate voltages, while MOS circuits that generate matched currents should operate at high effective gate voltages. For most purposes, a nominal V_{gst} of 0.1 V or less will suffice for voltage matching, and a nominal V_{gst} of 0.3 V or more will suffice for current matching. Assuming that the circuit designer adjusts the biasing of the transistors to these values, the matching now depends almost entirely on the care taken in transistor layout. The next three sections discuss layout considerations that affect MOS matching.

12.3.1. Geometric Effects

The size, shape, and orientation of MOS transistors all affect their matching. Large transistors match more precisely than small ones because increased gate area helps minimize the impact of localized fluctuations. Long-channel transistors match more precisely than short-channel ones because longer channels reduce channel-length modulation. Transistors oriented in the same direction match better than those oriented in different directions because of the anisotropic nature of monocrystalline silicon. This section discusses the impact of these and other geometric factors on MOS transistor matching.

Gate Area

MOS mismatches have been experimentally measured for a number of processes. These measurements reveal that the magnitude of the threshold voltage mismatch varies inversely with the square root of the active gate area. This relationship can be expressed in terms of the effective channel dimensions W_{eff} and L_{eff} as

$$S_{V_t} = \frac{C_{V_t}}{\sqrt{W_{\text{eff}} L_{\text{eff}}}} \qquad [12.16]$$

where s_{V_t} is the standard deviation of the threshold voltage mismatch and C_{V_t} is a constant.[18] The value of C_{V_t} is empirically determined by measuring the random mismatch between pairs of transistors of different sizes. The results apply only to transistors closely resembling the test devices used to derive C_{V_t}. The relationships between drawn dimensions and effective dimensions are not always known, and sometimes the drawn dimensions W_d and L_d must be substituted for the effective dimensions W_{eff} and L_{eff}. This substitution will have little effect on the accuracy of the predictions as long as both dimensions of the transistor are several times greater than minimum.[19]

Strictly speaking, Equation 12.16 applies only to MOS transistors that have been carefully laid out to ensure optimal matching. Poorly matched transistors often exhibit gross defects that do not scale as predicted. Once these gross defects have been eliminated, the residual threshold mismatches usually follow Equation 12.16 quite precisely. Theoretical studies suggest that residual threshold mismatches stem mostly from statistical fluctuations in the distribution of backgate dopants.[20] Statistical fluctuations in the distribution of fixed oxide charge may also play a minor role.

Random short-range variations also appear to determine the residual transconductance mismatches observed between well-matched devices. If the transconductance mismatch is described as a normalized ratio s_k/k, then it varies with the effective dimensions, W_{eff} and L_{eff}, as

$$\frac{s_k}{k} = \frac{C_k}{\sqrt{W_{\text{eff}} L_{\text{eff}}}} \qquad [12.17]$$

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[18] K. R. Lakshmikumar, R. A. Hadaway, and M. A. Copeland, "Characterization and Modeling of Mismatch in MOS Transistors for Precision Analog Design," *IEEE J. Solid-State Circuits*, SC-21, #6, 1986, pp. 1057–1066.

[19] Substituting drawn for effective dimensions will have very grave effects if either the width or the length of the matched devices is small; see S. J. Lovett, M. Welten, A. Mathewson, and B. Mason, "Optimizing MOS Transistor Mismatch," *IEEE J. Solid-State Circuits*, Vol. 33, #1, 1998, pp. 147–150.

[20] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching Properties of MOS Transistors," *IEEE J. Solid-State Circuits*, Vol. SC-24, #5, 1989, pp. 1433–1439. Also see Lakshmikumar, *et al.*, p. 1059.

where C_k is a constant. Possible causes for short-range variations in transconductance include linewidth variation, gate oxide roughness, and statistical variations in mobility. The relative importance of these causes is not known, although several authors have suggested that mobility variations predominate.

Transconductance mismatches can also arise from peripheral variations. These so-called *edge effects* rarely play a significant role in devices with dimensions of 2 μm or more, but they can increase the mismatches between short-channel or narrow-channel transistors. One should generally avoid using matched transistors with minimum dimensions significantly less than 2 μm, but if such devices must be used, then their transconductance mismatch can be accurately computed with the equation

$$\frac{S_k}{k} = \sqrt{\frac{C_k^2}{W_{\text{eff}}L_{\text{eff}}} + \frac{C_{kp1}^2}{W_{\text{eff}}^2 L_{\text{eff}}} + \frac{C_{kp2}^2}{W_{\text{eff}}L_{\text{eff}}^2}} \qquad [12.18]$$

where C_k quantifies the areal-based mismatches, and C_{kp1} and C_{kp2} quantify the peripheral-based mismatches. For devices with relatively large dimensions, Equation 12.18 reduces to the same form as Equation 12.17, and the constant C_k that appears in these two equations is thus the same quantity. A study has shown that edge effects may become significant for devices with a channel length of about one micron.[21]

Gate Oxide Thickness

Transistors with thinner gate oxides generally exhibit better matching than those with thicker gate oxides. In the case of transconductance matching, the critical factor is actually backgate doping, which process designers usually increase for low-voltage thin-oxide devices in order to minimize channel length modulation and retard device punchthrough. A higher backgate doping concentration reduces variations caused by the random scattering of dopant atoms throughout the backgate. However, circuit designers do not always wish to use thin oxide transistors for current matching applications, as their higher transconductances make it more difficult to obtain adequate effective gate voltages without resorting to either excessively narrow or excessively long devices.

Thinner gate oxides benefit threshold voltage matching in several ways. Researchers have shown that the constant C_{Vt} in Equation 12.16 depends upon both oxide thickness t_{ox} and backgate doping N_b:

$$C_{Vt} = at_{\text{ox}}\sqrt{N_b} \qquad [12.19]$$

Here, a is a constant of proportionality. Although the mismatch actually increases with higher backgate doping, the effect of oxide thickness dominates the equation, and V_t mismatch consequently improves as process dimensions shrink.[22] Thinner oxides also provide higher transconductances that decrease effective threshold voltages. This indirectly improves voltage matching between MOS transistors, as shown by Equation 12.14.

Circuit designers generally favor thin-oxide devices for matching. However, thick-oxide transistors tend to have higher operating voltage ratings than their thin-oxide counterparts. Although cascodes can enable the use of thin-oxide devices at

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[21] J. Bastos, M. Steyaert, R. Roovers, P. Kinget, W. Sansen, B. Graindourze, A. Pergoot, and E. Janssens, "Mismatch characterization of small size MOS transistors," *Proc. IEEE Conf. on Microelectronic Test Structures*, Vol. 8, 1995, pp. 271–276.

[22] M. J. M. Pelgrom, H. P. Tuinhout, and M. Vertregt, "Transistor matching in analog CMOS applications," *Int. Electron Devices Meeting Technical Digest*, 1998, pp. 915–918.

higher voltages, many circuit designers favor the simplicity of designs that employ thick-oxide devices. Thick-oxide transistors are also favored for analog circuitry in advanced submicron processes where the thin-oxide transistors suffer from severe channel length modulation and extremely limited operating voltages.

Channel Length Modulation

Channel length modulation can cause severe mismatches between short-channel transistors operating at different drain-to-source voltages. The systematic mismatch between the transistors is proportional to the difference between their drain-to-source voltages, and inversely proportional to their channel length. Drawn lengths of 10 to 20 μm are generally adequate for noncritical applications such as current distribution networks. Greater precision can be obtained by operating the matched transistors at equal drain-to-source voltages, for example, through the addition of cascodes. MOS designers rarely use source degeneration to combat channel length modulation because the low transconductance of MOS transistors makes it difficult to obtain adequate degeneration without using extremely large resistors.

Orientation

The transconductances of MOS transistors depend on carrier mobilities, and these in turn exhibit orientation-dependent stress sensitivities. MOS transistors oriented along different crystal axes will therefore exhibit different transconductances under stress. Since all packaged devices experience some stress, these mismatches can be avoided only by orienting matched transistors in the same direction. The devices in Figure 12.28A, which are oriented along the same crystal axis, match better than the devices in Figures 12.28B and 12.28C, which are not. Stress-induced mobility variations can induce current matching errors of several percent between rotated devices.[23] The use of tilted wafers may induce current matching errors of as much as 5%.[24]

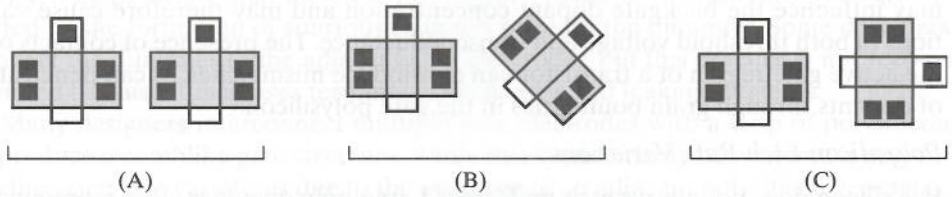

FIGURE 12.28 (A) Devices oriented in the same direction match more precisely than (B,C) those oriented in different directions.

Editing can easily introduce orientation errors if the design has not been properly partitioned. Consider a circuit that contains two matched transistors: M_1, located in cell X_1; and M_2, located in cell X_2. During top-level layout, the designer decides to rotate cell X_1 by 90°. Although this operation seems innocuous, it actually introduces a 90° difference between the orientations of M_1 and M_2. Errors of this sort can be prevented by grouping matched devices together in the same cells. This can sometimes make the schematic more difficult to comprehend, but it greatly reduces the risk of inadvertently introducing matching errors during editing.

MOS transistors that do not self-align must follow very strict orientation rules. Consider the asymmetric extended-drain NMOS transistors, M_1 and M_2, in Figure 12.29A. Each of these transistors is a mirror image of the other. The channel lengths of M_1 and M_2 are both defined by the overhang of their poly gates beyond

[23] Pelgrom, *et al.*, p. 1436.

[24] J. E. Chung, J. Chen, P.-K. Ko, C. Hu, and M. Levi, "The Effects of Low-Angle Off-Axis Substrate Orientation on MOSFET Performance and Reliability," *IEEE Trans. on Electron Devices*, Vol. 38, #3, 1991, pp. 627–633.

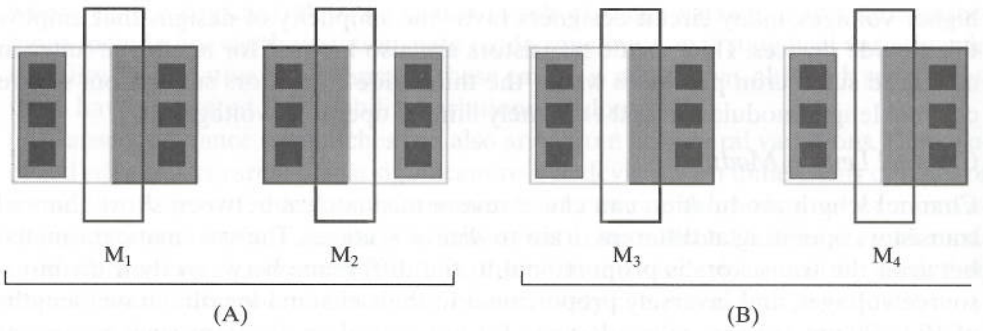

FIGURE 12.29 Extended-drain transistors that are (A) mirror images of each other experience mismatches that do not affect (B) superimposable transistors.

their respective N-well regions. Suppose that photolithographic misalignment causes the poly gates to shift to the right. This misalignment increases the channel length of M_1 and decreases the channel length of M_2. These mismatches are easily eliminated by ensuring that the matched devices are superimposable, as are M_3 and M_4 in Figure 12.29B. Even fully self-aligned transistors may experience slight orientation-dependent mismatches due to diagonal shifting of the source/drain implants (Section 12.3.5).

12.3.2. Diffusion and Etch Effects

The previous section examined sources of mismatch that depended solely upon geometry. Certain other types of mismatch are caused by the presence or absence of other structures near the matched transistors. For example, the presence of poly regions near the gate electrodes can cause slight variations in polysilicon etch rates. These variations produce mismatches in the effective widths and lengths of the matched transistors. Similarly, the placement of other diffusions near the channel may influence the backgate dopant concentration and may therefore cause variations in both threshold voltage and transconductance. The presence of contacts over the active gate region of a transistor can also induce mismatches, as can penetration of dopants through grain boundaries in the gate polysilicon.

Polysilicon Etch Rate Variations

Polysilicon does not always etch uniformly. Large poly openings clear more quickly than small ones because etchant ions have freer access to the sides and bottom of the large opening. The edges of the large opening therefore exhibit some degree of overetching by the time the smaller openings clear. This effect can cause variations in the gate lengths of poly-gate MOS transistors. Consider the layout in Figure 12.30A. The gate of transistor M_2 faces adjacent gates on both sides, but the gates of transistors M_1 and M_3 face an adjacent gate on only one side. The outside edges of the gates of M_1 and M_3 experience more erosion than the corresponding edges of the gate of M_2, so the gate lengths of M_1 and M_3 are slightly shorter than the gate length of M_2.

The etch rate variations experienced by MOS transistors are usually smaller than those experienced by poly resistors (Section 7.2.5), because poly gates do not lie as close together as poly resistor segments do. Many MOS transistors also use relatively long channel lengths. Even so, transistors that must achieve moderate or precise current matching should use dummy gates to ensure uniform etching. Failure to do so may produce current mismatches of 1% or more. Figure 12.30B shows an example of an array of MOS transistors incorporating dummies. Most designers make the dummy gates the same width as the active ones, but this precaution is not strictly necessary because the width of the poly strips is far less significant than their spacing.