7.2 CAUSES OF MISMATCH

Random mismatches stem from microscopic fluctuations in dimensions, dopings, oxide thicknesses, and other parameters that influence component values. Although these statistical fluctuations cannot be entirely eliminated, their impact can be minimized through proper selection of component values and device dimensions. Systematic mismatches stem from process biases, contact resistances, nonuniform current flow, diffusion interactions, mechanical stresses, temperature gradients, and a host of other causes. A major goal of designing matched components consists of rendering them insensitive to various sources of systematic error. The following sections discuss the major known causes of mismatch and techniques for combating them.

7.2.1. Random Statistical Fluctuations

All components exhibit microscopic irregularities, or fluctuations. In the case of a polysilicon resistor, the edges of the poly exhibit microscopic irregularities that give them a slightly ragged appearance. Some of these irregularities stem from the granularity of the polysilicon, while others result from imperfections in the photoresist. The granularity of the polysilicon also causes variations in poly thickness and resistivity. Other types of devices exhibit different types of fluctuations, but all of these fall into one of two categories: fluctuations that occur only along the edges of the device and fluctuations that occur throughout the device. The former are called *peripheral fluctuations* because they scale with device periphery, while the latter are called *areal fluctuations* because they scale with device area. The nature of these scaling relationships can be deduced from statistical arguments.

Consider the case of a pair of matched capacitors, each having capacitance C. The random mismatch due to peripheral and areal fluctuations has a standard deviation s_C, that equals[2,3,4]

$$s_C = \frac{1}{\sqrt{C}}\sqrt{k_a + \frac{k_p}{\sqrt{C}}} \qquad [7.4]$$

where k_a and k_p are constants representing the contributions of areal and peripheral fluctuations, respectively. The contribution of the peripheral term decreases as the capacitance increases. For sufficiently large capacitors, the areal term dominates and the random mismatch becomes inversely proportional to the square root of capacitance. Most practical matched capacitors follow the inverse-square-root relationship fairly closely, so doubling the size of a pair of capacitors decreases their random mismatch by about 30%. The matching of capacitors of different values is dominated by the value of the smaller capacitor, not the larger one. In other words, a 5pF capacitor matches a 50pF capacitor about as well as it matches another 5pF capacitor.

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[2] J. B. Shyu, G. C. Temes, and F. Krummenacher, "Random Error Effects in Matched MOS Capacitors and Current Sources," *IEEE J. Solid-State Circuits,* Vol. SC-19, #6, 1984, pp. 948–956.

[3] J. B. Shyu, G. C. Temes, and K. Yao, "Random Errors in MOS Capacitors," *IEEE J. Solid-State Circuits,* Vol. SC-17, #6, 1982, pp. 1070–1076.

[4] J. L. McCreary, "Matching Properties, and Voltage and Temperature Dependence of MOS Capacitors," *IEEE J. Solid-State Circuits,* Vol. SC-16, #6, 1981, pp. 608–616.

Now consider the case of a pair of matched resistors[5] having width W and resistance R. The random mismatch between these resistors has a standard deviation s_R that equals

$$s_R = \frac{1}{W\sqrt{R}}\sqrt{k_a + \frac{k_p}{W}} \qquad [7.5]$$

where k_a and k_p are constants representing the contributions of areal and peripheral fluctuations, respectively (Appendix D). This equation shows that random mismatches scale inversely with width. Doubling the width of a pair of matched resistors will at least halve their random offset. The mismatches also scale as the square root of resistance, so larger resistors match better than smaller ones. This leads to a very useful generalization concerning the widths of matched resistors. Suppose a resistance, R_1, requires a width, W_1, to obtain a certain degree of matching. The width, W_2, required to obtain the same degree of matching for a resistance R_2 equals the larger of the two following values:

$$W_2 = W_1\sqrt{\frac{R_1}{R_2}} \qquad [7.6A]$$

$$W_2 = W_1\sqrt[3]{\frac{R_1}{R_2}} \qquad [7.6B]$$

Equation 7.6A represents the extreme case where areal fluctuations dominate over peripheral fluctuations, while equation 7.6B represents the opposite extreme. The actual situation lies somewhere between these extremes, although areal effects generally predominate. As long as one takes the larger of the two widths given by the equations, the matching of the new resistor R_2 should always equal or exceed the matching of the original resistor R_1. In the case of matched resistors of different values, the smaller of the two resistances should be used in equations 7.6A and 7.6B.

An example will clarify the use of these equations. Suppose a pair of 6μm-wide 10kΩ resistors have a worst-case random mismatch of ±0.1%. What width is required to obtain the same degree of matching between 100kΩ resistors? Equation 7.6A predicts a minimum width of 1.90μm, while equation 7.6B predicts a minimum width of 2.78μm. The actual width required to obtain this degree of matching therefore lies somewhere between 1.90μm and 2.78μm. A conservative designer would probably make these resistors 3μm wide.

Equations 7.6A and 7.6B only apply to poly resistors in which the resistor is much wider than its largest poly grains. If this condition is not met, then the equations will underestimate the mismatch of the resistors. Most poly grains are less than 1μm across,[6] so matched poly resistors should be made at least 2 to 3μm wide.

N-type poly resistors seem to exhibit larger random mismatches than P-type poly resistors. On one advanced bipolar process, N-doped poly resistors exhibited approximately twice the random mismatch of P-doped poly resistors having similar dimensions and sheet resistance.[7] This effect may stem from dopant segregation

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[5] Resistor matching is also treated in W. A. Lane and G. T. Wrixon, "The Design of Thin-Film Polysilicon Resistors for Analog IC Applications," *IEEE Trans. on Electron Devices*, Vol. 36, #4, 1989, pp. 738–744.

[6] A. C. Adams, "Dielectric and Polysilican Film Deposition," in S. M. Sze, ed., *VLSI Technology*, 2nd ed., (New York: McGraw-Hill, 1983), p. 244.

[7] M. Corsi, private communication, 1998.

at grain boundaries.[8] The exact explanation remains unclear, so it is not certain that P-type poly resistors will always exhibit less random mismatch than N-type poly resistors.

7.2.2. Process Biases

The dimensions of geometries fabricated in silicon never exactly match those in the layout database because the geometries shrink or expand during photolithography, etching, diffusion, and implantation. The difference between the drawn width of a geometry and its actual measured width constitutes the *process bias*. Process biases can introduce major systematic mismatches in poorly designed components. Consider the case of two matched poly resistors having widths of 2μm and 4μm, respectively. Suppose that poly etching introduces a process bias of 0.1μm. The ratio of the actual widths equals (2 + 0.1)/(4 + 0.1), or 0.512. This represents a systematic mismatch of no less than 2.4%! Since most processing steps have biases of at least 0.1μm, the layout designer must ensure that all matched devices are insensitive to process biases. In the case of resistors, process biases can be virtually eliminated by simply making both resistors the same width.

Process biases can also affect the length of a resistor. The length of most resistors is determined by the placement of their contacts. Suppose that these contacts have a process bias of 0.2μm. If one matched resistor was 20μm long and the other was 40μm long, then the mismatch due to this bias would equal (20 + 0.2)/(40 + 0.2), or 0.503. This represents a systematic mismatch of about 0.5%. The simplest way to avoid this bias consists of dividing both matched resistors into segments of the same size. If the resistors of the previous example were laid out in 20μm segments, then the ratio of the resistors would equal (20 + 0.2)/[2·(20 + 0.2)], or exactly 0.5. The same stratagem has already been shown to eliminate systematic mismatches due to contact resistances and nonlinear current flow at the ends of the resistors. Section 7.2.6 explains how to divide matched resistors into arrays of optimally sized segments.

Capacitors also experience systematic mismatches caused by process biases. Suppose a pair of poly-poly capacitors, one measuring 10×10μm and the other 10×20μm, both experience a poly etch bias of 0.1μm. The actual area of the 10×10μm capacitor equals $(10.1)^2$, or 102.1μm^2, while the actual area of the 10×20μm capacitor equals (10.1·20.1), or 203.01μm^2. The ratio of these two areas equals 0.5029, which represents a systematic mismatch of 0.6%.

In theory, matched capacitors become insensitive to process biases when their area-to-periphery ratios equal one another. In the case of two capacitors of the same value, this can be achieved by using the same geometry for both capacitors. Identical matched capacitors are usually laid out as squares because this reduces their area-to-periphery ratio, which in turn minimizes the contribution of peripheral fluctuations to their random mismatch. The problem becomes somewhat more difficult if the capacitors have values that are not in simple ratio. Although the smaller capacitor should still be laid out as a square, the larger capacitor must be laid out as a rectangle. Suppose the smaller capacitor, C_1, has dimensions L_1 by L_1

[8] J. C. C. Tsai, "Diffusion," in S. M. Sze, ed., p. 312.