Chapter 2

Switched-Capacitor Building Blocks

SWITCHED-CAPACITOR circuits are pervasive in highly integrated, mixed-signal applications. This chapter describes the basic building blocks that comprise these circuits. These blocks are the sample-and-hold (S/H), gain stage, integrator, comparator. From these elements more complex circuits can be built such as filters, analog-to-digital converters (ADC), and digital-to-analog converters (DAC). All sampled-data circuits, such as these, require a pre-conditioning, continuous-time, anti-alias filter to avoid aliasing distortion. A more detailed discussion of this continuous-time block can be found in [31]. After the theory of operation of each block is described, a brief discussion of practical non-idealities follows. This chapter is not intended as a rigorous and detailed analysis; it is a brief overview. A more rigorous analysis can be found in the references.

2.1 Sample-and-hold (S/H)

The sample-and-hold is the most basic and ubiquitous switched-capacitor building block. Before a signal is processed by a discrete-time system, such as an ADC, it must be sampled and stored. This often greatly relaxes the bandwidth requirements of following circuitry which now can work with a DC voltage. Because the S/H is often the first block in the signal processing chain, the accuracy and speed of entire application cannot exceed that of the S/H.

2.1.1 Top-plate S/H

In CMOS technology, the simplest S/H consists of a MOS switch and a capacitor as shown in figure 2.1. When V_g is high the NMOS transistor acts like a linear resistor, allowing the output V_o to track the input signal V_i. When V_g transitions

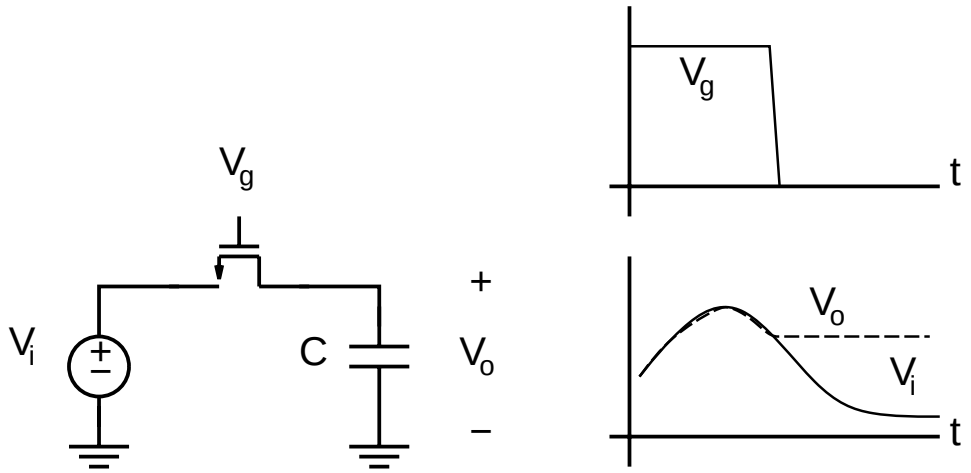

Figure 2.1 MOS sample-and-hold circuit

low, the transistor cuts off isolating the input from the output, and the signal is held on the capacitor at V_o.

There are several practical limitations to this circuit. Because the RC network has finite bandwidth, the output cannot instantaneously track the input when the switch is enabled. Therefore, a short acquisition period must be allocated for this (exponentially decaying) step response. After the S/H has acquired the signal, there will be a tracking error due to the non-zero phase lag and attenuation of the sampling network. The latter linear, low-pass filtering does not introduce distortion and is usually benign for most applications. The on-conductance, however, of the transistor is signal dependent:

$$g_{ds} = \mu C_{ox} \frac{W}{L}(V_g - V_i - V_t) \tag{2.1}$$

Thus the transfer function from input to output can become significantly nonlinear if $(V_g - V_i - V_t)$ is not sufficiently large. A detailed analysis of these dynamic errors can be found in [49].

When the switch turns off, clock feed-through and charge injection introduce error in the output. When the gate signal V_g transitions from high to low, this step AC couples to the output V_o via parasitic capacitances, such as C_{gs} and C_{gd}. Be-

cause the output is a high impedance node, there is no way to restore the DC level. This coupling is called clock feed-through. This error is usually not a performance limitation because it is signal-independent and therefore only introduces an offset and not distortion. To first order this error can be eliminated using a differential configuration. Charge injection, however, is a signal-dependent error. When switch is turned off quickly, the charge in the channel of the transistor is forced into the drain and source, resulting in an error voltage. The charge in the channel is approximately given by equation 2.2. Because q is signal dependent, it represents a gain error in the S/H output. There have been several efforts to accurately characterize this error [49, 69, 76, 77].

$$q = WLC_{ox}(V_g - V_i - V_t) \tag{2.2}$$

This circuit is also sensitive to parasitic capacitance. Any parasitic capacitance at the output change the amount of signal charge sampled, which is often the critical quantity in switched-capacitor circuits. Bottom-plate sampling can greatly reduce these errors.

The channel resistance of the switch contributes thermal noise to the output. This random error sets an upper bound on the signal-to-noise ratio (SNR). If the wide-band thermal noise is integrated over all frequencies, the resulting variance in the output voltage is only dependent on the sampling capacitance C [15].

$$\overline{v_o^2} = \frac{kT}{C} \tag{2.3}$$

Jitter in the sampling clock or aperture error also introduces a random error component to the output. If the sampling edge has an variance in time of σ_t^2, the worst case voltage variance while sampling a sine wave $V_i = \hat{V}\sin(\omega t)$ is [45] is

$$\overline{v_o^2} \leq (\hat{V}\omega)\sigma_t^2. \tag{2.4}$$

2.1.2 Bottom-plate S/H

A technique called bottom-plate sampling to first order eliminates some of the errors in the top-plate S/H circuit. Figure 2.2 shows the bottom-plate sampling configuration. While clocks ϕ' and ϕ are high, V_o tracks the input voltage V_i. When clock ϕ' transitions from high to low, switch M2 turns off, and the charge on node x is trapped. Because charge is conserved, the charge on capacitor C is now fixed $q = CV_i$. This is the defines sampling instant. When clock ϕ transitions from high to low, switch M1 is turned off and the output is isolated from the input.

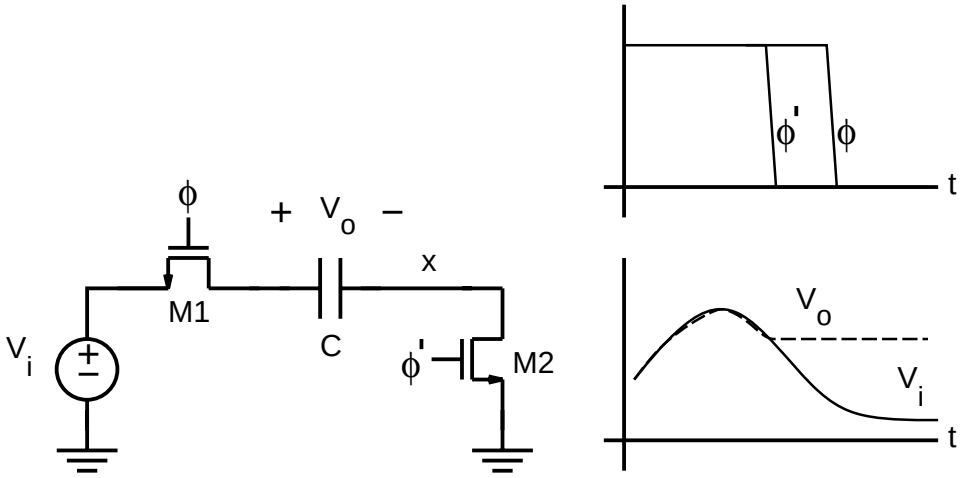

Figure 2.2 Bottom-plate sample-and-hold circuit

When M2 turns off, the voltage at node x is perturbed due to clock feed through and charge injection. In this case, however, the charge injection is signal-*independent* because drain and source see a fixed potential (ground). To first order this eliminates signal-dependent charge injection distortion. The remaining offset can be further rejected with a differential configuration. The charge injection from M1 does not alter the charge stored on capacitor C due to charge conservation.

Figure 2.3 shows a practical implementation of bottom-plate sampling in a differential configuration. This circuit uses a two-phase, non-overlapping clock. During phase ϕ_1 the input V_i is sampled differentially onto C_p and C_n as described

above. During phase ϕ_2 the opamp is put into a unity gain configuration. This drives $(V_{xp} - V_{xn}) \rightarrow 0$. Due to conservation of charge, the sampled input appears at the opamp output $V_o = V_i(\mathrm{sampled})$. Because the summing nodes of the opamp are driven to the same potential, no differential signal charge is stored on parasitic capacitance at the opamp input. Furthermore, the opamp provides a low-impedance output for driving any following signal processing blocks.

Although the opamp greatly improves the performance of the S/H circuit, it adds substantial complexity to its design. Any offset in the opamp will appear directly at the output in this configuration. For CMOS technologies this offset can be in the range of 10-50mV typically. For offset sensitive applications, there are several auto-zeroing techniques applicable to switched-capacitor circuits [24].

The finite DC gain of the opamp introduces a fixed gain error:

$$f = \frac{C}{C + C_{ip}} \tag{2.5}$$

$$V_o = \frac{a}{1 + af} \tag{2.6}$$

$$= \frac{1}{f}\frac{1}{1 + \frac{1}{af}} \tag{2.7}$$

$$\approx (1 + \frac{C}{C_{ip}})(1 - \frac{1}{af}) \tag{2.8}$$

$$\tag{2.9}$$

Where a is the DC opamp gain, f is the feedback factor, $C = C_p = C_n$, C_{ip} is the opamp input capacitance. This fixed error does not introduce distortion and is usually benign.

The finite bandwidth of the opamp limits the clock frequency of this circuit. The clock period must be sufficiently long to allow the desired level of settling accuracy at the opamp output. Typically the bias currents in the opamp can be increased to increase the opamp bandwidth at the expense of increased power consumption.

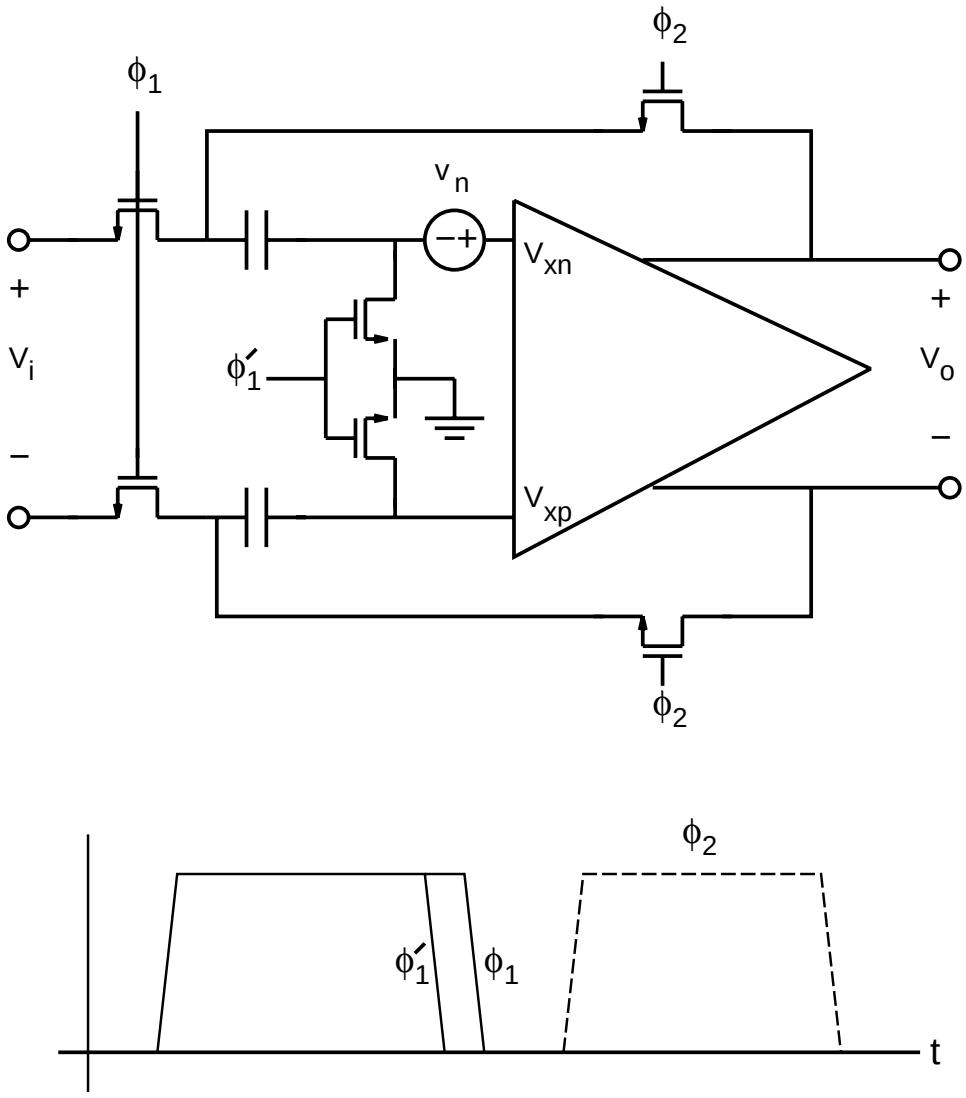

Figure 2.3 Practical fully differential sample-and-hold circuit

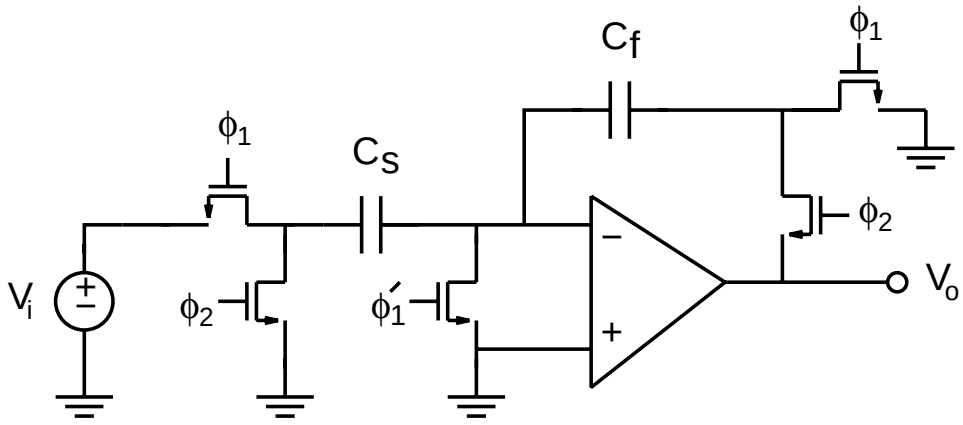

Figure 2.4 Single-ended gain stage

In addition to the fundamental kT/C sampling noise, the opamp will add thermal noise due to active elements. If the noise in the opamp can be represented as a single input-referred source v_n as shown in figure 2.3, the total output-referred noise will be:

$$\overline{v_o^2} = 2\frac{kT}{C} + \overline{v_n^2} \tag{2.10}$$

2.2 Gain stage

The sample-and-hold circuit shown in figure 2.3 can be modified to provide both gain and sample-and-hold functions. This operation is common in pipeline analog-to-digital converters (section 3.3) and filters (section 3.1). Figure 2.4 shows a gain stage that samples the input, applies gain, and holds the output value. A single-ended version is shown for simplicity, but the following analysis applies to a differential version which is most commonly used in practice.

To better understand the operation of this circuit, figures 2.2a and 2.2b show the states of the switches during phase 1 and phase 2 respectively. During phase 1 (figure 2.2a), the input V_i is sampled across C_s. The opamp is not used during this phase, and this time can be used to perform auxiliary tasks such as resetting common-mode feedback (section 5.3.8). The charge q is:

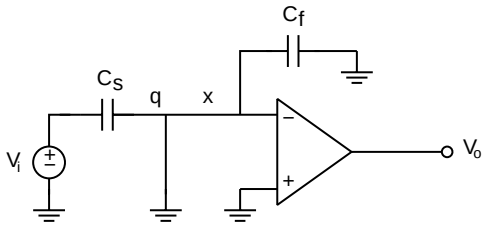

Figure 2.2a: Phase 1

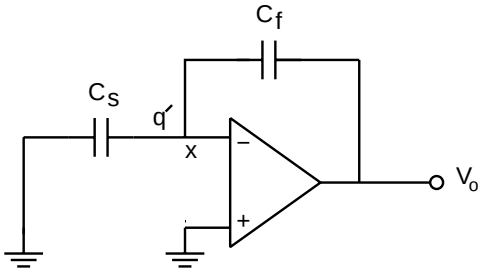

Figure 2.2b: Phase 2

$$q = C_s(0 - V_i) = -C_s V_i \tag{2.11}$$

Notice there is no charge stored on C_f since both sides are grounded. Bottom-plate sampling is employed, and the sampling instant is defined by ϕ_1' as before. During phase 2 (figure 2.2b), the opamp is put in a negative feedback configuration, forcing node x to zero (virtual ground). Because the input is also ground, there is no charge storage on C_s, and all the charge is transferred to C_f. Thus, a *voltage* gain of C_s/C_f is achieved. Analytically, charge on node x is conserved, so $q = q'$:

$$q = q' \tag{2.12}$$

$$-C_s V_i = C_f(0 - V_o) \tag{2.13}$$

$$\frac{V_o}{V_i} = \frac{C_s}{C_f} \tag{2.14}$$

If we consider the input V_i as a discrete-time sequence $V_i(n) = V_i(nT)$, where T is the sampling period, then the output is

$$V_o(n) = \frac{C_s}{C_f} V_i(n-1). \tag{2.15}$$

This equation reflects the one period latency of this discrete-time circuit.

Because this circuit incorporates an opamp, it has the same limitations as the sample-and-hold circuit in figure 2.3. In addition, the exact gain of the stage is de-

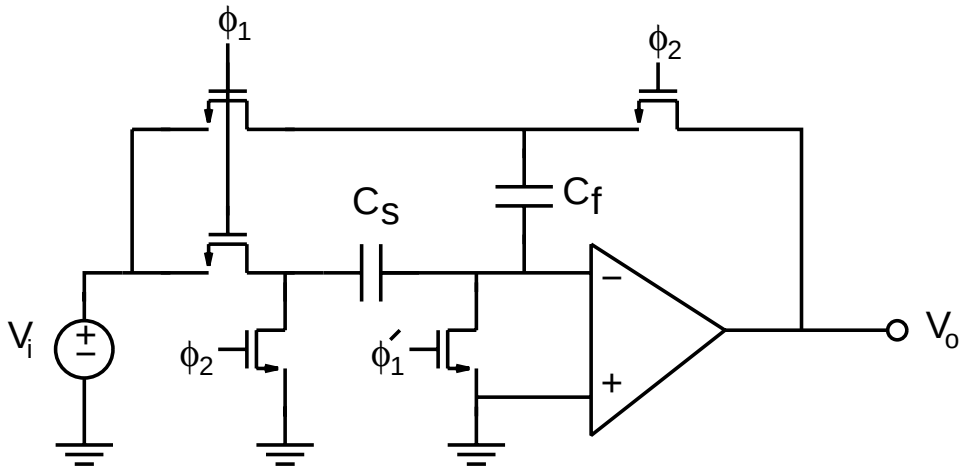

Figure 2.5 Improved settling speed gain stage

pendent on the capacitor matching of C_s and C_f. For example if $C_s = C_f + \Delta C$ then:

$$V_o(n) = \frac{C_s}{C_f} V_i(n-1) + \frac{\Delta C}{C_f} V_i(n-1) \tag{2.16}$$

In high-resolution applications, the second term can represent a significant error. Similarly if the capacitors have a voltage-dependent value, the gain will be distorted (section 6.4.2).

Figure 2.5 shows another gain stage configuration that uses both the feedback (C_f) and sampling (C_s) capacitors to sample the input. This configuration has the advantage that the opamp settling is inherently faster for a given stage gain [46] due a larger feedback factor.

The transfer function of this stage is:

$$V_o(n) = \left(1 + \frac{C_s}{C_f}\right) V_i(n-1) \tag{2.17}$$

Notice the gain is larger for the same capacitor loading. This effect can be significant for low-gain stages of 2 or 3 for example.

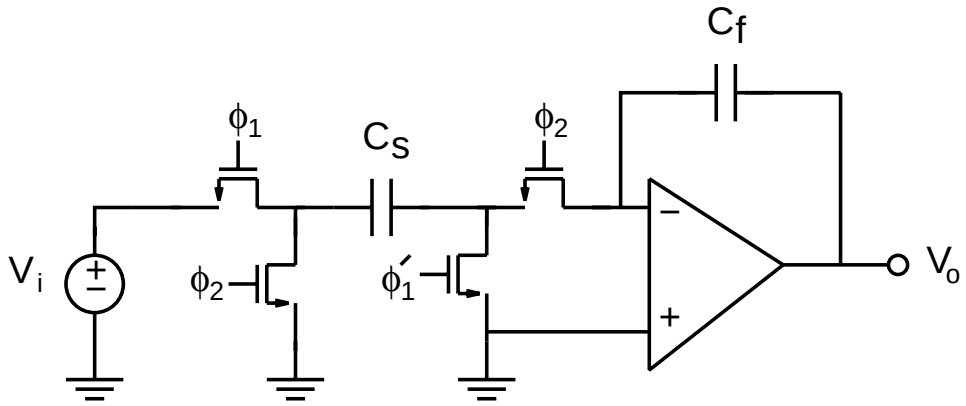

Figure 2.6 Switched-capacitor integrator

2.3 Integrator

Another modification of the basic sample-and-hold circuit yields a switched-capacitor integrator. Integrators are used throughout switched-capacitor filters (section 3.1) and sigma-delta modulators (section 3.2). Figure 2.6 shows a switched-capacitor integrator. For simplicity the single-ended version is shown, but these results apply to a differential implementation as well.

The same analysis used for the gain stage (above) can be used for the integrator. Unlike the gain stage, the feedback capacitor C_f is not reset each cycle. Therefore, C_f accumulates previous sampled values:

$$V_o(n) = V_o(n-1) + \frac{C_s}{C_f} V_i(n-1) \tag{2.18}$$

The integrator has the same performance limitations as the gain stage.

2.4 Comparator

Comparators are not strictly considered switched-capacitor elements. They, however, often employ switched-capacitor techniques and are used in switched-capacitor applications such as pipeline analog-to-digital converters and sigma-delta analog-to-digital converters. Figure 2.7 shows a comparator suitable for use in a two-phase, switched-capacitor circuit. For simplicity, a single-ended version is shown,

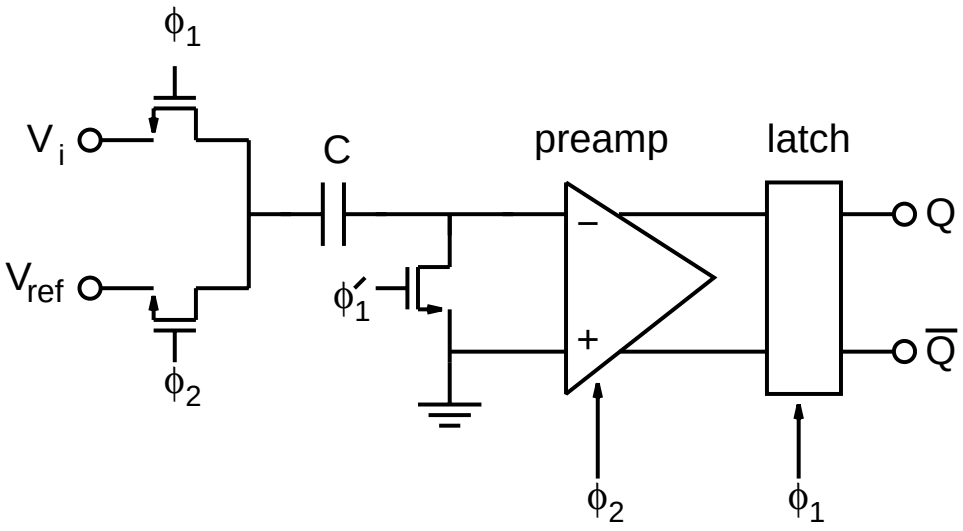

Figure 2.7 Switched-capacitor comparator

but this circuit can be extended to a fully differential implementation.

During phase 1 the input signal V_i is sampled across capacitor C. Again, bottom plate sampling is employed using the early clock phase ϕ_1'. During phase 2, the reference voltage V_{ref} is applied to the left side of the capacitor. The voltage difference $(V_{ref} - V_i)$ appears at the input of the pre-amplifier. The pre-amplifier amplifies this difference and applies it to the input of a regenerative latch. At the end of phase 2 the pre-amplifier outputs are disconnected from the input. At the beginning of phase 1 of the next cycle, the latch is strobed, creating digital logic levels at the output.

Any offset voltage of the pre-amplifier is directly referred to the input of the comparator. The potentially large offset of the latch is divided by the small-signal gain of the pre-amplifier when referred to the input. Multiple pre-amplifiers can be cascaded to further reduce the effective latch offset at the expense of power consumption. If a low offset is required, auto-zero techniques can be employed in the pre-amplifier(s) [3, 65, 22, 66].

The speed of the comparator is determined by the regenerative time constant of the latch. Consider the representative latch shown in figure 2.8. It consists of two inverters or amplifiers in a positive feedback loop, which are capable of

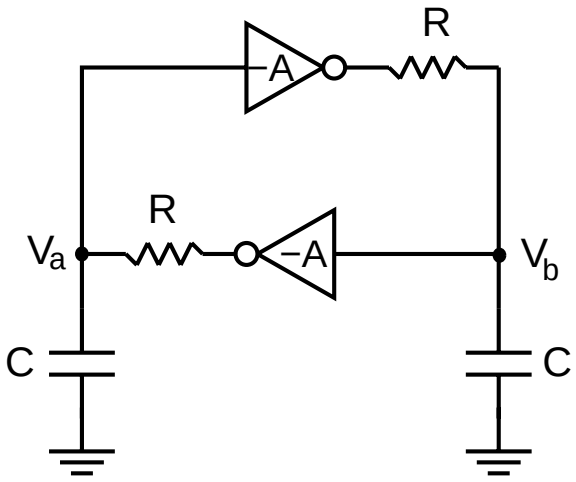

Figure 2.8 Regenerative latch time constant

amplifying a small difference in V_a and V_b to full logic levels. The time required for this amplification is dependent on the initial difference. If the initial difference between V_a and V_b when the latch is strobed is V_0, and the desired voltage difference is V_f, then the time required is [75, 66]

$$t_{comp} = \frac{\tau}{A-1} \ln\left(\frac{V_f}{V_0}\right) \tag{2.19}$$

where $\tau = RC$ and A is the small-signal gain of the inverters. Thus, for arbitrarily small inputs, the amplification time is arbitrarily long or meta-stable. If the input to the comparator is random, then there is a finite probability that the comparator will not be able to render a decision in a given time period. If the time given to make a decision is T, and the input is uniformly distributed from $[-V_f, V_f]$ then probability that the comparator will not amplify to full output levels is [75, 66]

$$P(t_{comp} > T) = \exp\left(\frac{-(A-1)T}{\tau}\right). \tag{2.20}$$

This result is *independent* of thermal noise and offsets. Therefore, if $P << 1$ then the mean time to failure (MTF) is given by

$$\mathrm{MTF} \approx \frac{1}{NfP} \tag{2.21}$$

where N are the number of concurrently operating comparators in the system and f is the frequency of comparisons per second. In a real design, τ and T must be chosen such that the mean time to failure is sufficiently long, such as the lifetime of the system (e.g. 20 years).