

# Administrivia

- Oral timeslot Doodle has been posted
  - Most students have grabbed a slot
- Need to arrange sit-down signup as well (upcoming)
- Come prepared to labs!
  - In particular lab 4.
- Low # of reflection submissions (24, 17, 17)
  - Common reasons, or just coincidence?

# Specifications and dynamic range

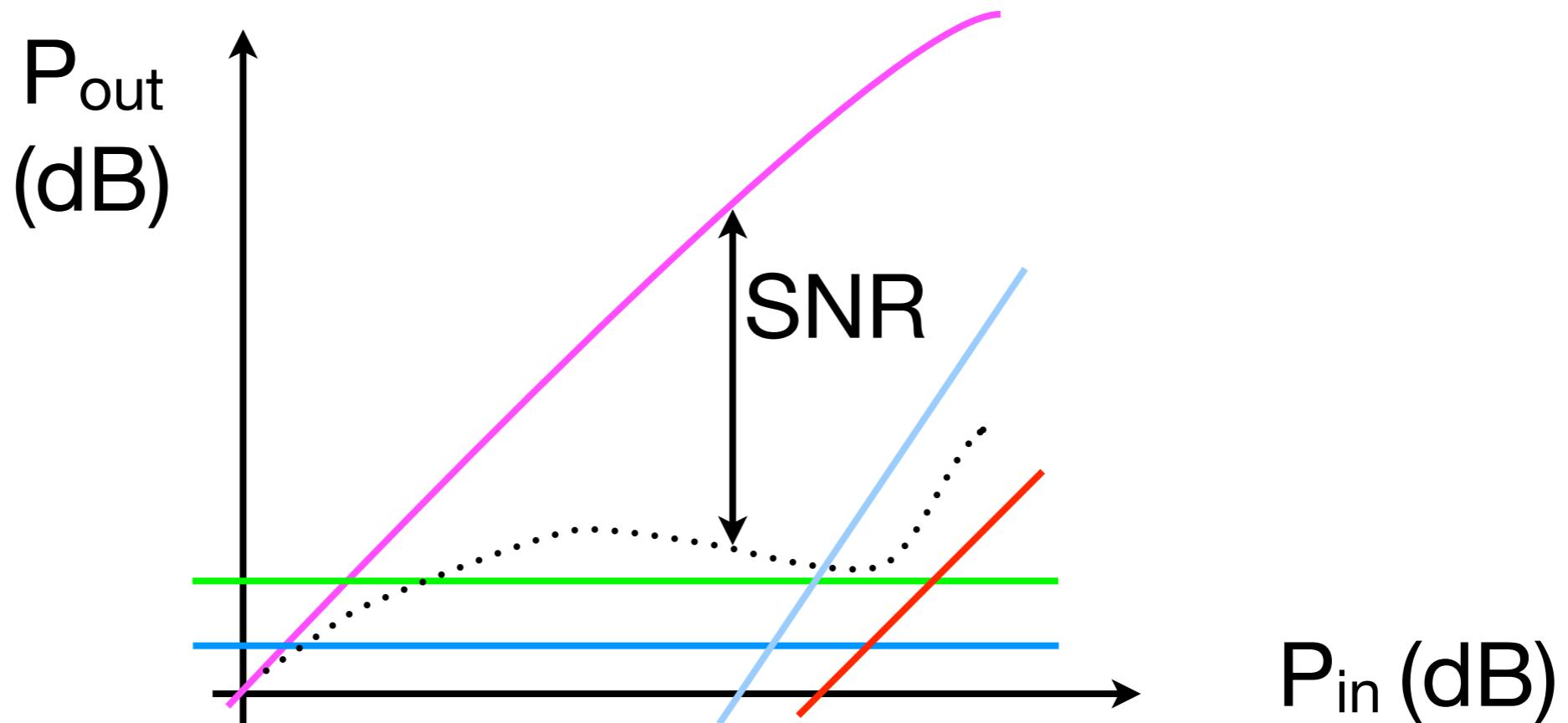
DAT116, Dec 3 2018

[larssv@chalmers.se](mailto:larssv@chalmers.se)

# Conversion phenomena

- Ideal
  - # bits
  - Sample rate, aliasing
- Non-ideal
  - noise
  - jitter
  - nonlinearities

# Manifestations



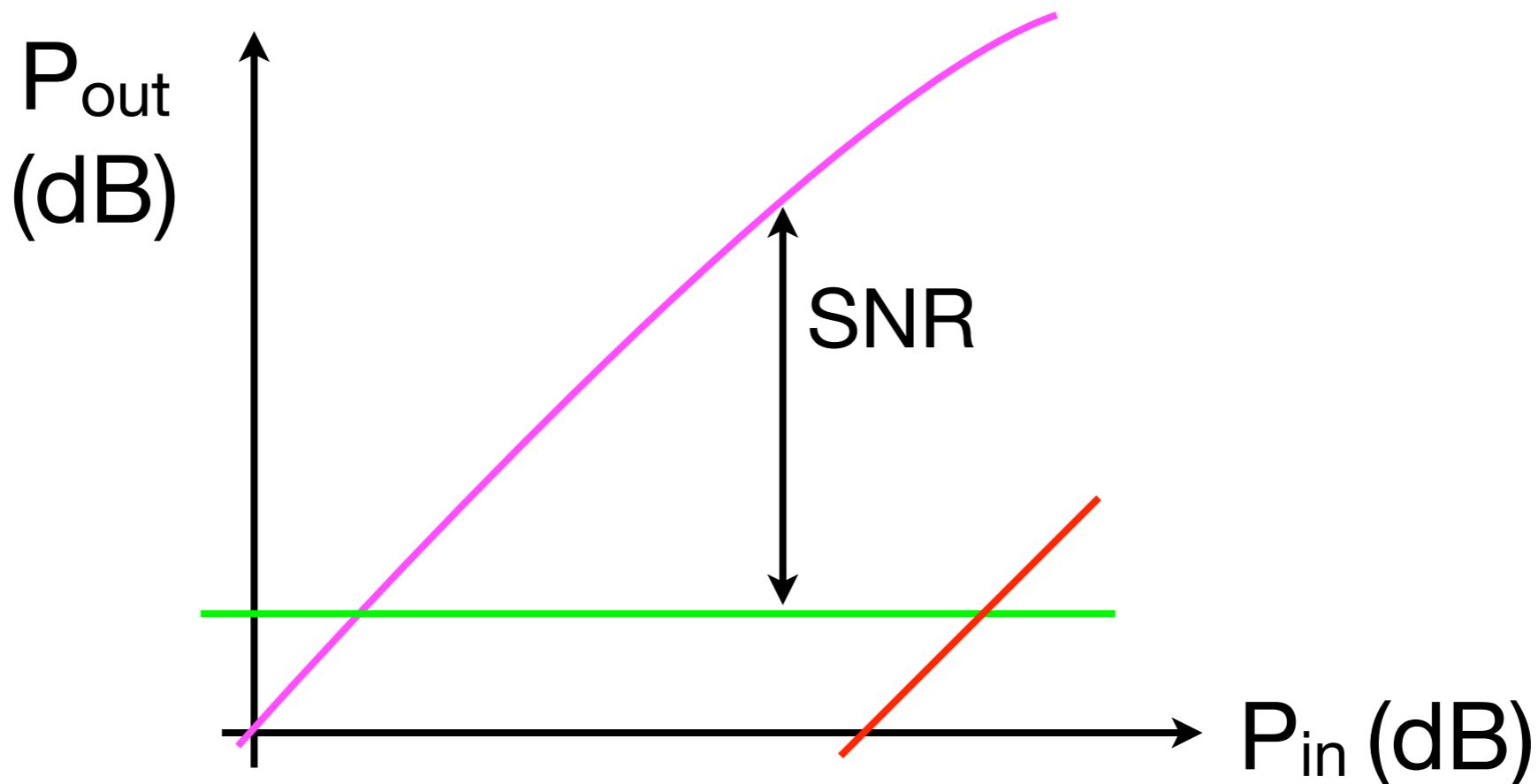
- Desired signal
- Thermal noise
- Quantization noise
- Sampling jitter
- Harmonics (2f, 3f, ...)
- Other stuff...

# Limits

- Small end
  - Noises
- Big end
  - Nonlinearities
- All over
  - Jitter
- Reading: Maloberti Ch. 2

# Performance measures

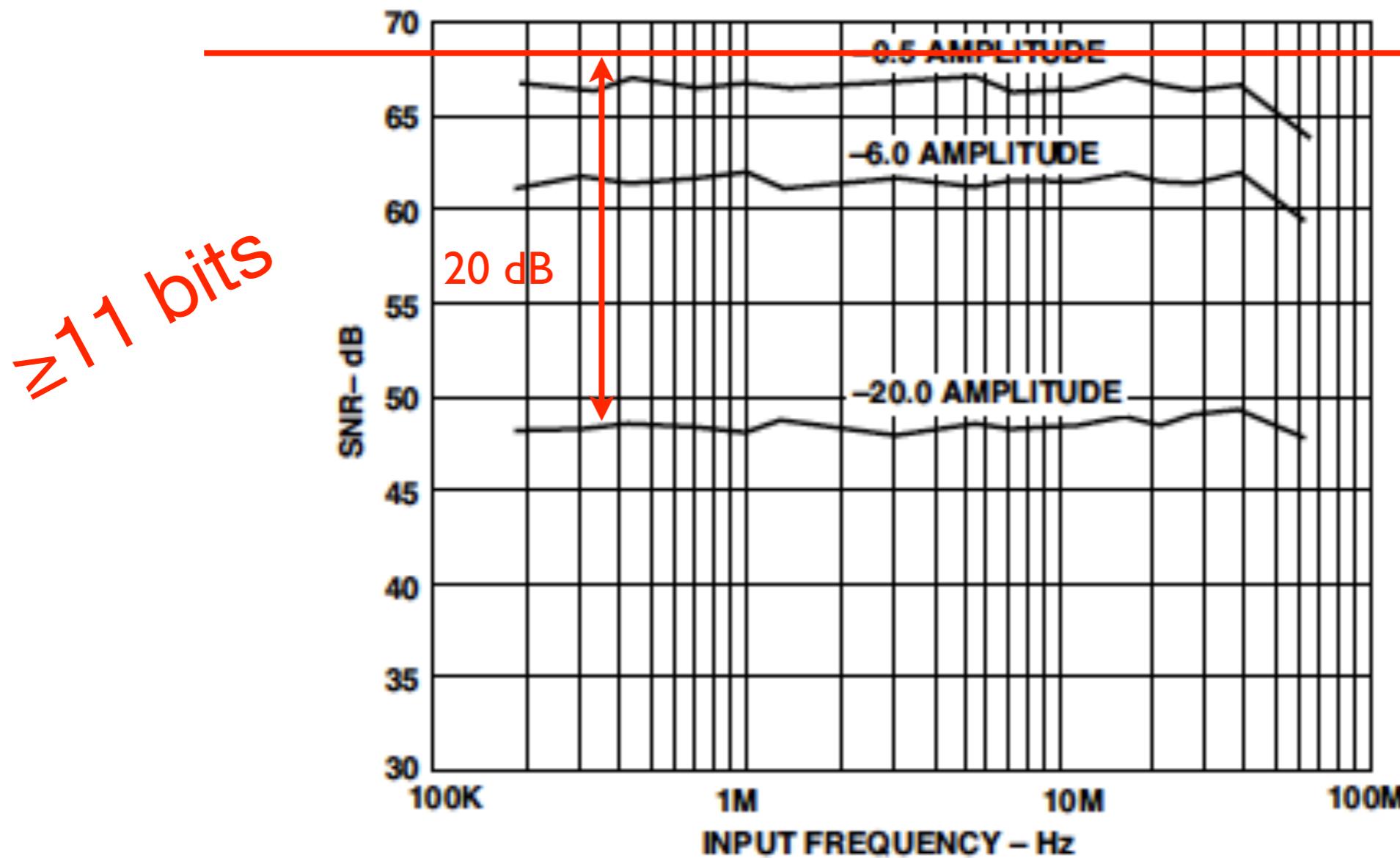
# Signal to Noise Ratio (SNR)



- Ratio of signal power to noise power (in dB):  $S / N$
- Typically assumes single-sinewave input
- Must specify input level, frequency, and bandwidth!
- Most often, largest value across input levels is given

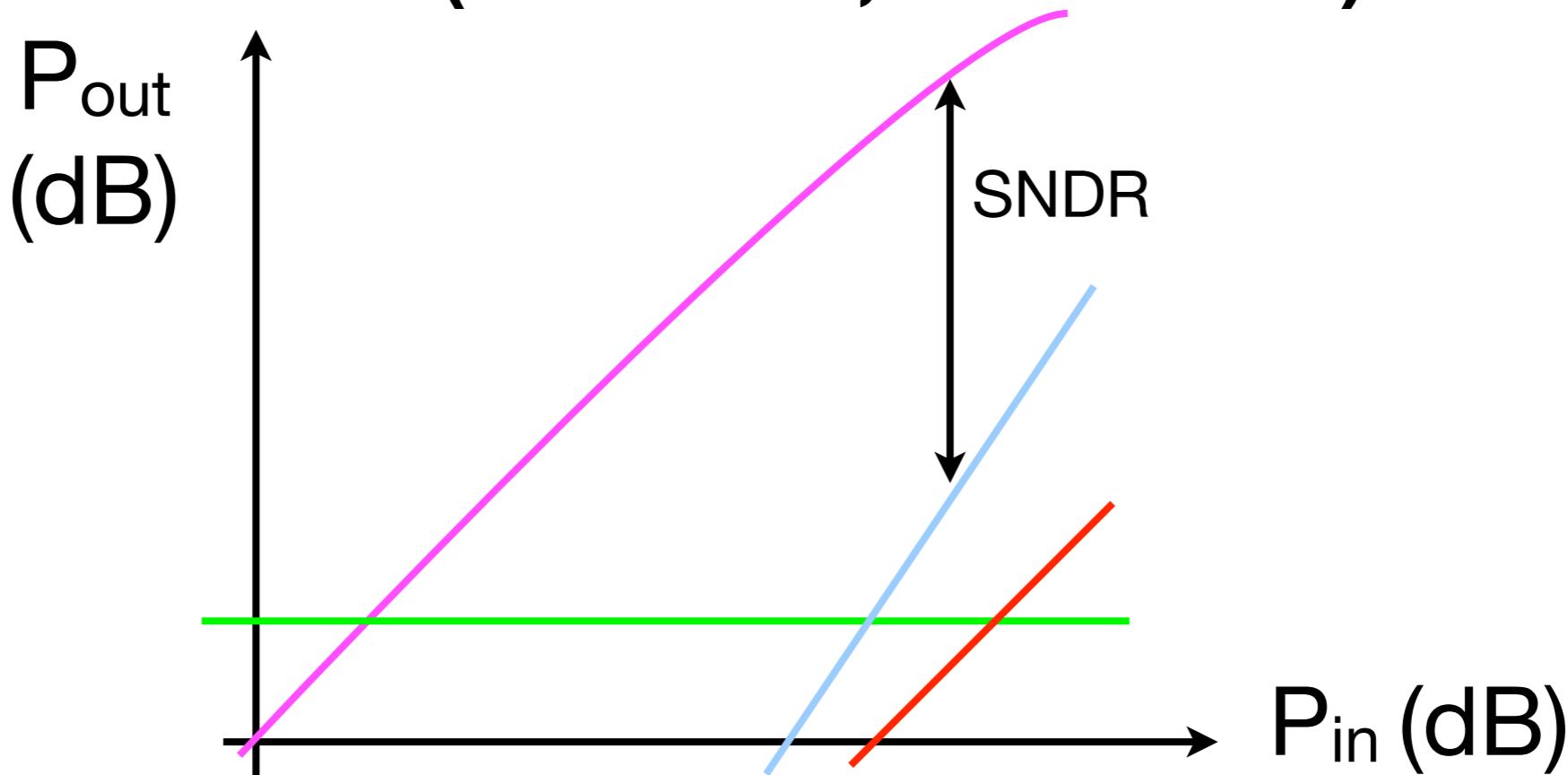
Resolution?

# ADC example



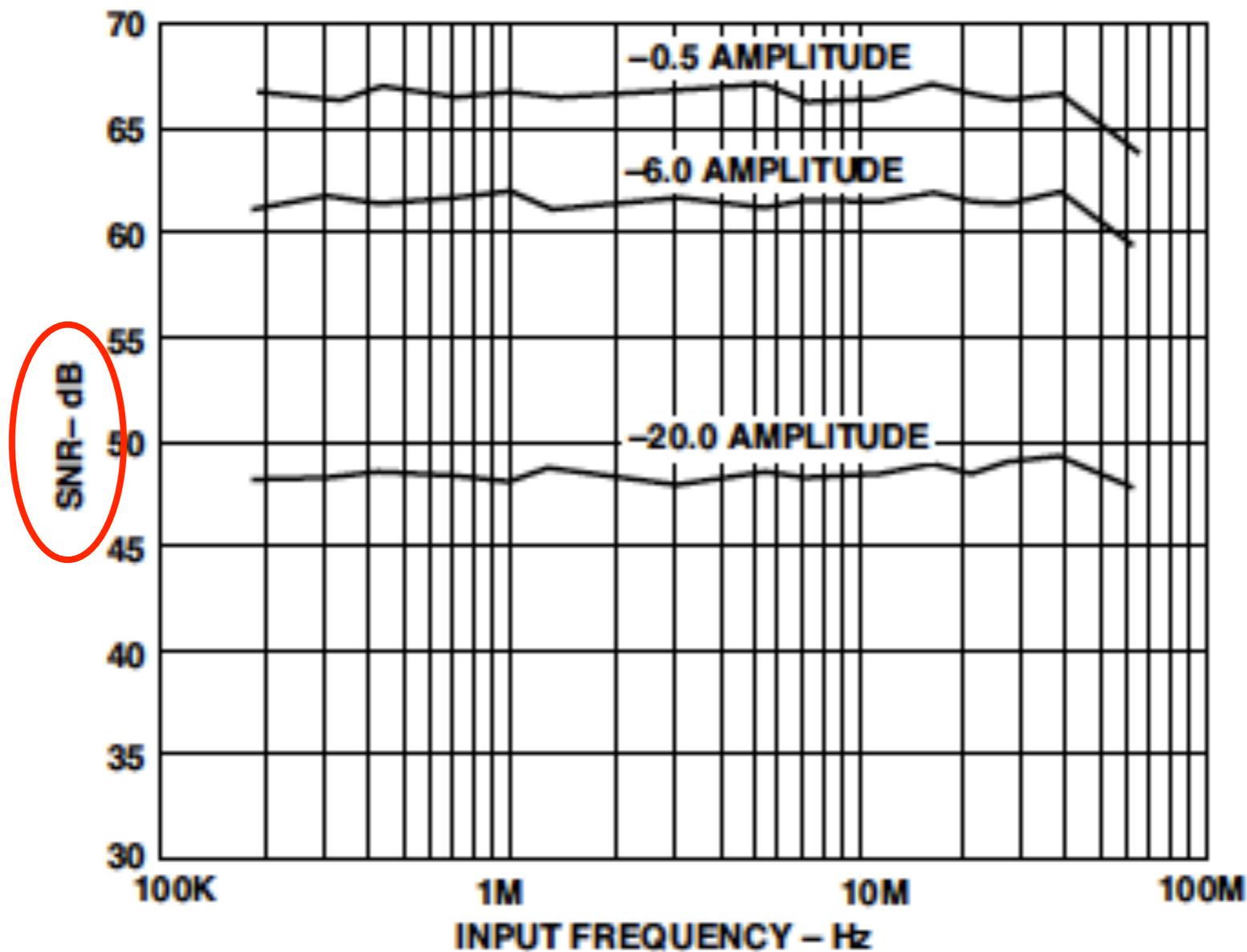
- SNR vs signal frequency at several amplitudes

# Signal-to-Noise-and-Distortion Ratio (SNDR, SINAD)



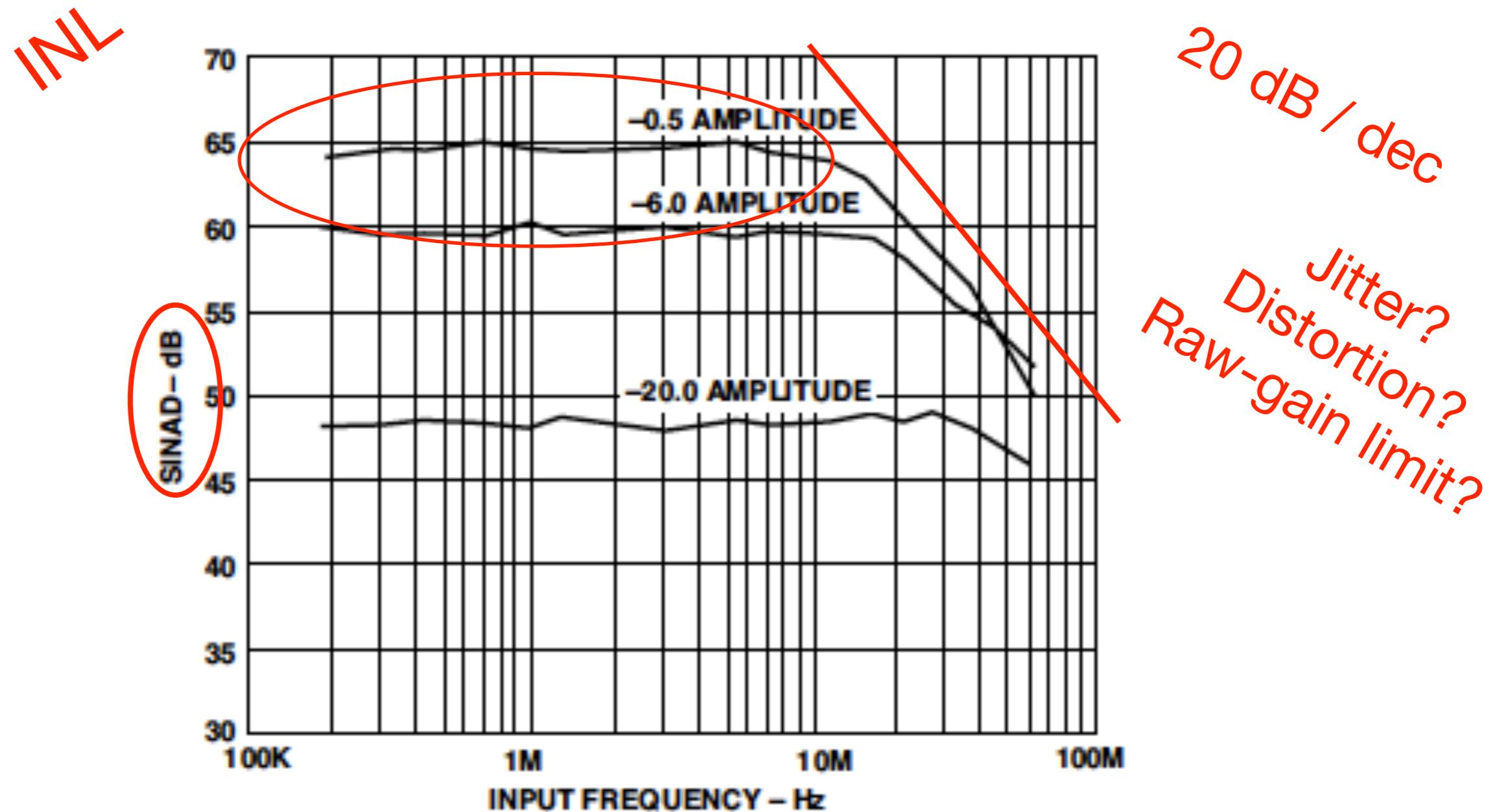
- Explicitly include harmonics:  $\text{SNDR} = S / (N + D)$ 
  - Sloppy terminology. “SNR” may include D too. Careful!
- Varies with level and frequency, just as SNR does
- Note: SNDR may shrink with increased power level!
- Beware measurement bandwidth!

# ADC example



- SNR vs frequency for several amplitudes

# ADC example

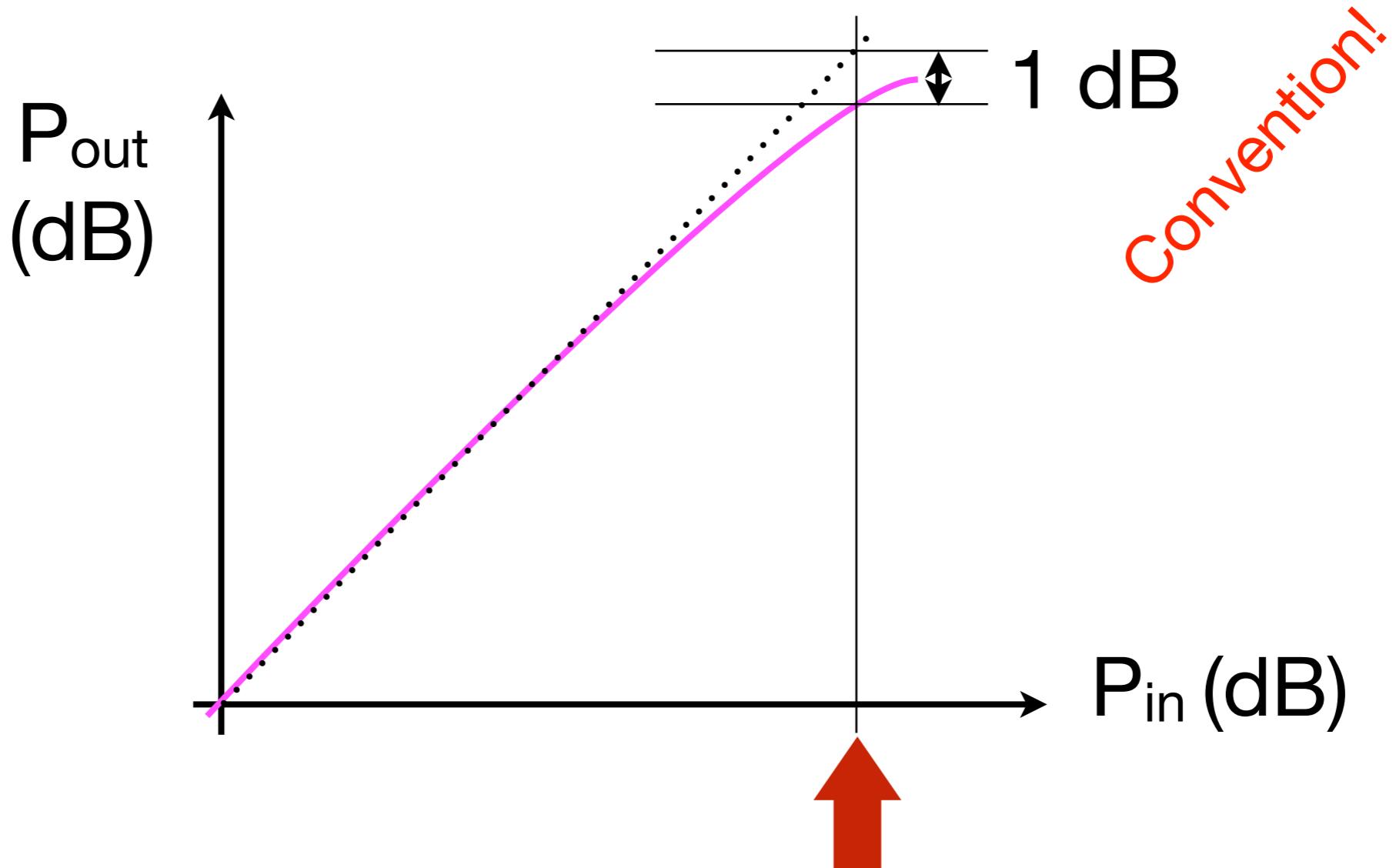


- SINAD vs frequency for several amplitudes

# Effective # of bits (ENOB)

- Relate total noise and distortion to a hypothetical “perfect” converter
- $\text{ENOB} = (\text{SINAD}_{\text{dB}} - 1.76) / 6.02$
- Should be close to actual # of bits
- May be difficult, esp. at high speeds
  - See previous slide!

# Compression point



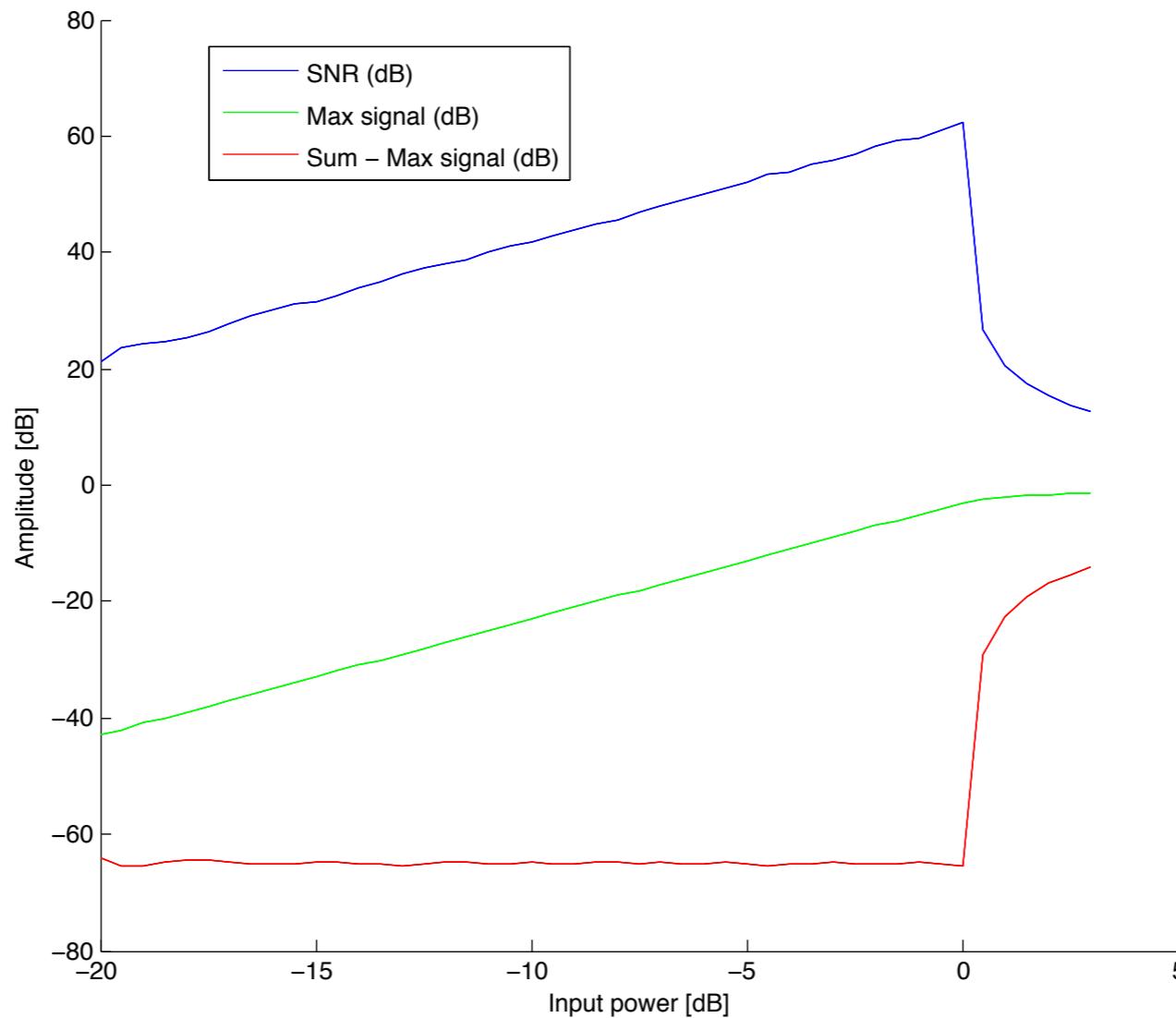
- Maximum “useful” input level

# Ex: CP for hard clipping



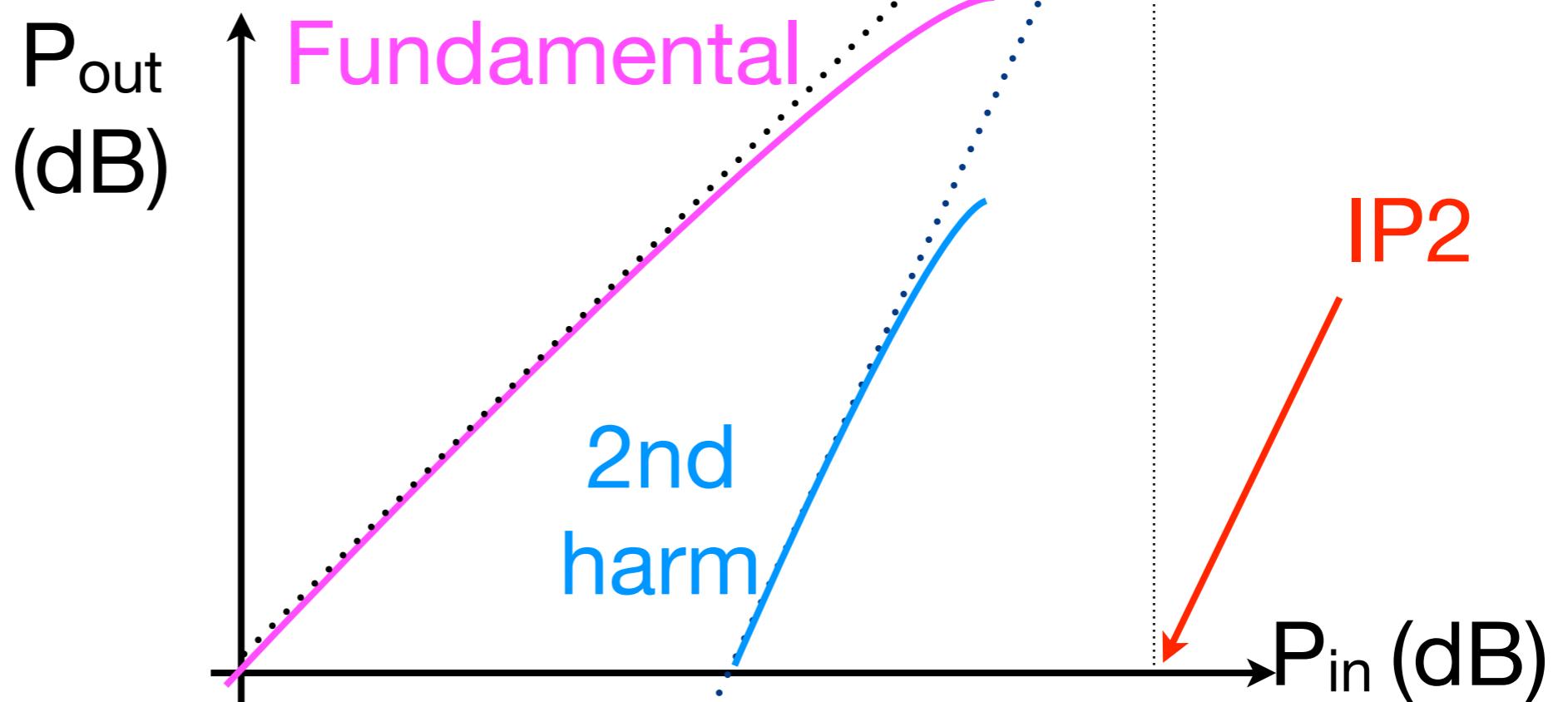
- Single sinewave clipped at 0dB

# Image from a Lab3 report...



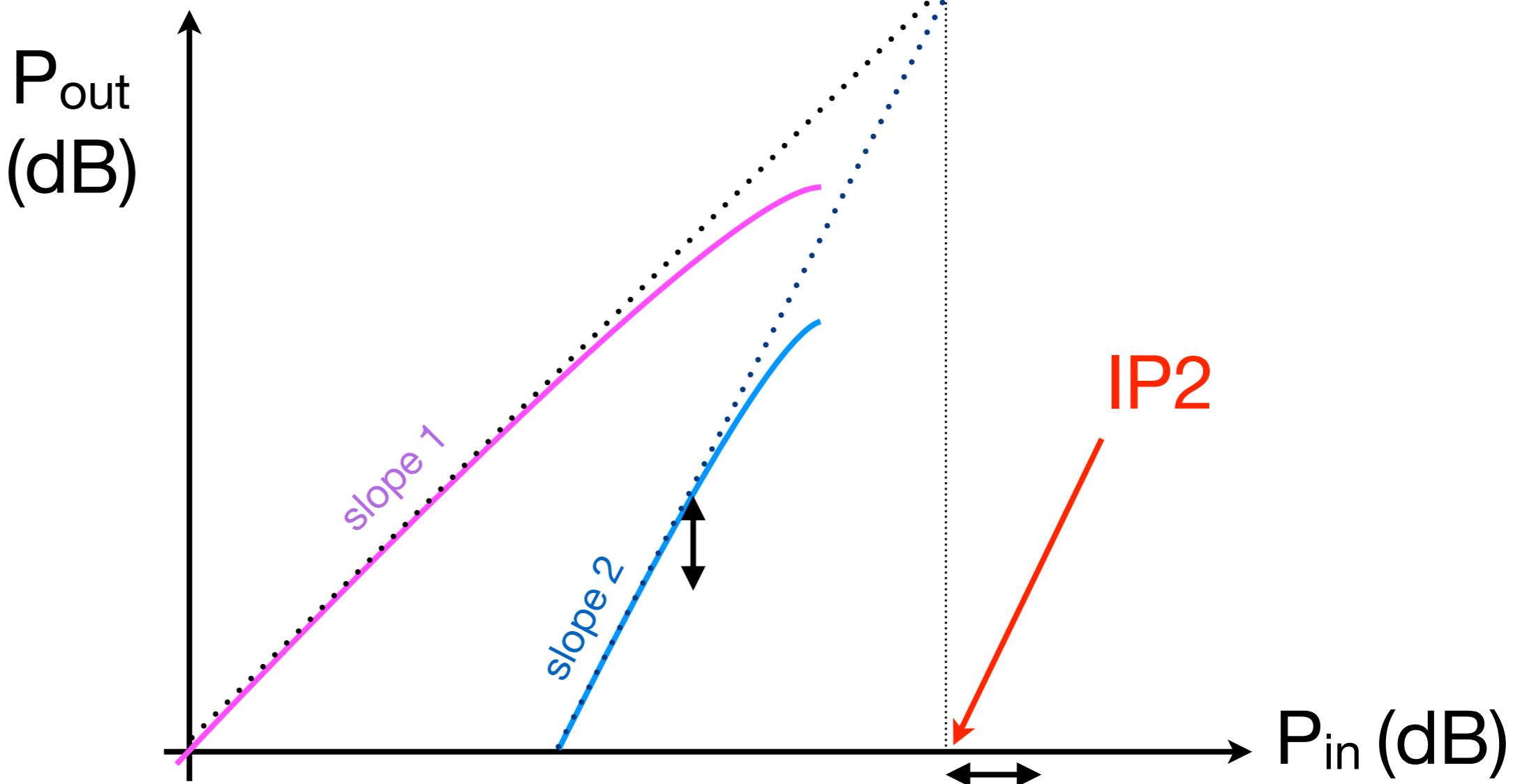
- SNR reduction mostly due to distortion rise

# Intercept point (IP)



- IP2, IP3 etc (per harmonic)
  - IP3 typically the most critical one
- With CP, relates  $H_n$  to fundamental

# High IP is good!



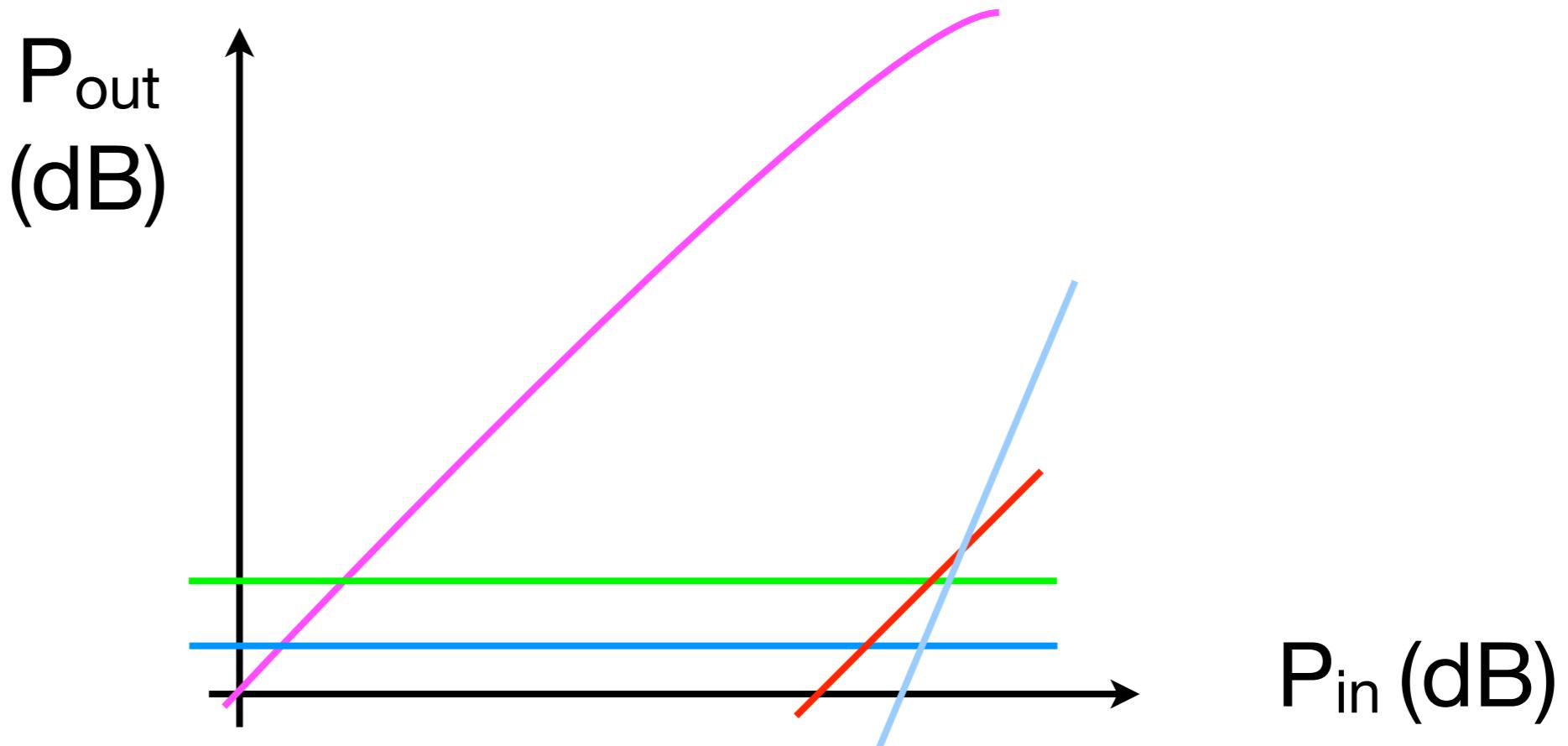
- Suppress harmonic  $n$  by  $x$  dB
- $IP_n$  increases by  $x / (n - 1)$  dB

# High-f distortion?

- Pure harmonic falls outside band of interest!
  - More important: 3rd-order intermodulation (IM)

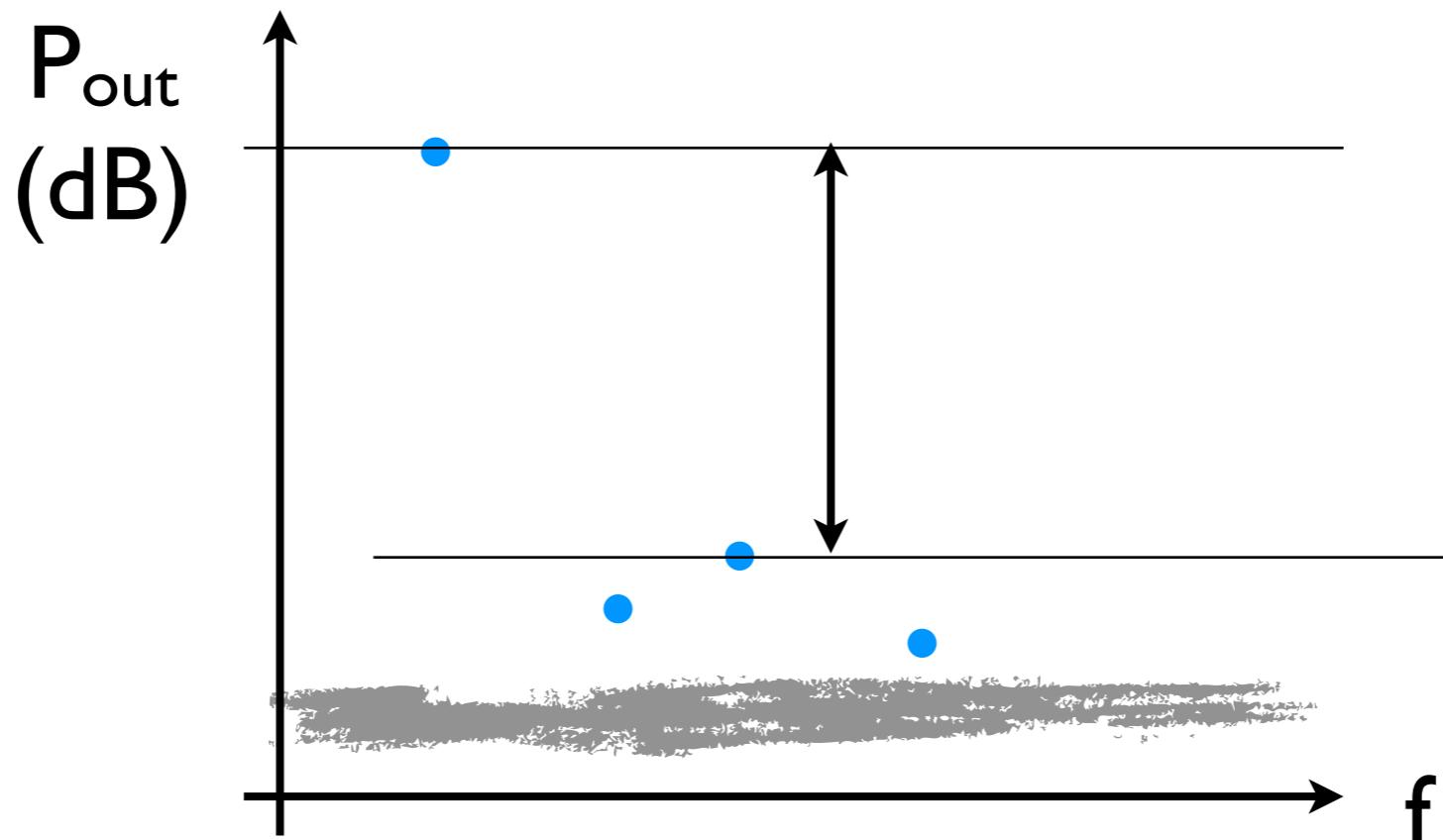
- With  $f_2 \approx f_1$ ,  $2f_1 - f_2 \approx f_1$  😣
  - Intermodulation products close to input signals!
  - Can't be removed by frequency-selective filter!
  - Magnitudes characterized by IP3

# Balance



- Useful dynamic range often limited by H3, jitter
  - Strive to make neither error much worse than the other

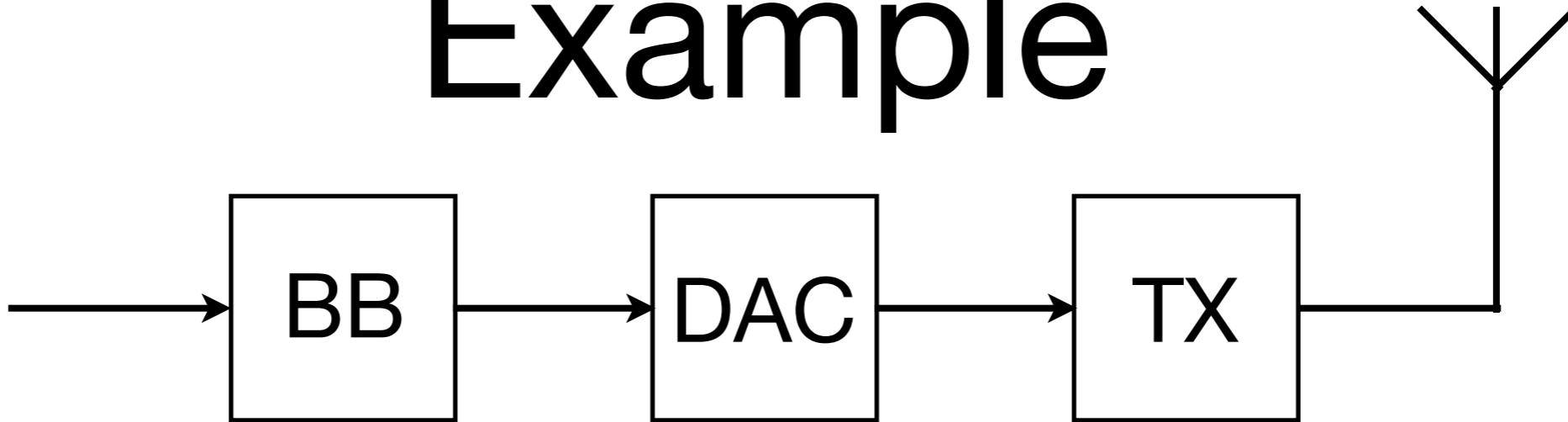
# Spurious-Free Dynamic Range (SFDR)



*Note:  
not power diagram*

- Signal vs. worst harmonic
  - Always numerically higher than SNDR
  - Important in e.g. telecom systems

# Example



- Radio modem (baseband, DAC, transmitter)
- Spectrum mask for transmitted signal
  - Specifies max transmitted power vs frequency
  - High power in intended band/channel, low elsewhere
- DAC SFDR may limit power outside intended band
  - Often given in dBc (relative to carrier, i.e. the intended signal)

# Additional specs

- Power
- Electrical levels
- Temperature stability
- Drift
- Latency
- Timing
- ...

The internet is full of  
Converter data  
sheets

# Converter vs. system

- Same specification terminology useful for full interface system!
  - Converter, filters, amplifiers, etc
- Useful for DACs as well as for ADCs
- From full specs, derive specs for blocks
  - Assign “noise/distortion budgets”

# Larger example

- Gigabit Ethernet signalling (twisted-pair copper wire)
- Issues:
  - Compatibility w/ 100Mb/s signaling
  - Cable properties
  - Error probabilities

# Twisted-pair cable



- Four pairs, twisted at different #turns / m
- Cabling standard states length  $\leq 100\text{m}$

# 100Mb/s signalling

- Use one pair per direction
  - Two pairs unused!
- Three voltage levels (+1, 0, -1)
- Apply channel coding to avoid DC transmission
  - Essentially a filter with 0 at DC

# 1 GB/s signalling

- As 100MB/s, but...
  - ... use all 4 pairs...
  - ... and each in both directions...
  - ... and 5 levels ( $\pm 2$ ,  $\pm 1$ , 0)
  - ... and better coding
- Figures from Roo et al (uploaded)

# Bidirectional signalling?

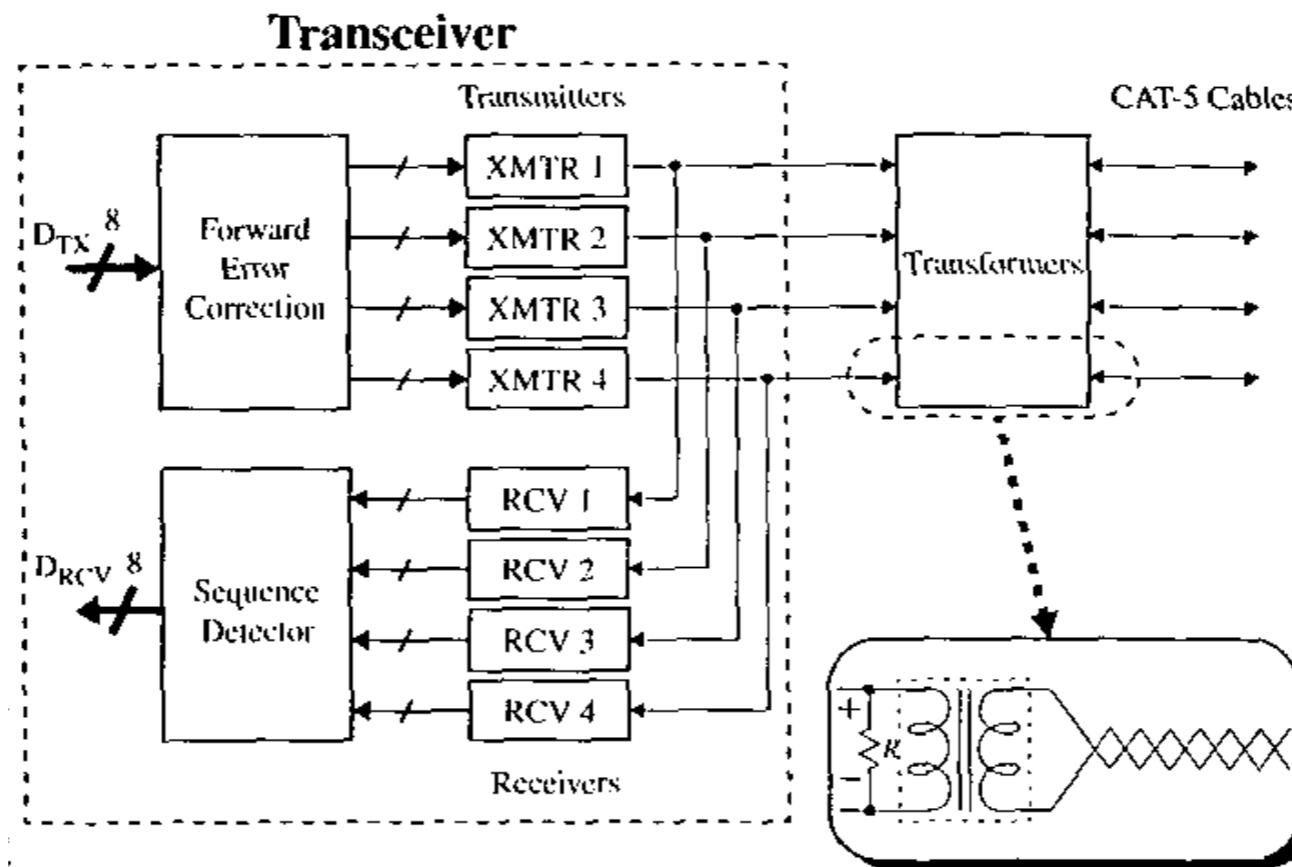
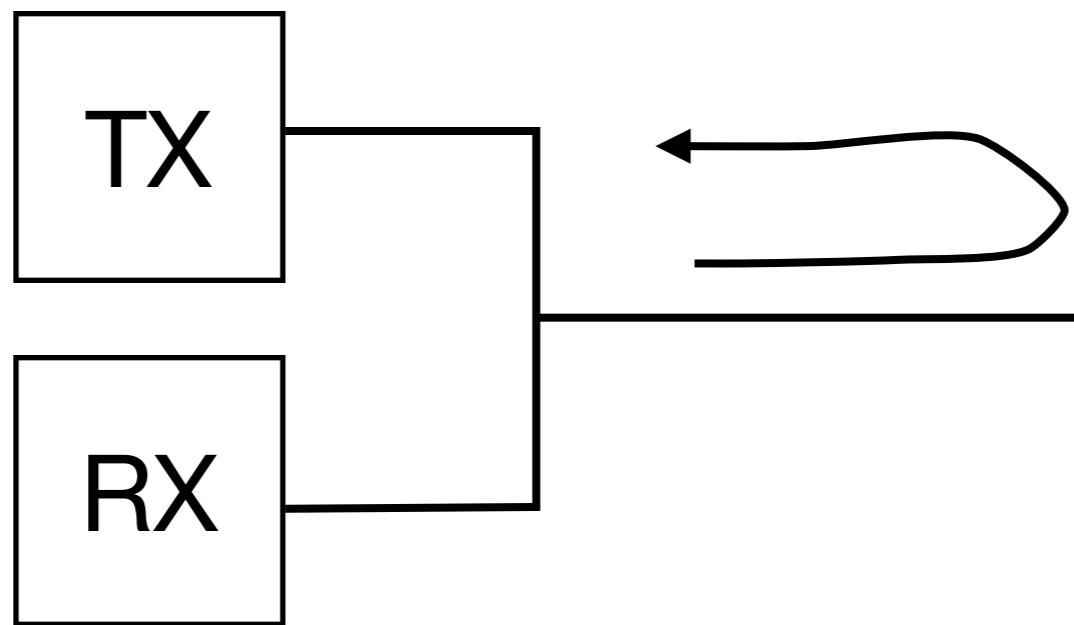


Figure 19.7.1: Gigabit transceiver system block diagram.

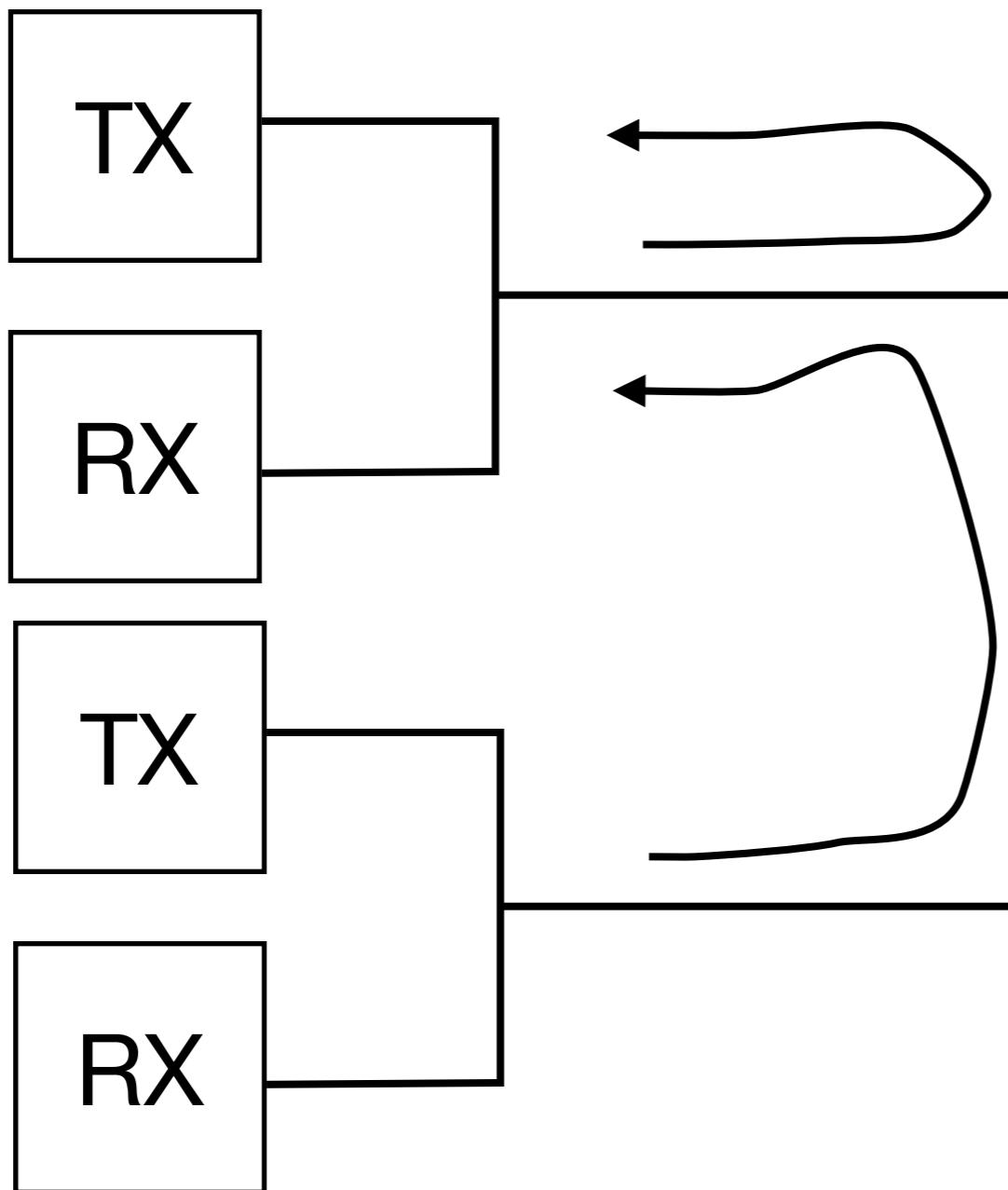
- Transmitter drives each line
- A receiver listens to the same line
- Must subtract transmitted signal from received signal

# Echo



- Received signal also contains delayed version of transmitted signal
- Echo depends on cable, contacts, etc
  - Transceiver must adapt to whatever is plugged in

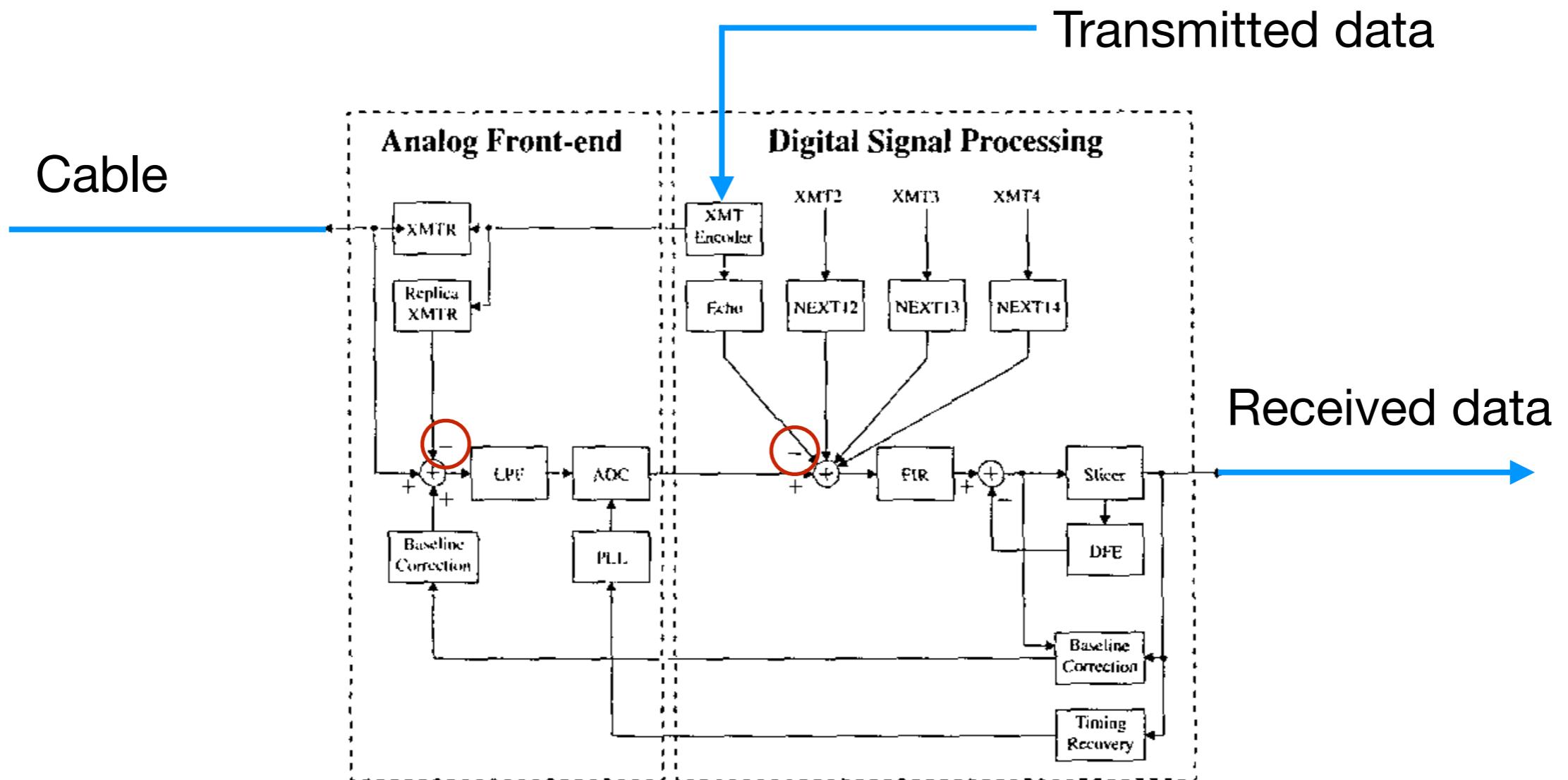
# More echos



“Crosstalk” echoes  
have lower power  
Not low enough  
to be ignored :-(

- All 4 near-end transmitters cause echo!

# PHY architecture

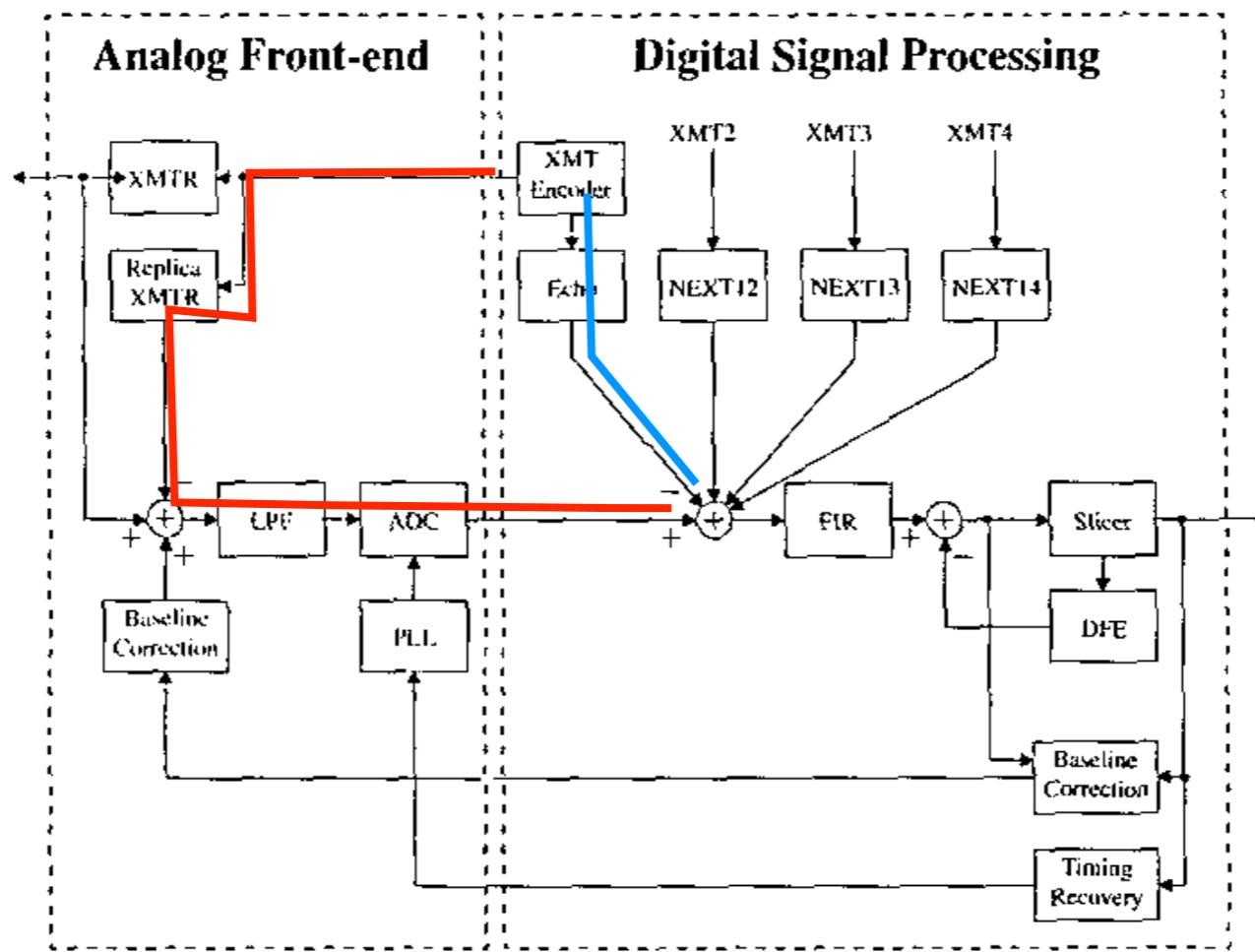


- Transmitted signal subtracted twice
  - Analogly(?) + digitally

# How specify ADC, DAC?

- Cable standard specifies frequency response, echo, allowable voltage, external noise
  - Calculate worst-case power loss @ max length
  - Derive worst-case (weakest) signal power at receiver input
- Allowable bit error rate set by Ethernet standard
  - Derive necessary SNR, thence ADC ENOB etc.
- Simulate to verify!

# DAC accuracy



- DAC-ADC path must cancel digital path
- High DAC accuracy needed, despite only 5 levels!

# Summary

- Many ways to specify data conversion / mixed-signal performance
- Most specification styles are related
  - Often possible to estimate one from the other
  - Questionable accuracy...
- Preferred performance measure application dependent

# Summary, cont.

- At system level, digital processing helps reduce requirements for ADC/DAC
- May also help improve ADC/DAC
  - Digital correction
  - Randomization
- Look forward to Theme 7!