Converter architectures and conversion errors

DAT116, Nov 22 2018

larssv@chalmers.se

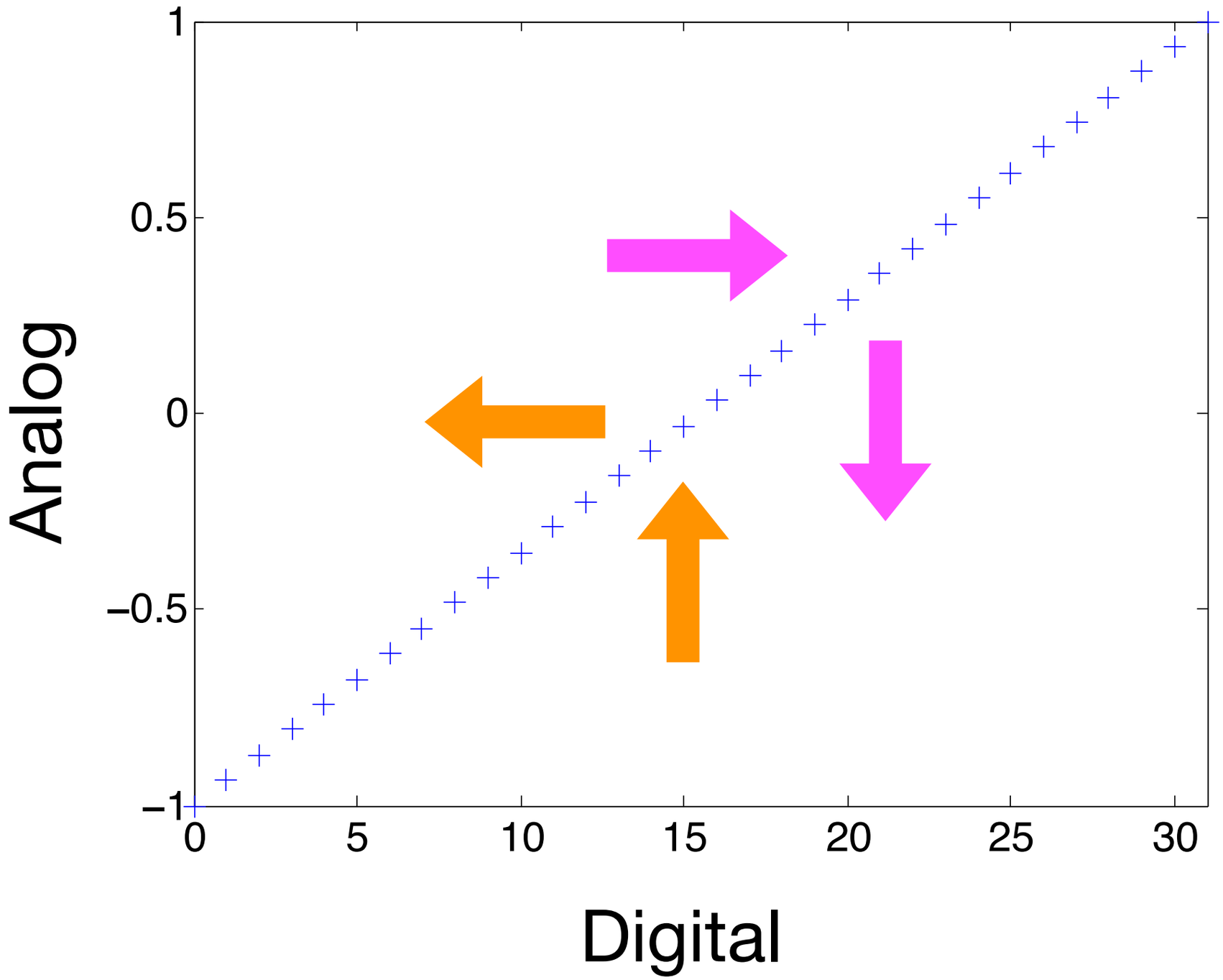
Why?

- Introduce major converter architectures
- Understand causes of quantization non-idealities
- Recognize certain common issues

What?

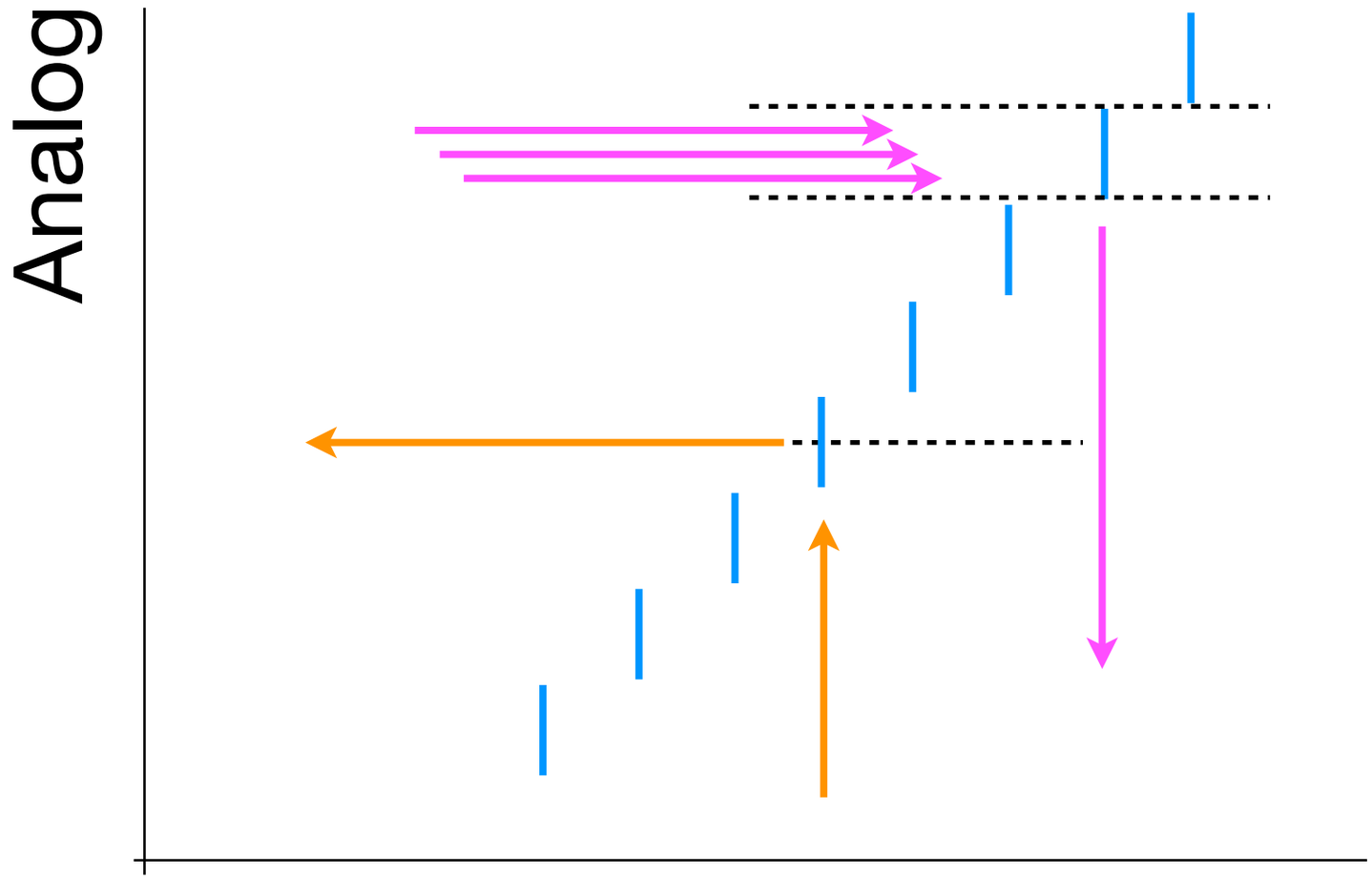
- Quantization mechanisms vs. error types
- Two main classes with different error characteristics; examples of each
  - Unary scaling
  - Binary scaling
- DACs vs ADCs; similarities and differences

ADC vs DAC



Mappings

A to D: interval to digit



D to A: digit to value

Levels w/ errors:
interval edges
(ADC),
values (DAC)

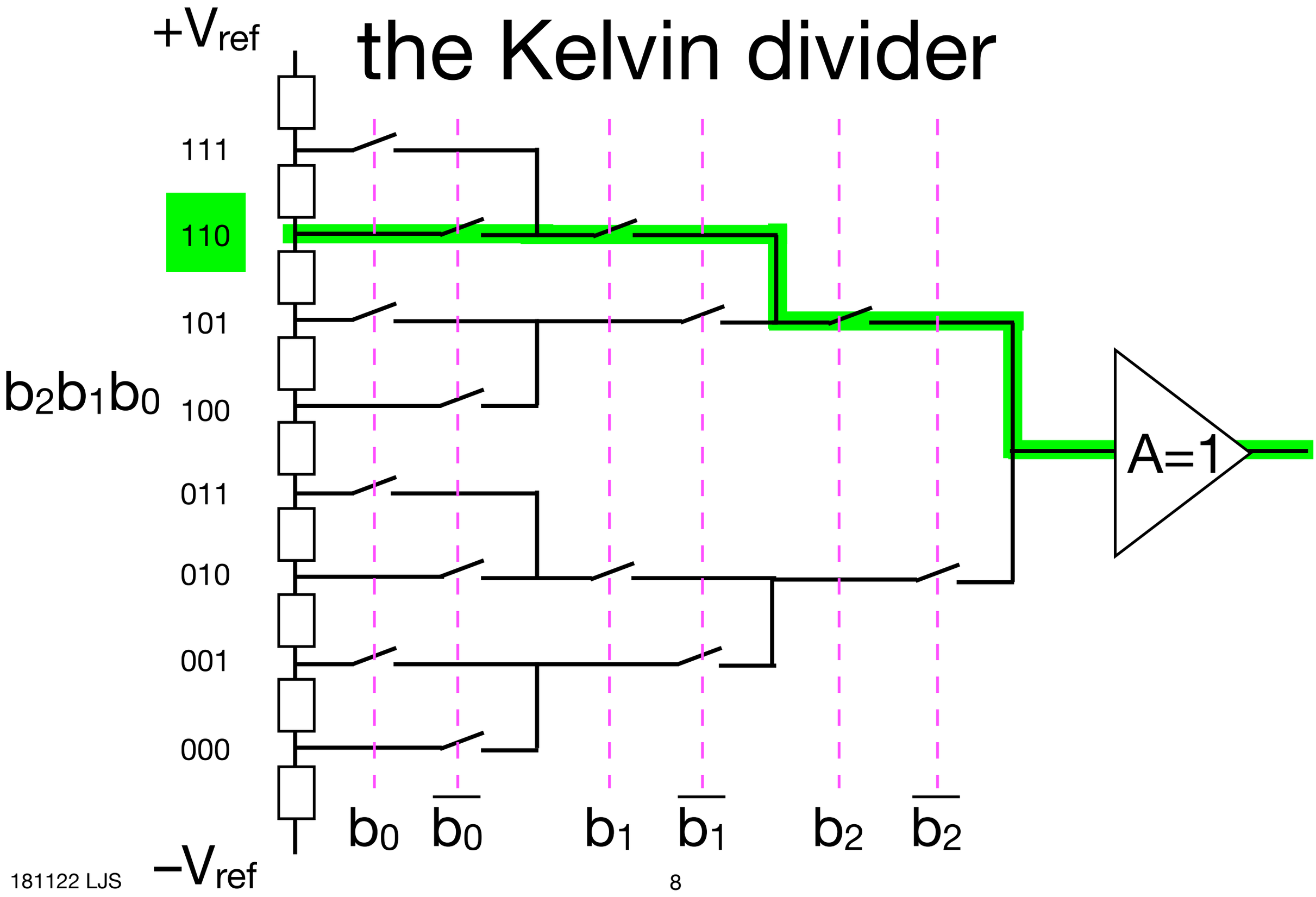
Numbers,
separations
of levels
similar

D-to-A conversion

DAC principles

- Unary scaling:
  - Kelvin divider
  - Current summer
- Binary scaling:
  - Current summer
  - Charge summer

Unary-scaling DAC: the Kelvin divider



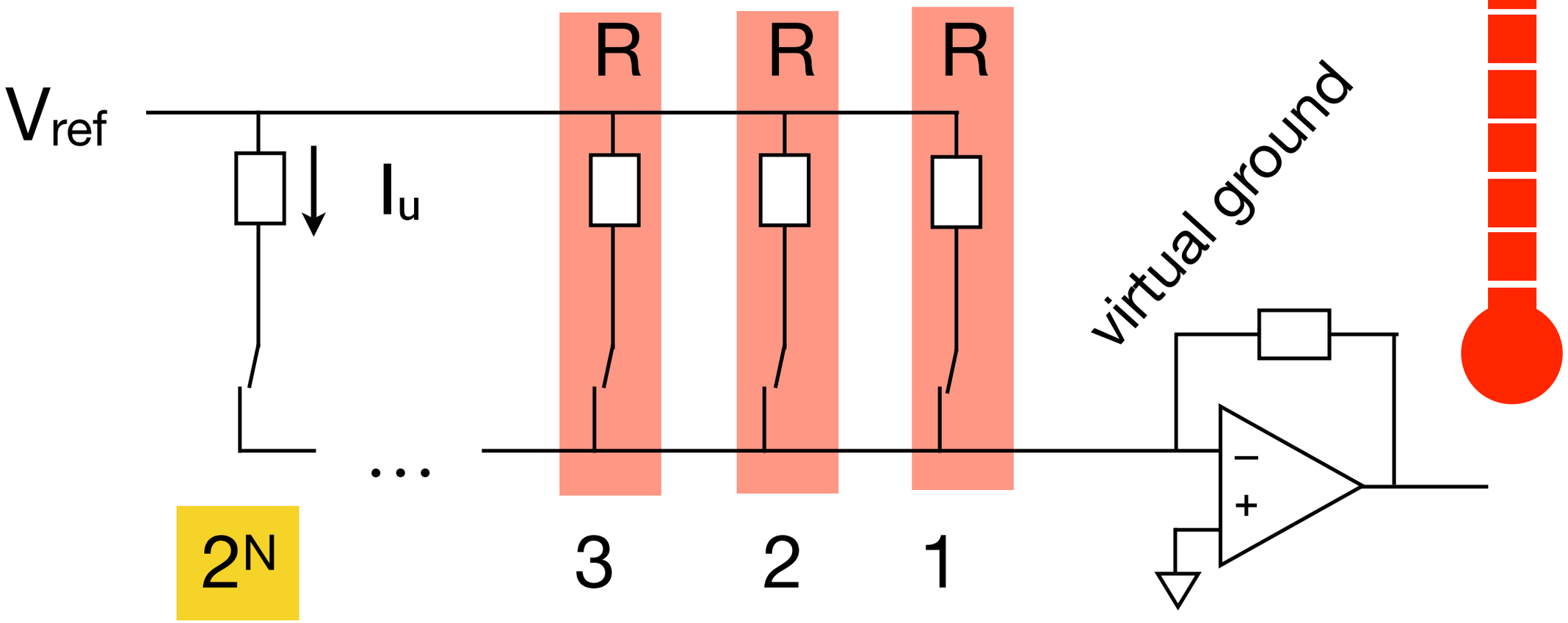
Kelvin divider performance

- Precision?
  - Resistance matching ($\sum R_i / \sum R$)
    - Large-area R_i to improve matching …
    - … thus large total size, so mfg gradients important
  - Larger random variations at ends of scale
- Speed?
  - Charge / discharge switch network C via R string
- Power?
  - C charging; DC current through R string
- Resolution?
  - ~6 bits

Used mostly as part of ADCs

Current-summing DAC

- Let V_{ref} and R define a <u>unit current</u> I_u
- Add several of those (<u>thermometer code</u>)



Other current generators possible

Current summer properties

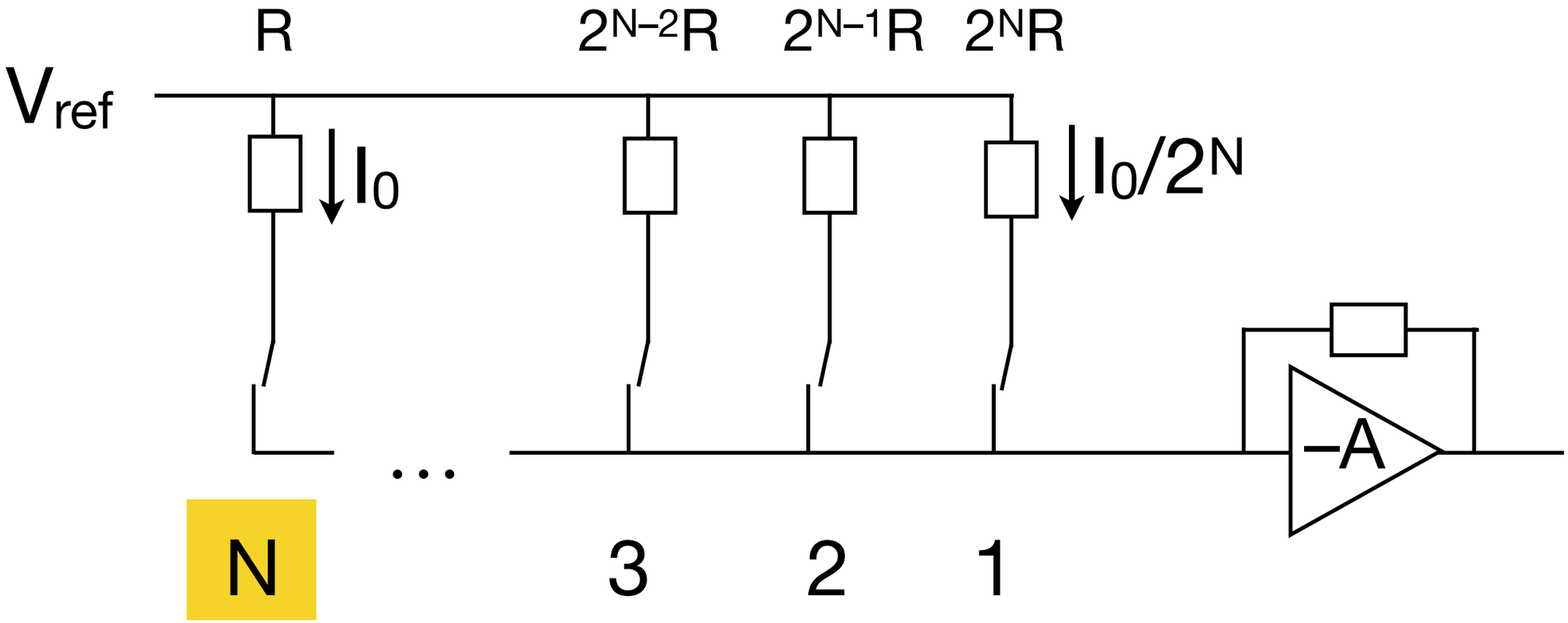
+ Good matching properties!
  - All sources nominally identical (unary scaling)
– High cost
  - ~2^N switches, current generators
– DNL limited by matching of neighbor R, switches
  - “Random” variations
– INL may be limited by manufacturing gradients
  - “Systematic” variations

Binary scaling

- Each current 1/2 of previous one

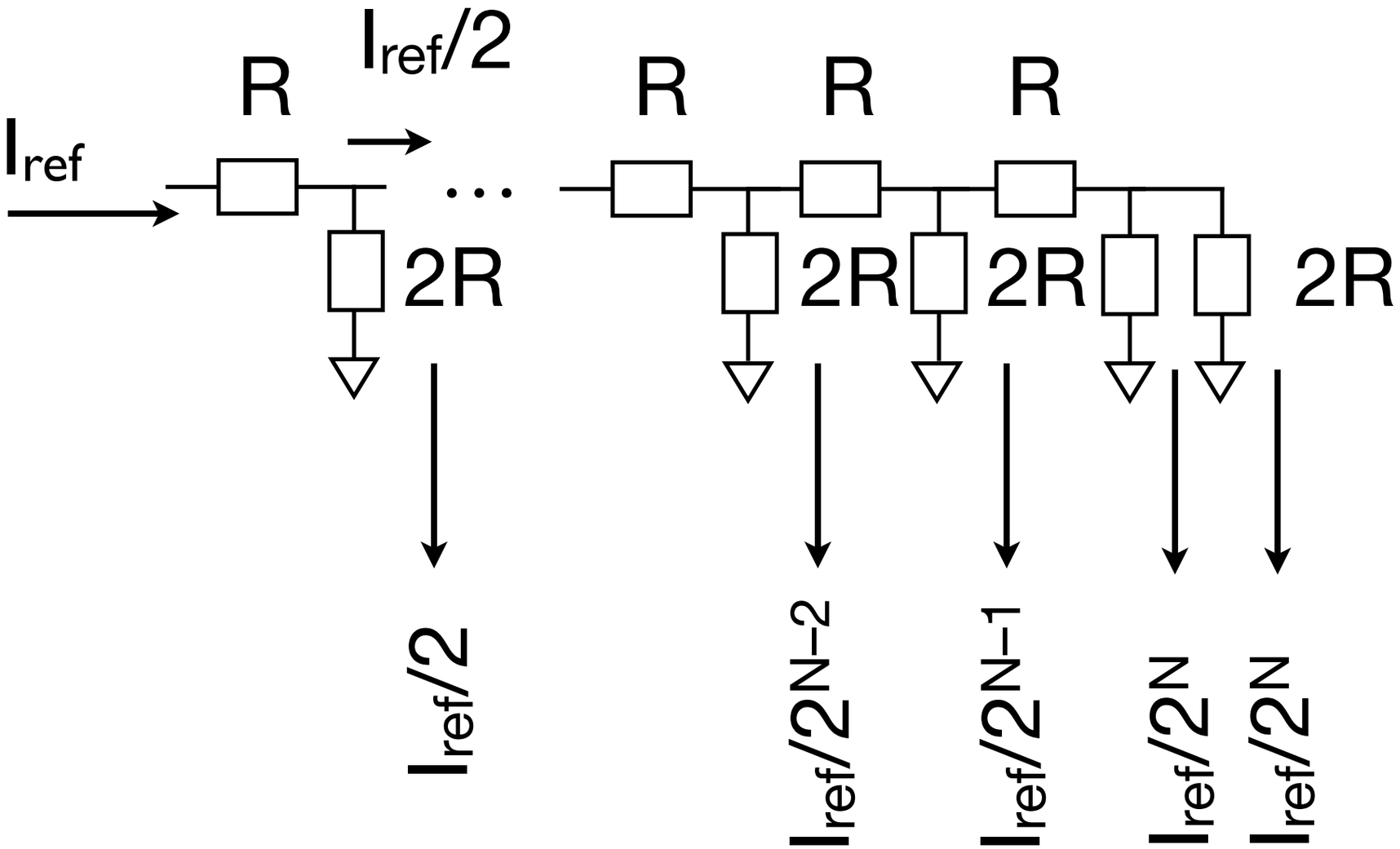
\+ ~N components! Good!

– Matching problems for large N (large R ratios)



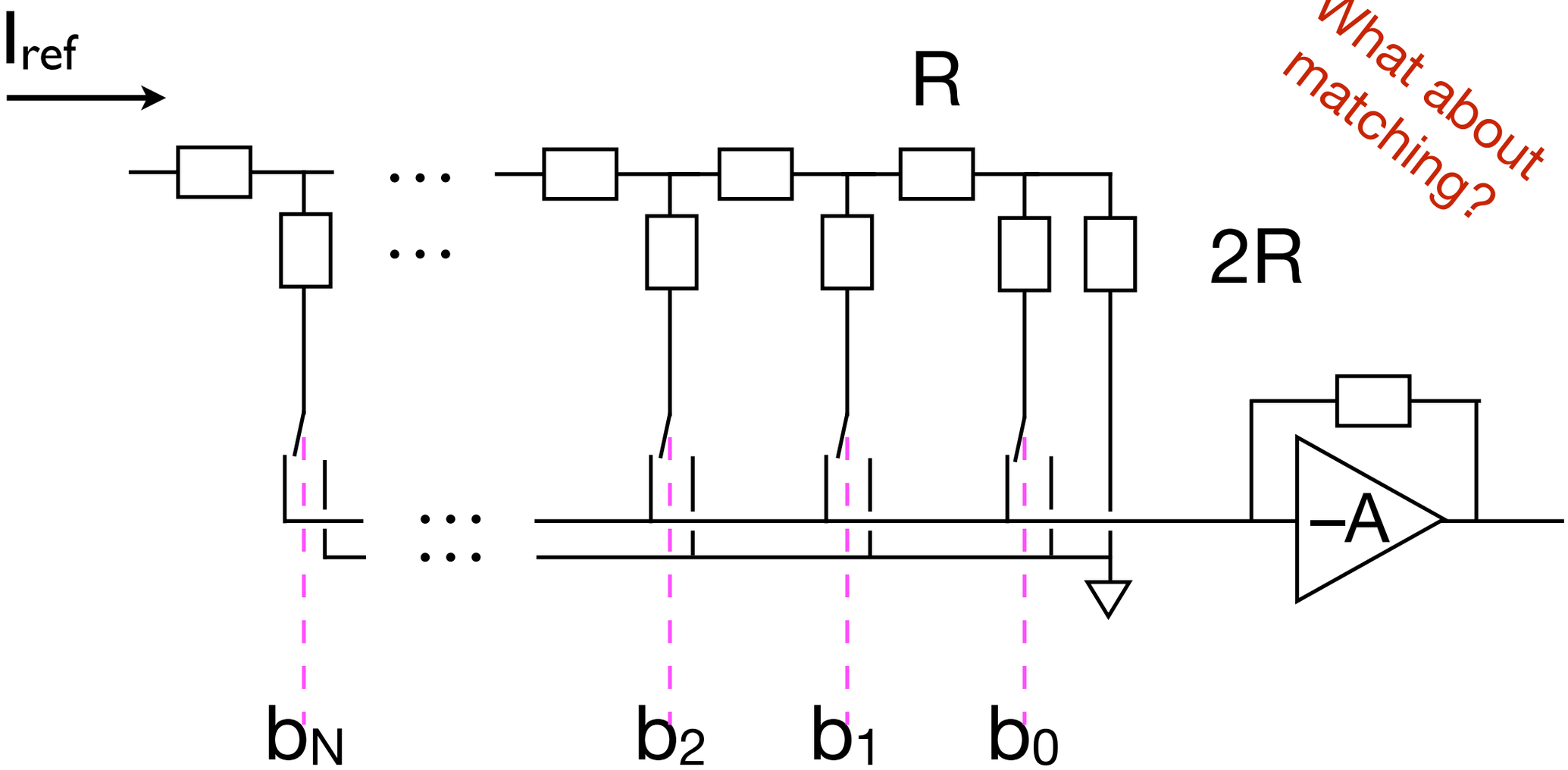
R-2R ladder

- Binary current scaling without large resistance ratios!



R-2R ladder

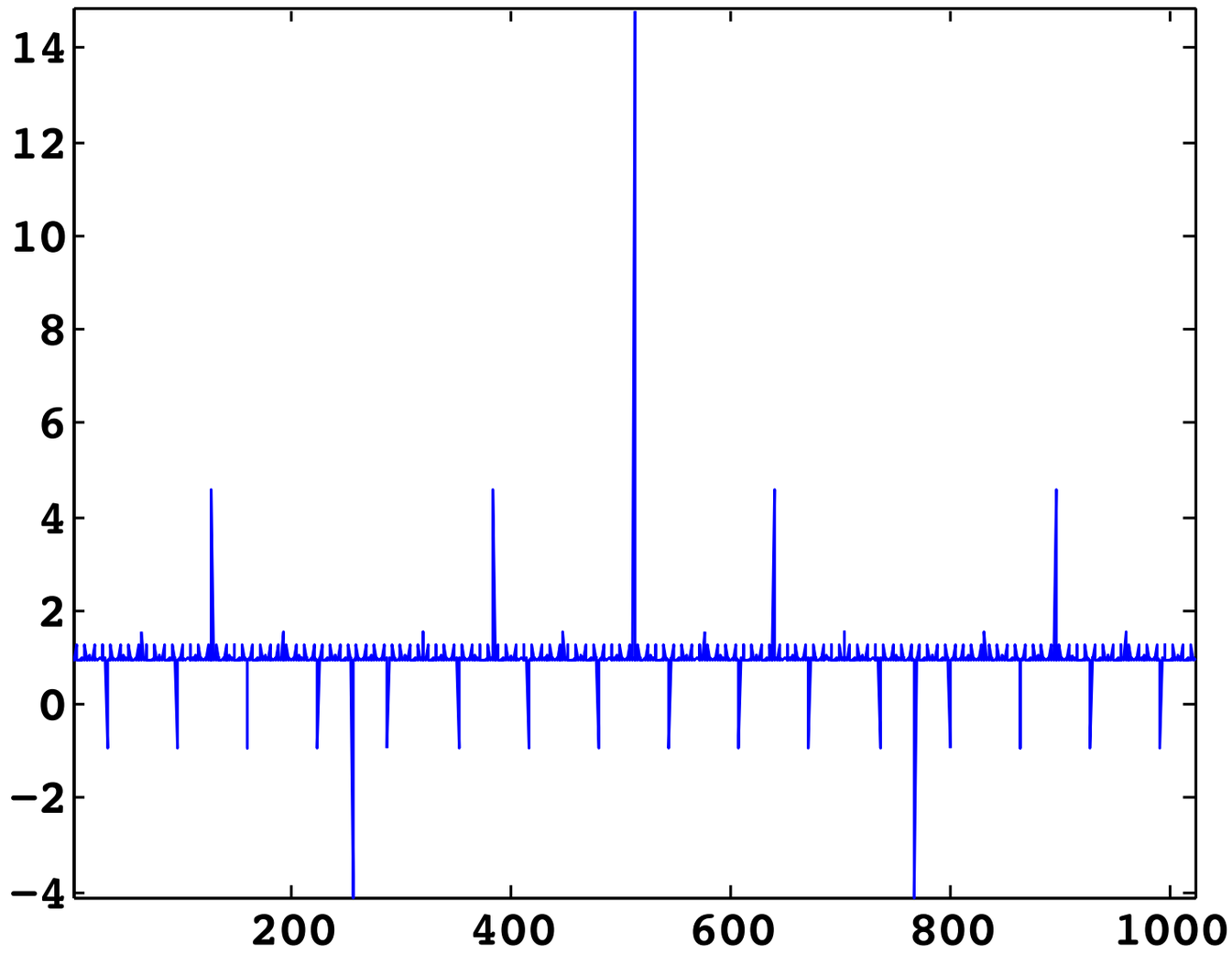
- Select some of the scaled currents; sum
- Discard rest (dump to ground)



DNL for R2R

- Random deviations from nominal R

...
011101
011110
011111
100000
100001
100010
100011
...



Typical binary-scaled

More in lab

R-2R properties

+ Few switches (~N)
+ Few resistances (~N)
+ Identical R_i help with matching

Binary scaling!

– Bad DNL when high-significance bit flips
– Glitches also worse than for Kelvin divider

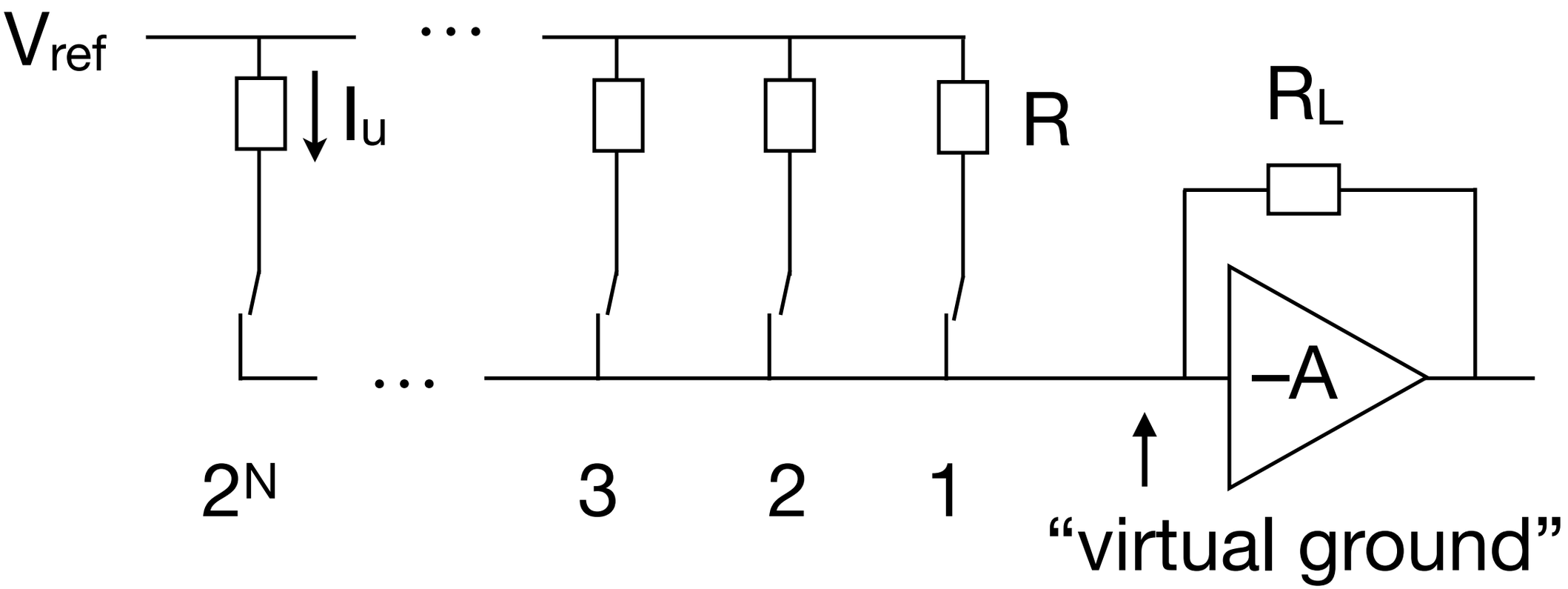
• Many variations of current-splitting topologies

Binary scaling ±

+ Few components (~N)
+ Less area
  - Less sensitive to gradients
– Bad DNL at MSB transitions
  - More in lab!

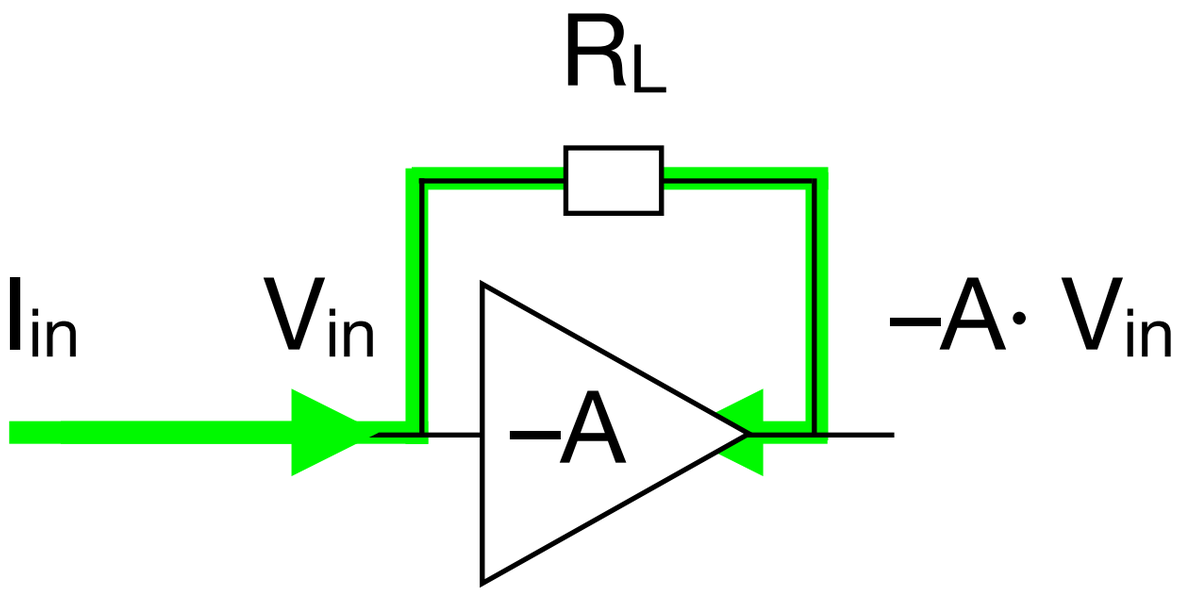
- More than ~7 bits requires trimmed R_i

Current-summer buffer (unary-scaling case)



$Z_{in} \approx 0$

Buffer input impedance (V_{in} / I_{in})



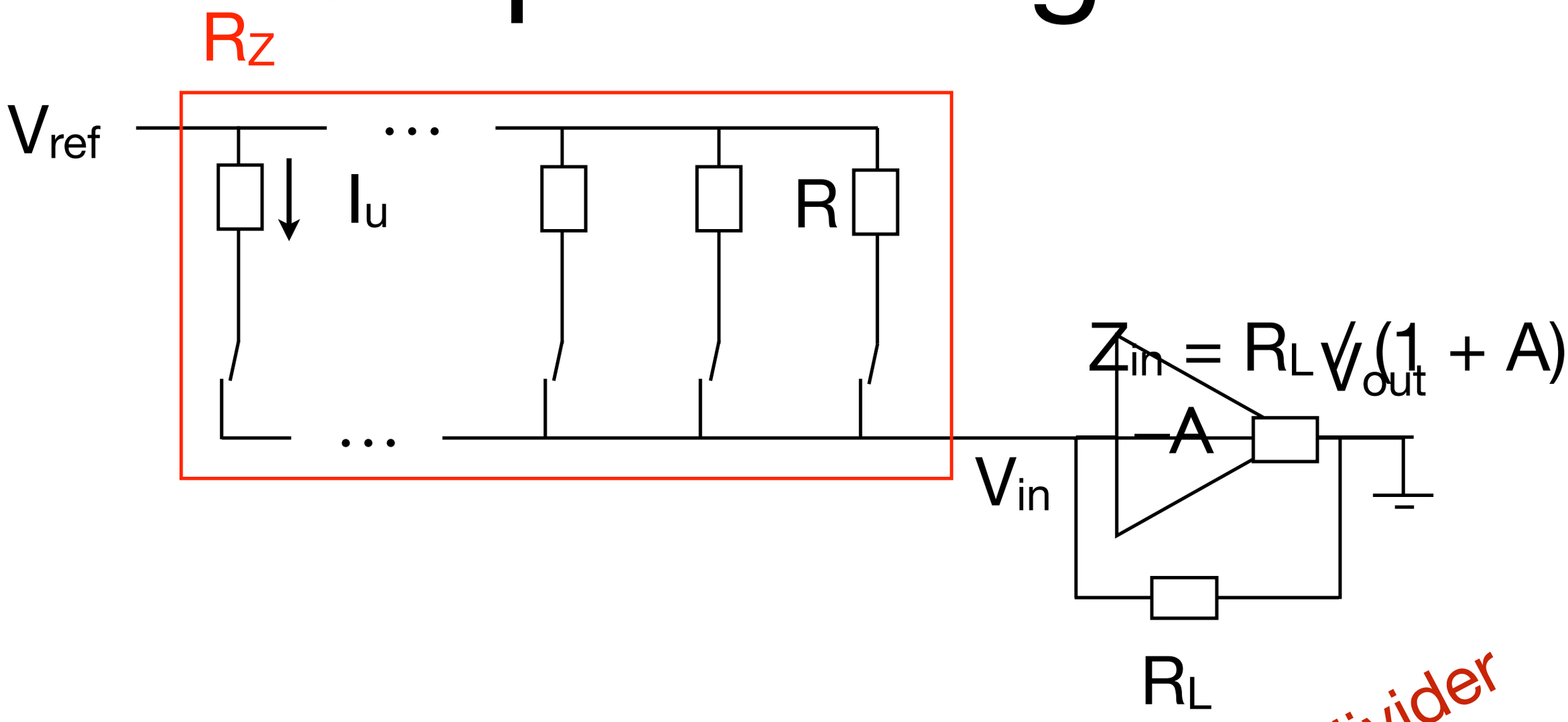
$$Z_{in} = V_{in} / I_{in}$$

$$I_{in} \cdot R_L = V_{in} \cdot (1 - (-A))$$

$$Z_{in} = V_{in} / I_{in} = R_L / (1 + A)$$

Large A means lower Z_{in}

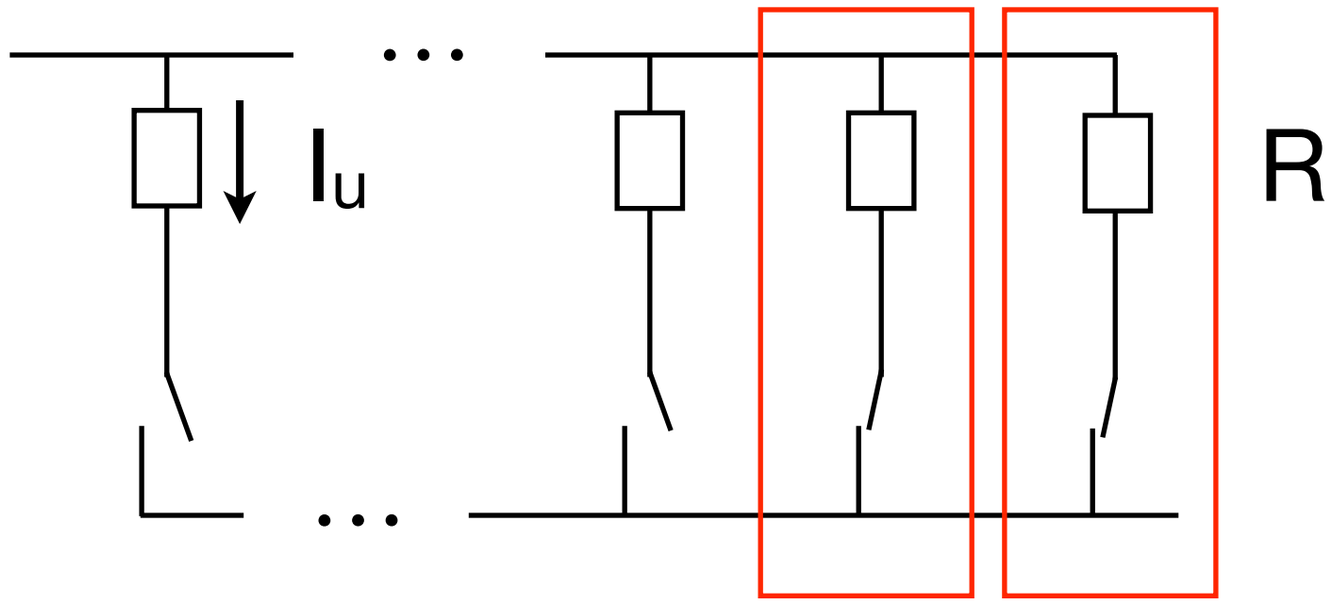
Output voltage



- $V_{out} = -A \cdot V_{in}$
- $V_{in} = V_{ref} \cdot (Z_{in} / (Z_{in} + R_Z))$

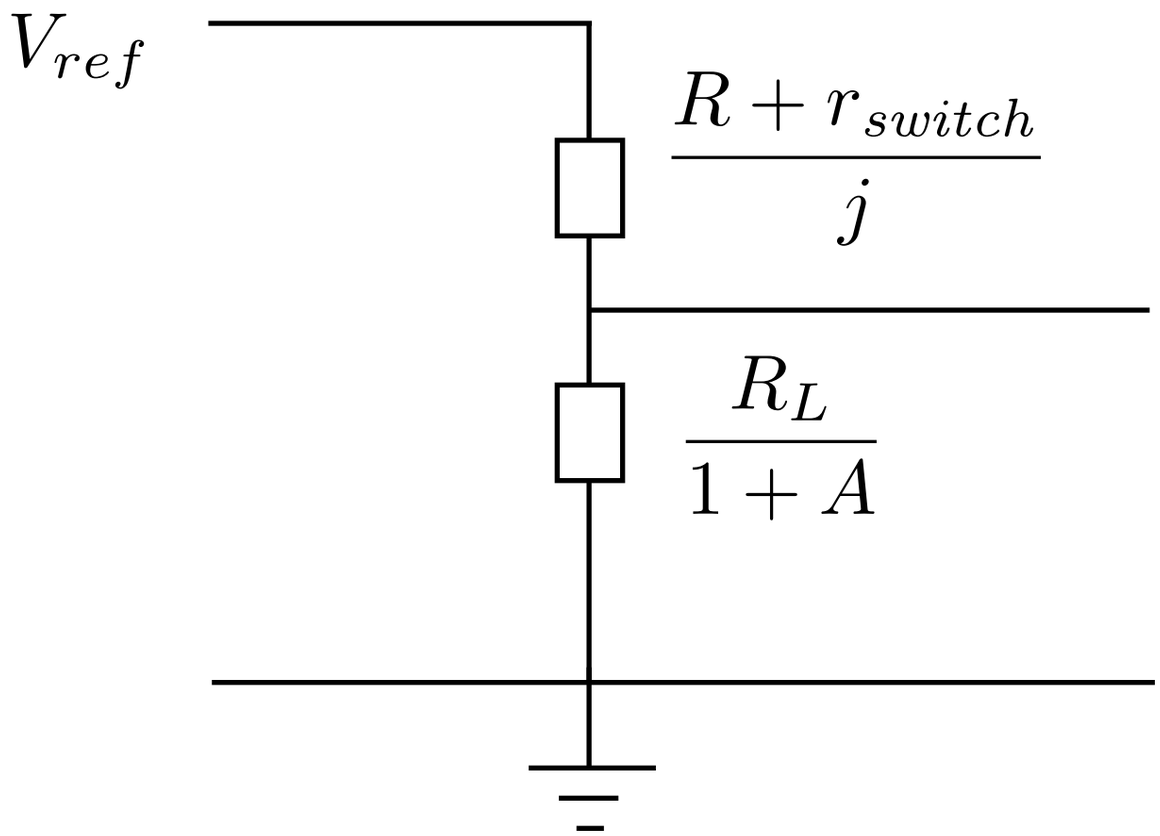
Voltage divider

Impedance of switched R_i



- Each branch: $R + r_{switch}$ (uniform)
- j connected branches: $(R + r_{switch}) / j$
  - Total impedance depends on j!

Voltage divider

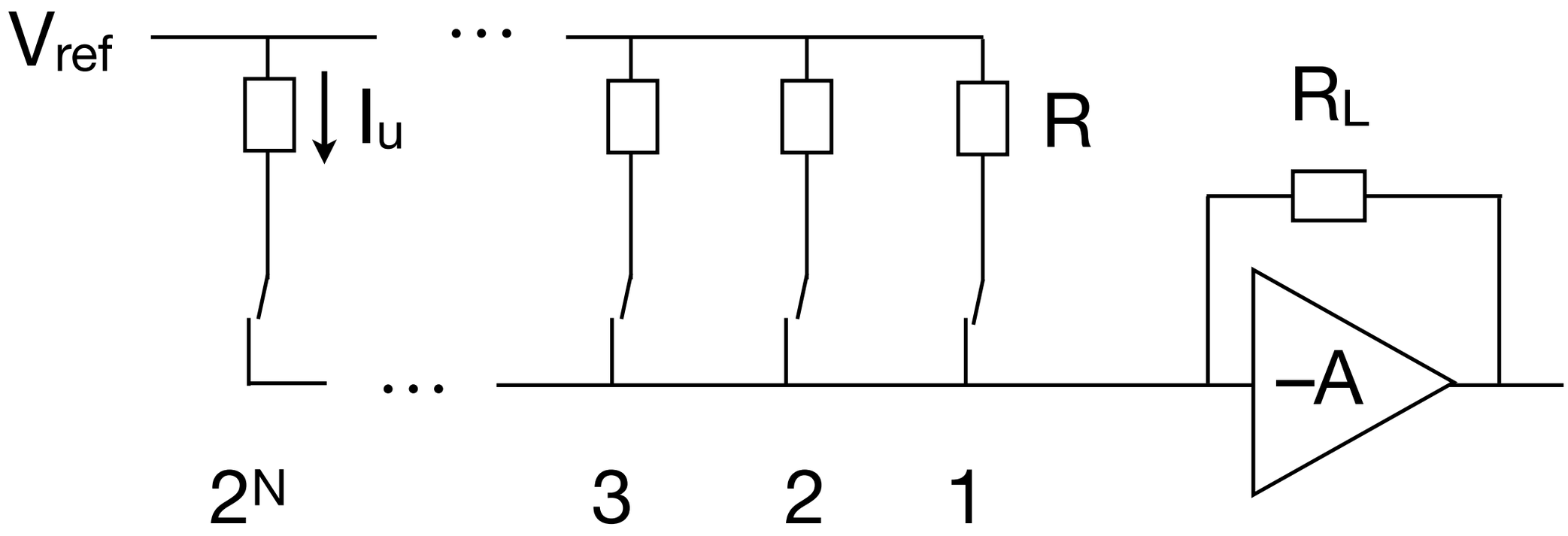


$$V_{ref} \frac{j \cdot R_L}{(R + r_{switch})(1 + A) + j \cdot R_L}$$

- Output voltage not linear in j!
- INL! Harmonic distortion!

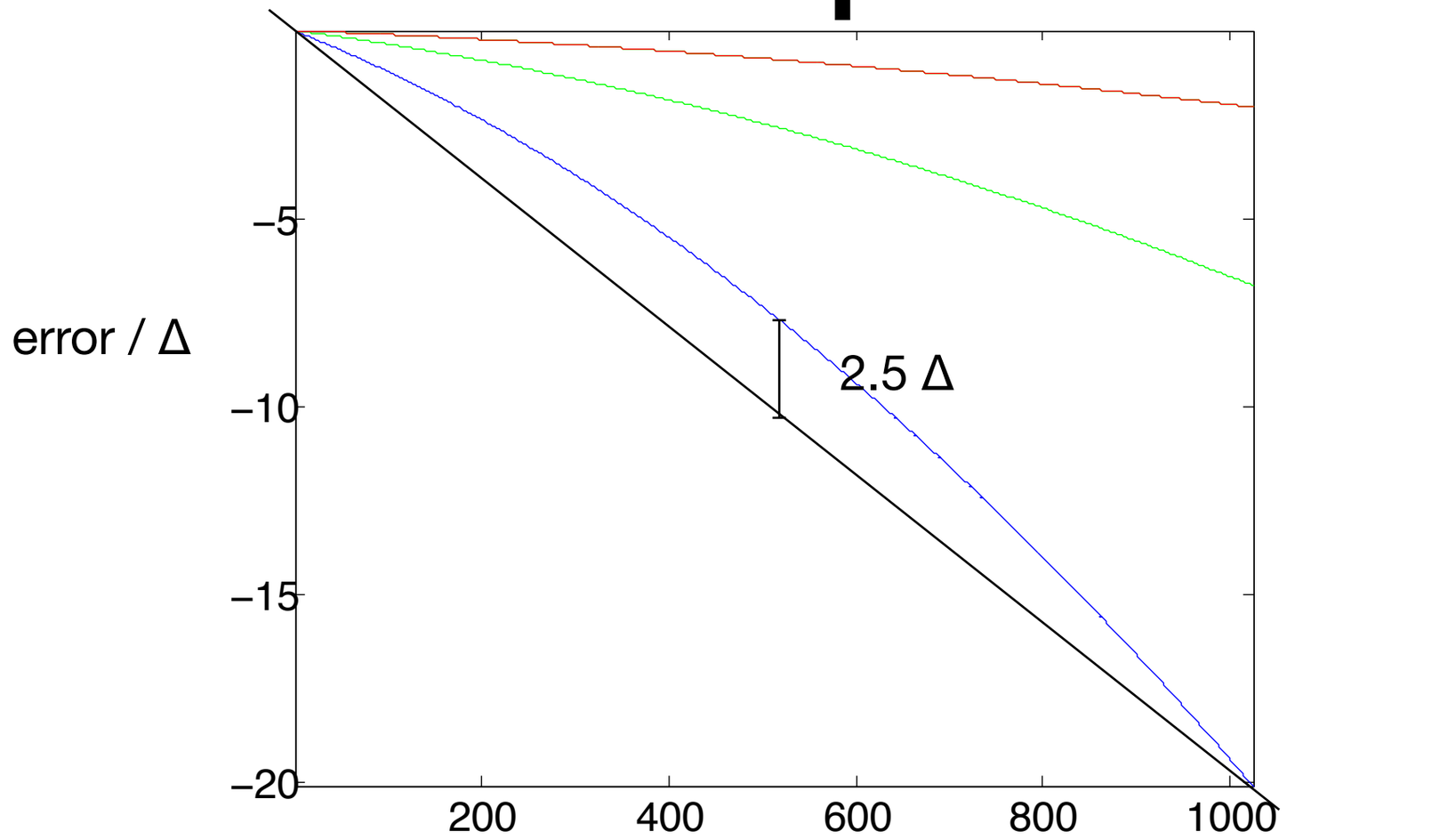
Despite all-linear resistors…

How bad is this?



- Assume that $R_L = R / 2^N$
  - Then, output range is approx. V_{ref}
- Calculate error (vs. $-V_{ref} \cdot j / 2^N$) as function of j

Error plot



- 10 bits, A = 100, 300, 1000
- Gain error + nonlinearity (second order)
- Improves with growing A

$$V_{ref}\frac{j \cdot R_L}{(R + r_{switch})(1 + A) + j \cdot R_L}$$

What to do?

- Reduce buffer Z_{in}, i.e., increase A
  - Costs speed and/or power
- Make branch currents less sensitive to Z_{in}
  - Increase branch Z!
  - Devices with gain can be used to change impedances
    - Cf. Z_{in} of buffer!
    - Costs speed, power, complexity…

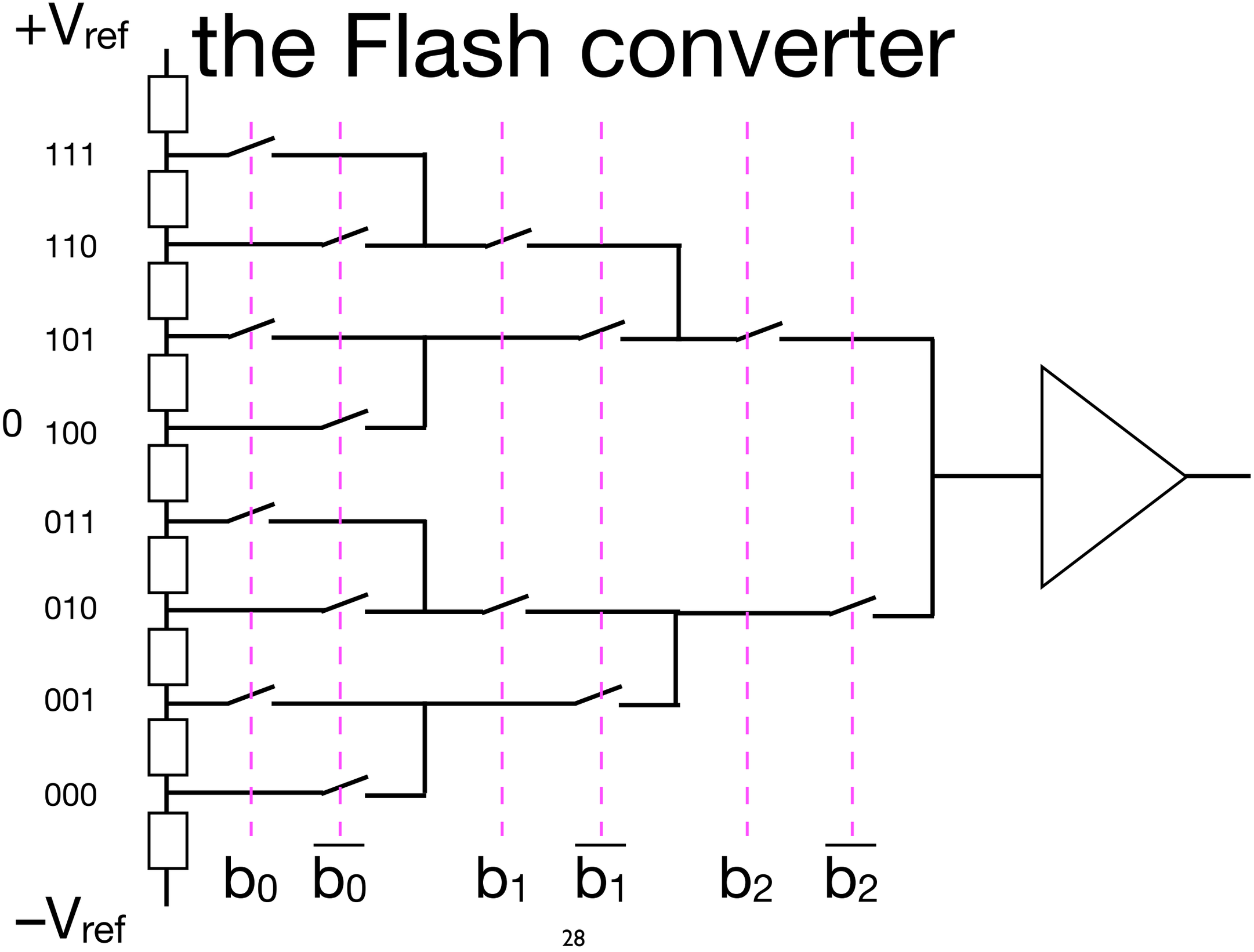
A-to-D conversion

ADC: DAC + compare

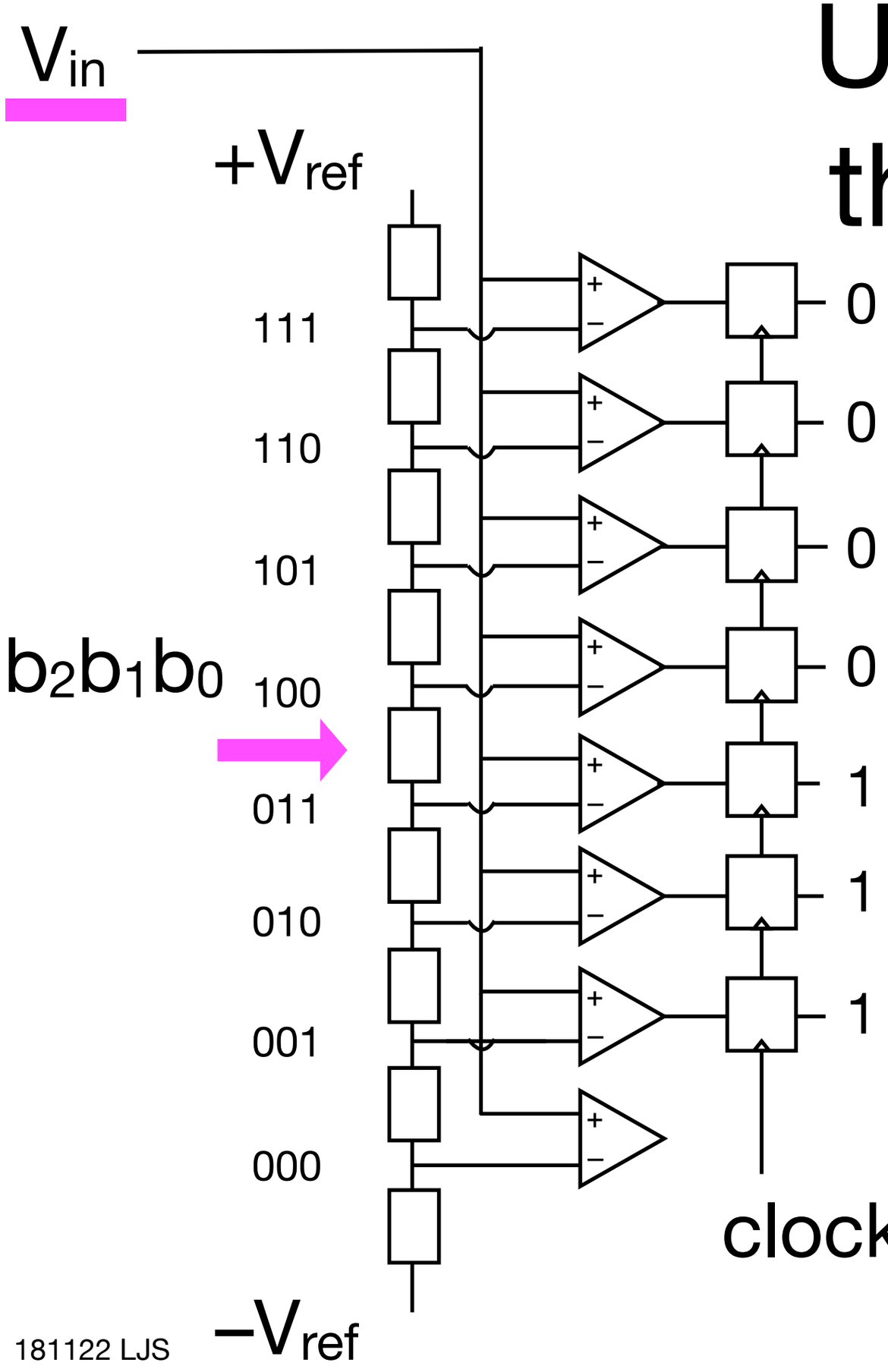
- Typical procedure for A/D conversion:
  - "Guess" a digital value
  - Perform a D/A conversion
  - Compare A/D input with D/A output
  - Adjust if necessary; repeat
- Design decisions:
  - Type of D/A converter
  - How control guess?

Flash converter
Pipelined converter
Successive-approximation converter

Unary-scaling ADC: the Flash converter



Unary-scaling ADC: the Flash converter

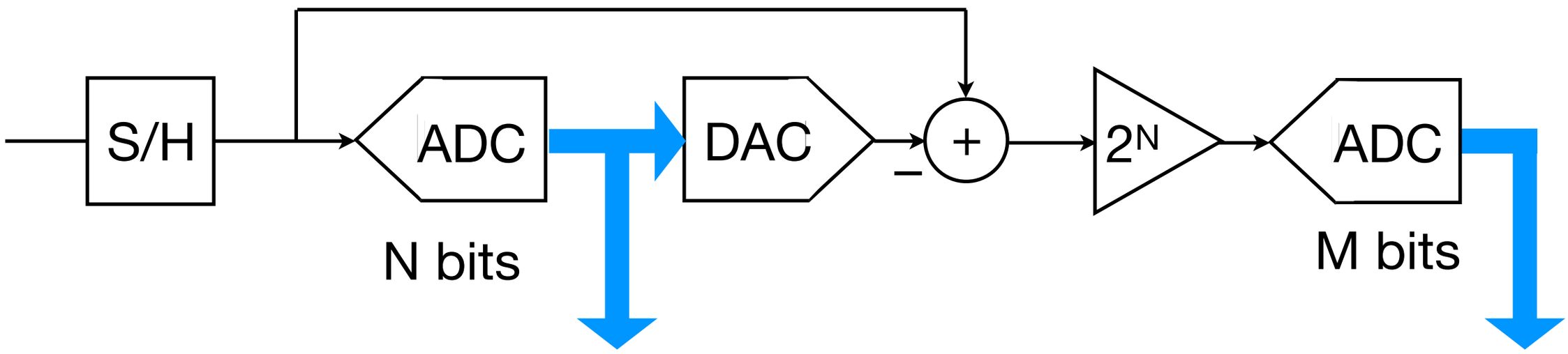


- Compare input with all Kelvin-divider levels in parallel
- Need to re-code digital result: 2^N to N bits
- Cf. thermometer code

Flash ADC properties

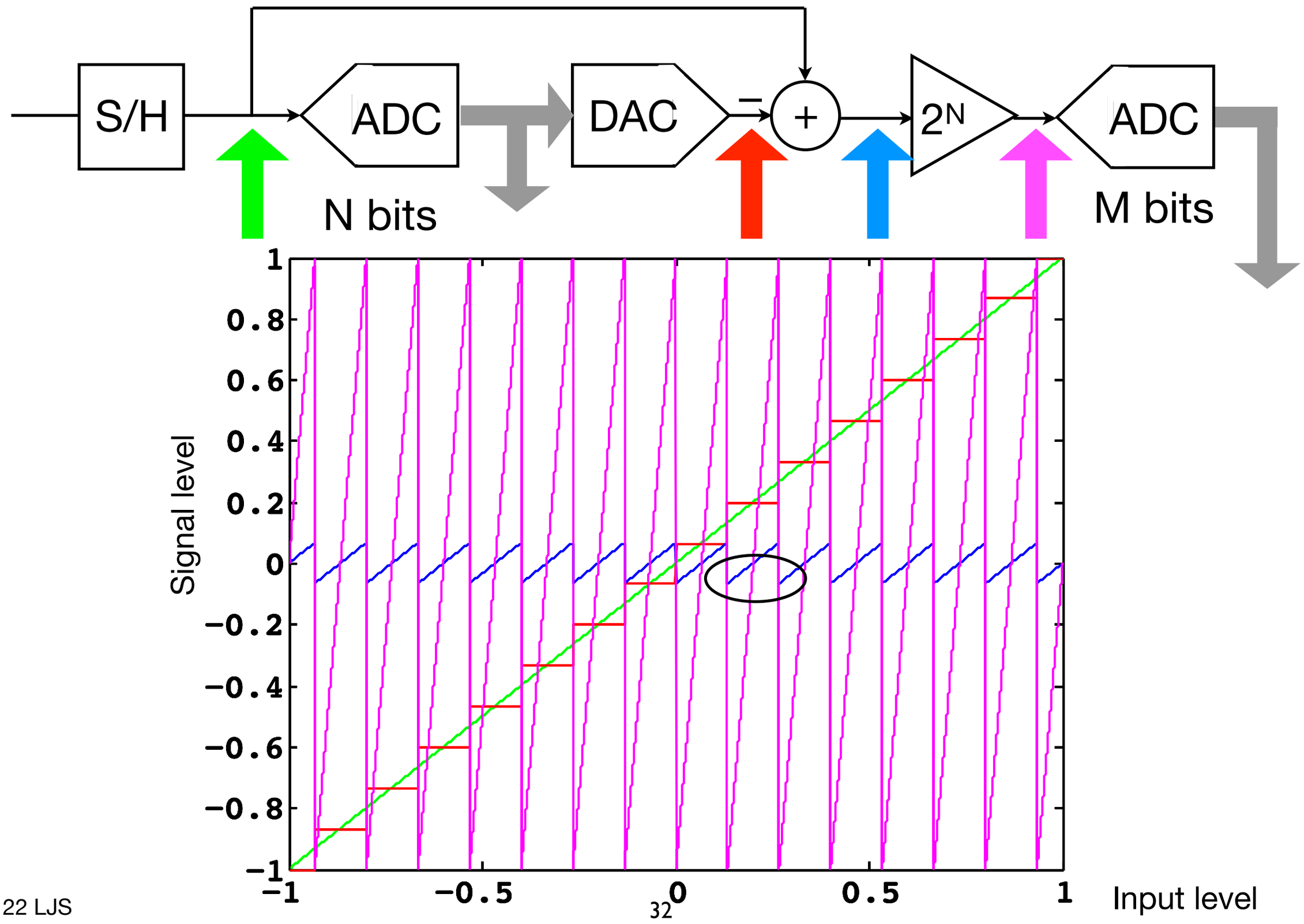
- High speed possible since highly parallel
- Large area since 2^N components
  - Unary scaling!
- High power (2^N components, R string)
- At most ~8 bits, several GHz
  - Limits: input signal distribution, clock distribution, power

Subranging converter

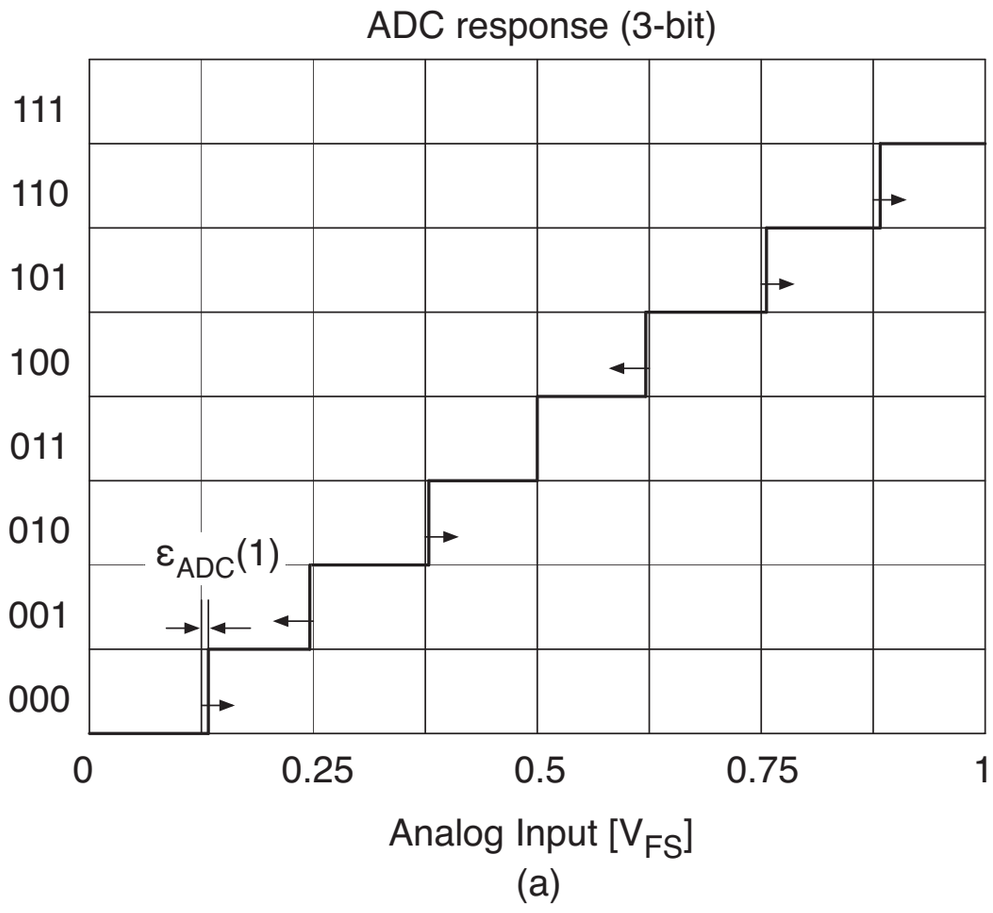


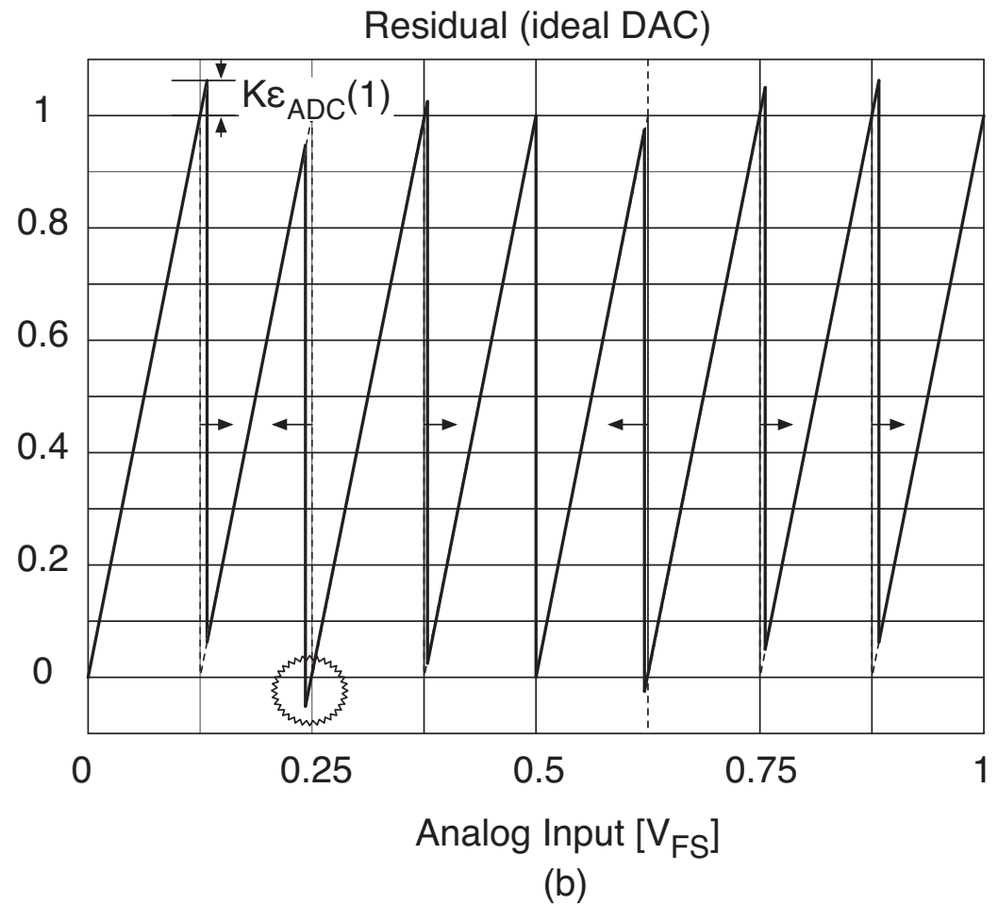
- Two (flash) converters: coarse (N bits) and fine (M bits)
  - Total resolution: N+M bits
- Two-stage conversion

Waveforms


S/H
ADC
DAC
−
+
2^N
ADC
N bits
M bits
Signal level
Input level
1
0.8
0.6
0.4
0.2
0
−0.2
−0.4
−0.6
−0.8
−1
−1
−0.5
0
0.5
1

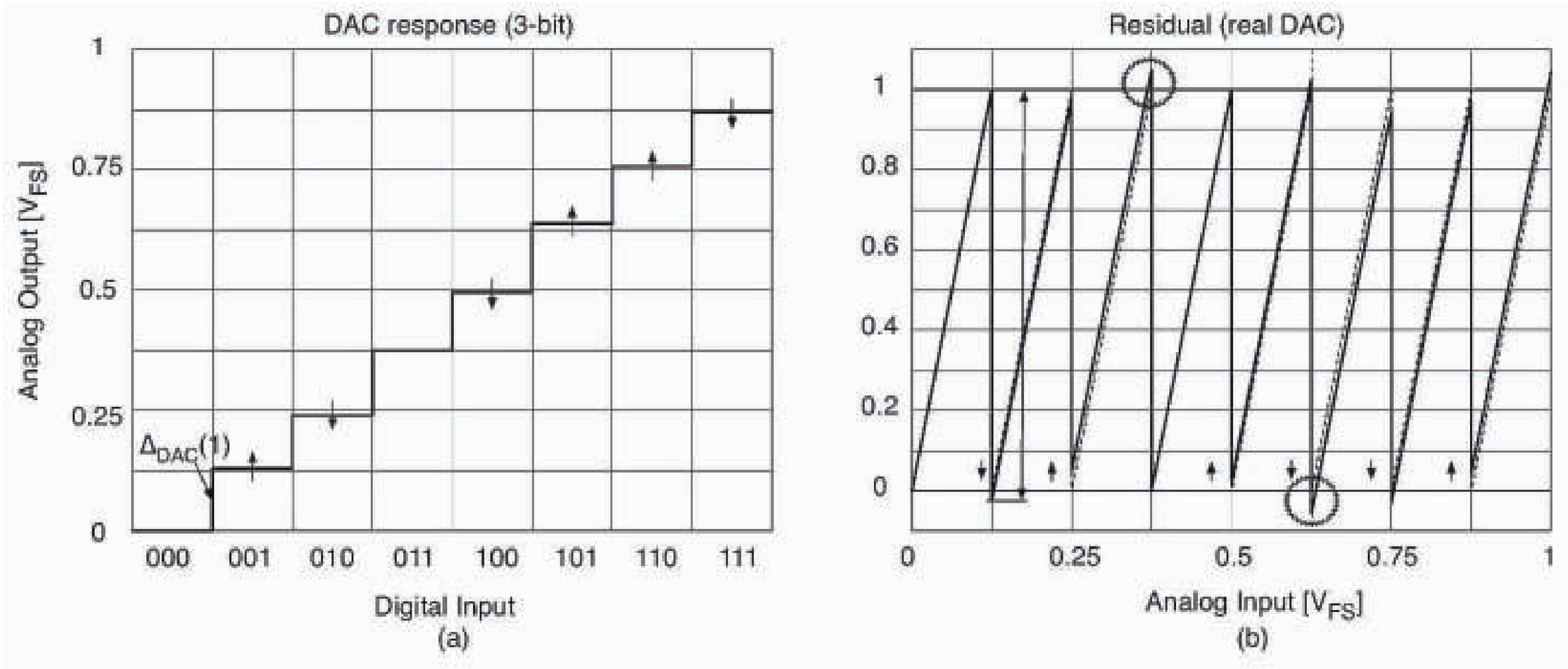
ADC errors





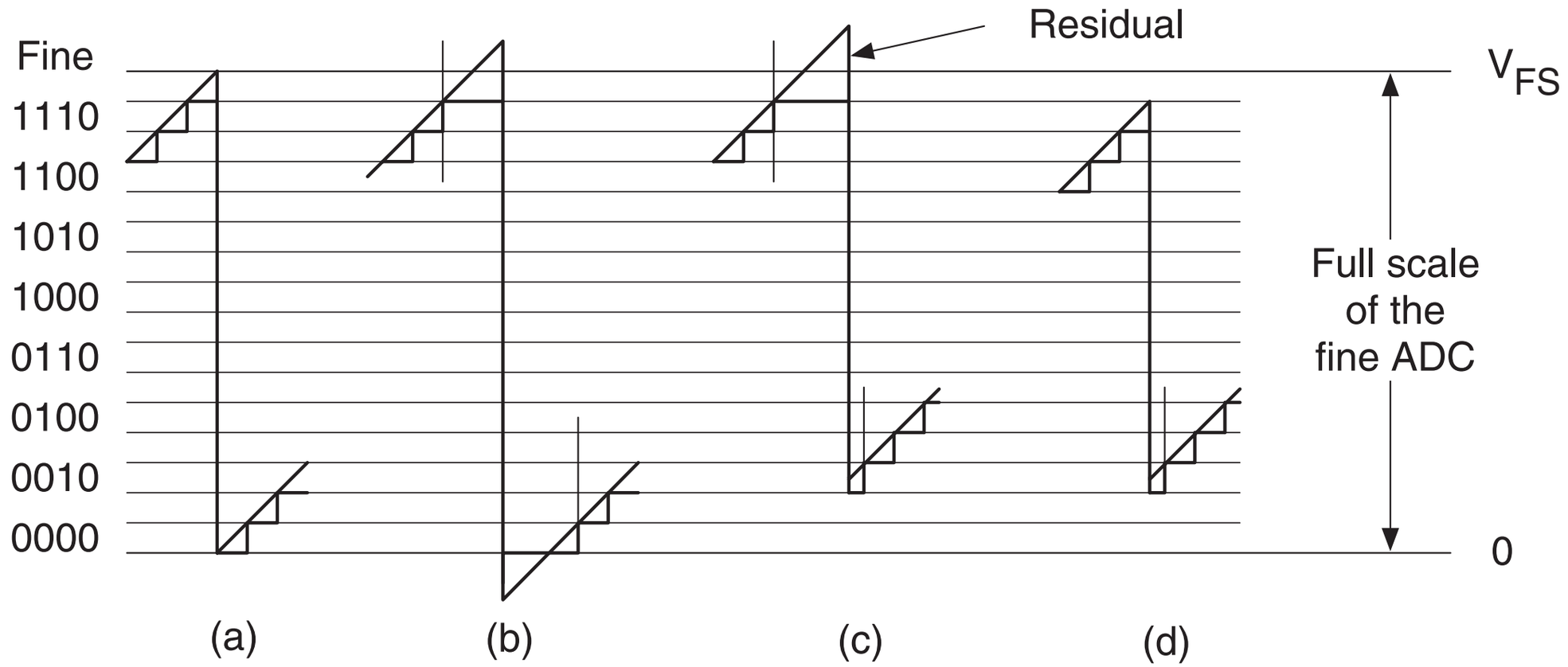
- Vertical lines in residue diagram move sideways

DAC errors



- Angled lines in r.d. move up, down
- Gain errors change slope

Combined errors



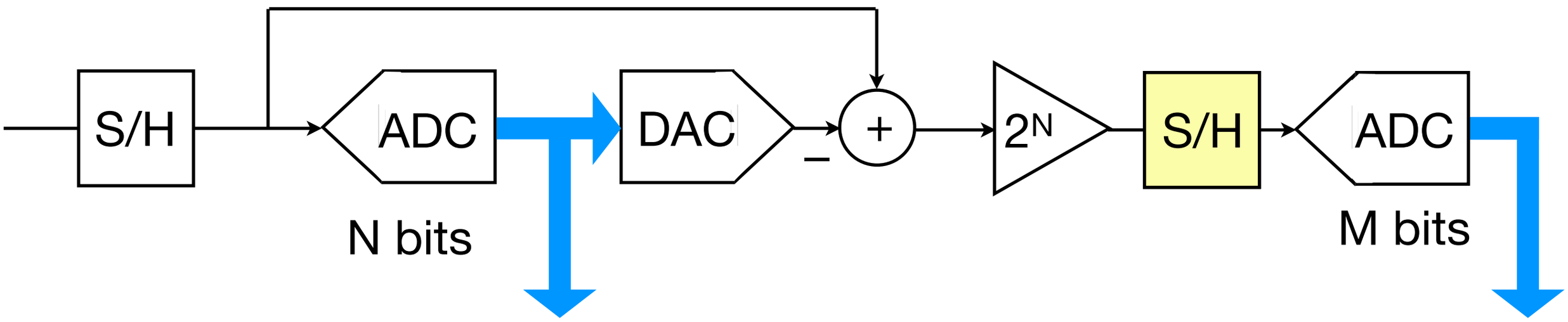
- Missing codes can appear at borders!

Subranging pros + cons

+ Complexity is 2^N+2^M rather than 2^{N+M}
+ Lower-precision first ADC may allow higher speed than one-stage, full-precision ADC

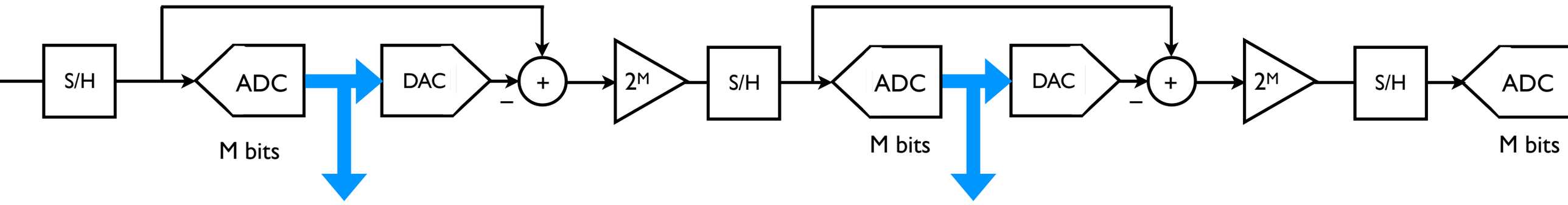
– Increased latency
– High speed requirements at 2nd stage
– 2^N residue amplifier is very critical
  - Missing codes, etc.
  - Can be electronically calibrated (theme 7)

Reduce speed req's



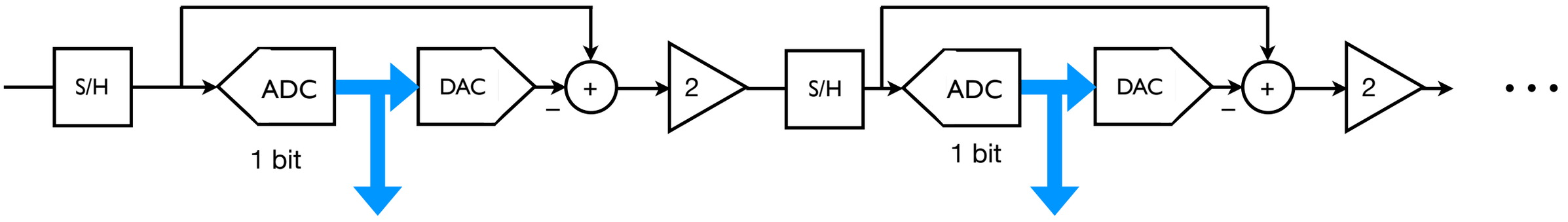
- Pipelining!
- Two samples in process simultaneously
- Need to delay first-stage bits before assembly

Pipelined converter



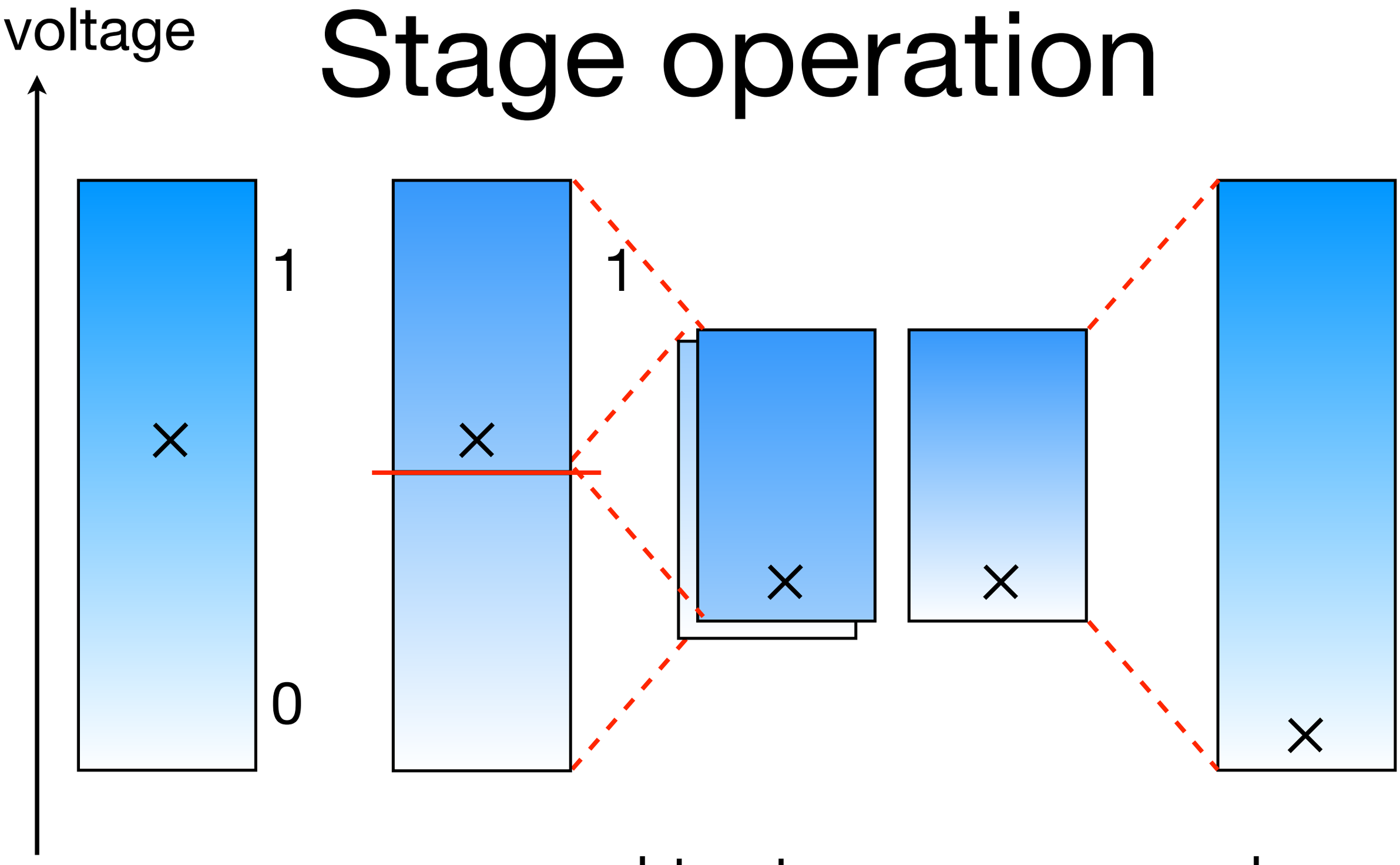
- Three stages (or more…)
  - How to choose # of stages?
- N-bit total precision, M bits/stage
  - (N/M) 2^M comparators — Grows with M
  - N/M amplifiers, S/Hs — Shrinks with M

One-bit-per-stage pipeline

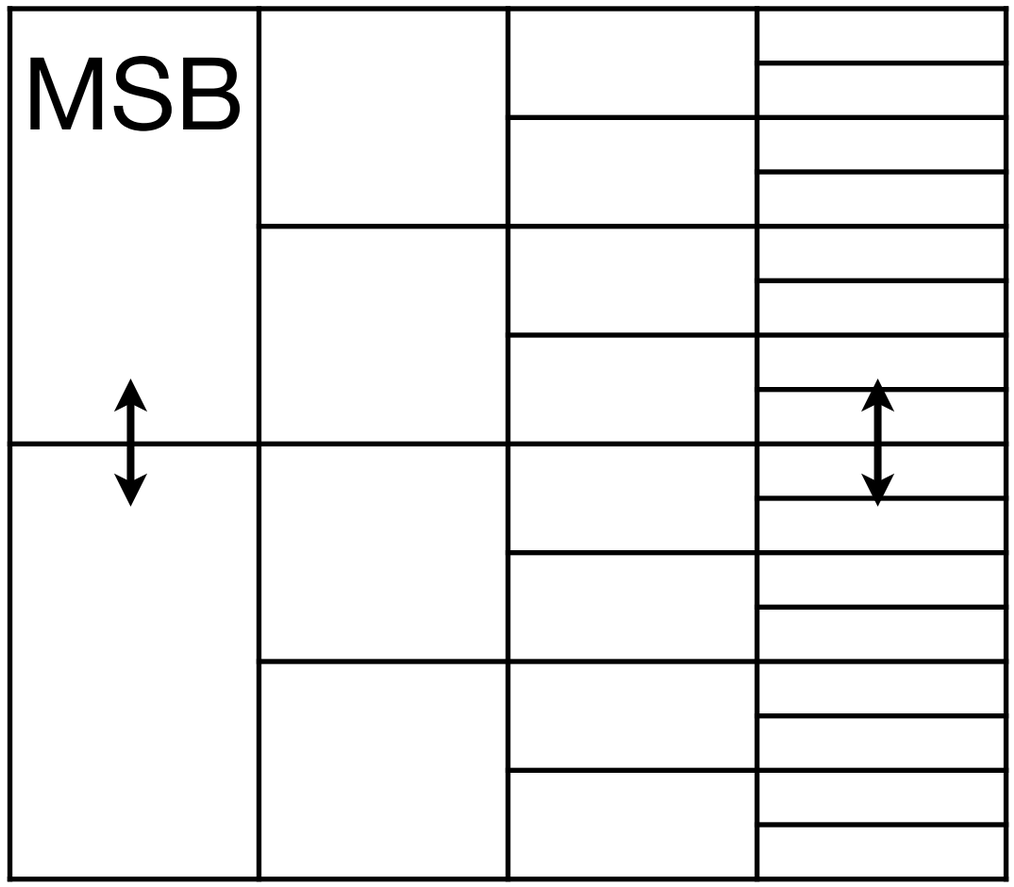


- Take the previous design to its logical extreme 😀
- ADC: comparator, DAC: two switches (to $\pm V_{ref}$)
  - Note: no worries about ADC, DAC non-linearity!
  - Only gain, offset errors

Stage operation

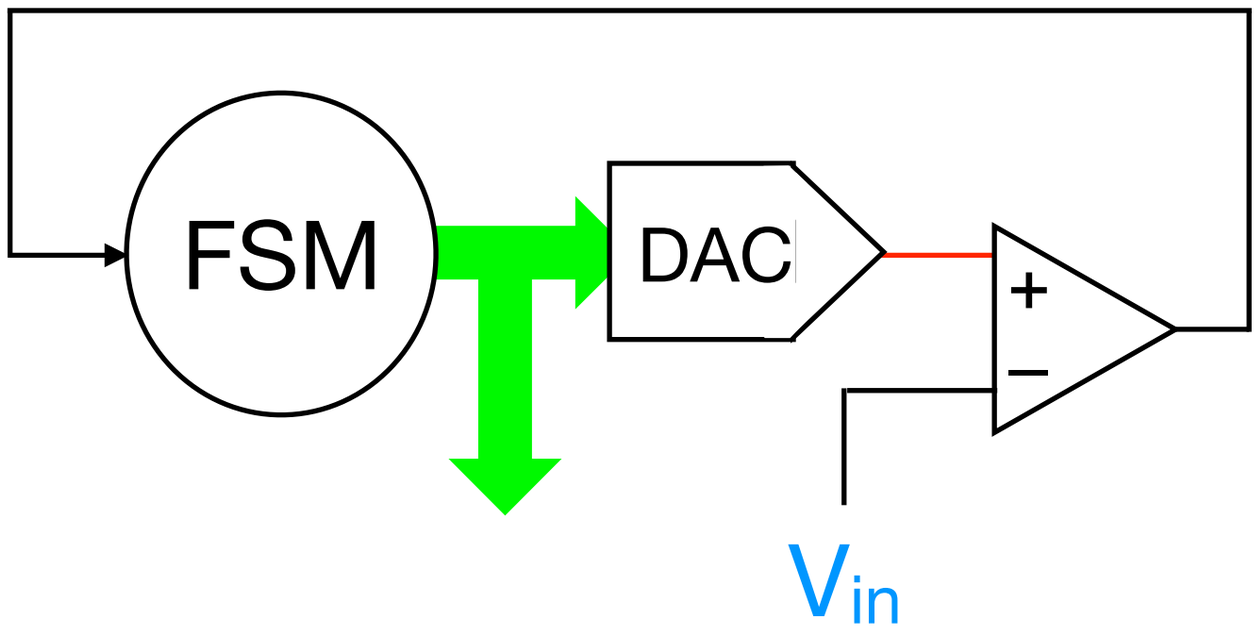


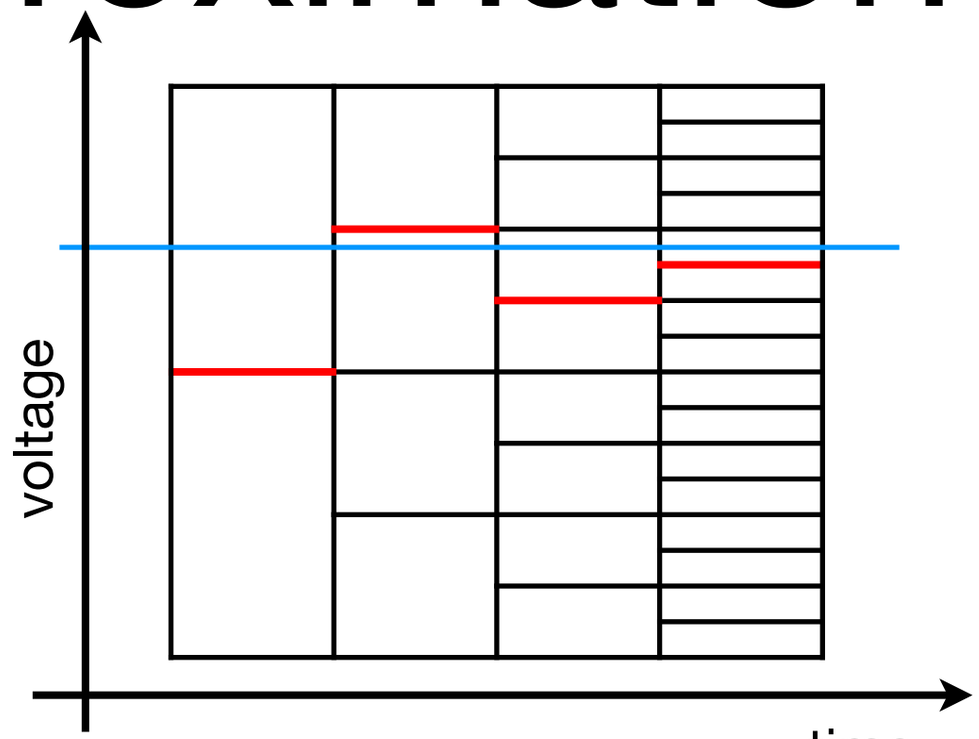
Performance limits



- Comparator offset etc. affects first decision most
  - 1% relative error in MSB means ENOB < 7
- Binary scaling!
  - Compare with R-2R DAC!

Successive approximation





- Simple Finite State Machine sets bits in sequence from MSB downwards, depending on previous bits
  - Search by interval halving / bisection
- One full conversion in N cycles

\+ No subtractions or other analog processing

– DAC needs to be good to N bits!

Low-power opportunities

Summary

- Converter architecture affects properties
  - Reachable resolution
  - Maximum speed
  - Power dissipation
  - …
- Two major classes: unary vs. binary scaling
  - Differ in error characteristics