Power and performance limits

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ADC power limit

- ADC frequently critical component for mixed-signal system
- Fundamental limits on power dissipation
- Some system architectures are not buildable!
- Investigate limit, illustrate with recent data (Murmann; uploaded)

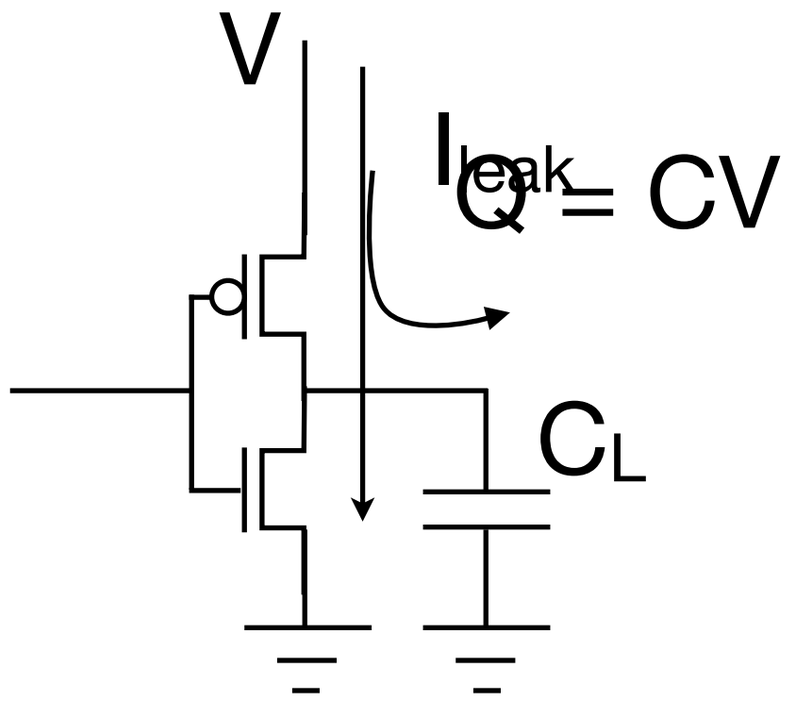
Digital circuit power

- Simple case: inverter + C
- $P_{total} = P_{active} + P_{leakage}$
- $P_{active} \approx \beta_1 \cdot f_{ck} \cdot C_L \cdot V^2$
- $P_{leakage} = I_{leak} \cdot V$

  $\approx \mu \cdot I_{sat} \cdot V$

  $\approx \mu \cdot (C_L V / (t_{ck} / \beta_2)) \cdot V$

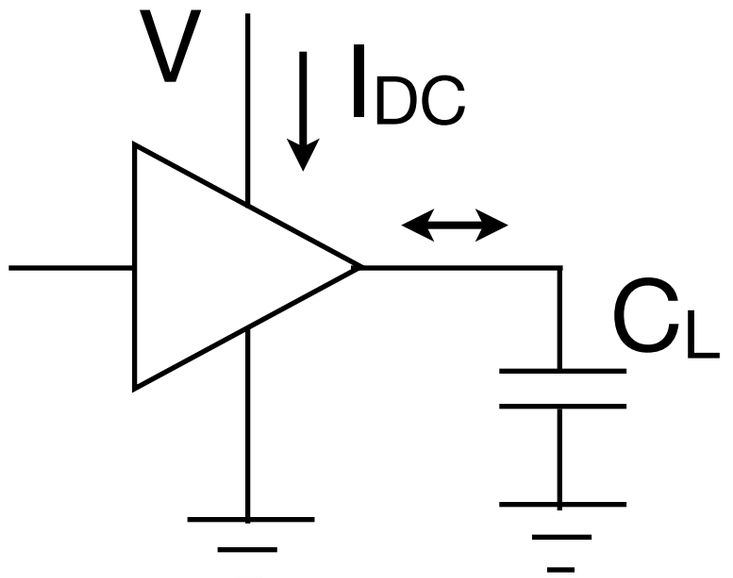
  $\approx \mu \cdot \beta_2 \cdot f_{ck} \cdot C_L \cdot V^2$



Reduction: keep C_L, V, f_{ck} small

Analog circuit power

- Simple case: “class-A” driver circuit
- Constant current draw
  - Then, $P_{analog} = I_{DC} \cdot V$
  - I_{DC} chosen according to load
  - If capacitive load C_L, must be able to cover swing in one cycle (slewing)
  - So, $P_{analog} = I_{DC} \cdot V \approx (C_L V / \beta_3 t_{ck}) \cdot V$ $= f_{ck} \cdot C_L \cdot V^2 / \beta_3$



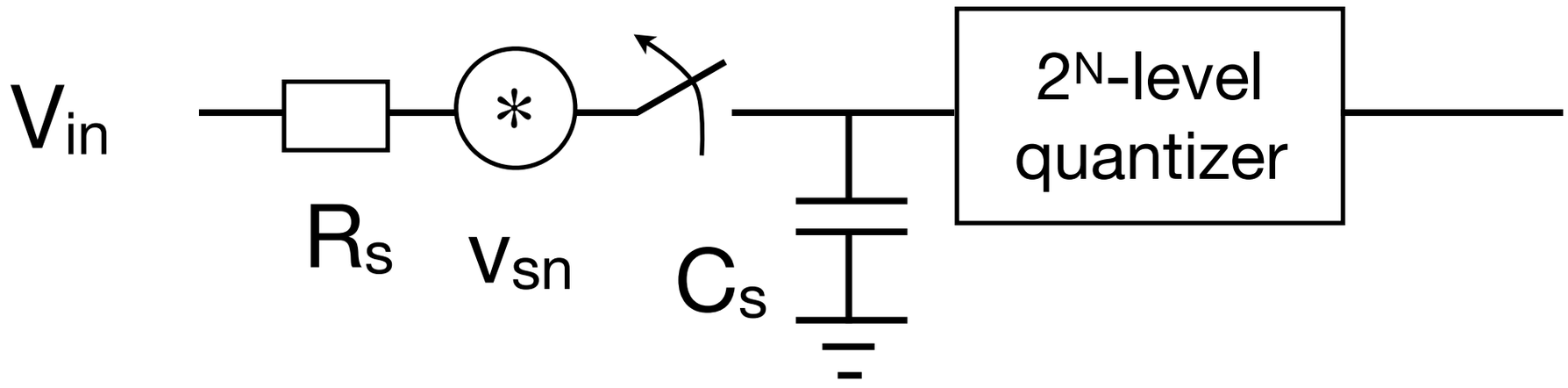
Reduction: keep C_L, V, f_{ck} small

[Assuming rail-to-rail swing]

Limits?

- Minimum f_{ck} set by signal bandwidth (Nyquist etc.)
- Minimum V set by performance requirements
  - Switching speed, analog bandwidth
  - … so ultimately by signal bandwidth…
- C remains!
  - How small can it be?

Recall sampler kT/C noise



- v_{sn} in series with V_{in}
  - V_{in} + v_{sn} sampled on capacitance

$$\overline{v_{sn}^2} = kT/C_S$$

- Need large C_S for low $\overline{v_{sn}^2}$
  - Cost: area, power

Recall quantization noise

- Quantization noise depends on resolution

$$\overline{v_{qn}^2} = \Delta^2 / 12 = (V_{FS} / 2^N)^2 / 12$$

  - Need high resolution for low quantization noise
    - Cost: Component count, area, and/or clock rate

Noise addition

- Uncorrelated noise powers may be added
- Adding sample noise and quantization noise:

$$v_{ntot}^2 = v_{sn}^2 + v_{qn}^2$$

- No use overdesigning either term!
  - Cost for diminishing benefit

- Yes, there are more noise sources…
  - …but let's keep it simple for now…

A good choice for C_S

- Assumption: balanced design when $v_{sn}^2 = v_{qn}^2$; then:

$$v_{sn}^2 = kT/C_S$$

$$v_{qn}^2 = (V_{FS} / 2^N)^2 / 12$$

$$kT/C_S = (V_{FS} / 2^N)^2 / 12$$

- C_S expressed in V_{FS} and N:

$$C_S = (12\ kT /\ V_{FS}^2) \cdot 2^{2N}$$

C_S values

$C_S = (12\ kT / V_{FS}^2) \cdot 2^{2N}$ Factor 4 per bit (16 per 2 bits)

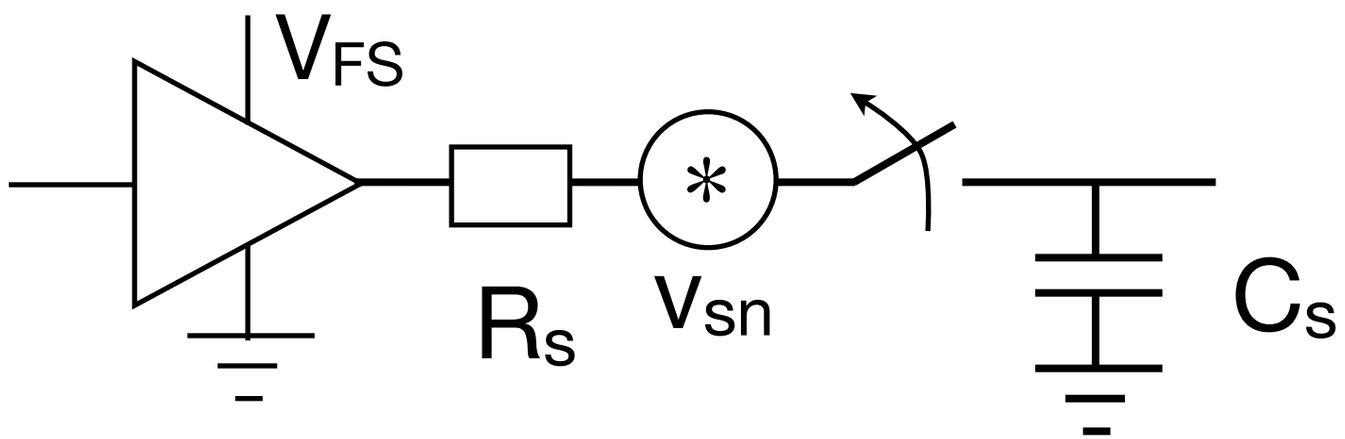
N	C_S
4	13 aF
6	0.2 fF
8	3 fF
10	52 fF
12	0.8 pF
14	13 pF
16	214 pF

High sample cap cost at high end!

On-chip example:

- 0.18 µm process
- V_{FS} = 1.0 V
- Gate cap of smallest transistor: ~0.9 fF
  - C_S will not limit performance below 8 bits
- 13 pF ~ 6000 µm²
  - SRAM: ~100 µm² /bit

What drives the sampler?



- Sample capacitance is load of some analog circuit!
  - Simple assumption: class-A driver, best efficiency
- $P_S = f_S \cdot C_S V_{FS}^2 = f_S \cdot ((12\ kT / V_{FS}^2) \cdot 2^{2N}) V_{FS}^2$

  $= 12\ kT\ f_S\ 2^{2N}$

  Independent of V_{FS}!
- Power needed to drive minimum C_S across full range from one sample to the next
  - O/w full amplitude cannot be reached at Nyquist!

Examples

$$P_S = 12\ kT\ f_S\ 2^{2N}$$

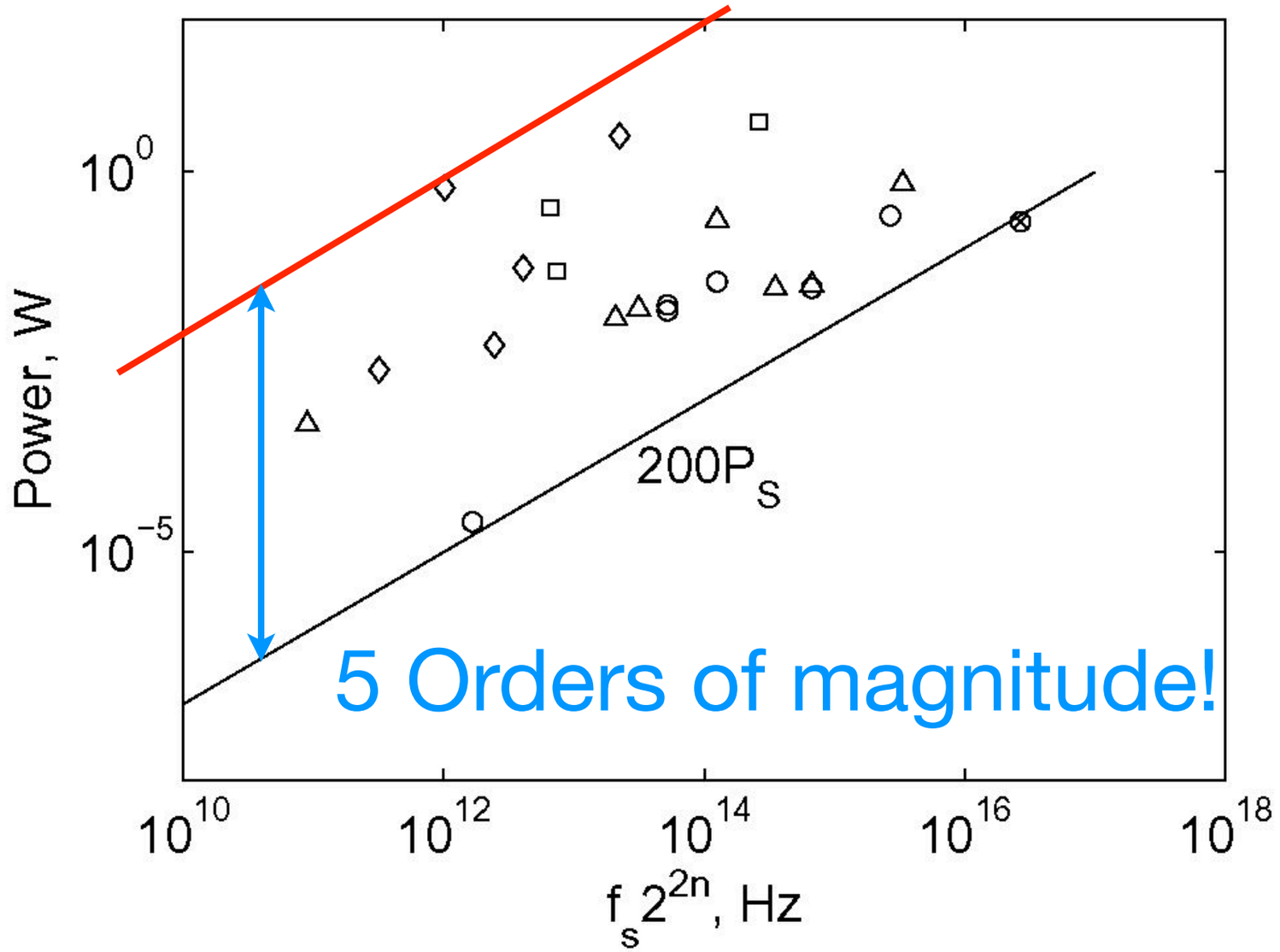
$$[k = 1.38 \times 10^{-23},\ T = 300]$$

- 10 bits, 10 MS/s: P_S = 0.5 uW
- 14 bits, 100 MS/s: P_S = 1.3 mW
- 18 bits, 1 GS/s: P_S = 3.4 W
- 24 bits, 50 GS/s (from teaser video): P_S = 70 kW

Absolute vs practical?

- $P_S = 12\ kT\ f_S\ 2^{2N}$ is "limit" for power!
  - …under certain assumptions…
    - Note: limit of "sample power" only!
    - Rest of ADC needs power too
    - Total power necessarily <u>larger</u> than P_S
    - Practical state of the art?

Reality check



△,○: Pipelined

□, ◇: Flash

High-speed converters

ISSCC 2002, 2006

[Svensson, Andersson, Bogner, NorChip 2007]

Performance points

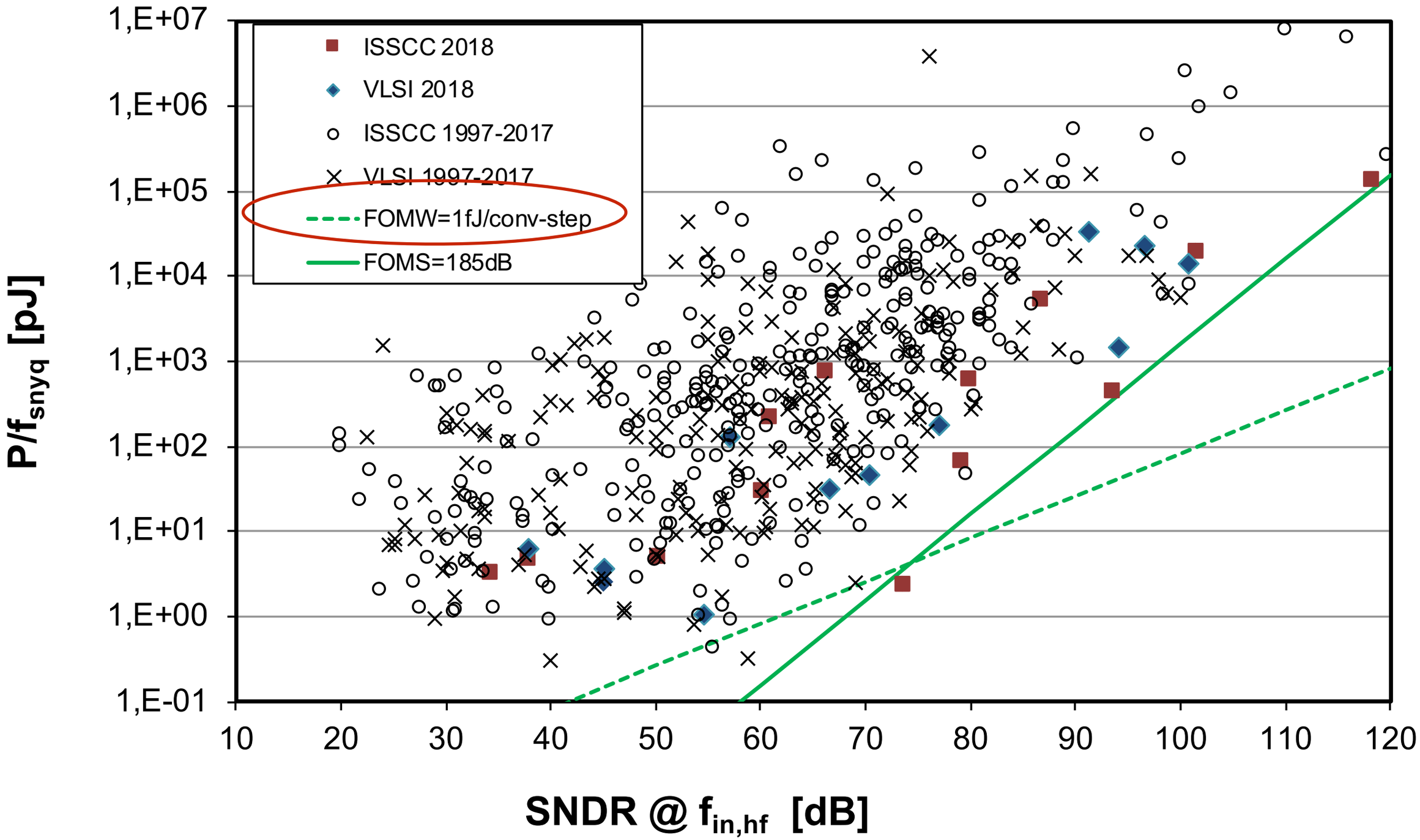
- $P / P_S = 200…20000000$ for exceptional, high-speed converters (in 2006)… but:
  - What about lower speeds?
  - Does resolution matter?
  - What happens with technology progression?
- Can we find some common Figures of Merit (FoMs) to compare different ADC designs?

Example FoM

- Compare converter designs wrt power
  - Compensate for f_S, SNDR
    - Low f_S: should be cheap
    - Low SNDR: should be cheap
  - FoM = P / ($f_S \cdot 2^{ENOB}$) [or similar expression; see Maloberti chap. 2]
    - Loosely, energy per “conversion step”
    - Low FoM values are better!
- Applied to 537 excellent designs (ISSCC, VLSI Symposium, 1997 – 2018)

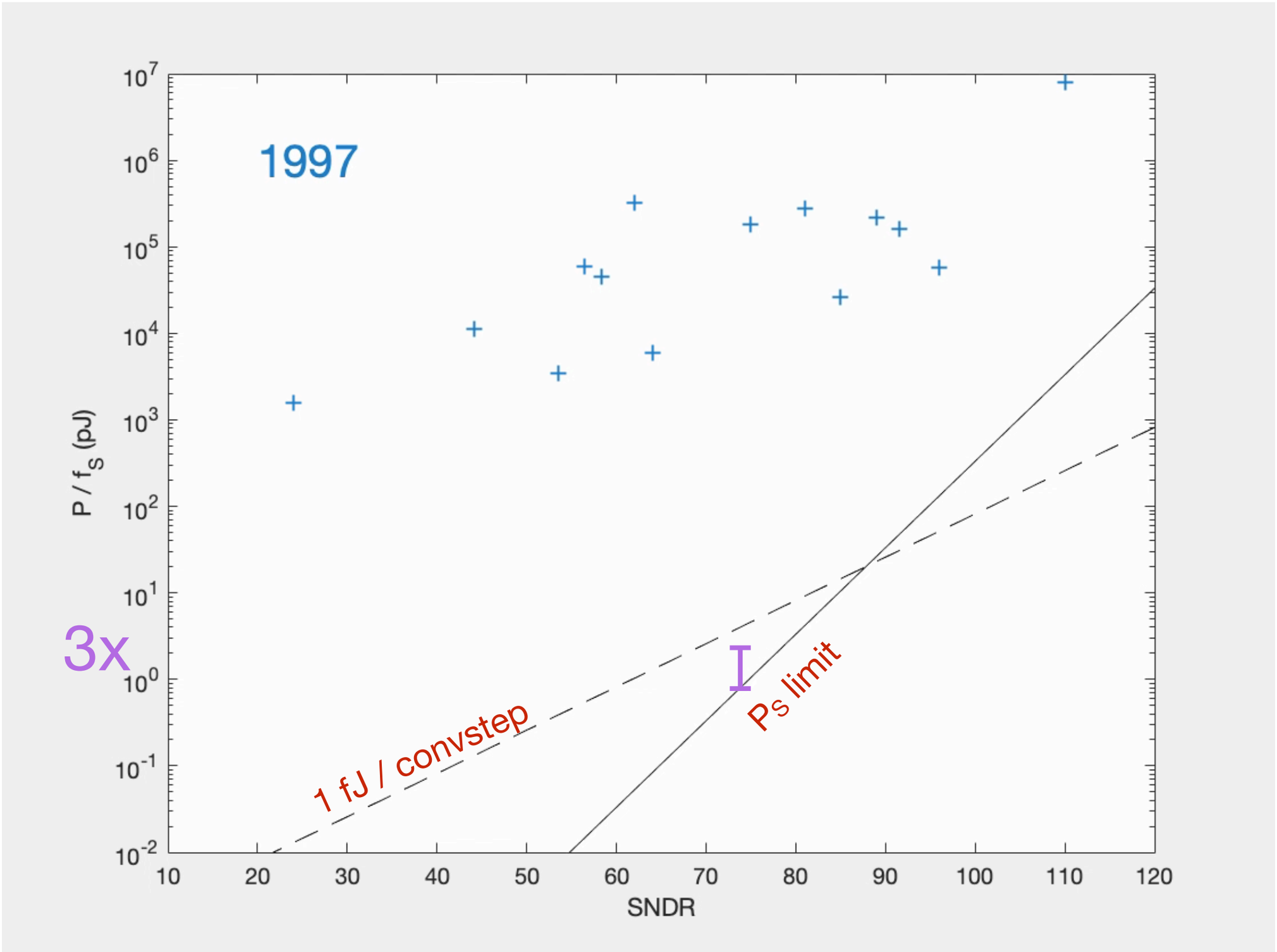
ENOB = (SNDR – 1.76) / 6.02

ISSCC+VLSIS FoMs



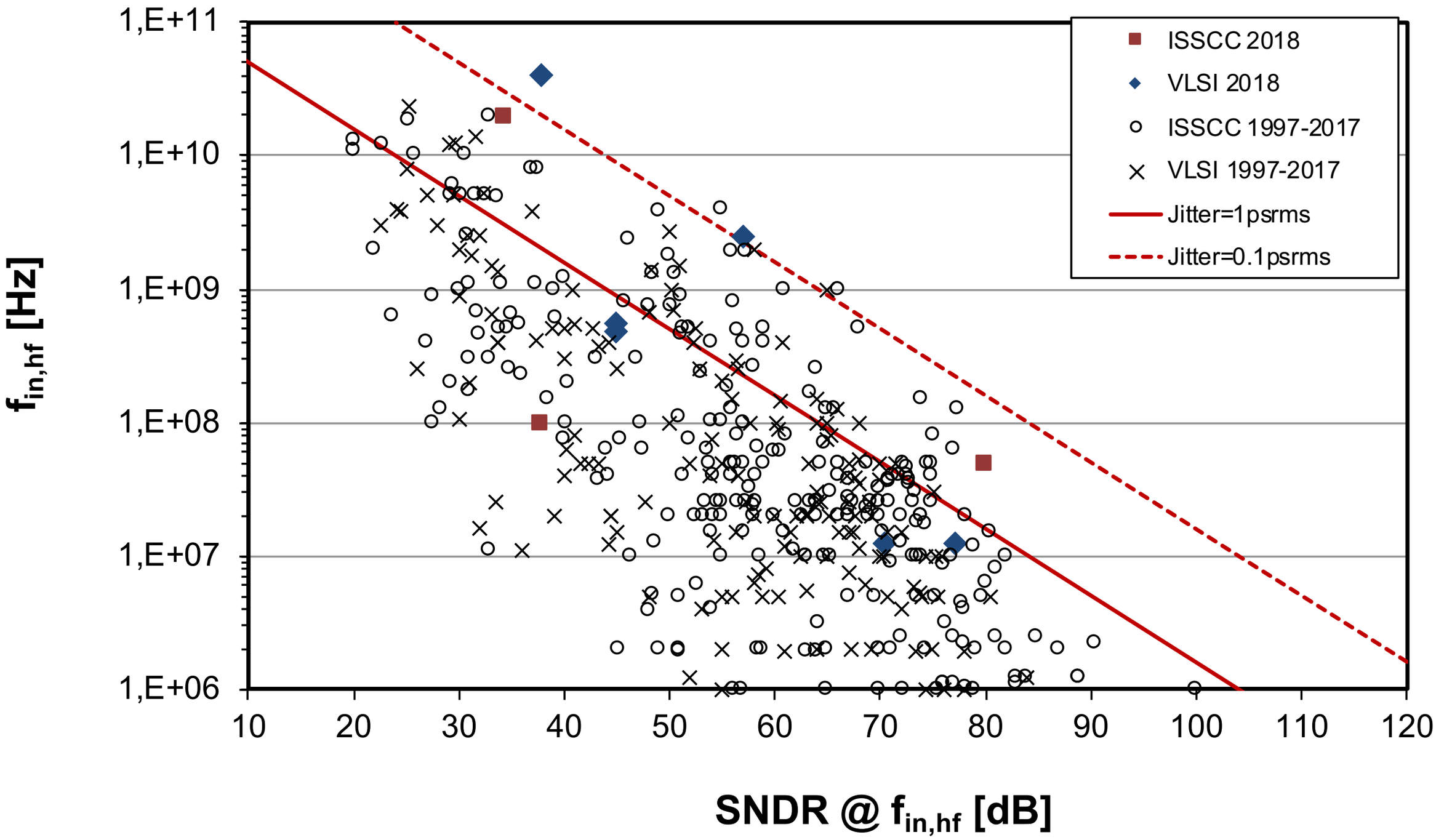
[Murmann, ADC Performance Survey]

ISSCC+VLSIS FoMs



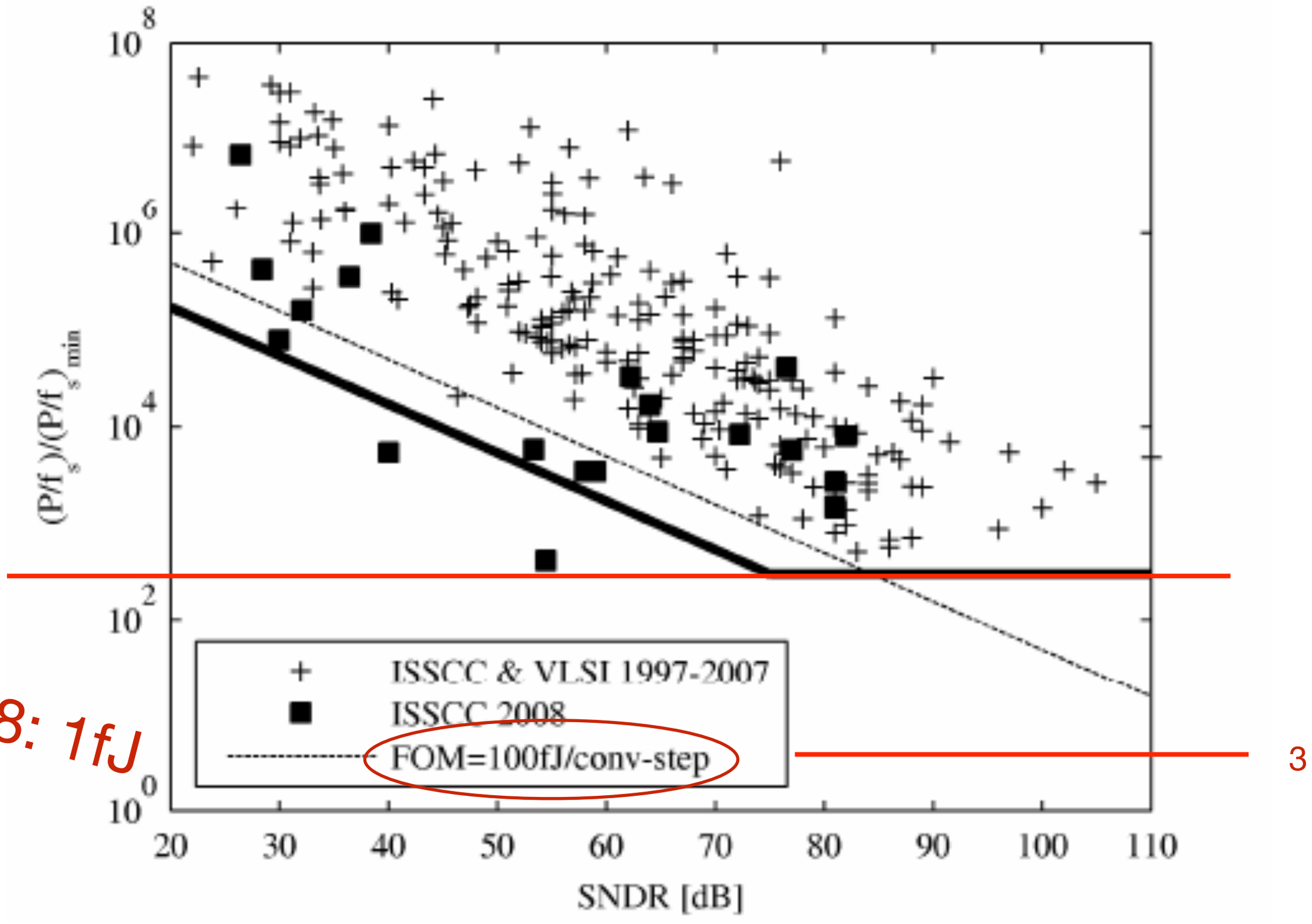
[Murmann, ADC Performance Survey]

Jitter limit



[Murmann, ADC Performance Survey]

Noise limit (2008)



[Murmann, CICC 2008]

E_{ADC} vs E_{NAND}

SNDR (dB)	E_{ADC}	E_{ADC} / E_{NAND}
30	21 nJ	4700
50	168 nJ	38000
70	1.35 uJ	300000
90	10.8 uJ	2400000

- Complete ADC energy per conversion (in 2008) vs energy of one NAND-gate logic transition in 90-nm CMOS
- Digital logic more “affordable” for higher resolutions!
  - Even more in newer technologies
- Increasingly attractive to use digital methods to improve performance!

Later: Digital assist

[Murmann, CICC 2008]

Analog? D/A?

- ADCs show <u>fundamental</u> limits clearly!
  - Other limits (hard/soft) apply elsewhere
- All capacitances show kT/C noise!
  - Filters, oscillators, etc
- For D/As, main problem often matching
  - Addressed by digital means

Summary

- Sample noise sets energy limit on ADCs as we know them
- Present ADCs close in on these limits!
- Future progress likely mostly at lower resolutions
  - Shrinking voltage swing