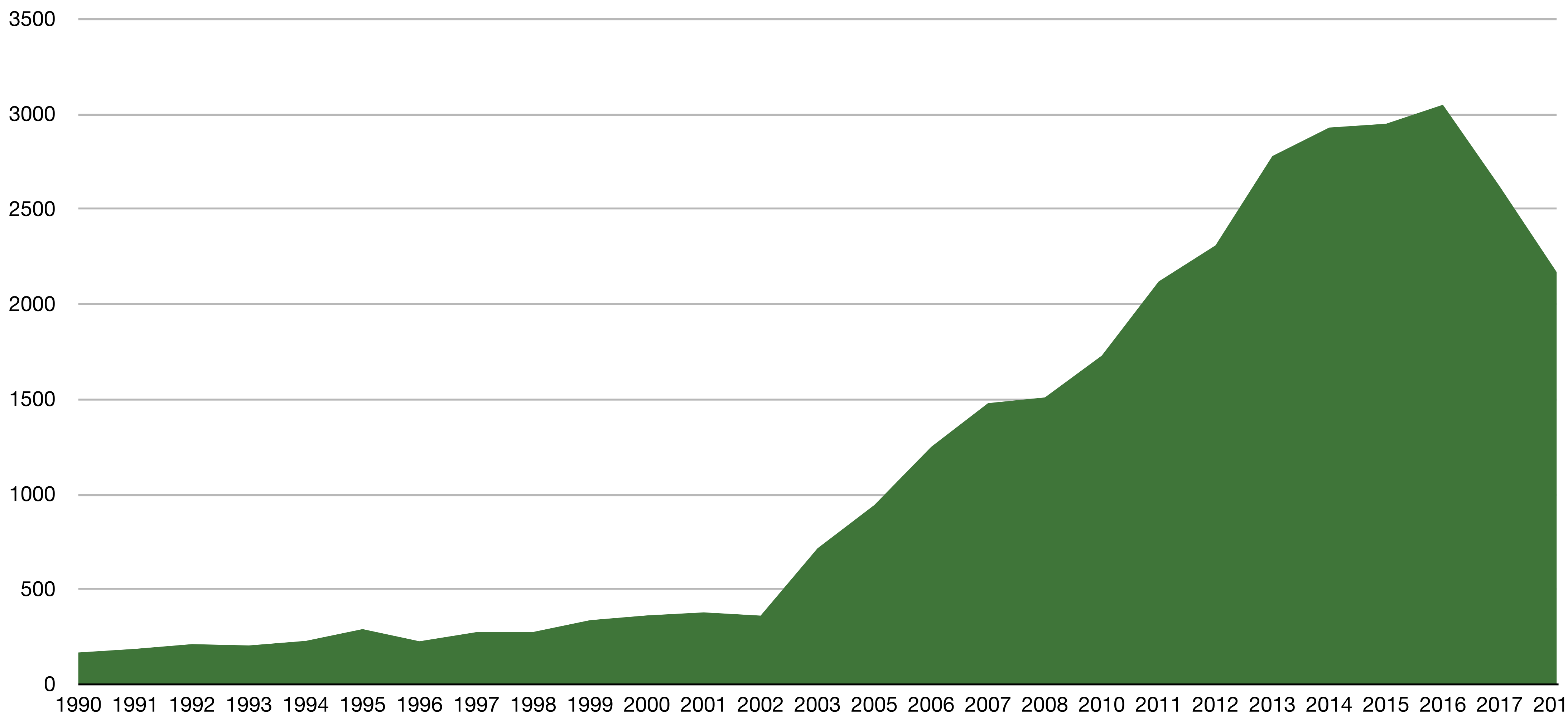
Variability and matching

DAT116, Nov 12 2018
Lena Peterson
Lars Svensson

Preliminary version!

New problem on horizon!?



- Number of hits in Google Scholar for keywords vlsi variability vs. year of publication

Naah. Old news.

- **Analog** design was ever such!
  - Parameter spread of active components:
    - Transistors
    - Amplifiers
    - ...
  - Temperature, aging, …
- Lately, also a problem for **digital** design
  - => Renewed interest!

Dimensions of variability

- Time **independent** vs time **dependent**
  - Time scales
- **Global** variations vs **local** variations
  - Space scales
- **Deterministic** vs **random**

Division of topic

- Monday Nov 12
- Variability and **matching**
    - Transistors, resistors and capacitors
- Thursday Nov 15 (8-10! due to DATE-IT)
    - Variability and **feedback**

Matching - motivation

Digital-to-analog conversion DAC - resistors

Resistors are R and 2R (which can be implemented as R+R)
How to select R?

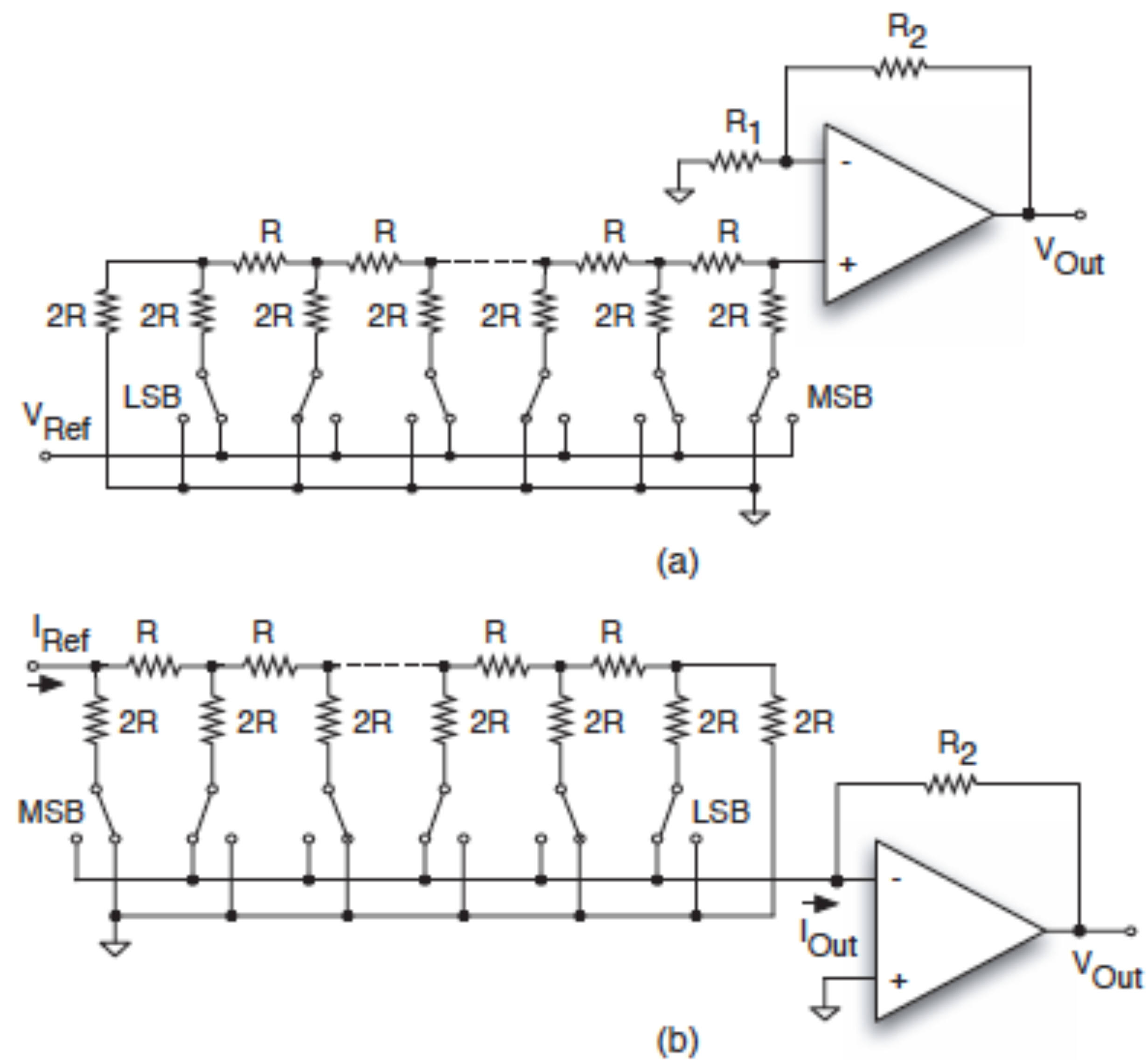


Figure 3.17. (a) Use of the voltage-mode R-2R ladder network. (b) Use of the current-mode R-2R ladder network in an output voltage DAC.

Source: Maloberti Ch. 3

Matching - motivation

Digital-to-analog conversion DAC - capacitors

The spread in C values is due to the number of bits. How large must the unit capacitor C_u be?

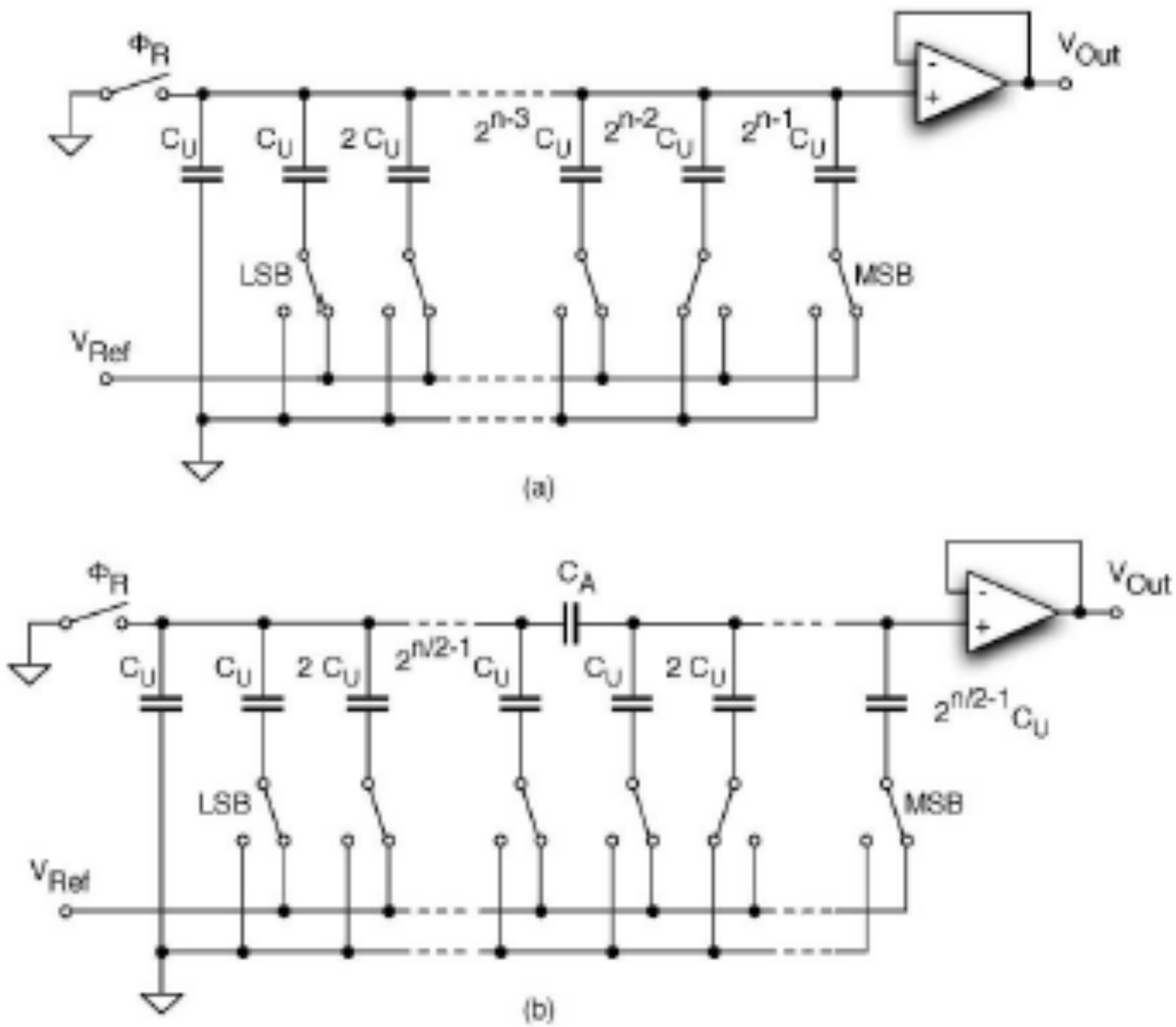


Figure 3.28 (a) n-bit Capacitive divider DAC. (b) The use of an attenuator in the middle of the array reduces the capacitance spread.

Source: Maloberti Ch. 3

Matching - motivation

Digital-to-analog conversion DAC - current sources

All current sources identical - how large must I_u be?

The MOS transistor can be used as a current source.

How large (physically) to make the transistors.

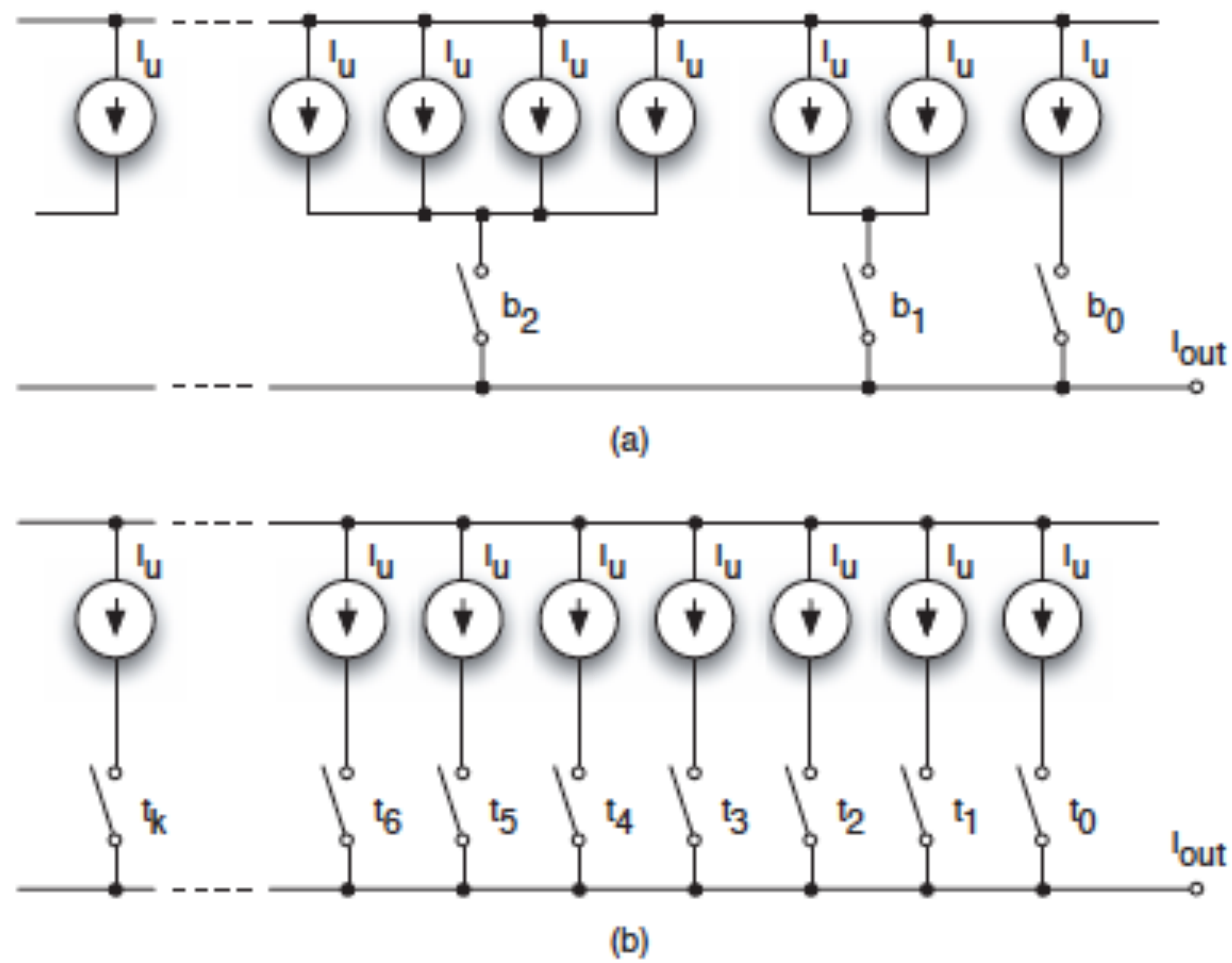


Figure 3.32. (a) Binary weighted control. (b) Unary weighted control.

Source: Maloberti Ch. 3

MOS transistor as current source

- ON or OFF
  - The threshold voltage, $V_{T,}$ determines the state
- When fully ON how much the current you get is determined by this equation:

$$I_{DSAT} = \boxed{\beta}(V_{DD} - \boxed{V_T})^2$$

$$\beta = \mu C_{ox} \frac{W}{L}$$

Time scales

Max current CPU clock frequency: 4 GHz => period: 250 ps

fabrication:
lithography
dopants
process corners

IR drop
temperature
gradients

IR drop
clock jitter
HF noise
(thermal)

power supplies
temperature
LF noise (1/f)

static

seconds = 10^0
billions of clock cycles

microseconds = 10^{-3}
millions of clock cycles

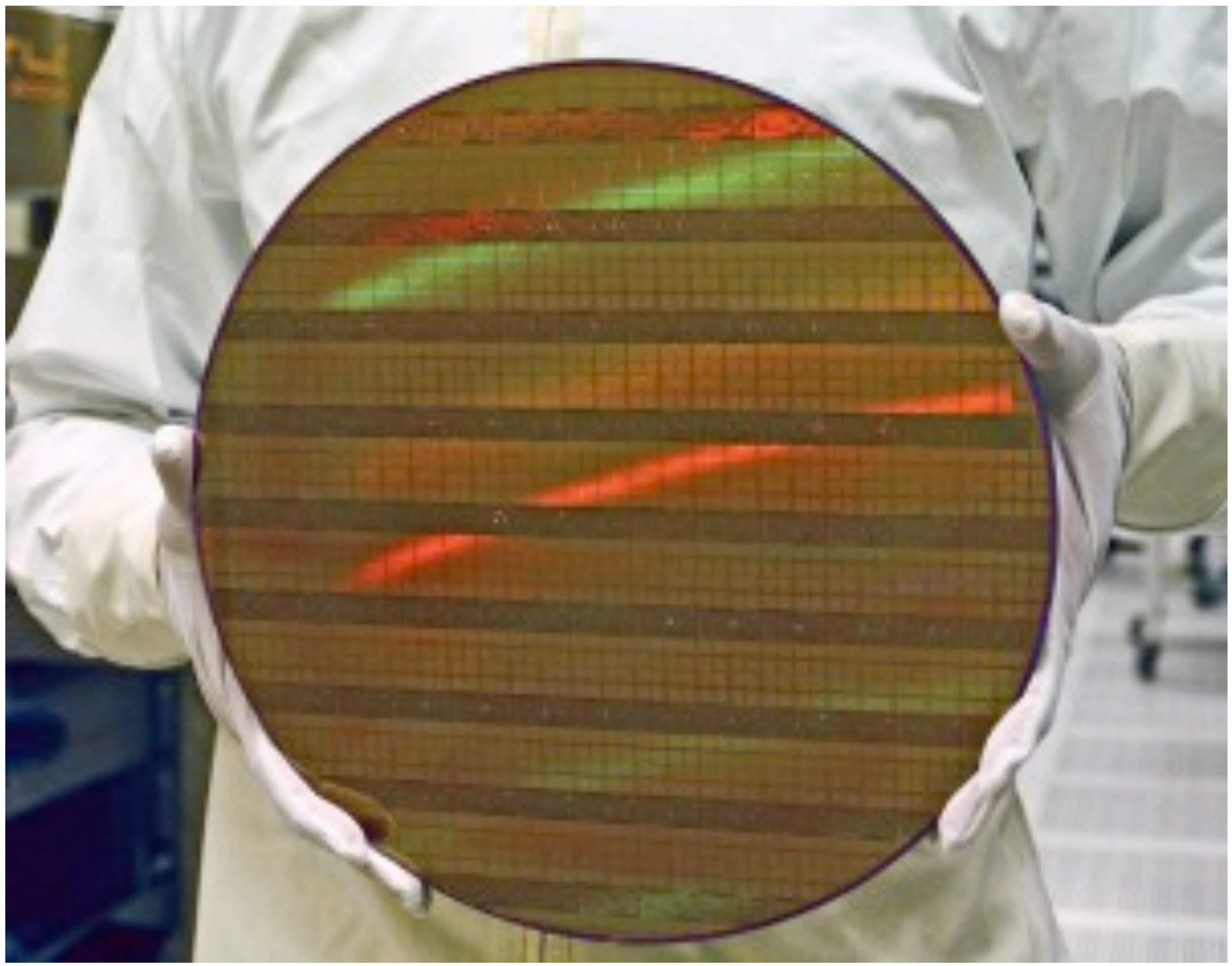
250 ps

picoseconds = 10^{-12}
less than one clock cycle

Static variability

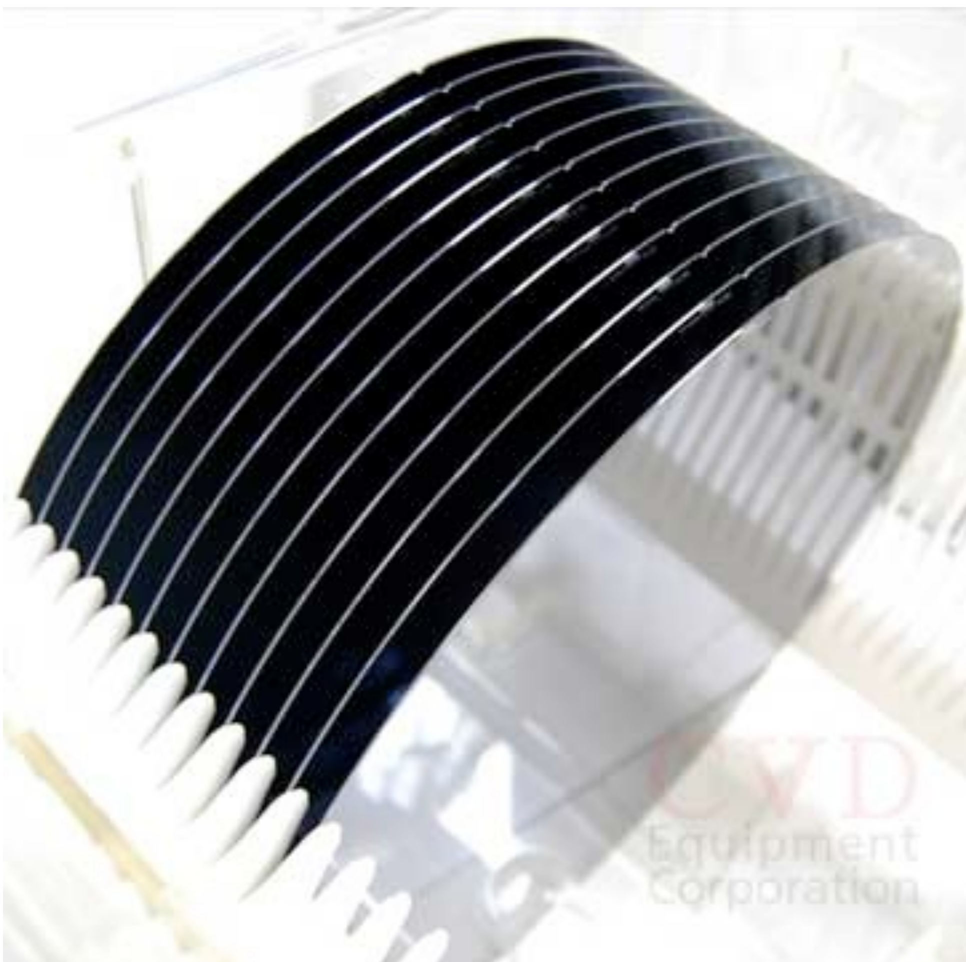
- Two devices, nominally identical, come out differently
    - Random + predictable
- Note: more insights move more of variations from r to p
- What is knowable in principle may still be efficiently handled by statistical methods

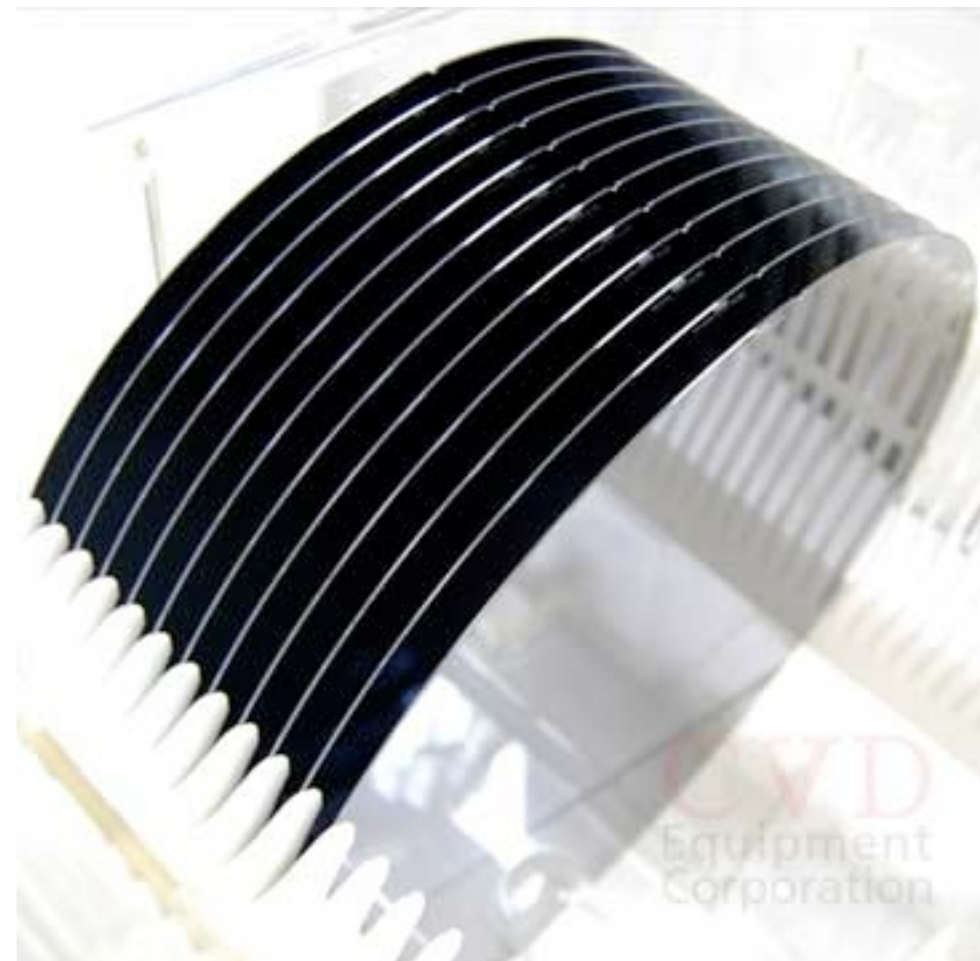
Chips are fabricated on wafers



Current Intel 300-mm wafer (photo from Intel)

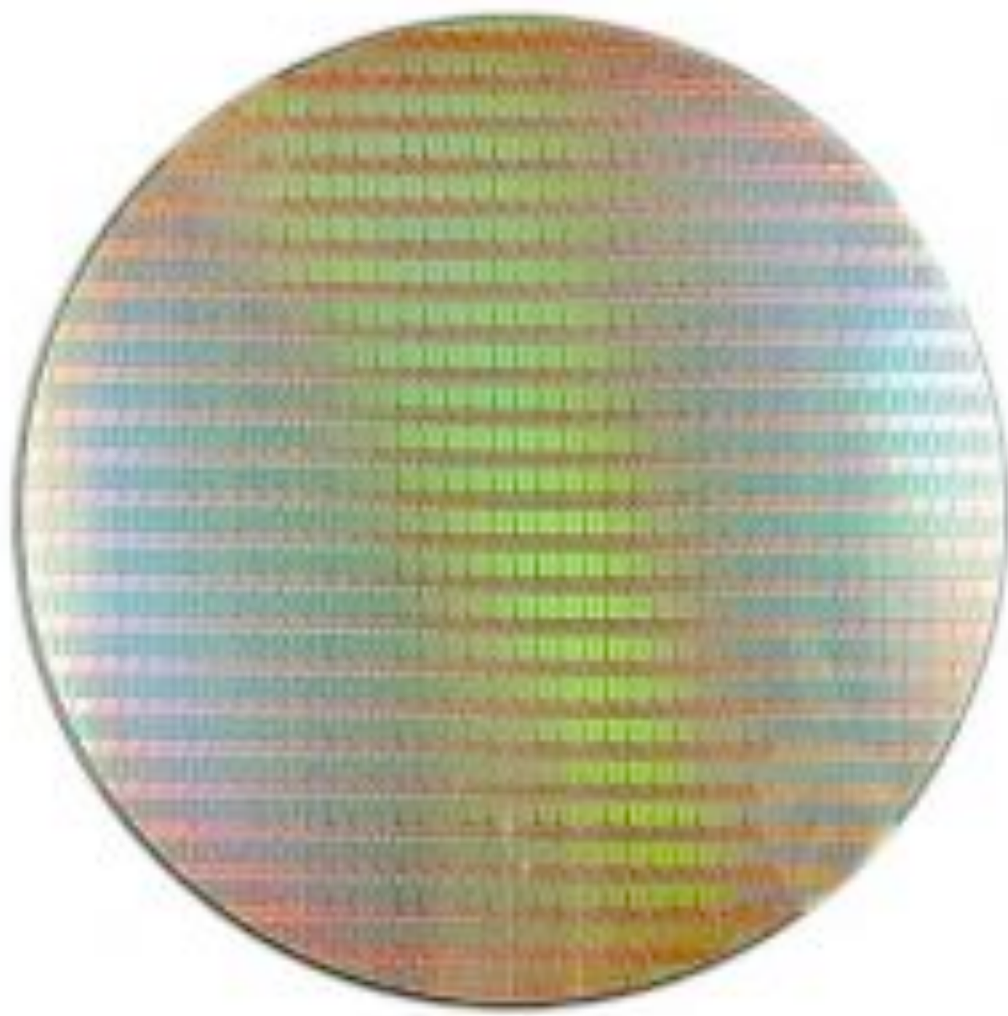
Source 1

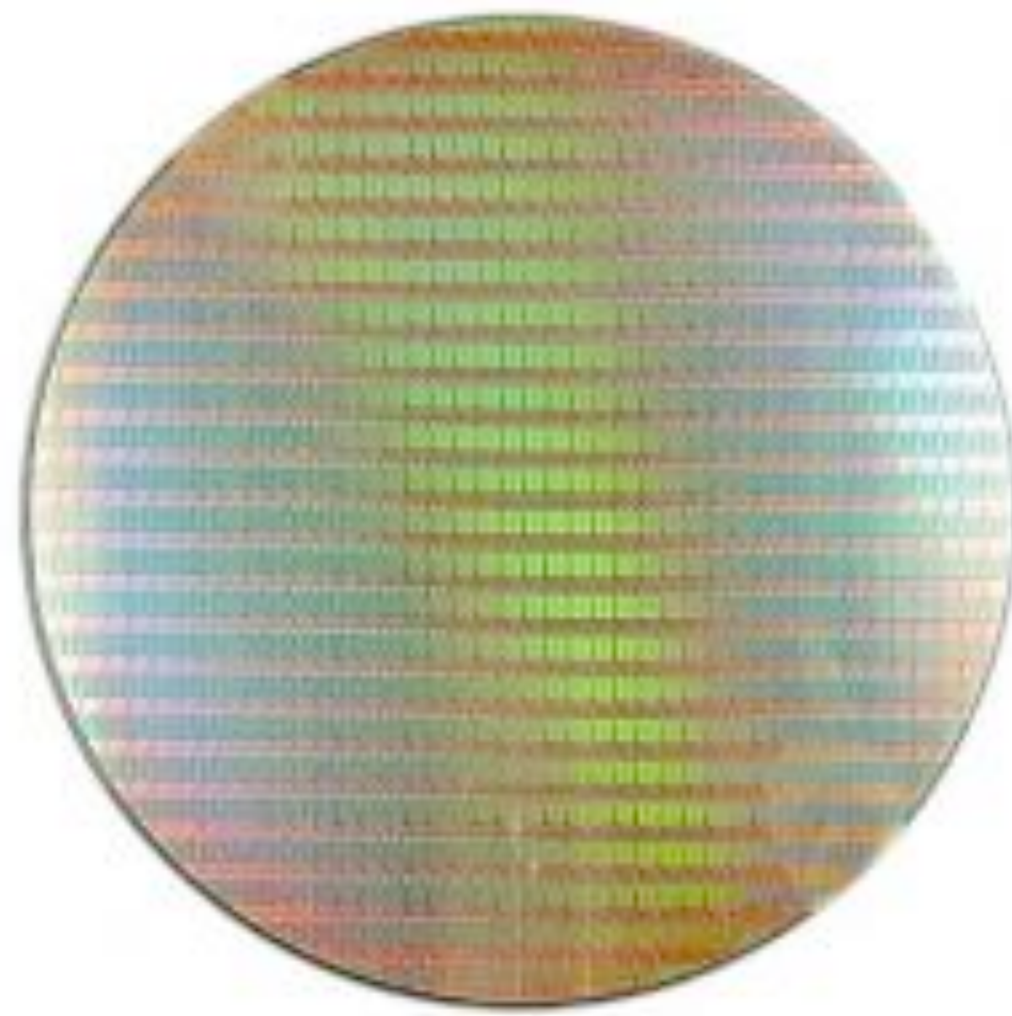




- 2 “boats” (wafer batches) will differ
  - Equipment may have changed

Source 2

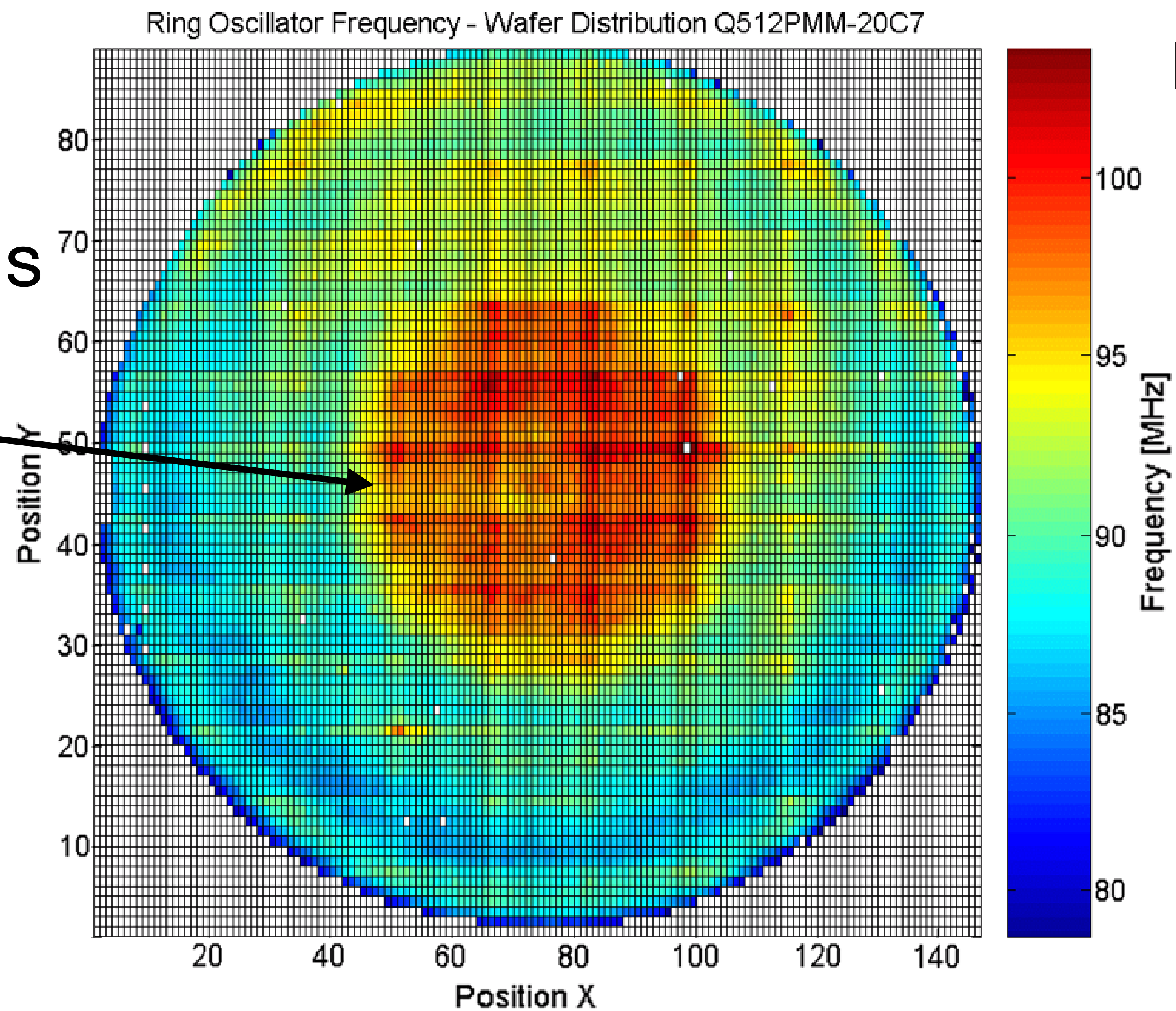




- Wafers from same boat will differ
    - Slight differences in processing steps

Source 3

Each square is one chip



Fast

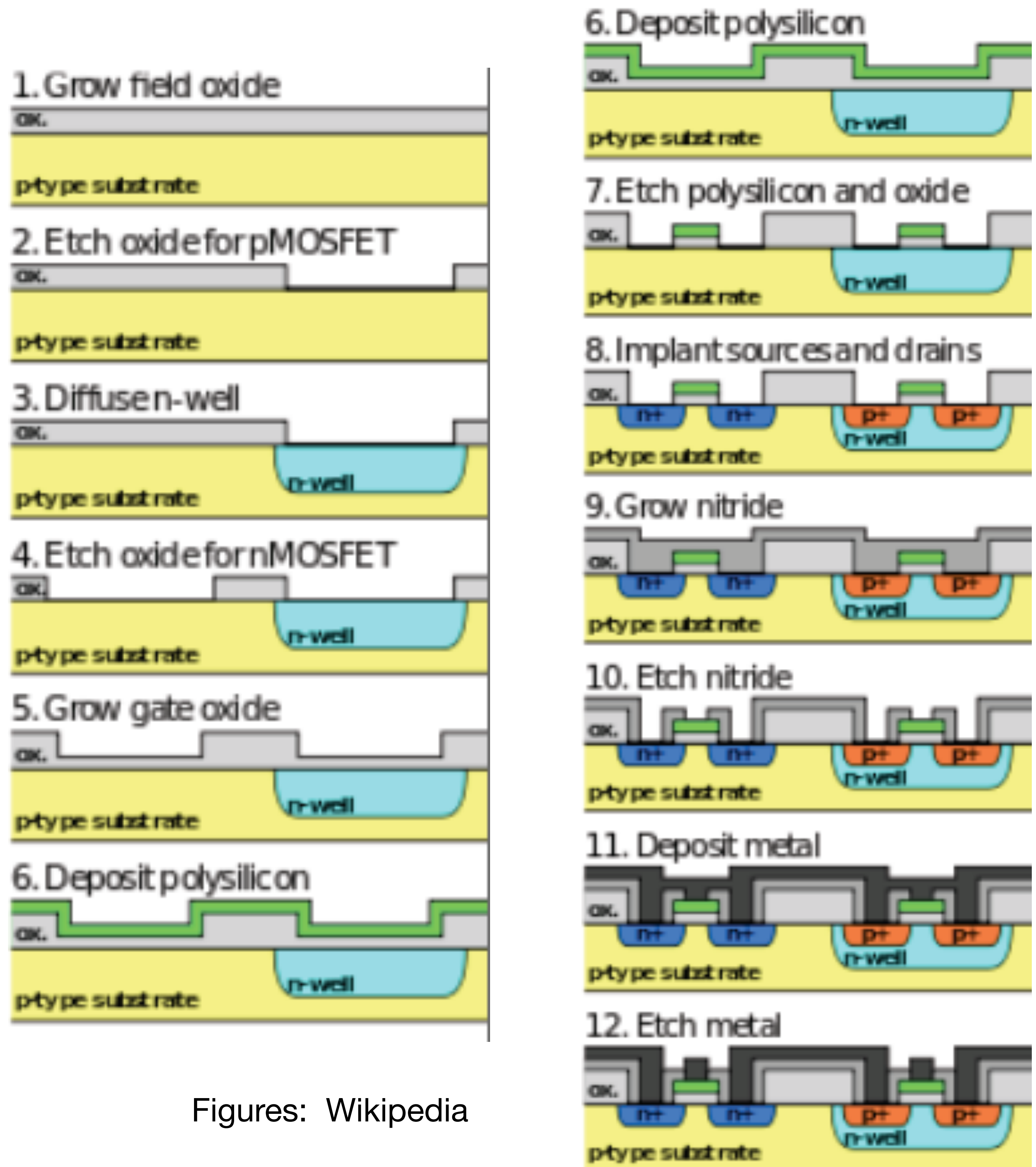
Slow

- Chips from same wafer will differ

Source: Pelgrom: Analog-to-Digital Conversion 2010. Springer. Fig. 11.4

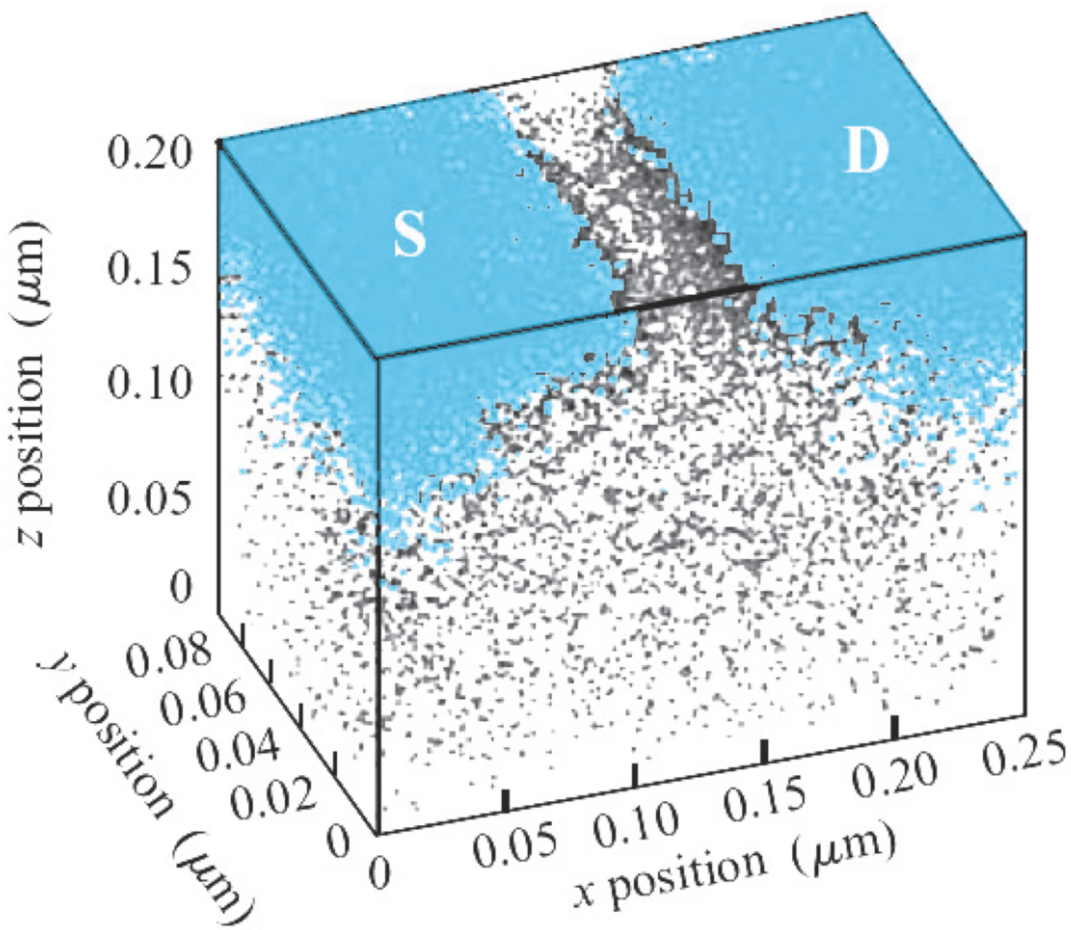
CMOS fabrication steps

Grow
Etch
Diffuse
Etch
Grow
Deposit
Etch
Implant
Grow
Etch
Deposit
Etch
...



Figures: Wikipedia

Source 5

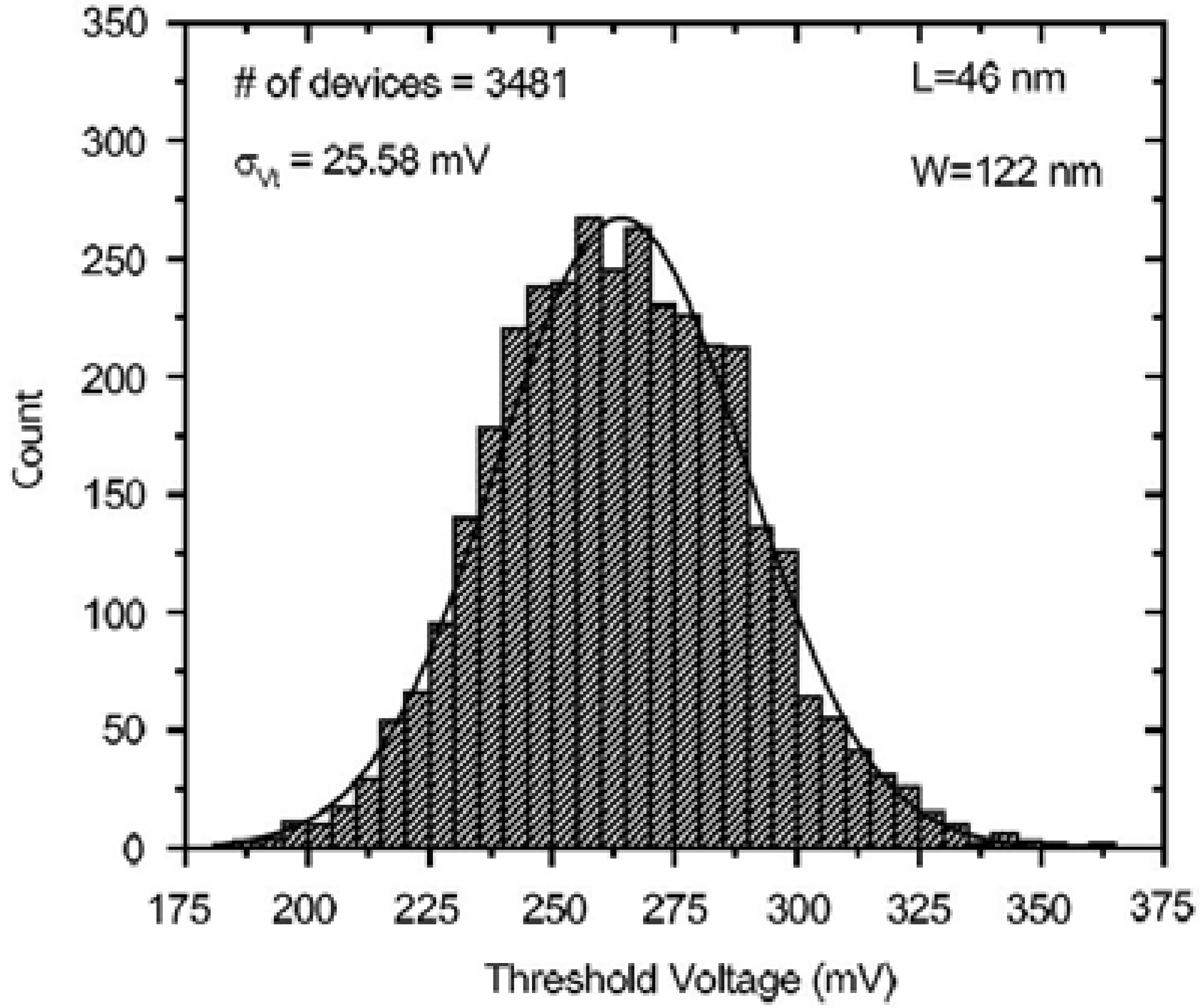


- Pure random variations
  - i.e. what is still unpredictable …

How handle?

- Designs should depend on **ratios**, not on absolute values
  - Usually means selecting different circuit topology.
- **Matching rules:**
  - Use identical sizes
  - Minimize predictable/controllable differences
  - Increase device size to reduce random differences

Matching example V_T



Parameter fluctuation (1)

- Parameter *P* describes physical property of device
  - Deterministic + random function
  - Different values at different locations on wafer (x,y): *P*(x,y)

Parameter fluctuation (2)

Describe the **difference** in *P* between two points, *ΔP*, mathematically:

$$\Delta P(x_{12}, y_{12}) = P(x_1, y_1) - P(x_2, x_2)$$

which can also be written as:

$$\Delta P(x_{12}, y_{12}) = \frac{1}{\text{area}} \left[\iint\limits_{\text{area}(x_1, y_1)} P(x', y') dx' dy' - \iint\limits_{\text{area}(x_2, y_2)} P(x', y') dx' dy' \right]$$

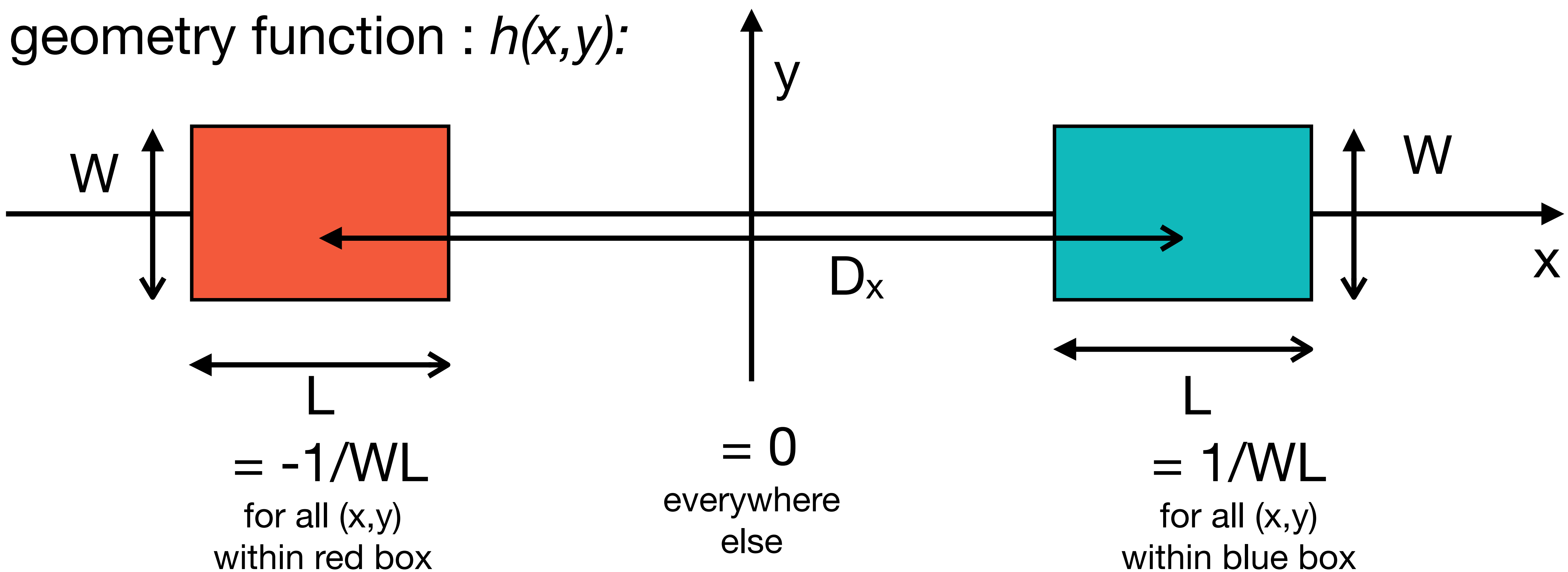
In the Fourier domain this convolution becomes a multiplication:

$$\Delta \mathcal{P}(\omega_x, \omega_y) = \mathcal{G}(\omega_x, \omega_y) \mathcal{P}(\omega_x, \omega_y)$$

Can analyze **geometry** and **mismatch generating source** separately!

Geometry function in x,y plane

geometry function : *h(x,y)*:

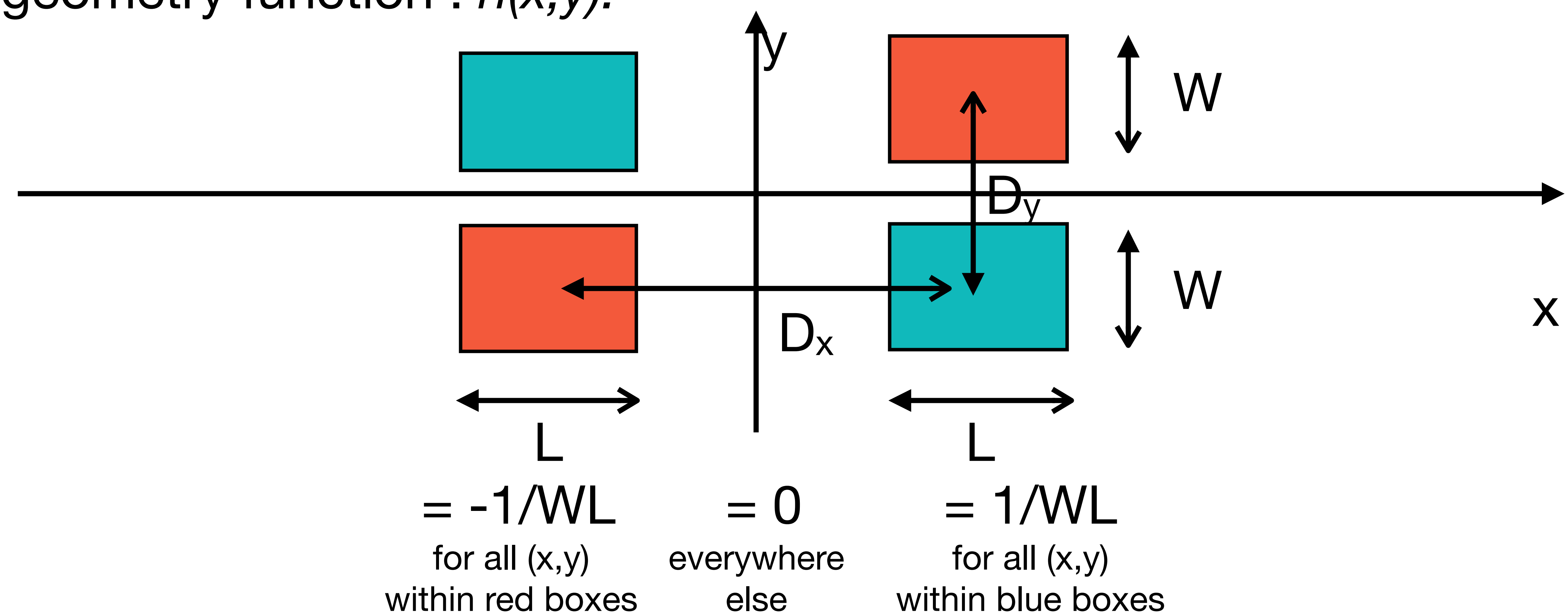


Fourier transform (after some manipulation):

$$\mathcal{G}(\omega_x, \omega_y) = \frac{\sin(\omega_x \frac{L}{2})}{\omega_x \frac{L}{2}} \frac{\sin(\omega_y \frac{W}{2})}{\omega_y \frac{W}{2}} \left[2 \sin(\omega_x \frac{D_x}{2}) \right]$$

Another geometry function in x,y

geometry function : *h(x,y):*



Fourier transform (after some more manipulations):

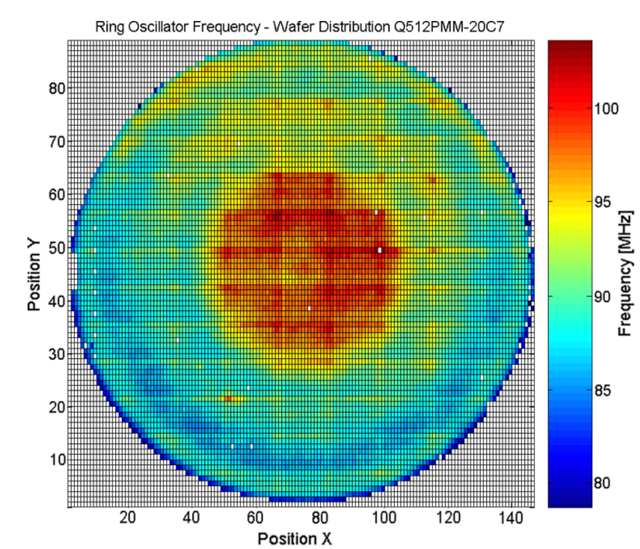
$$\mathcal{G}(\omega_x, \omega_y) = \frac{\sin(\omega_x \frac{L}{2})}{\omega_x \frac{L}{2}} \frac{\sin(\omega_y \frac{W}{2})}{\omega_y \frac{W}{2}} \left[\cos(\omega_x \frac{D_x}{2}) - \cos(\omega_y \frac{D_y}{2})\right]$$

Mismatch generation source: *P*(x,y)

- *P*(x,y) of “class 1”:
  - Total mismatch of parameter *P* is due to mutually independent events
  - Effects on the parameter are so small that contributions are linear
  - The correlation distance between events is small compared to device size
- Result is a Possion process which converges to Gaussian with 0 mean.
- Corresponds to spatial “white noise”. Characterized by **one constant** for all spatial frequencies.

Mismatch generation source *P*(x,y)

- *P*(x,y) of “class 2”:
  - Total mismatch of parameter *P* is due to mutually independent events
  - Effects on the parameter are so small that contributions are linear
  - The correlation distance between events is **large** compared to device size



Finding the power (= variance) of ΔP

Sum the power contributions =
Integrate the squares over all spatial frequencies:

$$\sigma^2(\Delta P) = \frac{1}{4\pi^2} \int\limits_{\omega_y=-\infty}^{\infty} \int\limits_{\omega_x=-\infty}^{\infty} \left|\mathcal{G}(\omega_x, \omega_y)\right|^2 \left|\mathcal{P}(\omega_x, \omega_y)\right|^2 d\omega_x d\omega_y$$

With two rectangular devices and
a mismatch generation source of class 1 we get:

$$\sigma^2_{\Delta P} = \frac{A_P^2}{WL}$$

Here A_P is the proportionality constant for parameter ΔP

Average (relative) or absolute quantity?

This relation holds for *averaged* or *relative* values of parameter *P* (for example threshold voltage of MOS transistor)*:*

$$\sigma^2_{\Delta P} = \frac{A_P^2}{WL}$$

Absolute number of events are proportional to WL (for example number of charges in MOS transistor channel). The relation is then:

$$\sigma^2(\Delta P) = A_P^2 WL$$

Conclusion of derivation

Variability example: OP27

OP27–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP27A/E Min	OP27A/E Typ	OP27A/E Max	OP27F Min	OP27F Typ	OP27F Max	OP27C/G Min	OP27C/G Typ	OP27C/G Max	Unit
INPUT OFFSET VOLTAGE[1]	V_{OS}			10	25		20	60		30	100	µV
LONG-TERM V_{OS} STABILITY[2, 3]	V_{OS}/Time			0.2	1.0		0.3	1.5		0.4	2.0	µV/M_O
INPUT OFFSET CURRENT	I_{OS}			7	35		9	50		12	75	nA
INPUT BIAS CURRENT	I_B			±10	±40		±12	±55		±15	±80	nA
INPUT NOISE VOLTAGE[3, 4]	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		0.08	0.18		0.08	0.18		0.09	0.25	µV p-p
INPUT NOISE Voltage Density[3]	e_n	f_O = 10 Hz		3.5	5.5		3.5	5.5		3.8	8.0	$nV/\sqrt{Hz}$
		f_O = 30 Hz		3.1	4.5		3.1	4.5		3.3	5.6	$nV/\sqrt{Hz}$
		f_O = 1000 Hz		3.0	3.8		3.0	3.8		3.2	4.5	$nV/\sqrt{Hz}$
INPUT NOISE Current Density[3, 5]	i_n	f_O = 10 Hz		1.7	4.0		1.7	4.0		1.7		$pA/\sqrt{Hz}$
		f_O = 30 Hz		1.0	2.3		1.0	2.3		1.0		$pA/\sqrt{Hz}$
		f_O = 1000 Hz		0.4	0.6		0.4	0.6		0.4	0.6	$pA/\sqrt{Hz}$
INPUT RESISTANCE												

MOS transistor matching

$$I_{DSAT} = \boxed{\beta}(V_{DD} - \boxed{V_T})^2$$

where $$\beta = \mu C_{ox} \frac{W}{L}$$

Threshold voltage matching - absolute (since averaged quantity)

$$\sigma^2_{\Delta VT} = \frac{A^2_{VT}}{WL}$$

Current factor matching - relative (since absolute quantity)

$$\frac{\sigma^2_{\Delta\beta}}{\beta^2} \approx \frac{A^2_{\beta}}{WL}$$

Has to analyze contributions from μ, Cox, W and L

Finding proportionality constant A_{VT} from measurements

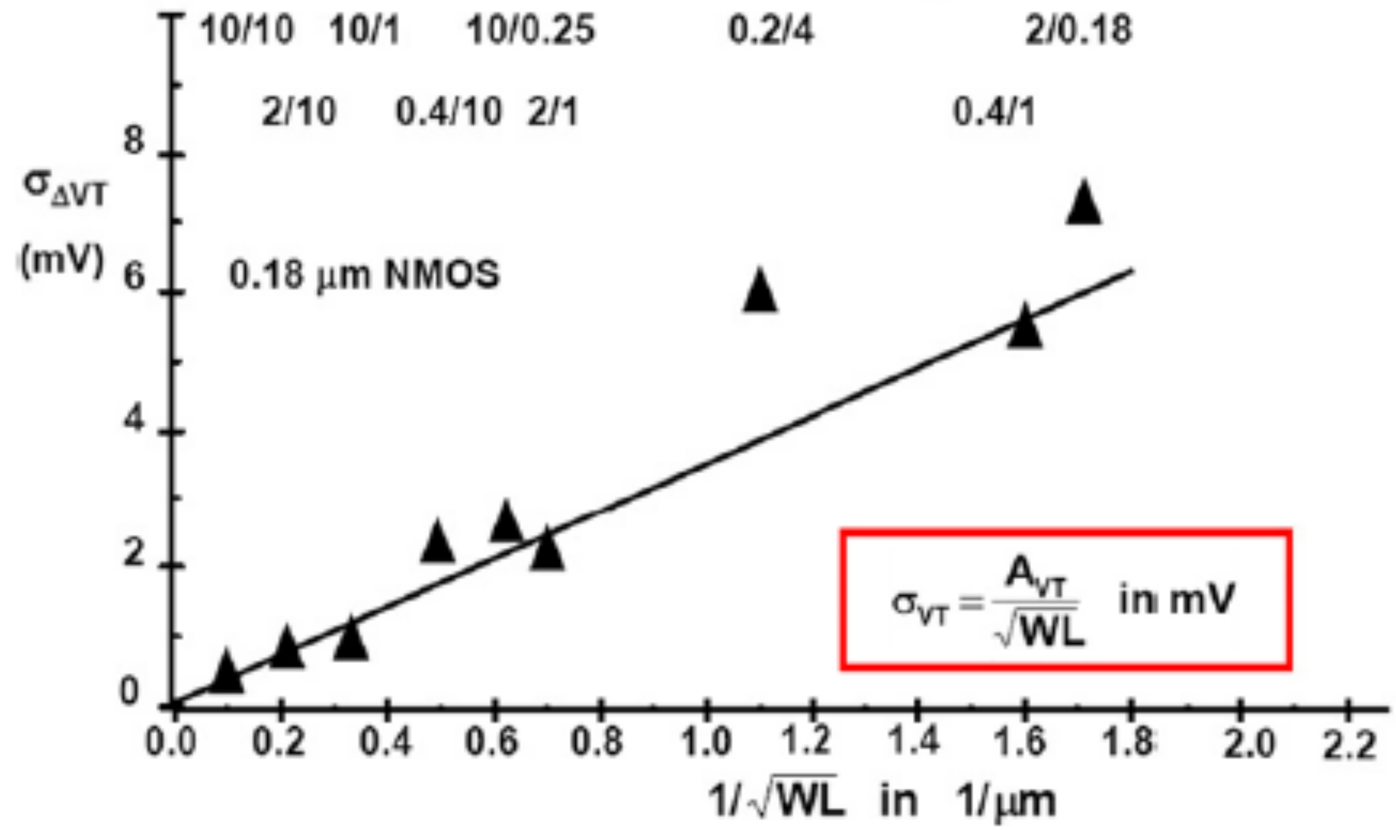
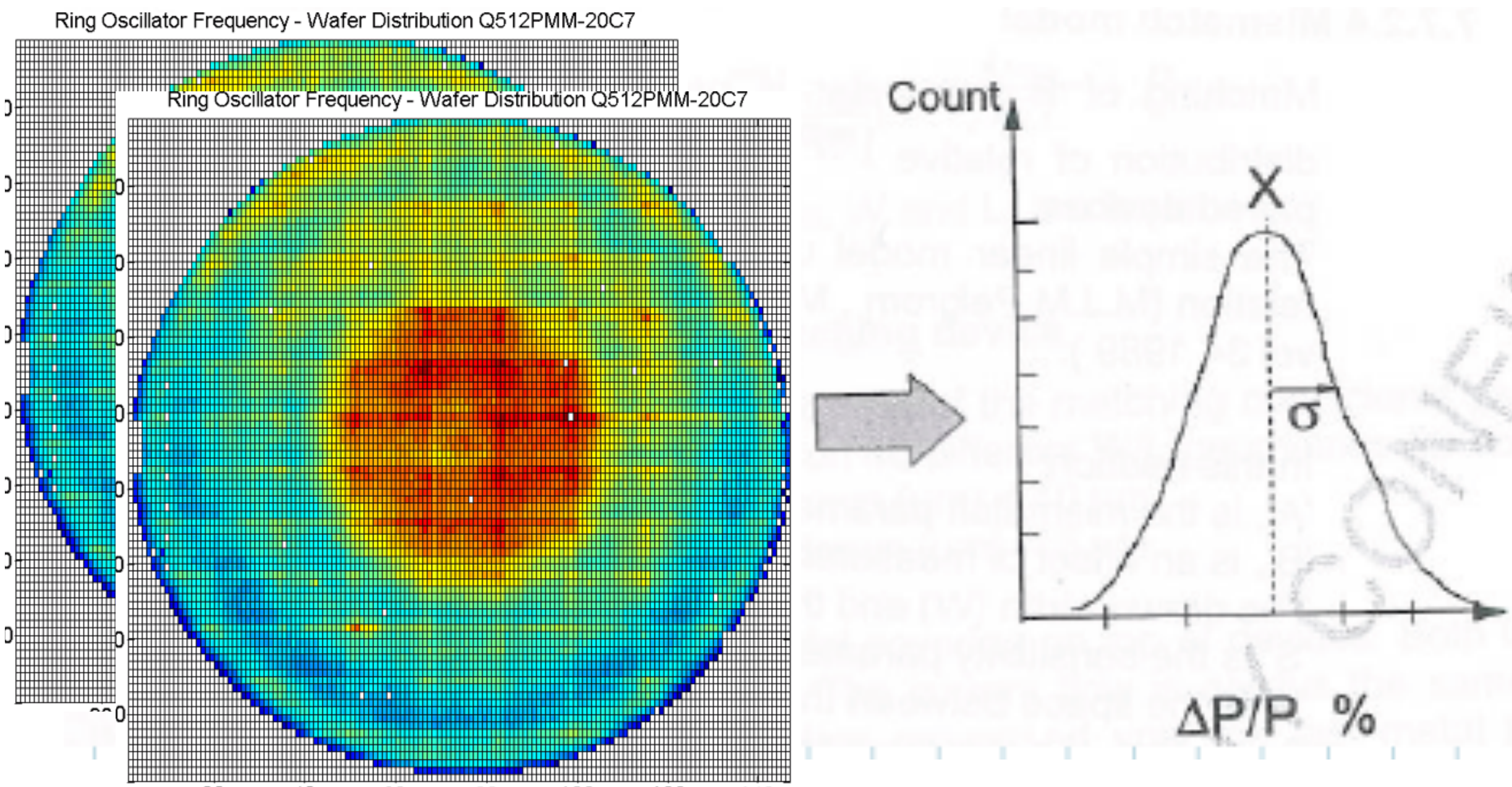


Fig. 11.18 The standard deviation of the NMOS threshold and the relative current factor versus the inverse square root of the area, for a 0.18 µm CMOS process

Can also calculate from first principles

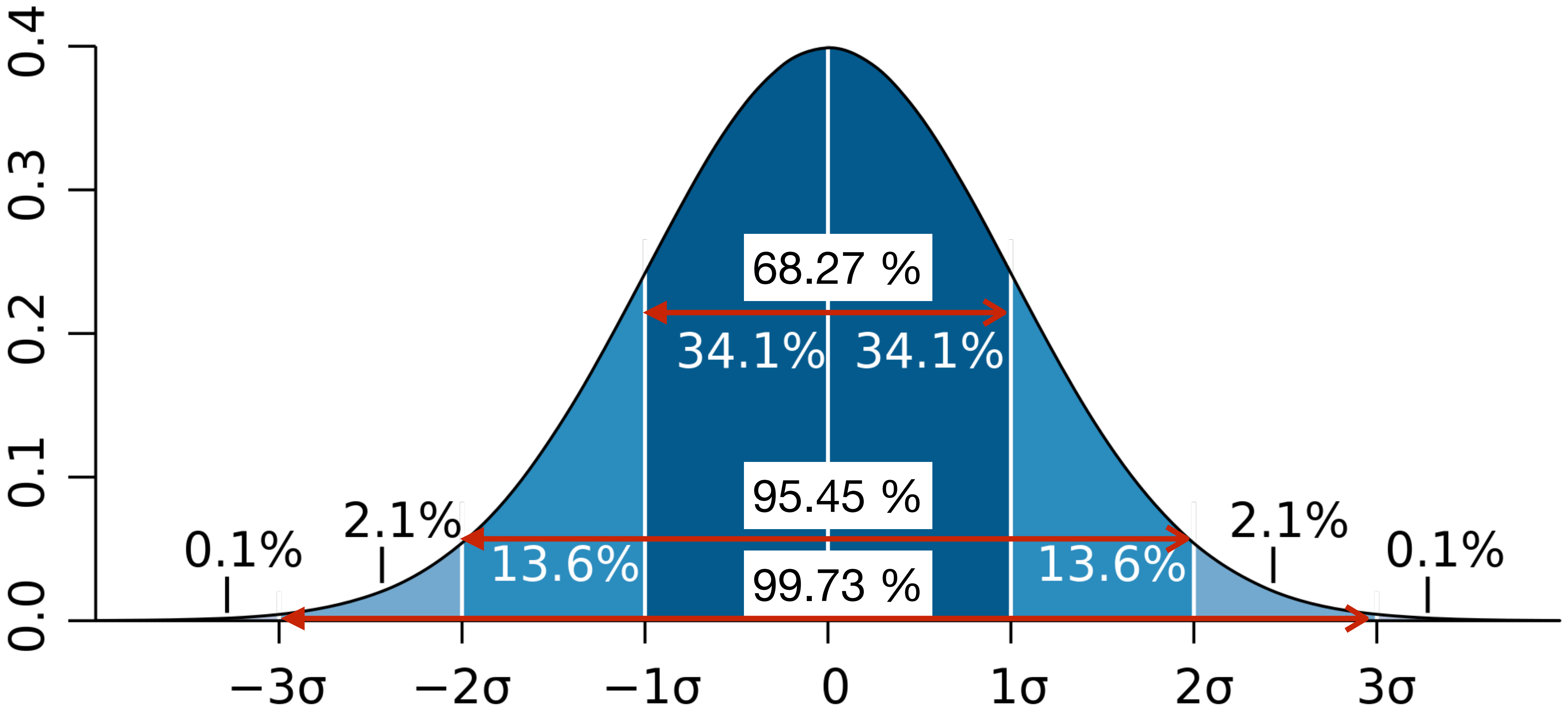
From Pelgrom 2010

From measurements to statistics



Measured mismatch translated into statistical model
Assumption: Gaussian distribution

Translation continued



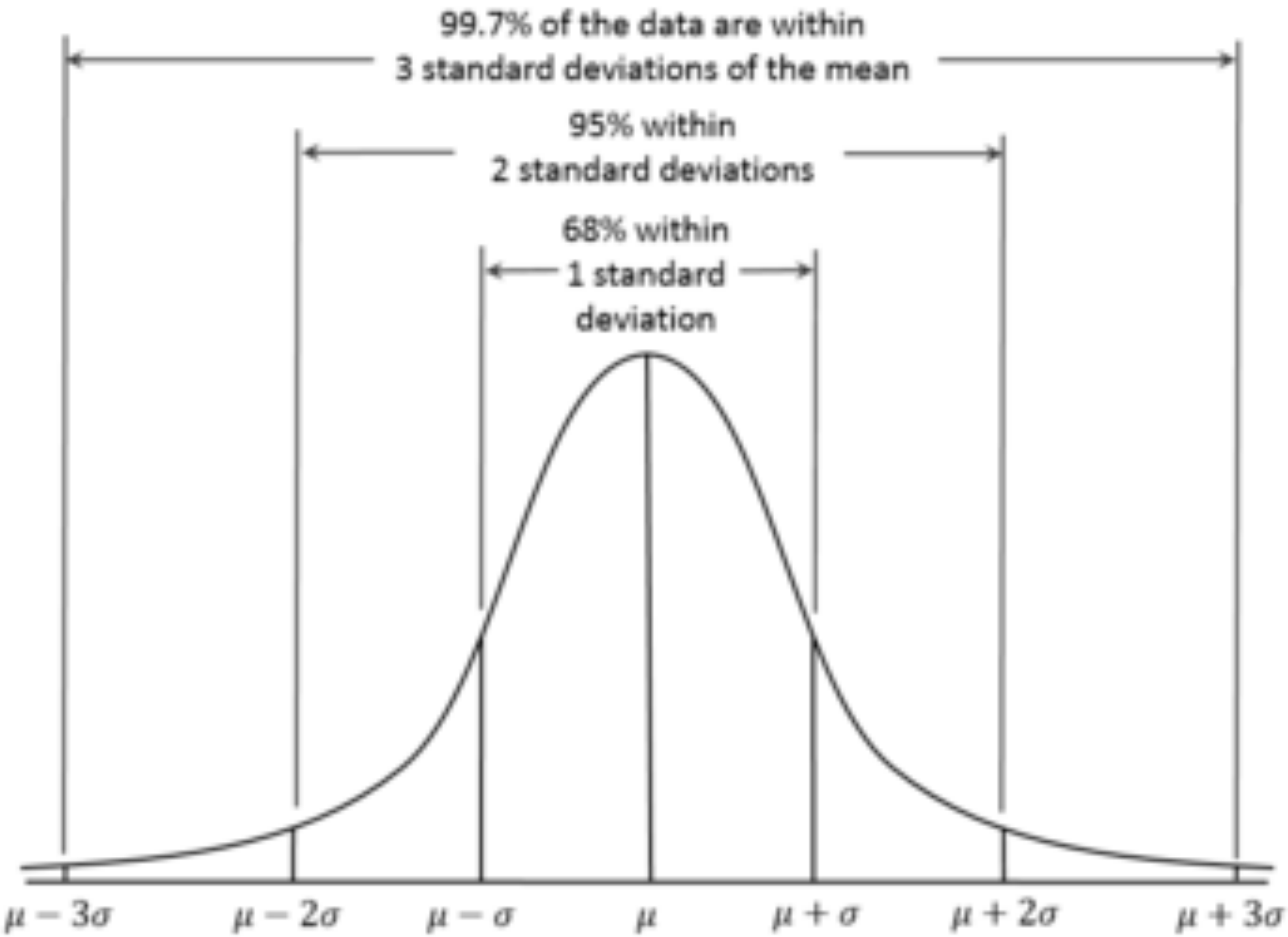
The percentage of chips that are within the limit af acceptance, depending on the number of standard deviations the variations are kept within.

Source: Wikipedia

An example

- We want to match V_T of two nMOS transistors in the 65 nm process:
  - The difference in V_T should be at most 10 mV and we know that $A_{V_T} = 5.4\,[mV\,\mu m]$
  - How wide do we have to make them?
    - Assume the length L = 1 μm
    - Assume that we do all the layout perfect.
    - Assume that staying within 3σ is “enough”.

Is 1, 2 or 3 stdv or more enough?



MOS transistor as current source revisited

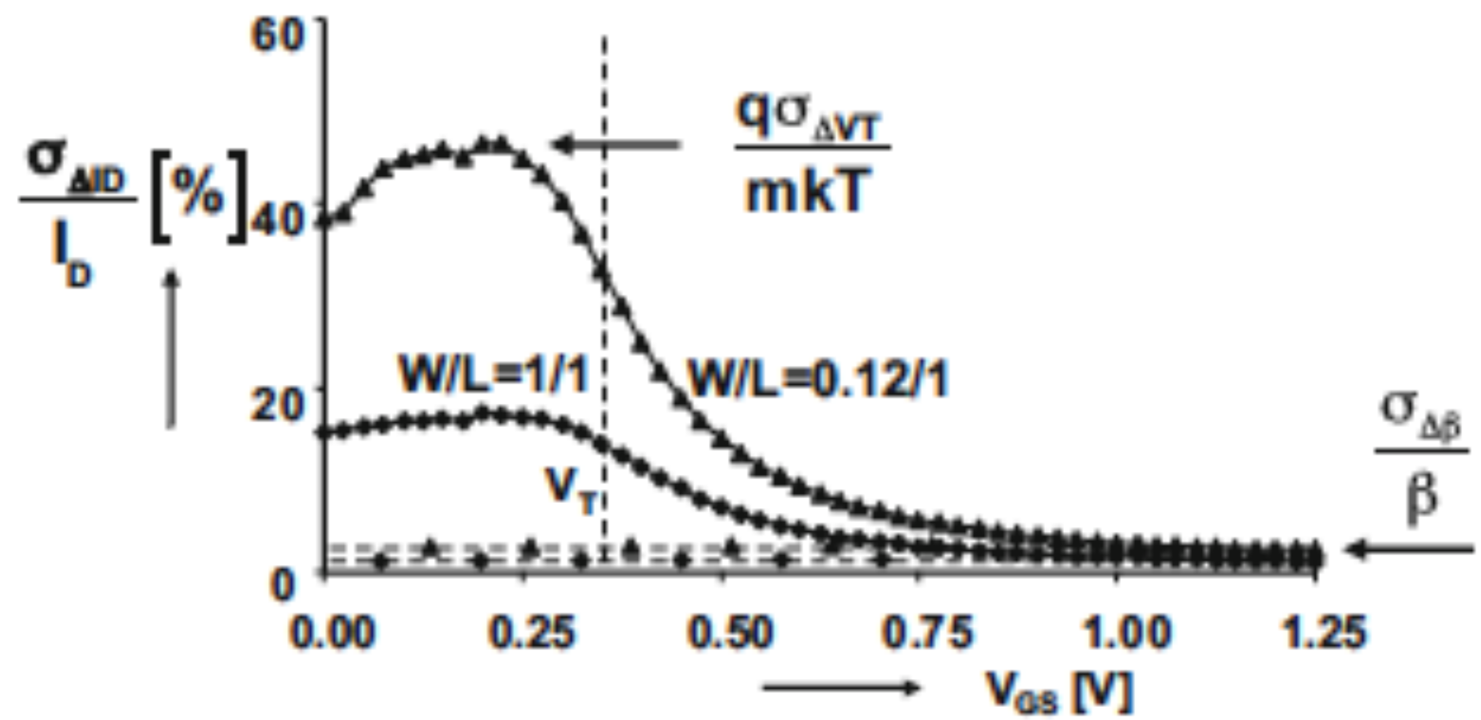


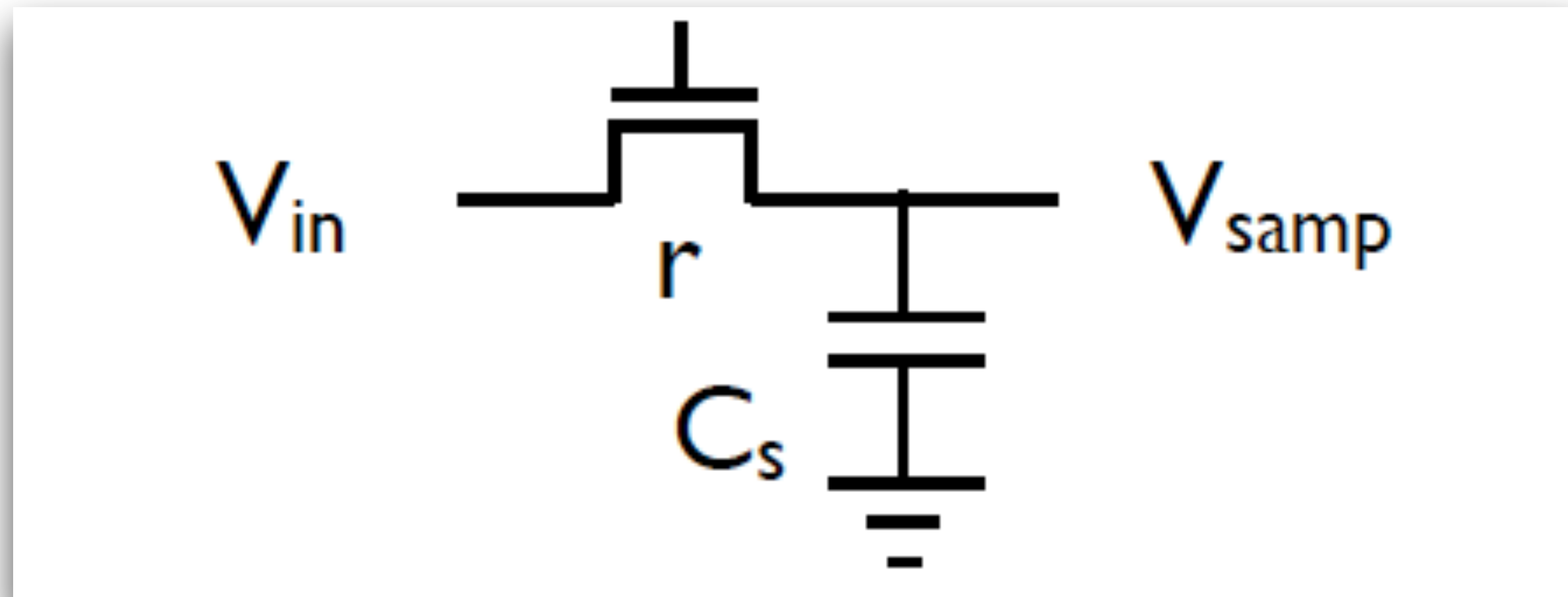
Fig. 5.36 The relative current mismatch for two 65-nm technology transistor geometries swept over the full voltage range. Measurements by N. Wils/H. Tuinhout

Note that one reason that the relative mismatch is lower around and below VT is that the current is much lower!

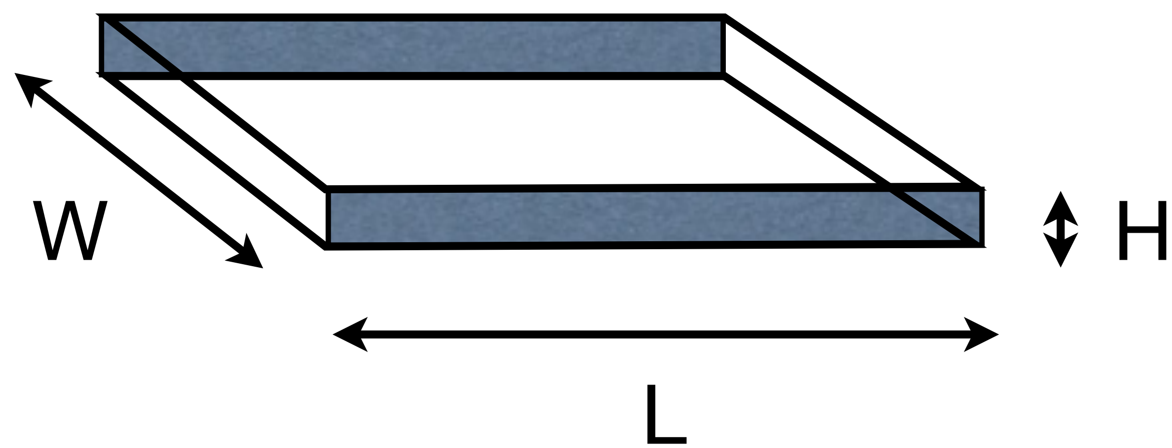
Passive components

- Better matching than for transistors
  - When setting gain!
    - => Feedback and variability next time.
- Also used in DAC and ADCs
  - R2R or C2C ladders, for example.

From last week - sampling



On-chip resistor (ideal)



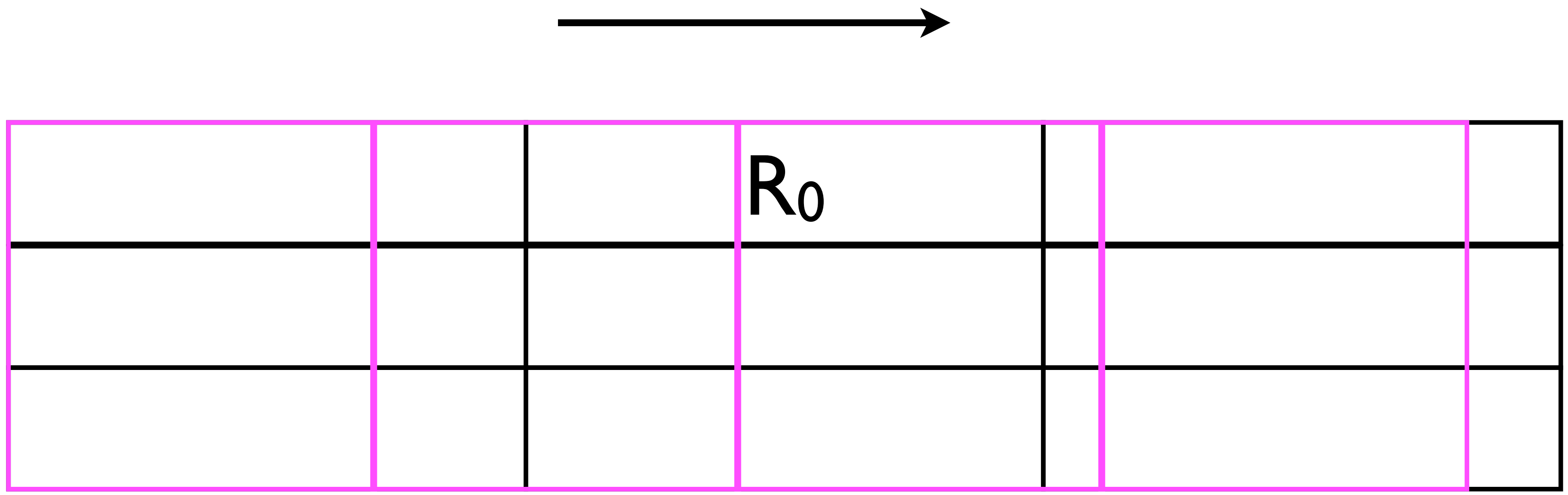
- Rectangular slab of some material

$$R = r \cdot L / (W \cdot H)$$

- Height given by process
- Value determined by length and width

Top view

direction of current



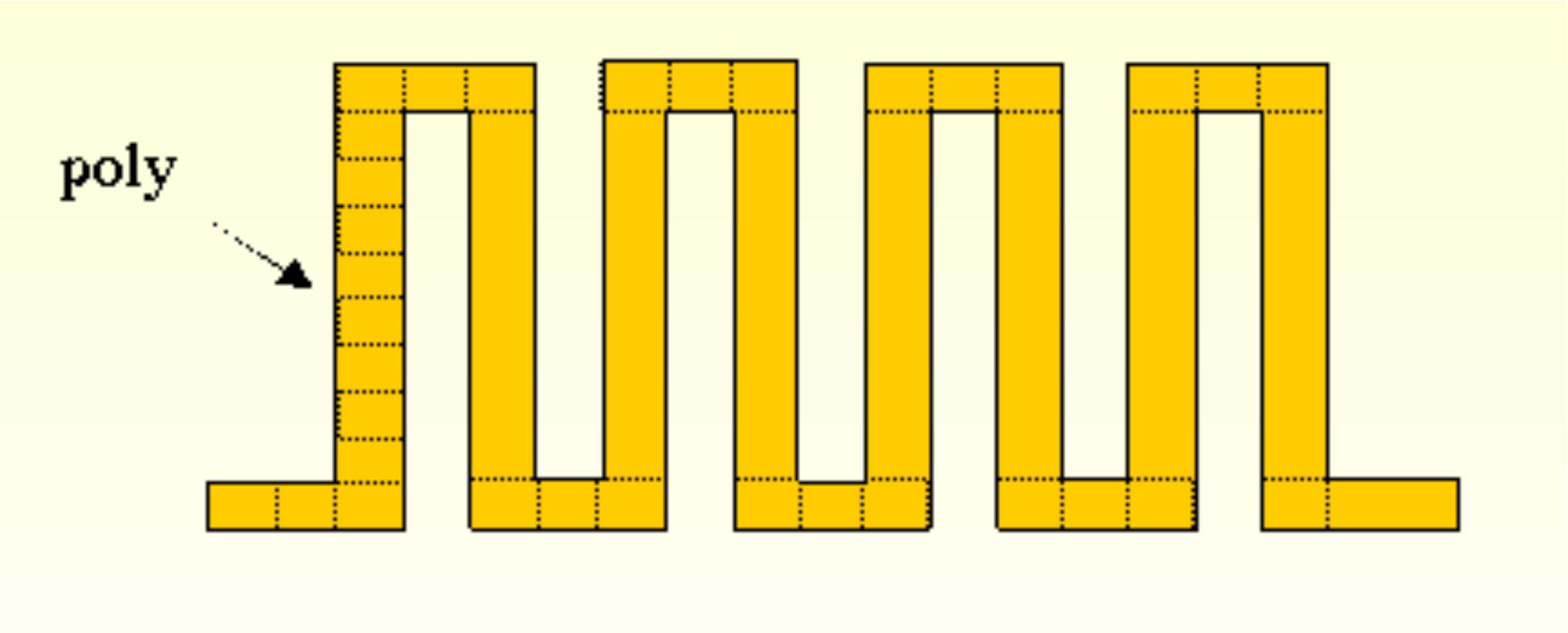
- Nominal resistance set by aspect ratio, L / W
- $R = r \cdot L / (W \cdot H) = (r / H) \cdot (L / W)$

resistivity per square

Small values?

- Inaccuracies at ends

Large values?



- Need large L / W
- Minimum W set by process design rules
- L is "only" parameter!
- Long and narrow…

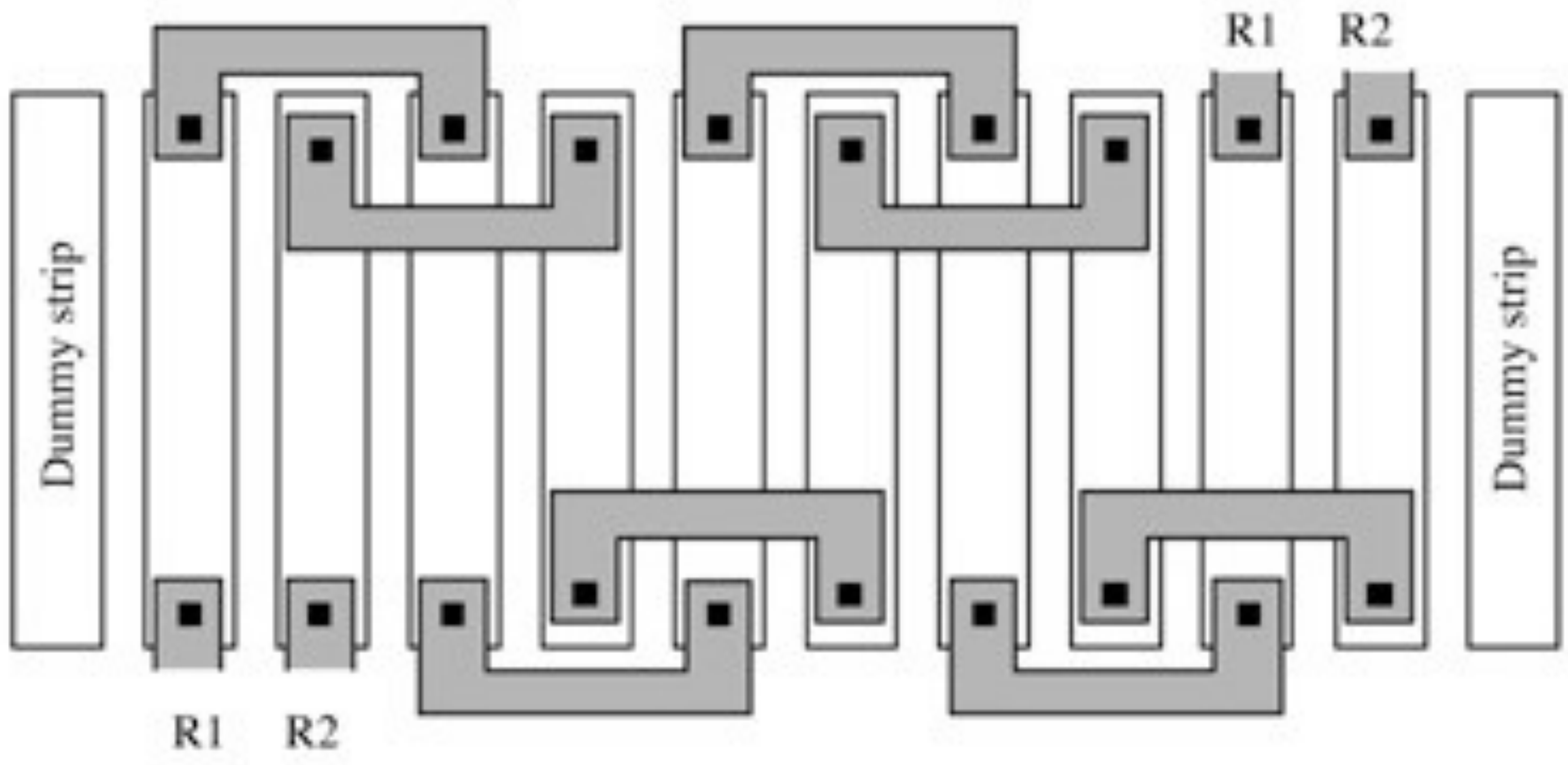
Corners count for 0.5 square

Accuracy?

- $R = (r / H) \cdot (L / W)$
- r: material property
- H: set by process for each layer

- Geometrical inaccuracies affect mostly W
  - Predictable error + random variations
  - Large W is better (at an area cost…)

Relative accuracy?



- Affected by environment
- For close matching, strive for identical environments!

Resistance values?

- 65 nm process (typical values):
  - P+ diff: R_{SH} = 244 Ω/□
  - N+ diff: R_{SH} = 130 Ω/□
  - P+ poly: R_{SH} = 712 Ω/□
  - N+ poly: R_{SH} = 180 Ω/□
  - High-res P+ poly: R_{SH} = 6 kΩ/□

High resistance requires special layer

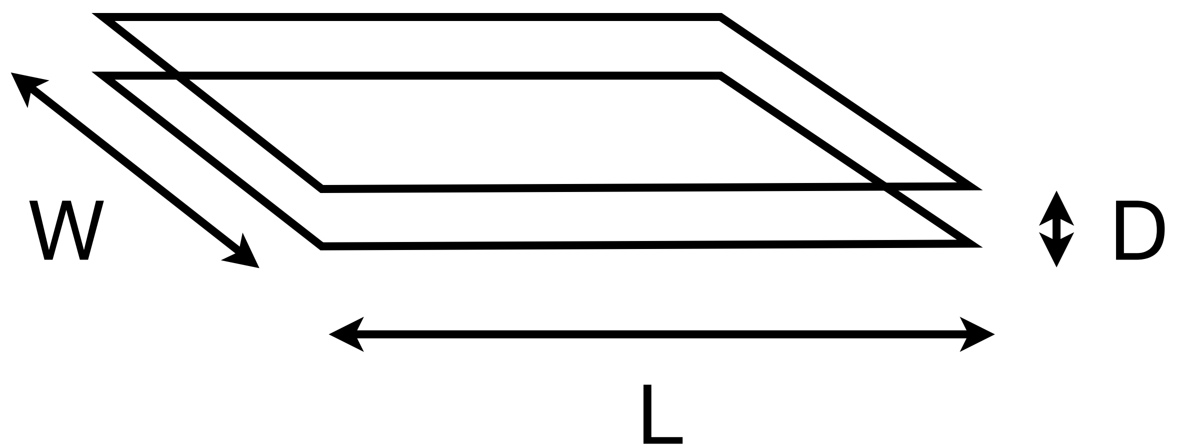
Resistance matching

$$\frac{\sigma^2_{\Delta R}}{R^2} \approx \frac{A_R^2}{WL}$$

For diffused/poly resistors typical values:

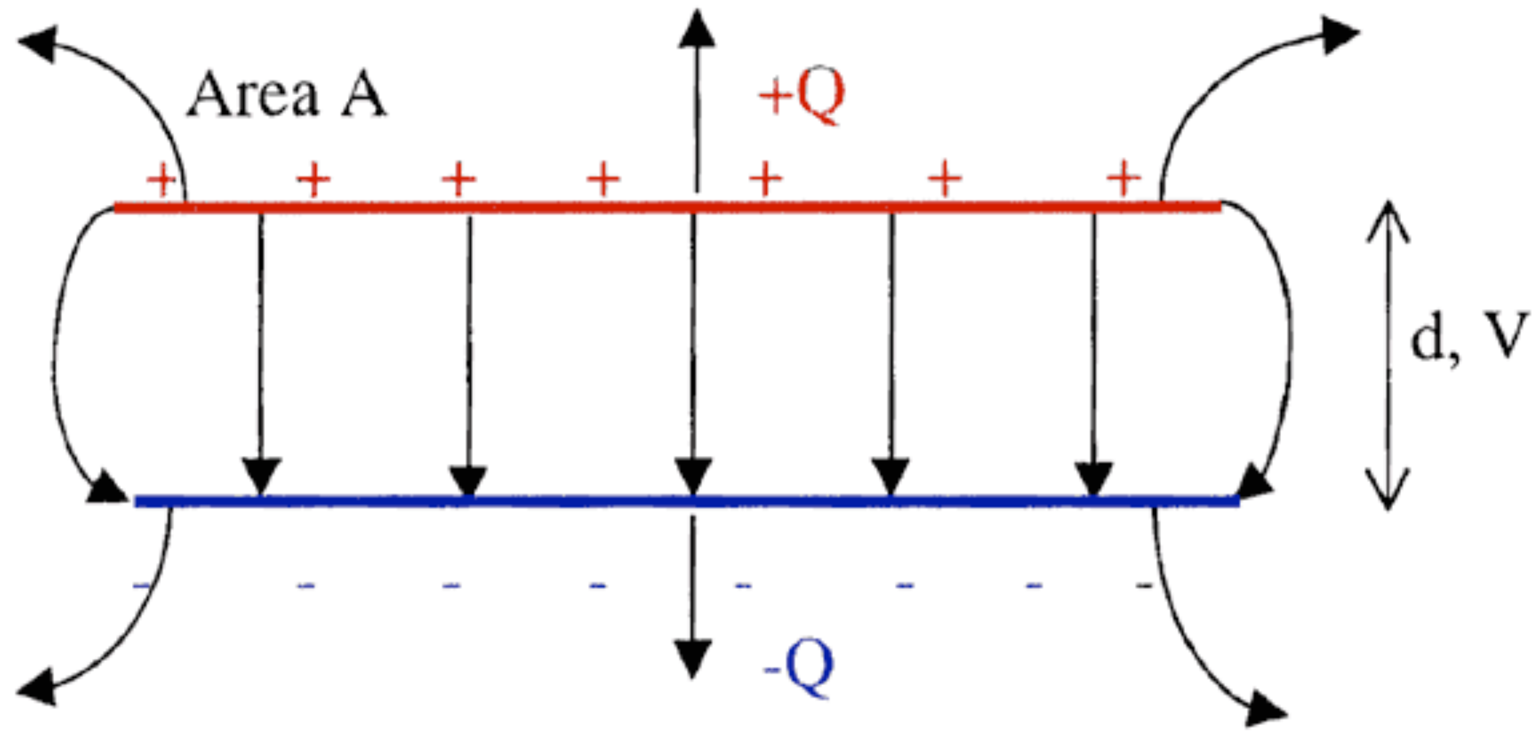
$$A_R = 0.5/5\ \%\ \mu m$$

On-chip capacitors



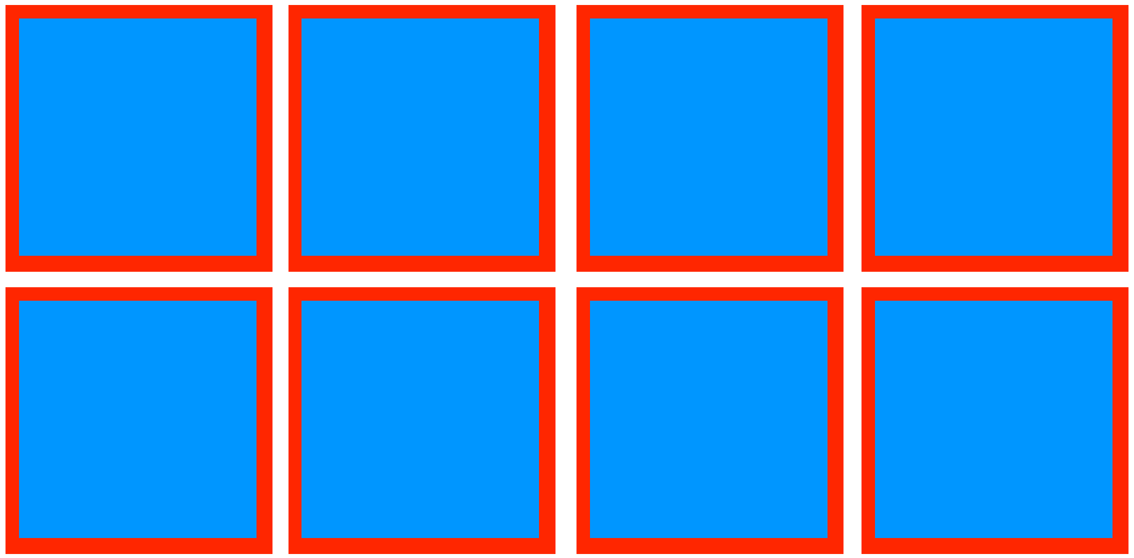
- Two conductor sheets
- One isolator sheet
- D given by process; W, L set by designer
- $C = c \cdot W \cdot L / D = (c / D) \cdot (WL)$ Area

Accuracy?



- Simple equation assumes uniform field
  - Edge fields unaccounted for!
  - Better absolute accuracy: use less edge
  - Better relative accuracy: use constant edge per area

Best relative accuracy



- Repeat unit capacitance
- Dummies around edges

Capacitance values?

- 65 nm process: no extra layer for capacitors
  - Fringe capacitor: 1.6 fF/μm^2
  - Striped stacked M1-M5 capacitor: 0.75 fF/μm^2

Capacitance matching

$$\frac{\sigma^2_{\Delta C}}{C^2} = \frac{A^2_C}{WL}$$

Assuming capacitors large enough that area effects dominate

But since the capacitance is always proportional to the capacitor area we can also express the matching as

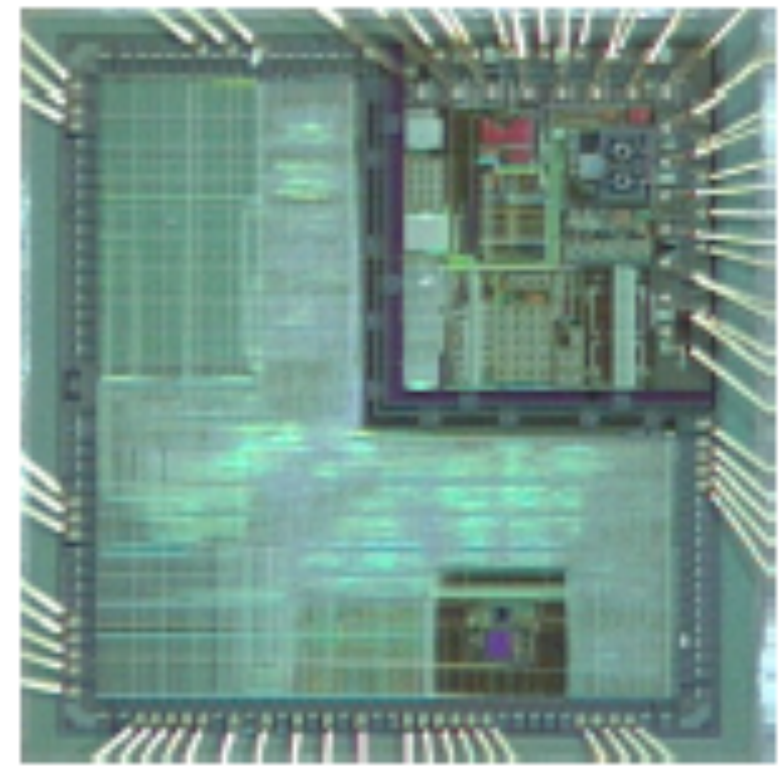
$$\frac{\sigma^2_{\Delta C}}{C^2} = \frac{A^2_C}{C}$$

$$\frac{\sigma_{\Delta C}}{C} = \frac{A_C}{\sqrt{C}}$$

$$A_C = 0.3\ \% \sqrt{fF}$$

Physical separation in mixed-mode system

- Example:
- Single-chip bluetooth transceiver Ericsson 2001
- 25% is RF part 75% is digital electronics
- Keep them apart!
- Use separate supplies.



Example due to
Sven Mattisson Ericsson research

Summary

- Passives:
- Pick C over R for on-chip use
  - Less bias current, less edge uncertainty
- Absolute component precision on chip abysmal (±20%, etc)
  - Relative precision not so bad
    - ±1% “easily” attainable

Summary, cont.

- Precision difficult for extreme values
- Large values and high relative precision cost area => $ and also W
- Mixed-mode systems: Separate analog and digital parts on the same chip as much as possible
- Clocked analog systems a problem!

Thursday

- Variability & feedback