On-chip filter implementations

DAT116, Dec 13 2018

larssv@chalmers.se

Why?

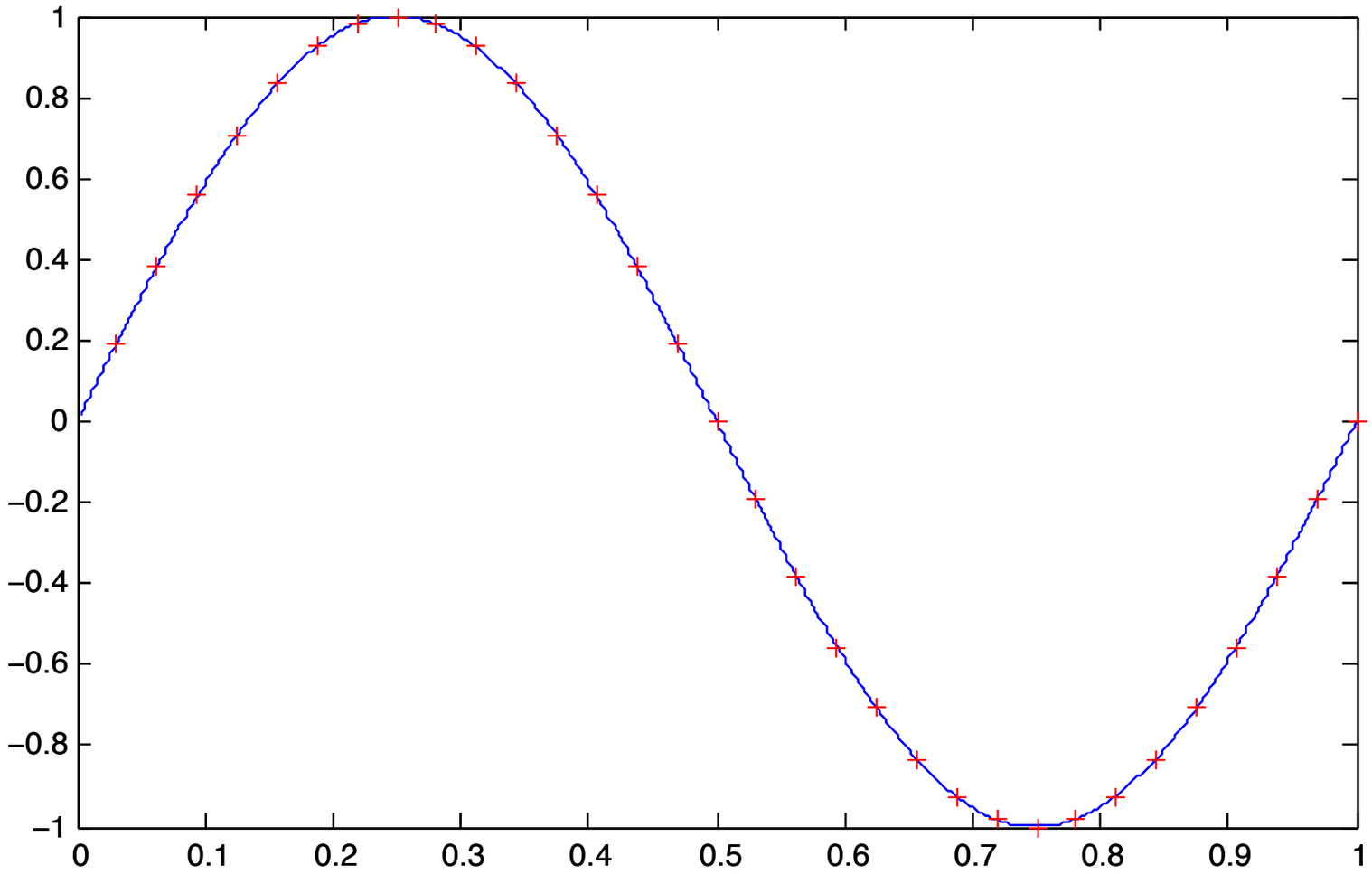
- Implementation insight helps understand limitations
  - True for all technologies, not only electronic circuits!
  - Switched-capacitor circuits and dual-rail signalling are ubiquitous in integrated filters
    - … and in ADCs, DACs
    - Learn to recognize some simple forms

Outline

- Basic switched-capacitor (SC) circuits
  - Some sources of performance limitations
  - A few examples
- Dual-rail signalling: benefits + drawbacks

Discrete-time signals

Recap slide

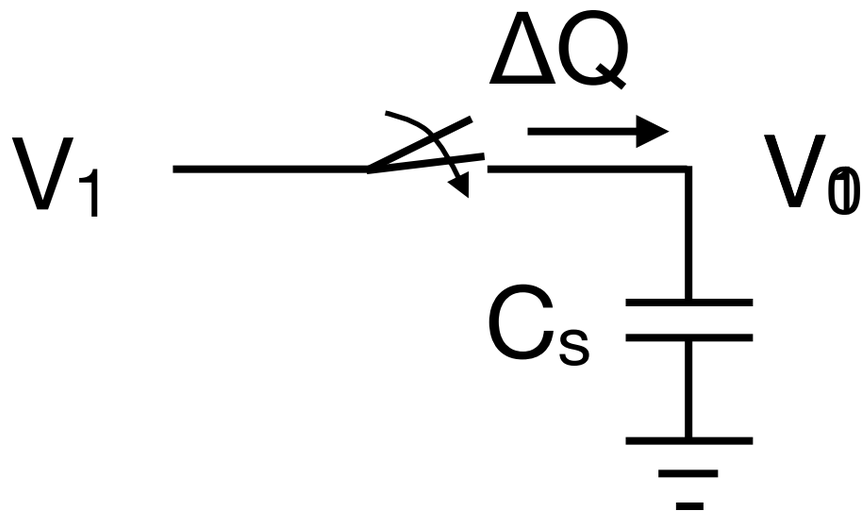


$f_s = 32$

$y = \sin(2\pi \cdot t),\ 0 < t \leq 1$

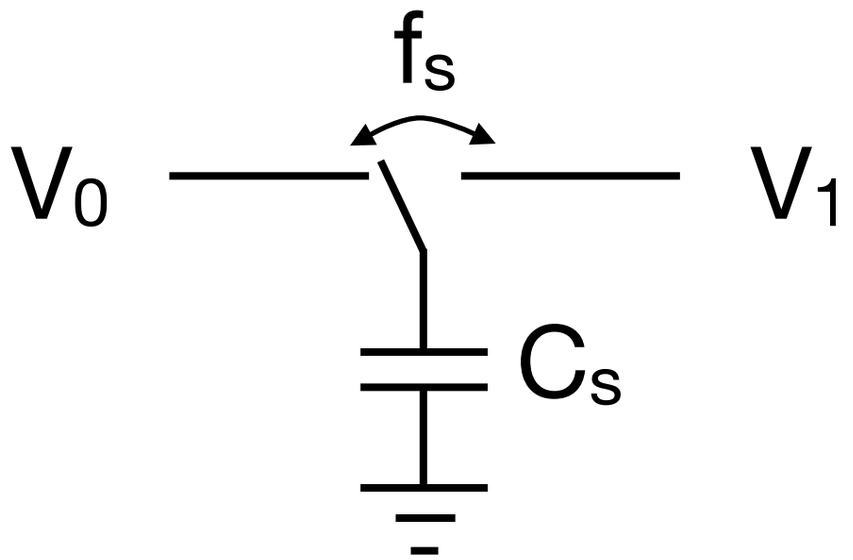
$y = \sin(2\pi \cdot t_k),\ t_k = (k / f_s)$

A switched capacitor



$$\Delta Q = (V_1 - V_0)\, C_s$$

“Resistor”



- $\Delta Q = (V_0 - V_1) \cdot C_s$
- $I = \Delta Q \cdot f_s = (V_0 - V_1) \cdot f_s C_s$
- … so, a “resistor” from V_0 to V_1; $R = 1 / f_s C_s$
- Note: R controlled by f_s !

HISTORY

If the condenser is now removed, and a resistance coil substituted for it, and adjusted till the steady current through the galvanometer produces the same deflexion as the succession of discharges, and if R is the resistance of the whole circuit when this is the case,

$$\frac{E}{R} = \frac{2EC}{T}; \qquad (1)$$

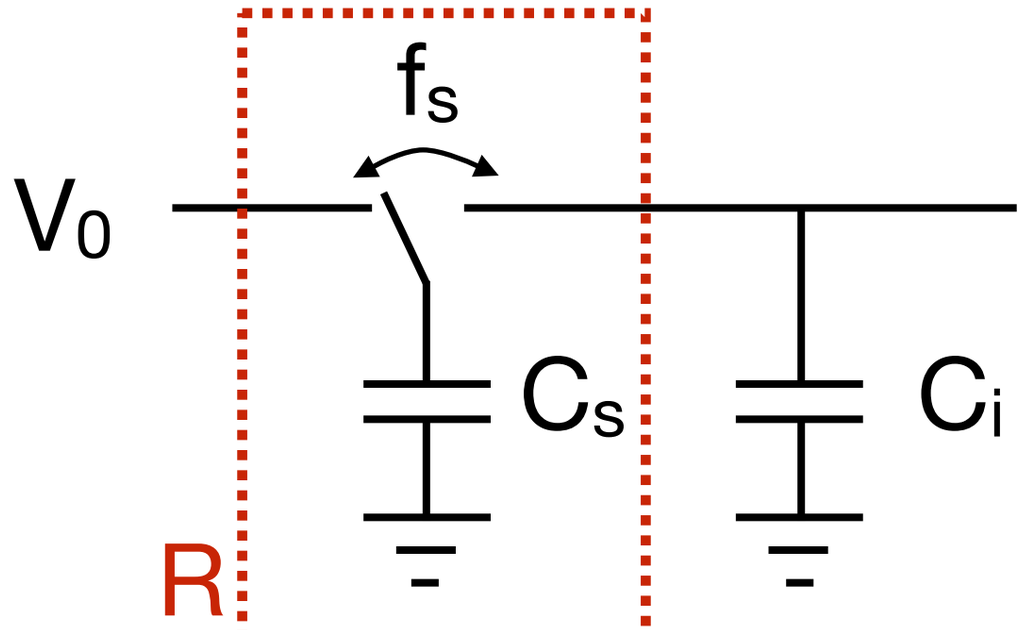
or

$$R = \frac{T}{2C}. \qquad (2)$$

[James Clerk Maxwell. A Treatise on Electricity and Magnetism. 1873.]

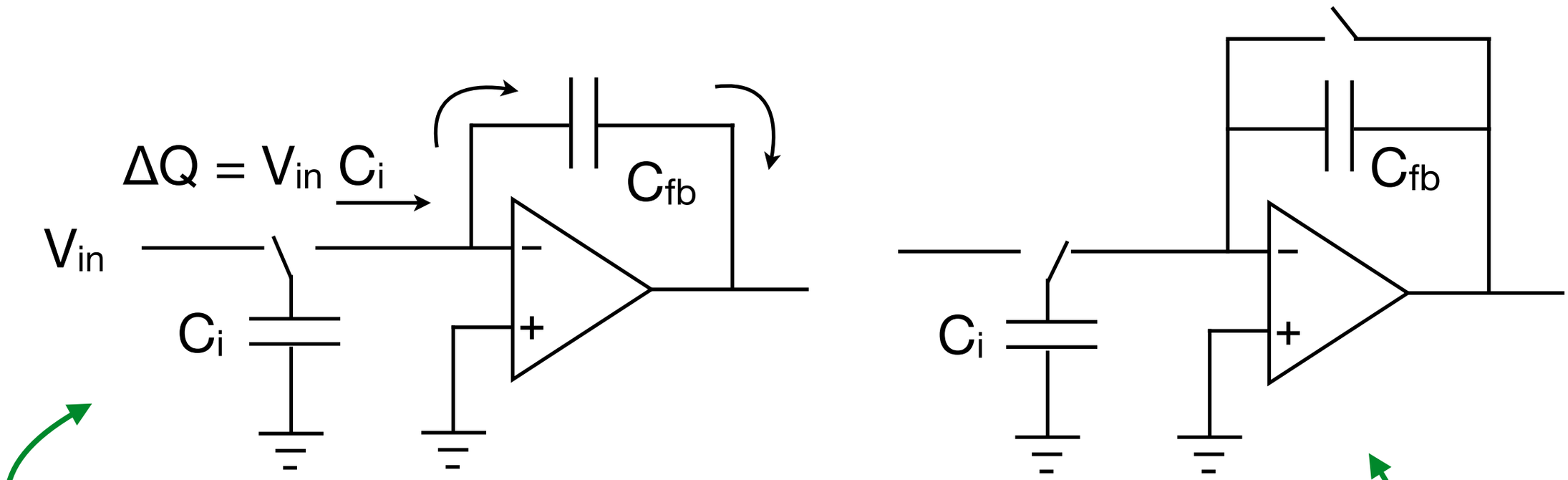
IC applications came later.

Simple low-pass link



- Time constant given by $R \cdot C_i = C_i / (f_s \cdot C_s)$
- Depends on
  - capacitance ratio (accurate)
  - frequency (accurate and controllable)

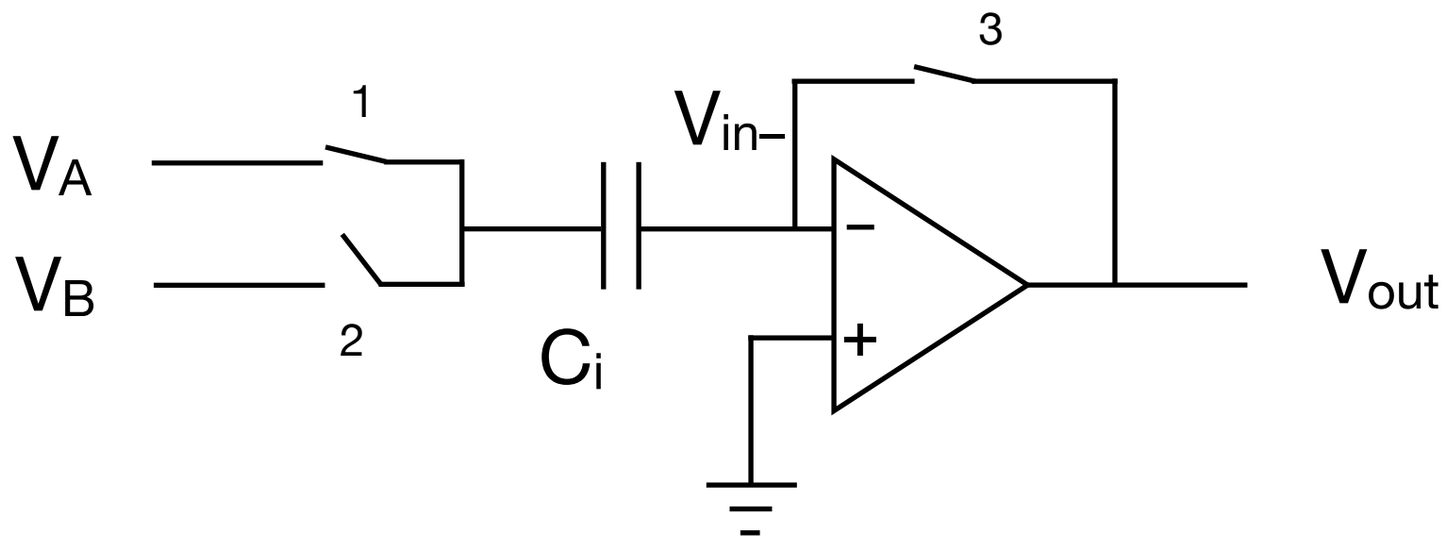
Opamp circuits



- Integrator: $V_{out} = -(C_i / C_{fb}) \cdot \int V_{in}\, dt$
- Inverting amplifier
  - Reset integrator after each cycle!
  - Gain: $-C_i / C_{fb}$

Cf. resistor-based circuit:
gain: $-R_{fb} / R_i$

Comparator

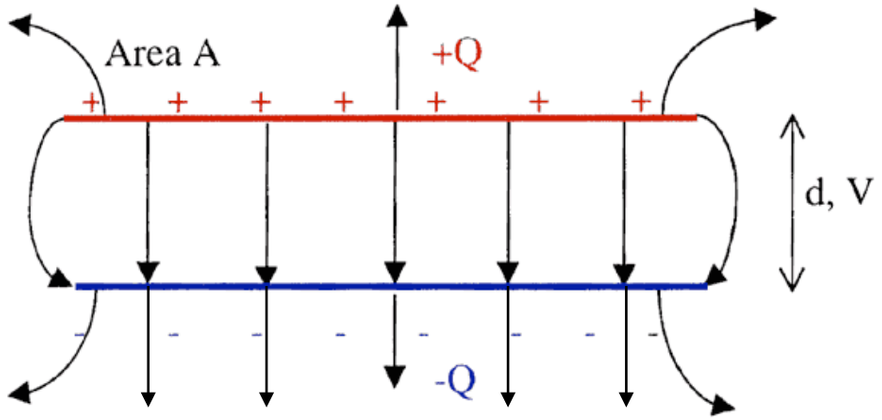


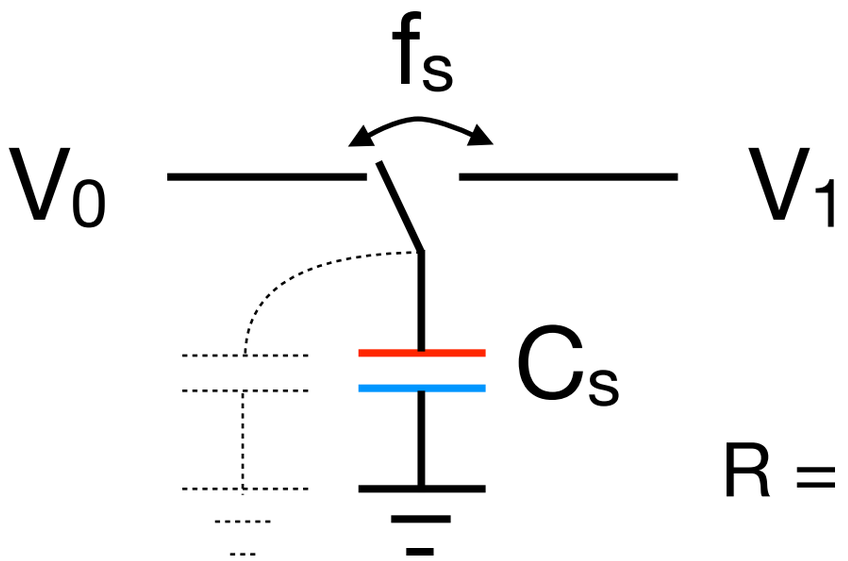
- Phase 1: switches 1 and 3 closed, switch 2 open
  - V_{out}, V_{in-} close to 0
  - ~ V_A across C_i
- Phase 2: switches 1 and 3 open, switch 2 closed
  - Still ~ V_A across C_i
  - $V_{in-} \approx V_B - V_A$
  - V_{out} swings to maximum or minimum voltage

Non-idealities

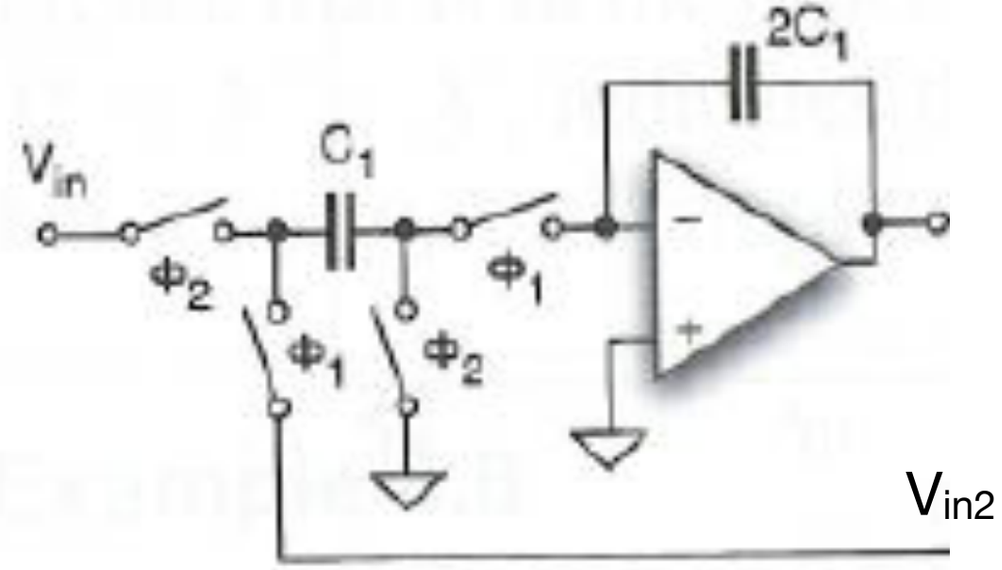
- Significant sources of deviations from ideal behavior:
  - Stray capacitances
  - Charge injection
  - Offset voltages
  - Limited gain
  - Settling time

Stray caps





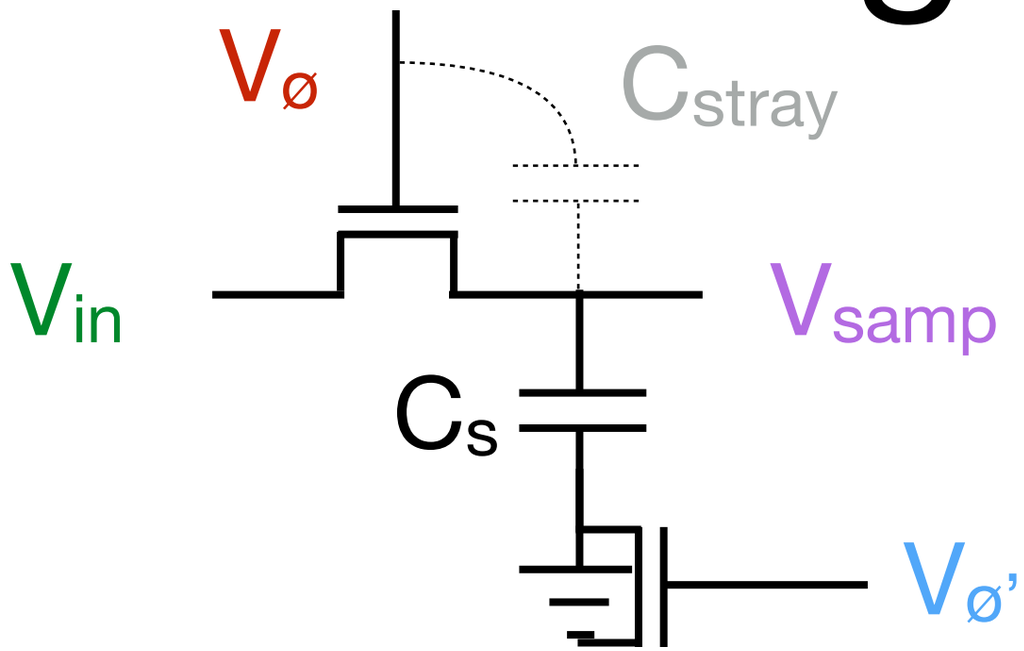
$$R = 1 / (f_s C_s)$$

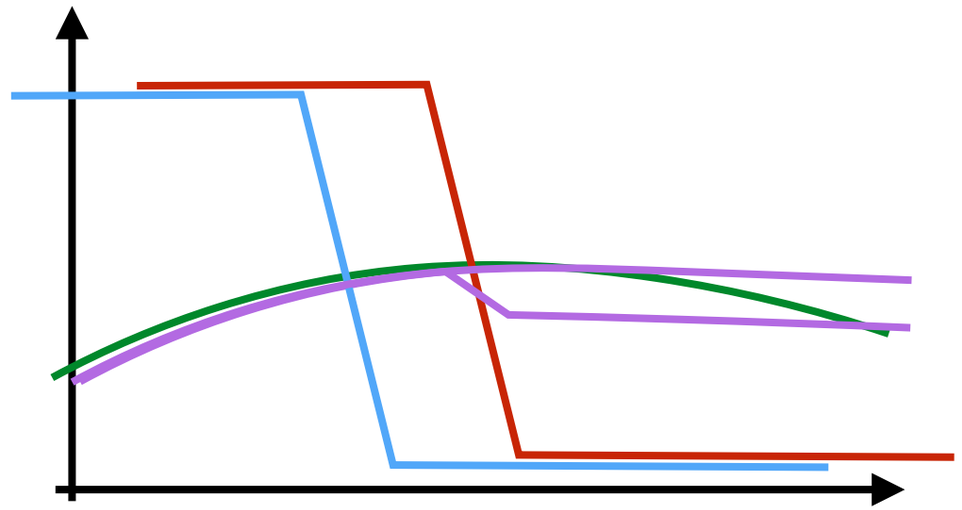


[Maloberti, fig 6.28]

- Integrated capacitors suffer from stray capacitances
  - Asymmetrical (most from bottom plate)
- Simple SC R still sensitive to top-plate stray capacitances!
- Standard circuit solution exists
  - Bonus: switch control allows “free” signal inversion

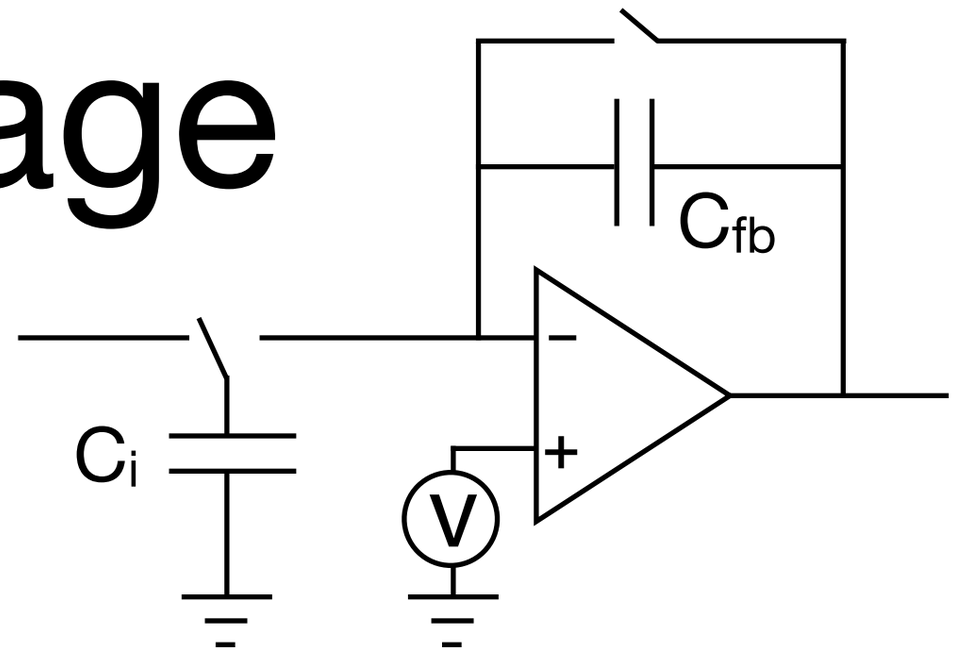
Charge injection





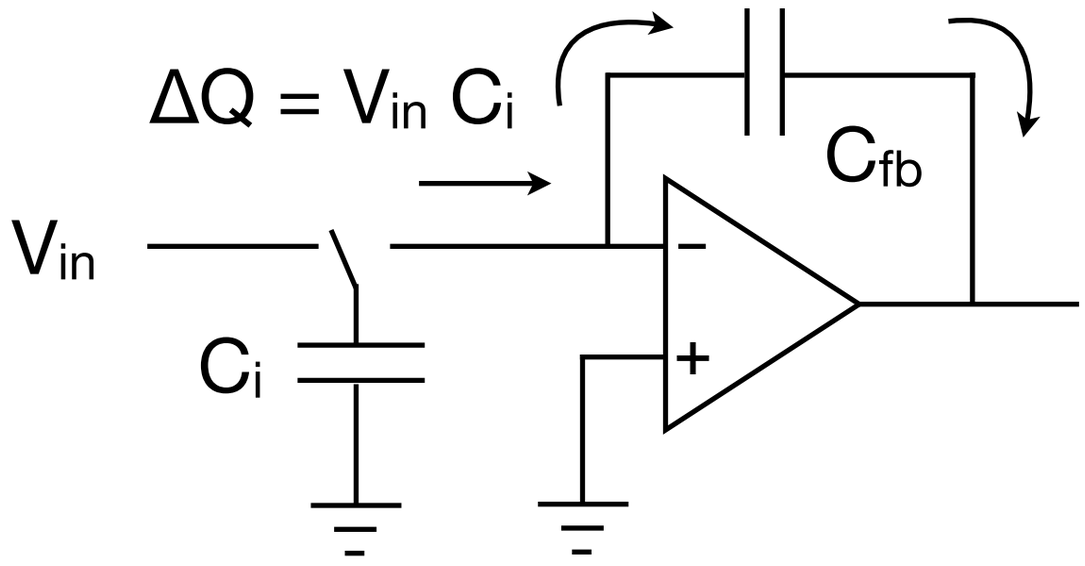
- Non-linear C_{stray} couples edge from $V_{ø}$ to V_{samp}
  - Non-linear → step depends on V_{samp}: distortion!
- Introduce <u>bottom-plate sampling</u>
  - Isolate charge on C_S with $V_{ø'}$ (no voltage dependence); <u>then</u> disconnect from V_{in} with $V_{ø}$

Offset voltage



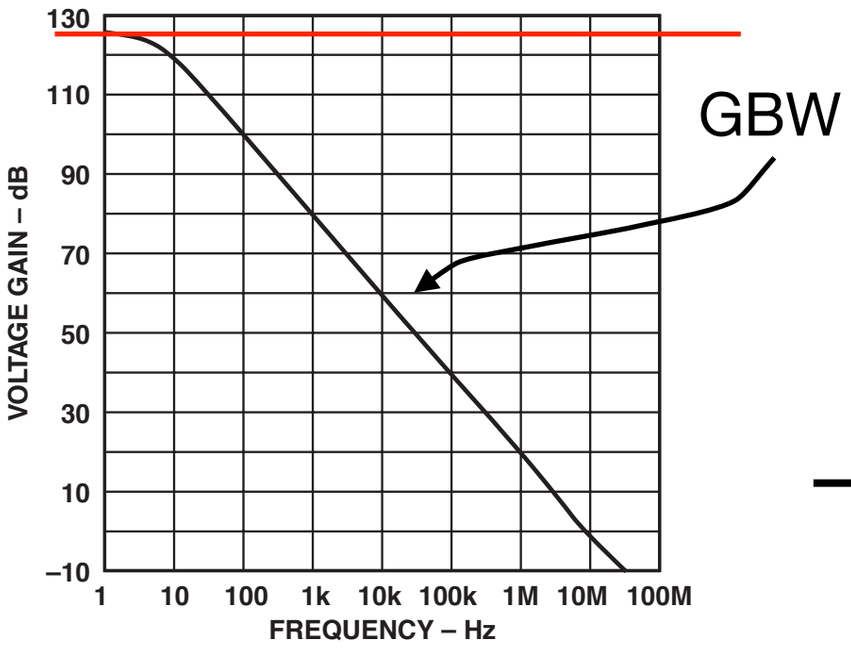
- Offset: voltage difference <u>at inputs</u> for $V_{out} = 0$
  - Conventionally <u>represented as</u> voltage source in series with positive input
  - Small value (ideally =0), but worse with increasing circuit variations (theme 2!)
- Reset phase sets output, negative input to ≈ V_{off} !
  - O/w, V_{off} would be amplified at output…

Limited gain

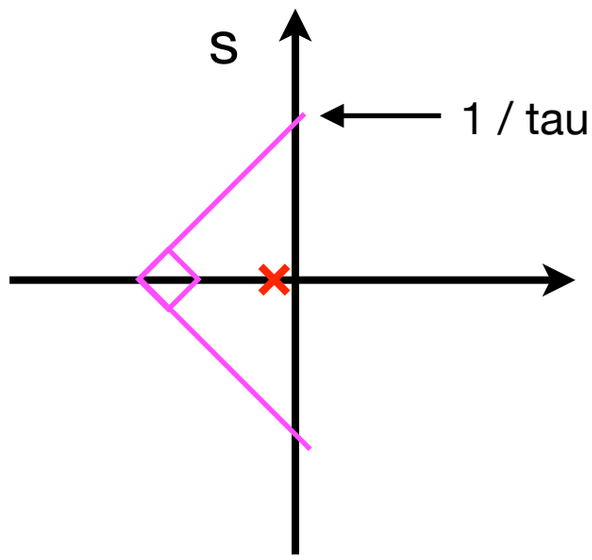


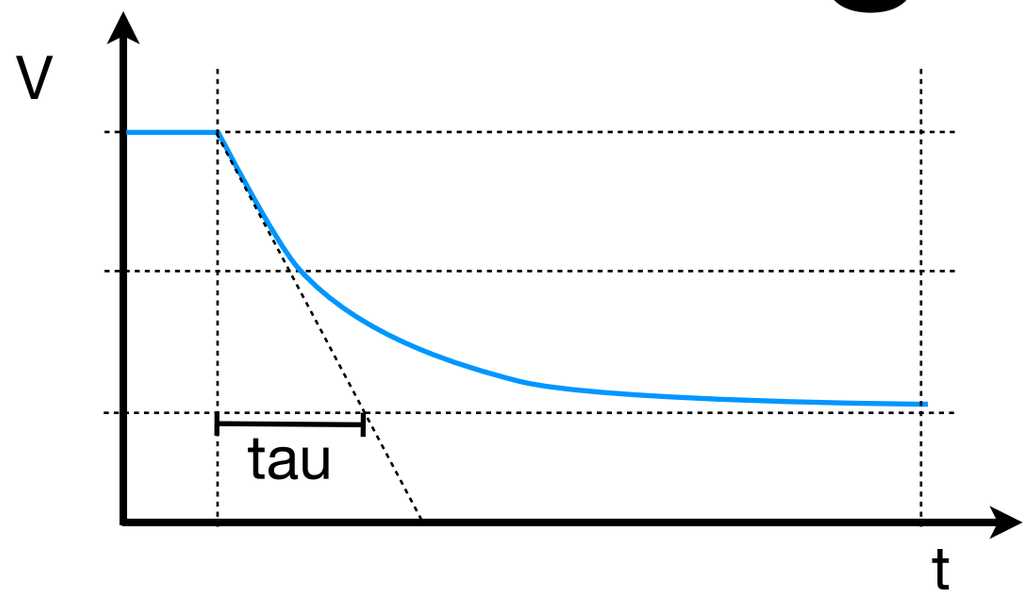
- Negative input not pulled all the way to ground
  - Charge transfer incomplete
- Output settles to “wrong” value
  - Worse with lower gain
- Compare with CT case: discrepancy D = Aß / (1 + Aß)

Linear settling



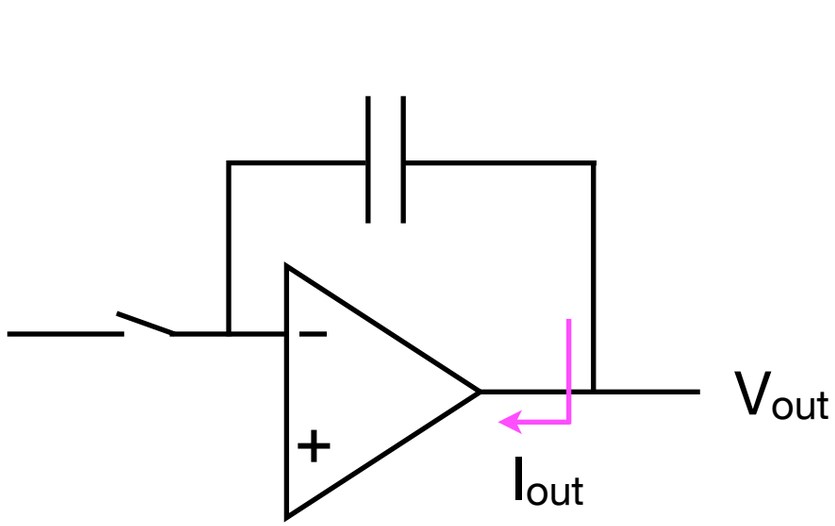
TPC 16. Open-Loop Gain vs. Frequency

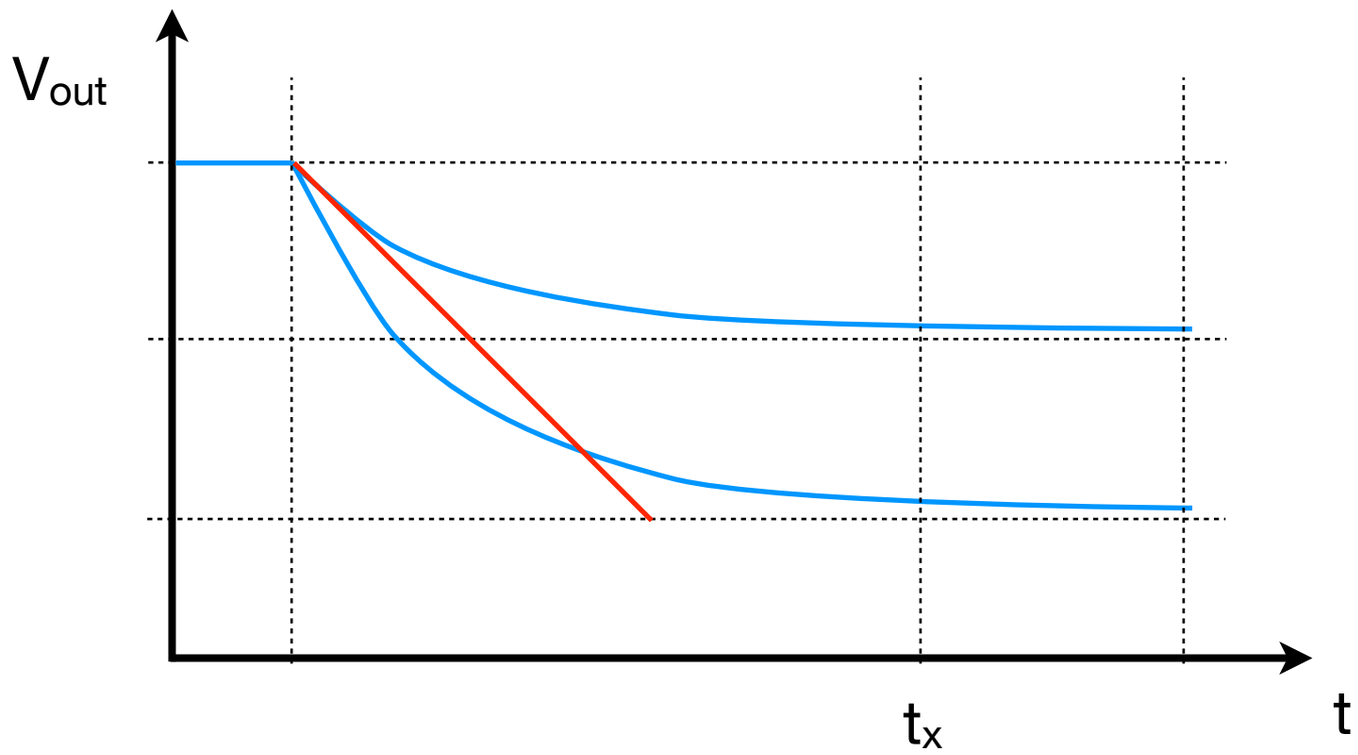




- OP-amp with one dominant pole is <u>first-order system</u>
  - Step response is a damped exponential
- Feedback moves pole!
- Time constant tau determines settling speed
  - 3 · tau to 95%; 5 · tau to 99%; 9 · tau to 99.9%; etc
  - Select GBW for desired accuracy (tradeoff: $, W)

Nonlinear settling (slewing)





- Ideally, settling error shrinks exponentially with time
  - Remaining final error (%) at time t_x depends only on amplifier gain and on time spent vs pole position
- If limited max current I_{out}, error also depends on level
  - Worse at high amplitudes! Non-linear! Distortion!

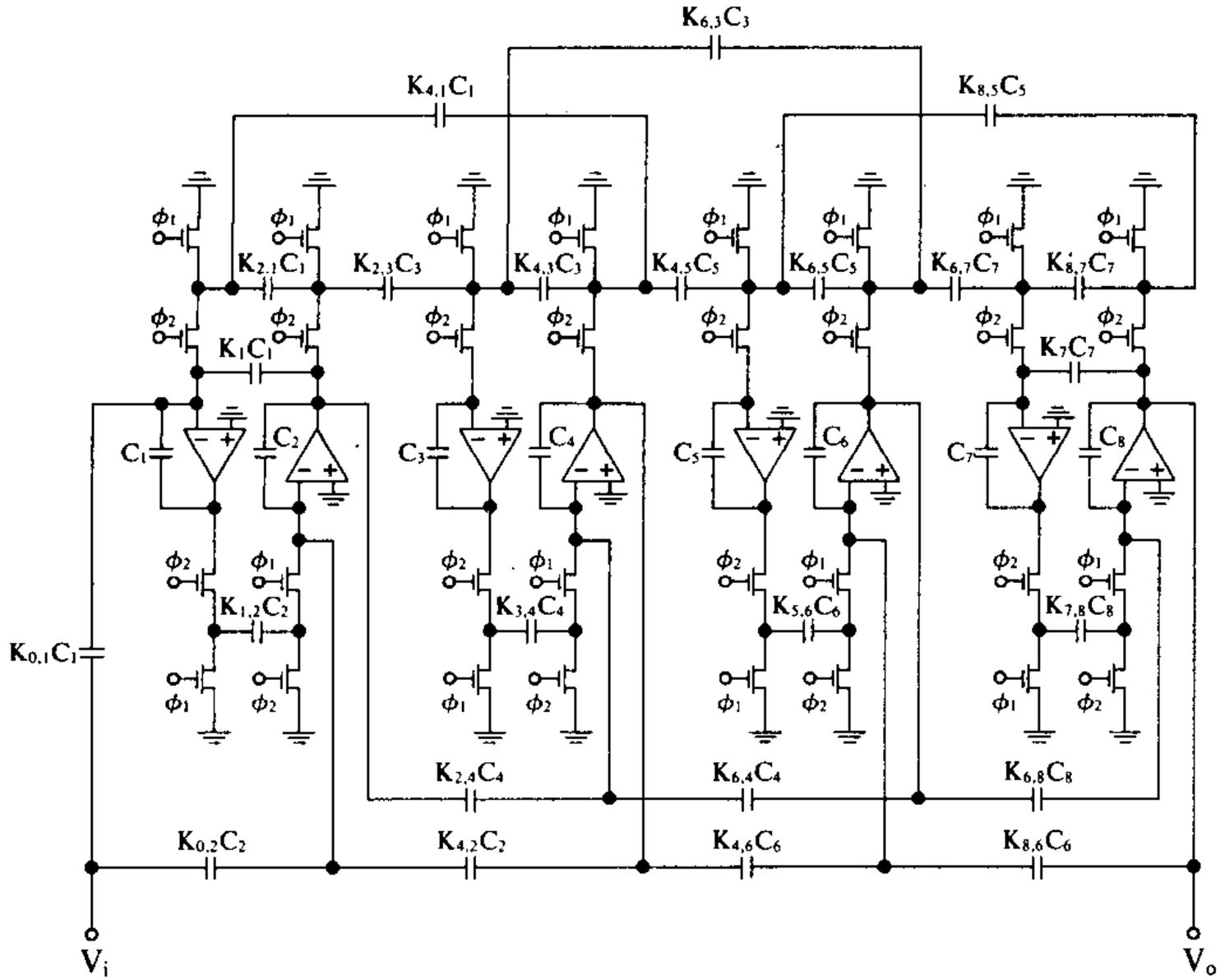
How size capacitances?

- Small C brings high speed
- Small C brings low power
- Small C brings matching problems
  - Best matching for small-integer ratios (2, 3, 4, 5, etc)
  - Does not fit Butterworth etc. poles :-(
- Small C brings fundamental noise problems
  - Noise power: kT / C

SC drawbacks

- Sampling brings aliasing problems
  - Will need CT anti-alias pre-sampling filter
  - Need a GBW ~5x the clock frequency, so 10x highest signal frequency
    - Worse than BW margin for continuous-time implementations
    - High GBW costs power!

Example: SC ladder filter



- CT filter design styles re-usable in DT!

[Martin, Sedra; IEEE Trans on CAS, June 1980]

Performance example

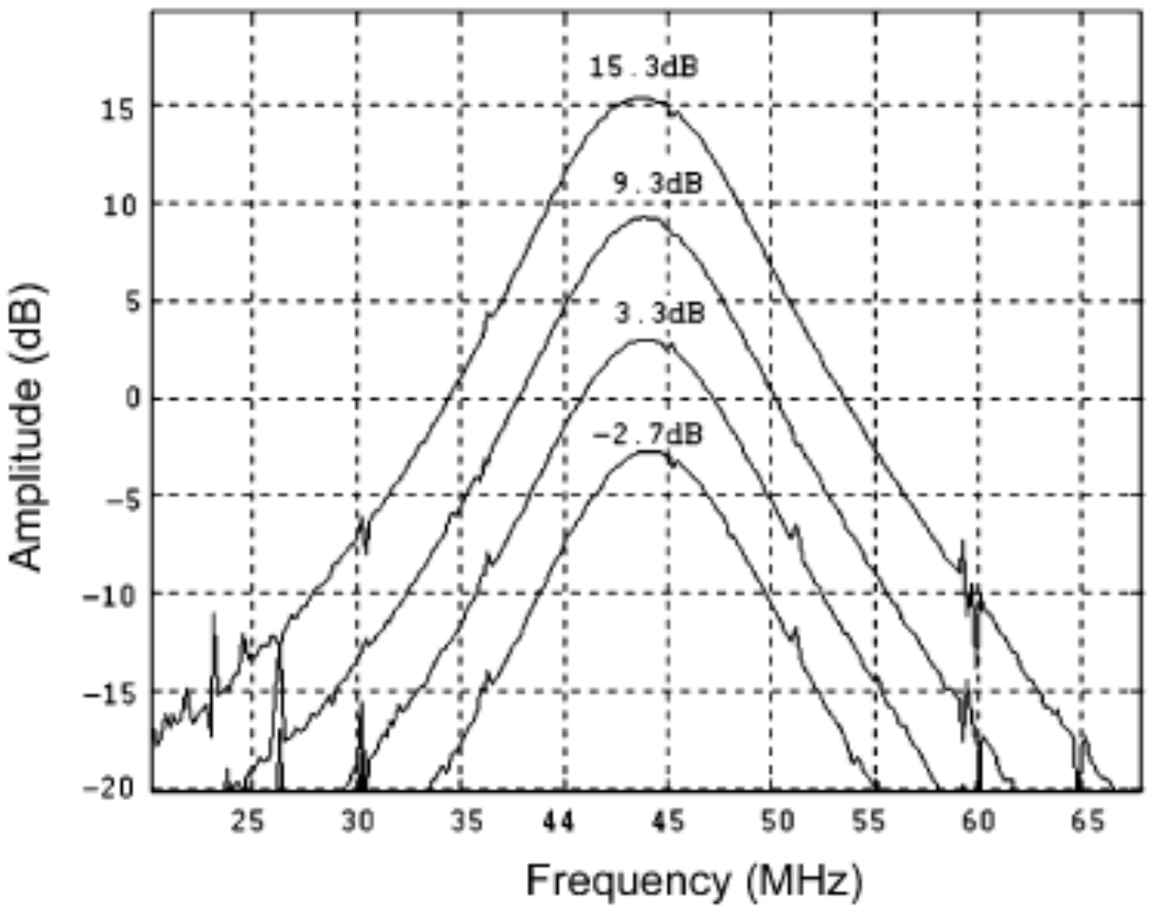


TABLE I
SUMMARY OF THE MEASURED RESULTS OF THE OPAMP

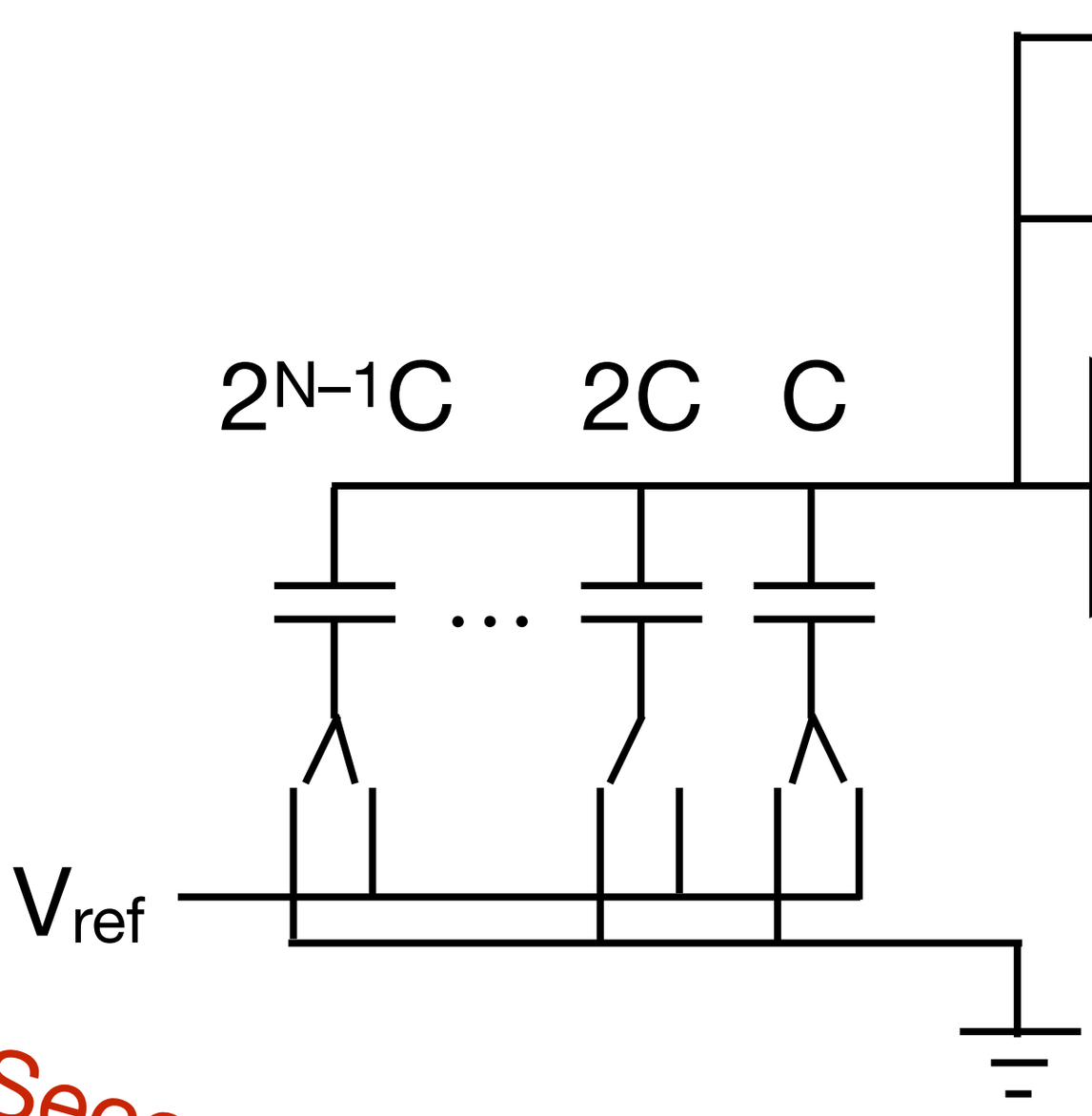
Parameters	Results
Technology	0.35μm CMOS
Supply Voltage	3V
Low-Frequency Gain	56 dB
Unity-Gain Frequency	600 MHz
Phase Margin	50°
Power Consumption	30.8 mW
Single-Ended Output Swing	0.9 V_{PP}
0.1% Settling Time @ 1.5pF	<5ns

Parameters	This design	J. Silva-Martinez [12]	R. F. Neves [13]
Technology	0.35-um CMOS	0.35-um CMOS	0.8-um CMOS
Supply voltage	3V	3V	5V
Power consumption	92.7 mW	54mW	125mW
Sampling frequency	176MHz	68MHz	100MHz
No. of Clock phases	3	4	42
Orders of filter	6	6	N/A
Q	7	32	7.5
Center frequency	44MHz	10.7MHz	37.5MHz
Vin @ IM3 = 3%	0.893Vp-p		N/A
Total output noise	383.0 μVrms	N/A	N/A
Dynamic range (3% IM3)	58.3 dB	58 dB (SNR)	34dB SNDR with Vout = 0dBm
Active area	0.52mm^2	0.84mm^2	7.27mm^2

- 6-order filter, 176 MHz clock, < 100 mW, 0.35um CMOS

[Ng et al, IEEE Journal of Solid-State Circuits, March 2005]

Other SC circuits: DAC



Second example later

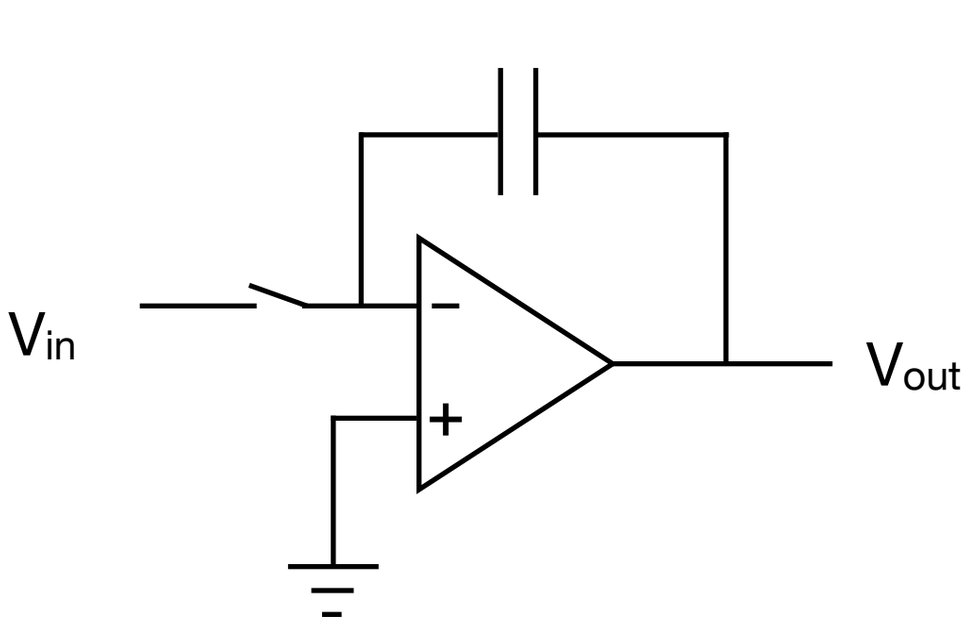
- 2 clock phases
- Offset cancellation
- Good for ~7 bits (cap ratios)
- Similar to R-based DAC!

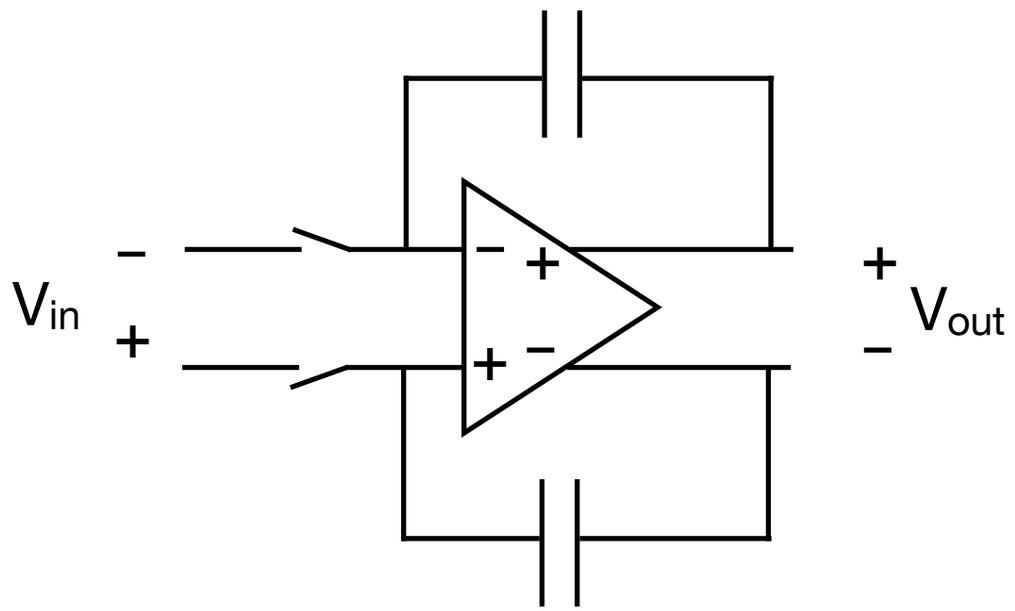
Dual-rail signalling

Dual-rail signalling

- Almost universal in on-chip analog circuits
- Not only in DT filters
  - CT filters from theme 4!
- Increased complexity
  - Benefits outweigh costs
- Often ignored for simpler drawings :-/

What?





- Signals maintained as voltage <u>differences</u>
- Symmetrical circuits

Dual-rail + and –

1. Twice the swing
2. Improved SNR
3. Common-mode coupled noise eliminated
4. Even-order harmonics cancel out

1. Twice the hardware
2. Twice the power
3. Relies on symmetry
4. CMFB circuitry needed

1. Twice the swing

- If single-rail swing from –1 to +1, then dual-rail swing is from (–1) – (+1) = –2 to (+1) – (–1) = 2
- Important at low supply voltages in modern processes

2. Improved SNR

- Signal voltage amplitude doubled
  - Signal power up by 4x (6dB)
- Uncorrelated random noise at both rails adds as powers
  - Noise power up by 2x (3dB)
- 3dB SNR improvement!

3. Coupled-noise reduction

- Externally-generated noise (from supplies, substrate, capacitive coupling) tends to be highly correlated
  - If identical (ideal case), does not affect output at all!
- Even better SNR improvement

4. Harmonic reduction

- Even-order nonlinearities are cancelled

- Consider DR circuit with slight nonlinearity *h*
  - Inputs: $x_+ = a \sin(wt)$; $x_- = -a \sin(wt)$
  - Outputs: $y_+ = h(a \sin(wt))$; $y_- = h(-a \sin(wt))$

  - Taylor expansion: $h(x) = h_0 + h_1 x + h_2 x^2 + \ldots$
  - But $x^{2n} = (-x)^{2n}$, so no even harmonics in $(y_+ - y_-)$

1. Twice the hardware

- Twice as many capacitors
- Twice as many switches
- Twice as many wires
- …

- Affordable with present-day miniaturization

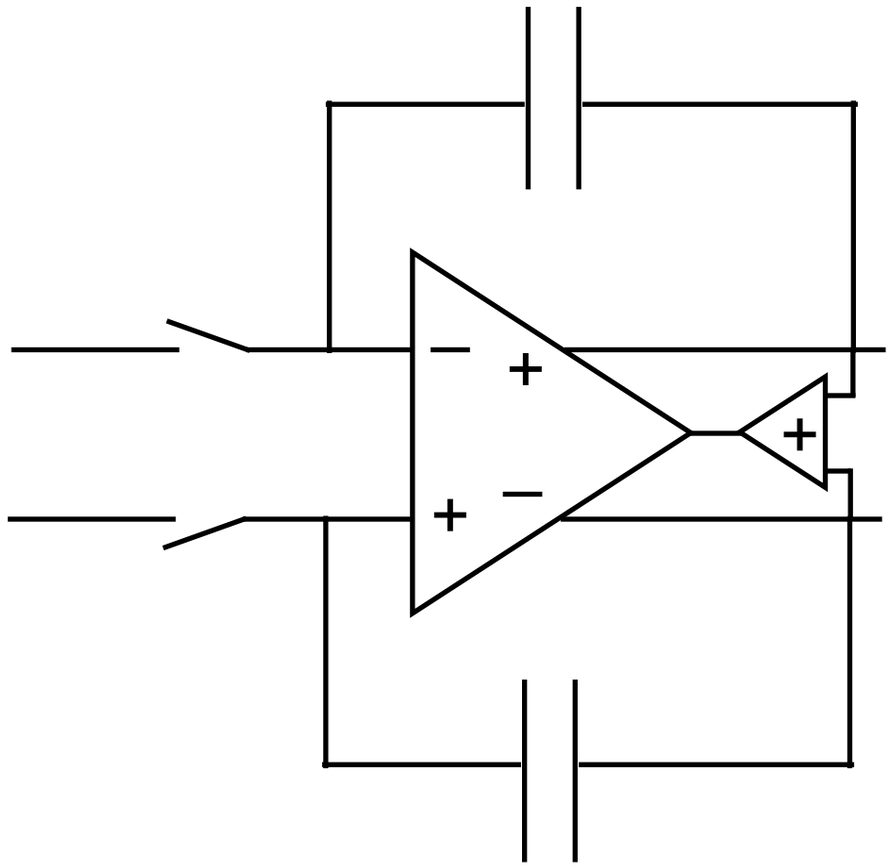
2. Twice the power

- Twice the capacitive load driven to the same swing as before
- Twice the number of switches to control
- May be traded for the 3dB SNR improvement…

3. Relies on symmetry

- Benefits assume that all paths are symmetrical!
  - Example: harmonics won't cancel perfectly if one capacitive load is larger!
- Symmetry is never perfect
  - Layouts
  - Variability

4. CMFB circuits needed

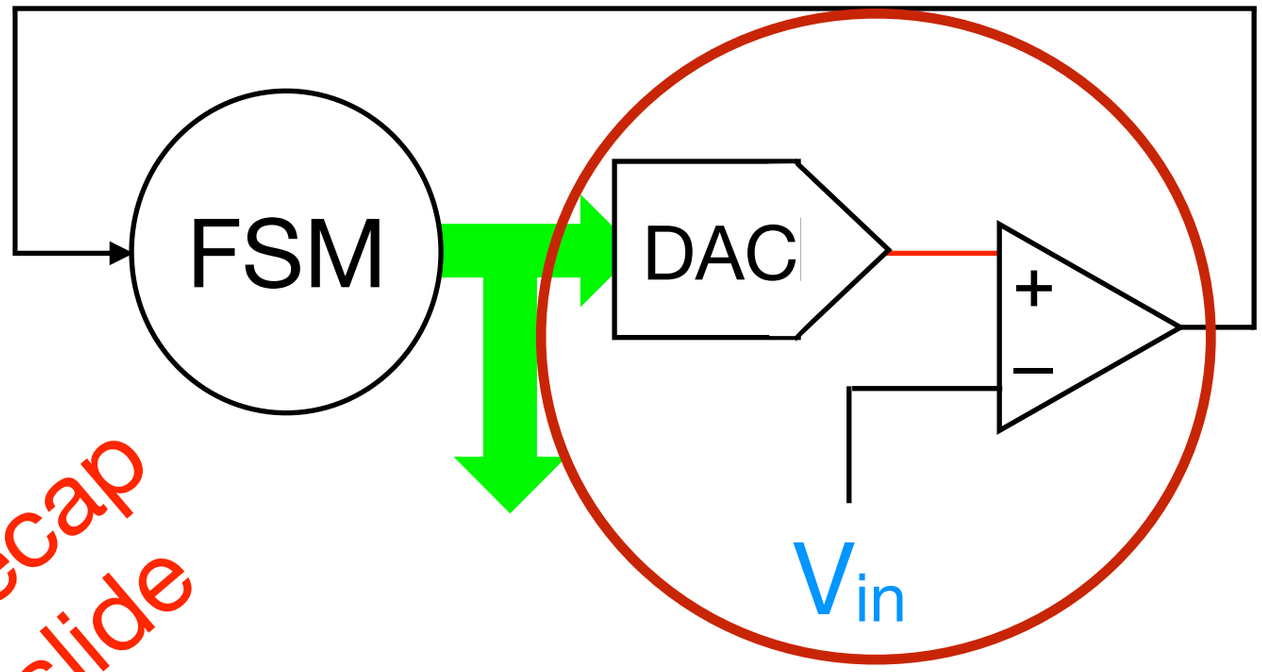


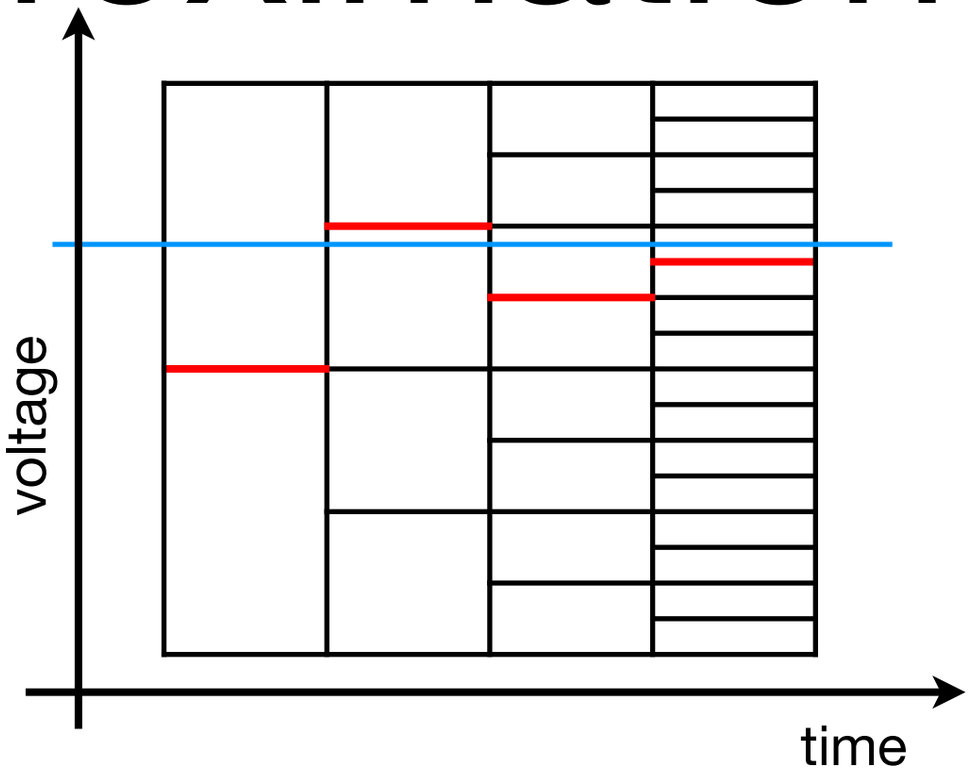
Non-standard schematic symbol

- Common-mode feedback circuits needed to control <u>average</u> output voltages
  - Extra input (here) or added to both DM inputs
- Extra feedback loop! Stability issue!

Two combined examples

Successive approximation





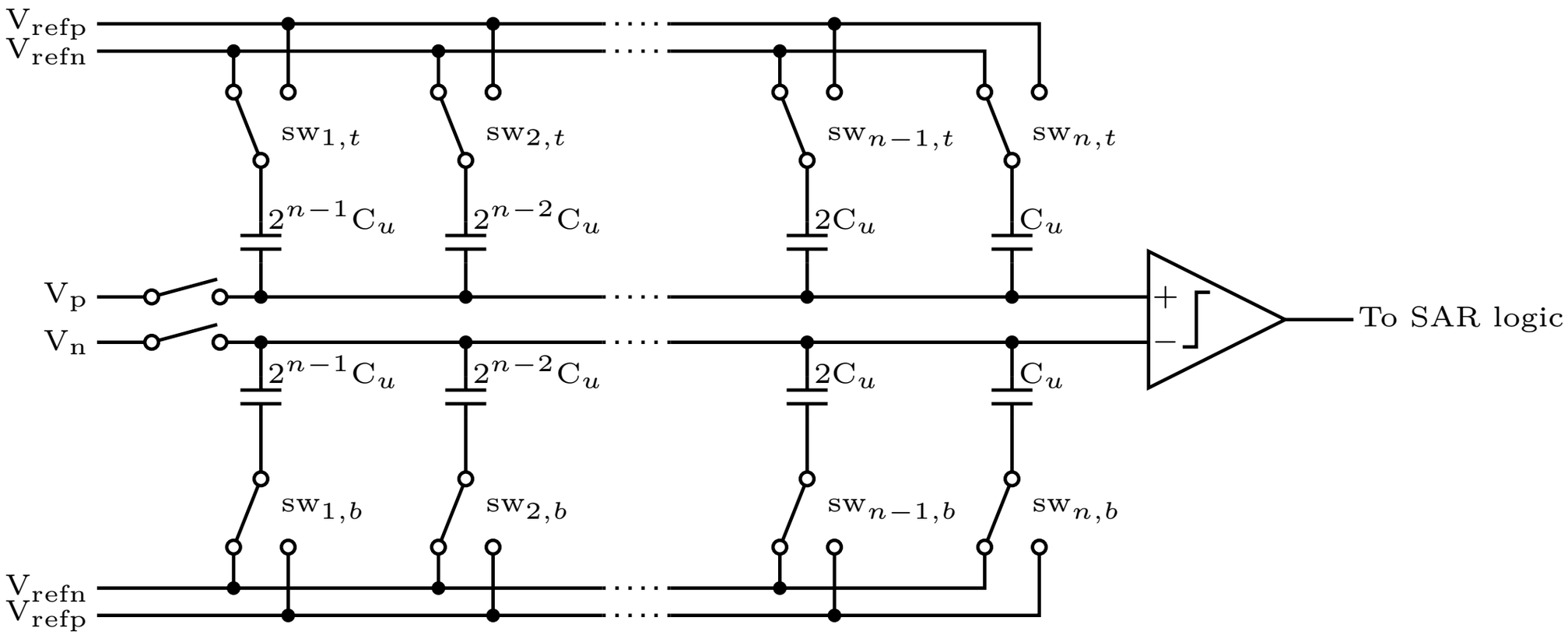
Recap slide

- Simple Finite State Machine sets bits in sequence from MSB downwards, depending on previous decisions
  - Search by interval halving / bisection
- One full conversion in N cycles

\+ No subtractions or other analog processing

– DAC needs to be good to N bits!

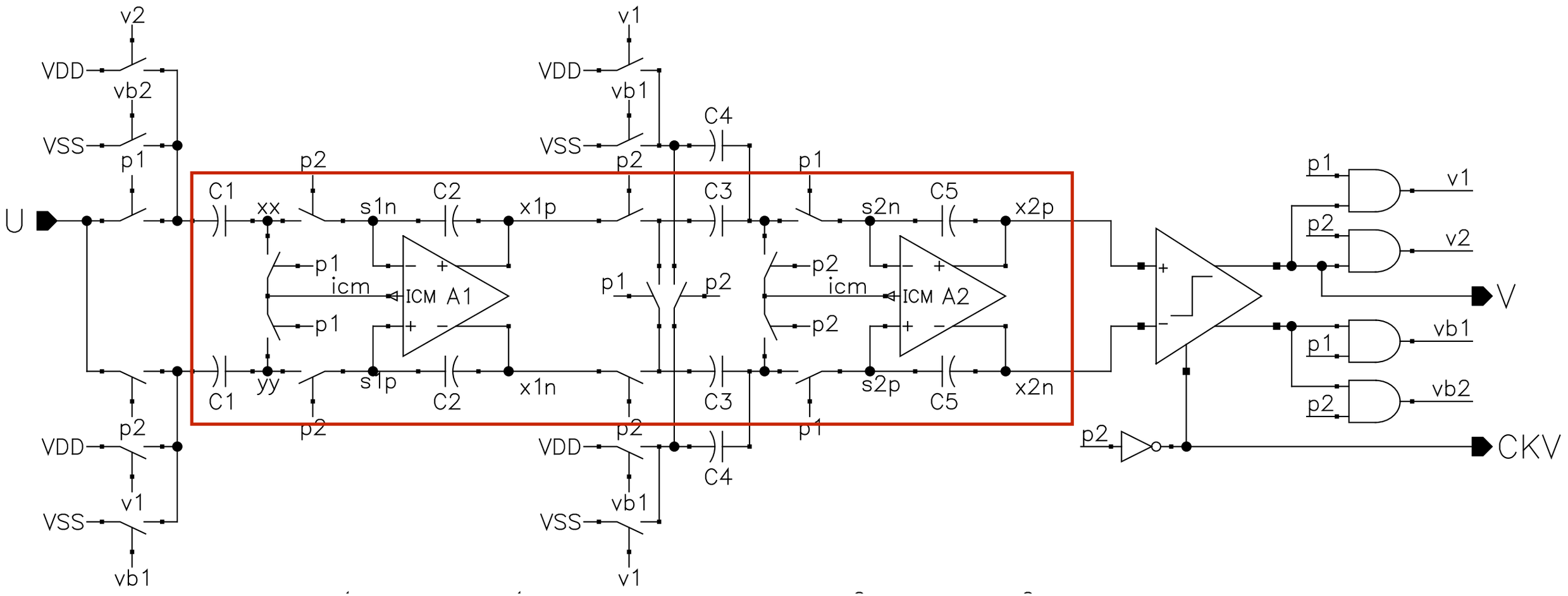
DAC + comparator



- DAC capacitors also work as ADC sample cap!
- Capture value on caps, then switch back plates to zero out difference by binary scaling
- Principle used for lowest-FoM ADCs today!
  - Also for high speed (next week!)

[Victor Åberg]

Forward-looking example



- Two-integrator filter
- Part of Sigma-Delta ADC (also next week!)

[Pavan, Schreier, Temes: Understanding Delta-Sigma Data Converters, 2017]

Summary

- SC circuits allow high-performance analog circuits on silicon
  - Good accuracy
  - Controllability
- Dual-rail signalling ubiquitous in on-chip analog and mixed-signal circuits
  - May be used even if not shown in schematics!